UNIVERSITÀ DEGLI STUDI DI PAVIA

DIPARTIMENTO DI ELETTRONICA

DOTTORATO DI RICERCA
IN MICROELETTRONICA
XXII CICLO

DC-DC CONVERTERS AND LOW-NOISE AMPLIFIER FOR PORTABLE APPLICATIONS

Relatore:
Chiar.mo Prof. Franco Maloberti

Coordinatore del Corso di Dottorato:
Chiar.mo Prof. Rinaldo Castello

Tesi di Dottorato
di Massimiliano Belloni

ANNO ACCADEMICO 2009 - 2010

INDEX

INTRODUCTION

Nowadays almost every portable electronic product uses components that are designed to operate from a constant voltage source provided by the battery. Since the source voltages achieved from the batteries may not necessarily match the component supply-voltage rating, or may vary considerably around the nominal specifications, DC-DC converters or regulators are required. Portable applications demand regulators with high power efficiency (defined as the ratio between input and output power) together with small area and low height profile to reduce the overall cost.

The aim of this research is to provide innovative solutions that achieve cost reduction while preserving high power efficiency.

Several options exist in order to generate a constant supply voltage from a variable DC power supply and the chosen one depends on different system requirements (such as the load current level, load current and input voltage variation response, noise tolerance and the physical size of the solution). DC regulators can be basically classified in linear and switching regulators, as discussed in detail in Chapter 1.

In the case of a linear regulator, the supply power is transferred continuously from the input supply to the output load. Typically, the linear regulator offers small physical size and low noise operation. However, the higher the difference between input and output voltages, worse the linear regulator efficiency. Furthermore, the linear regulator is able to provide only output voltages lower than the input voltage source.

In the case of a switching regulator, the supply power is transferred from the input to the output in burst. This makes the switching regulator more efficient, but at the expense of adding switching noise to the system and requiring additional off-chip components such as inductors, capacitors and MOSFETs.

Charge pump switching regulators are used typically when area and cost are more important than power efficiency and a higher output voltage ripple can be tolerated.

They provide a flatter profile than inductive solutions since the capacitors are usually smaller than the inductors. On the other hand, when power efficiency is the most important parameter, as for many battery operated applications, the inductive switching regulator is often the best solution. However, the price to pay is a significantly increased PCB area mainly due to the off-chip inductor.

The inductor cost in terms of area can be appreciated in Figure I that shows an evaluation board for a commercial DC-DC regulator (National Semiconductor LM3100 step-down converter). IC, Inductor, input and output capacitors footprints have been highlighted.

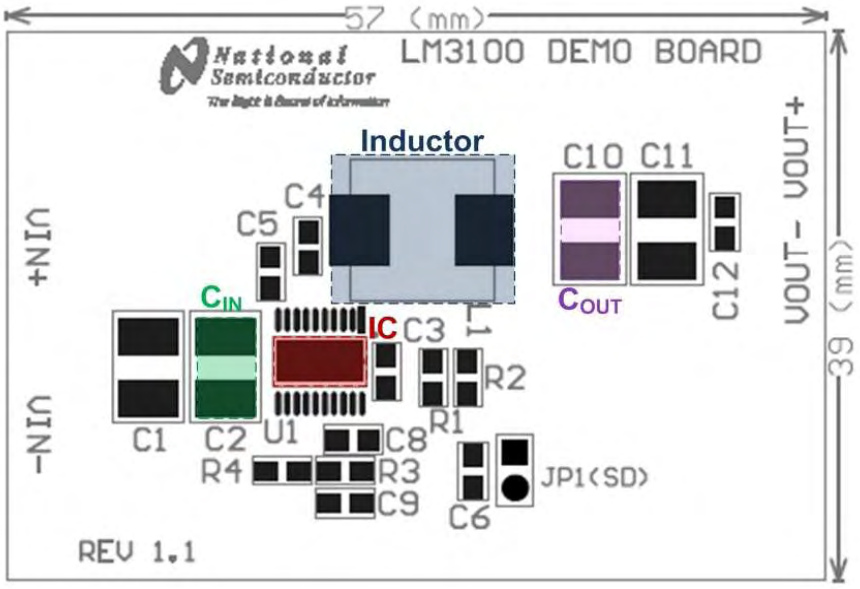

Fig. I: National Semiconductor LM3100 step-down converter evaluation board.

In order to decrease the inductor cost, two basic approaches can be followed:

1) Design systems that provide many outputs using only one inductor.
2) Design systems that use a smaller inductor and that eventually allow System-in-Package integration.

The first approach has lead to the single-inductor 4-output DC-DC buck converter research activity, reported in Chapter 2. This was the first 4-output buck converter IC reported in the literature.

The second strategy has lead to the design of a high switching frequency, 60MHz, DC-DC buck converter, reported in Chapter 3.

Even if some works, with a higher switching frequency, are present in the literature, their performance in terms of power efficiency, output voltage ripple and line and load regulations are not so good. On the other hand, the designed IC has shown significant improvements respect the state of the art.

In order to preserve the system power efficiency even for small output currents, light load modes (such as Pulse-Frequency-Modulation or Discontinuous-Conduction-Mode) need to be activated sensing the current flowing in the power train of the DC regulator. For this purpose, a low-noise amplifier has to be used.

The low noise and input offset research activity is the subject of Chapter 4 and has led to significantly improvements respect the state of the art especially for the input supply current/input noise trade-off issues.

Chapter 5 summarized the achieved performance in each research area, comparing each of them with the results reported in the literature.

CHAPTER 1

DC-DC CONVERTER FUNDAMENTALS

Nowadays almost every electronic product uses components that are designed to operate from a constant voltage source. These components may be digital, such as microprocessors and FPGAs, or analog, such as line drivers, amplifiers or PLLs. Both of them have different requirements in terms of supply voltage levels, supply voltage tolerances and current consumption levels.

Figure 1.1 shows an example of today electronic products requirements.

Since the source voltages from batteries or line transformers may not necessarily match the component supply voltage rating, or may vary considerably around the nominal specifications, DC-DC converters or regulators are required.

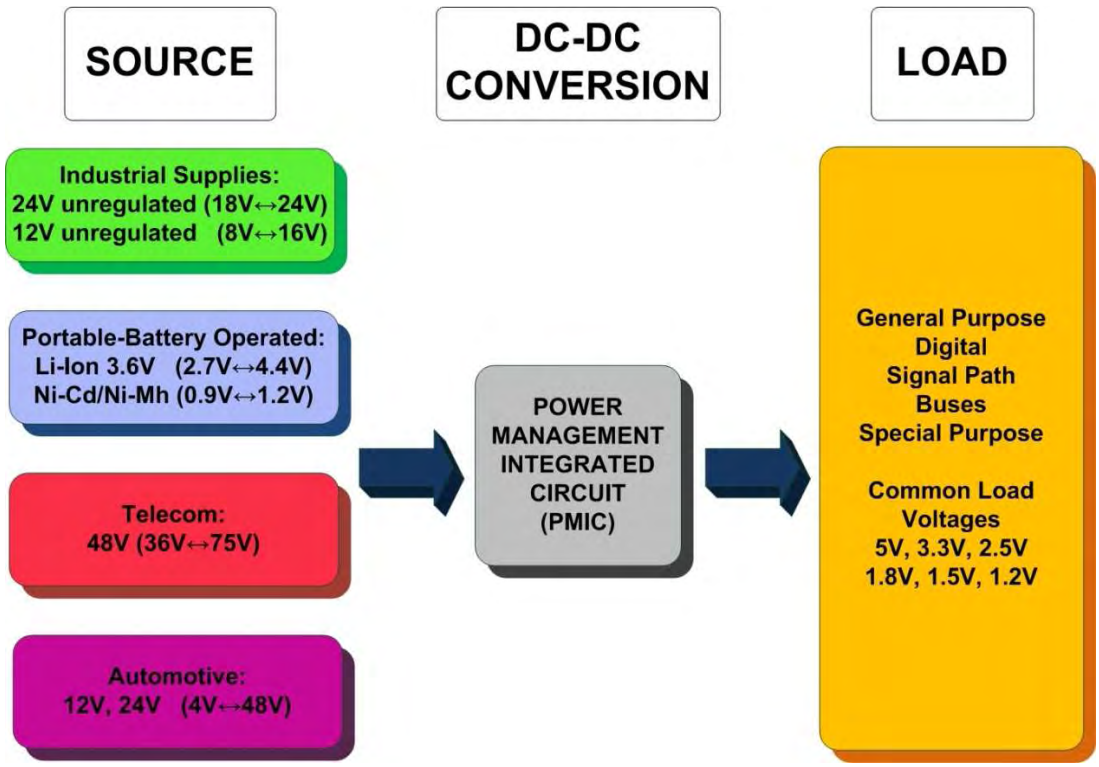

Fig. 1.1: Nowadays electronic products requirements examples.

A DC-DC regulator provides a constant DC output voltage and contains circuitry that steadily holds the output voltage at the designed value (which could be higher or lower than the input battery voltage) regardless of changes in load current or input supply voltage, assuming that the load current and input supply voltage are within the specified operating range for that regulator.

A feedback input is necessary for the regulator to know the state of the output voltage so that it can be kept within the tolerances required by the power supply design requirements. Therefore, the converters control the output voltage to the specifications by comparing the output voltage (or current or both) to an internal reference.

The ratio of output power P_{OUT} (output voltage V_{OUT} times output current I_{OUT}) to input power P_{SUPPLY} (input supply voltage V_{SUPPLY} times supply current I_{SUPPLY}) is called power efficiency, η, of the converter:

$$\eta = \frac{P_{OUT}}{P_{SUPPLY}} = \frac{V_{OUT} \cdot I_{OUT}}{V_{SUPPLY} \cdot I_{SUPPLY}} \tag{1.1}$$

The change over time of the output voltage and current as response to a change in the input supply voltage or load is called transient response. Specifically, the response to input supply change is called line regulation and the response to load change is referred to as load regulation. Ideal regulators have no change to the set output voltage.

Some regulators have a small ripple in the output voltage even at steady-state, when input voltage and output load are stable. This ripple is called steady-state output noise.

With regard to portable battery operated systems, the use of voltage regulators extends the lifetime of the system and avoids difficult wide power supply range circuit design. Regardless of the battery output voltage as it declines during discharge, the voltage regulator always provides the required output voltage.

1.1 DC-DC CONVERTERS OPTIONS

Several options exist in order to generate a constant supply voltage from a variable DC power supply. The chosen one depends on different system requirements such as load current level, load current and input voltage variation responses, noise tolerance and physical size of the solution.
As shown in Figure 1.2, there are two basic types of regulators:

- Linear regulators.
- Switching regulators.

In the case of a linear regulator the supply power is transferred continuously from the input supply to the output load. Typically, the linear regulator offers small physical size and low noise operation, but, on the other hand, it has low efficiency, since it is similar to a variable resistor that consumes a power from the source P_{SUPPLY} equal to the output load current times the difference between input and output voltage:

$$P_{IN,LINEAR} = I_{OUT} \cdot \left(V_{SUPPLY} - V_{OUT}\right) \tag{1.2}$$

Therefore, the higher the difference between input and output voltages, worse the linear regulator efficiency. Furthermore, the linear regulator is able to provide only output voltages lower than the input supply voltage.

In the case of a switching regulator, the supply power is transferred from the input to the output in burst. This makes the switching regulator more efficient, but at the expense of adding switching noise to the system and requiring additional external components as inductors, capacitors and MOSFETs.

Basically, there are two main types of switching regulators:

- Inductor based (inductive).
- Charge pump (capacitive or inductorless).

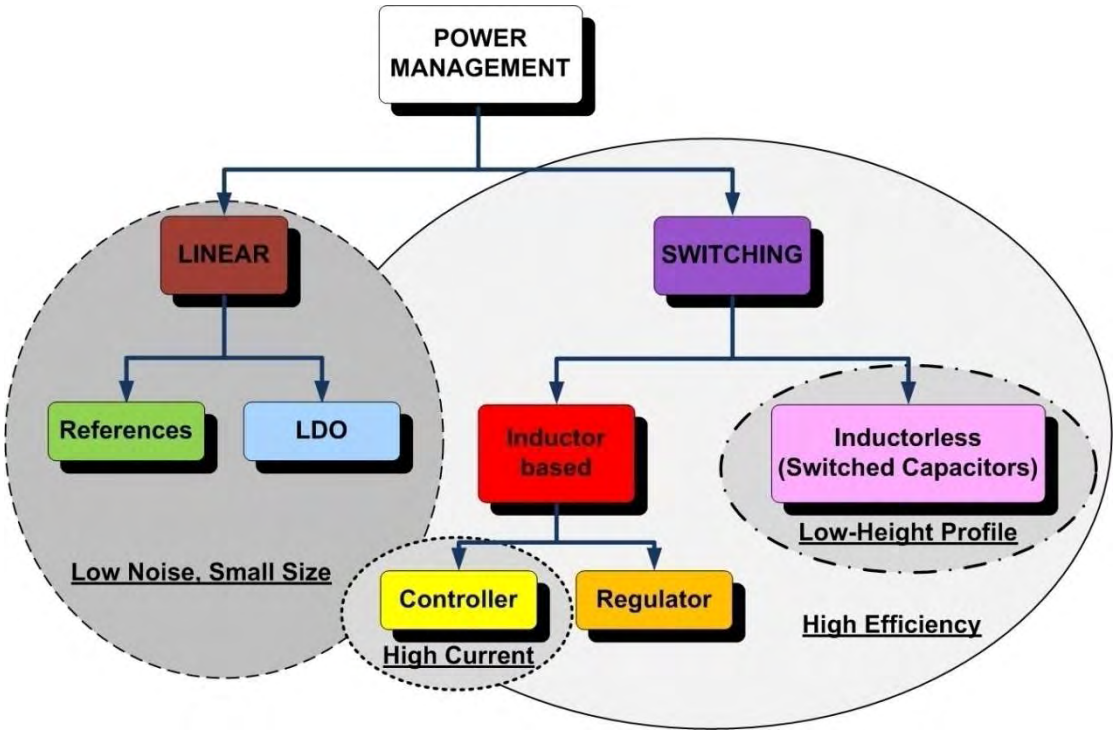

Fig. 1.2: Linear, inductive and charge pump solutions.

The inductor based regulator for low to medium load current levels integrates the switching elements (MOSFETs devices for high efficiency).
While, for higher load current levels, due to internal heat issues, the switching elements are not integrated. Such switchers are called controller.

The charge pump switcher is also known as switched capacitor regulator.
The charges from the input supply voltage are stored on a capacitor. Then these stored charges are transferred (switched) to the output. Since charge pump switchers produce discrete (integral and fractional) multiples of the input voltage, a post regulation is required. Typically, the regulation is achieved by including a linear regulator inside the charge pump switcher device. This post regulation typically leads to worse efficiency than the one of the inductive switchers.
Table 1.1 compares the performance of the three solutions, assuming same system requirements implemented without an optimized selection.

	Linear	Inductive	Charge Pump
Efficiency	20-60%	90-95%	50-70%
PCB Area	Very Small 2 Capacitors	Largest, Big Inductor 2 Capacitors	Medium Size 3-4 Capacitors
Ripple	Very Low	Low	Moderate
EMI	Very Low	Moderate	Low
Cost	Lowest	Highest	Medium

Tab.1.1: Linear, inductive and charge pump solution performance comparison.

As already mentioned, the solution with lowest cost, ripple and EMI interference is the linear regulator. It is worth to point out that this is not the most power-efficient choice. Furthermore, the linear regulator may create local heating in case of heavy load applications.

When power efficiency is the most important parameter, as for many battery operated applications, the inductive switching regulator is often the best solution. However, the price to pay is a significantly increased PCB area, higher ripple and EMI interference.

On the other hand, charge pump regulators are used typically when area and cost are more important than power efficiency and a higher output voltage ripple can be

tolerated. They provide a flatter profile than inductive solutions since the capacitors are usually smaller than the inductors.

1.2 INDUCTOR BASED DC-DC SWITCHING REGULATOR – BUCK CONVERTER TOPOLOGY INTRODUCTION

Consider the ideal circuit illustrated in Figure 1.3(a). The switch produces a rectangular voltage waveform $v_s(t)$ as shown in Figure 1.3(b). The voltage $v_s(t)$ is equal to the DC input voltage V_g when the switch is in position 1, while is equal to zero when the switch is in position 2.

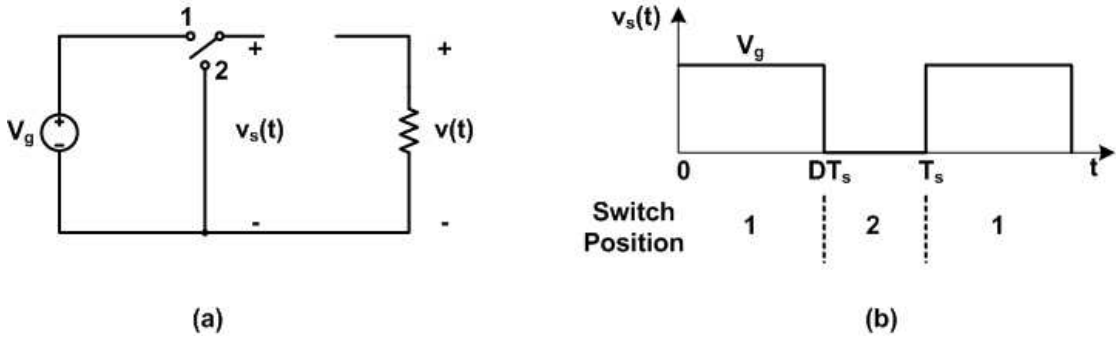

Fig. 1.3: Ideal switch, (a) to reduce the voltage DC component, and (b) its output voltage waveform $v_s(t)$.

The inverse of the switching period T_s is called switching frequency, f_s.

The duty ratio D is the fraction of the switching period that the switch spends in position 1 and it is a number between zero and one. The complement of the duty ratio, D', is defined as (1-D).

From the Fourier analysis, it is known that the DC component of $v_s(t)$ is given by its average value $\langle v_s(t) \rangle$:

$$\langle v_s(t) \rangle = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt \tag{1.3}$$

As depicted in Figure 1.4, the integral in (1.3) is given by the highlighted area under the curve. Therefore, the average value $\langle v_s(t) \rangle$ is:

$$\langle v_s(t) \rangle = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt = \frac{1}{T_s} \left(DT_s V_g \right) = DV_g \tag{1.4}$$

As stated by the equation (1.4), the switch reduces the input DC voltage V_g by a factor D.

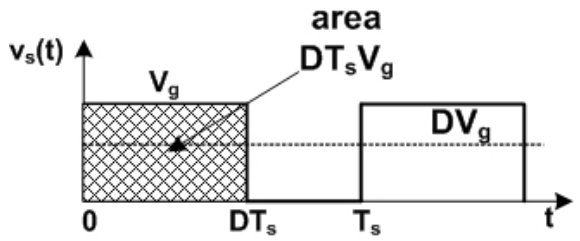

Fig. 1.4: Determination of switch output voltage DC component.

In order to obtain a DC output voltage, a low-pass filter has to be inserted. The filter will be designed to pass the DC components of v(t), but to reject the components of $v_s(t)$ at the switching frequency and its harmonics.
Thus, the output voltage v(t) will be essentially equal to the DC component of v(t):

$$v(t) \approx \langle v_s(t) \rangle = DV_g \tag{1.5}$$

The circuit shown in Figure 1.5 is the ideal buck converter.

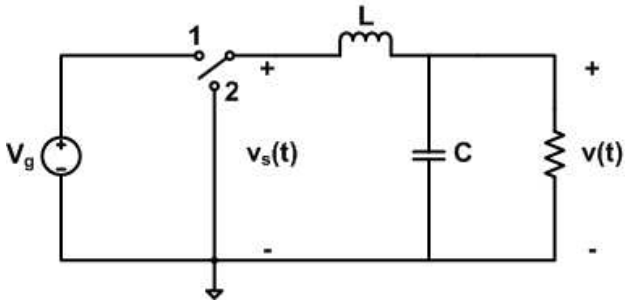

Fig. 1.5: Insertion of lossless low-pass filter - ideal buck converter circuit.

The low-pass filter is realized by ideal lossless elements (inductor L and capacitor C). To the extent that they are ideal, no active power is dissipated and then a power efficiency approaching 100% can be obtained.

Output voltage control can be achieved adjusting the duty ratio D. Figure 1.6 depicts the control characteristic of the DC-DC buck converter. The output voltage given by equation (1.5) is plotted vs. duty cycle.

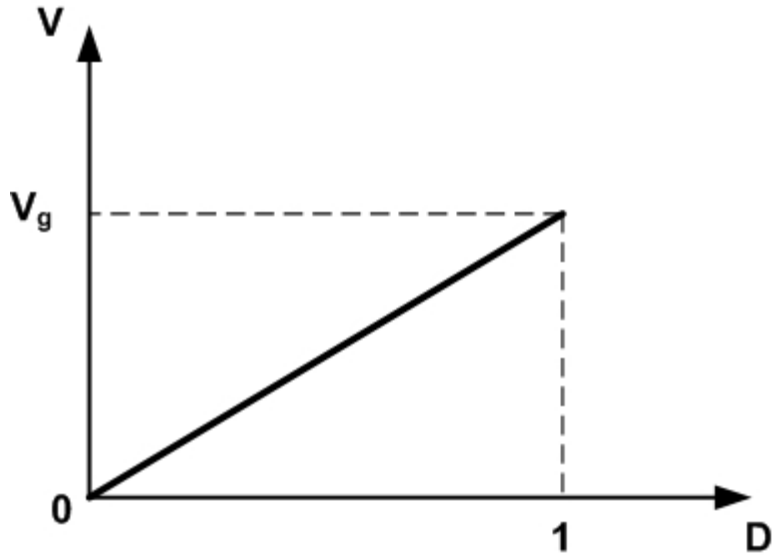

Fig. 1.6: Ideal buck converter DC output voltage V vs. duty cycle D.

It is worth to point out that the buck converter has a linear control characteristic.

Furthermore, since $0 \leq D \leq 1$, the output voltage is less than or equal to the input supply voltage. For this reason, the buck converter is also called step-down converter.

As it will be discussed later, in the Pulse-Width-Modulation (PWM) DC-DC switching regulator, the closed loop adjusts the duty cycle D accordingly in order to maintain the output voltage regulation, regardless of changes in the output load or in the input supply voltage.

1.3 SMALL RIPPLE APPROXIMATION, INDUCTOR VOLT-SECOND BALANCE AND CAPACITOR CHARGE BALANCE

Since in practice it is not possible to realize an ideal LC low-pass filter that completely rejects the components at the switching frequency and its harmonics, at least some small amount of high-frequency harmonics reaches the output.
Then, the output voltage waveform v(t) appears as in Figure 1.7, and can be expressed as:

$$v(t) = V + v_{ripple}(t) \tag{1.6}$$

Therefore, the output voltage waveform v(t) consist of the desired DC component V, plus a small undesired AC component $v_{ripple}(t)$ that arises from the switching harmonics incomplete attenuation by the LC low-pass filter.

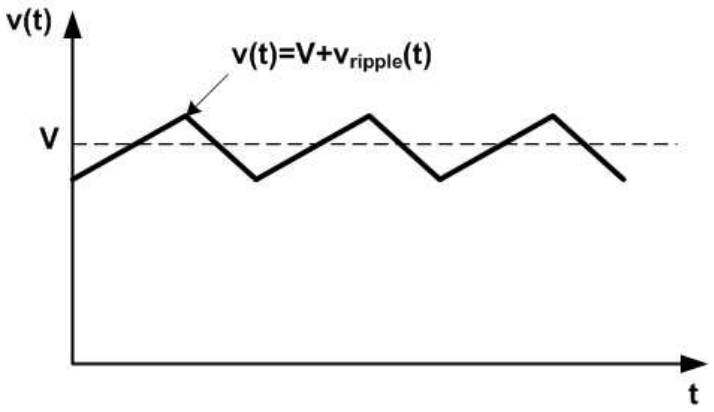

Fig. 1.7: Output voltage waveform.

Since the required output voltage ripple is usually less than 1%, it is possible to assume that the magnitude of the switching ripple is much smaller that the DC component:

$$\left\| v_{ripple}(t) \right\| \ll V \tag{1.7}$$

Therefore, neglecting the small ripple term $v_{ripple}(t)$, the output voltage v(t) is well approximated by its DC components V:

$$v(t) \approx V \tag{1.8}$$

This approximation is known as the small-ripple approximation and it greatly simplifies the analysis of the converter waveforms.

Consider now the inductor current waveform $i_L(t)$ in details. With the switch in position 1, the left side of the inductor L is connected to the input voltage V_g and the circuit reduces to Figure 1.8(a).

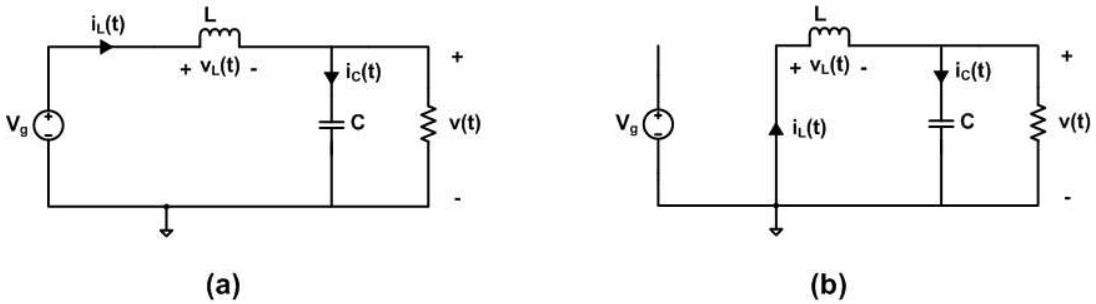

Fig. 1.8: Ideal buck converter circuit: (a) switch in position 1, (b) switch in position 2.

Since the small-ripple approximation holds, the inductor voltage $v_L(t)$ can be expressed by:

$$v_L(t)=V_g-v(t) \approx V_g-V \tag{1.9}$$

Therefore, with the switch in position 1, the inductor voltage $v_L(t)$ is essentially constant and equal to (V_g-V), as shown in Figure 1.9, while the slope of the inductor current waveform $i_L(t)$ is:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g-V}{L} \tag{1.10}$$

Thus, during subinterval 1, the inductor current slope is positive and essentially constant.

Similar arguments apply when the switch is in position 2. The left side of L is connected to ground, leading to the circuit of Figure 1.8(b).
Then the inductor voltage $v_L(t)$ during the second subinterval is given by:

$$v_L(t) = -v(t) \approx -V \tag{1.11}$$

While, the inductor current waveform $i_L(t)$ slope can be expressed as:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{-V}{L} \tag{1.12}$$

Thus, during subinterval 2, the inductor current slope is negative and essentially constant.

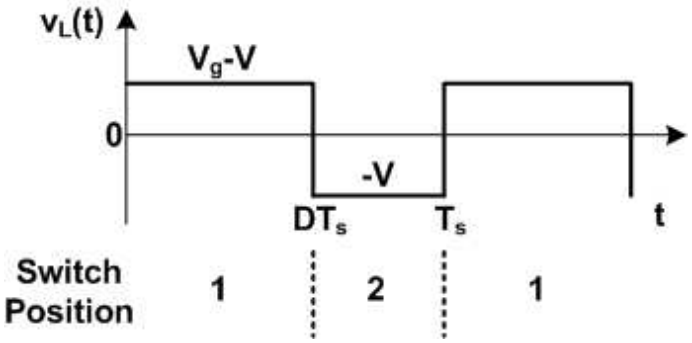

Fig. 1.9: Ideal buck converter circuit steady-state inductor voltage waveform.

Figure 1.10 shows the inductor current waveform $i_L(t)$. Here, $i_L(t)$ begins at some initial value $i_L(0)$.
As depicted in Figure 1.10, the peak inductor current is equal to the DC component I plus the peak-to-peak average ripple Δi_L. This peak current flows not only in the inductor, but also trough the semiconductor devices that realize the switch.
The knowledge of the peak current is necessary when designing this power devices and their metal trace interconnections.
Since $i_L(t)$ waveform is symmetrical with respect to I, during subinterval 1 the inductor current increases by $(2\Delta i_L)$.

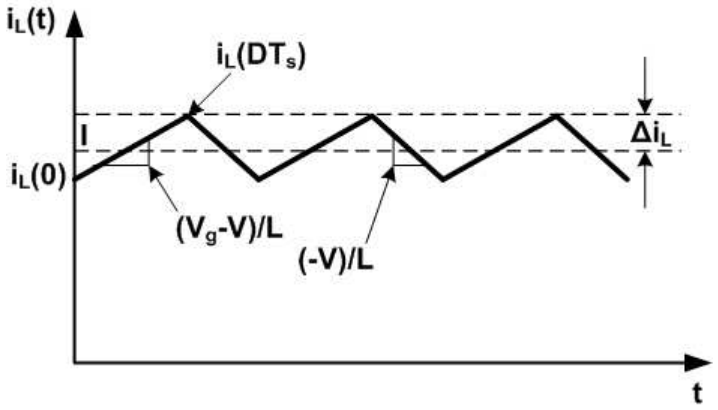

Fig. 1.10: Ideal buck converter circuit steady-state inductor current waveform.

Then, the change in current ($2\Delta i_L$) is equal to the slope times the length of the first subinterval DT_s as stated in:

$$(2\Delta i_L) = \left(\frac{V_g - V}{L}\right) - (DT_s) \tag{1.13}$$

solving for Δi_L:

$$\Delta i_L = \left(\frac{V_g\text{-}V}{2L}\right) \cdot (DT_s) \tag{1.14}$$

A trade-off between peak current issues and efficiency issues lead to typical values of Δi_L which lie in the range 30-40% of the maximum rated output current.
Therefore, the inductor value can be chosen such that a desired current ripple Δi_L is achieved, as expressed in:

$$L = \left(\frac{V_g\text{-}V}{2\Delta i_L}\right) \cdot (DT_s) = \left(\frac{V_g\text{-}V}{2\Delta i_L f_s}\right) \cdot D = \left(\frac{V}{2\Delta i_L f_s}\right) \cdot \left(1 - \frac{V}{V_g}\right) \tag{1.15}$$

It is also possible to solve the converter exactly, without the use of the small-ripple approximation, involving for instance the Laplace transform, but this is a great deal of work.

On the other hand, the small-ripple approximation is easy to apply, and quickly gives expressions that help in the converter design.

It is worth to point out that the inductor current waveform $i_L(t)$ of Figure 1.10 is drawn under steady-state conditions.

There is not net change in the inductor current $i_L(t)$ over a complete switching period and the relation $i_L(nT_s) = i_L((n+1)T_s)$ holds. This consideration leads to the inductor volt-second balance principle:

$$\left[i_L(T_s) - i_L(0)\right] = \frac{1}{L}\int_0^{T_s} v_L(t)dt = 0 \tag{1.16}$$

Therefore, in the steady-state, the integral of the applied inductor voltage must be zero. Multiplying both side by (L/T_s):

$$\frac{1}{T_s}\int_0^{T_s} v_L(t)dt = \left\langle v_L \right\rangle = 0 \tag{1.17}$$

Then, in equilibrium, the average applied inductor voltage is zero. This holds for any switching converter. Applying the volt-second balance to the buck converter circuit:

$$\int_0^{T_s} v_L(t)dt = \left(V_g - V\right)\cdot\left(DT_s\right) + \left(-V\right)\cdot\left(D'T_s\right) = 0 \tag{1.18}$$

Since $(D+D')=1$, solving for V:

$$V = DV_g \tag{1.19}$$

which coincides with the equation (1.4) obtained previously. Similar arguments can be applied to the output capacitor. Integrating the defining equation of a capacitor:

$$\left[v_C(T_s) - v_C(0)\right] = \frac{1}{C}\int_0^{T_s} i_C(t)dt = 0 \tag{1.20}$$

In the steady-state the net change over one switching period of the capacitor voltage must be zero.

Therefore, the integral of the capacitor current over one switching period has to be zero. This leads to the capacitor amp-second balance principle that holds in the steady-state:

$$\frac{1}{T_s}\int_0^{T_s} i_C(t)dt = \langle i_C \rangle = 0 \tag{1.21}$$

Using the KCL at the output node, it is possible to write:

$$i_C(t) = i_L(t) - i_{LOAD}(t) = i_L(t) - \frac{v(t)}{R_{load}} = i_L(t) - \frac{V}{R_{load}} \tag{1.22}$$

Averaging both terms of equation (1.22):

$$\langle i_C(t) \rangle = \langle i_L(t) \rangle - \frac{V}{R_{load}} \tag{1.23}$$

Since the capacitor amp-second balance principle holds:

$$\langle i_C(t) \rangle = 0 \Rightarrow \langle i_L(t) \rangle = \frac{V}{R_{load}} = I_{LOAD} \tag{1.24}$$

Therefore, in a buck converter, the average inductor current equals the load current in the steady-state.

1.4 BUCK CONVERTER OUTPUT VOLTAGE RIPPLE ESTIMATION

The small-ripple approximation predicts zero output voltage ripple, regardless the value of the output filter capacitance.

Since the only component of the output capacitor current arises from the inductor current ripple Δi_L, it cannot be neglected when calculating the output capacitor voltage ripple. Thus, a more accurate approximation must be used.

Accounting for the inductor current ripple Δi_L, the capacitor voltage ripple can be related to the total charge contained in the positive portion of the $i_C(t)$ current waveform.

Referring to Figure 1.10, the DC component I must flow entirely through the resistive output load, while the AC switching ripple divides between the resistive load and the output capacitor.

In a well-designed converter, the output capacitor provides a low impedance path for the AC switching ripple that flows almost entirely through the output capacitor. Therefore, the capacitor current waveform $i_C(t)$ is equal to the inductor current $i_L(t)$ minus the DC component I, as shown in Figure 1.11.

The current ripple is linear with peak value Δi_L.

The change in capacitor voltage can be related to the total charge q contained in the positive portion of the current waveform $i_C(t)$ by the capacitor relation Q=CV:

$$q = C \cdot (2\Delta v) \tag{1.25}$$

As depicted in Figure 1.11, the charge q is the integral of the current waveform $i_C(t)$ between its zero crossing points.

For this example, it can be expressed as the area of the shaded triangle. Owing to the waveform symmetry, the zero crossings occur at the center points of DT_s and $D'T_s$ subintervals. Hence, the base dimension of the triangle is $T_s/2$.

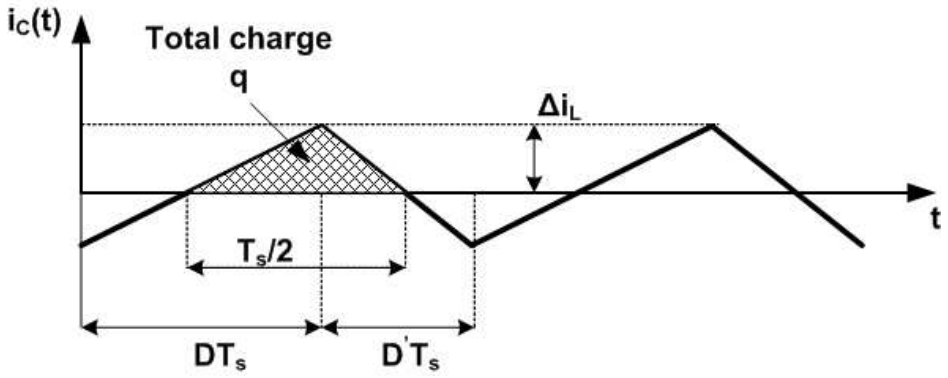

Fig. 1.11: Ideal buck converter circuit steady-state output capacitor current waveform.

Thus, the total charge q is given by:

$$q = \frac{1}{2} \cdot (\Delta i_L) \cdot \left(\frac{T_s}{2} \right) \tag{1.26}$$

Solution for the voltage ripple peak amplitude Δv is expressed by:

$$\Delta v = \frac{\Delta i_L T_s}{8C} = \frac{\Delta i_L}{8Cf_s} \tag{1.27}$$

This equation can be used to select the proper value of the capacitance C such that the output voltage ripple Δv required by a specific application is achieved.
In practice, also the additional voltage ripple caused by the capacitor equivalent series resistance (ESR) must be included.

1.5 MOS BUCK DC-DC SWITCHING CONVERTER – PULSE WIDTH -MODULATION (PWM) WAVEFORMS

Figure 1.12(a) shows the synchronous, while Figure 1.12(b) the non-synchronous buck DC-DC switching converter. The synchronous architecture uses a NMOS transistor as a low-side switch instead of a diode.

At high-current and low-output voltage levels, the diode voltage loss (usually around 700mV) could become significant in comparison to the output voltage.

Therefore, in this case, the synchronous structure is preferred, since the drain-to-source voltage across a MOS transistor can be significantly lower than the equivalent voltage drop across a diode.

When the high-side switch is a PMOS device, this configuration can reach a duty cycle equal to 1 without voltage-boost for the PMOS transistor gate driving.

On the other hand, when a NMOS device is used as the high-side switch, often a capacitor and a diode boost are required to reach unary duty cycles.

Figure 1.13 shows the MOS buck DC-DC switching converter current and the voltage waveforms of the so called switching node ($V_{SW}(t)$ voltage in Figure 1.12) in the PWM operation.

As already discussed, the inductor current rises at the high-side switch turns on and transfers energy from the input to the inductor. The inductor current falls as the low-side switch turns on and transfers the inductor energy to the output load.

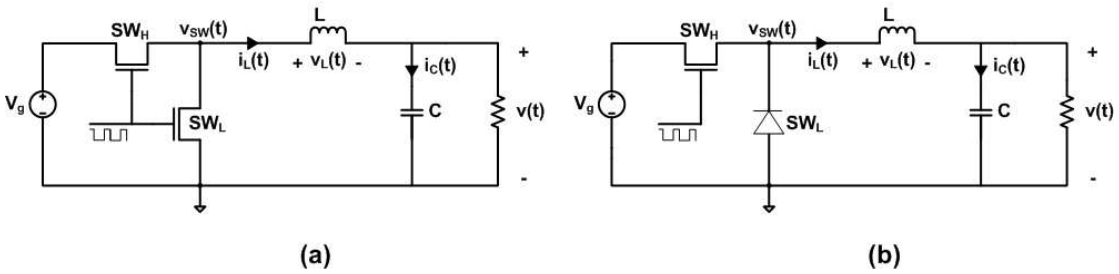

Fig. 1.12: (a) Synchronous buck DC-DC switching converter, and its non-synchronous implementation (b).

As shown in Figure 1.13, the output current I_{LOAD} equals the average value of the inductor current I_L.

It is possible to define a useful parameter, called the current ripple ratio r, which is the ratio of the AC to the DC value of the inductor current, while the converter is delivering the maximum load:

$$r = \frac{2\Delta i_L}{I_L} = \frac{2\Delta i_L}{I_{LOAD,max}} = \left(\frac{V_g - V}{L f_s I_{LOAD,max}} \right) \cdot D = \left(\frac{V}{L f_s I_{LOAD,max}} \right) \cdot (1 - D) \qquad (1.29)$$

As stated by equation (1.29), the current ripple ratio r is proportional to (1-D). This parameter is important, as it determines the inductance L and the physical size of most of the power components.

It can be shown that, by increasing r, the inductor size is reduced. However, a ratio r of 0.3–0.4 usually represents the most optimum choice for any topology.

The inductor peak current $I_{L,pp}$ can be expressed as:

$$I_{L,pp} = I_{LOAD,max} \cdot \left(1 + \frac{r}{2} \right) \qquad (1.30)$$

While, the rms inductor current $I_{L,rms}$:

$$I_{L,rms} = I_{LOAD,max} \cdot \sqrt{\left(1 + \frac{r^2}{12} \right)} \qquad (1.31)$$

The inductor peak current value $I_{L,pp}$ needs to be known so as to accurately evaluate the energy handling requirement of the inductor and to avoid core saturation.

As shown in Figure 1.13, the buck converter input current is discontinuous, with short rise and fall times. For this reason, an input capacitor is mandatory, in order to provide a low-impedance supply for the converter and to reduce the noise on the input supply.

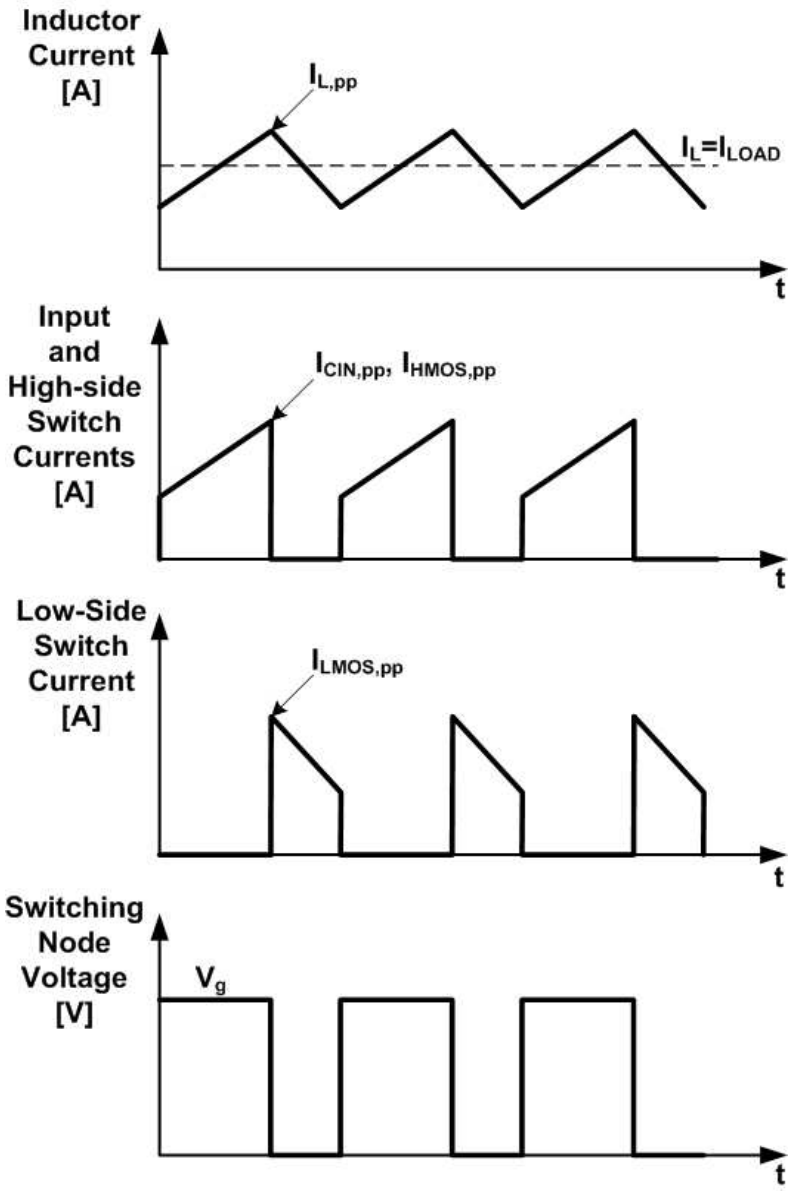

Fig. 1.13: MOS buck DC-DC switching converter current waveforms and switching node voltage waveform in PWM.

The input capacitor peak current $I_{CIN,pp}$ equals the inductor peak current $I_{L,pp}$, while the input capacitor rms current $I_{CIN,rms}$ is:

$$I_{CIN,rms} = I_{LOAD,max} \cdot \sqrt{D \cdot \left[(1-D) + \frac{r^2}{12} \right]} \tag{1.32}$$

The input capacitor rms current $I_{CIN,rms}$ is a key parameter. It determines the basic and minimum selection criteria since the capacitor must be rated at least for the worst case rms current that may pass through it.
Indeed, manufactures do not ensure any life expectation on a capacitor operating with a rms current higher than its rated value.
The output capacitor also needs to be at least big enough to handle the worst case rms current, $I_{COUT,rms}$, through it:

$$I_{COUT,rms} = I_{LOAD,max} \cdot \frac{r}{\sqrt{12}} \tag{1.33}$$

The peak to peak current, $I_{COUT,ppl,,}$ is expressed as:

$$I_{COUT,pp} = I_{LOAD,max} \cdot r \tag{1.34}$$

$I_{COUT,pp}$ through the output capacitor determines, as already mentioned, an additional output voltage ripple contribution:

$$\Delta v_{esr} = I_{COUT,pp} \cdot r_{esr} \tag{1.35}$$

Where r_{esr} is the equivalent series resistance of the output capacitor.
It is worth to point out that, in practice, this output voltage ripple contribution is the major component of the noise spectrum at the output of the power supply.
While, with regard to high-side and low side switches currents, they can be expressed respectively by:

$$I_{HMOS,rms} = I_{LOAD,max} \cdot \sqrt{D \cdot \left[1 + \frac{r^2}{12}\right]} \tag{1.36}$$

$$I_{LMOS,rms} = I_{LOAD,max} \cdot \sqrt{(1-D) \cdot \left[1 + \frac{r^2}{12}\right]} \tag{1.37}$$

It is evident from Figure 1.13 that the MOS switches peak currents $I_{HMOS,pp}$ and $I_{LMOS,pp}$ equal the inductor peak current $I_{L,pp}$.

1.6 DESIGNING FOR HIGH EFFICIENCY PWM BUCK CONVERTERS

Nowadays, the power efficiency is the most important parameter for a DC-DC regulator.

As already mentioned, the converter power efficiency is defined as the ratio of the converter output power to converter input power. Since the input source supplies the output power and the energy consumed by the converter losses, it is possible to write:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{1.38}$$

Therefore, an efficiency-oriented design, should minimize the power losses contributions. Then, it is important to evaluate the impact of each component on the overall losses.

Each loss component can be characterized into the two following categories:

- DC losses (conduction losses and quiescent operating current)
- AC losses (switching losses)

Figure 1.14 shows the buck DC-DC switching regulator circuit parasitic elements that are the main source of power dissipation.

This Figure includes all the series parasitic resistances (switch on-resistances and inductor winding resistance), switching node parasitic capacitance, C_{sw}, and parasitic drain-body diodes of the MOS power transistors.

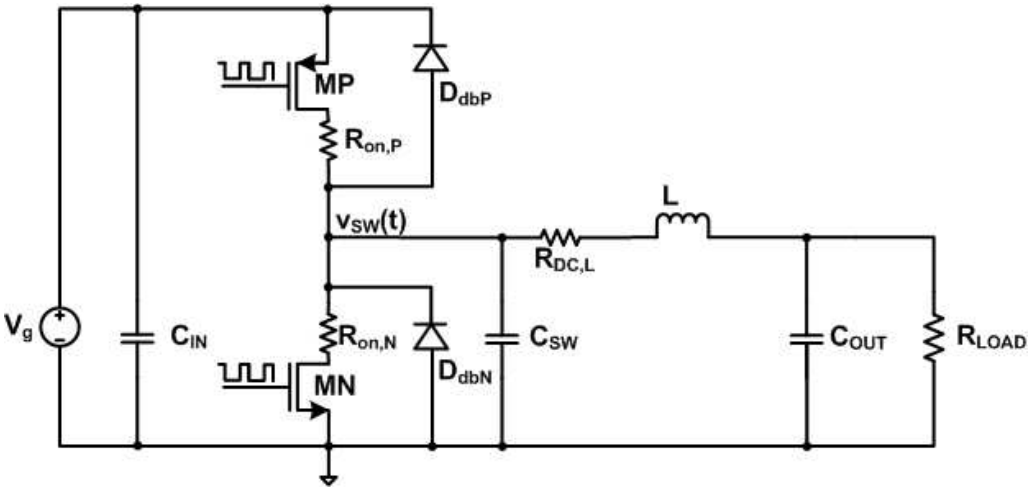

Fig. 1.14: MOS buck DC-DC switching converter including main parasitic components.

1.6.1 CONDUCTION LOSSES

Current flowing through non-ideal power transistors, filter elements and metal interconnections results in a power dissipation in each component equal to:

$$P_{conduction,i} = I_{rms,i}^{\ 2} \cdot R_i \tag{1.39}$$

where I_{rms} is the root mean squared current through the i-th component, and R_i is the parasitic resistance of the i-th component. In PWM mode, the rms current has a DC and an AC component:

$$I_{rms,i}^{\ 2} = I_{rms,DC,i}^{\ 2} + I_{rms,AC,i}^{\ 2} \tag{1.40}$$

It can be shown that:

$$I_{rms,DC,i}^{\ 2} = d_i \cdot I_{LOAD}^{\ 2} \tag{1.41}$$

$$I_{rms,AC,i}^{\ 2} = d_i \cdot \frac{1}{3}\left(\frac{\Delta I_L}{2}\right)^2 \tag{1.42}$$

where d_i is a weighting factor that indicates the switching period fraction of time in which the current flow through the i-th component, I_{LOAD} is the DC load current, and ΔI is the peak-to-peak inductor current ripple.
Since, decreasing the load current, the DC conduction loss scales quadratically, it degrades the regulator power efficiency at heavy loads. On the other hand, the AC conduction loss is a fixed quantity and then decreases the efficiency at light loads.

1.6.2 AC LOSSES – GATE-DRIVE LOSSES

Pulling up and down the gate of a power transistor each switching cycle dissipates a dynamic average power:

$$P_{gate} = E_{gate} f_s \tag{1.43}$$

where E_{gate} is directly proportional to the gate energy transferred per off-to-on-to-off gate transition cycle (which can include some energy due to Miller effect), and includes dissipation in the driver circuitry. Since the gate-drive loss is independent of the load current, it degrades the light load efficiency.

1.6.3 AC LOSSES – GATE-DRIVE TIMING ERRORS

Three mutually exclusive mechanisms of losses due to timing errors in the switching of the power MOSFETs are described below. Each contribution is independent of the output load.

1.6.3.1 NO DEAD-TIME: SHORT CIRCUIT LOSS

A short-circuit path may temporarily exist between the input rails during power MOSFETs switching transitions.

To avoid potentially large short-circuit losses, it is necessary to provide dead-times in the conduction of the MOSFETs with local digital feedback to ensure that the two devices never conduct simultaneously.

1.6.3.2 DEAD-TIMES TOO LONG: BODY-DIODE CONDUCTION

If the lengths of the dead-times are too long, the parasitic body diode of the low-side NMOS power transistor may be forced to pick up the inductor current for a fraction of each switching cycle.
Since the forward bias diode voltage V_{diode} is around 700mV, in low-voltage applications it can be comparable to the output voltage and its conduction loss may be significant:

$$P_{diode} \approx 2 \cdot \left(I_{LOAD} V_{diode} t_{err} f_s \right) \tag{1.44}$$

where t_{err} is the timing error between complementary power MOSFET conduction intervals, I_{LOAD} is the output current and f_s is the switching frequency. Furthermore, when the PMOS device is turned on, it must remove the excess minority carrier charge from the body diode, thus dissipating an energy bounded by:

$$E_{rr} \approx Q_{rr} V_g \tag{1.45}$$

where Q_{rr} is the stored charge in the parasitic body diode.

1.6.3.3 DEAD-TIMES TOO SHORT: CAPACITIVE SWITCHING LOSS

In a hard-switched converter, the PMOS transistor MP charges parasitic capacitance C_{sw} to V_g each switching cycle, thus dissipating an average power given by:

$$P_{C_{sw},LH} \approx \frac{1}{2} C_{sw} V_g^{\,2} f_s \tag{1.46}$$

where C_{sw} includes reverse-biased drain-body junction diffusion capacitance C_{db} and some or all of the gate-drain overlap (Miller) capacitance C_{gd} of the power transistors, wiring capacitance from their interconnection, and stray capacitance associated with bonding wires and pads.

When the MP device is turned off, the inductor begins to discharge C_{sw} from V_g to ground. If low-side NMOS transistor MN is turned on exactly when V_{sw} reaches ground, this transition is lossless.

If the NMOS device is turned on too late, V_{sw} will be discharged below ground, until the body diode is forced to conduct. If the NMOS transistor is turned on too early, it will discharge V_{sw} to ground through its channel, introducing losses:

$$P_{C_{sw},HL} \approx \frac{1}{2} C_{sw} V_{sw}^{\ 2} f_s \le \frac{1}{2} C_{sw} V_g^{\ 2} f_s \tag{1.47}$$

1.6.4 QUIESCENT OPERATING POWER

The PWM and the other control circuitry consume static power. In low-power applications, this control power may contribute substantially to the total losses, even at full-load.

1.6.5 IMPROVING LIGHT-LOAD EFFICIENCY

While a PWM DC-DC converter can be designed to be highly efficient at heavy-load, the light-load efficiency is degraded, since many of its losses components are independent of load current, and, therefore, dissipate a significant amount of power compared to the output power.

For Instance, Figure 1.15 plots the estimated conduction losses, gate-drive losses and quiescent operating power versus output current in the range 10mA→1A for a PWM buck converter with the following parameters:

- $R_{on,P}$, $R_{on,P}$ =60mΩ

- R_{DCL}=100mΩ
- V_{supply} =3.6V
- D=0.5
- I_{ripple}=100mA
- F_s =3MHz
- $C_{p,MP}$ =20pF
- $C_{p,MN}$=6pF
- I_q=1mW

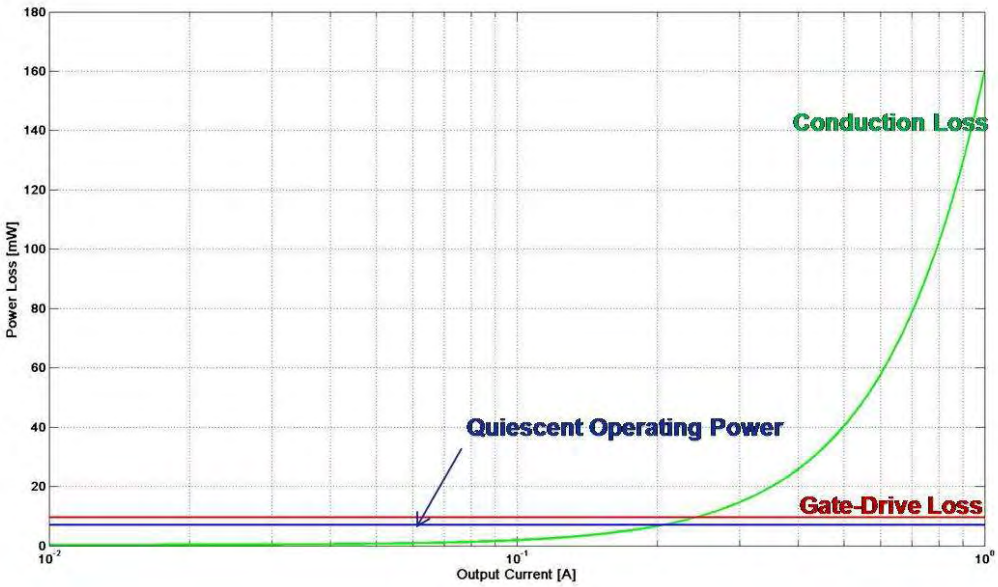

Fig. 1.15: Estimated conduction losses, gate-drive losses and quiescent operating power versus output current in the range 10mA→1A for a PWM buck.

It can be noted that, as the load scales downward, the AC losses and quiescent operating power become increasing significantly, and the total dissipation in the converter asymptotes to a fixed minimum power dissipation.

Figure 1.16 plots the resulting estimated power efficiency versus output current in the range 10mA→1A.

From this Figure, it may be concluded that a PWM converter which is 95% efficient at full load is roughly 50% efficient at one percent of the full load.

For instance, in portable applications, if the converter would be used at full load for little of its operating time, energy loss at light load would be the dominant limitation on battery run-time, and improving efficiency at light load would become essential.
One control scheme which achieves high light load power efficiency is the Pulse-Frequency-Modulation (PFM). In this scheme, the converter operates only in short bursts at light load.

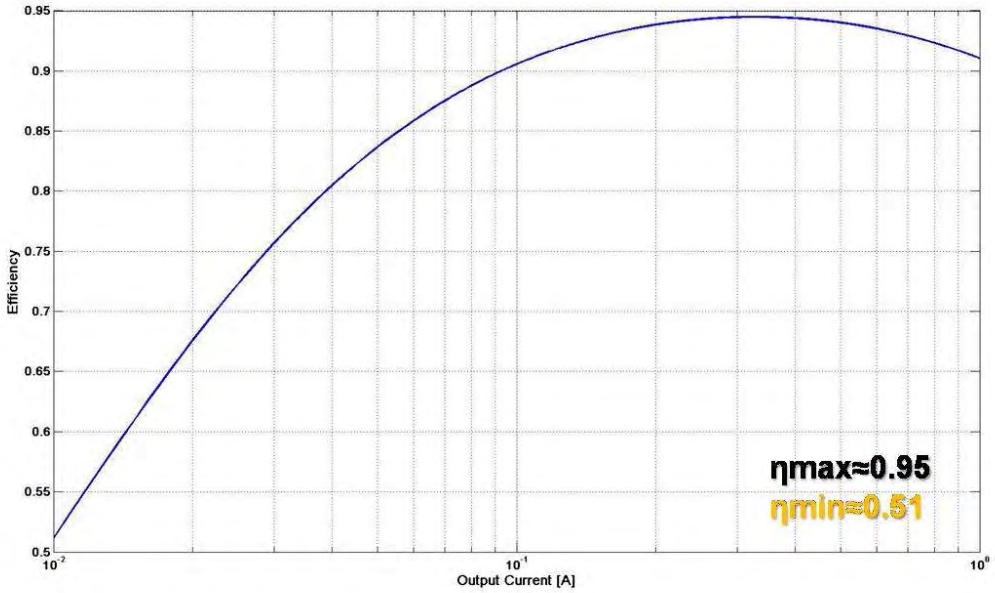

Fig. 1.16: Estimated power efficiency versus output current in the range 10mA→1A for a PWM buck.

The PFM mode can be implemented with single-burst per cycle or multiple-bursts per switching cycle.
Between bursts, both power MOSFETs are turned off and the circuit idles with zero inductor current. Then, the output filter capacitor sources the load current.
When the output is discharged to a certain threshold below a reference voltage, the converter is activated for another burst, returning charge to the output capacitor. Therefore, the load-independent losses in the circuit are reduced and the light-load power efficiency is sustained. As the load current decreases, the idle time increases.

Thus, regulation is achieved when the charge delivered through the inductor is equal to the charge consumed by the load.

Figure 1.17 shows the switching node voltage V_{SW}, inductor current I_L and output voltage V_{OUT} waveforms of the commercial National Semiconductor IC LM3686 step-down converter working in PFM mode.

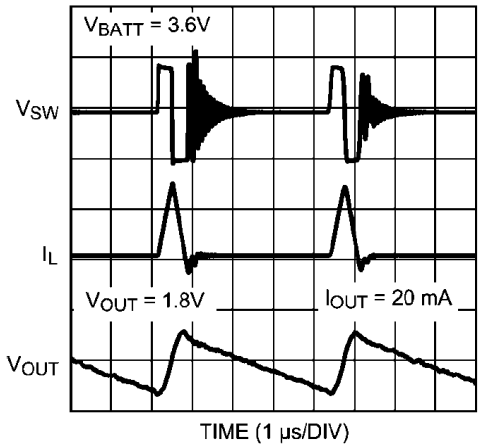

Fig. 1.17: Switching node voltage V_{SW}, inductor current I_L and output voltage V_{OUT} waveforms of the National Semiconductor LM3686 step-down converter working in PFM mode.

Some solutions sense the output current and switch automatically between PWM and PFM modes to obtain an efficiency curve as flat as possible even on a wide range of load currents.

It is worth to point out that, one major drawback of PFM control is that the switching period (the time between charge bursts) is a function of load.

Thus, the converter appears almost chaotic and the switching noise unpredictable. This is not well-suited to several applications as wireless communications applications.

Moreover, PFM mode leads to higher output voltage ripple and, with regard to dual-mode PFM-PWM switching regulators, the switching between the two modes leads to worse load-regulation transient responses and higher voltage drops during transitions.

Figure 1.18 shows switching node voltage V_{SW}, inductor current I_L, output voltage

V_{OUT} , output current I_{OUT} waveforms of the commercial National Semiconductor LM3671 step down converter during mode change.

Output voltage is set to 1.5V and the output current change from 50mA to 400mA.

It can be noted the higher output voltage ripple relative to the PFM mode and the mode change output voltage drop of about 60mV.

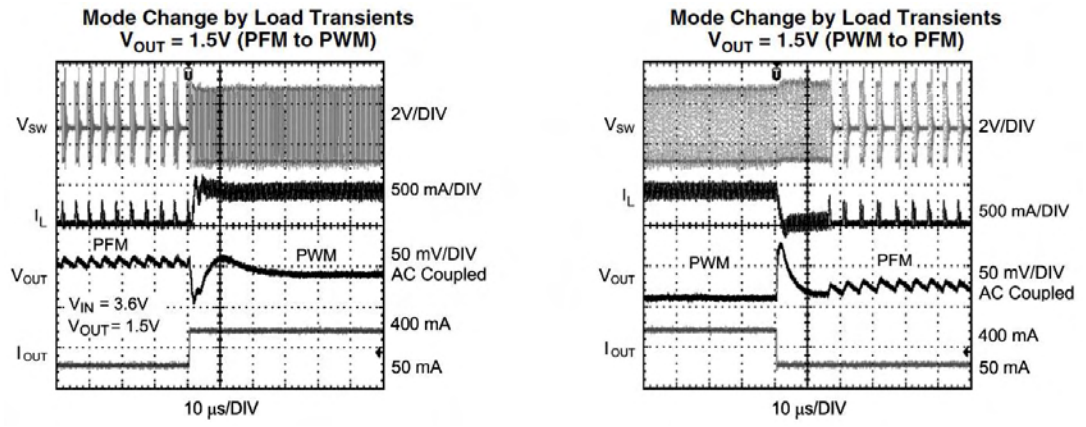

Fig. 1.18: Switching node voltage V_{SW}, inductor current I_L, output voltage V_{OUT} and output current I_{OUT} waveforms of the National Semiconductor LM3686 step-down converter during mode change, V_{OUT} is set to 1.5V.

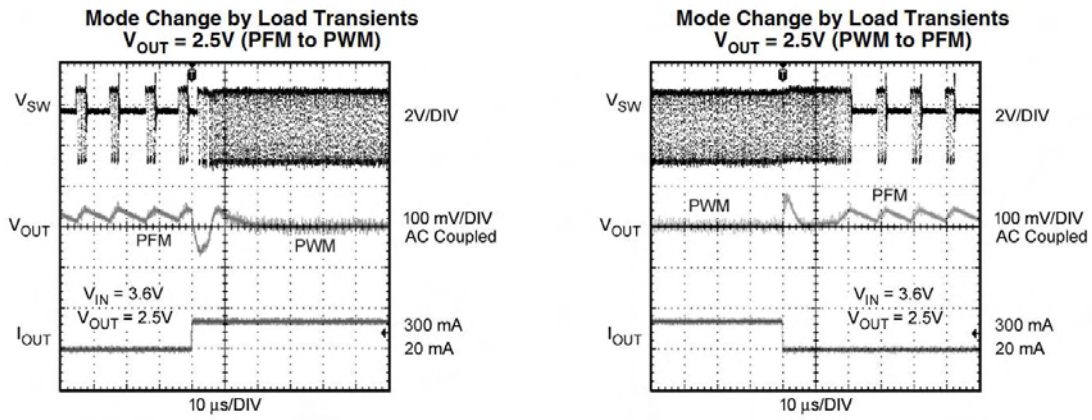

Fig. 1.19: Switching node voltage V_{SW}, inductor current I_L, output voltage V_{OUT} and output current I_{OUT} waveforms of the National Semiconductor LM3686 step-down converter during mode change, V_{OUT} is set to 2.5V.

Figure 1.19 shows the same waveforms, but with the output voltage sets to 2.5V and the output current changing from 20mA to 300mA.
Also in this case, it can be noted the higher output voltage ripple relative to the PFM mode and the mode change output voltage drop of about 100mV.
As already discussed in Sections 1.3 and 1.5, the inductor ripple current magnitude depends only on the chosen inductor value, input, output voltages and the switching frequency of the regulator design. The inductor ripple current magnitude does not depend on the output current I_{LOAD}. Therefore, when the output current reduces below the ripple level, the inductor current can go negative. During this time the inductor current is not productive (it leads to loss but it does not contribute to the I_{LOAD}).

To improve power efficiency and to avoid such losses, other than the previously discussed PFM mode, there is also the Discontinuous-Conduction-Mode (DCM). In DCM the switching frequency is constant but, when the reversal of inductor current during the on-time of the low-side NMOS power device is detected, this switch is opened. Then, during the remaining part of the switching period, both power switches are off. In non-synchronous regulators that use diode instead of the low side NMOS power switch the DCM occurs automatically. While, the synchronous regulators that use DCM mode have to implement zero cross detect.

The MOSFETs used as switches have lower limits on how fast they can be opened and closed. This minimum possible on-time of the PMOS limits, in constant frequency DCM mode, the minimum load current at which the output stays in regulation. If the output load current is reduced beyond this limit, the output voltage will start to rise, limited only by over voltage protection or some other breakdown.

1.6.6 INDUCTOR CURRENT SENSING

Both PFM and DCM modes need the inductor current zero cross detect. A straightforward approach is to put a sense resistor on the power train and measure the voltage drop across it. However, this approach is not suitable for low input voltage applications, since it may degrade the power efficiency at heavy loads. Another possibility, since the current reversal happens when the low-side NMOS power switch is on, is to sense the voltage drop across the on-resistance of the NMOS power switch, as shown in Figure 1.20.

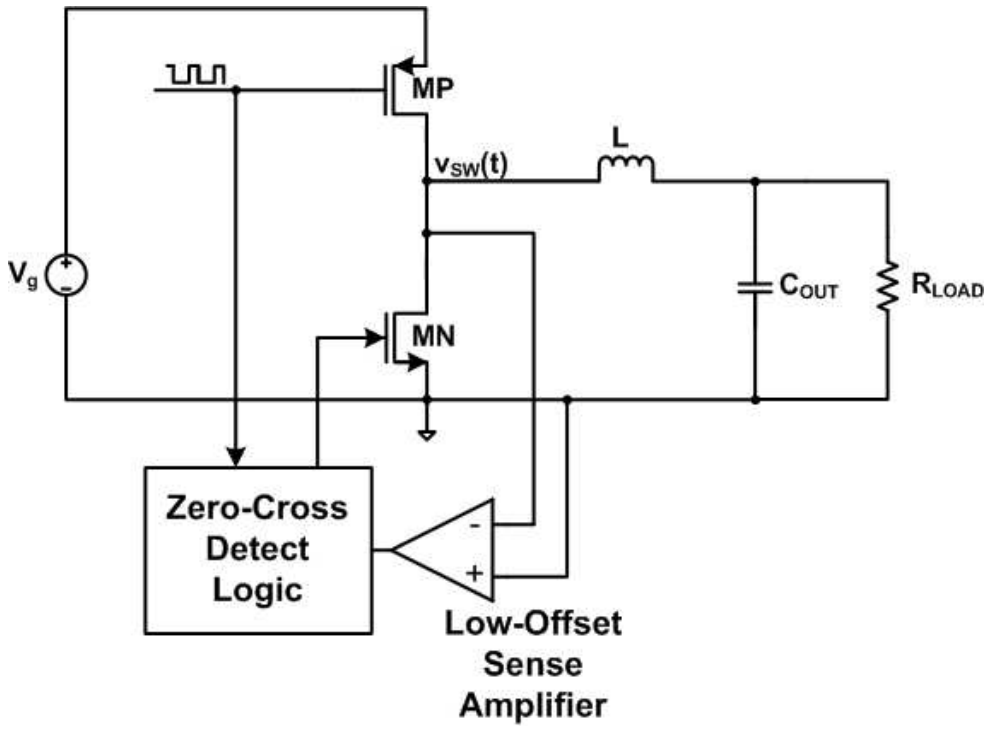

Fig. 1.20: Inductor current zero cross detect with micro-power low-offset operational amplifier.

It is worth to point out that, since the voltage drop to sense to achieve zero cross detect, and to avoid the timing errors, is in the hundred μV range and this operation requires a low-offset operational amplifier.

In addition, to avoid light load efficiency degradation, the zero cross detection circuit and, in particular the operational amplifier, must have a very low quiescent operating current.
The Micro-Power chopper correlated-double-sampling amplifier presented in Chapter 4 is suitable for this application.

1.7 VOLTAGE-MODE CONTROL (VMC) BUCK REGULATORS

Voltage-mode control (VMC) buck regulators sense the output voltage at the feedback pin and modulate the duty cycle D accordingly to maintain output voltage regulation.
The goal of a voltage regulator design is to realize a system whose behavior is as close as possible to the one of an ideal voltage-controlled voltage-source, with the highest power efficiency and highest immunity against input and output disturbances.
Figure 1.21 shows the block diagram of the VMC buck regulator. The VMC converter consists of three main sections:

- Modulator stage.
- Output filter and power stage.
- Feedback and error-amplifier stage.

The modulator contains a PWM comparator that compares the timing saw-tooth waveform (with frequency is equal to the switching frequency) with a control voltage $V_{control}$. Modulator gain depends on the saw-tooth peak to peak amplitude.
The comparator gives at his output a constant-frequency, variable-pulse-width signal that drives the output filter and the MOSFETs power stage.
Power stage and output filter consist of high-side and low-side power switches and the LC output low-pass filter network. The gain of this stage depends on the duty cycle D.
Since the system is a closed-loop regulator, it typically needs a compensation control circuit in order to comply with the required static and dynamic performance.

In most VMC regulators the compensation circuit is made of an operational amplifier and a set of passive components to realize the error amplifier. The output voltage is sensed by means of a voltage divider usually embedded in the compensation control circuitry.

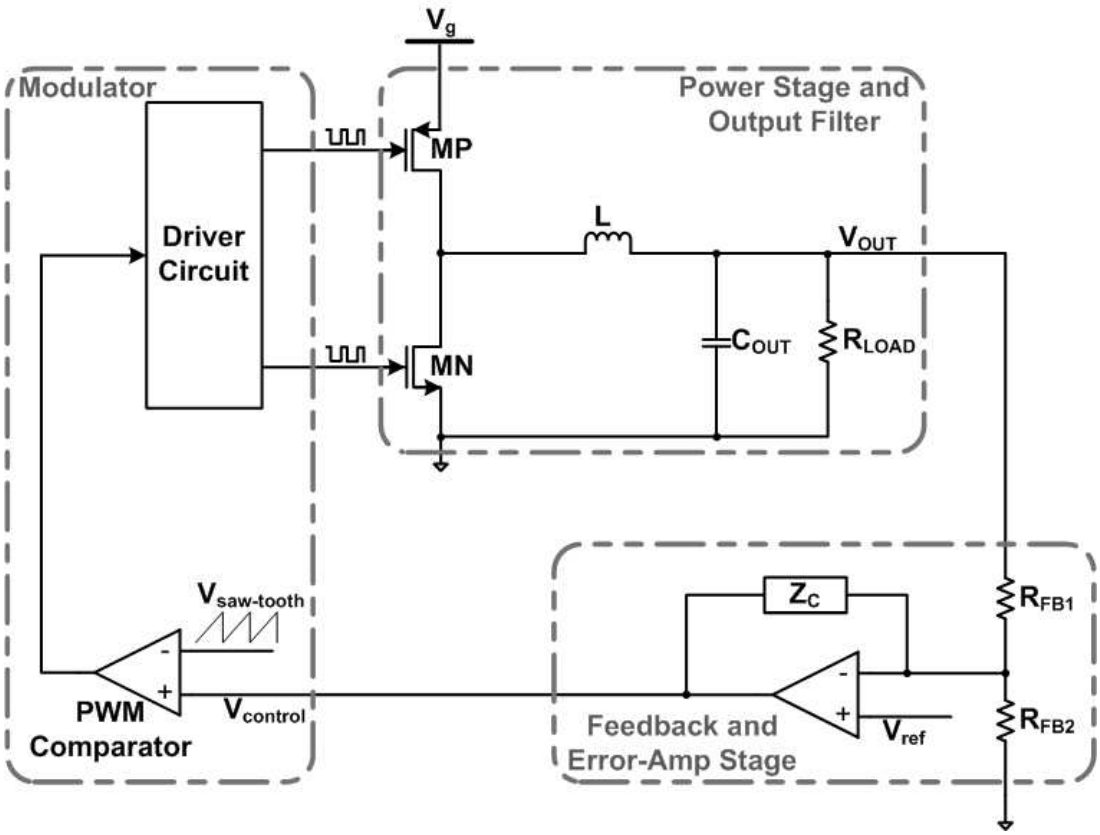

Fig. 1.21: Voltage-mode control (VMC) buck regulator block diagram.

The VMC topology has a large amplitude saw-tooth waveform, which provides good noise margin for a stable modulation. It is easy to design and analyze since it has a single feedback path.

Since the control loop does not have to sense the inductor current, low duty cycle are generally available to voltage-mode control devices.

On the other hand, there are some compensation issues that arise from the fact that the closed loop gain varies with the duty D and the double LC pole may need a second order compensation network. Furthermore, mode change gives additional compensation issues.

Moreover, any change in the supply voltage has to be first sensed at the output and then corrected by the feedback, thus leading to slow transient responses to line voltage changes.

1.8 CURRENT-MODE CONTROL (CMC) BUCK REGULATORS

Current-mode control (CMC) architectures may help in realizing voltage regulators with good dynamic performance when the input supply voltage is susceptible of fast and sharp transient variations. Figure 1.21 shows the block diagram of a CMC buck regulator.

While in a VMC regulator a saw-tooth waveform, separately generated, is compared to a control voltage $V_{control}$, in a CMC regulator the inductor current is converted to a voltage signal and replaces the saw-tooth waveform. Then, the CMC involves two loops. An inner loop, realizing a form of feed-forward, and an outer voltage loop, realizing a classical output voltage feedback.

Nowadays, the most popular type of CMC is the so called peak-current-mode control.

In peak CMC the high-side switch is turned-off when the inductor current reaches a threshold level, determined by the difference between the control signal (provided by the voltage error amplifier of the feedback loop) and a compensation ramp signal. Without descending in details, compensation ramp is necessary to avoid sub-harmonic oscillations in applications requiring duty cycles higher than 0.5.

The first advantage of the CMC is that the control-to-output transfer function (defined in Section 3.4) has a single pole system at low frequency, since the inductor has been controlled by the current loop. This improves the phase margin and requires only first-order compensation circuits.

Second, since the inductor current rises with a slope determined by the difference between input and output voltage, the regulator immediately responds to line variations. Moreover, regulator current limiting is inherent in CMC.

On the other hand, the main disadvantages are that the control is highly susceptible to switching node noise and the cost represented by the additional power dissipation of the current sensing circuit.

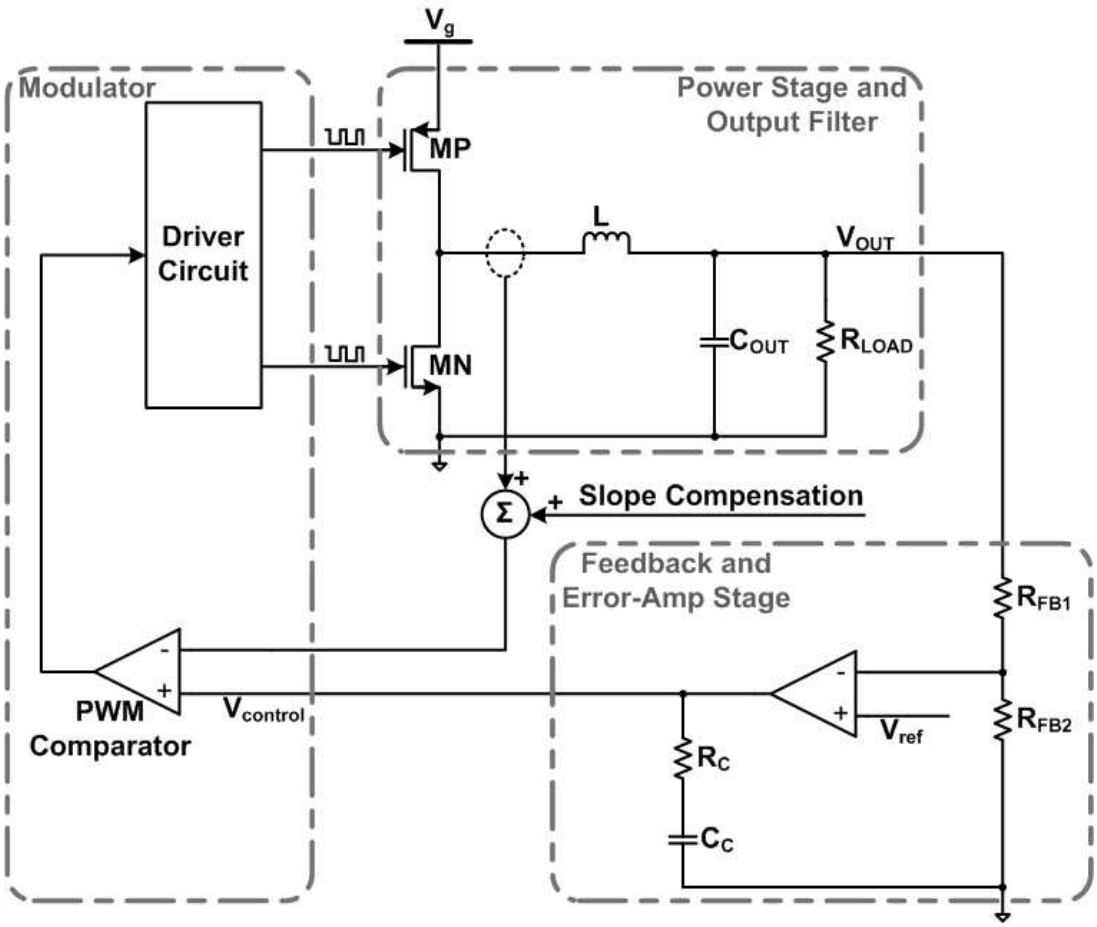

Fig. 1.22: Current-mode control (CMC) buck regulator block diagram.

1.9 TRANSIENT RESPONSE

The ability of the DC-DC converter to keep the output voltage V_{OUT} in regulation when input supply or output load changes, is called line and load regulation respectively.

The transient response shows how quickly the regulator gets the V_{OUT} back in regulation. As discussed in Section 1.7, in VMC the output voltage is sensed at the feedback pin of the regulator. While, as discussed in Section 1.8, CMC regulators sense also the switch current.

When the output load current changes, it momentarily translates to a voltage change at the output, due to the output impedance of the regulator. In response to the load change, the regulator closed-loop control automatically adjusts the duty cycle D (or the switching frequency f_s depending on the PWM/PFM mode of operation). This translates to a change in the currents in the various components and, hence, in a input source current variation.

At steady-state, the duty cycle goes back to satisfy the $V_{OUT} = DV_g$ equation.

Similar change in frequency or (and) duty cycle occurs in response to a line change, to keep the output voltage in regulation.

Figures 1.23(a) and 1.23(b) show a stable regulator (National Semiconductor LM3678 step-down converter) responding to a change in the output load.

In Figure 1.23(a), the input supply voltage is 3.6V while the output voltage is set to 1.2V. Load changes from 0 to 500mA. While, in Figure 1.23(b), the input supply voltage is 3.6V while the output voltage is set to 0.8V. Load changes from 0 to 500mA.

Figures 1.24(a) and 1.24(b) show a stable regulator (National Semiconductor LM3678 step-down converter) responding to a change in input supply voltage.

In Figure 1.24(a) the output load is 500mA while the output voltage is set to 1.2V. Input supply changes from 3 to 3.6V. In Figure 1.24(b), the output current is 500mA while the output voltage is set to 0.8V. Input supply changes from 0 to 500mA.

The smaller the parasitic impedances (e.g., ESR of C_{OUT}, DCR of the inductor) and faster the switches, the quicker the regulator will react to a load transition.

On the other hand, such smaller impedances could also lead to higher ripple, noise and loss of ability to reach the steady-state.

Load-regulation for a dual-mode converter was already shown in Figures 1.18 and 1.19.

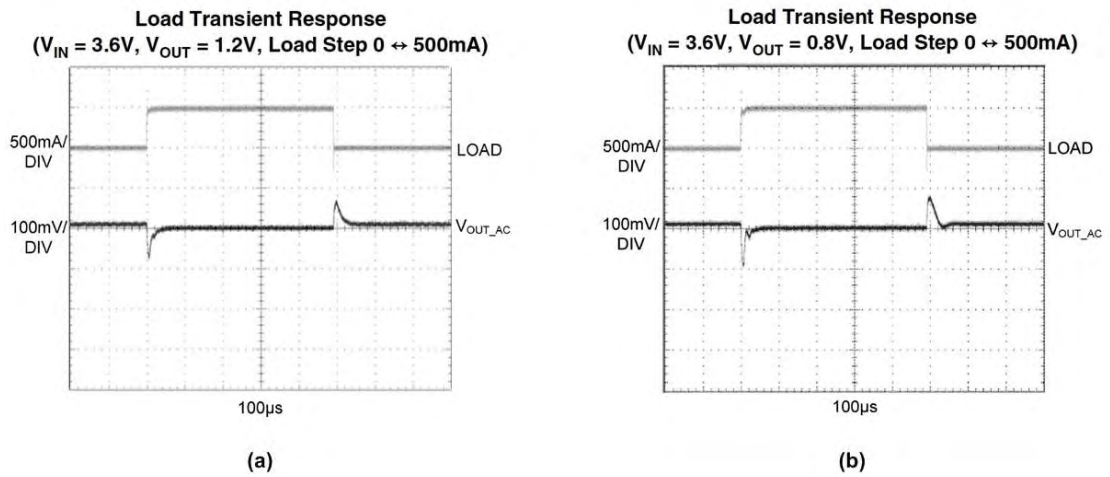

Fig. 1.23: National Semiconductor LM3678 step-down converter output current LOAD and ac-coupled output voltage V_{OUT_AC} waveforms. Load changes from 0 to 500mA and vice versa.

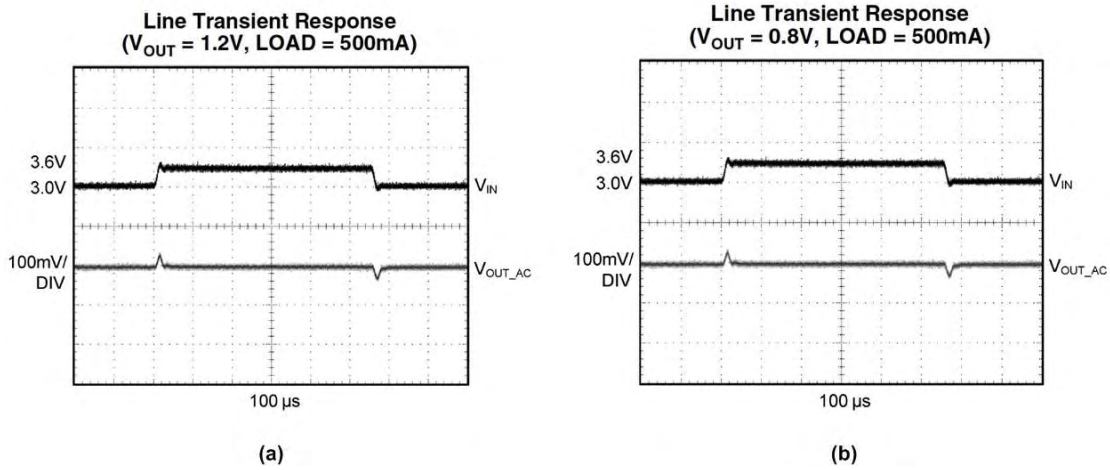

Fig. 1.24: National Semiconductor LM3678 step-down converter input supply voltage V_{IN} and ac-coupled output voltage V_{OUT_AC} waveforms. Input supply voltage changes from 3.0 to 3.6V and vice versa.

1.10 REAL LIFE DC-DC CONVERTER ISSUE - SWITCHING NOISE

As known, any inductor, even parasitic ones, represents a stored energy equal to $E_L=(1/2)LI^2$.

Most of the parasitic inductances that have to be considered are those associated with traces, bond-wires, lead terminations, etc. From an applications point of view, the design needs to be concerned about PCB trace inductances in particular. It is worth to point out that not all PCB trace inductances are trouble-makers. For instance, the traces in series with the inductor L are "benign" because they can be looked at as just being lumped together with the main inductor. A freewheeling path is available for them too, the same as the freewheeling path of the main inductor. However, certain other trace inductances do not have any freewheeling path, and will therefore lead to voltage spikes across the board, as stated by the basic equation $v_L(t)=L(\delta I/\delta t)$. Voltage spikes increase converter noise and ripple and may lead to anomalous and unexpected behavior of control sections of the IC (the so called controller-upset). These traces are considered high-frequency or critical traces from the viewpoint of PCB layout, and their associated inductances are considered to be uncoupled. Even if the parasitic inductance may be small (the rule-of-thumb is 20nH per inch of trace inductance) it can be lethal. For instance, the switching of 1A of current in ns in a 1inch trace will theoretically produce a voltage spike of 20V. A high ($\delta I/\delta t$) occurs in a given trace whenever the current through it is either suddenly forced to zero (from a finite value) or suddenly increased to a finite value (from zero). This may happen during a switch transition, since the main inductor is determining the direction and path of current flow, and this flip-flops between the main charging path and the freewheeling path at every switch transition. Note that even if small parasitic capacitances can help to suppress these spikes, they may not avoid the controller upset. Therefore, besides focusing on layout alone, it is also possible to reduce the noise spikes by slowing down the switching transitions.

BIBLIOGRAPHY

[1] R. W. Erickson and D. Maksimovic, “Fundamentals of Power Electronics (Second Edition)”, Kluwer Academic Publisher, 2004.

[2] National Semiconductor Corporation, “Meeting Power Design Challenges – High-Performance Seminar Series 2007”.

[3] National Semiconductor Corporation, “Knowledge is Power – Power Design Technical Courses 2007”.

[4] National Semiconductor Corporation web-site, http://www.national.com.

[5] Maxim Corporation web-site, http:// www.maxim-ic.com.

CHAPTER 2

A SINGLE-INDUCTOR 4-OUTPUT DC-DC BUCK CONVERTER

The continuous market growth of battery-operated systems and the need of optimizing the power consumption in multi-processors by a dynamic regulation of the supply voltage expand significantly the portable power management market.

In addition to conventional DC-DC devices, [1], there is an increasing need of DC-DC converters capable to generate many outputs while using a single inductor.

The reason is that, when on the same system it is required to generate multiple supply voltages, the increased PCB area, the augmented number of components, and the reduced reliability for the many inductors used, become problematic, [2] and [3].

The new single-inductor 4-output buck converter discussed here gives the solution.

To have multiple outputs it is necessary to time-share the inductor current between

various output loads.

For this reason, the feedback loop that regulates the output voltages becomes a multi-feedback loop, with stability issues and output load and cross regulation constrains.

Moreover, for multiple output architectures, it is necessary to use extra power switches. Then, the cost in terms of reduced efficiency has to be affordable.

In addition, for these kinds of converters, the load switches must separate voltages that may have significantly different values. Therefore, the load switch drivers must account for problems that are specific of the multiple output function.

2.1 SINGLE-INDUCTOR MULTIPLE-OUTPUT BUCK CONVERTER ARCHITECTURE

A DC-DC converter with multiple outputs time-shares the inductor current among the different output loads. Figure 2.1 shows a DC-DC buck converter with M-output.

While a conventional single-inductor single-output buck has just a Pulse Width Modulation (PWM) control for the switches on the supply side (namely MP and MN), the M-output buck uses M additional power switches (namely SW_1, SW_2, ..., SW_M) for the time-sharing of the inductor current.

For a CMOS process, these power switches can be realized with n- channel, p-channel or complementary devices. The choice depends on a trade-off between complexity and cost.

In this kind of system, the regulator foresees M control loops, with as inputs the M output voltage errors defined as $\varepsilon_i = (V_{set,i} - V_{out,i})$.

Assuming a PWM control, the control subsystem, together with the drivers, provides M control signals. One is used to obtain the buck converter switching, and the others (M-1) to divide the clock period into M slots and then to obtain the inductor current time-sharing.

Even if the buck converter operates in the continuous conduction mode, the current I_i, delivered to the C_{oi} output capacitor, is discontinuous, since it goes to zero when the

corresponding load switch opens. Thus, during the discontinuous period, the load current is provided by the output capacitance C_{oi}.

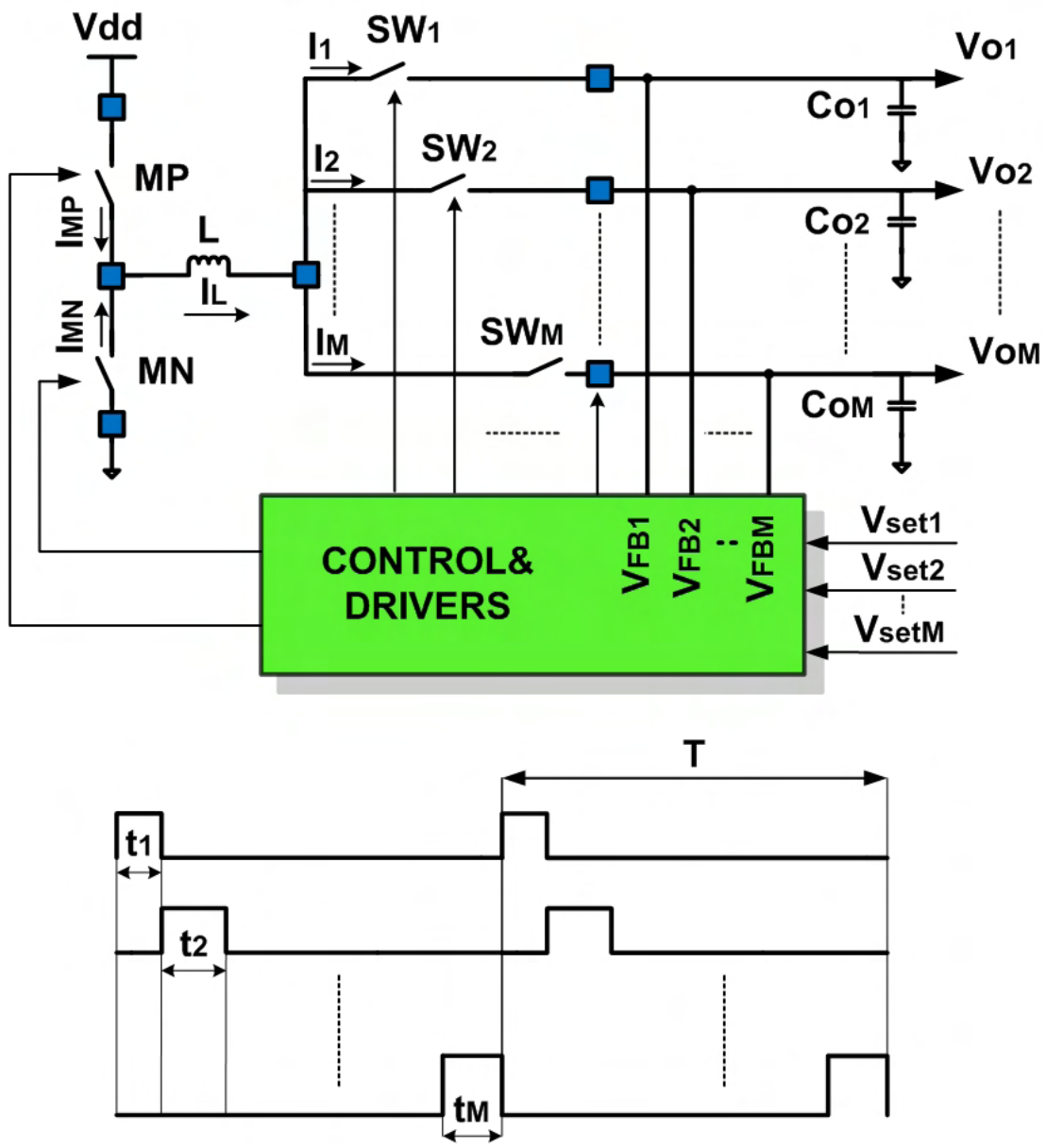

Fig. 2.1: Single-inductor multiple-output buck converter architecture.

2.2 DESIGN TARGETS

The project has been carried out in cooperation with National Semiconductor Corporation Power Management Group. Table 2.1 summarizes the project design targets established to meet actual industrial applications requirements.

The aim of this work is to realize a 4-output buck converter with a supply voltage that can range from 2.3V to 5V, a total output current capability of 1.8A and a single-channel capability of 800mA.

The four output voltages can be independently regulated and can range from 0 to 500mV below the supply voltage.

The switching frequency is 3MHz, while the inductor and the output capacitor sizes are respectively 1uH and 10uF. The used technology is a 0.5µm CMOS process.

Supply Voltage [V]	2.3→5
Output Voltages [V]	0 →(V_{supply} - 0.5)
Outputs	4
(Total) Output Current [A]	0.1 → 1.8
(Single) Output Current [A]	0 → 0.8
Switching Frequency [MHz]	3
Inductor [µH]	1
Output Capacitors [µF]	10
Technology	CMOS 0.5 µm
Substrate Type	p-epi

Tab.2.1: Design targets.

2.3 SINGLE-INDUCTOR 4-OUTPUT BUCK CONVERTER ARCHITECTURE AND DESIGN CONSIDERATIONS

Figure 2.2 shows the conventional PWM voltage mode control (VMC) buck converter. Its operation is well known and has been discussed in Section 1.7.

The output voltage is subtracted to the input voltage setting to obtain the output voltage error, ε. The voltage error is amplified and used as threshold of a saw-tooth signal whose period is the inverse of the switching frequency. The resulting PWM pulse is used to control the power switches.

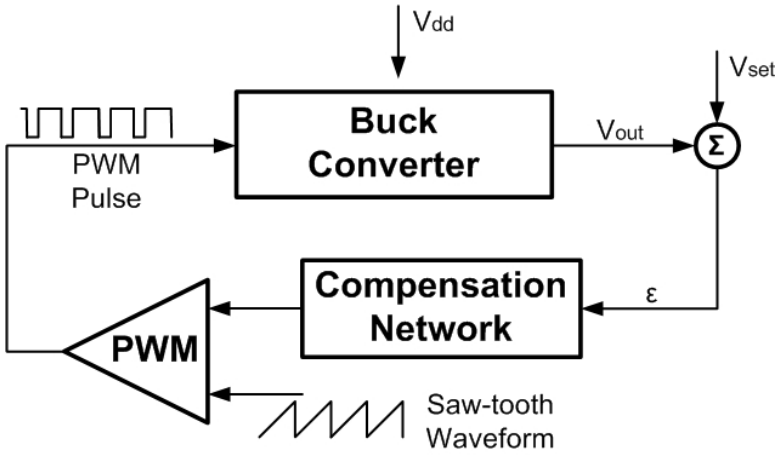

Fig.2.2: Switching regulator closed loop control system.

With four output branches it is necessary to foresee four control loops whose outputs determine four PWM control pulses. Figure 2.3 depicts the overall architecture of the designed single-inductor 4-output DC-DC buck converter.

The high-side and low-side power switches MP and MN obtain the conventional buck structure, while the four n-channel load switches (SW_1, SW_2, SW_3 , SW_4) time-share the inductor current among the four output loads.

In multiple-output DC-DC converters, an important design issue regards the load power switches driving strategy as it affects the overall system effectiveness, in terms of area and power. As already mentioned, there are three possibilities: use of a p-channel, an n-channel or a complementary switch.

The choice depends on the expected regulated voltage, and the cost-efficiency trade off.

If the regulated voltage is relatively large, much higher than the transistor threshold, then the use of a p-channel is a good solution: the overdrive is enough and the series conductance caused by the extra switch can become affordable with a reasonable transistor aspect ratio. As known, the threshold voltage changes because of the body effect and, in order to cancel it, it is necessary to connect the substrate to the source. This is admitted with a single output and n-well technologies, but is not possible with multiple outputs because of the possibility of having the terminal connected to the inductor at a voltage that is the higher than the switched output.

The limit is not negligible because the body effect can worsen the threshold by 100-200 mV and this increases the series resistance significantly.

Another possible solution is to use complementary power switches, but there are limits: the silicon area is almost doubled and the power required to charge and discharge the gate of the power transistors significantly increased. Therefore, complementary switches can be used only for applications with very low current for which the sizing of the power switches is not an issue.

The other possible solution is to use an n-channel transistor that for being properly closed requires a voltage higher than the supply. As known, the request can be satisfied by charge pumps. The switching of one or more pumping capacitances enables reaching the high voltages as required by non-volatile memories. However, the gate capacitance of the power transistor can be as high as 15 pF and the corresponding charge that must be provided leads to area and efficiency issues.

In work, a different approach, named self boosted snubber, ensures to overcome the above limits.

The operation of the self boosted snubber circuit will be described in details in the Section 2.11.

The use of the proposed solution allows using n-channel devices without power efficiency penalties and saving silicon area.

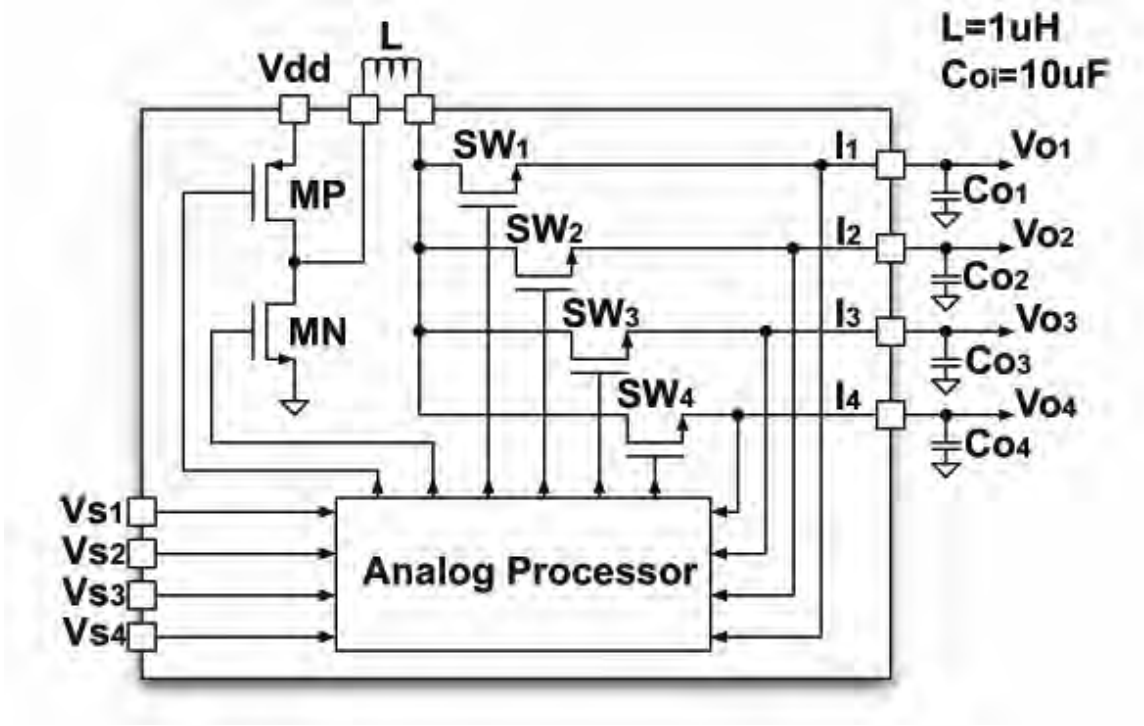

Fig.2.3: Single-inductor 4-output buck converter block diagram.

In a single-inductor 4-output buck converter, the PWM control has to determine the buck switching main duty-cycle and the four inductor current time-sharing slots. So the regulator will process four control equations and the system will manage four control loops with as inputs the four output voltage errors.

When designing a single-inductor multiple-output DC-DC regulator, it is mandatory to ensure simple control and closed-loop stability in each working condition. Also, a low load and cross regulation among the different outputs must be ensured. Therefore, each control loop has to meet both dynamic and static system performance.

The time-sharing of the inductor current can be appreciated in the Figure 2.4, that shows an example of inductor and load switches currents waveforms. When the high-side MP switch is on, the inductor stores energy from the supply and gives energy to the loads. As shown in the Figure, during this time the inductor current rises with positive slopes, depending on which output voltage is connected to the inductor right terminal.

While, when the low-side MN switch is on, the inductor gives energy to the loads and during this time the inductor current falls with negative slopes, depending again on which output voltage is connected to the inductor right terminal.

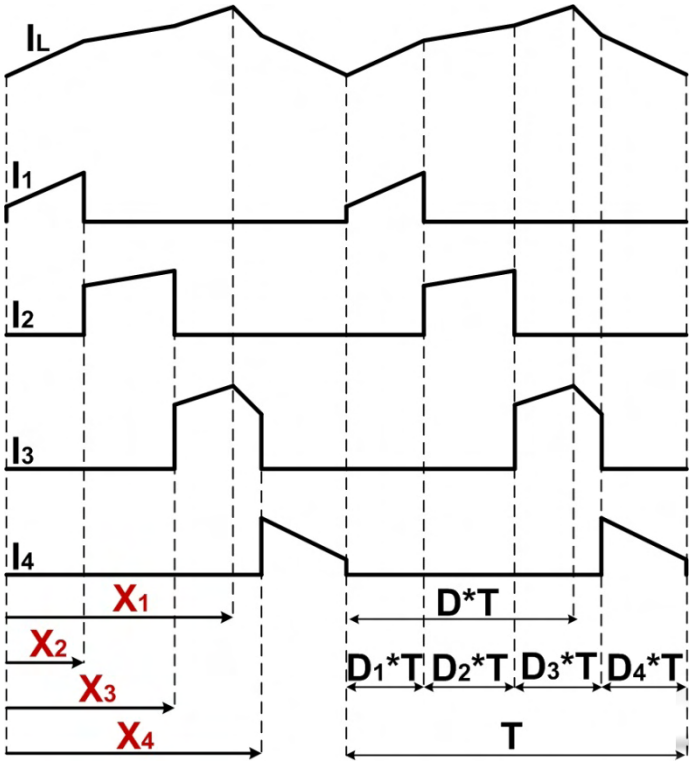

Fig.2.4: Single-inductor 4-output buck converter inductor current time sharing.

A main duty cycle D and 4 sharing duty cycles D_i can be defined. They can be expressed, respectively, as reported below.

$$D=\frac{T_{on,MP}}{T} \tag{2.1}$$

$$D_i=\frac{T_{on,SW_i}}{T}\ , i = 1, 2, 3, 4 \tag{2.2}$$

Therefore, inherently to the PWM control, the regulator must determines the four unknown times X_1, X_2, X_3 and X_4, depicted in Figure 2.4, processing four control equations.

2.4 CONTROL EQUATIONS

As discussed in the previous section, a set of four control equations has to be determinate. The control variables will be the four output voltage errors ε_i (and then the four settling voltages), while the controlled variables will be the four unknown times X_1, X_2, X_3 and X_4. In order to obtain the simplest set of control equations, the idea is to write them as a linear combination of the four voltage errors ε_i as here reported, where k_1, k_2 ,k_3, k_4 are a set of generic gain constants:

$$\begin{cases} X_1 = k_1(a_{11}\varepsilon_1 + a_{12}\varepsilon_2 + a_{13}\varepsilon_3 + a_{14}\varepsilon_4) \\ X_2 = k_2(a_{21}\varepsilon_1 + a_{22}\varepsilon_2 + a_{23}\varepsilon_3 + a_{24}\varepsilon_4) \\ X_3 = k_3(a_{31}\varepsilon_1 + a_{32}\varepsilon_2 + a_{33}\varepsilon_3 + a_{34}\varepsilon_4) \\ X_4 = k_4(a_{41}\varepsilon_1 + a_{42}\varepsilon_2 + a_{43}\varepsilon_3 + a_{44}\varepsilon_4) \end{cases} \tag{2.3}$$

As shown by the system of equations (2.4), if the DC loop-gain is high enough, the effect of the feedback is to null each error combination, thus leading to the proper four steady-state times $\overline{X_1}$, $\overline{X_2}$, $\overline{X_3}$ and $\overline{X_4}$:

$$\begin{cases} a_{11}\varepsilon_1 + a_{12}\varepsilon_2 + a_{13}\varepsilon_3 + a_{14}\varepsilon_4 = 0 \\ a_{21}\varepsilon_1 + a_{22}\varepsilon_2 + a_{23}\varepsilon_3 + a_{24}\varepsilon_4 = 0 \\ a_{31}\varepsilon_1 + a_{32}\varepsilon_2 + a_{33}\varepsilon_3 + a_{34}\varepsilon_4 = 0 \\ a_{41}\varepsilon_1 + a_{42}\varepsilon_2 + a_{43}\varepsilon_3 + a_{44}\varepsilon_4 = 0 \end{cases} \rightarrow \begin{cases} X_1 \rightarrow \overline{X_1} \\ X_2 \rightarrow \overline{X_2} \\ X_3 \rightarrow \overline{X_3} \\ X_4 \rightarrow \overline{X_4} \end{cases} \tag{2.4}$$

To ensure meaningful solutions, the control equations must be independent and then the determinant of the system characteristic matrix A must not be 0:

$$\det(A) = \det\begin{pmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ a_{41} & a_{42} & a_{43} & a_{44} \end{pmatrix} \neq 0 \tag{2.5}$$

Imposing this condition is possible to determine the control equation coefficients.

Therefore, the various used solutions differ because of the utilized matrix A. Obliviously, simple coefficients and a reasonable control sequence has to be chosen in order to achieve a realizable control circuit.

Even if from the mathematical point of view exist several characteristic matrixes that satisfy the previous condition, the chosen solution, here reported, represents the best trade-off between complexity and effectiveness.

$$\overline{A}=\begin{pmatrix} +1 & +1 & +1 & +1 \\ +1 & -1 & -1 & -1 \\ +1 & +1 & -1 & -1 \\ +1 & +1 & +1 & -1 \end{pmatrix} \tag{2.6}$$

This particular coefficients choice is also justified by an intuitive view that it will be illustrated in the next paragraph.

2.4.1 CONTROL EQUATIONS INTUITIVE VIEW

Consider for example the waveform relative to the first unknown time X_1.

If $\Delta(\varepsilon_1+\varepsilon_2+\varepsilon_3+\varepsilon_4)$ is higher than 0, it means that the whole system needs more energy. Then the time X_1 should increase.

While if $\Delta(\varepsilon_1+\varepsilon_2+\varepsilon_3+\varepsilon_4)$ is less than 0, it means that the whole system needs less energy. Then the time X_1 should decrease. It can be noted that this is consistent with the first control equation.

Consider now the waveform relative to the second unknown time X_2.

If $\Delta\varepsilon_1-\Delta(\varepsilon_2+\varepsilon_3+\varepsilon_4)$ is higher than 0, it means that the first output channel needs more energy. Then the time X_2 should increase.

While if $\Delta\varepsilon_1-\Delta(\varepsilon_2+\varepsilon_3+\varepsilon_4)$ is less than 0, it means that the first output channel needs less energy. Then the time X_2 should decrease. It can be noted that this is consistent with the second control equation.

The same hold for the other control equations.

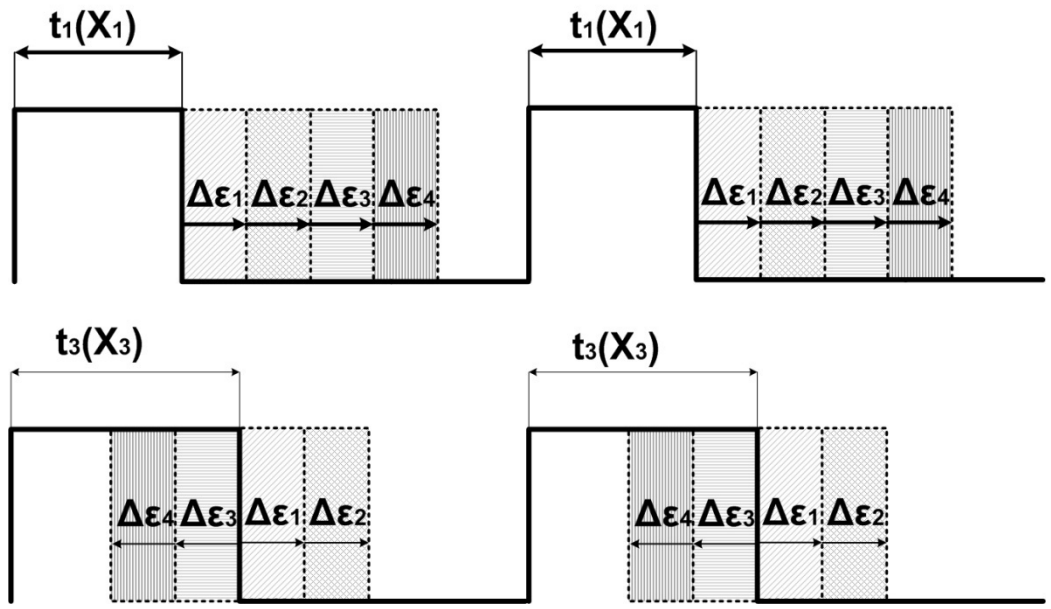

Fig.2.5: Single-inductor 4-output control equation intuitive view.

2.5 SINGLE-INDUCTOR 4-OUTPUT CLOSED LOOP CONTROL

The conceptual scheme of the proposed closed loop VMC system that follows from the previous considerations is shown in Figure 2.6, together with the four PWMs output pulses.

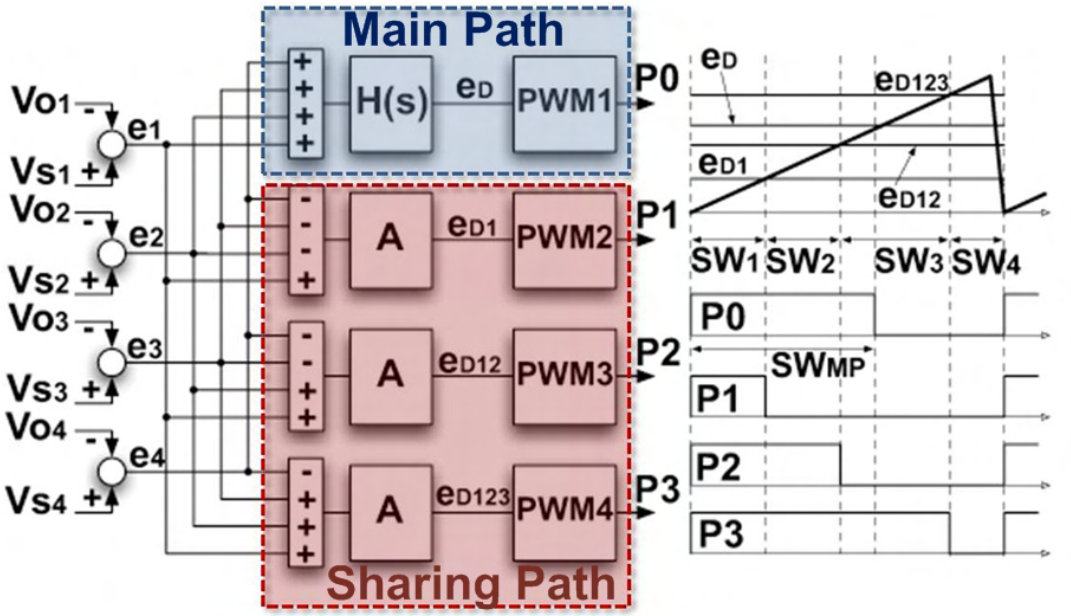

Fig.2.6: Conceptual scheme of the single-inductor 4-output closed loop control system.

It consist of a main path that controls the high-side and low-side main power switches MP and MN, and three sharing paths that manage the sharing of the inductor current controlling the load power switches SW_i.

Since only the main path loop "sees" the two poles due to the external inductor and the output capacitors, only the main path needs frequency loop compensation.

Therefore H(s) in the main path is a first-order zero-pole filter that achieve the loop compensation, while A blocks in the sharing paths are just amplifiers.

2.6 SINGLE-INDUCTOR 4-OUTPUT SYSTEM BLOCK DIAGRAM

The previous considerations lead to the overall system block diagram shown in the Figure 2.7.

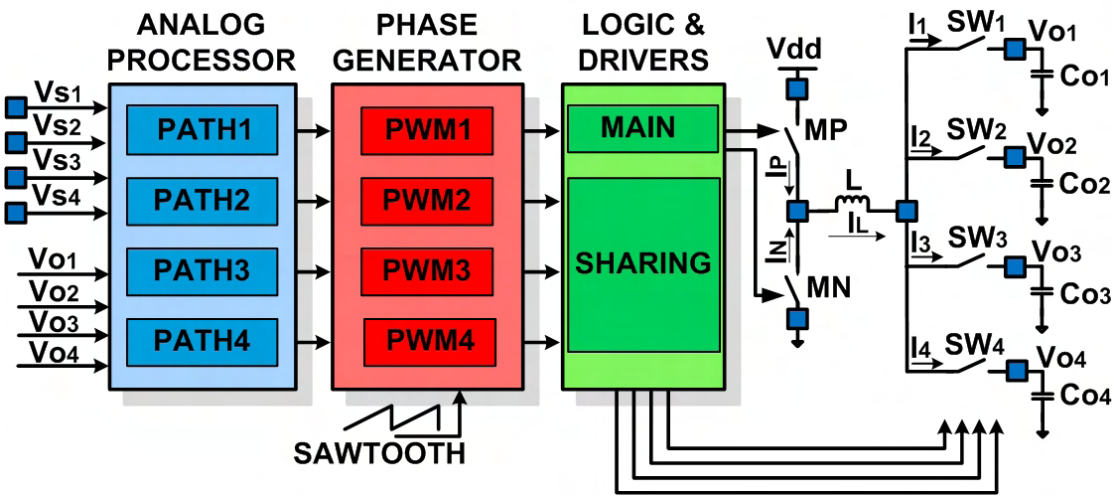

Fig.2.7: Single-inductor 4-output system block diagram.

As it was said before, the four control paths process the four output voltage errors and generate four control voltages. Then the phase generator process the four control voltages leading to four control phases.

The following digital logic, together with the main and the sharing drivers, combines the control phases and obtains the proper power switches driving phases that drive the buck power stage.

In order to minimize the number of the active stages and then the system quiescent power consumption, the analog processor has been realized by a switched-capacitor discrete-time circuit that achieves the error combinations given by the control equations as well as other functions. The PWMs has been realized with continuous-time comparators.

2.7 DISCRETE-TIME ANALOG PROCESSOR - MAIN PATH

The main processing channel shown in the Figure 2.8 consists of three sections.
The first section combines the errors with the proper sign and provides the gain, while the second section is the first order zero-pole filter.
The branch including C_5 and V_b achieves a DC level shift of the error combination. Then, the flip-around double sample-and-hold decouples the filter from the PWM, thus limiting the kickback from the switching part. It also and eliminates the glitches produced by switching from phase 1 to phase 2.
The other channels only have two sections: one is an amplifier that processes the errors by providing a gain and shifting the DC level, and the other is the sample-and-hold.

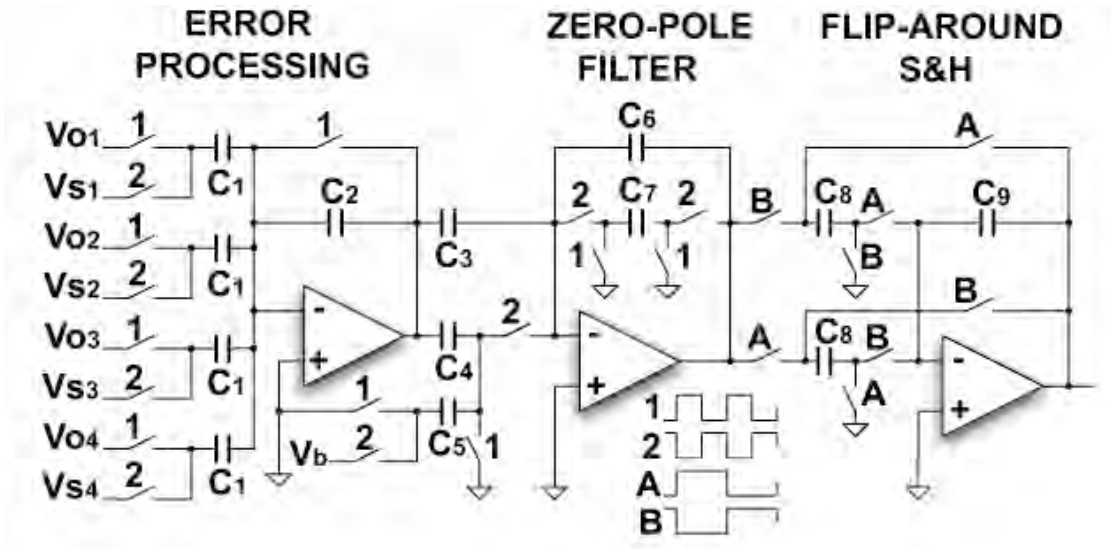

Fig.2.8: Discrete-time analog processor – Main path.

The unity capacitance used in the SC processors is 100fF.
The Operational Transconductance Amplifiers (OTAs) are based on a conventional two-stage architecture with switching-pole splitting compensation. The two stage topology has been preferred in order to achieve the maximum output voltage range.

With regard to the error processing OTAs, it can be noted that frequency compensation is needed only during phase 1 (when the feedback factor is 1), while, during the phase 2, the feedback factor compensates the operational amplifier by strongly reducing its bandwidth.

Then, as shown in Figure 2.9, a switching compensation have been implemented, decreasing the required quiescent current of each op-amp. During phase 1, the switch is closed and the larger capacitor C1 achieves the pole-splitting effect. While, during phase 2, the combined effect of the feedback factor and the smaller capacitor C2 provide the proper phase margin.

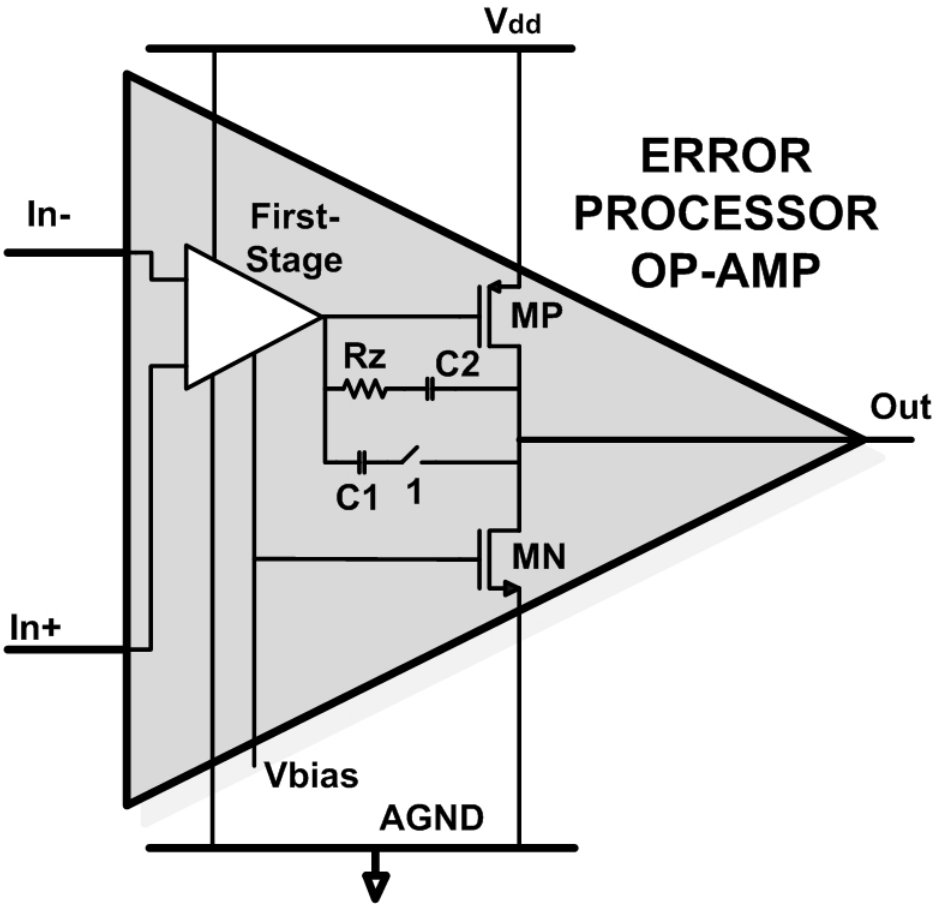

Fig.2.9: Switching compensation of the error processor op-amp.

Thanks to the Correlated Double Sampling technique, the first-stage input voltage offset is compensated and the operational amplifier 1/f noise is reduced.

In order to reduce the thermal noise, the operational amplifier input pair has been realized with n-channel transistors. The switches KT/C noise is pretty low too.

2.8 PWM MODULATOR

The PWM modulator is realized by a continuous-time comparator with common mode feedback, a saw-tooth generator, a monostable multivibrator and a enabled JK flip-flop, as shown in Figure 2.10.

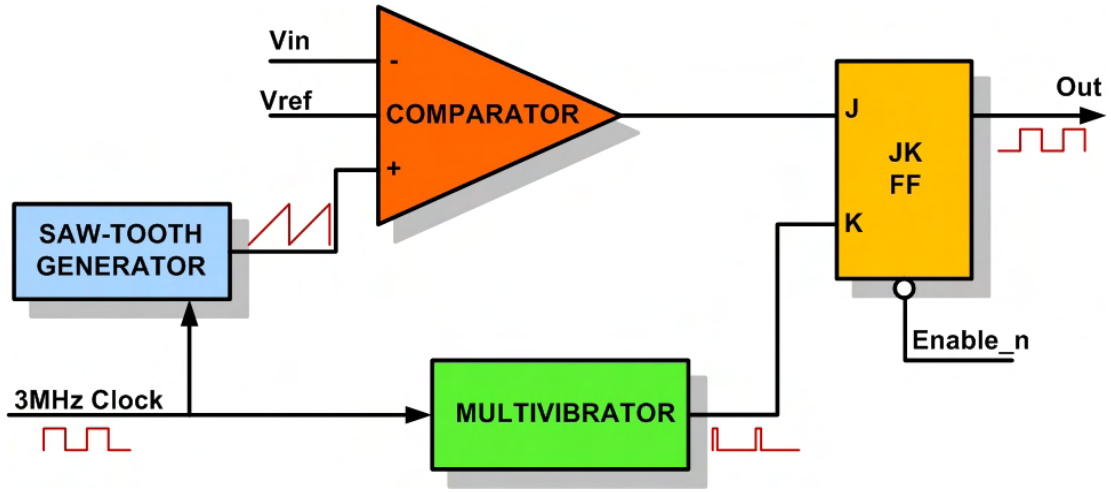

Fig.2.10: Single-inductor 4-output PWM modulator circuit.

At the start of each clock cycle, the multivibrator output digital pulse resets the output of the JK flip-flop to the low logic level 0.

When the PWM input voltage, V_{in}, crosses the saw-tooth waveform, the output of the comparator goes to the high logic level 1 and sets the FFJK output to the high logic level 1, thus obtaining the PWM control pulse. The frequency of the saw-tooth waveform and multivibrator pulses is 3MHz.

The PWM comparator has been realized using a n-channel differential gain stage with resistive loads followed by a inverter chain. This configuration achieves high speed together with a pretty low power consumption.

As it can be noted in the Figure 2.11, a continuous-time common mode feedback has been added to improve the comparator performance.

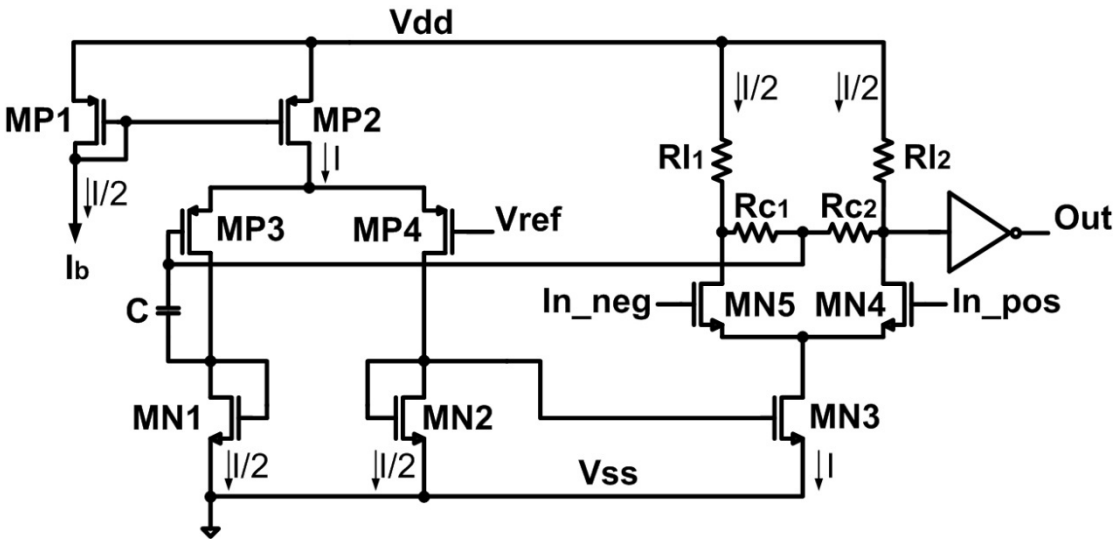

Fig.2.11: Comparator with CMFB circuit used in the PWM modulator.

When the comparator common mode voltage differs from the reference voltage V_{ref}, the CMFB circuit adjusts the input pair tail current and then the comparator common mode voltage. Figure 2.12 shows the monostable multivibrator circuit.

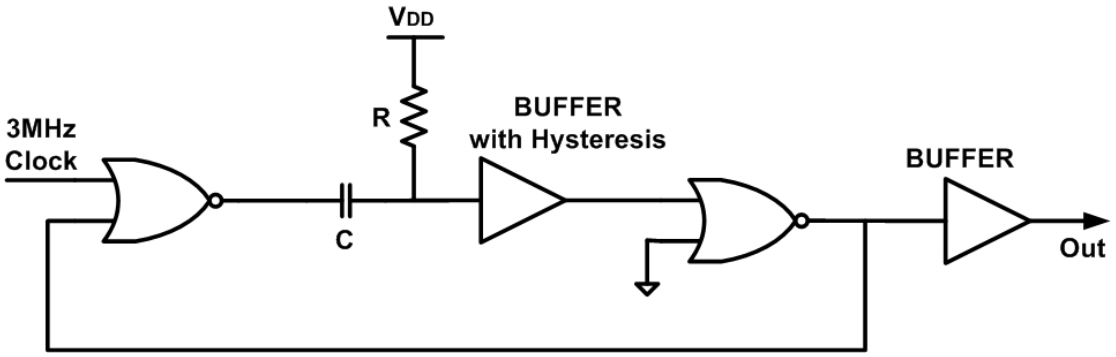

Fig.2.12: PWM modulator monostable multivibrator.

As known from the theory, the RC product fixes the duration of the output digital pulses:

$$\Delta t_{pulse} = R \cdot C = 6.06K \cdot 1.6pF = 9.6ns \quad (2.6)$$

The buffer with hysteresis, placed before the second NOR gate, avoids spurious output pulses due to the resistance and capacitance noise.

2.9 MAIN DRIVER AND SHARING LOGIC CIRCUITS

Figure 2.13 shows the main driver circuit. In order to avoid high shoot-through current spikes during buck commutations, the main driver senses the gate voltage of the high-side and low-side power switches, MP and MN, and provides a time disoverlap between the two driving phases, as shown in Figure 2.14.

This circuit reduces also the switching voltage spikes issues due to the parasitic bonding inductances of the ground and power supply pads.

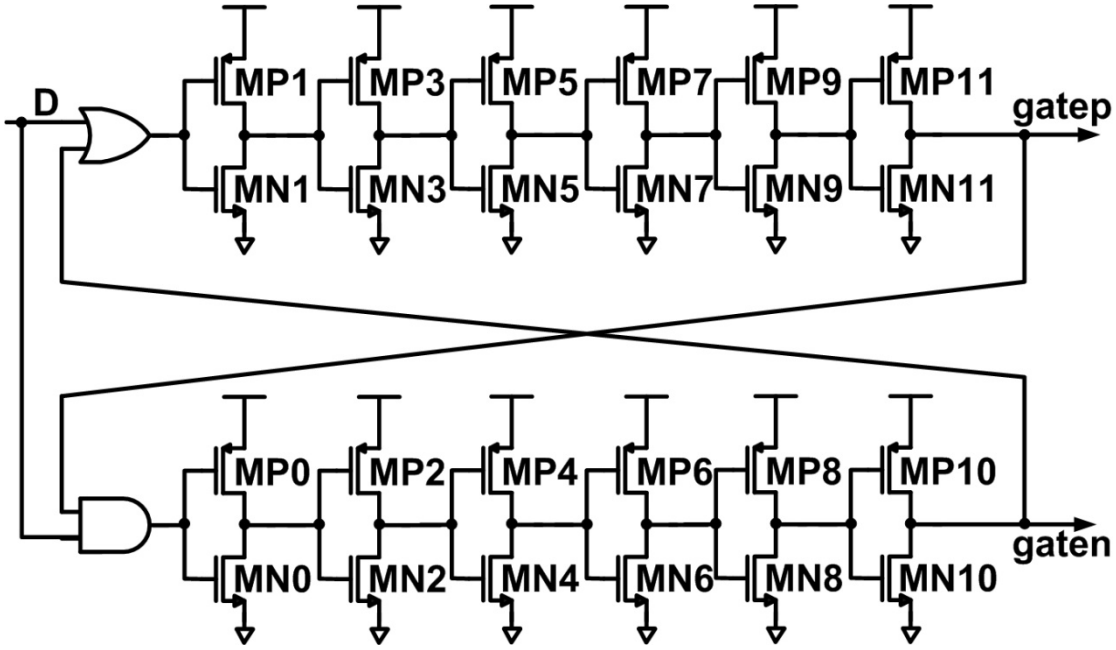

Fig 2.13: Main driver circuit.

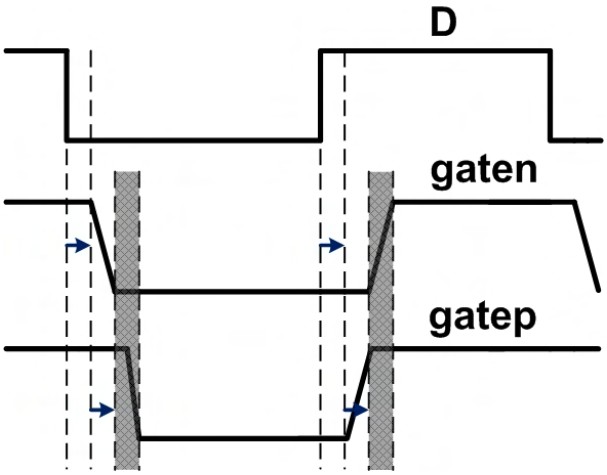

Fig 2.14: Main driver input and output phases.

The sharing logic provides the four load switching driving phases combining the four PWM control pulses.

The digital feedback loops avoid short-circuits among different outputs during the inductor current time-sharing commutations. Hence, the feedback senses the load switches gate voltages and achieves a time-disoverlap between their driving phases.

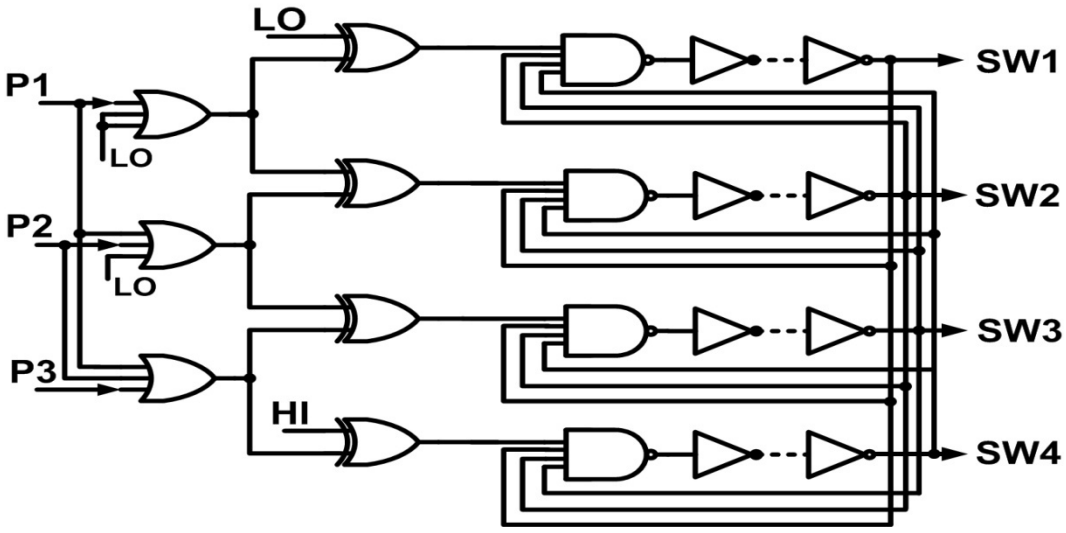

Fig 2.15: Main driver output phases.

As shown by the Figure 2.15, the time disoverlap is provided by the gate time delays in the digital feedback paths.

2.10 POWER STAGE AND OUTPUT SWITCHES DRIVING STRATEGY

The Figure 2.16 shows the buck converter power stage together with the external inductor and output capacitors.

All the power transistors has been realized with the minimum channel length of 0.5µm. The high-side PMOS transistor is 300mm wide while the low-side NMOS transistor is 60mm wide.

As it was said before, in this work the use of n-channel MOS load switches has been preferred in order to save system area. These load NMOS transistors are 30mm wide.

In addition, since the output voltage can range up to 500mV below the supply voltage, the load switches need boosted driving phases with the intention of ensure low load switches on-resistance.

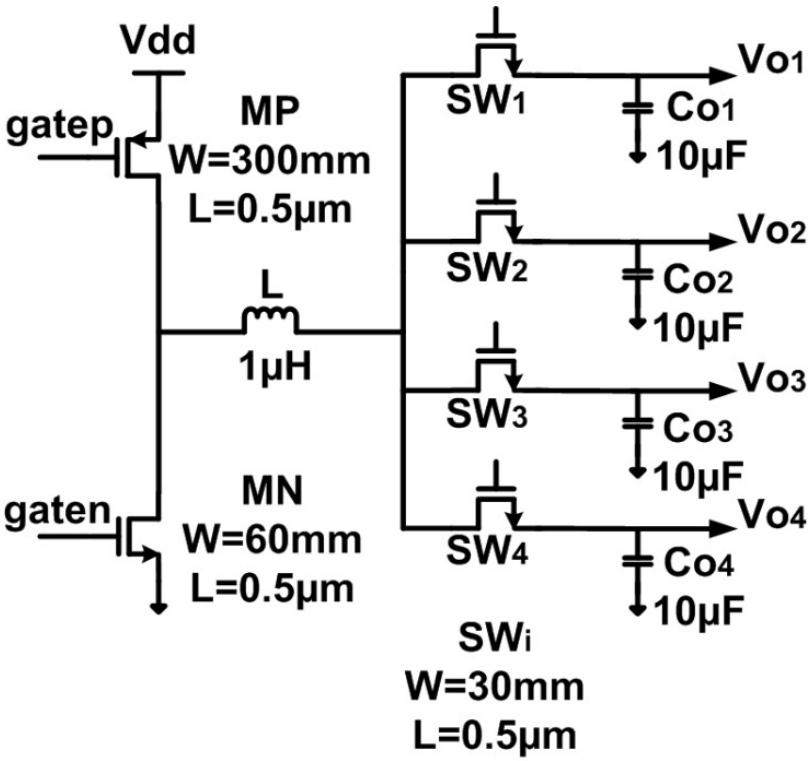

Fig 2.16: Single-inductor 4-output buck converter power stage.

The adopted solution proposes a new circuit that has been called self-boosted snubber circuit since it combines two features:

- ❖ It protects the right terminal of the inductor during the sharing commutations against the switching voltage spikes.
- ❖ It provides boosted load switching driving phases recycling the inductor current during the disoverlap times.

Therefore this solution does not require extra power from the input supply.

2.11 SELF-BOOSTED SNUBBER CIRCUIT

As shown in Figure 2.17, the self-boosted snubber circuit is realized by a integrate diode D, two capacitors (C_{int} internal and C_{ext} external), four conventional voltage doublers charge pumps (cp) and four inverter stages.
ESD pads clamp the load switches gate voltages to around 5V also protecting them against the switching voltage spikes.

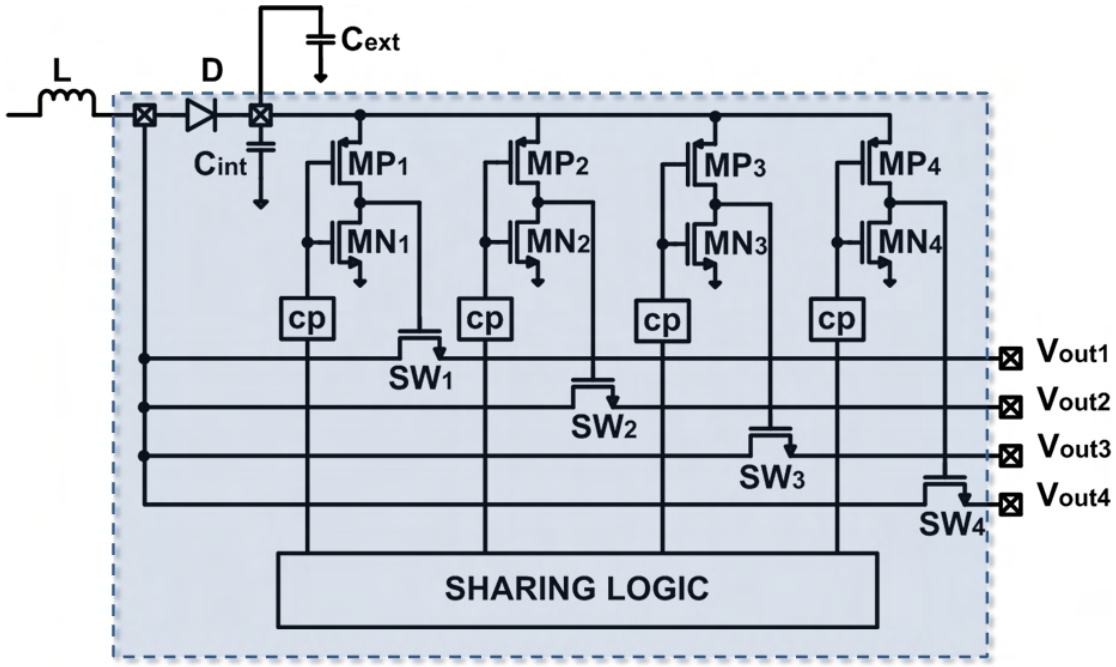

Fig 2.17: Single-inductor 4-output self-boosted snubber circuit.

Consider for instance the case in which all the switches are off.

The only path available for the inductor current is toward the diode and the snubber capacitors. Therefore the inductor current start to charge these capacitors with an almost constant voltage slope. Consequently, the voltage of the inductor right side starts to rise linearly followed by the snubber capacitor top plates, as shown in Figure 2.18.

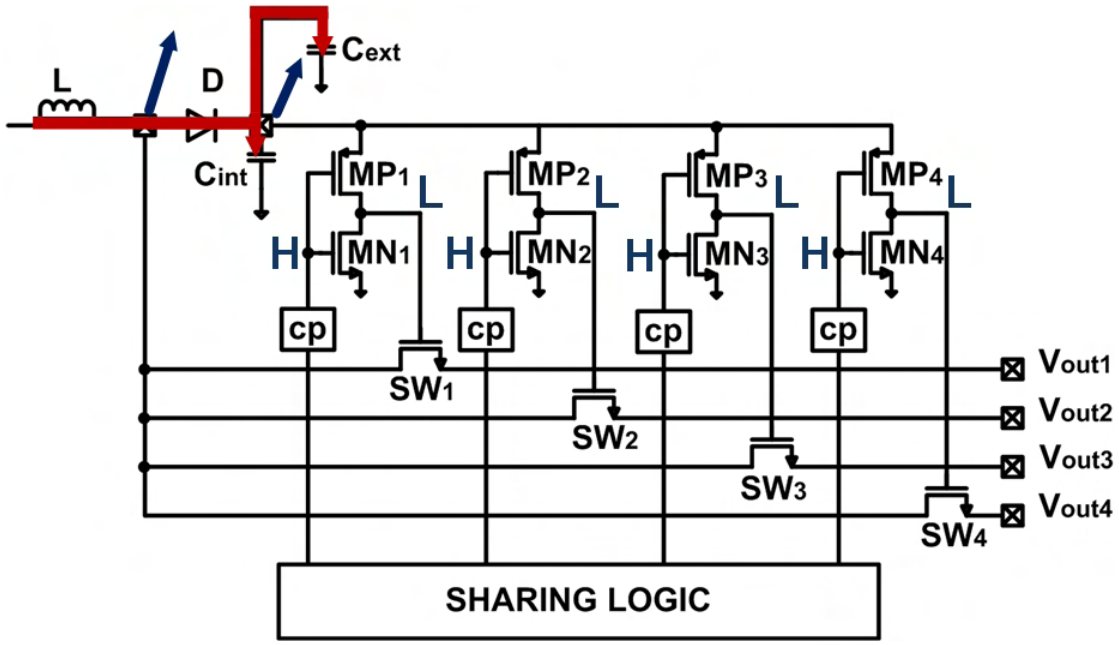

Fig 2.18: Self-boosted snubber circuit - phase (a).

When the digital logic pull down the MN2 gate, MP2 turns-on and the snubber capacitors share their charge with the SW2 parasitic gate capacitance.

Therefore the gate voltage starts to increase following the snubber capacitors top-plate voltage, as shown in Figure 2.19.

Then the SW2 load switch turns-on and the inductor current starts to flow towards the second output branch. The Diode D is now off and the snubber capacitors sustain the SW2 gate voltages, as shown in Figure 2.20.

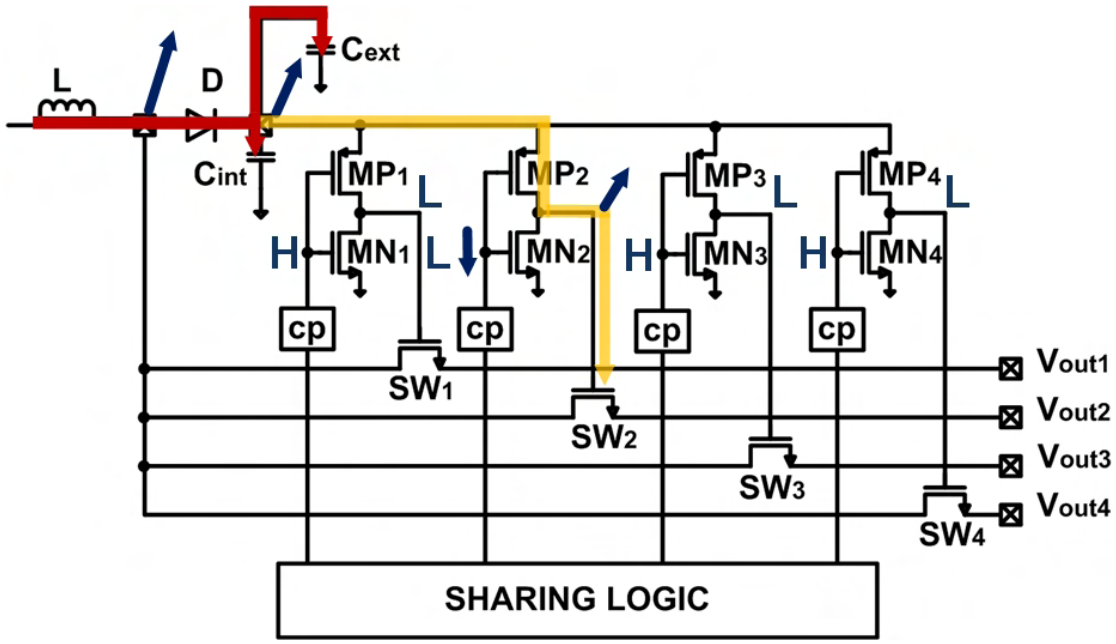

Fig 2.19: Self-boosted snubber circuit – phase (b).

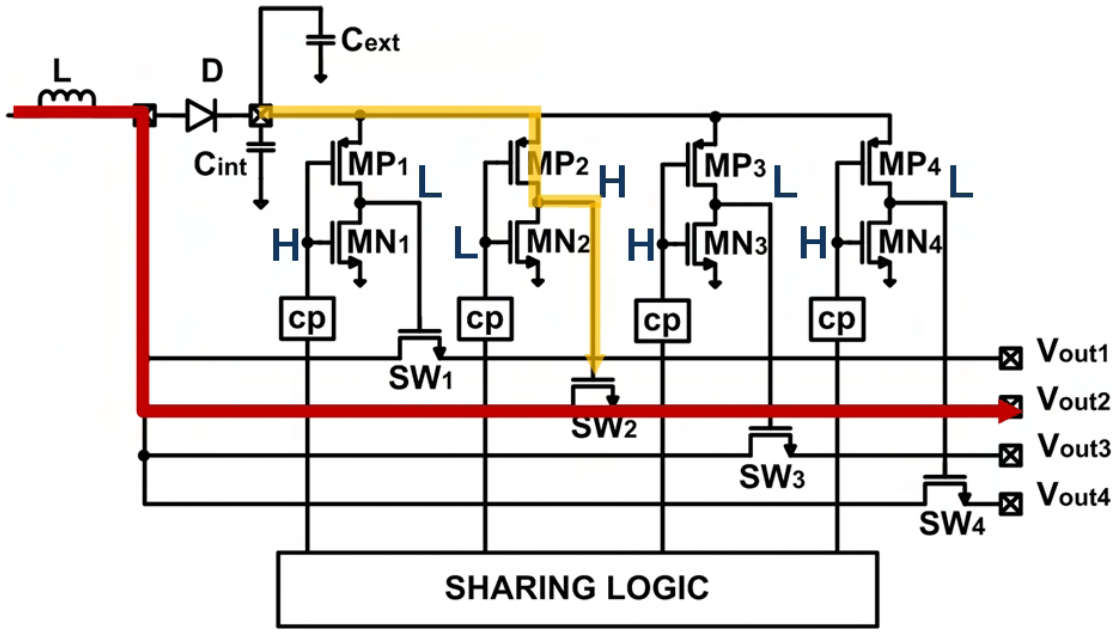

Fig 2.20: Self-boosted snubber circuit – phase (c).

2.12 SINGLE-INDUCTOR 4-OUTPUT LAYOUT CONSIDERATIONS

In order to obtain IC full functionality, the layout of a switching DC-DC converter is as important as the transistor-level design.

The main issue is due to the fact that, in this kind of systems, on the same low-resistive substrate (for the used technology a p-epi substrate) there are quiet analog sub-circuit (e.g control circuit, current and voltage bias references…) together with noisy digital logic, drivers and switching power transistor.

Switching power transistors inject high current spikes leading to noise coupling between analog and switching parts. This may cause the so called ground bounce which in turn can lead to controller upsets.

Therefore, in order to mitigate this problem, the common followed strategies are:

1) If it is available in the used process, place switching power MOS transistor in a isolated p-well.
2) Physically separate the analog from the switching part placing them as far as possible (obliviously without waste silicon area).
3) Provide a separate low-impedance path from the switching part substrate connection to IC ground pin.
4) Use guard rings or deep n-well tranches in order to increase the resistance between analog and switching substrate.

Since in the used process the p-well is not provided, only the strategies 2), 3), 4) have been followed when drawing the layout.

Figure 2.21 shows the layout of the SIMO buck converter. Analog and power switching part have been highlighted together witch each respective ground pin.

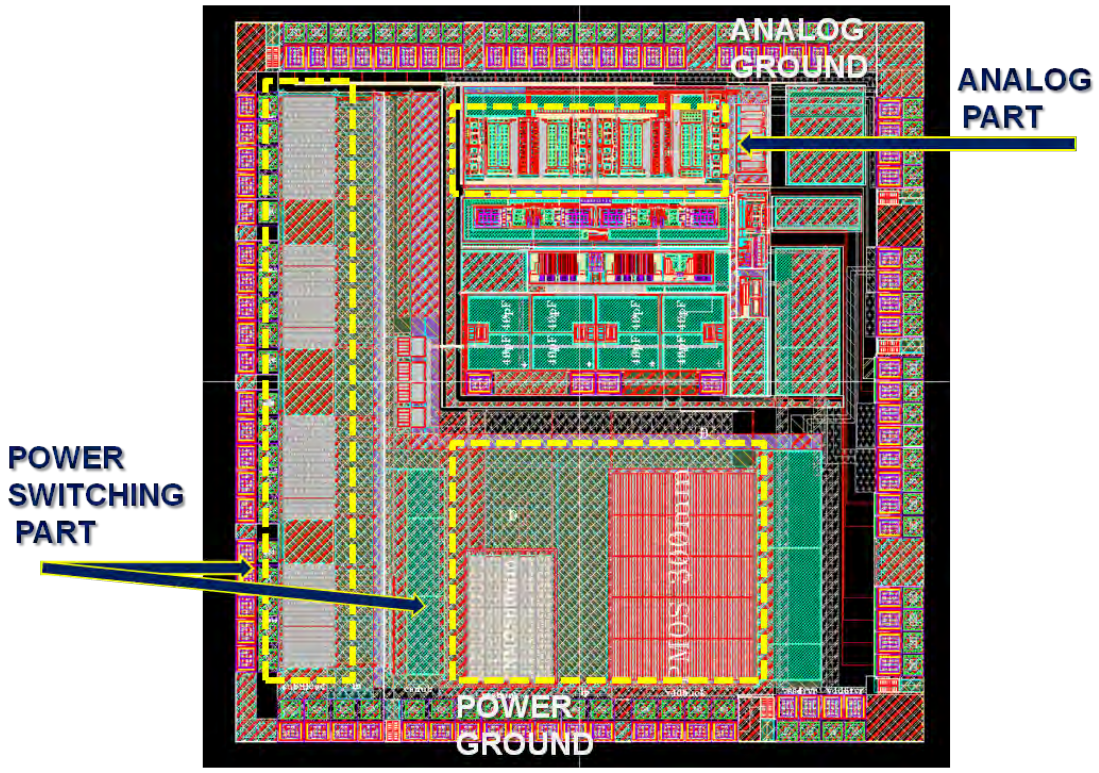

Fig 2.21: Single-inductor 4-output buck converter top level layout.

Another aspect that has to be taken into account is the parasitic resistances of the switching converter power train.

In order to do not degrade the heavy load system power efficiency, it is necessary to minimize the parasitic resistance of the metal traces connecting the power MOS devices to each IC pin. This has been achieved placing multiple power pins as close as possible to the power MOS drain and source connections and using stacked metal trace for routing.

Moreover, in order to make the power MOS devices current density as uniform as possible to minimize the switch on-resistance, drain and source metal connections have been drawn as in Figures 2.22 for main power transistors (MP and MN) and as in Figure 2.23 for each load power devices (SW_1, SW_2, SW_3 and SW_4).

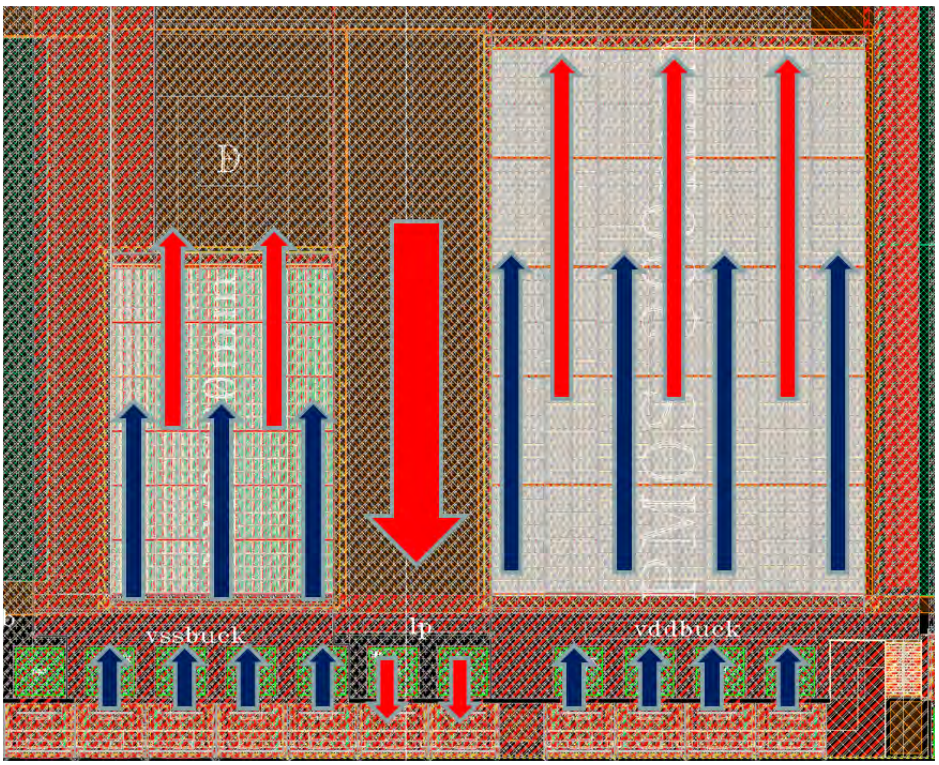

Fig 2.22: Single-inductor 4-output buck converter main switches layout.

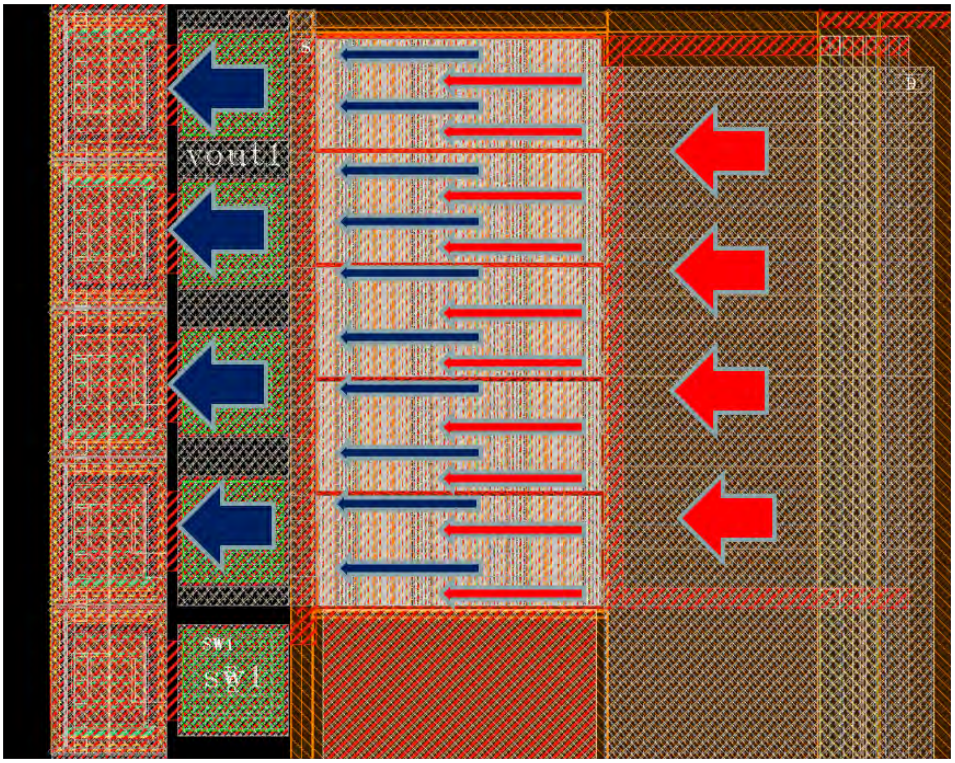

Fig 2.23: Single-inductor 4-output buck converter load switches layout.

2.13 SINGLE-INDUCTOR 4-OUTPUT IC PROTOTYPE

The Figure 2.24 shows the microphotograph of the chip. A 0.5um gate length process with 5 metals and 2poly has been used. The active area is 3.5mmx3.8mm.

It is possible to note the control circuit, the high-side and low-side MP and MN switches and the load switches SW_i.

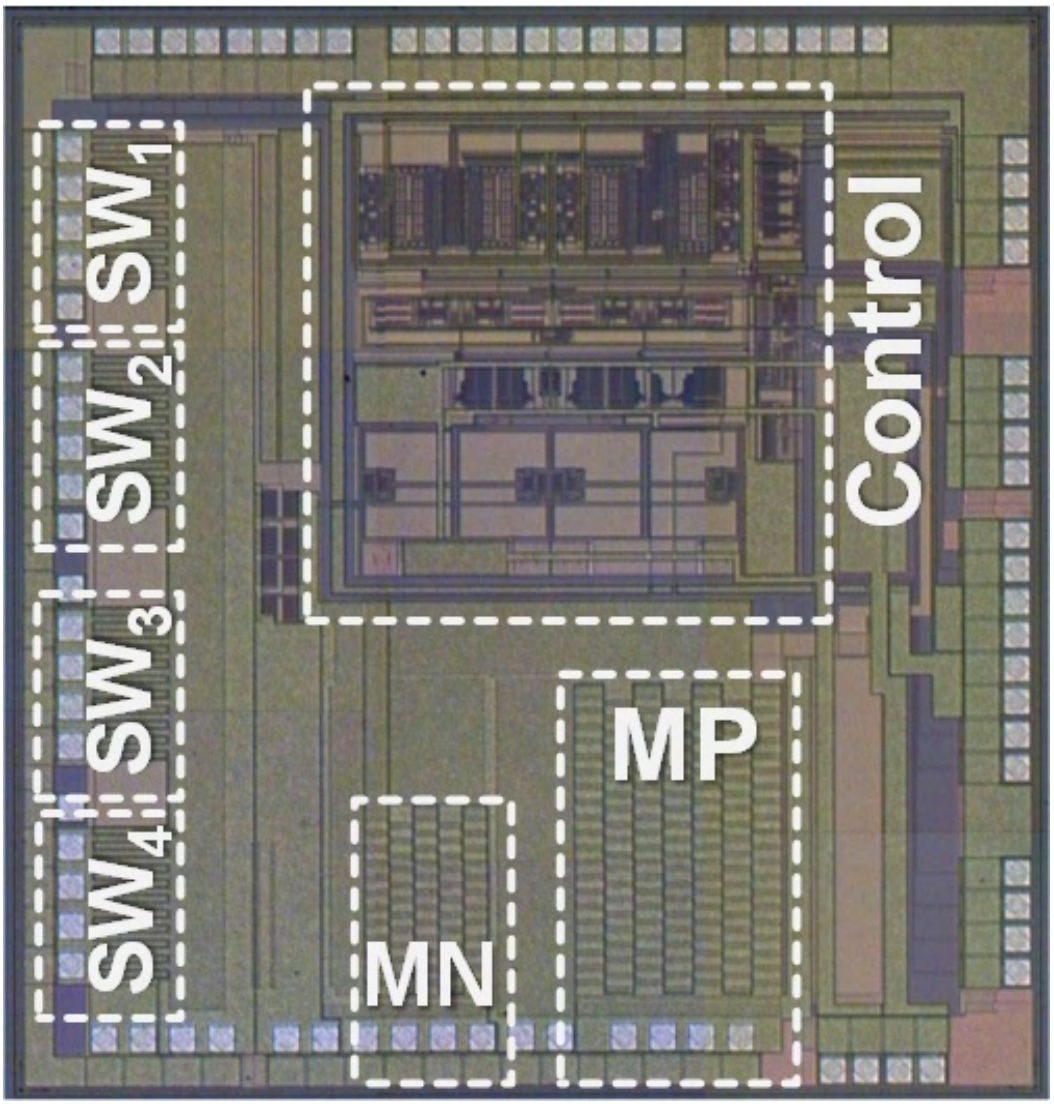

Fig 2.24: Single-inductor 4-output prototype microphotograph.

2.14 SINGLE-INDUCTOR 4-OUTPUT TEST PCB

In order to obtain a working prototype, a good design of the switching power converter PCB is mandatory.

In particular, with regard to the switching regulators PCB design, the basic rule to follow is that every AC path in the board is considered critical, whereas any DC path is not.

Indeed, stray inductances in the AC current paths can induce large voltages spikes, which couple into sensitive circuitry increasing the output voltage ripple and causing controller upsets (circuit performance anomalies).

On the other hand, lines carrying DC currents seldom leads to problems, because DC currents does not cause voltage spikes or couple AC to other traces.

Therefore the stray inductance of any AC current paths must be minimized reducing the area of the AC current loops. With regard to the buck topology, the critical AC path traces are shown bold in Figure 2.25.

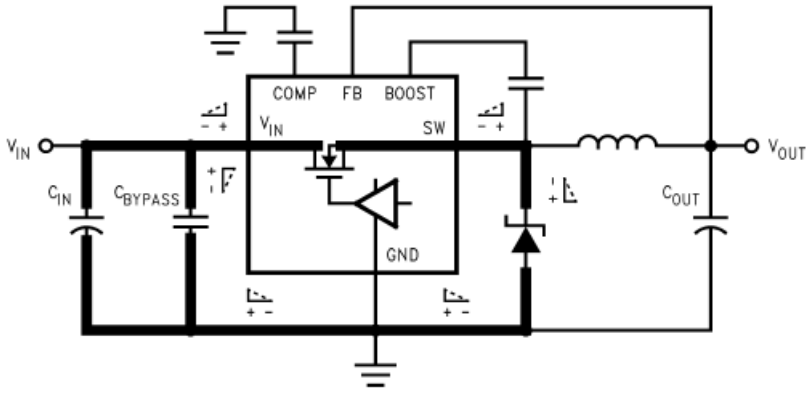

Fig 2.25: Single-inductor single-output buck converter AC current loop.

Then, the first mandatory rule is to place the input bypass capacitor as close as possible to the IC supply and ground pins.

Another issue that has to be taken in account is the so called ground bounce.

Any small but abrupt change in the ground pin can induce ground plane voltage drops that depend on the local ground plane resistance.

The solution is to run separate ground shapes on a layer (e.g. top layer) "single-point connected" with a quiet ground plane (e.g. middle layer).

Finally, with regard to the DC current path, in order to preserve the overall system power efficiency, the parasitic resistances of that traces that carry high currents must be minimized and multiple via have to be used.

The Figure 2.26 shows the single-inductor 4-output test PCB. 4-layers have been provided. The top layer is red while the bottom layer is blue.

The middle1 (analog ground plane) and middle2 (digital ground plane) layers are not shown. The power and the analog top ground planes, the star connected input power supply traces and the four output voltage traces can be noted.

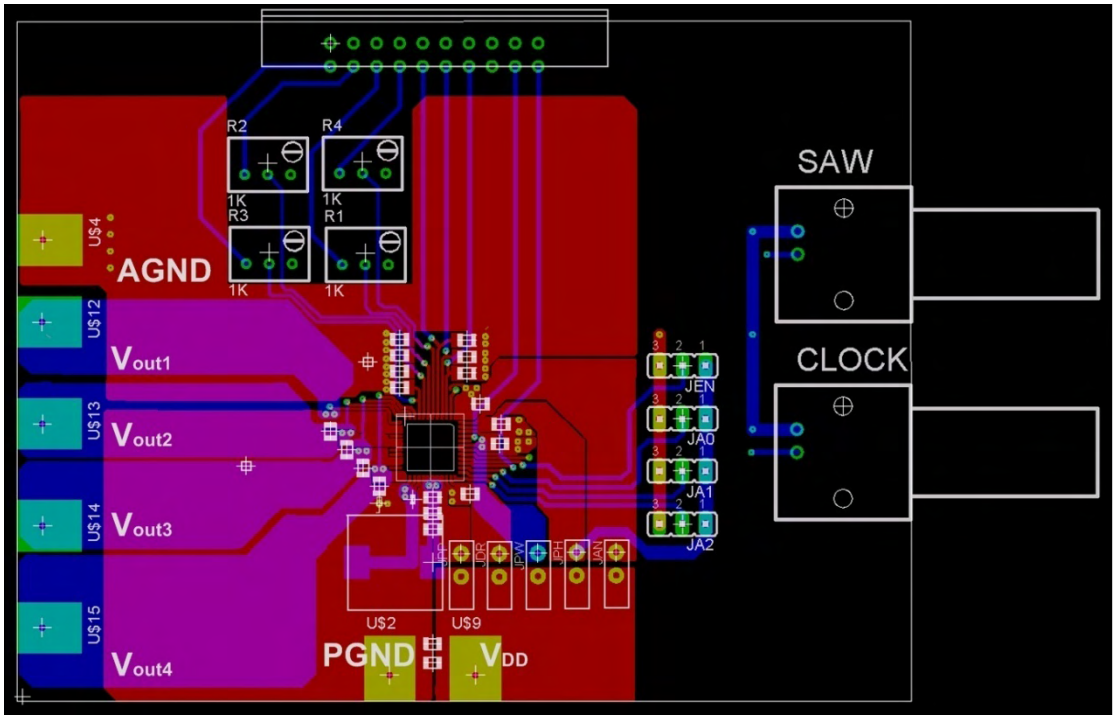

Fig 2.26: Single-inductor 4-output prototype test PCB.

With regard to the previous consideration, in the Figure 2.27 the input bypass capacitor and the single point connection between the different ground plane have been highlighted.

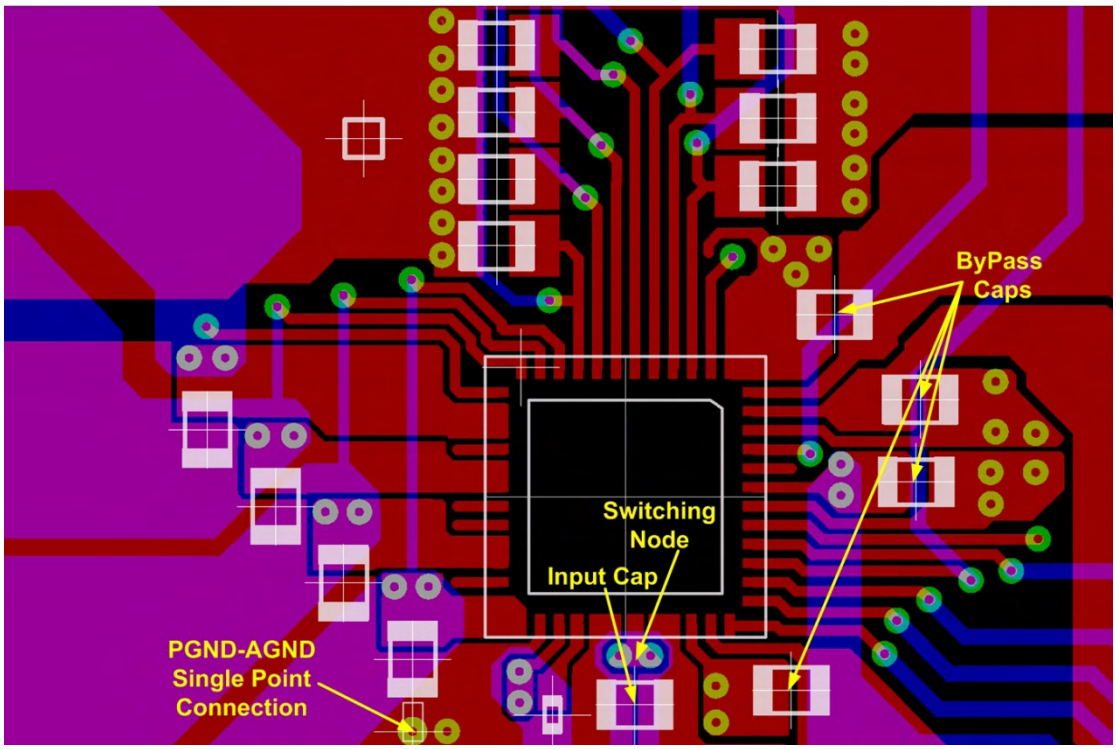

Fig 2.27: Single-inductor 4-output prototype test PCB - details.

2.15 SINGLE-INDUCTOR 4-OUTPUT MEASUREMENTS

This Section depicts the measurements results.

The Figure 2.28 shows 3 of the 4 output voltages (V_{out2} = 1.0V, V_{out3} = 1.2V, V_{out4} = 1.4V), and the switching node voltage waveforms in the steady-state.

The output currents are respectively 200mA, 240mA and 300mA. The first output voltage, not shown, V_{out1} = 1.6V while Iout1 = 350mA.

It can be noted from the switching node voltage waveform a good stability of the main loop. The main duty in this case is about 60%.

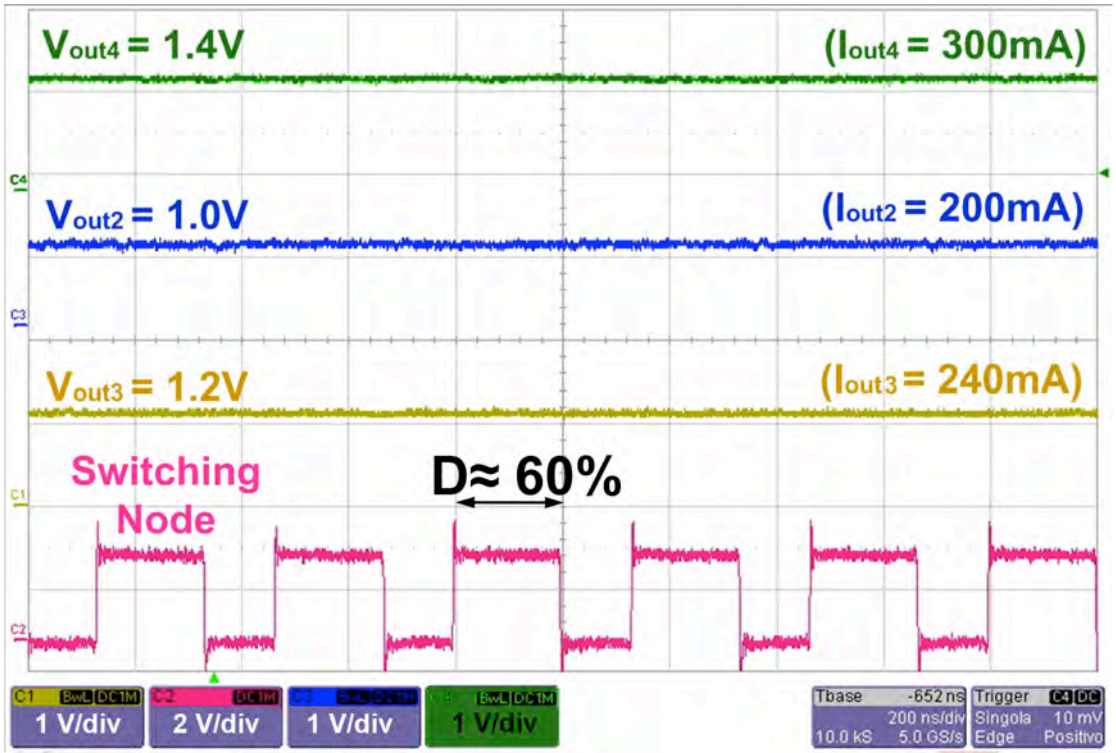

Fig 2.28: Single-inductor 4-output output voltages and the switching node voltage waveforms steady state measurement.

The Figure 2.29 shows a output voltage ripple measurements.

It is possible to see the 4 output waveforms in the steady state ac coupled, with a vertical scale of 50mV.

In this measurements the four output voltages are set respectively to 1.5V, 1.0V, 1.2V and 1.8V, while the four output currents are respectively 150mA, 200mA, 240mA and 400mA.

It's possible to note some switches commutation ringing due to the parasitic inductances that lead to an increased output voltage ripple. In this case the maximum output voltage ripple is about 65mV.

The ripple ringing looks periodic because it occurs in correspondence of the power switches commutations.

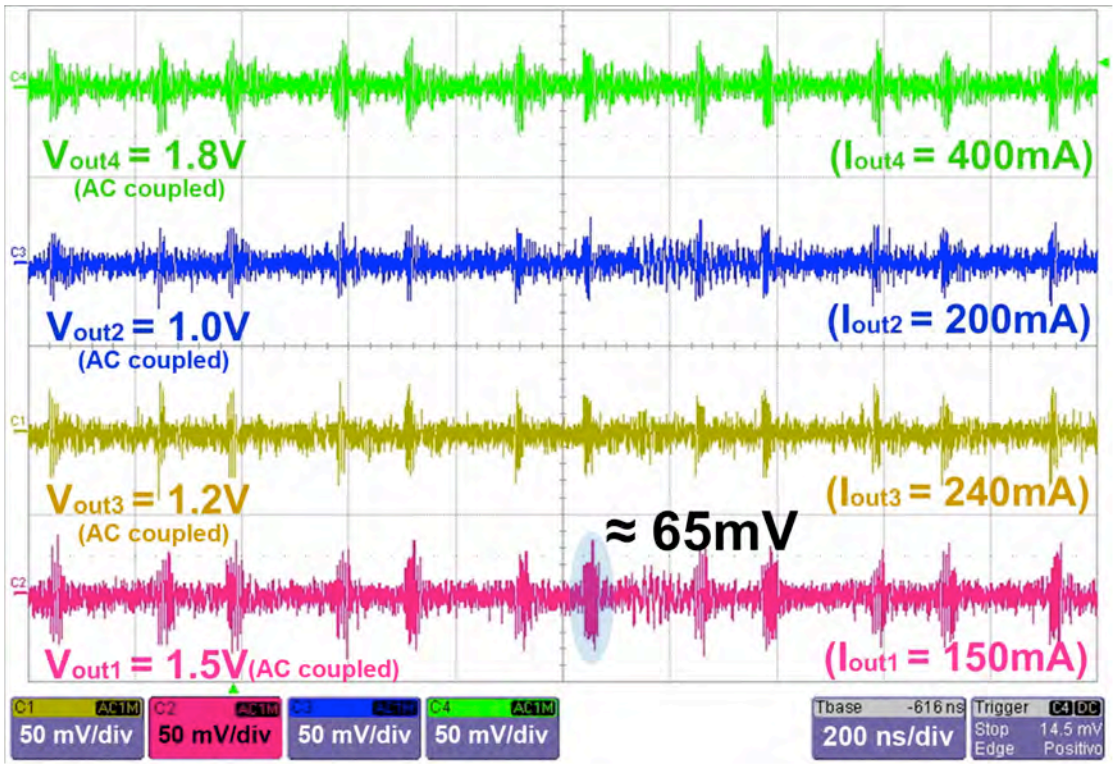

Fig 2.29: Single-inductor 4-output output voltage ripple measurement.

Figure 2.30 shows cross regulation measurements.

For these measurements an input filter slows down the transient response of the converter in order to avoid transient cross regulation drops of the output voltages. However the converter it's pretty fast since it sets in about 80us.

In this measurement $Vout_2$, $Vout_3$ and $Vout_4$ are set at their proper voltage level (1.5V, 1.2V, 1.0V respectively), while $Vout_1$ changes from 0.7 to 1.6V and vice versa. The output currents are respectively 150mA, 100mA, 300mA and 230→560mA.

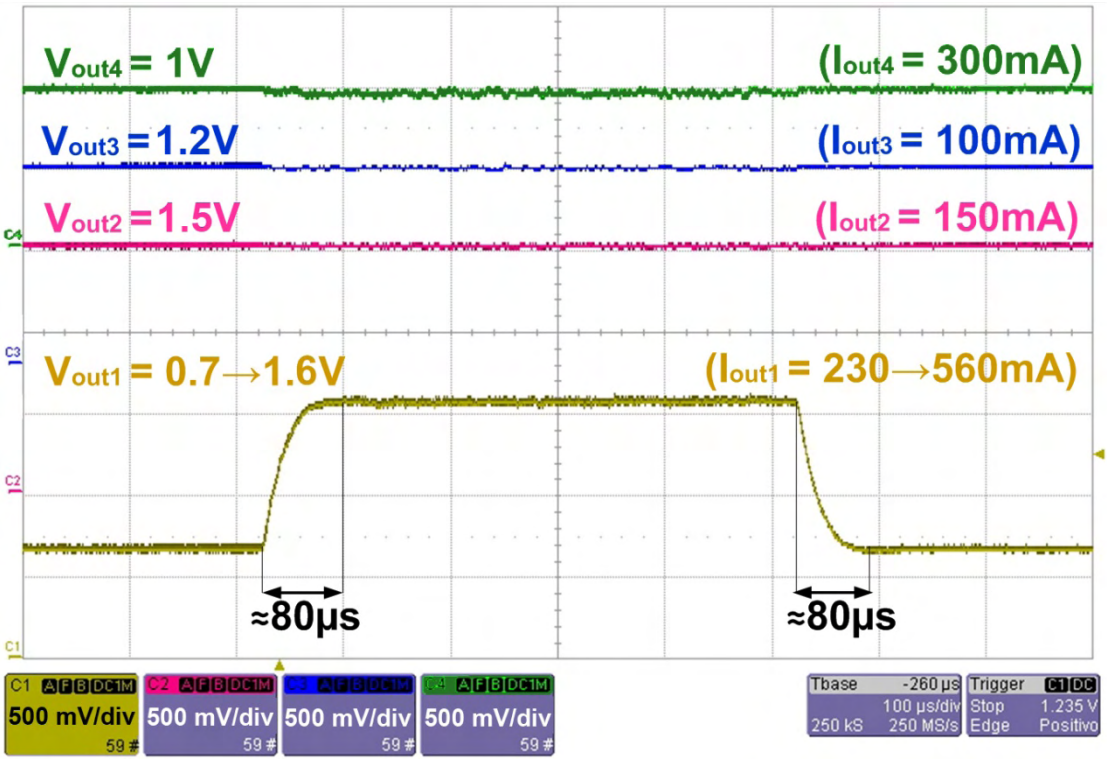

Fig 2.30: Single-inductor 4-output cross regulation measurement.

The Figure 2.31 shows again a cross-regulation measurement but with the output voltages that does not change AC coupled with a 100mV vertical scale.

In this measurements $Vout_1$, $Vout_2$ and $Vout_4$ are set at their proper voltage level, (1.4V, 1.0V, 1.2V respectively), while $Vout_3$ changes from 0.7 to 1.6V and vice versa.

The output currents are respectively 300mA, 50mA, 155mA and 280→640mA.

From the Figure, cross regulations of about 40mV on the first and on the fourth output voltages can be noted.

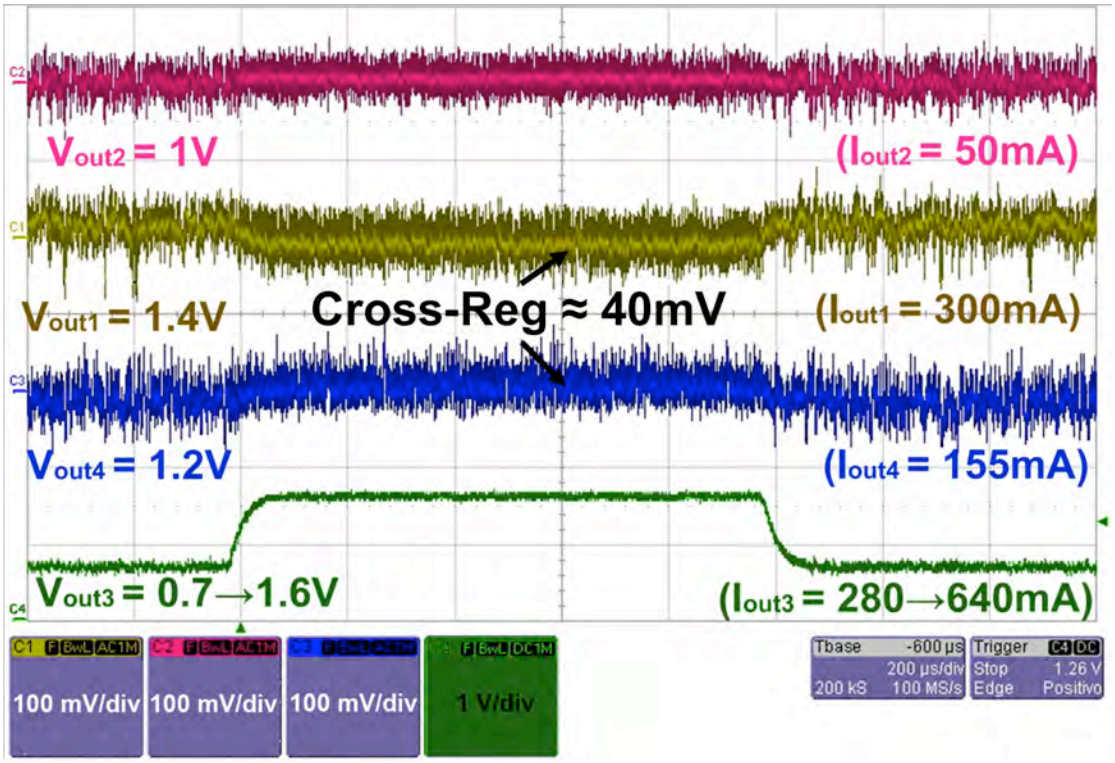

Fig 2.31: Single-inductor 4-output cross regulation measurement – output voltages AC coupled.

In order to emulate a load regulation response, the input filter has been disabled and a step change of the second reference voltage has been applied .

In this measurement $Vout_1$, $Vout_3$ and $Vout_4$ are set at their proper voltage level (1.4V, 1.0V, 1.2V respectively), while $Vout_2$ changes from 0.7 to 1.6V and vice versa. The output currents are respectively 300mA, 50mA, 155mA and 280→640mA.

As shown in the Figure 2.32, the bigger transient drop is of about 160mV and is on the fourth output voltage, while the first output voltage has a cross regulation of about 60mV.

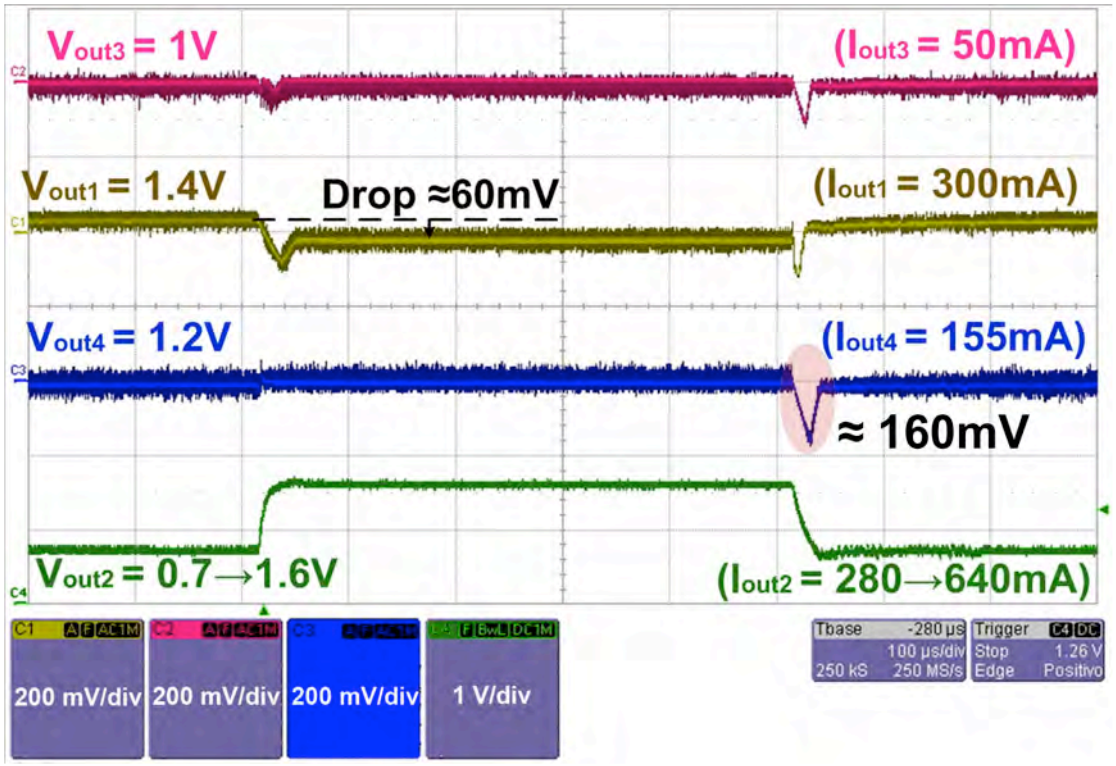

Fig 2.32: Single-inductor 4-output emulated load regulation measurement – output voltages AC coupled.

The Figure 2.33 shows $Vout_4$, its gate voltage, the clock signal and the switching node voltage waveforms.

It can be noted that the self-boosted snubber circuit boost up the switch gate voltage at 5.5V clamped by the protection pads.

Some $Vout_4$ ringing of about 80mV peak during the load switch commutations has been observed in this condition.

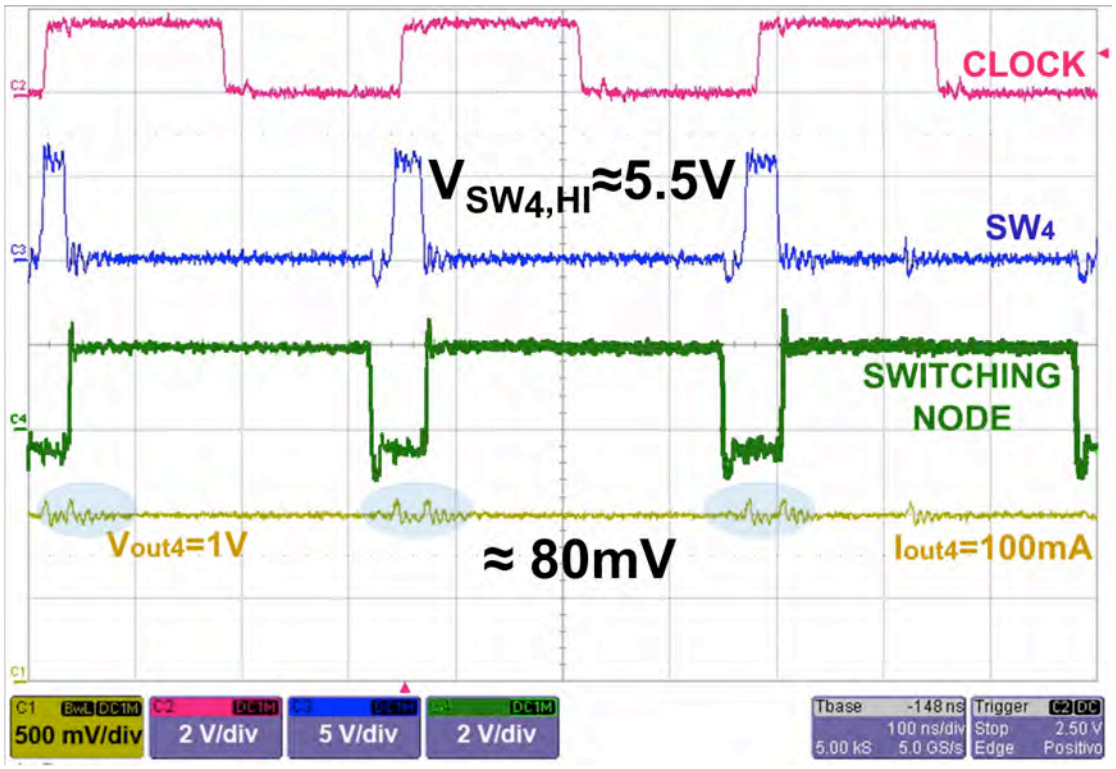

Fig 2.33: Single-inductor 4-output measurement waveforms.

The Figure 2.34 shows the measured power efficiency as a function of the fourth output current with $Iout_1$, $Iout_2$, $Iout_3$ fixed.

The supply voltage is at its minimum value of 2.3V. The efficiency peak is of about 85% at 330mA.

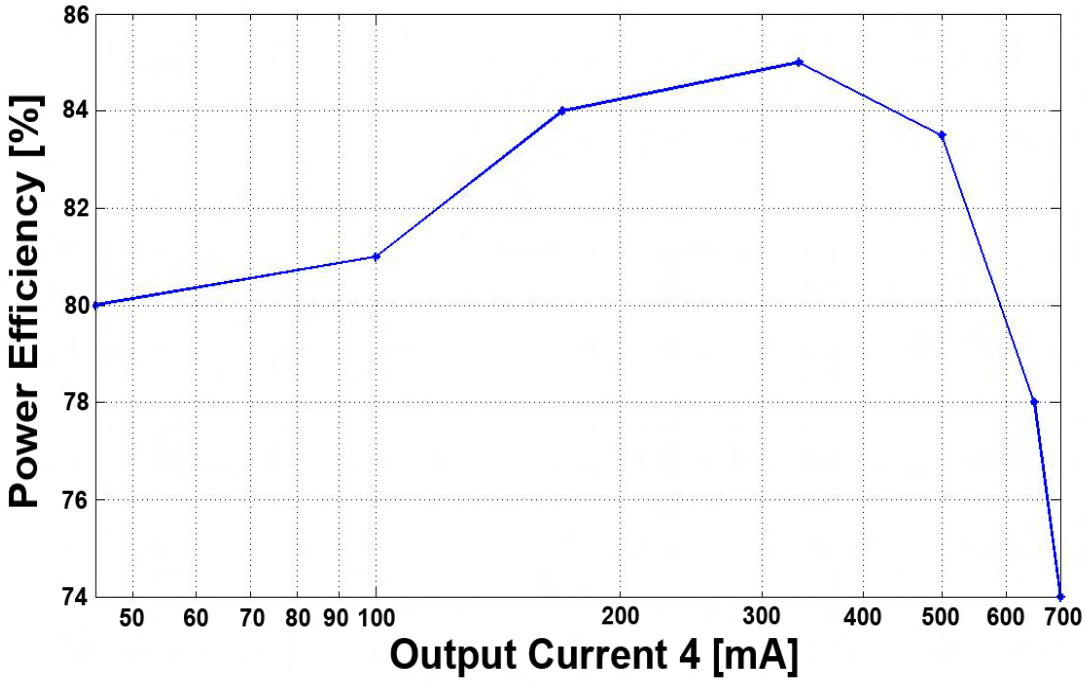

Fig 2.34: Single-inductor 4-output power efficiency measurement.

2.16 SINGLE-INDUCTOR 4-OUTPUT PERFORMANCE SUMMARY

Table 2.2 summarize the measured system performances.

Experimental results show that, with a 2.3V minimum supply, it is possible to independently regulate the four outputs in the range 0 - 1.8V with a total current capability of 1.2A. With a higher supply voltage, the 1.8A overall driving capability provides the maximum single-channel current of 0.8A in one channel and the remaining in the others. Lower currents are obviously possible, but the minimum average inductor current needed by the self-boosting switch drivers is 0.1A.

The voltage ripple is lower than 90mV for all operating conditions. The circuit operates with supplies up to 5V. However, since the ESD protection on the self-boosted drivers output limits the boosted voltage to about 5V, the regulated outputs can only go up to 3.6V.

The maximum cross and load regulation have been respectively 40mV/V and 45mV/V.

The measured peak power efficiency is 85%.

Supply Voltage [V]	2.3→5
Output Voltages [V]	0 →(V_{supply} - 0.5)
Max Output Voltage [V]	3.6
(Total) Output Current [A]	0.1 → 1.8
(Single) Output Current [A]	0 → 0.8
Max Voltage Ripple [mV]	90
Max Cross-Regulation [mV/V]	40
Max Load-Regulation [mV/V]	45
Peak Efficiency [%]	85

Tab 2.2: Single-inductor 4-output performance summary.

REFERENCES

[1] N. Mohan, T.M. Undeland, and W.P. Robbins, "Power Electronics - Converters, Applications, and Design – Second Edition", John Wiley & Sons, INC., Ch. 7.

[2] B. Arbetter, R. Erickson, and D. Maksimovic, "DC-DC converter design for battery-operated systems", *IEEE Power Electronics Specialist Conference*, vol. 1, pp. 103 – 109, June 1995.

[3] V. Kursun, S.G. Narenda, V.K. De, and E.G. Friedman, "Analysis of buck converters for on-chip integration with a dual supply voltage microprocessor", *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 11, pp. 514 – 522, June 2003.

BIBLIOGRAPHY

[1] R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics (Second Edition)", Kluwer Academic Publisher, 2004.

[2] National Semiconductor Corporation, "Meeting Power Design Challenges – High-Performance Seminar Series 2007".

[3] National Semiconductor Corporation, "Knowledge is Power – Power Design Technical Courses 2007".

[4] National Semiconductor Corporation web-site, http://www.national.com.

[5] Maxim Corporation web-site, http:// www.maxim-ic.com.

CHAPTER 3

A DC-DC BUCK CONVERTER WITH VERY HIGH SWITCHING FREQUENCY

Modern portable devices more and more require the use of several DC-DC converters that provide different output voltage levels with minimum volume and off-chip components.

Applications possibly share the inductors or miniaturize the single DC-DC converter block.

The first method has been applied to design the single-inductor 4-output DC-DC buck converter discussed in details in Chapter 2.

The strategy used for this work miniaturizes the single DC-DC converter block increasing the operating frequency. In this way, smaller off-chip inductance and output capacitance sizes are then allowed. Small values of inductor and capacitor

enable on-chip or in-package integration while preserving overall power efficiency that is higher than a linear regulator over a large range of output current.

If the generated voltage V_{out} is D times the supply voltage, the efficiency of the linear regulator is D. Therefore, the goal is to keep system efficiency well above D for an extended range of output current.

Just obtaining very high switching frequency with conventional architectures, [1] and [2], is not practical. The goal of this part of the research activity is to develop a new control circuit that achieves, for 1A output current capability, a power efficiency higher than what reported in published research results, [3] and [4].

3.1 HIGH SWITCHING FREQUENCY BENEFITS AND ISSUES

There are several benefits arising from the DC-DC converter switching frequency increase.

At first, as already briefly discussed, a higher switching frequency enables a smaller LC product of the output low-pass filter, which in turn allows smaller external component and may enable on-chip or in-package integration.

In addition, a higher closed-loop control cut-off frequency can be achieved, obtaining also faster load and line regulation transient responses.

On the other hand, the increase of the switching frequency in conventional DC-DC converters architectures requires operational amplifiers in the control loop with an augmented bandwidth, larger slew-rate and faster PWM comparators.

As known, more speed in the operational amplifiers and in the comparators requires more current. The increase is linear if the input transistors are in weak inversion, almost quadratic if they are in saturation. Typically, weak inversion is not possible and the power cost of the control section becomes remarkable for switching frequencies above 20-30MHz thus degrading light load power efficiency.

In addition, since the dynamic losses increase linearly with the increase of the frequency , at light loads, the system power efficiency is further reduced.

Moreover, the control circuit poles may affect the closed-loop stability leading to control loop compensation issues.

Furthermore, due to the faster current derivatives, switching current spikes may cause ground bounce which in turn may lead to controller upsets and unexpected circuit behavior. Therefore, in order to achieve high switching frequency control system, in this work a new PWM controller architecture has been provided.

3.2 DESIGN TARGETS

The project has been carried out in cooperation with National Semiconductor Corporation Power Management Group. Table 3.1 summarizes the project design targets established to meet actual industrial applications requirements.

However, some key performance, as the allowed input supply voltage range, has been limited by SOA requirements of the used technology that is a 0.18µm CMOS process, optimized for data converter applications. This process is not suitable for switching converter applications but, on the other hand, it was the only one available to realize this IC prototype. In particular, the allowed maximum supply voltage is 2.8V.

The output current capability is 1A. The output voltage ranges from 0 to 500mV below the applied input supply voltage. The switching frequency is 60MHz while the inductor is 36nH and the output capacitor is 4.7µF.

Supply Voltage [V]	2.2→2.8
Output Voltages [V]	0 →(V_{supply} - 0.5)
Output Current [A]	0 → 1
Switching Frequency [MHz]	60
Inductor [nH]	36
Output Capacitors [µF]	4.7
Technology	CMOS 0.18 µm
Substrate Type	p-epi

Tab.3.1: Design targets

3.3 HIGH SWITCHING FREQUENCY BUCK CONVERTER ARCHITECTURE

The key feature of this design is a new VCM control method that replaces the conventional VCM operational amplifier based scheme discussed in Section 1.7.

Other than allowing enhanced light load efficiencies, this innovative solution is promising for switching frequencies in the hundred MHz range that would need operational amplifiers with multi-GHz unity gain frequencies.

The Figure 3.1 shows the proposed high-frequency synchronous-rectification buck VCM regulator architecture.

In this implementation, the output voltage error is processed in the current domain by a voltage-to-pulse converter (V2P block in the diagram), which digital output signal directly controls the power switches driver circuit (DRVR block in the diagram).

Moving in the current domain significantly spares power and achieves controls up to very high frequency with pseudo-integral features.

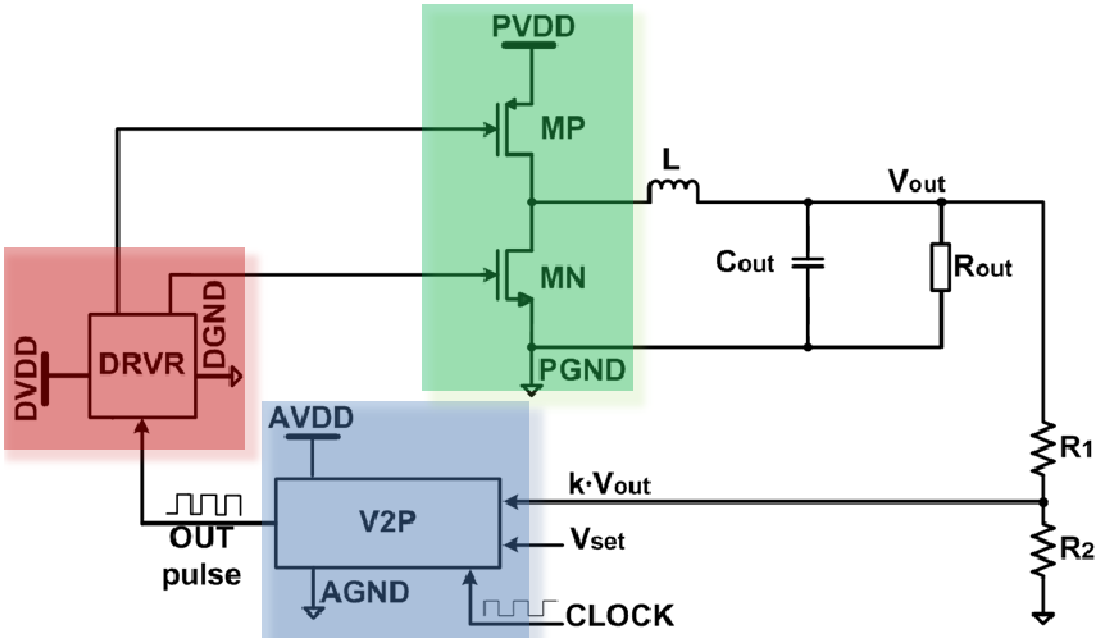

Fig. 3.1: Proposed high frequency buck converter architecture.

Even if the architecture seems to be very simple, the design of the voltage-to-pulse converter is the not trivial at all since it is strictly related to the overall closed-loop control system performances. Therefore, in order to optimize the architecture design, a system-level model of the overall regulator is required.

The AC small-signal model of the converter is normally used to analyze the variations of the output voltage around the desired steady-state value. In fact, the model allows an approximated estimation of the regulator dynamic behavior. Then, each part of the system will be represented by a corresponding block in the small-signal architecture model, as it will be illustrated in the next Sections.

3.4 BUCK CONVERTER AC SMALL-SIGNAL MODEL AND TRANSFER FUNCTION

The DC-DC buck converter is, like any other switching regulator, a nonlinear system. As already mentioned, the AC small-signal model allows the designer to analyze the effect of perturbations on output voltage obtaining a simplified linear dynamic model of the converter, which is of great help in design of the control components.

Using standard averaging and linearization techniques around a DC operating point, perturbation of output voltage can be approximated by the linear superposition of the effects of perturbations of input voltage, output current and duty cycle.

Even if exact explicit expressions can be derived analytically, some approximated expressions can be obtained for practical control design.

The main issues to be considered, concerning the involved transfer functions, are:

- Parasitic series resistance (impedance) of the output capacitor ESR.
- Parameter tolerances of the off-chip components, such as the inductor and the output capacitor.
- Effect of line and load conditions.

The appropriate small-signal average model for the proposed high frequency buck converter circuit in Laplace Domain is manifested in Figure 3.2.

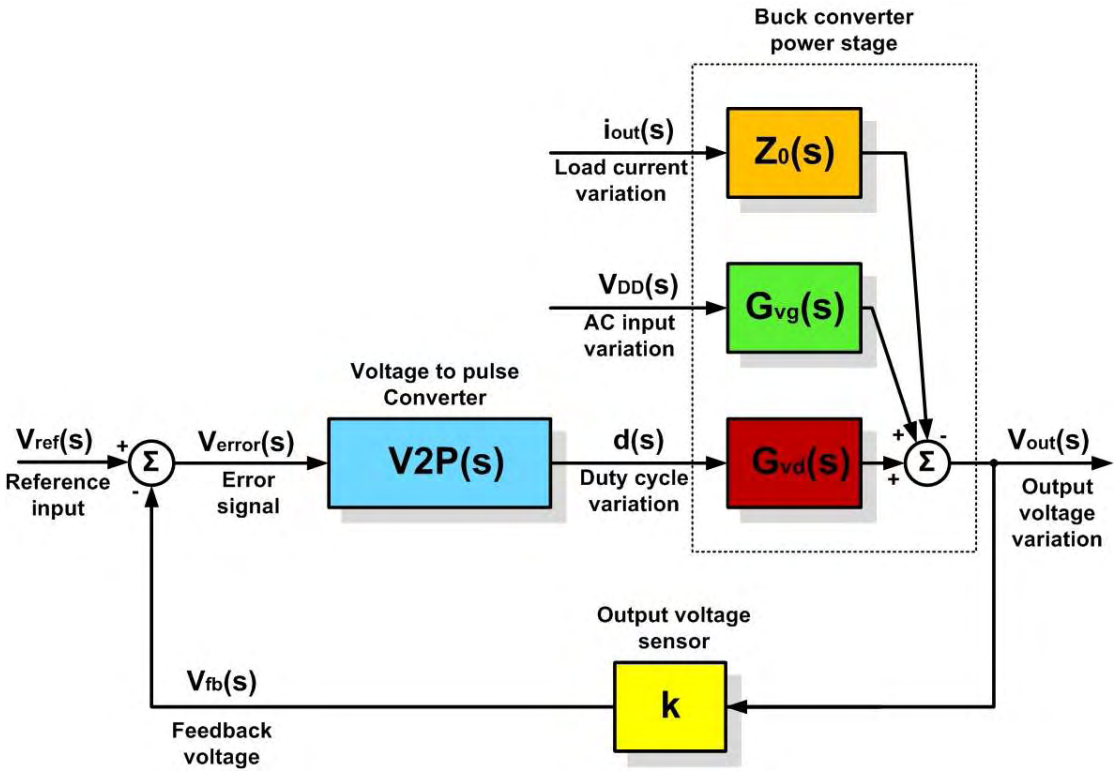

Fig. 3.2: Small-signal average model for the proposed high frequency buck converter circuit in Laplace Domain

Referring to Figure 3.2:

- the duty-to-output transfer function G_{vd} expresses the sensitivity of output voltage V_{out} to duty cycle d variations, when input voltage V_{DD} and output current i_{out} are locked at their steady state values:

$$G_{vd}(s)=\left.\frac{V_{out}(s)}{d(s)}\right|_{i_{out}=0,V_{DD}=0} \tag{3.1}$$

- the line-to-output transfer function G_{vg} expresses the sensitivity of output voltage V_{out} to input voltage V_{DD} variations, when duty cycle d and output current i_{out} are locked at their steady state values:

$$G_{vg}(s)=\left.\frac{V_{out}(s)}{V_{DD}(s)}\right|_{i_{out}=0,d=0} \tag{3.2}$$

- the load-to-output (output impedance) transfer function Z_{out} expresses the sensitivity of output voltage V_{out} to output current i_{out} variations, when input voltage V_{DD} and duty cycle d are locked at their steady state values:

$$Z_{out}(s)=-\left.\frac{V_{out}(s)}{i_{out}(s)}\right|_{V_{DD}=0,d=0} \tag{3.3}$$

Manipulating the AC small-signal block diagram and solving for $V_{out}(s)$:

$$V_{out}(s)=G_{vg}(s)\cdot V_{DD}(s)-Z_{out}(s)\cdot i_{load}(s)+G_{vd}(s)\cdot d(s) \tag{3.4}$$

The expression of G_{vd} , G_{vg} and Z_{out} are well know from the theory and have been reported in equations (3.5), (3.6), and (3.7):

$$G_{vg}(s)=\overline{D}\cdot\frac{1+(ESR\cdot C)\cdot s}{1+(ESR\cdot C)\cdot s+\left(L\cdot C+ESR\cdot C\right)\cdot s^2} \tag{3.5}$$

$$G_{vd}(s)=\overline{V_{DD}}\cdot\frac{1+(ESR\cdot C)\cdot s}{1+(ESR\cdot C)\cdot s+\left(L\cdot C+ESR\cdot C\right)\cdot s^2} \tag{3.6}$$

$$Z_{out}(s)=\overline{R_{load}}\cdot\frac{1+(ESR\cdot C)\cdot s}{1+(ESR\cdot C)\cdot s+\left(L\cdot C+ESR\cdot C\right)\cdot s^2} \tag{3.7}$$

These expressions have been reported in their simplest form. In fact, these equations have been derived without considering any parasitic in the power train at exception of the capacitor ESR parasitic resistance, which is the one that, for this design, play the most important role in system stability.

3.4.1 BUCK CONVERTER OPEN LOOP TRANSFER FUNCTION

The open-loop control-to-output voltage transfer function is given by equation (3.6), or more succinctly in its normalized form by:

$$G_{vd}(s)=\overline{V_{DD}}\cdot\frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q_0\omega_0}+\frac{s^2}{\omega_0^{\,2}}} \tag{3.8}$$

As Evident from equation (3.8), the power stage transfer function of a VCM buck converter has a complex double pole related to the LC output filter and a left half plane zero due to the output capacitor ESR, the locations of which are given respectively by:

$$f_0=\frac{\omega_0}{2\pi}=\frac{1}{2\pi\sqrt{LC\cdot\left[1+\frac{ESR}{R_{load}}\right]}}\approx\frac{1}{2\pi\sqrt{LC}} \tag{3.9}$$

$$f_{ESR}=\frac{\omega_{ESR}}{2\pi}=\frac{1}{2\pi\cdot ESR\cdot C} \tag{3.10}$$

where f_o and f_{ESR} represent the LC filter complex double pole and output capacitor ESR zero, respectively. The expression of the LC output filter quality factor Q_0 is:

$$Q_0=R_{load}\sqrt{\frac{C}{L}} \tag{3.11}$$

3.4.2 INDUCTOR AND OUTPUT CAPACITOR SELECTION AND OPEN-LOOP BUCK CONVERTER BODE DIAGRAM

Although the buck converter topology and its operation are quite well understood, the choice of operating parameters and of commercial inductor and capacitor components to realize a good project is not trivial at all.
Inductor, output capacitor, current and voltage ripple amplitudes, LC filter complex double pole placement are all elements strictly related each other and have a strong impact on the converter's global performances.
With regard to the inductor selection, as discussed in Section 1.3, for the inductor current ripple Δi_L holds the equation (if the small ripple approximation holds):

$$\Delta i_L = \frac{D \cdot (V_{DD} - V_{out})}{L f_{sw}} \tag{3.12}$$

Usually, as a rule of thumb, Δi_L is chosen as the 40% of the maximum output current and it is evaluated in the worst case (for the buck converter) of $V_{DD} = V_{DD,max}$ and $D = 0.5$. Therefore:

$$L \geq \frac{0.5 \cdot (V_{DD,max} - 0.5V_{DD,max})}{0.4 I_{out,max} f_{sw}} = \frac{0.5 \times (2.8-1.4)}{0.4 \times 60 \times 10^6} \approx 30nH \tag{3.13}$$

Considering also the inductor parameters, summarized in Table 3.2, such as tolerance, saturation current and DC series resistance, the chosen inductance, is 36nH.

Figures 3.3 And 3.4 show the inductor value dependence on current and operating frequency. It is evident that the selected inductor complies with all the requirements.

Part number[1]	L ±10%[2] (µH)	DCR ±5%[3] (mOhms)	SRF typ[4] (MHz)	Isat[5] (A)	Irms[6] (A)
SLC7649S-360KL_	0.036	0.17	1150	100	39
SLC7649S-500KL_	0.050	0.17	900	84	39
SLC7649S-700KL_	0.070	0.17	750	65	39
SLC7649S-101KL_	0.100	0.17	110	42	39

Tab.3.2: Selected inductor characteristics.

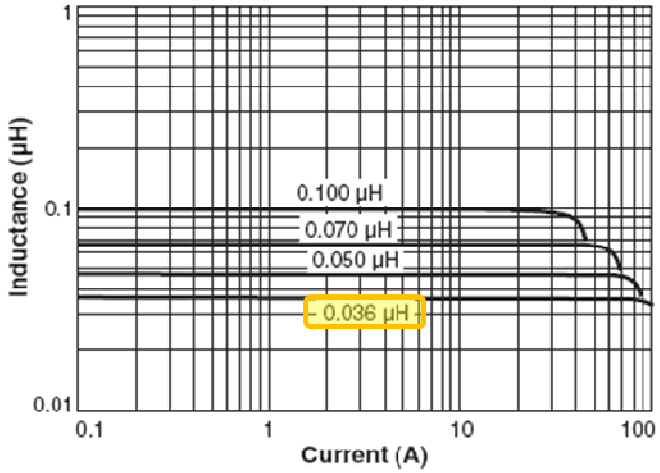

Fig. 3.3: Selected inductance (µH) vs. current (A).

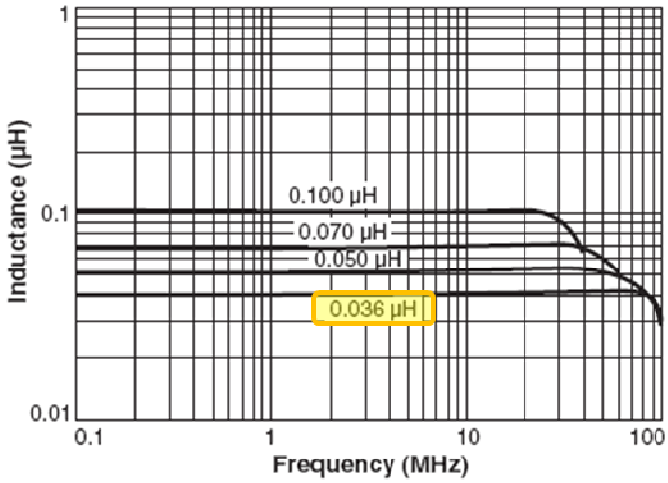

Fig. 3.4: Selected inductance (µH) vs. switching frequency (MHz).

While, with regard to the output capacitor selection, as discussed in Section 1.4, for the output voltage ripple ΔV_{out} holds the equation (if the small ripple approximation still holds):

$$\Delta V_{out} = \frac{DV_{out}}{R_{load} C f_{sw}} \tag{3.14}$$

Usually, as a rule of thumb, ΔV_{out} is chosen lower than the expected output voltage error and it is evaluated in the worst case (for the buck converter) of $V_{out} = V_{out,max}$ and $D = 0.5$.

Therefore:

$$C \geq \frac{DV_{out,max}}{R_{load,min} \cdot 0.1 \cdot V_{error,max} \cdot f_{sw}} = \frac{0.5 \times 1.4}{2.3 \times 1.4 \times 10^{-3} \times 60 \times 10^{6}} \approx 3.6\mu F \tag{3.15}$$

Considering also capacitor parameters, summarized in Table 3.3, such as tolerance, rated voltage and ESR series resistance the chosen capacitance is 4.7µF.

Temperature characteristic		X5R
Climatic category (IEC 60068-1)		55/85/56
Standard		EIA
Dielectric		Class 2
Rated voltage[1)]	V_R	6,3; 10; 16; 25
Test voltage	V_{test}	$2,5 \cdot V_R$/5 s
Capacitance range / E series	C_R	100 nF ... 22 µF (E3+)
Max. relative capacitance change	$\Delta C/C$	±15
Dissipation factor (limit value)	tan δ	$< 50 \cdot 10^{-3}$
Insulation resistance[2)] at +25 °C	R_{ins}	$> 10^4$
Time constant[2)] at +25 °C	τ	> 500
Operating temperature range	T_{op}	–55 ... +85
Ageing[3)]		yes

Tab.3.3: Selected capacitor characteristics.

Figure 3.5 illustrates the output capacitor ESR dependence on the operating frequency. It can be noted that the ESR relative to the 60MHz switching frequency is about 40mV.

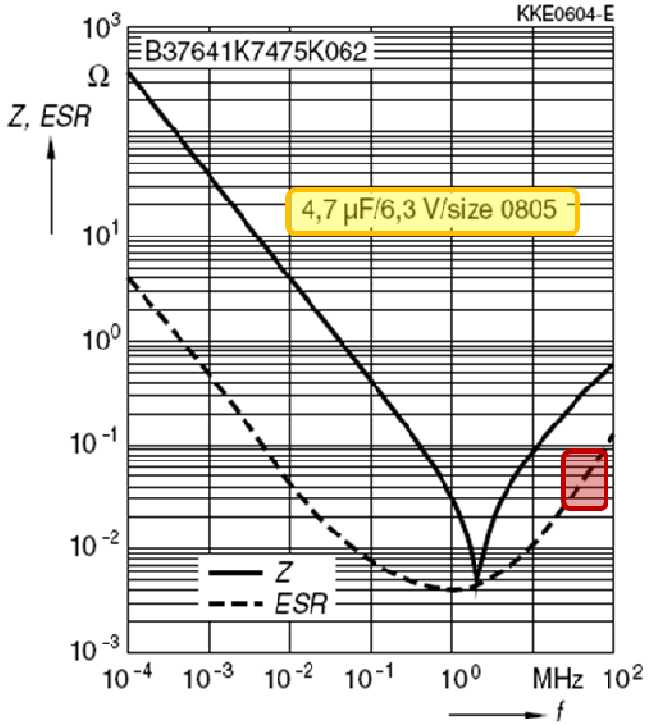

Fig. 3.5: Selected capacitor impedance and ESR vs. switching frequency.

On the basis of the inductor and output capacitor values and their tolerances, it is possible to estimate the frequency of the two LC poles and of the ESR zero, that are respectively:

- p1=60↔80KHz
- p2=1.95↔2.45MHz
- z_{ESR}=0.65↔0.9MHz

It can be noted that for this calculation has been considered the closed loop stability worst-case corresponding to D = D_{max} = 0.9 and I_{out} = I_{max} =1A.

It is worth to point out that, since the converter switching frequency is quite high, the ESR zero lies in the frequency range of interest and may helps in closed-loop stability. Figure 3.6 depict the relative estimated bode diagram.

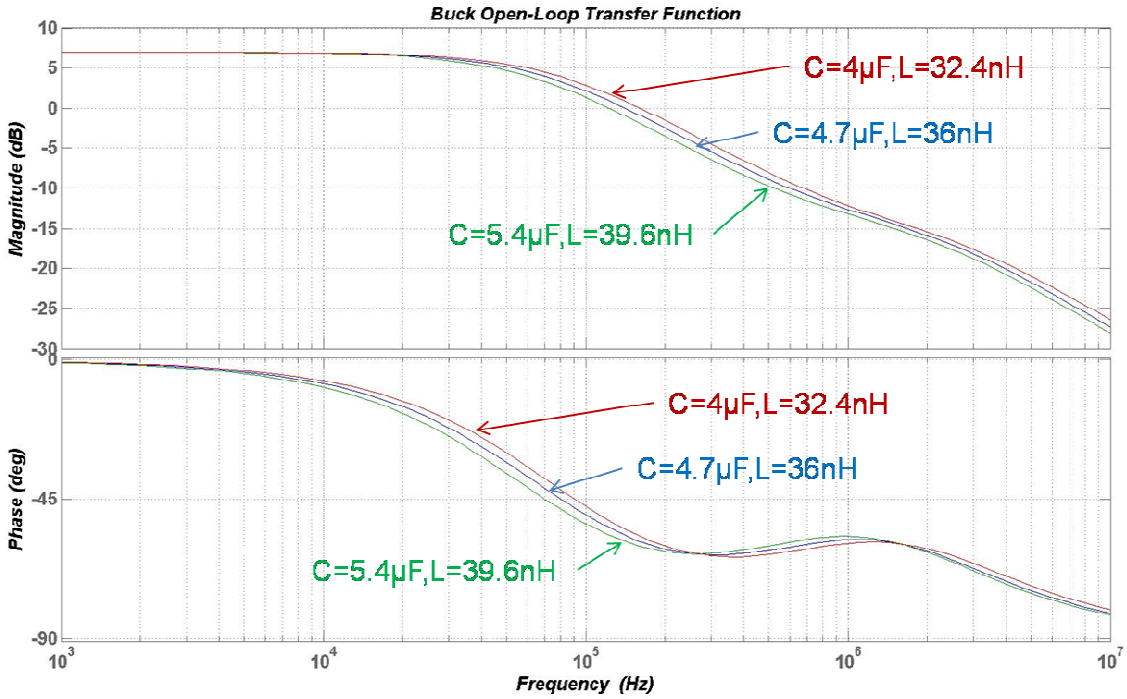

Fig. 3.6: Open-loop high frequency buck converter bode diagram.

3.5 VOLTAGE-TO-PULSE CONVERTER CIRCUIT

The Figure 3.7(a) depicts the basic operating principle of the voltage-to-pulse converter circuit, while the Figure 3.7(b) shows the circuit relative voltage waveforms.

Consider for instance the case in which the input clock signal CLOCK is low. The upper switch MP is on while the lower switch MN is off.

Therefore, the capacitor C1 is discharged, the voltage $V_{c,bot}$ is equal to the supply voltage V_{DD} and the output of the inverter OUT PULSES is at the low logic level 0.

When the input clock signal rises to the high logic level 1, the upper switch MP turns off while the lower switch MN turns on.

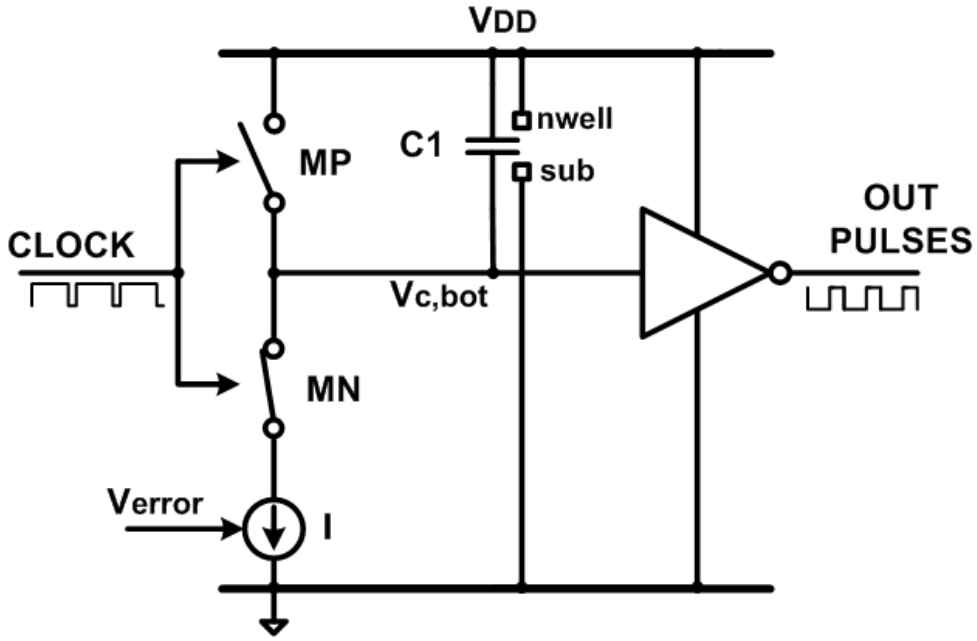

Fig. 3.7(a): Principle of the voltage-to-pulse converter circuit.

Then, the current generator I start to charge the capacitor C1 with a approximately constant current that depends on the applied output voltage error V_{error} (this is true if the error voltage variation is small and if the current generator output resistance is high enough).

When the node voltage $V_{c,bot}$ falls below the supply voltage V_{DD} minus the inverter threshold voltage V_{TH}, the output of the inverter rises to the high logic level 1.

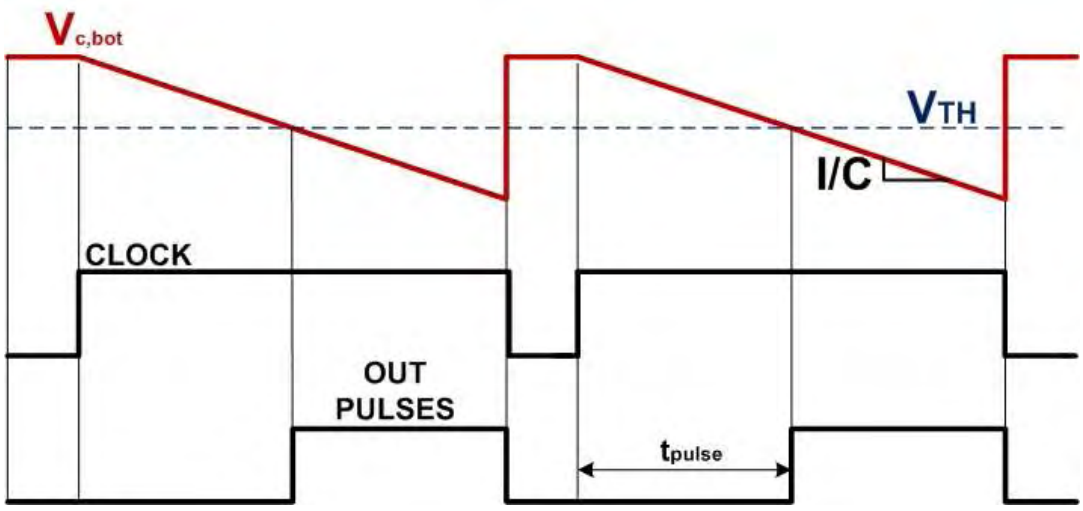

Fig. 3.7(b): Voltage-to-pulse circuit waveforms.

As a result, a delay time t_{pulse} between the rising edge of the input clock signal and the rising edge of the inverter output pulse has been provided. Furthermore the obtained variable delay time t_{pulse} depends on the applied output voltage error V_{error}.
An approximate relationship between the delay time and the voltage error can be expressed as:

$$t_{pulse} = \frac{C1 \cdot (V_{DD} - V_{TH})}{I(V_{error})} \tag{3.16}$$

In order to meet the control circuit requirements, an higher voltage error must lead to a longer delay time, while a lower voltage error must lead to a shorter delay time.
It is possible to note that the voltage-to-pulse output current flowing in the capacitor C1 charging phase is, in the worst case, equal to the current I. This is true if the inverter crowbar is avoided with a suitable control logic.

3.5.1 VOLTAGE-TO-PULSE CONVERTER CIRCUIT DETAILS

Figure. 3.8 shows a more detailed circuit schematic.
The input differential pair (PMOS transistors MP_4 and MP_5) transforms the applied output voltage error $\varepsilon = (V_{set} - kV_{out})$ into a current and provides a transconductance gain, G_m.
Then, the transconductance stage output current $I_4 = [(I_B/2) - G_m\varepsilon]$ is 1:1 mirrored by the cascode current mirror (NMOS transistors MN_1, MN_2, MN_4 and MN_6) and used to charge the capacitor C_1 (n-well shielded), initially discharged at V_{DD} by the PMOS switch MP_3.
The cascode current mirror configuration provides a mirroring factor that does not depend on the capacitor bottom plate voltage, thus preventing control nonlinearity.
Besides, the dummy PMOS switch MP_1 provides a path for the current I_1 during the capacitor discharging phase then avoiding additional current mirror turn on delays.
The trigger signal starting the capacitor charge is a short pulse synchronous with the input clock provided by a internal multivibrator.

The duty cycle of the trigger signal is 0.95 and clamps to the same value the maximum switching duty cycle achievable from the voltage-to-pulse converter.

At the circuit start-up the duty cycle of the trigger signal is gradually increased with an exponential transient providing soft-start.

The output control, started at the beginning of the switching period, ends when V_{G0} crosses the threshold voltage of MP_0, V_{thP0}, and is enforced by a tapered inverter chain.

Since the voltage V_{G0}, during the charge transient, decreases slowly, in order to prevent the MP_0-MN_0 inverter crowbar, the pull-down NMOS transistor MN_0 is driven by the fast trigger signal. In this way, when the pull-up PMOS transistor MP0 charge the capacitor C_1, NM0 is off.

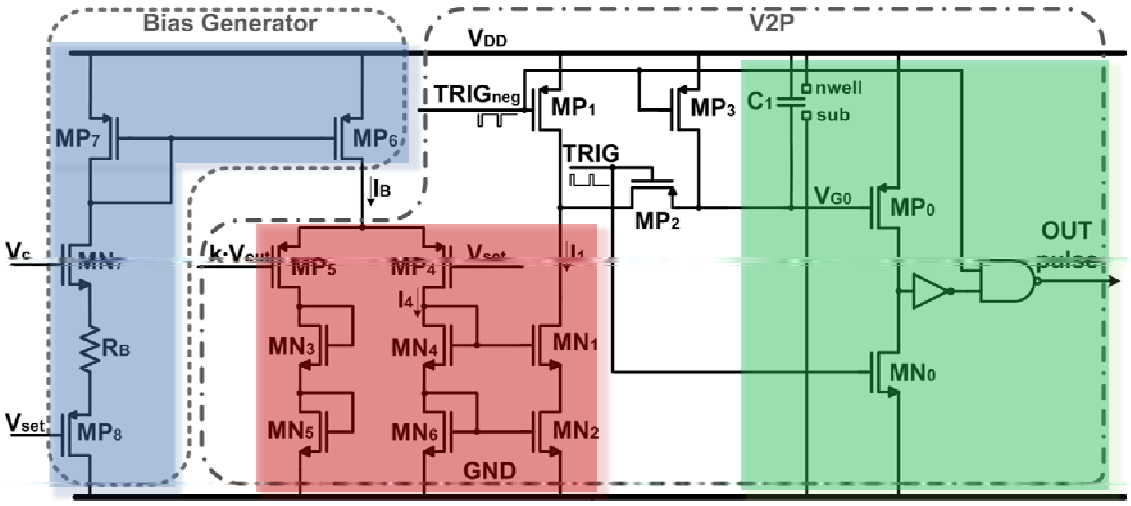

Fig. 3.8: Voltage-to-pulse converter circuit details.

3.5.2 VOLTAGE-TO-PULSE CONVERTER DESIGN CONSIDERATIONS

With balanced signals at the voltage-to-pulse converter input, the charge current of C_1 is $I_1 = I_B/2$ with duty cycle $D = 2C_1V_{thP0}/(I_BT_{sw})$.

Therefore, if the system needs a steady-state duty cycle $D^* = 0.5$, a bias current $I_B=C_1V_{thP0}/(T_{sw})$ should be used.

With C_1 = 0.15pF, V_{thP0} = 0.7V and $f_{sw} = 1/T_{sw}$ = 60MHz, I_B results 6.3µA, a very low value when compared with current of conventional control loops at same switching frequency. Also, the required silicon area is negligible.

The voltage-to-pulse converter has been designed in order to provide the whole range of duties cycles needed with a input voltage error bounded by ±2%($V_{out,min}$).

As additional feature, this design provides the bias current of the PMOS input differential pair with a proper dependent bias generator. It uses two voltages, the setting and a suitable control, V_{set} and V_c, as shown in Figure 3.8. The two voltages and the integrated resistor R_B determine the bias current.

The voltage V_{set} gives a rough control of the bias current that diminishes at high settings. Moreover, a sudden change of setting voltage gives rise to an immediate response that changes the duty cycle decreasing the circuit transient response time.

The control of V_c obtains a fine trimming and can be open loop or closed loop. Open loop uses an external voltage. Closed loop processes the error in the current domain by using a replica of the error current I_4 that is integrated on an RC with large time constant (off-chip for this implementation) to increase I_B when $I_4 > I_B$.

The scheme has an equivalent loop gain. Its value for a quiescent duty cycle D^* with bias current I_B^* is given by the expression of D as function of the error ε:

$$D=\frac{D^*}{1-\frac{G_m\varepsilon}{I_B^*/2}} \approx D^* \cdot \left(1+\frac{G_m\varepsilon}{I_B^*/2}\right) \tag{3.17}$$

linearly proportional to the error around the expected duty cycle.

In conventional counterparts, the loop gain and the amplitude of saw-tooth, V_s, gives the sensitivity to error $\delta D/\delta\varepsilon = A_0/V_s$.

An equivalent sensitivity is provided by the derivative of equation (3.17). It results:

$$\frac{\partial D}{\partial \varepsilon}=\left.\frac{A_0}{V_s}\right|_{eq}=\frac{2D^*G_m}{I_B^*} \tag{3.18}$$

This design uses MOS transistors in saturation; therefore, $G_m = I_B^*/V_{ov}$:

$$\frac{\partial D}{\partial \varepsilon} = \frac{A_0}{V_s}\bigg|_{eq} = \frac{2D^*}{V_{ov}} \tag{3.19}$$

Since the overdrive voltage is around 65mV, with $D^* = D_{max} = 0.9$ and $V_s = 1V$, the equivalent gain is $A_{0V2P,max} = 26.4$.

Therefore, in the frequency range of interest, the voltage-to-pulse converter has a first-order transfer function which pole is related to the cascode current mirror output impedance as shown by:

$$VTP(s) \approx \frac{A_{0,V2P}}{1+\frac{s}{p_{V2P}}} = \frac{A_{0,V2P}}{1+\frac{s}{R_{out,cascode}C_1}} \tag{3.20}$$

Figure 3.9 depicts the estimated closed loop circuit bode diagram for the stability point of view worst-case. This bode diagram considers the inductor and output capacitor tolerances. It can be noted that the estimated cut-off frequency lies in the range from 5.9MHz to 6.4MHz, while the estimated phase margin lies in the range from 40° to 43°. Therefore, in order to keep the circuit complexity as low as possible, the frequency compensation is not needed.

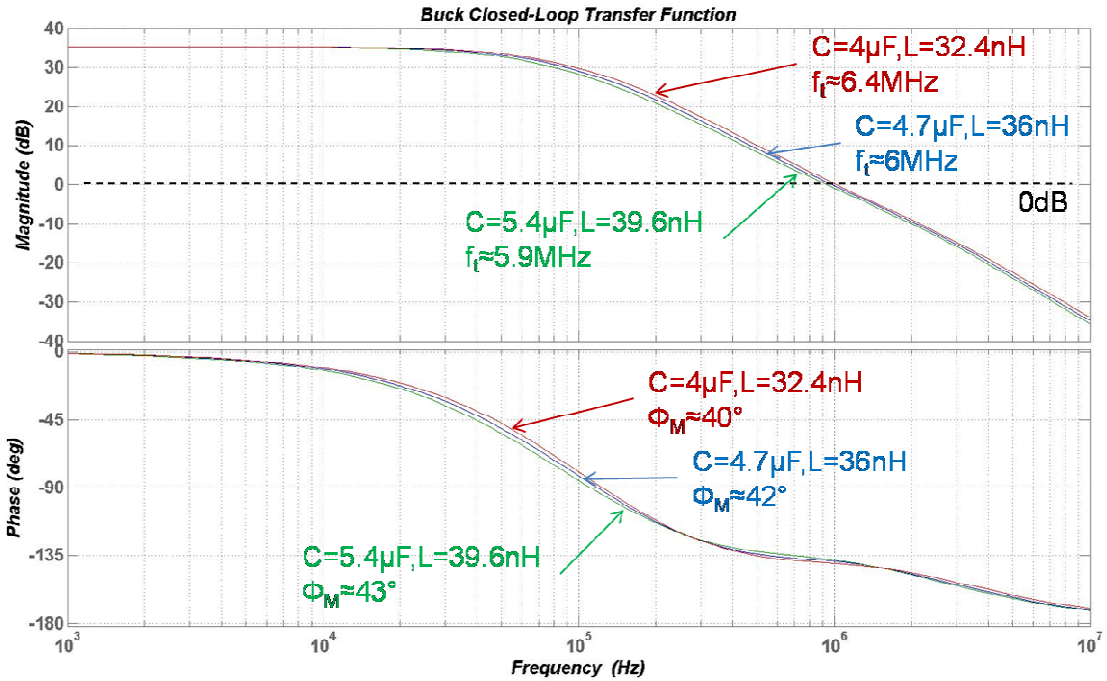

Fig. 3.9: Estimated closed-loop high frequency buck converter bode diagram.

3.6 HIGH SWITCHING FREQUENCY BUCK CONVERTER IC PROTOTYPE

The Figure 3.10 shows the chip microphotograph. A 0.18um gate length process with 5 metals and 2 poly layers has been used.

Power transistors, MP and MN, their drivers, DRVR, and the voltage-to-pulse converter, V2P, are highlighted. The active area is 1.2mm x 0.76mm, with 0.003mm^2 used for the current-mode and V2P converter.

As briefly discussed in Section 3.2, the used process is usually employed to design data converter circuits and it is not suitable for switching regulator.

In particular, two key aspects have limited the achievable circuit performance:

1) The process not provide any thick metal layer able to sustain large amount of currents in the buck power train (even the top metal has limited allowable current density).
2) Safe-Operating-Area of the provided MOS transistors limits the maximum input supply voltage to 2.8V.

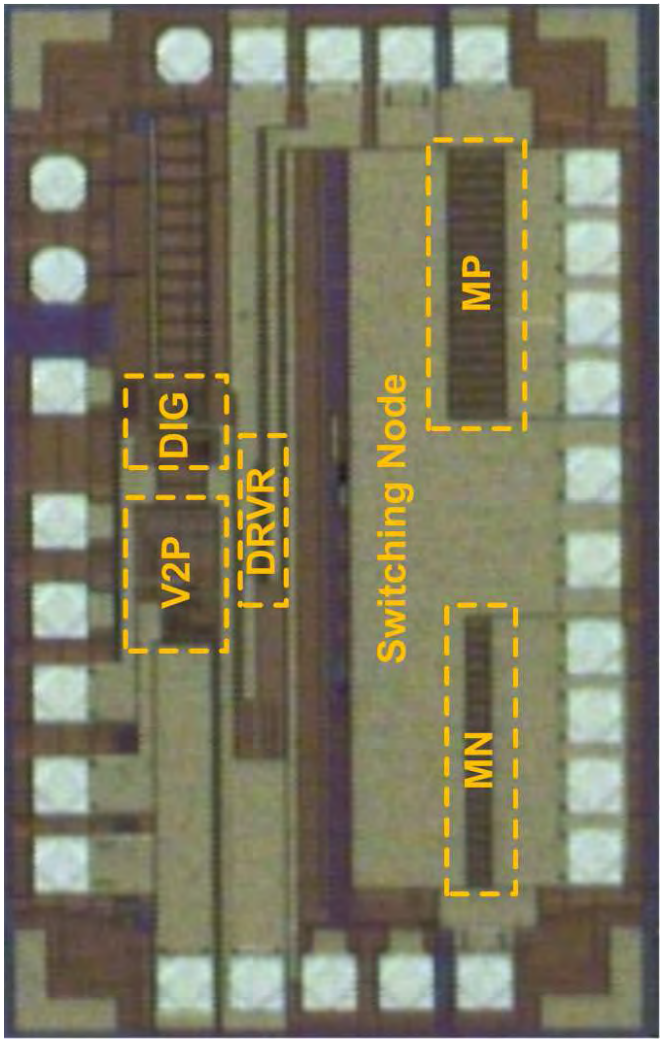

Fig 3.10: High switching frequency buck converter IC prototype microphotograph.

3.7 SINGLE-INDUCTOR 4-OUTPUT TEST PCB

In order to design the test PCB for the high frequency buck converter IC prototype, the guidelines discussed in Section 2.13 have been followed also for this work.

The Figure 3.11 shows the high frequency buck converter test PCB. Even for this design a 4-layer PCB has been provided. The top layer is red while the bottom layer is blue.

The middle1 (analog ground plane) and middle2 (digital ground plane) layers are not shown. The power top ground plane, the star connected input power supply traces and the output voltage trace can be noted.

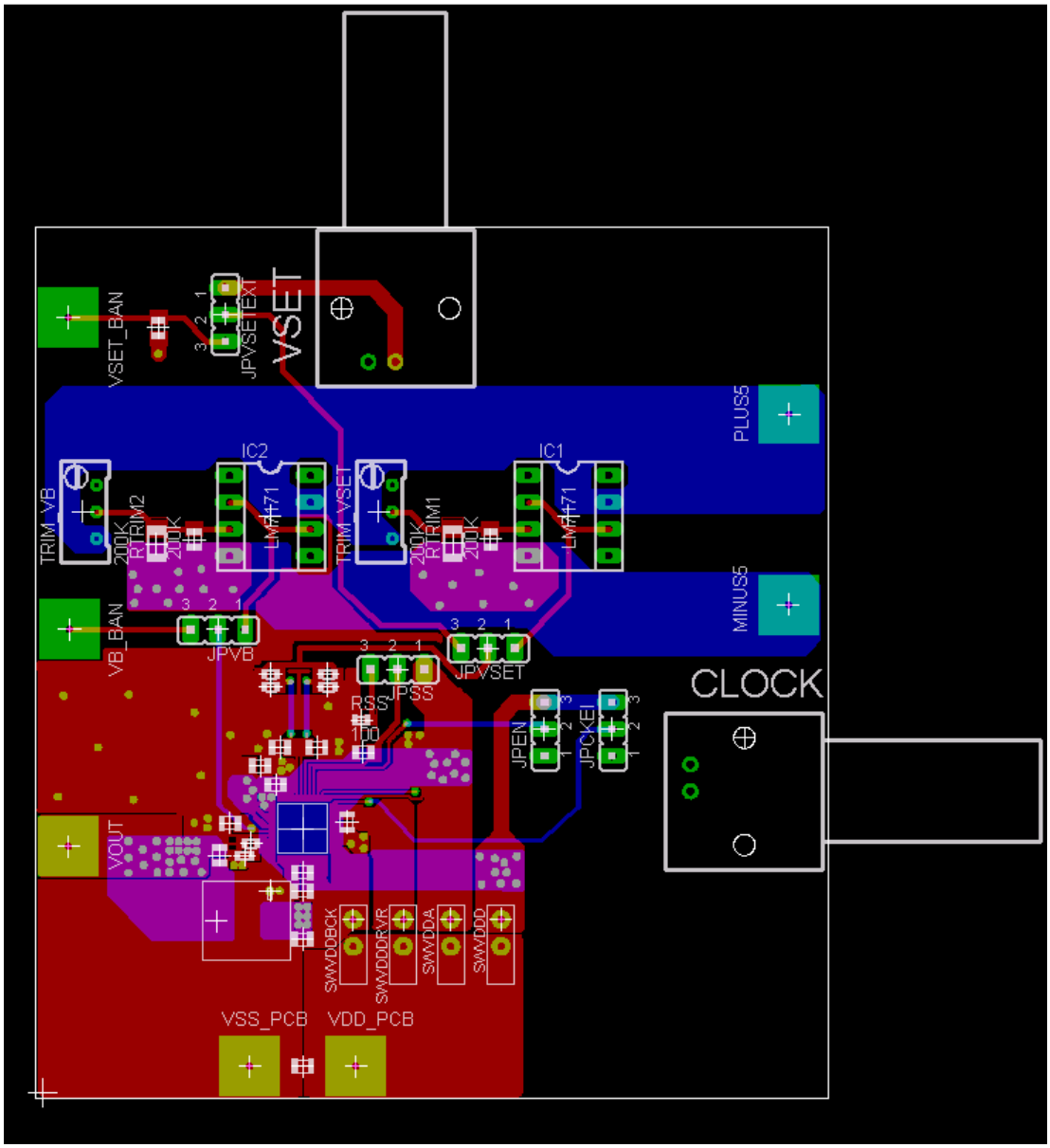

Fig 3.11: High switching frequency buck converter prototype test PCB.

In the Figure 3.12 the input bypass capacitor and the single point connection between the different ground plane have been highlighted.

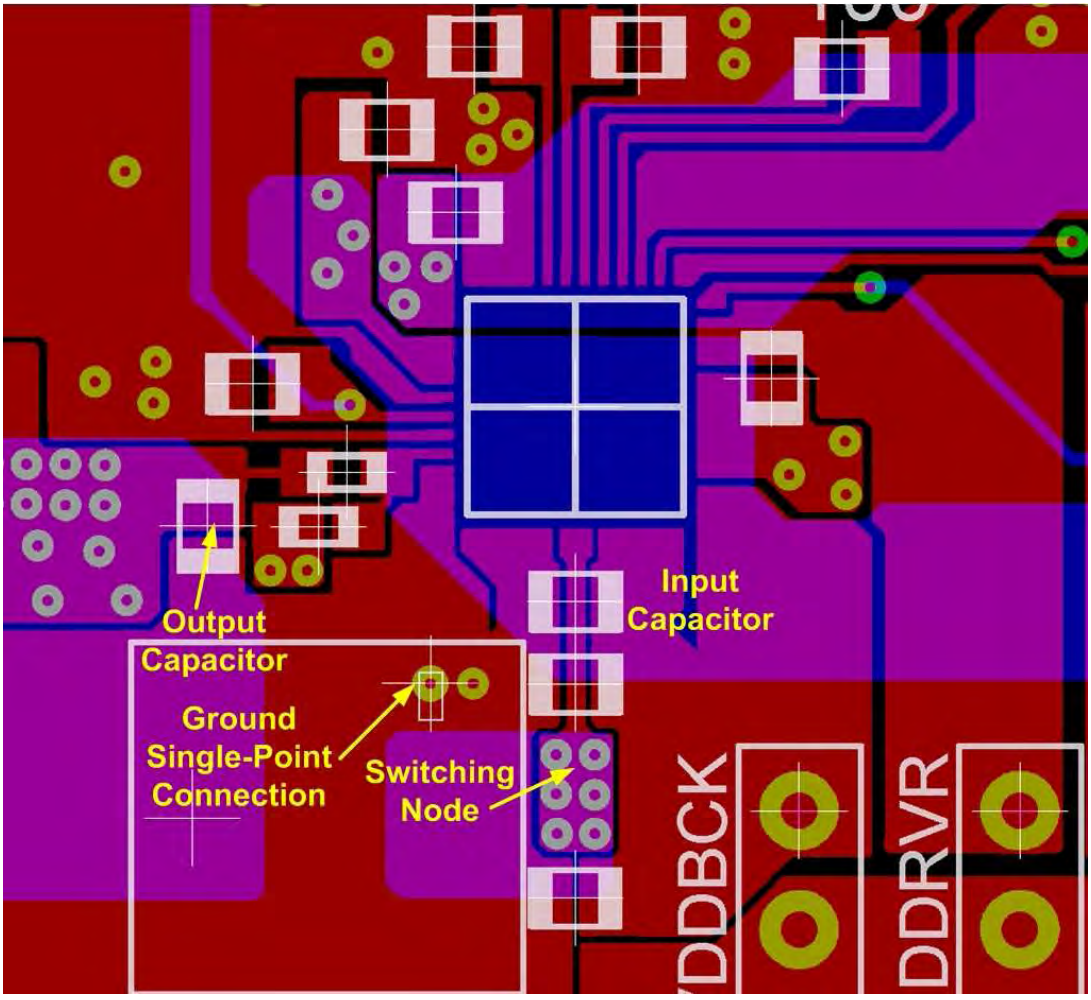

Fig 3.12: High switching frequency prototype test PCB details.

3.8 MEASUREMENTS RESULTS

Due to the limits of the used process technology, the applied supply voltage ranges from 2.2 to 2.8V.

The nominal switching frequency is 60MHz but the circuit has been also tested with a switching frequency of 120MHz.

Experimental results show that, at 2.2V minimum supply, the output regulation range from 0.5 to 2V with 1A output current capability.

Measurements show an increased output noise voltage due to the parasitic inductances introduced by current loops of the used probes.

The power efficiencies for V_{out} = 1.1V and 1.65V (V_{dd} = 2.2V, D = 0.5 and 0.75, respectively) are shown in Figure 3.13. The same Figure also gives the power efficiency with higher supply voltage (2.8V) and same values of D. Peak efficiency equals 92% and 93% for 2.8V and 2.2V supply voltages, respectively, and D = 0.75.

Higher supply causes larger dynamic dissipation and this worsens the efficiency at low currents. However, the low power of the control (only 45µA), sustains the overall efficiency at almost one decade below the peak.

The measured light load power efficiency it is roughly 20% lower than the simulated one. This is due to the fact that, since the used process do not employ thick metal layers, in order to meet the metal maximum current density constrains, the switching node metal trace is very wide, thus increasing its parasitic capacitance and then its associated dynamic losses.

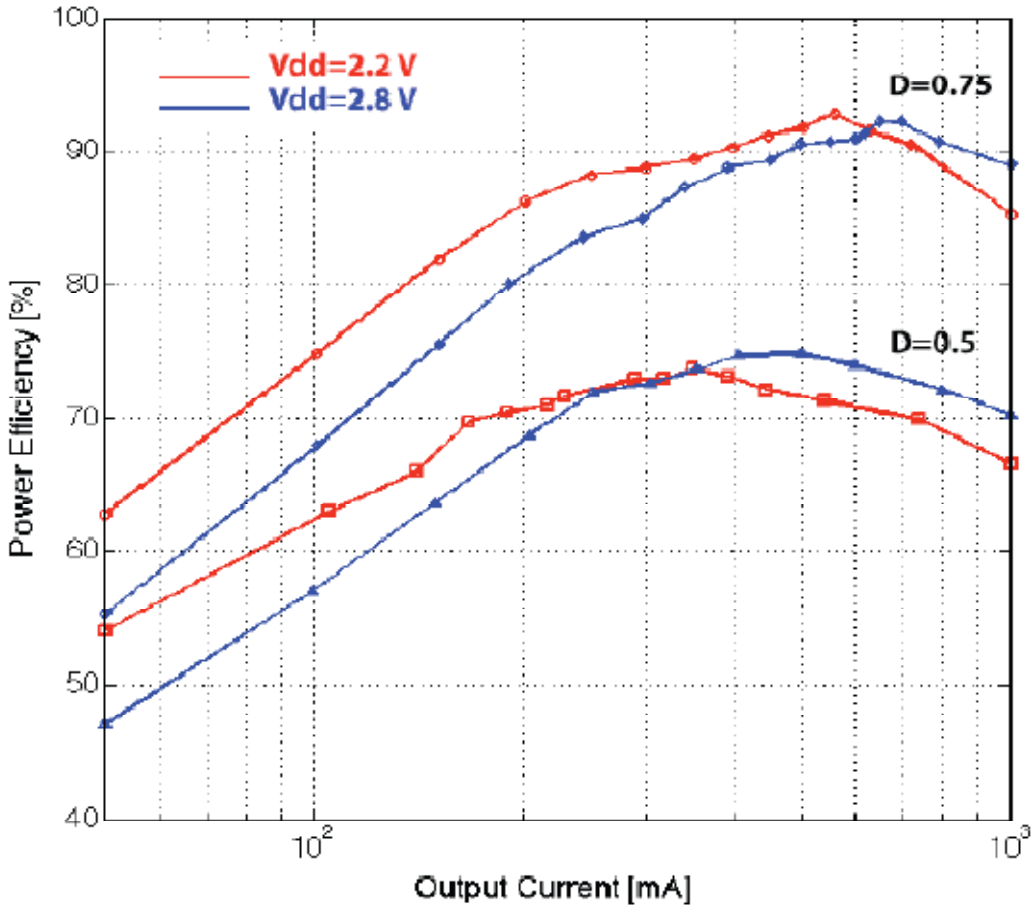

Fig 3.13: Measured system power efficiency with V_{dd}=2.2-2.8V, D=0.5-0.75 and 60MHz switching frequency.

Figure 3.14 shows a load regulation measurement with output current, I_L, switched from 0A to 500mA by on-off current control on PCB.

The load switching speed is 6µs and limits the overall load transient response time that is around 8µs (the simulated one was less than 2µs).

In this measurement the switching frequency is 60MHz while the supply voltage is 2.8V. The output voltage V_{out} is sets to 1.4V.

The low frequency ringing of the 1.4V output voltage is mainly caused by the PCB and probe coupling. For this measurement the load regulation is about 18mV/V.

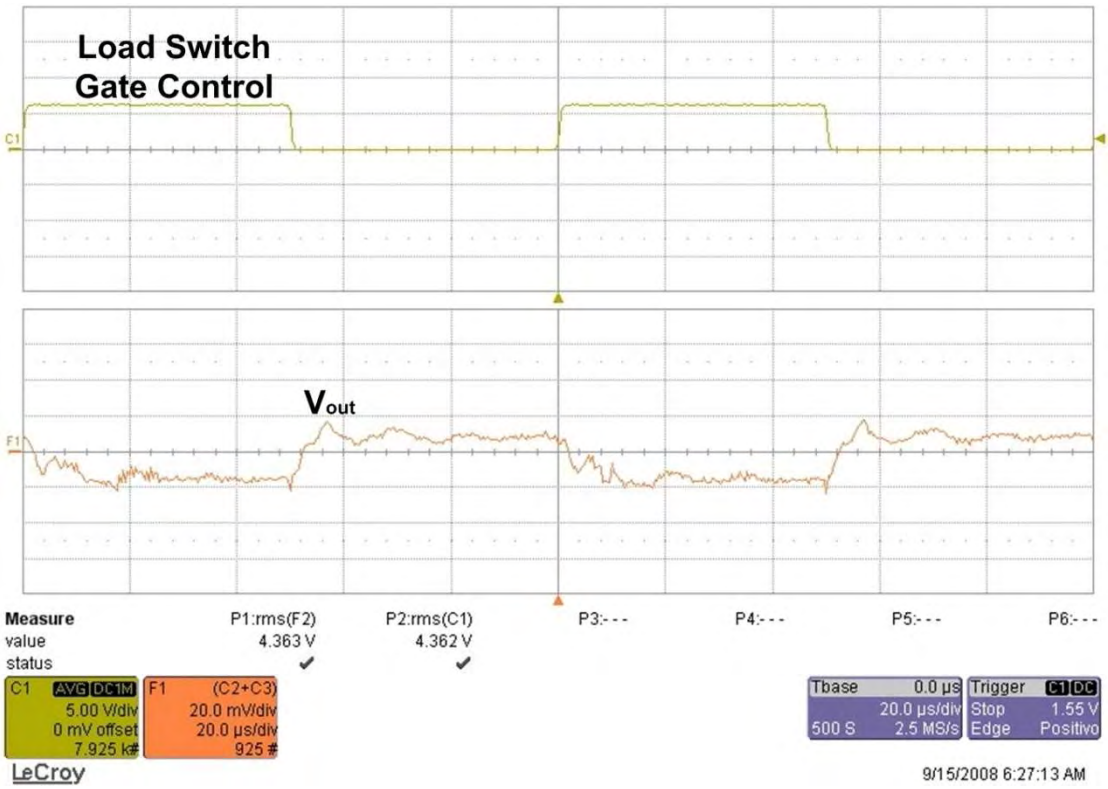

Fig.3.14: Load regulation measurement with a 50% duty cycle and 60MHz switching frequency.

Figure 3.15 shows a load regulation measurement with output current, I_L, switched from 0A to 500mA by on-off current control on PCB.

The load switching speed is still 6µs and limits the overall load transient response time that is around 7µs (the simulated one was less than 1µs).

In this measurement the switching frequency is 120MHz while the supply voltage is 2.8V. The output voltage V_{out} is sets to 1.4V.

As for the previous measurement, the low frequency ringing of the 1.4V output voltage is mainly caused by the PCB and probe coupling.

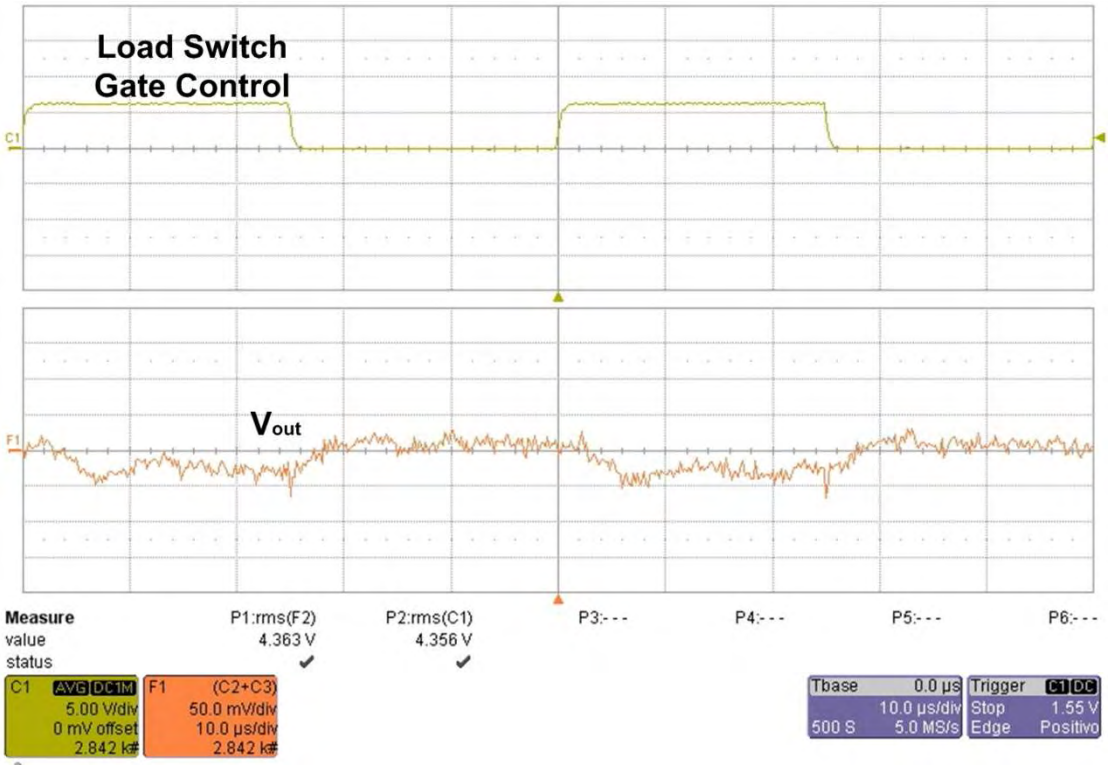

Fig.3.15: Load regulation measurement with a 50% duty cycle and 120MHz switching frequency.

Figure 3.16 shows a output voltage V_{out} measurement with a step input reference voltage V_{ref}, variation from 0.5V to 2.2V. It can be noted that the overall response time is around 10µs.

In this measurement the switching frequency is 60MHz while the supply voltage is 2.8V. The output load is 3Ω.

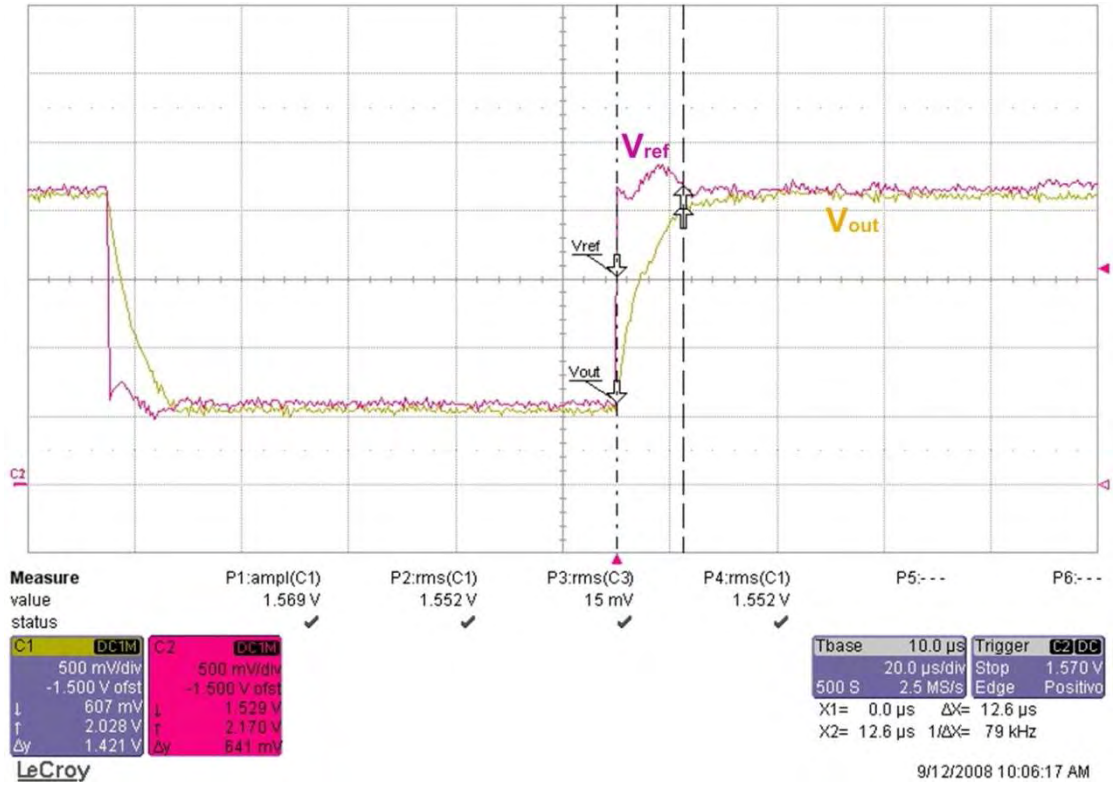

Fig.3.16: Input reference voltage step-variation measurement with 60MHz switching frequency.

Figure 3.17 depicts the line regulation measurements for two different output voltages (0.9V and 1.5V) and different load conditions (0 and 300mA output current).
The line regulation is always less than 6mV/V with no load and less than 0.5mV/V with an output current of 300mA.

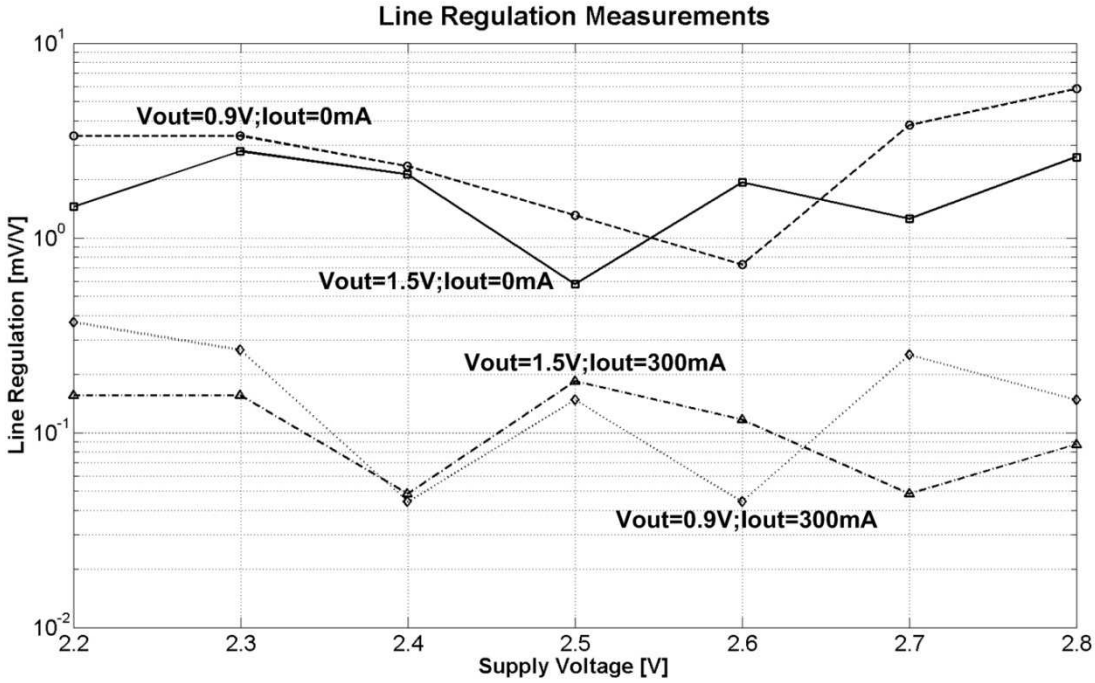

Fig.3.17: Line regulation measurement with 60MHz switching frequency.

Since the control is able to operate at higher frequency, allowing lower inductor values, the circuit has been tested also at 120MHz with halved inductance.

Even if the design is optimized for a switching frequency of 60MHz, with size of the power transistors such to obtain the peak efficiency higher than 90% of Figure 3.18, the circuit obtains good performance.

Figure 3.18 gives the obtained efficiency. The results are good.

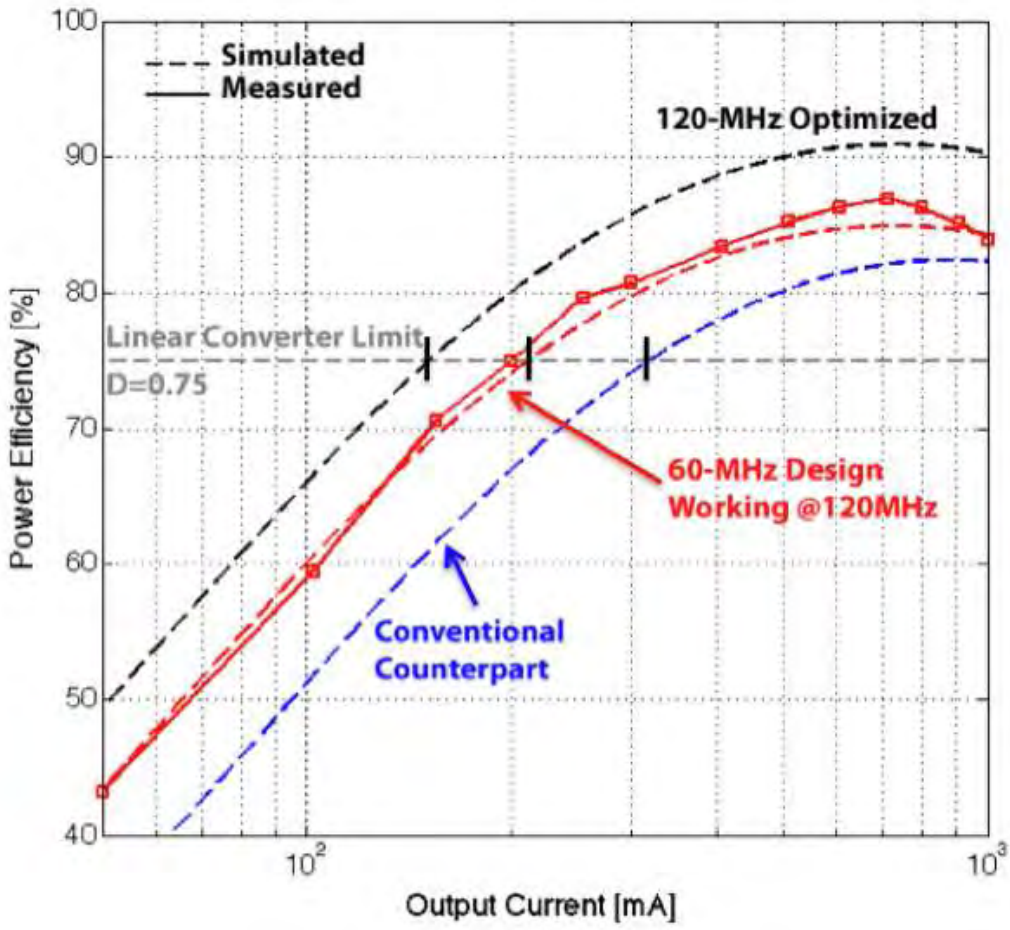

Fig.3.18: Measured and ad-hoc design estimated system power efficiency with V_{dd}=2.8V, D=0.75 and 120MHz switching frequency.

However, an ad-hoc design with a proper trade-off between static and dynamic dissipation would give even better results. The peak efficiency is 87% at 0.7A and the linear efficiency crossing point is 200mA.

The Figure compares the simulated efficiencies for this design and the one of the conventional counterpart. The crossing point is at 200mA for this circuit while it is at 320mA for the conventional counterpart. Simulations at the transistor level optimized for 120MHz switching frequency predict a peak efficiency of 91% at 0.56A and crossing point at 150mA (Figure. 3.18).

The measurements and simulation results show that the method may be used in SiP with inductors in the 10-15nH range and output capacitors of few µF.

With currents of hundreds of mA, the switching frequency can be further increased while maintaining high the peak efficiency.

3.9 HIGH FREQUENCY BUCK CONVERTER PERFORMANCE SUMMARY

Table 3.4 summarizes the measured system performance.

Supply Voltage [V]	2.2→2.8
Output Voltage [V]	0.5→ (V_{dd}-0.2)
Output Current [A]	0→1
Nominal Switching Frequency [MHz]	60
Allowed Switching Frequency [MHz]	Up to 120
Inductor [nH]	36
Output Capacitor [µF]	4.7
Max Output Voltage Ripple [mV]	10
Peak Power Efficiency @ 60MHz [%]	93
Peak Power Efficiency @ 120MHz [%]	88
Max Line regulation [mV/V]	8
Load Regulation @ 60MHz [mV/V]	20
Load Regulation @ 120MHz [mV/V]	25

Tab.3.4: Circuit performance summary.

REFERENCES

[1] J. Wibben and R. Harjani, "A High-Efficiency DC–DC Converter Using 2 nH Integrated Inductors", *IEEE J. of Solid-State Circuits*, vol. 43, pp. 844-854, April 2008.

[2] M. Wens and M. Steyaert, "A Fully-Integrated 130nm CMOS DC-DC Step-Down Converter, Regulated by a Constant On/Off-Time Control System", *Proc. of 2008 IEEE European Solid-State Circuits Conference*, pp. 62-65, Sept. 2008.

[3] P. Hazucha, G. Schrom, J. Hahn, B.A. Bloechel, P. Hack, G.E. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233-MHz 80%–87% Efficient Four-Phase DC–DC Converter Utilizing Air-Core Inductors on Package", *IEEE J. of Solid-State Circuits*, vol. 40, pp. 838-845, April 2005.

[4] K. Onizuka, K. Inagaki, H. Kawaguchi, M. Takamiya, and T. Sakurai, "Stacked-Chip Implementation of On-Chip Buck Converter for Distributed Power Supply System in SiPs", *IEEE J. Solid-State Circuits*, vol. 42, pp. 2404-2410, Nov. 2007.

BIBLIOGRAPHY

[1] R. W. Erickson and D. Maksimovic, "Fundamentals of Power Electronics (Second Edition)", Kluwer Academic Publisher, 2004.

[2] National Semiconductor Corporation, "Meeting Power Design Challenges – High-Performance Seminar Series 2007".

[3] National Semiconductor Corporation, "Knowledge is Power – Power Design Technical Courses 2007".

[4] National Semiconductor Corporation web-site, http://www.national.com.

[5] Maxim Corporation web-site, http:// www.maxim-ic.com.

CHAPTER 4

A MICRO-POWER CHOPPER CORRELATED DOUBLE SAMPLING AMPLIFIER

Many instrumentation applications need operational amplifiers with very high gain (more than 120dB) and extremely low offset. These op-amps are used to obtain large voltage gain, typically 60dB or more. Since the bandwidth of used signals is low, the speed requests are limited and often a cut-off frequency f_T as low as 100kHz is enough. The input referred offset must be in the µV range and, in addition, the power consumption has to be very low to meet portable applications requirements.

The above requests are conventionally satisfied by the autozero or the chopper stabilization techniques, [1] and [2].

However, the need of ultra low power makes the autozero technique unsuitable because it is necessary to use very large autozero capacitors. The only usable method is the chopper stabilization technique that works well at low frequency, but generates spurs at multiples of the chopping frequency. The cancellation of spur tones requires on chip low pass or band-pass filters whose implementation increases the complexity and the power consumption.
This innovative design uses chopper modulation, but avoids the chopper ripple at the chopping frequency by combining input chopping with correlated double sampling (CDS) technique at the output of the amplifier first stage.

4.1 CONVENTIONAL SOLUTIONS AND LIMITS

Nowadays, the two basic techniques widely used to reduce the offset and the low-frequency noise of op-amps, are the autozero and the chopper stabilization techniques. The fundamental difference between them is the offset handling.
While the autozero principle first measures the offset and then subtracts it in a next phase, the chopper approach modulates the offset to higher frequencies.
In this section both approaches are described and discussed, highlighting advantages and drawbacks of each technique.

4.1.1 AUTOZERO TECHNIQUE

A basic scheme to implement the autozero technique is depicted in Figure 4.1.
As already mentioned, the autozero process requires at least two phases: a sampling phase (P1) during which the offset voltage, V_{OS}, and the noise voltage, V_N, are sampled and stored, and a signal-processing phase (P2) during which the offset-free stage is available for operation.
During the sampling phase, the amplifier is disconnected from the signal path. Its inputs are short-circuited and set to an appropriate common-mode voltage.

The offset is nulled using an auxiliary input port in the analog or in the digital domain by means of an appropriate feedback configuration and/or a dedicated algorithm.
As a result, the DC offset is completely cancelled out, as required in high precision amplifiers.

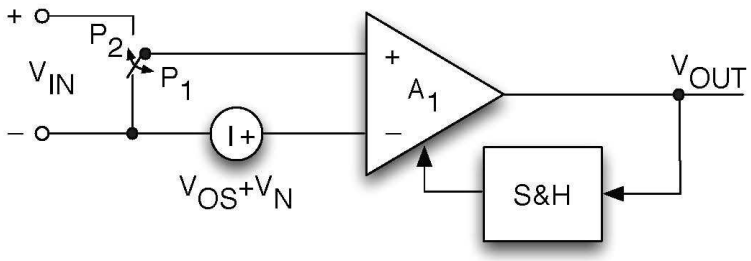

Fig. 4.1: Basic scheme for autozero technique.

Besides the offset, the autozero technique also removes the amplifier 1/f noise, which makes sense because offset can be considered as low-frequency noise.
Since the efficiency of the autozero process for the noise reduction strongly depends on the correlation between the noise sample and the instantaneous noise value from which this sample is subtracted, the wideband thermal noise component is not reduced.
The typical input referred noise power spectrum of an autozero amplifier shows, at frequencies lower than the autozeroing frequency, an almost white residual noise. However, this residual noise is not equal to the thermal noise floor, as it is increased by the ratio of the unity-gain bandwidth of the amplifier and the autozeroing frequency. The reason for this is that, due to the sampling action, the high-frequency noise components are folded back to the baseband. The higher the bandwidth of the amplifier, the more noise is sampled on the storing capacitor.
Another drawback of this circuit is that the charge injected by the switches is also stored on sampling capacitors leading to an additional residual offset.

4.1.2 CHOPPER TECHNIQUE

An alternative technique for the suppression of the low frequency noise and offset is the chopper stabilization technique. The latter is substantially different with respect to the autozero technique since the chopper approach does not use sampling, but it applies modulation to transpose the signal to a higher frequency where there is no 1/f noise, and then demodulates it back to the baseband after amplification.
The scheme of Figure 4.2(a) describes the principle of chopper technique.

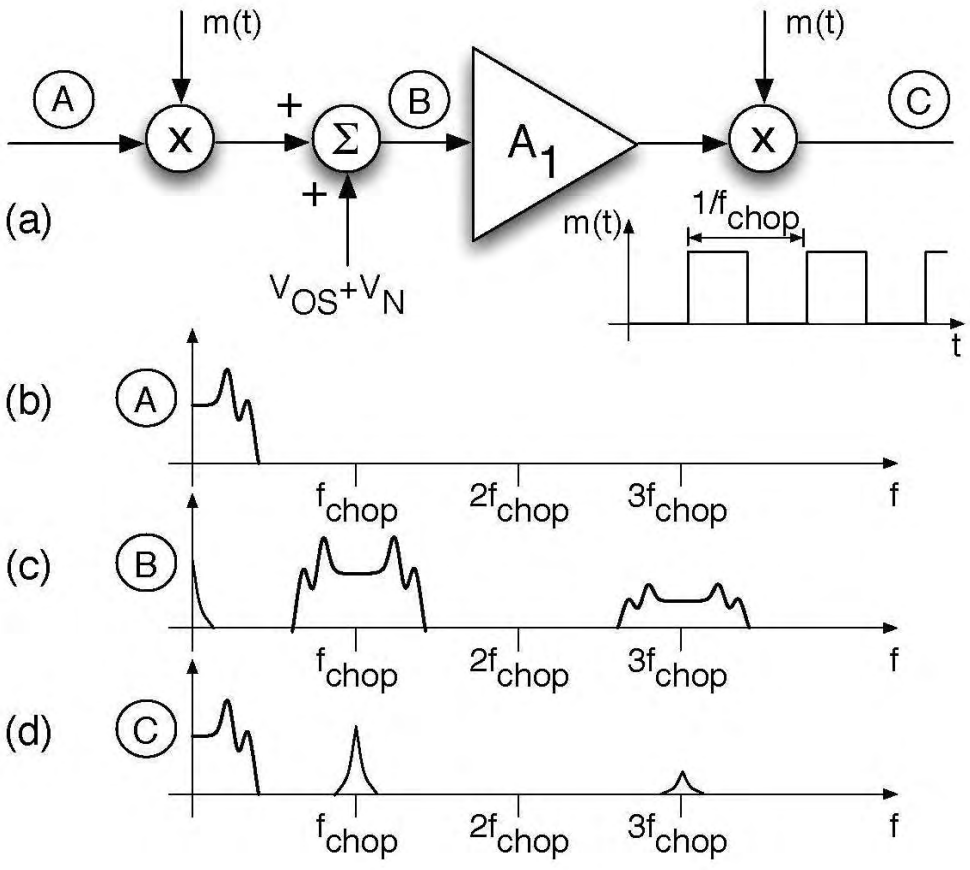

Fig. 4.2: Basic scheme for chopper technique.

The band limited input signal is multiplied by the square wave carrier signal m(t) with period $T = 1/f_{chop}$. After this modulation, the signal is added to the offset voltage and to the 1/f noise and it is transposed to the odd harmonic frequencies of the

modulation signal. It is then amplified and it is demodulated back to the original band, as shown in the conceptual spectra shown in Figure 2(b-d). It results that spurs at f_{chop} and its odd multiples deteriorate the output spectrum.

A low-pass filter can possibly reduce the amplitude of the offset and the 1/f noise contributions. At low frequencies, the input referred noise of a chopper amplifier is then be determinate by operational amplifier white noise floor.

In many cases, even after filtering, residual spurs are still present in the output spectrum and this, in many applications, cannot be accepted.

The above drawback can be overcome by using an intentionally jittered chopper signal, [3], which blurs the spurs power and spreads it around f_{chop} and its multiples. The method is effective, but the level of the noise floor increases and, therefore, there is a trade-off between the achieved noise floor level and the presence of spur tones. An alternative solution consists in removing the spur tones by using a notch filter, that replaces or is placed after the low-pass filter [4], centered at f_{chop} and multiples.

In this case, the required notch filter implies additional circuitry and can be both implemented with active or passive SC scheme.

4.2 PROPOSED RIPPLE-FREE CHOPPER STAGE

The innovative solution proposed in this work avoids the generation of the spur tones at the chopping frequency and its multiples by removing the second chopper. This ripple free operation is obtained with a sampled data correlated double sampling block at the output of the amplifier first stage, as schematically shown in Figure 4.3.

The chopped input signal, added to offset and 1/f noise, is amplified by A_1. Assuming that offset and 1/f noise do not saturate the amplifier A_1, their contribution is removed by the AC coupling, while the input signal is detected by the correlated double sampling method.

During one phase, capacitor C_{cds} is charged to the output while, during the complementary phase, the output drives the series of the pre-charged capacitors C_{cds} and C_s.

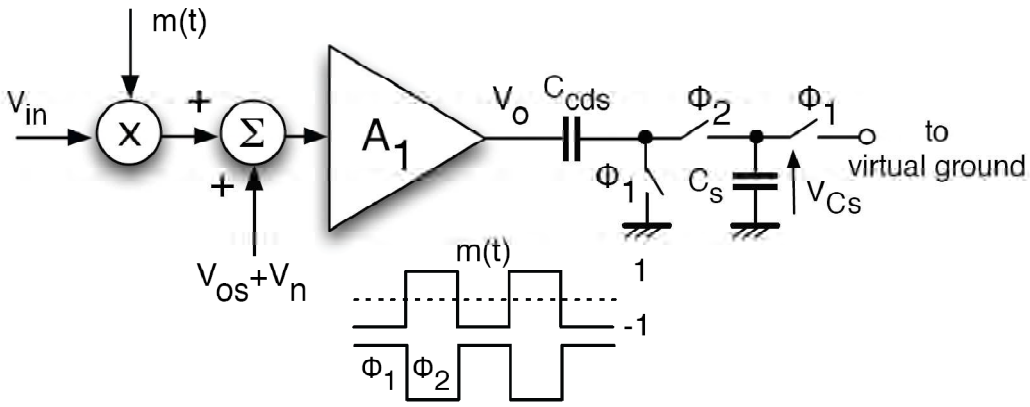

Fig. 4.3: Simple single path CDS scheme.

Thanks to the input chopping, the output voltage V_o is:

$$V_O(1)=A_1\cdot\left[\left(-V_{in}(1)+V_{os}\right)+V_n(1)\right] \tag{4.1}$$

$$V_O(2)=A_1\cdot\left[\left(+V_{in}(2)+V_{os}\right)+V_n(2)\right] \tag{4.2}$$

where V_{os} and V_n are the offset and the input referred noise, respectively. By inspection of Figure 4.3, during Φ_1:

$$Q_{cds}(1)=-V_{o1}(1)C_{cds} \tag{4.3}$$

$$Q_{Cs}(1)=0 \tag{4.4}$$

Therefore, during Φ_2, the voltage across C_s becomes:

$$V_{Cs}(2)=C_{cds}\cdot\frac{-V_o(1)+V_o(2)}{C_{cds}+C_S} \tag{4.5}$$

that, using (4.1) and (4.2), becomes:

$$V_{Cs}(2) = \frac{A_1 C_{cds} \cdot \left[V_{in}(1) + V_{in}(2) - V_n(1) + V_n(2) \right]}{C_{CDS} + C_S} \tag{4.7}$$

showing that the input signal passes through the sampled data function $(1+z^{-1})$ while the noise through the high pass function $(1-z^{-1})$. Since this method does not involve any chopping of the amplified offset, no coupled ripple results.

Equation (4.7) verifies the high-pass attenuation of the 1/f noise. However, the power of the white noise doubles. This is a cost of this method and the one used in [4] that mainly involves the input referred noise of the amplifier A_1.

The 2kT/C noise of the output sampling is negligible being referred to input divided by A_1^2.

Actually, the output of the first amplifier is differential. Also, it is better to have a control of the next amplifier during both phases. Therefore, a complete scheme of the method is the one of Figure 4.4 that uses two CDS structures working in ping-pong fashion on both outputs.

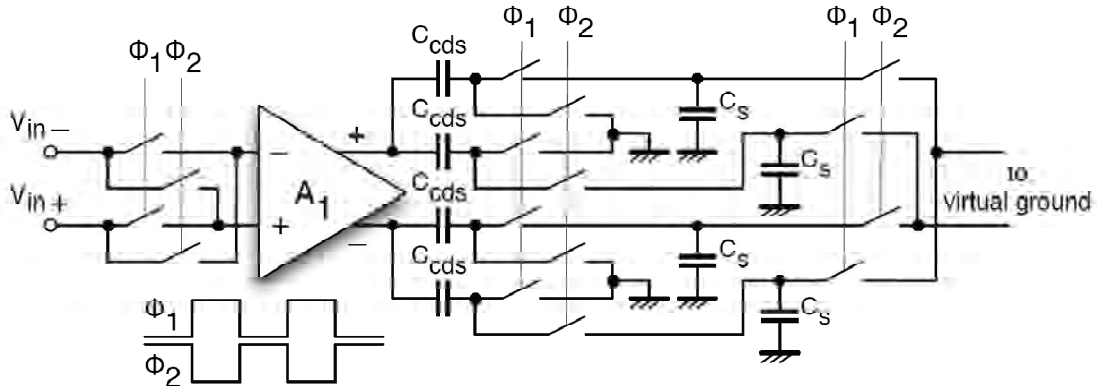

Fig. 4.4: Chopper and CDS scheme.

Notice that the AC coupling at the output of the gain stage naturally removes offset, but opens the loop at DC.

To remain in a linear region of operation, it is required to keep the input referred offset low and to limit its amplification.

Therefore, the proposed circuit implementation uses a band pass amplifier with low gain at DC and high gain at the chopping frequency. Figure 4.5 shows the conceptual implementation of the amplifier.

The capacitor C between the sources of the input pair transistors, M1 and M2, at the chopping frequency establishes a low impedance. Then, at f_{chop}, the stage gain is determined by the transconductance of the input pair and the output resistance.

While, at DC, the input pair is disconnected and the stage gain is given by the ratio between the output resistance and one of the bias current sources output resistance.

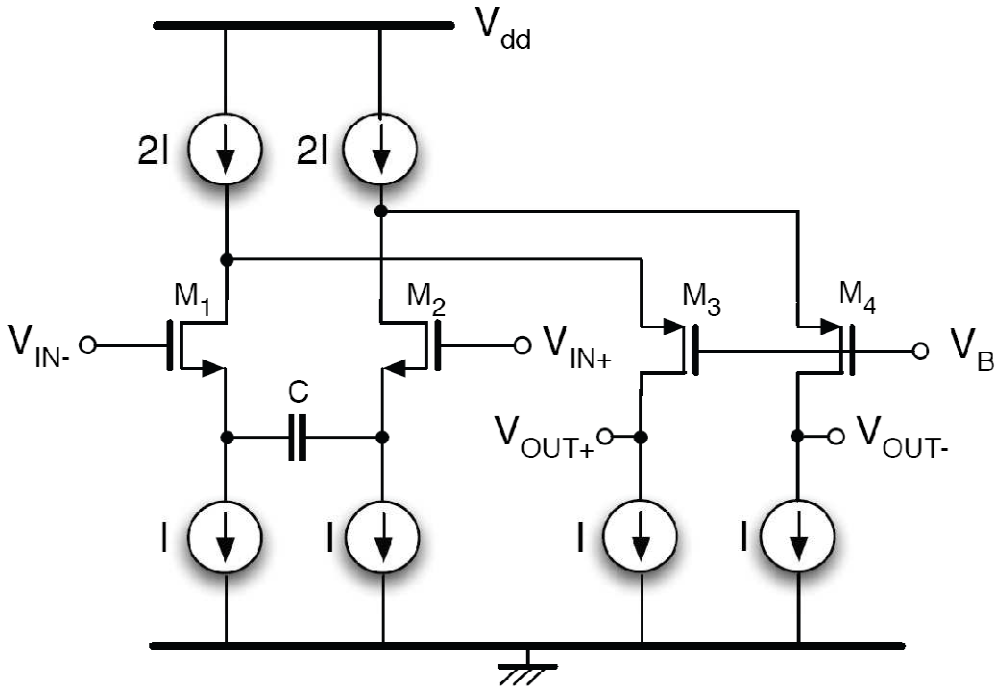

Fig. 4.5: Schematic diagram of an amplifier with band-pass response.

4.3 PROPOSED CHOPPER CDS AMPLIFIER ARCHITECTURE

Figure 4.6 shows the overall block diagram of the proposed amplifier architecture.

The chopped input signal, added to offset and 1/f noise, is amplified by the first stage. Assuming that offset and 1/f noise do not saturate the amplifier first stage, their

contribution is removed by AC coupling, while the signal is detected by the correlated double sampling method, as discussed in Section 4.2.

During one phase, two of the four C_{cds} capacitors are charged to the differential outputs and, during the complementary phase, they are connected to C_s. The other two capacitors operate with complementary control.

Since the term due to signal is inverted because of chopping and C_s has been discharged during the previous phase, the charge on C_s is $2V_dA_1C_{cds}/(C_{cds}+C_s)$, where V_d is the differential input and A_1 the voltage gain. This charge is then integrated into C_C during the next phase to obtain the output voltage.

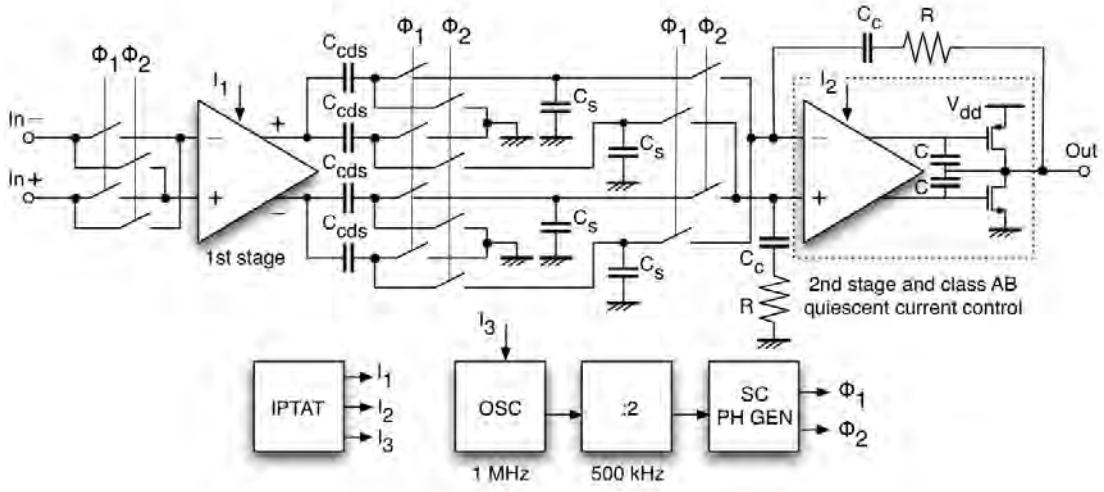

Fig. 4.6: Chopper CDS amplifier block diagram.

The scheme of Figure 4.6 includes a cascode second stage that drives a class AB output stage whose bias control limits the AB quiescent current.

The reference currents mirror a IPTAT main current source for minimizing the temperature dependence of the residual offset.

The 500kHz on-chip phase generator is based on a 1MHz ring oscillator.

The relatively high chopping frequency enables a wide signal band and spreads the folded noise in a wide frequency band.

Since the method does not involve any chopping of the amplified offset, no coupled ripple results. Indeed, the CDS of the chopped signal obtains demodulation, but does not involve the offset.
However, correlated double sampling operates on the 1/f noise. This CDS action is mitigated by the band-pass response of the first amplifier that provides low gain at low frequency.

4.4 FIRST STAGE BAND PASS AMPLIFIER WITH RAIL-TO-RAIL INPUT

Figure 4.7 shows the schematic diagram of the first stage band pass amplifier with rail-to-rail input. It is a differential folded cascode architecture with complementary input pair stages.
The use of zero-threshold transistors optimizes the dynamic range at input and output and allows the use of cascode configuration in each current mirror branches.
The input voltage is rail-to-rail thanks to the complementary input pairs and thanks to an adaptive bias currents generator that senses the input common-mode voltage and achieves the right node current balance.
The impedance between the sources of the NMOS input pair, MN_0 and MN_1, and PMOS input pair, MP_0 and MP_1, at the chopping frequency f_{chop} is low, because of the large coupling capacitors C_N and C_P (30pF). Indeed, at f_{chop}, the stage gain is almost determined by the sum of the transconductance of the PMOS and NMOS input pairs and the output resistance.
While, at DC, the two input pairs are disconnected and the stage gain is given by the ratio between the output resistance and one of the two cascodes that make the bias current sources. Moreover, the low frequency differential gain is further reduced by a DC lock of the output voltages that operates as a CMFB.

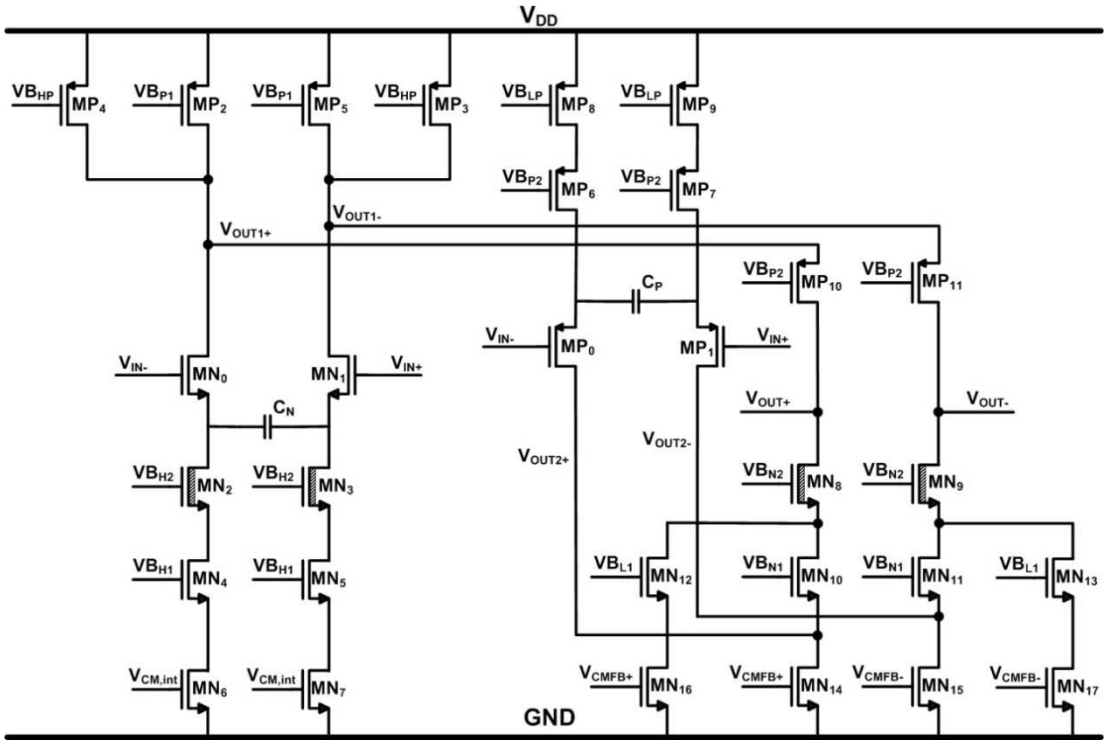

Fig. 4.7: First stage amplifier schematic diagram.

Unity gain buffers and band-reject networks realize an inner closed loop toward auxiliary inputs, MN_{14}, MN_{15}, MN_{16},and M_{17}. The inner loop provides 0dB attenuation at low and high frequency. Therefore the inner feedback becomes ineffective in the rejection band.

Figure 4.8 shows the DC lock circuit details. Capacitors C_0 and C_1 are 6pF, while C_2 and C_3 are 50fF. Resistors R_0 and R_1 are 500KΩ. The output buffers bias current is 400nA.

PMOS transistors fixed bias voltages, VB_{P1} and VB_{P2}, and NMOS transistors fixed bias voltages, VB_{N1} and VB_{N2}, are provided by a conventional cascode-arrangement bias circuit shown in Figure 4.9.

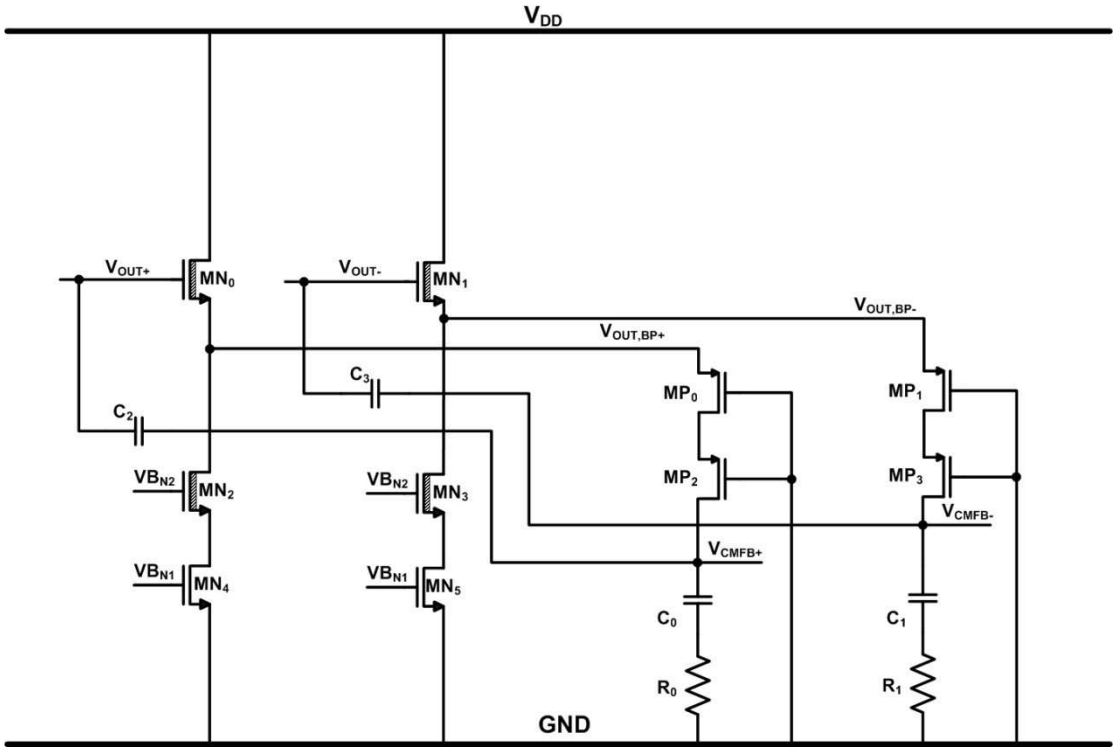

Fig. 4.8: DC lock circuit details.

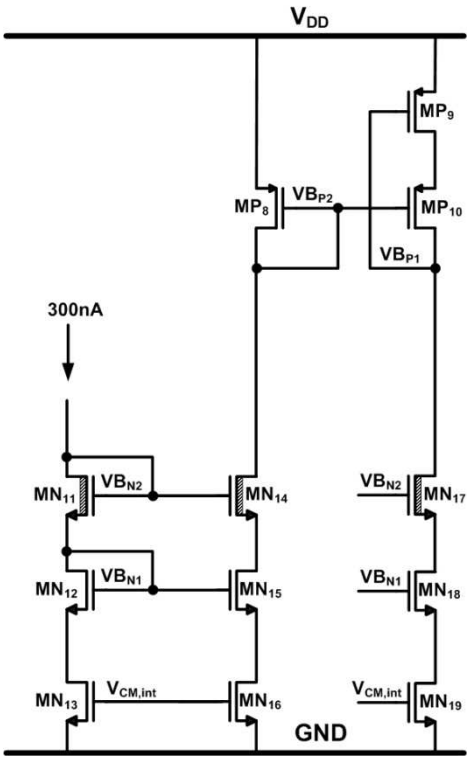

Fig. 4.9: Fixed bias voltages generator circuit.

PMOS and NMOS transistors adaptive bias voltages, VB_{HP}, VB_{LP}, VB_{L1}, VB_{H1} and VB_{H2} are provided by the adaptive reference generator circuit shown in Figure 4.10 This adaptive bias generator achieves amplifier first stage rail-to-rail input operations. Voltage $V_{CM,int}$, provided externally by a pad, is the internal common mode and has been designed at 1.1V.

Therefore, due to the DC lock circuit feedback loop, at DC, the first stage positive and negative output voltages are locked at 1.1V regardless of the input common mode voltage.

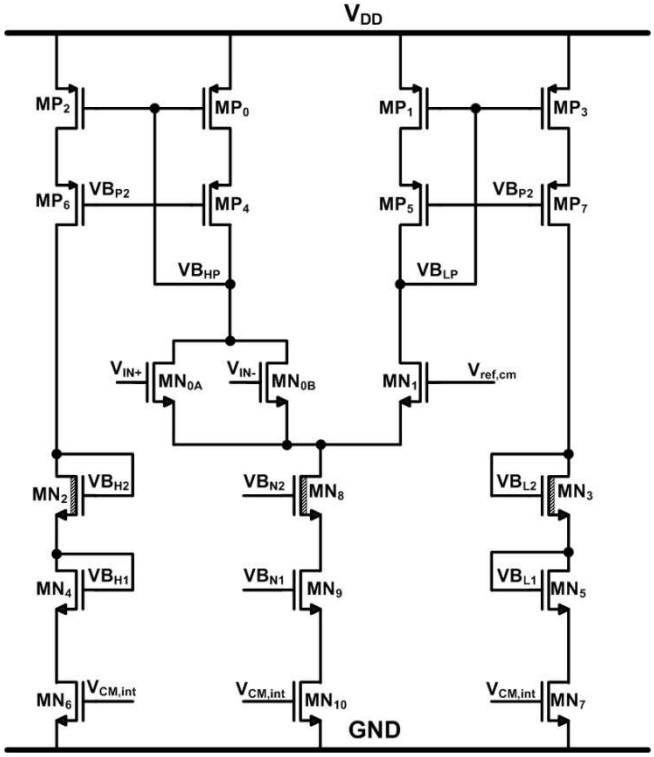

Fig. 4.10: Adaptive bias voltages generator circuit.

The input common mode voltage is sensed by the transistors MN_{0A} and MN_{0B}. If this voltage equals the reference voltage $V_{ref,com}$ (designed as one half of the supply voltage), the differential pair bias current I_{MN9} is equally divided in each side branch. Then, both PMOS and NMOS first stage input pairs work.

Consider now the case in which the input common mode voltage equals V_{DD}. Then, the input pair bias current I_{MN9} flows entirely into the left branch, while the right

branch is off. Therefore only the NMOS input pair, NM_0 and NM_1, works. Thus, current balance in each first-stage amplifier node is achieved.

On the other and, if the input common mode voltage equals 0, then the input pair bias current I_{MN9} flows entirely into the right branch, while the left branch is off. Therefore only the PMOS input pair, PM_0 and PM_1, works. Then, current balance in each first-stage amplifier node is still achieved.

The simulated results show a DC gain of -20dB and 51dB at the chopping frequency. The peak of the gain is at around 112kHz.

The 300nA input bias current is provided by the PTAT bias current generator as already mentioned. The first stage band pass amplifier overall current consumption (considering band pass amplifier, bias circuit and DC lock) is 9µA. The noise voltage at the chopping frequency is white and it is around 35nV/√Hz.

4.5 SECOND STAGE WITH RAIL-TO-RAIL CLASS AB OUTPUT

As already mentioned, the second stage is composed by a folded cascode amplifier with rail-to-rail class AB output.

A class A output stage would be not suitable for this design. In fact, even if the class A output has the advantage of easy biasing, it has the disadvantage of limited current-drive in one of the directions. Biasing the class A at a high current level may alleviate that disadvantage, but then it is no longer a low current design.

Then, a class AB output stage has been chosen in order to achieve low current design together with heavy loads driving capability.

The traditional class AB output stage is a source-follower and it is shown in Figure 4.11. It can be biased at a low voltage level and still it provides high currents for heavy loads. However, it is not rail-to-rail.

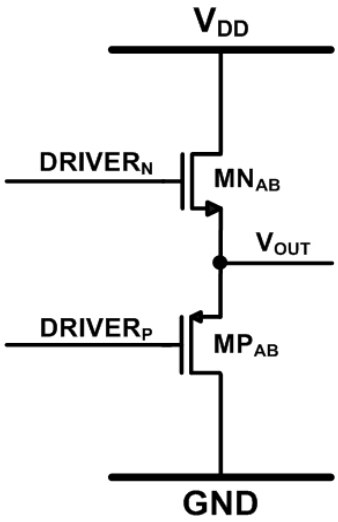

Fig. 4.11: Traditional source-follower class AB output stage.

Since this design requires rail-to-rail outputs in most cases, the class AB output stage must be drain-driven style. Figure 4.12 shows the common approach that uses the floating current sources MP_0 and MN_0.

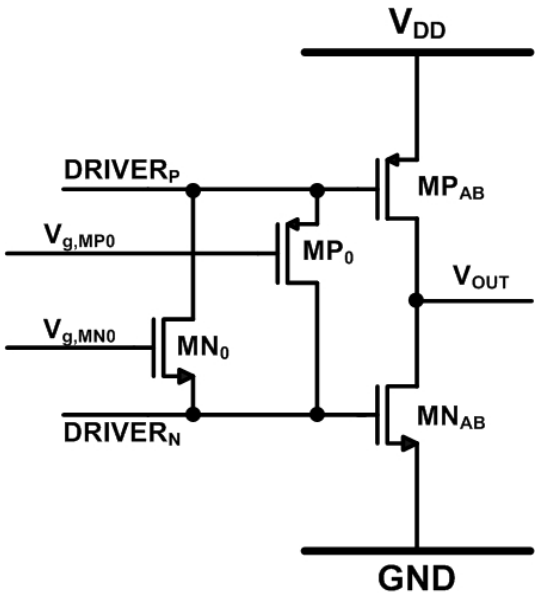

Fig. 4.12: Class AB output stage with floating current sources MP_0 and MN_0.

However, this architecture requires a supply voltage higher than two times V_{gs} plus a saturation voltage V_{dsat}.

Then, considering also process corners, this circuit is not suitable for the 1.8V minimum supply voltage design requirement.
Therefore, the designed class AB output stage must have the following features:

- Rail-to-rail output.
- Low quiescent current and high drive-current capability.
- Input supply voltage wide margin: V_{gs} plus V_{dsat} design.

The circuit in Figure 4.13 achieves these goals. It is composed by a NMOS input pair folded cascode with a split cascode that drives the class AB output stage.
In this circuit, the output stage (MP_{AB} and MN_{AB} transistors) is biased at 1.2uA, monitoring the output driver current.
If the bias current increases, that would increase the voltage fed back to MP_{0P}. That, in turn, would pull down the $DRIVER_N$ voltage and push up the $DRIVER_P$ voltage, thus restoring the proper bias voltage level.
The differential current from the NMOS input pair (MN_0 and MN_1 transistors) acts on the folded cascode to increase both $DRIVER_P$ and $DRIVER_N$ which would drive Vout low. Or, in the opposite direction, both drivers would drive Vout high thus providing voltage gain.
The output is single ended. In order to minimize the input offset voltage, for the NMOS input pair has been used 0.18µm gate length transistors which drain voltage are protected by the NMOS natural cascode transistors MN_2 and MN_3.
In fact, transistor level simulations show that, for the used process, a 0.5µm NMOS transistors input pair (with same aspect ratio) leads to higher input referred offset voltage. NMOS input pair transistor MN_0 and MN_1 have W=1.2mm and L=1.6µm.
Resistors R_1 and R_2 slightly decrease the overall voltage gain but help in reducing the contribution of PMOS transistors MP_2 and MP_3 to the input referred offset.
Cadence Monte Carlo simulation show that the stage has an input referred systematic offset of about 25µV with a sigma variation of about 200µV.

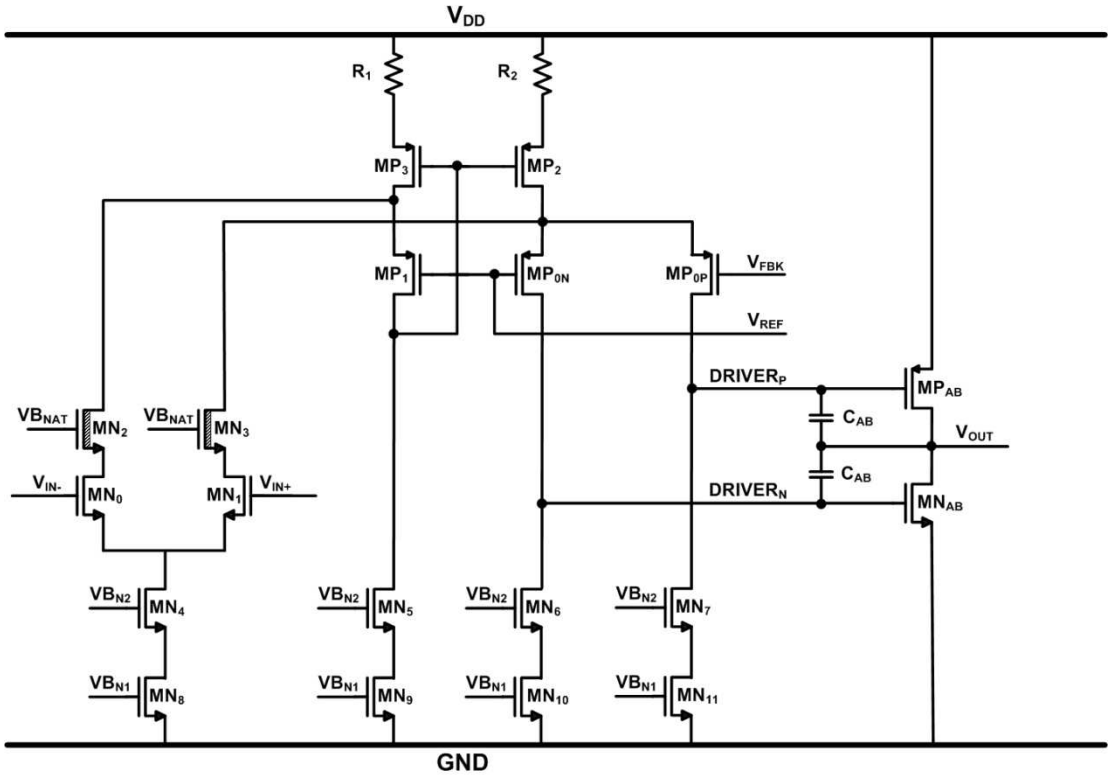

Fig. 4.13: Second stage with class AB output.

The two capacitors C_{AB} form the Miller capacitances wrapped around the drivers MP_{AB} and MN_{AB} respectively.

Therefore, the cost of this class AB architecture is that two Miller caps are needed. In this design, they are each 3pF, and the output can drive a 1nF cap load. Their size could be reduced, at the expense of a higher output stage bias, or reduced capacitive load drive.

PMOS driver MP_{AB} transistor has W=120µm and L=2µ while NMOS driver MN_{AB} transistor has W=48µm and L=2µ.

Natural NMOS transistor bias voltages VB_{NAT} and cascode current mirrors bias voltages VB_{N1} and VB_{N2} are provided by the circuit shown in Figure 4.14.

The 100nA input current is provided by the PTAT current generator that will be described in Section 4.6.

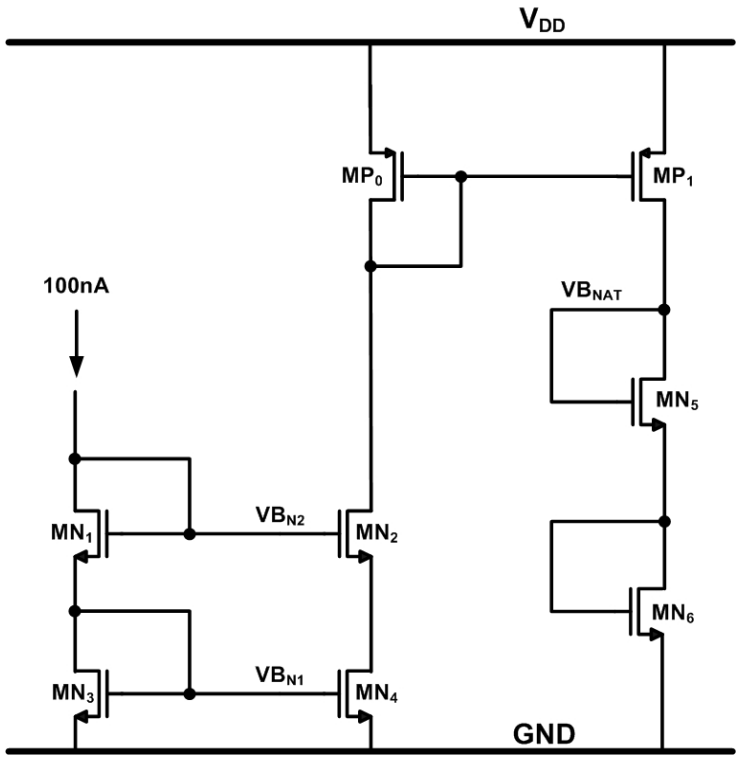

Fig. 4.14: Second stage with class AB output bias circuit.

4.5.1 CLASS AB BIAS CURRENT MONITOR AND FEEDBACK

The implemented class AB bias current monitor circuit is shown in Figure 4.15.

The monitoring of the output-stage bias current is done by MOS devices $MP_{AB,mirror}$ and $MN_{AB,mirror}$ interleaved with the drivers in the layout. Monitor transistors are six times smaller than the drivers.

A PMOS mirror is necessary for the monitored current from the n-driver.

In this design, the monitor current levels are at 100nA and they flow into a pair of resistors, R_2 and R_3, to establish a proper bias level for the split cascode.

The diode connections of MP_1 and MP_2 establish the proper bias level V_{FBK} for the PMOS transistor MP_{0P}. A similar structure establishes a reference level V_{REF} for MP_{0N}. With 5V input supply, the V_{REF} and V_{FBK} voltages are 3.85V.

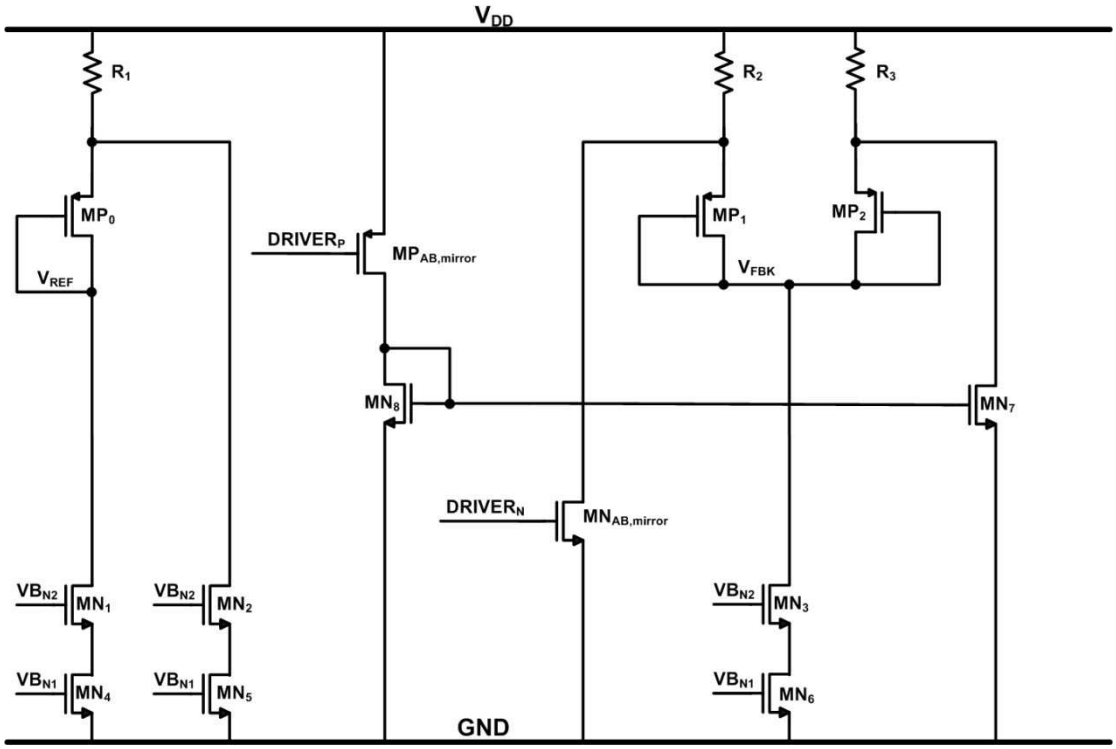

Fig. 4.15: Second stage class AB output bias current monitor circuit.

The PMOS diodes achieve several benefits. Suppose for instance that there is a heavy load pulling V_{out} down, say 1mA. The monitor current would be so large as to back-bias the MP_1 diode, thus protecting the rest of the circuit against inversion and malfunction. The bias current formerly in the diode would shift to the other diode, thus slightly decreasing the V_{FBK} voltage and reducing the bias level of the unloaded driver to perhaps 70% of its nominal value, 1.2uA.

It is necessary to keep the unloaded driver biased as close to its nominal bias, since that reduces cross-over distortion and enhances its fast response (no turn on delays).

Considering process variations and device mismatches, the three PMOS diodes MP_0, MP_1, and MP_2 nicely track each other as well as the V_{gs} of the split cascode, and to lesser extent, the V_{gs} of MP_{AB}.

This configuration allows the folded cascode, MP_2 and MP_3, PMOS current mirror to operate with sufficient V_{ds} to stay in the active region. In addition, the V_{gs} of the PMOS transistor MP_{AB} must be large enough to keep MP_{0P} in the active region.

Transistor level simulations show that the second stage folded cascode with class AB output has an overall DC gain of 133dB with a cut-off frequency of 210KHz. The total current consumption is 3.5µA.

4.6 PTAT BIAS CURRENT GENERATOR

As know, a PTAT current reference is achieved by applying a voltage proportional to the thermal voltage $V_T = kT/q$ across a given resistance. The circuit shown in Figure 4.16 accomplishes this function.

Bipolar transistors Q_A and Q_B, whose emitter area has a ratio 1 to n, are diode connected. Their current to voltage characteristics are exponential, as expressed by the equations:

$$V_{BEA} = V_T \cdot \ln\left(\frac{I_A}{AI_{SS}}\right) \tag{4.8}$$

$$V_{BEB} = V_T \cdot \ln\left(\frac{I_B}{nAI_{SS}}\right) \tag{4.9}$$

Where A is the junction area of the emitter of Q_A. Assume that the operational amplifier is ideal, with zero input voltage offset and infinite voltage gain.

If the MP_6 and MP_7 PMOS transistor are matched, then the two branches carry the same current. Therefore, the voltage across the resistance R becomes:

$$RI_A = V_{BEA} - V_{BEB} = V_T \ln\left(\frac{I_A}{AI_{SS}} \cdot \frac{nAI_{SS}}{I_A}\right) \tag{4.10}$$

which results in:

$$I_A = \frac{V_T}{R} \cdot \ln(n) = T \cdot \left[\frac{k}{qR} \cdot \ln(n)\right] = T \cdot k_{PTAT} \tag{4.11}$$

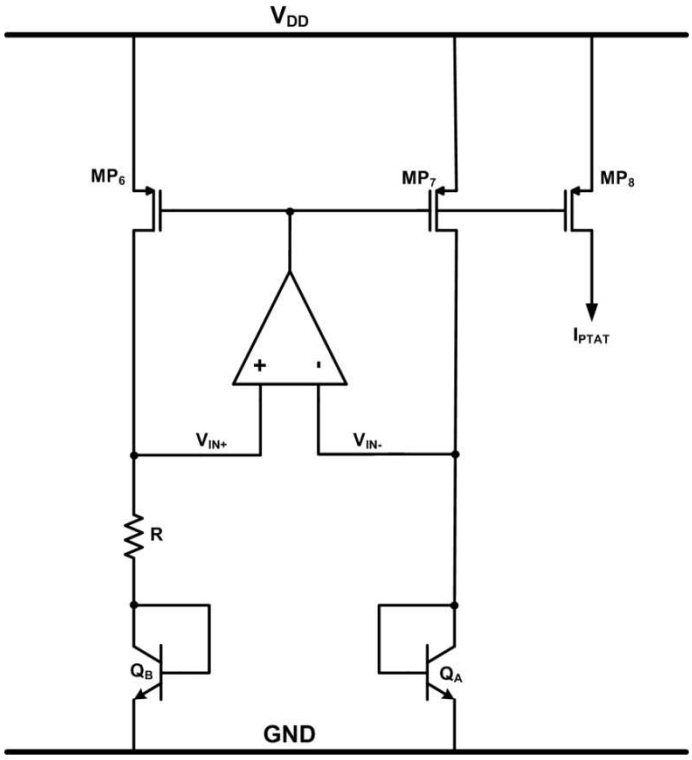

Fig. 4.16: PTAT current generator circuit.

Therefore, the I_A branch current is proportional to the absolute temperature by a positive temperature coefficient k_{PTAT}.

Since, at room temperature, V_T is approximately 26mV, with n=4 and R=360KΩ a 100nA current can be obtained.

Notice that this circuit admits work in the state with zero current. Then, a start-up circuit it is required.

4.6.1 PTAT BIAS CURRENT GENERATOR OPERATIONAL AMPLIFIER DESIGN

The PTAT bias current generator circuit needs an operational amplifier whose input common-mode voltage is the V_{BE} of the used bipolar transistors (for the used process around 0.6V). Moreover, since the operational amplifier output node drives two

PMOS current sources, its output quiescent voltage should be below the difference (V_{DD}-$V_{th,p}$).

Considering the minimum input supply voltage, 1.8V, since the $V_{th,p}$ of a PMOS transistor with 0.5µm gate length is around 0.9V, the output voltage results as low as 0.8–0.9V. In addition, the gain of the operational amplifier must be around 60 dB without any bandwidth constraints.

The above design conditions lead to the following considerations:

- The input common-mode voltage makes it difficult to accommodate an NMOS input differential stage. Possibly, a level shift of the input voltages toward the supply rail is necessary.
- To ensure active region operation even with process variations, the low output voltage prevents the use of cascode configurations. Therefore, a two-stage architecture should be used.
- The required biasing conditions can lead to a significant input referred offset, which can become the key limit to the correct operation of the PTAT circuit.

In order to overcome all the previous discussed issues, the operational amplifier has been realized as shown in Figure 4.17. The used start-up circuit is also depicted.

It can be noted that the circuit does not use an input differential stage but two grounded bipolar transistors Q_D and Q_E.

The combination of the diode connected BJT in the PTAT bias current generator and the BJT of the op-amp input stage constitutes a current mirror. Therefore, the currents in the input stage of the op-amp do not need control, being a replica of the current in the PTAT structure.

The bias voltage , generated within the startup circuit, is also obtained from the PTAT circuit by mirroring the I_A current of Figure 4.17.

The signal current generated by the input differential pair Q_D and Q_E is folded and collected by two diode connected MOS transistors MN_1 and MN_3.

Since the input gain stage is fully symmetrical, its systematic offset is practically zero.

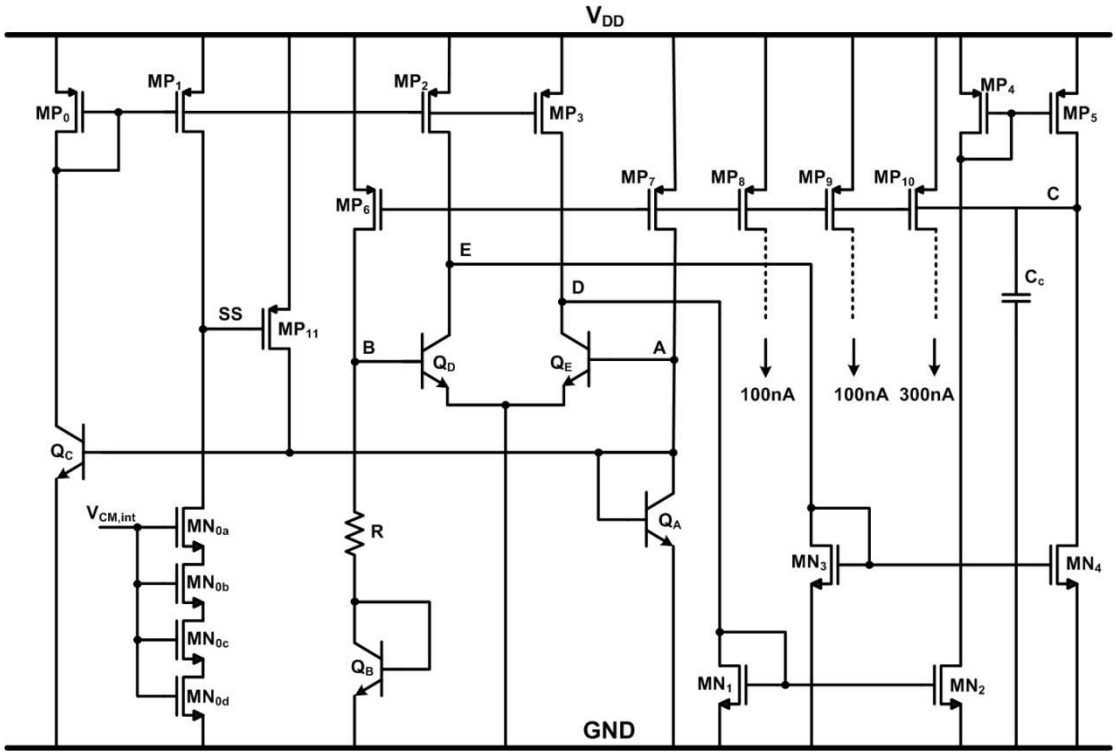

Fig. 4.17: PTAT current generator circuit with op-amp and start-up circuit.

The second stage is a push–pull circuit. Since the quiescent value of the output voltage is one V_{GS} below V_{DD}, the V_{DS} voltages of PMOS transistors MP_4 and MP_5 match, and the systematic offset of the second stage is nearly zero as well.

Moreover, for the same reason, excellent power supply rejection ratio and common-mode rejection ratio are achieved.

The bias current in the operational amplifier is 200nA and matches the 100nA current flowing in the PTAT. Mirroring the PTAT current I_A with PMOS transistors MP_8, MP_9, MP_{10}, the PTAT bias current generator provide a 100nA current for the second stage with class AB output, 100nA for the ring oscillator and 300nA for the band pass first stage.

Circuit total power consumption at room temperature is 900nA.

The PTAT current I_A as a function of the temperature, from -40°C to 125°C, has been obtained by a transistor level simulations. From this simulations the current I_A at -40°C, 27°C and 125°C is respectively 78nA, 100nA and 133nA.

Then, at 125°C, the chopper CDS amplifier current consumption is around 33% higher than the 25°C one.

The 1pF compensation capacitance C_C ensures the stability of the whole PTAT circuit under any operating conditions.

The startup circuit ensures that additional current is continuously provided to the BJT diodes Q_A and Q_B until the PTAT circuit reaches the proper steady state operating point.

In particular, if the current in the diode Q_A is zero, the current in Q_C is zero as well, and the PMOS current sources MP_0 and MP_1 are off. The gate voltage SS of PMOS device MP_{11} is pulled down to ground, thus injecting a significant current into the diode Q_A.

At the end of the startup phase, when the circuit reaches the normal operating conditions, the current in PMOS device MP_1 and the value of resistance provided by the NMOS transistors M_{N0a}, M_{N0b}, M_{N0c}, M_{N0d}, bring the gate of the PMOS device MP_{11} close to V_{DD}, thus turning off the startup circuit.

Observe that a weak startup current in the operational amplifier may be a source of a significant systematic offset, which could lead the PTAT to a meta-stable operating point.

It is worth to point out that, this is not the case in the circuit used, because the operational amplifier is controlled with the same reference current used in the PTAT. Consequently, an exact tracking of the currents in the input differential stage and in the current sources is achieved, nulling the systematic offset even during the startup phase.

4.7 500KHZ RING OSCILLATOR

The chopping clock signal is internally provided by the ring oscillator circuit shown in Figure 4.18.

The ring oscillator circuit is made of a cascade of three inverter stages (MN7-MP6, MN8-MP7 and MN9-MP8) that achieves an overall delay time of 1µs, thus obtaining

a 1MHz digital waveform. The proper time delay is provided by the combined effect of the 1µA inverter bias currents and PMOS and NMOS inverter transistors gate length (L = 8µm).

Process variations and mismatches cause a 20% variation on the nominal oscillating frequency. However, this frequency variation has only a slight impact on the amplifier input offset voltage. Moreover, the 100nA circuit bias current is fed by the PTAT current generator, thus tracking temperature variations.

The 1MHz digital waveform is enforced by two inverter stages. Then, a toggle flip-flop provides the internal 500kHz clock signal.

START is an external digital signal that can disable the 1MHz clock. The ring oscillator supply voltage is 1.8V.

A proper digital circuit (supplied at 1.8V) provides two non-overlapped phases to correctly drive the chopper and CDS circuit transmission gate switches. Transmission gate switches phases go from 0 to V_{DD} thanks to level shifters cells.

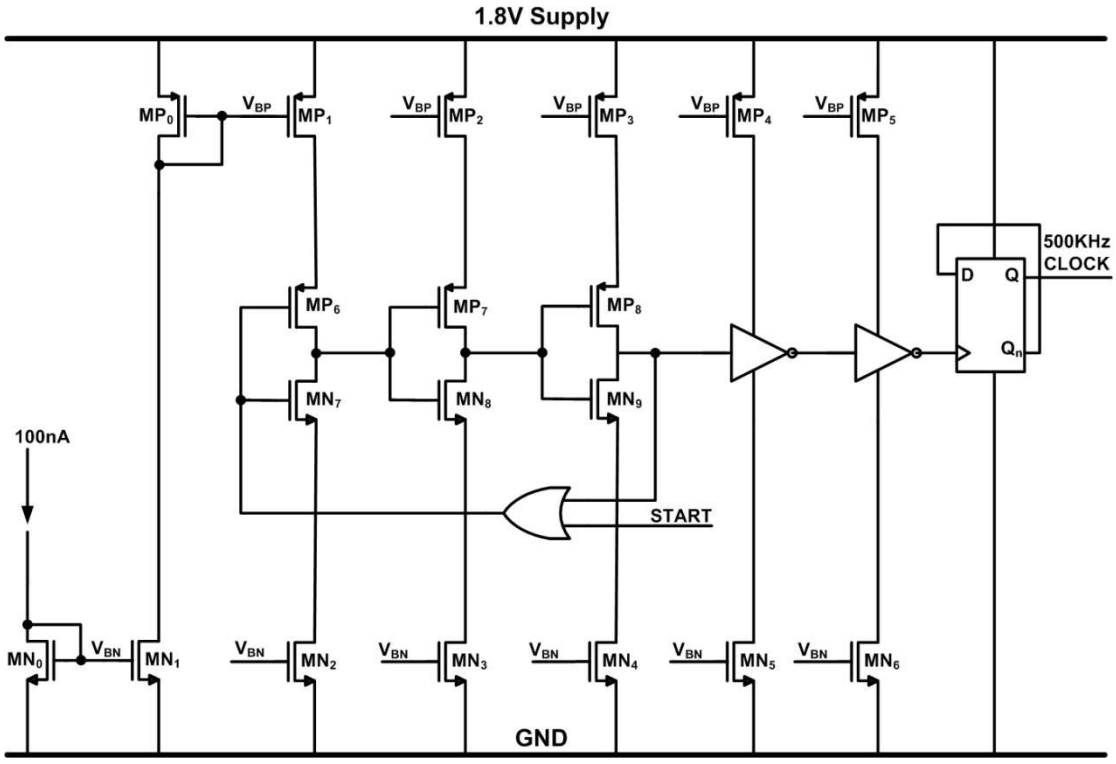

Fig. 4.18: 500kHz ring-oscillator circuit.

4.8 CHOPPER CDS AMPLIFIER PROTOTYPE

The Figure 4.19 shows the chip microphotograph. The chopper CDS amplifier has been fabricated in a mixed 0.18-0.5µm 5V dual poly 6 metal layers CMOS process with natural transistors. The total area (including pads) is 1.21mm x 0.95mm.
The avoidable chip population is made of 44 ICs.

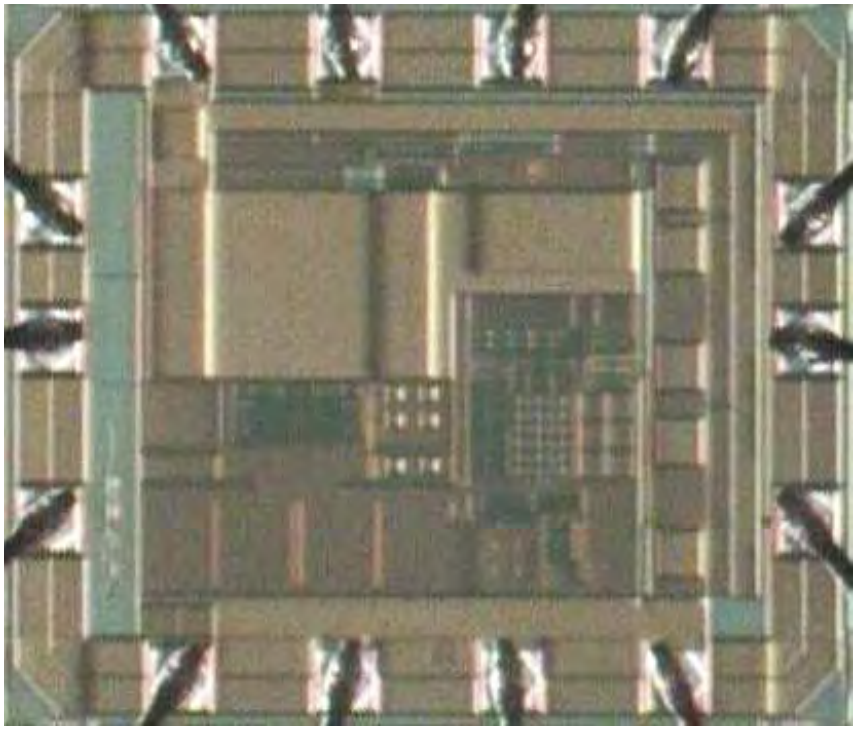

Fig 4.19: Chopper CDS amplifier prototype microphotograph.

4.9 CHOPPER CDS AMPLIFIER TEST PCB

In order to make the chopper CDS amplifier IC prototype measurements, two dual-layer PCBs have been designed. One has been used to make the AC measurements, in particular to obtain the amplifier frequency response and the noise spectrum.
The other PCB verifies the amplifier DC performance, such as input offset and offset temperature variations. This DC board uses a servo-loop to keep the output of the

class AB output stage at one half of the supply voltage independently on the input common mode voltage to verify the amplifier input rail-to rail operation.

4.10 CHOPPER CDS AMPLIFIER MEASUREMENTS RESULTS

This Section discussed the obtained measurements results.
The measured Bode diagram from 50Hz to 1MHz is shown in Figure 4.20. It can be noted that at 20dB of gain the phase margin is 71° at 26kHz, as expected from simulations, with an extrapolated GBW of 260kHz. The designed overall open loop DC gain is 168dB with the dominant pole at 1.1mHz.

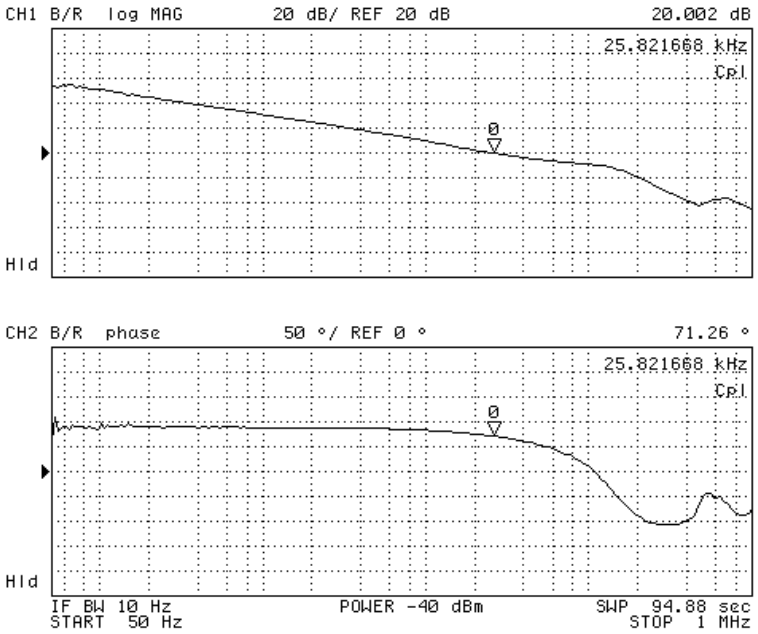

Fig 4.20: Measured Bode diagram from 50Hz to 1MHz.

It is worth to point out that the amplifier has been designed stable for gains higher than 20dB. This design choice is to ensure low input noise density and low power. Since the circuit is not for unity gain use, the supply power is optimized by increasing first stage bias current instead of adding an extra feed-forward path to obtain stability in a buffer configuration.

The measured input noise density spectrum of Figure 4.21 shows a low frequency level of 37nV/√Hz without flicker noise. The result almost matches the periodic steady-state simulation results and periodic noise analyses made with Spectre.
The spectrum is flat up to the limit of the test equipment (10Hz) and does not show any tone at the chopping frequency (500 kHz) or its multiples. Noise measurements are made with the proposed amplifier configured for a closed-loop gain equal to 1027.

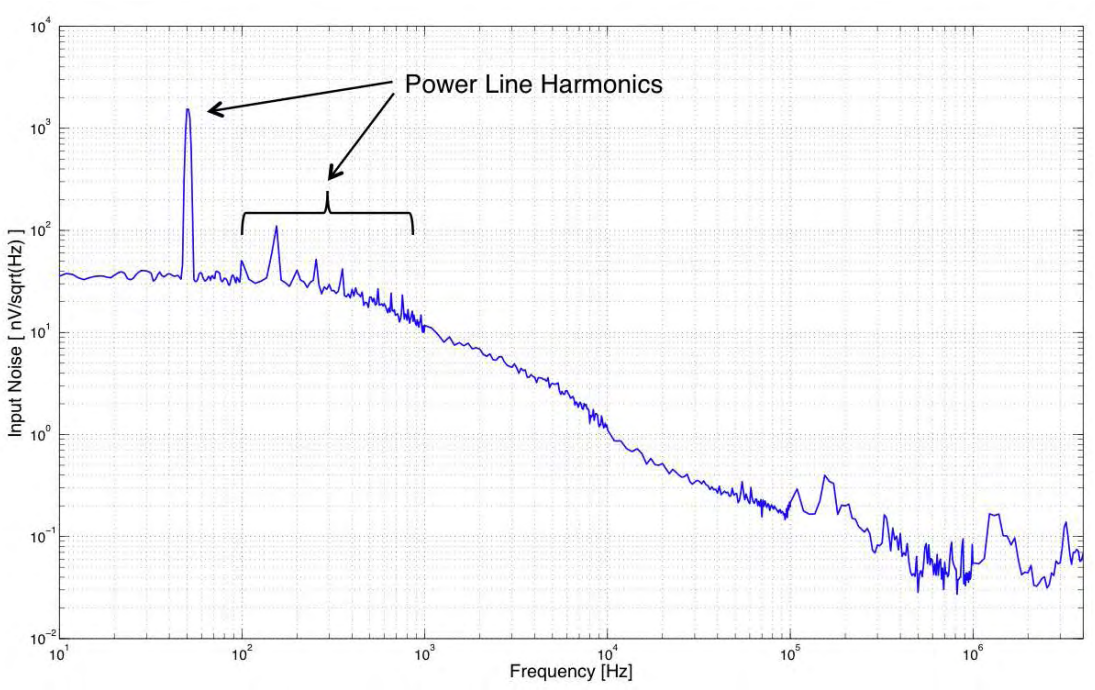

Fig 4.21: Measured input noise spectrum with 1027 closed-loop gain.

The measured offset voltage over the 44 available samples gives the population distribution of Figure 4.22, showing a variance of about 2µV. The measured variance is about 1µV higher than the simulated one likely because of higher mismatches and input chopper residual offset than expected.
The chopper CDS amplifier operates from -40 to 125°C. The temperature dependence is better than 0.03µV/°C.

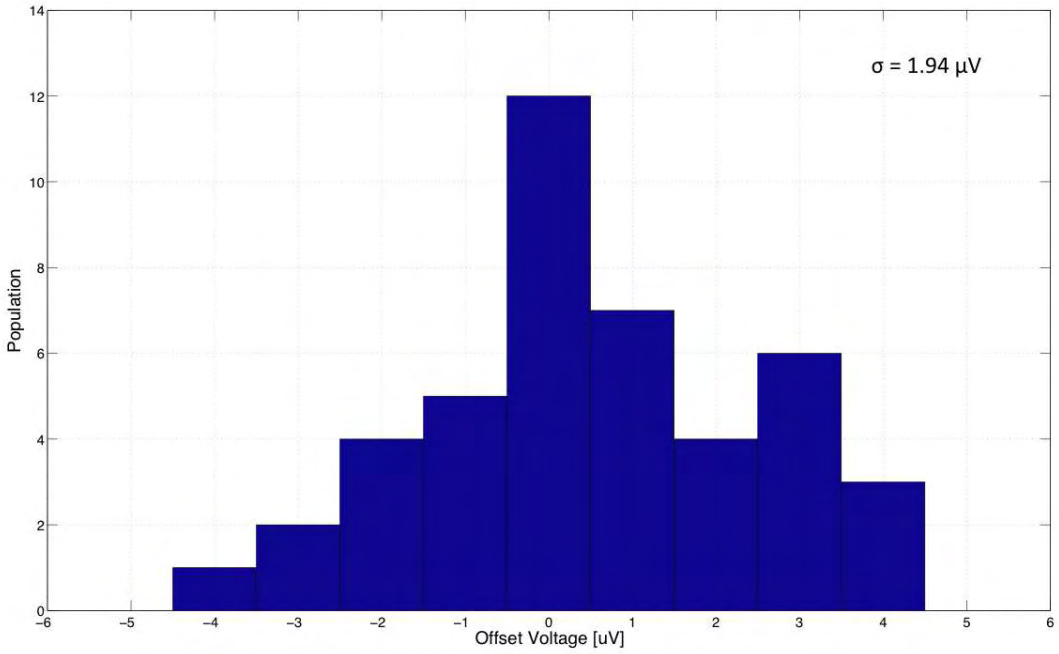

Fig 4.22: Measured offset voltage distribution over 44 samples.

The low-frequency noise measurement of 0.8µVpp over 0.1 to 10Hz, illustrated in Figure 4.23, demonstrates that the input noise density of 37 nV/√Hz is substantially flat to DC.

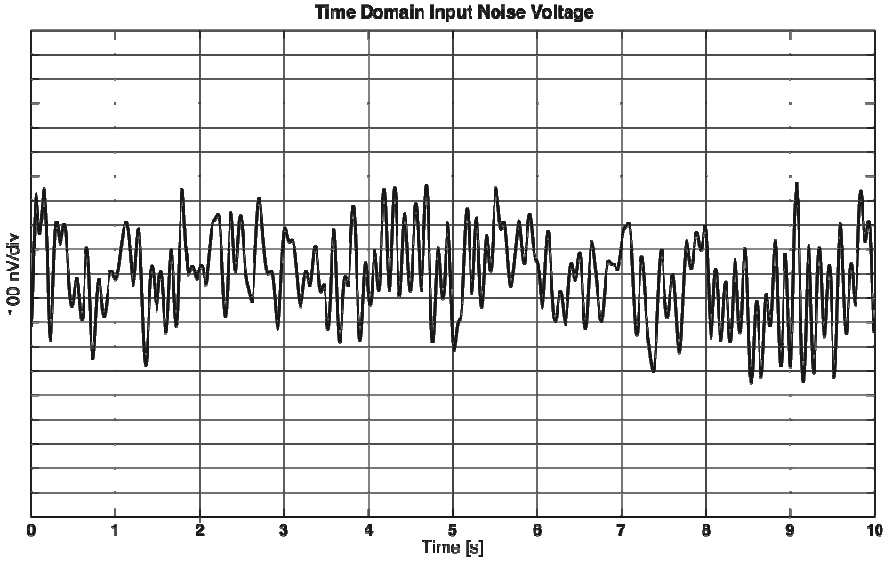

Fig 4.23: 0.1 to 10Hz noise measurement.

4.11 CHOPPER CDS AMPLIFIER PERFORMANCE SUMMARY

Table 4.1 summarizes the measured chopper CDS amplifier performance. The amplifier works with an input supply voltage range from 1.8V to 5V and from -40 to 125°C. The quiescent current of the analog part is 12.8µA while the internal oscillator and the digital logic consume 1.6µA. The total current consumption is 14.4µA.

The measured input noise density at DC of 37nV/√Hz and the low current consumption give a noise efficiency factor $v_{n,i} \cdot \sqrt{[2I_{tot}/(\pi U_T \cdot 4kT)]}$ [4] of 5.5. The obtained figure is 33% and 37% less than the state of the art ones obtained by [5] and [6], respectively.

The offset voltage variance is about 2µV with a temperature dependence is better than 0.03µV/°C. Rail-to-rail input is achieved. A class AB output stage ensures 1nF load capacitance driving capability. The total area (including pads) is 1.21mm x 0.95mm.

Supply Voltage [V]	1.8→5
Chopping Frequency [kHz]	500
Input Noise Density at DC [nV/√Hz]	37
Offset Voltage Standard Deviation [µV]	1.94
Analog Supply Current [µA]	12.8
Digital Supply Current [µA]	1.6
Common Mode Input Range [V]	0→5
GBW (extrapolated) [kHz]	260
Offset Temperature Dependence [µ V/°C]	<0.03
Process	Mixed 0.18-0.5µm CMOS
Chip Area (Including Pads)	1.21mm x 0.95mm
Noise Efficiency Factor	5.5

Tab.4.1: Circuit performance summary.

As already pointed out, the chopper CDS amplifier has been designed stable for closed-loop gains higher than 20dB. This design choice is to ensure low input referred noise density and low power.

In fact, since the circuit is not for unity gain use, power is optimized by increasing first stage current instead of adding an extra path to obtain stability in a buffer configuration.

REFERENCES

[1] I. E. Opris, and G. T. A. Kovacs, “A Rail-to-Rail Ping-Pong Op-Amp”, *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1320-1324, Sept. 1996.

[2] A. T. K. Tang, “A 3μV-Offset Operational Amplifier with 20nV/√Hz Input Noise PSD at DC Employing Both Chopping and Autozeroing”, *IEEE International Solid-State Circuits Conference Dig. Tech. Papers*, pp. 386-387, Feb. 2002.

[3] F. Geusa, A. Agnes, and F. Maloberti, "Use of Chopper-Notch Modulator in Chopper Amplifiers for Replica Images Cancellation", *Proc. of IEEE International Conference on Electronics, Circuits and Systems*, pp. 566-569, Sept. 2008.

[4] M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, “A Micropower Low-Noise Monolithic Instrumentation Amplifier for Medical Purposes”, *IEEE Journal of Solid-State Circuits*, vol. SC-22, pp. 1163-1168, Dec. 1987.

[5] R. Burt, and J. Zhang, “A Micropower Chopper-Stabilized Operational Amplifier Using a SC Notch Filter With Synchronous Integration Inside the Continuous-Time Signal Path”, *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2729-2736, Dec. 2006.

[6] [1] R. Wu, K. A. A. Makinwa, and J. H. Huijsing, “A Chopper Current-Feedback Instrumentation Amplifier with a 1mHz 1/f Noise Corner and an AC-Coupled Ripple-Reduction Loop”, *IEEE International Solid-State Circuits Conference Dig. Tech. Papers*, pp. 322-323, Feb. 2009.

BIBLIOGRAPHY

[1] F. Maloberti, “Analog Design for CMOS VLSI Systems”, Kluwer Academic Publisher, 2001.

[4] National Semiconductor Corporation web-site, http://www.national.com.

[5] Texas Instruments Corporation web-site, http:// www.ti.com.

CHAPTER 5

CONCLUSIONS

The PhD research activity has led to the design of innovative solutions for portable systems. Three IC prototypes have been developed achieving significant improvements to the state of the art.

With regard to the single-inductor 4-output buck converter activity, Table 5.1 compares the measured system performance [3] with the reported single-inductor multiple-outputs works in [1], [2] and [4].

It is worth to point out that this research has led to the first 4-output buck converter architecture. It can also be noted that the 1.8A total and 0.8A single-channel output current capabilities are quite high and allow more degrees of freedom in the output current sharing respect to the other works.

Moreover, the 3MHz switching frequency is the highest one reported. Such high value allows the use of a 1µH off-chip inductor and achieves faster transient responses. The 85% peak efficiency is the highest one reported.

	[1] JSSCC07	[2] JSSCC08	**This Work [3] ISSCC08**	[4] ISSCC09
Outputs	5	2	**4**	5
Converter Topology	Boost	Boost	**Buck**	Buck-Boost
Supply Voltage [V]	2.5→4.5	2.7→4.5	**2.3→5**	2.5→4.5
Output Voltages [V]	(4-outputs) 5→ 12 (1-outputs) 12→ -5	-4.8→4	**0→(V_{supply}-0.5)**	(3-outputs) 2→ 9.5 (1-outputs) 6→ 10 (1-outputs) 8→ 12
Inductor [µH]	10	10	**1**	4.7+1
Output Capacitor [µF]	4.7	10	**10**	10
Switching Frequency [MHz]	0.7	1	**3**	1
Total Output Current [A]	0→0.11	0→0.1	**0.1→1.8**	0→0.145
Single Output Currents [A]	0→0.04	0→0.1	**0→0.8**	0→0.05
Peak Power Efficiency [%]	80.8	80	**85**	83

Tab.5.1: Single-inductor 4-output research activity achievements comparison.

With regard to the high switching frequency buck converter activity, Table 5.2 compares the measured system performance [7] with the reported high frequency architectures in [5] and [6].

Even if [5] and [6] circuits work with a higher switching frequency, their performance in terms of power efficiency, output voltage ripple and line and load regulations are not so good. On the other hand, the designed IC has shown a very high peak power efficiency, 93%, an output voltage ripple of only 10mV and maximum line and load regulation of respectively 10mV/V and 20mV/V. Furthermore, the 1A output current capability is the highest one ever reported.

Therefore, in terms of regulation performance, this research has led to significant improvements respect the state of the art.

	[5] ISSCC07	[6] ESSCIRC08	**This Work [7] ESSCIRC09**
Supply Voltage [V]	3.3	2.6	**2.2→2.8**
Output Voltage [V]	2.3	1.2	**0.5→ (Vdd-0.2)**
Output Current [A]	0.07	0.15	**0→1**
Switching Frequency [MHz]	200	300	**60/120**
Inductor [nH]	22	9.8	**36 (18@ 120MHz)**
Max Output Voltage Ripple [mV**]**	23	110	**10**
Peak Power Efficiency [%]	62	52	**93**
Line regulation [mV/V]	-	83	**10**
Load Regulation [mV/V]	-	51	**20**

Tab.5.2: High switching frequency research activity achievements comparison.

With regard to the micro-power low-noise chopper amplifier activity, Table 5.3 compares the measured system performance [9] with Texas Instrument Corporation IC OPA333 that is actually the state of the art.

Thanks to the design choice of compensate the amplifier for 20dB gain, the power consumption has been optimized and a 37% of reduction of the noise efficiency factor, defined in Section 4.11, respect to [8] has been achieved.

Thus, also this activity has led to significantly improvements respect the state of the art especially for the input supply current/input noise trade-off issues.

	[8] JSSCC 06	**This Work [9]** **ISSCC 10**
Supply Voltage [V]	1.8→5.5	**1.8→5**
Chopping Frequency [kHz]	125	**500**
Input Noise Density at DC [nV/√Hz]	55	**37**
Offset Voltage Standard Deviation [µV]	3	**1.94**
Supply Current [µA]	17	**14.4**
Common Mode Input Range [V]	0→5	**0→5**
GBW [kHz]	350	**260**
Offset Temperature Dependence [µV/°C]	<0.02	**<0.03**
Noise Efficiency Factor	8.7	**5.5**

Tab.5.3: Micro-power low-noise chopper amplifier research activity achievements comparison.

Concluding, each research activity has provided innovative solutions and significant improvements with respect to the state of the art.

REFERENCES

[1] H.-P. Le, C.-S. Chae, K.-C. Lee, S.-W. Wang, G.-H. Cho, G.-H. Cho, "A Single-Inductor Switching DC–DC Converter With Five Outputs and Ordered Power-Distributive Control", *IEEE J. of Solid-State Circuits*, vol 42, pp. 2706 – 2714, Dec. 2007.

[2] Y.-J. Woo, H.-P. Le, G.-H. Cho, G.-H. Cho, S.-I. Kim, "Load-Independent Control of Switching DC-DC Converters With Freewheeling Current Feedback", *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 2798 - 2808, Dec. 2008.

[3] M. Belloni, E. Bonizzoni, E. Kiseliovas, P. Malcovati, F. Maloberti, T. Peltola, T. Teppo, "A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current", *Proc. Of 2009 IEEE International Solid-State Circuits Conference*, pp.444-626, 3-7 Feb. 2008.

[4] K.-S. Seol, Y.-J. Woo, G.-H. Cho, G.-H. Cho, J.-W. Lee, S.-I. Kim, "Multiple-output step-up/down switching DC-DC converter with vestigial current control", *Proc. Of 2009 IEEE International Solid-State Circuits Conference*, pp. 442-443, 8-12 Feb 2009.

[5] K. Onizuka, K. Inagaki, H. Kawaguchi, M. Takamiya, T. Sakurai, "Stacked-Chip Implementation of On-Chip Buck Converter for Distributed Power Supply System in SiPs2", *IEEE J. of Solid-State Circuits*, vol 42, pp. 2404 – 2410, Nov. 2007.

[6] M. Wens, K. Cornelissens, M. Steyaert, "A Fully-Integrated 0.18µm CMOS DC-DC step-Up Converter, Using a Bondwire Spiral Inductor", *Proc. Of 2007 IEEE European Solid-State Circuits Conference*, pp. 268-271, Sept 2007.

[7] M. Belloni, E. Bonizzoni, F. Maloberti: "High Efficiency DC-DC Buck Converter with 60/120-MHz Switching Frequency and 1-A Output Current", to appear on *Proc. Of 2009 IEEE European Solid-State Circuits Conference*.

[8] R. Burt, J. Zhang, "A Micropower Chopper-Stabilized Operational Amplifier Using a SC Notch Filter With Synchronous Integration Inside the Continuous-

Time Signal Path", ", *IEEE J. of Solid-State Circuits*, vol 41, pp. 2729 – 2736, Dec. 2006.

[9] M. Belloni, E. Bonizzoni, F. Maloberti: " A Micro-Power Chopper-Correlated Double Sampling Amplifier with 2μV Standard Deviation Offset and 37nV/√Hz Input Noise Density"; to appear on *Proc. Of 2010 IEEE International Solid-State Circuits Conference*.