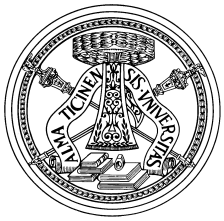

Università degli Studi di Pavia

Facoltà di Ingegneria

Dipartimento di Elettrica

Dottorato di Ricerca in Microelettronica
XXIV ciclo

LOW VOLTAGE LOW POWER SIGMA-DELTA MODULATORS IN 65-nm CMOS TECHNOLOGY

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Tesi di Dottorato
di Oscar Belotti

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I would like to dedicate this thesis to my loving parents ...

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I would like to express my gratitude to Prof. Franco Maloberti, for the professional and personal guidance and the constant support at all stages of this research. Also, I would like to thank all the group of "Car Receiver Radio" (Antonella, Gianluigi, Claudio, Simone and Matteo) in STMicroelectronics Castelletto (Milan) for all the support in the chips realization.

I take this opportunity also to thank all the people in the laboratory and not for their support.

Oscar.

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Chapter 1

Introduction

1.1 This thesis work

The rapid growth of the market of portable, battery powered electronic systems for telecommunications creates new challenges for low cost, low power, high performance data converters. Moreover, the modern trend of moving processing to the digital domain in very large scale integration (VLSI) systems is pushing toward deep submicron technology, that on the contrary is not attractive for analog function. Therefore, the reduction of the voltage headroom introduces severe constraint for achieving an acceptable dynamic range due to the increased sensitive to noise and makes also problematic the driving of CMOS switches. At the same time, low threshold voltage enhances the leakage dissipation and the saturation of the transconductance g_m with the reduction of the output resistance affects the intrinsic gain.

The goal of this research is to explore efficient design techniques for the design of $\Sigma\Delta$ ADC, that based on the increased support of digital assistance, allow to relax the performance of the analog circuitry. In particular, the aim is to investigate the effectiveness of techniques that allow to reduce the swing of the output of the operational amplifiers in order to relax slew-rate and GBW requirements with benefits in terms of reduced power consumption and better linearity.

The activity of my research work involves the complete design and realization of two chips both realized with a 65 nm CMOS technology, courtesy offered by STMicroelectronics.

The first chip realization proposed a new second-order low-pass multi-bit hybrid continuous-time (CT) $\Sigma\Delta$ modulator implemented with a general purpose (GP) 65-nm CMOS technology. The circuit ensures jitter immunity granted by the use of multi-rate switched-capacitor (SC) DACs that further reduce the requirement of the operational amplifier in term of gain, bandwidth and slew-rate. A combination of analog and digital feedforward paths allows to reduces integrators output swing. The modulator provides a measured 10.8 bits of resolution over a signal bandwidth of 1.1 MHz and a spurious free dynamic range (SFDR) of 78 dB. The chip draws 1.1 mW from a 1-V supply, leading to a Figure of Merit (FoM) equal to 280 fJ/conversion-level

at the state of the art compared with other 65 nm chip operating in the same frequency range ([1], [2] ,[3], [4]).

The development of this innovative CT architecture suggests the study of new design methodology that allows to obtains a CT modulator with same noise shaping of a Discrete-Time (DT) prototype without any constraint about the shape of the feedback DAC. The method operates entirely in the time domain and accounts for any non-idealities of real implementations. Moreover, the procedure can be effectively implemented directly with circuit simulators during the design step, allowing the exact design with transistor level blocks. Extensive behavioral simulations confirm the effectiveness of the proposed method.

The second chip realization proposed a new third-order low-pass multi-bit discrete-time (DT) $\Sigma\Delta$ modulator implemented with a high performance (HP) 65 nm CMOS technology. The proposed architecture obtains a third order noise shaping behavior with only two operational ampliers by using the noise shaping enhancement technique. Moreover, the implementation of a fully digital feedforward ensures a noise-like swing at the output of the operational amplifier, allowing the use of the telescopic scheme with gain boost. The modulator provides a simulated 14 bits of resolution over a signal bandwidth of 2.2 MHz and a signal to noise and distortion ratio (SNDR) of 83.27 dB. The chip draws 2.3 mW from a 1.2-V supply, leading to a Figure of Merit (FoM) equal to 43.8 fJ/conversion-level, the best of the state of the art in this frequency range.

In addition, the work includes the analysis of two new low-power $\Sigma\Delta$ modulator architectures. The first one present the design of a third order modulator realized with only two operational ampliers, that achieves complex conjugate zeros allowing to increase the signal bandwidth and to obtain a SNR improvement of about 8 dB. The second architecture exhibits a new smart technique that virtually double the oversampling ratio of a conventional second order $\Sigma\Delta$ modulator. Accounting for a limited cost, the resolution increases by about 2-bit and power just increases by few percents. Therefore, the FoM diminishes by a factor close to 3.5.

1.2 Structure of the Thesis

Fig. 1.1 summarizes the general structure of this thesis work, which is organized as follows.

Chapter 2 introduces the analysis of the predominant limiting physical effects that affect the analog performance of the transistors. Furthermore, the chapter analyzes in detail the impact of the technology scaling on the design of analog circuit and the realization of the layout.

Chapter 3 presents a brief overview about the two basic concepts of oversampling and noise shaping, that are the fundamental principles of the $\Sigma\Delta$ architecture. The structure of discrete-time (DT) $\Sigma\Delta$ will be analyzed in detail from theoretical and implementation point of views. Moreover, the chapter introduces to the theoretical aspects behind the implementation of the continuous-time CT $\Sigma\Delta$ counterpart, highlighting the benefits and the differences with

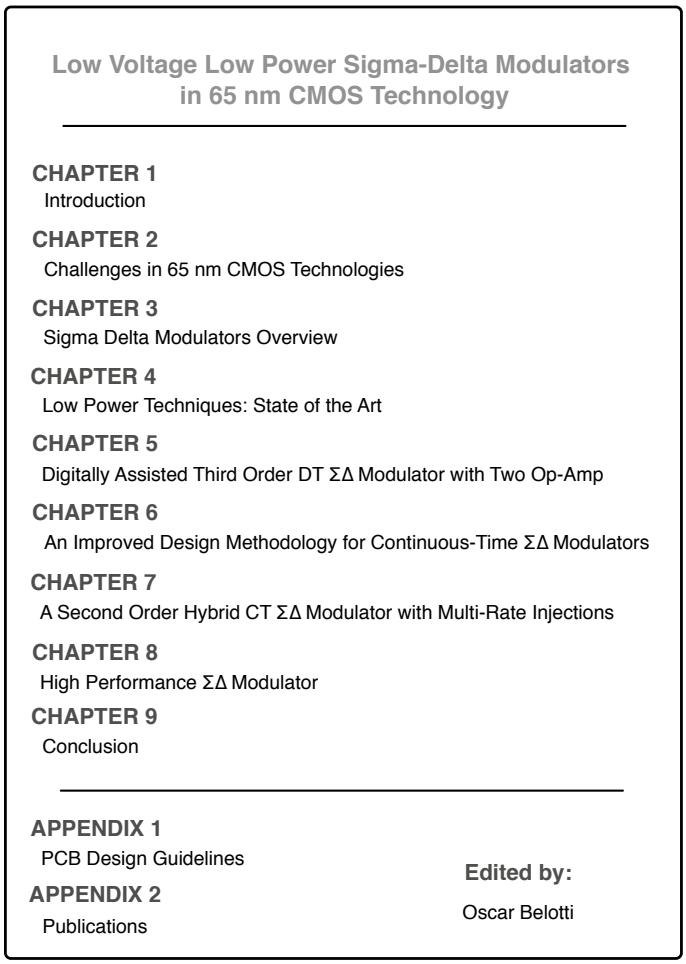

Figure 1.1: Thesis structure.

the DT scheme. The chapter ends with the description of the most common metrics used to characterize the performance of a $\Sigma\Delta$ modulator.

Chapter 4 introduces to the design trade-off for low power $\Sigma\Delta$ architectures. The chapter, also presents the state of the art of recent published low power DT $\Sigma\Delta$ architectures. In particular, these techniques include the reduction of the number of operational amplifiers, the DAC resolution reduction, the use of parallelism and operational amplifier swing reduction.

In **Chapter 5** a novel high power efficiency $\Sigma\Delta$ modulator is presented. The chapter explains in detail the synthesis and the design of a low power third order discrete time (DT) $\Sigma\Delta$ modulator targeted for WCDMA specification in a 65 nm CMOS technology. The modulator achieves about 14 bit over 2.2 MHz input signal bandwidth. The proposed architecture obtains a third order noise shaping behavior with only two operational amplifiers by using the noise

shaping enhancement technique. Moreover, the structure integrates a new swing reduction technique that reduces the swing of the two integrators to a very small level comparable with the dynamics of a quantization noise. The last feature allows implementing a single telescopic stage operational amplifiers increasing the final power efficiency. The integration of different power reduction techniques limits the power consumption to 2.3 mW, thus yielding an optimum FoM of only 43.8 fJ/conversion-level.

Chapter 6 introduces a new general design methodology for continuous-time CT $\Sigma\Delta$ modulator without any limitation about the shape, number and different typology of the feedback DACs used in the same modulator. The approach allows the system level compensation of non-idealities associated with the implementation of the real analog blocks. The key point of the proposed methodology is its simplicity because the procedure allows hand calculation also for complex modulator. Moreover it is suitable for designer, because it is circuits oriented, so that could be simply implemented with circuit simulator directly at transistor level, during the design step. An example design, demonstrate the effectiveness of the proposed approach.

Chapter 7 illustrates the design of a novel second order low-pass multi-bit multi-rate hybrid continuous-time (CT) $\Sigma\Delta$ modulator implemented with a 65-nm CMOS technology targeted for low-rate data transmission wireless network, ad defined by standard IEEE 802.15.4. The circuit ensures jitter immunity granted by the use of multi-rate switched-capacitor (SC) DACs that further reduce the requirement of the operational amplifier in term of gain, bandwidth and slew-rate. A combination of analog and digital feedforward paths allows to reduces integrators output swing. The modulator provides a measured 10.8 bits of resolution over a signal bandwidth of 1.1 MHz and a spurious free dynamic range (SFDR) of 78 dB. The chip draws 1.1 mW from a 1-V supply, leading to a Figure of Merit (FoM) equal to 280 fJ/conversion-level at the state of the art compared with other 65 nm chip operating in the same frequency range.

Chapter 8 introduces two new design concepts for high-performance very low power DT $\Sigma\Delta$ modulators for wide-band applications. The first proposed $\Sigma\Delta$ architecture exhibits a third order noise shaping behavior with only two operational amplifiers. The modulator achieves complex conjugate zeros that allow to increase the signal bandwidth and to obtain a SNR improvement of about 8 dB. Moreover, the design uses a fully digital technique to reduce both amplifiers output swings in order to relax the requirement of the analog blocks.

The second architecture exhibits a new smart technique that virtually doubles the oversampling ratio of a conventional second order $\Sigma\Delta$ modulator. This approach, described with more detail in this chapter, is based on the prediction scheme that allows to build the value of next sample achieving an interpolation by a factor two. Accounting for a limited circuitry cost, the resolution increases by about 2-bit and power just increases by few percents. Therefore, the FoM diminishes by a factor close to 3.5. Circuit level schemes indicate that the architecture does not requires higher op-amp bandwidth. The method can be used with multi-bit quantizer without requiring additional efforts for the DEM. Behavioral level simulations, considering the slew-rate, bandwidth and DC gain limits of the amplifier, demonstrate the effectiveness of the

proposed solutions.

Chapter 9 explains the results obtained in this work and introduces to possible future developments.

Additional material is included in two appendices. **Appendix A** introduces some guidelines for the design of multilayers boards used for testing high performance data converters. **Appendix B** presents the list of publications published in this PhD course.

Chapter 2

Challenges in 65 nm CMOS Technology

2.1 Introduction

The silicon technologies evolution toward nanometer CMOS process (90 nm, 65 nm and below) has been driven by the consumer market request of low-cost highly integrated portable systems with very demanding performance. The rapidly downscaling of transistor size over the last 40 years, as predicted by the well known "Moore's Law", allows nowadays the integrations of complex systems on a single die (SoC).

These integrated systems are mixed-signal design, embedding high performance analog circuit (RF frontends, filters and high speed data converter) together with high density digital circuits (multiple processors, DSP, large memory blocks) on the same chip. The increased number of function per unit area reduces the chip's size and consequently the final cost of the system. Moreover small feature sizes of the transistors increase their intrinsic speed with less power consumption, allowing systems processing at very high frequencies. However, scaled technologies need low voltage in order to increase the reliability of the transistors against electromigration process, leakage currents and breakdown events. For instance, 65 nm technology uses a supply voltage of 1.2 V.

Nanometer CMOS technologies pose new hard challenges for circuits design due to new predominant physical effects (leakage currents, short-channel effects, reduced supply voltage, increased sensitivity to process variations, ecc ...) and enhancement of already existing limits in other previous technologies (reduced voltage headroom).

Not only, managing rising design complexity in crazy market with very stringent time-to market needs new design methodologies and powerful software tools (not only for circuit design but also for layout step) that help the designer to increase his efficiency and consequently the final yield.

In other word, the main question is whether the limits related to the intrinsic physical characteristics of the 65 nm transistors become a real bottleneck for circuit design avoiding to keep driving up circuits performances.

This chapter present a brief overview on physical limits that affect 65 nm technology, with some guidelines about new proposed circuit design technique.

2.2 Physical limits of the 65 nm technology

The VLSI technology ensures high levels of integration thanks to the transistor's unique characteristic of negligible standby power, allowing the fabrication of chips with many hundred of millions of transistor. However, as the CMOS scaling moves forward to deeper nanometer process, the resulting electrical barriers in the devices begin to lose their insulating properties due to thermal injection and quantum mechanical tunneling. This causes a rapid rise of the power with practical limit on the reachable integration level as well as on the operating switching speed. Limits are the short-channel effect, the tunneling leakage through gate oxide, high field effects, increased process variability, dopant number fluctuations, lithography, interconnect delays and electrostatic scale length [5],[6].

- **Subthreshold leakage current**

  Threshold voltage (V_{TH}) is the gate voltage at which the Fermi level at the oxide-semiconductor interface is symmetrical with respect to the bulk position. Under this value, the current decreases exponentially, with a rate that on logarithmic scale is inversely proportional to the thermal energy KT. This term is due to some thermally distributed electrons at the source that have enough energy to overcome the potential barrier controlled by the gate voltage and reach the drain. The current conducted by a transistor whit V_{GS}=0 is:

$$I_{subthreshold} = I_o e^{-\frac{V_{TH}}{\frac{nKT}{q}}} \tag{2.1}$$

  where I_o is a measure of diffusion of the minority carriers in the channel and it's inversely proportional to the L. The subthreshold current increases exponentially with the decreasing of V_{TH}. Another phenomena, called Drain Induced Barrier Lowering (DIBL) contributes to change V_{TH}. This phenomena occurs when the depletion region around the source and the drain interact with each other, causing a reduction in the potential barrier at the source level.

  The leakage current is becoming a limiting factor in terms of power consumption that can not be ignored in order to continue reducing the size of transistors and increasing the level of integration that is now required. Anyway, the problem can be mitigate by using a mix of transistors with different threshold voltage, without affecting the speed of the circuit.

- **Gate leakage current**

  The shrinking of the CMOS process imposes that the gate oxide thickness must be reduced in proportion to the channel length in order to keep short-channel effect under control. This is required in order to guarantee a good control over the charge of the channel. Nowadays, the oxide film is so thin that is subjected to quantum-machanical tunneling effect, leading to a gate leakage that increases exponentially as the oxide thickness is scaled down. The current leakage is described by:

$$I_{gate-leakage} = KW\left(\frac{V_{GB}}{t_{ox}}\right)e^{-\frac{\alpha t_{ox}}{V_{GB}}} \tag{2.2}$$

  where K and α are fit factors. The leakage current is dominated by electrons that from tunneling, pass through the gate-oxide, from the silicon inversion layer to the positively biased gate. This current affects the overall power consumption and the functionality at the circuit level. Another issue with the thin gate oxide is the loss of inversion charge due to inversion layer quantization and polysilicon-gate depletion effects.

- **Short-Channel Effect**

  The short channel effect is related to the reduction of the threshold voltage (V_{TH}) in short channel device due to electrostatic charge sharing between the gate and the source/drain regions. The reduction of this effect requires that both the oxide thickness and the gate-controlled depletion region in substrate must be resized in proportion to the length L. This causes an increased channel doping concentration, that leads to higher electric fields at the silicon surface. The reduction worsen if the voltage of the drain increases (Drain-Induced Barrier Lowering effect DIBL). The effect can be mitigated with some additional steps (HALO) that permit to have a modified doping profile. In narrow channel case (the channel width is the same order of magnitude of the thickness of the depletion region under the gate) an increase in W, gives rise to an increase in V_{TH} due to the additional inversion layer charge close to the edge of the channel. In particular its effect is irrelevant for large value of W, but assumes importance for narrow W influencing the value of V_{TH}, that rises.

  The velocity of the carriers in the short channel rises up due to the effect of increased level of the electric field across the channel. At low level electric field (ξ), below of a critical value ξ_c, the velocity increases proportionally to the electrical filed as defined by the mobility μ. For high electric fields the velocity saturates (v_{sat}) to approximately 10^5 m/s, as depicted in Fig. 2.1.

$$\begin{aligned} v &= \frac{\mu_n \xi}{1+\frac{\xi}{\xi_c}} \quad for \quad \xi \leqslant \xi_c \\ v &= v_{sat} \quad for \quad \xi \geqslant \xi_c \end{aligned} \tag{2.3}$$

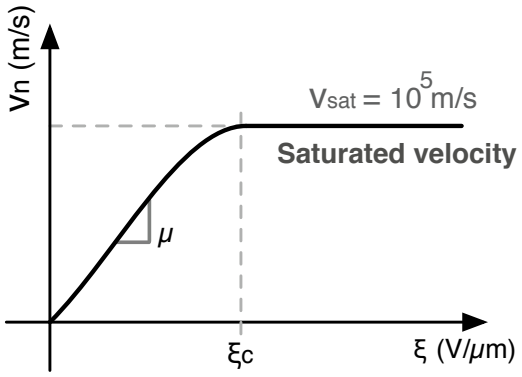

Figure 2.1: Effect of velocity saturation.

The main consequence of this phenomena is that short-channel devices show a larger saturation region due to the velocity saturation of the carriers. The current of the drain changes linearly with the overdrive voltage (V_{GS}-V_{TH}), and the transcondctance saturates to g_{msat}:

$$\begin{aligned} I_D &= v_{sat} C_{ox} W (V_{GS} - V_{TH} - V_{DASAT}) \\ g_{msat} &\cong v_{sat} C_{ox} W \end{aligned} \tag{2.4}$$

- **Discrete doping effects**

  The discreteness of the dopant atoms is another key limit against the technology scaling. Standard ion implantation an annealing processes, are able to control with quite accuracy the average concentration of doping, but do not control exactly where the dopant ends effectively. This randomness at atomic scale, causes spatial fluctuations in the local doping concentration that gives rise to a high variation of threshold voltages. Remind that the fluctuations of dopants can be described with Poisson statistics resulting in a standard deviation equal to the square root of the number of dopants. The decreasing of the channel dimension, involves the reduction of the number of dopants that realize a given doping concentration. This increase the uncertainty on threshold voltages for low number of dopants.

- **Lithography**

  Extensions methodologies beyond today's lithography technologies are strictly necessary in order to continue the development of CMOS into nanoscale area. In the past optical photolithography has overcame predicted resolution limits many times thank to a combination of improved lenses with higher numerical aperture and the adoption of shorter

wavelength illumination. Anyway with the advent of modern technology below the 45 nm, this optical technology is not able to define all the required geometry due to interference problem. Thus, X-ray lithography was introduced as good candidate to overcome this limits, but poses some hard challenges, for example in mask fabrication and precise control of the mechanical stress in the absorber-covered material of the membrane on the mask.

Recently, another technique, called electron beam lithography was introduced. It is based on electron beam which properly directed by a deflection system, traces the desired geometry with a focused spot on a e-sensitive resist substrate. Many correction schemes are implemented to compensate pattern distortion due to electron scattering (known as proximity effects). Anyway, high accuracy pattern placement can be achieved with a good interferometry and suitable control of the noise in the electron beam deflection systems. This technique ensures to reach definitions of 32 nm.

- **Device Reliability**

  The shrinking of the transistor dimensions down to nanometer scale imposes the reduction of the supply voltage to keep the electric field constant in order to ensure lifetime reliability. The main recommendations concern to the maximum voltage applicable to the terminals to avoid too much stress to the devices to prevent the onset of destructive phenomena such as dielectric and junction breakdown, threshold instability and hot carrier injection.

2.3 Analog circuit design challenges in 65 nm

The greatest impact of the technology scaling is the reduction of the supply voltage (V_{DD}) in order to ensure device reliability avoiding destructive phenomena, like junction breakdown. In 65 nm process, the maximum supply voltage is 1.2 V. Moreover, the decreasing feature sizes of the modern CMOS process gives rise to the scaling of the threshold voltage (V_{TH}), but not in proportion to the reduction of the supply voltage, as shown in Fig. 2.2. This figure shows also that for deeper technology (from 45 nm), the V_{TH} inverts the decreasing trend of the last steps in order to reduce leakage current and short channel effects.

Lower supply voltage is beneficial for digital circuits, since the dominant source of power dissipation, is the dynamic power consumption, which is linked to supply voltage with a quadratic relationship:

$$P_{dymanic} = \alpha C f V_{DD}^2 \tag{2.5}$$

where α is the activity factor, C is the total node capacitance, f is the processing frequency and V_{DD} is the supply voltage. Therefore, the power consumption in digital circuits is reduced in scaled technology. Otherwise, the reduction of the overdrive voltage (V_{OV}=V_{DD}-V_{TH}) makes difficult the design of analog blocks. The limit is aggravated by the fact that the threshold volt-

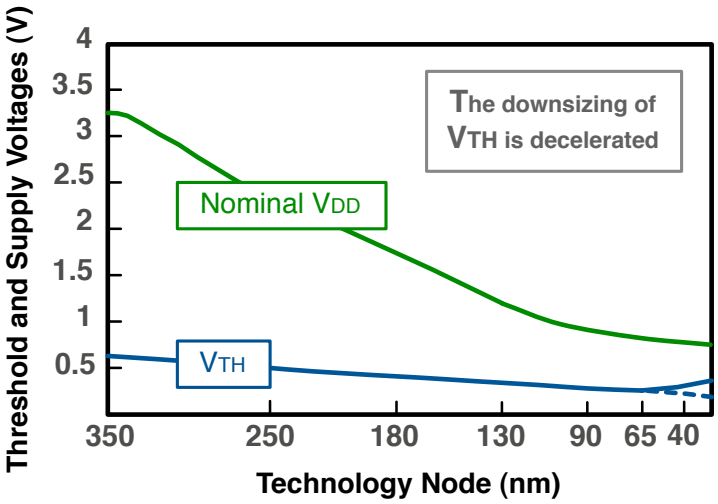

Figure 2.2: Threshold and supply voltages versus technology node.

age is very sensitive to many effects, such as technology variations (process, supply voltage and temperature variation), analog design choices (device mismatch, short channel effect, reduced headroom voltage) and layout design (WPE and STI effects). The mismatch of a transistor pairs is described with a normal distribution with mean μ and standard deviation σ:

$$\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}} \tag{2.6}$$

where $A_{V_{TH}}$ is a technology constant, which is proportional to the MOS oxide thickness. As a consequence, scaled technology ensures a better matching with the same device's area (WL), but in order to mitigate short channel effects, larger size devices are required.

The transconductance of the transistor in strong inversion and subthreshold region is given by the following expressions respectively:

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} = \frac{2I_D}{V_{OV}} \tag{2.7}$$

$$g_m = \frac{I_D}{\frac{nKT}{q}} \tag{2.8}$$

Technology scaling introduce a g_m increase due to reduction of the overdrive voltage. On the contrary, the output conductance (g_{ds}) is increased strongly with the CMOS shrinking due to short-channel effects. This result in lower intrinsic transistor DC gain (g_m/g_{ds}), proving a big problem for the design of operational amplifiers. In analog design the performance in terms of Dynamic range (DR) and power consumption, are often limited by the thermal noise, which is

inversely proportional to the bias current ($\propto 1/I_D$). The power consumption of a operational amplifier, which drive a capacitor is:

$$P_C = V_{DD} I_D \tag{2.9}$$

The parameter that define the speed of the operational amplifier is the unitary frequency, which is given by:

$$f_u = \frac{g_m}{2\pi C} \tag{2.10}$$

The dynamic range, defined as the ratio between the maximum signal amplitude of the analog output and the noise level, is given by:

$$DR = \frac{V^2_{Out-rms}}{\frac{KT}{C}} \propto \frac{V^2_{DD} C}{KT} \tag{2.11}$$

where KT/C represents the thermal noise. Thus combining equations (2.7), (2.9), (2.10) and (2.11) it is possible to obtain a generic relationship that expresses the power dissipation as a function of the dynamic range, unitary frequency and supply voltage:

$$P \propto DR \cdot KT \cdot f_u \cdot \left(\frac{V_{OV}}{V_{DD}}\right) \tag{2.12}$$

As a consequence, the reduction of the power supply voltage, as required by technology scaling, involves the increase in load capacitor to guarantee the same dynamic range. This gives rise an increase in analog power consumption, so a higher voltage is beneficial in order to reduce the final power consumption. Insufficient voltage headroom makes stacking of transistors no longer efficient, so in the last year some works [7], propose new architectures for high voltage (2.5 V) operational amplifier with high gain and high bandwidth. Anyway, the rules of reliability (electrostatic discharge, bias temperature instability, punchthrought effect, breakdown and hot carrier injection) make the design a real challenge, in order to increase the lifetime of the devices.

Otherwise, at lower power supply voltages, a multistage amplifier [8] is needed to achieve high DC gain. These amplifiers require large compensation capacitor for stability, consume more current, require multi feedback loop for controlling common-mode voltage of the intermediate node and are noisier than a single stage telescopic amplifier.

However, as indicated in equation (2.8), in order to increase the gain it is possible to force the MOS to operate in sub-threshold region ($V_{GS} < V_{TH}$). In this region the MOS presents some useful advantages, such as, minimum overdrive, small gate capacitance and large gain (at least 30% more compared to the gain in strong inversion region). On the contrary, the devise has low speed and the terms $A_{V_{TH}}$ is three times higher than the value in saturation, leading to a mismatch and consequently an input offset, which requires a compensation scheme to be removed.

At the end, the reasons that justifies the continuous effort in the technological evolution

toward deeper technology is the final speed (or, equivalently its intrinsic bandwidth) of the MOS device. The unity gain frequency of the transistor is given by the following relation derived by the quadratic law for drain current.

$$f_T \propto \frac{g_m}{2\pi C_{GS}} \propto \frac{V_{GS} - V_{TH}}{L^2} \tag{2.13}$$

The relationship shows that the transistor unity gain increase with the CMOS technology scaling. Anyway, this fast technology evolution poses hard challenges in front of engineers also for the basic analog block, such as switch and operational amplifiers design.

2.3.1 Layout Design in 65 nm

The devise size shrinking in scaled technologies introduces many new issue in the layout design due to the onset of two new effects, called Shallow Trench Isolation (STI) stress effect and Well Proximity Effect (WPE) [9]. Both effects have a profound impact on final MOS performance and should not be underestimated in order to avoid failures.

- **Well proximity Effect**

  The use of high energy implants is required to form the deep well profiles needed for latch-up protection and lateral punch-through. During the implant process, atoms can scatter laterally from the edge of the photoresist mask and should be absorbed in the silicon surface near the well edge, as shown in Fig. 2.3 (a). The scattering create a non-uniformity well doping near the mask edge, that changes with the later distance from the well edge. The consequence of this is the variation of the threshold voltage and other electrical characteristics as a function of this distance. The impact of the WPE on the threshold also depends on the S/D (source/drain) orientation of the MOS, as shown in Fig. 2.3 (b). MOS with the source oriented towards the well-edge, creates a higher threshold voltage, that limit current flow for low V_{GS}, but also generates a higher g_m which enhances current flow for larger V_{GS}. On the contrary, MOS with the drain oriented towards the well-edge will conduct more current at low V_{GS} and less current at high V_{GS}. Fig. 2.4 shows a layout solution that can mitigate WPE effect: it is necessary to ensure a sufficient distance between the well edge and the S/D of the transistor (in a 65 nm technology it is recommended at least 3 μm).

- **Shallow Trench Isolation**

  For deeper CMOS technologies, the most prevalent isolation scheme between two different active areas, is shallow trench isolation. It replaces the LOCOS process, where the "bird's beak" (Fig. 2.5) was an evident limitation to its size reduction. The STI process step consists in a oxide deposition into a trench, getting to an abrupt separation between the active region and isolation. Anyway this steep transition applies a mechanical stress to

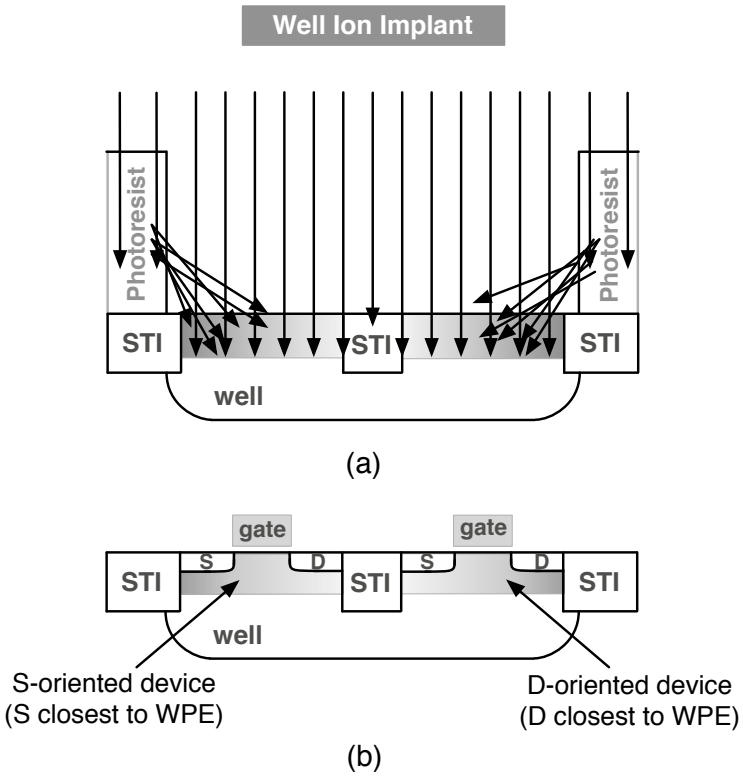

Figure 2.3: A depiction of the WPE limit.

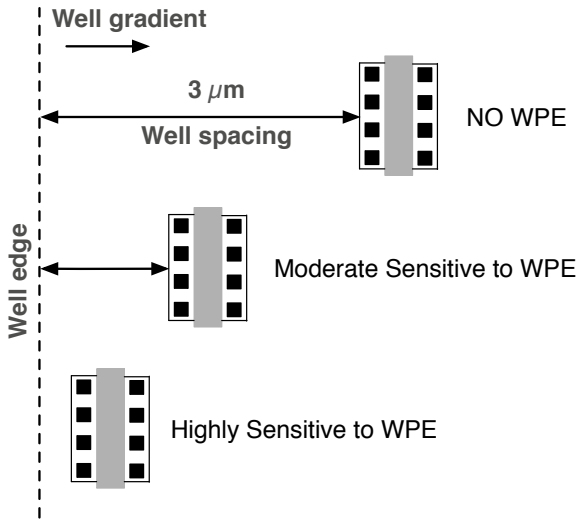

Figure 2.4: Evaluation of the WPE effect versus the distance from the well edge.

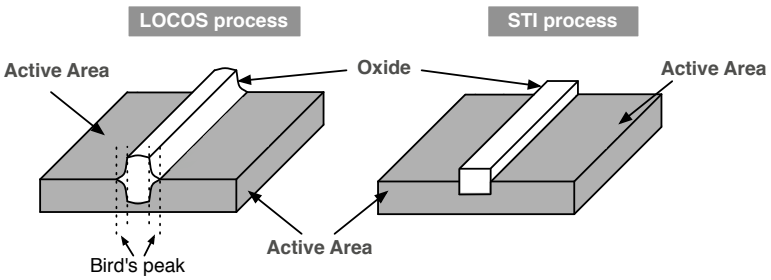

Figure 2.5: Isolation using LOCOS and STI process.

the active area edge (Fig. 2.6) that increases the value of the threshold voltage and the current in saturation. These effects are relevant and must be included in the model of the transistor. The stress state is non-uniform and depends on the overall size of the active area, linking the MOS electrical characteristic to the layout step.

Fig. 2.7 shows the STI effect for different layout design. In the first case (a) the mechanical pressure is applied on both side, increasing the threshold voltage to the value V_{THa}. In case (b), the value V_{THb} is lower compared to V_{THa} because STI stress acts only on the external sides, so the internal edges are immune. This suggest to use external dummy in order to protect internal device against STI pressure, as depicted in case (c). The final result is that V_{THc} is lower than V_{THb} and V_{THa}. However, dummy devise could be expensive in terms of area and added parasitics capacitance.

The nature of the problems introduces difficulties in following the conventional design flow, because their effects could be evaluated only during layout step. Anyway, it is important to predict their effects also during the schematic design at simulation level. This could be done using appropriate transistor model for both proximity effects, that assuring consistency between layout and schematic. Therefore, it is absolutely important for analog designer understands this kind of problems in order to avoid harmful circuit failure.

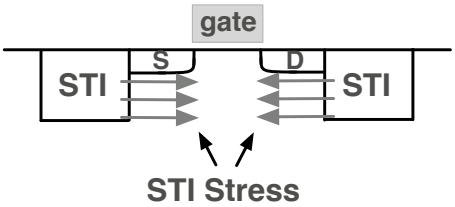

Figure 2.6: A depiction of the STI stress effect.

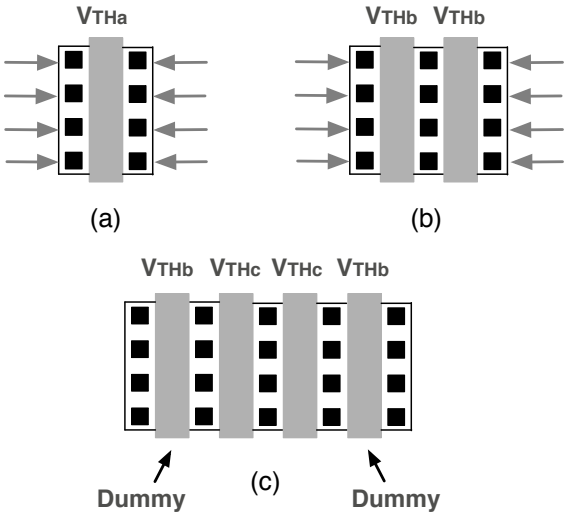

Figure 2.7: Influence of STI effect for different layout design.

Another key point in advanced process regards the delay associate to the interconnections. A first-order approximation of the interconnect delay is:

$$t_{wire} = \frac{rCL^2}{2} = \rho\kappa\left(\frac{L}{\lambda}\right)^2 \tag{2.14}$$

where r and C are the resistance and capacitance per unit length, ρ and κ are the same parameter per unit area, while λ is the wire pitch. From the equation it is clear that if the interconnection length and pitch shrink identically, the wire delay remain constant.

Deeper technologies are also prone to voltage drop effect, due to the intrinsic resistance associated with the grid used to distribute power and ground to the internal circuitry. This means that the circuits closest to the primary power or ground pins are well fed, which is not true for the circuits near the core. The problem is exacerbated with transient voltage effects, that occur when internal node switching from one value to another, causing spikes and consequently variation of the supply voltage. These effects can be minimized with an optimal power network design by increasing the width of power and ground traces.

2.4 Design of Integrated Mixed-signal Systems

The design of high integrated mixed-signal systems on chip, where sensitive analog circuits are integrated on the same die with large digital circuitry, introduces the necessity of new powerful tools able to perform the signal integrity analysis [10]. The need of the coexistence of analog and digital circuits, in recent years has stimulated the development of new and accurate

techniques that allow to model and analyze the unwanted signal interactions through crosstalk or coupling phenomena. All parasitic signals generated in the system, such as digital switching noise, inductive crosstalk from supply line or substrate coupling, can degrade the performance of the analog part. These models allow to simulate the propagation of digital switching noise injected into the substrate shared with analog circuit, in order to estimate the effect of the mutual influence between the circuits.

This justifies the growing need for analog CAD tools that permit to rise up the analog design productivity by including the manufacturing awareness into the design in order to increase the final testability and insensitivity to yield-limiting mechanism of the schematic. The managing of the design complexity of the mixed-signal systems requires the use of a top-down approach, that defines the conventional design flow in different steps: system specification, architectural design, circuit design, circuit layout and system layout assembly.

The procedure permits to increase the overall system performance, ontaining the optimization of each blocks, in terms of power consumption, architectural design and interface with other blocks. Thus, the adoption of massif CAD tools in the flow of the circuit design is justified by the goal of maximizing the final yield and by the necessity to speed up the entire design procedure to observe the time-to market.

Therefore, the future of the scaling will be dominated by application specific and product systems constraints on reliability, adaptivity, mobility, cost, power consumption, reusability and software support.

Chapter 3

Sigma Delta Modulation Overview

3.1 Introduction

The interest in the fields of Sigma-Delta ($\Sigma\Delta$) analogue-to-digital converters (ADCs) drastically increased over the last few years, as confirmed by extensive works appeared on conference and journal publications. The basic idea of $\Sigma\Delta$ modulator was patented around 50 years ago, but nowadays it is common in many high-resolution low-frequency applications, including high-fidelity audio, speech processing, sensor applications and voice-band data telecommunications. Its success is related with its intrinsic insensitivity to analog circuit imperfection and non-idealities of most building blocks.

Furthermore, the demand for increased performance and conversion bandwidth in the modern telecommunication portable systems requires innovative $\Sigma\Delta$ architecture with very low power consumption. Moreover, the shrinking toward nanometer technologies (below 90nm) provides the worst analog feature of the MOS devices, due to reduced voltage supply, low intrinsic gain and high sensitivity to process variation. The combination of these two factors makes the design of $\Sigma\Delta$ modulator a real hard challenge.

Thus, the intention of this chapter is to present a brief but clear explanation of the theoretical principles underlying the processing in Sigma-Delta modulators, with emphasis on practical issues and trade-off that must be taken into account in order to optimize their performance in terms of power consumption and silicon area. At the end, the chapter introduces a comparison between the characteristics that distinguish the class of Discrete-Time (DT) Sigma-Delta ($\Sigma\Delta$) modulators from the class of Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulators.

All information provided will be useful to understand the work developed in this thesis.

3.2 Fundamental of ΣΔ Modulators

The fundamental processes involved in the analog to digital conversion are the **sampling** and the **quantization**, as shown in Fig. 3.1 ([11], [12], [13], [14], [15]). Assuming that the information associated to a continuous time signal $X_{IN}(t)$ is limited in the signal bandwidth f_B ($|f_{X_{IN}}| \leqslant f_B$), the sampling time process is completely reversible. The input signal $X_{IN}(t)$is sampled with a S/H circuit, at a fixed sampling frequency f_S: in a frequency domain this translates in a periodicity of the original signal spectrum at multiples of f_S. As depicted in Fig. 3.2, it is clear that it is possible to reconstruct the original input signal only if the Nyquist theorem is satisfied:

$$f_S \geqslant 2f_B \tag{3.1}$$

where $2f_B$ is normally referred to as Nyquist frequency (f_N). The reconstruction could be done with a low pass filter, called antialiasing filter (AAF). This filter avoids that high frequency components of the input signal would be folded or aliased into the signal bandwidth f_B, causing a corruption in the signal information. The ADC that uses f_N as a sampling frequency, is called Nyquist rate converter.

The quantization process, realized by the quantizer, maps the continuous range of amplitude of its input signal, into a discrete set of level (2^N-1), where N are the number of bits of the quantizer). This step degrades the quality of the input signal and introduces an error, called *quantization error* (ϵ_q).

The levels of the quantizer are uniformly spaced by a quantity called quantization step:

$$\Delta = \frac{F_S}{2^N - 1} \tag{3.2}$$

where F_S is the full-scale output range.

The quantization is not a reversible process, leading a loss in the resolution of the digitized signal. This quantization error, ϵ, after the linearization of the quantizer (this is valid under assumptions which are normally met in practice [12]), can be modeled as an additive white

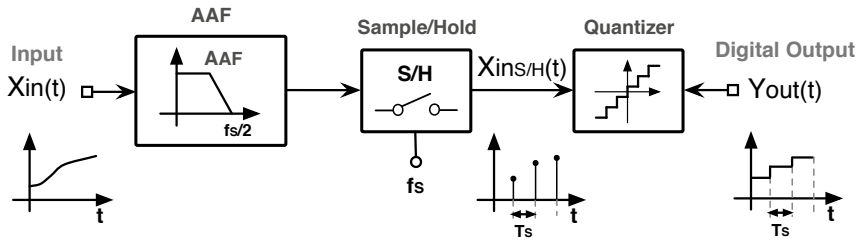

Figure 3.1: Block diagram of a Nyquist rate ADC.

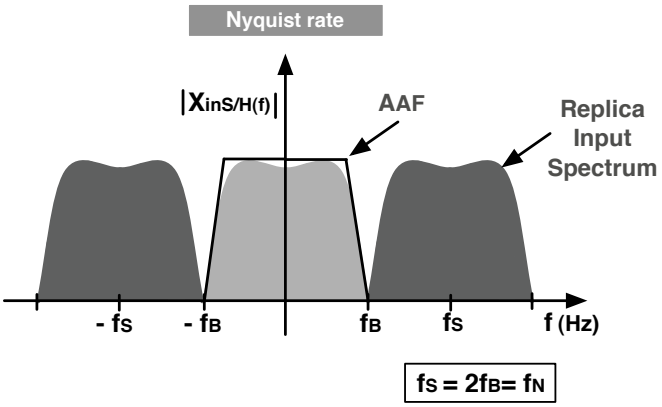

Figure 3.2: Antialiasing filter for Nyquist rate ADCs.

noise source, so that its quantization noise power ($\sigma^2(e)$) is uniformly distributed in the range $[-f_S/2, f_S/2]$. Since the signal at the input of the quantizer is sampled, all the quantization noise power $\sigma^2(e)$ is folded in the frequency range $[-f_S/2, f_S/2]$. Therefore, thank to the white noise approximation, the spectral density of the quantization noise is:

$$S_E(f) = \frac{\sigma^2(e)}{f_S} = \frac{1}{f_S}\left[\frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2}\sigma^2(e)de\right] = \frac{\Delta^2}{12f_S} \tag{3.3}$$

It is important to note that the quantization error power is inversely proportional to the quantizer resolution.

The process of $\Sigma\Delta$ modulator is based in the combination of two signal processing techniques, namely **oversampling** and **noise shaping**. Thanks to these two techniques, the $\Sigma\Delta$ modulator transfers most of the signal processing tasks to the digital domain, where the power consumption is decreased by exploiting the reduction of the supply voltage. The Nyquist theorem imposes that the sampling frequency must be at least twice the signal bandwidth. In practice this requires an abrupt low-pass AAF, which is very hard to be designed. Indeed, increasing the sampling frequency, the transition band of the filter increases, leading to relaxed requirements placed on the AFF (as depicted in Fig. 3.3), with benefit in terms of power consumption, less phase distortion and easier design. The oversampling ratio OSR is defined as:

$$OSR = \frac{f_S}{2f_B} = \frac{f_S}{f_N} \tag{3.4}$$

Moreover, the oversampling permits to reduce the in-band quantization noise power, spreading

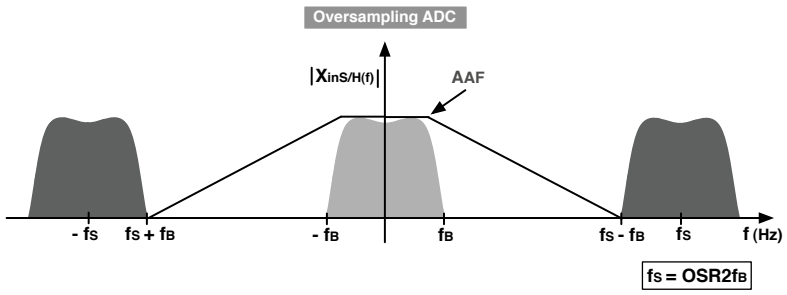

Figure 3.3: Antialiasing filter for Oversampling ADCs.

this power over a larger frequency band, as shown in Fig. 3.4.

$$P_e = \int_{-f_B}^{f_B} S_E(f)df = \frac{\Delta^2}{12OSR} \tag{3.5}$$

The effectiveness of the oversampling ADC can be further increased pushing the in-band quantization noise power toward high frequencies. This means change the white spectrum of the quantization noise into a shaped spectrum. For example, the quantization error, generated as the difference between the analog signal at the input of the quantizer and its quantized output, could de shaped by a filter, such as high-pass type or band-stop type.

The oversampling and noise-shaping concepts can be merged to build a new family of ADCs, called Sigma-Delta (ΣΔ) modulator. Fig. 3.5 (a) illustrates the complete block diagram of a Discrete-time ΣΔ modulator. The noise shaping behavior is obtained with the feedback loop, reported in Fig. 3.5 (b). The architecture of the loop consists of basic blocks including a discrete-time filter H(z), a quantizer and a DAC, that closes the feedback path. If the gain of

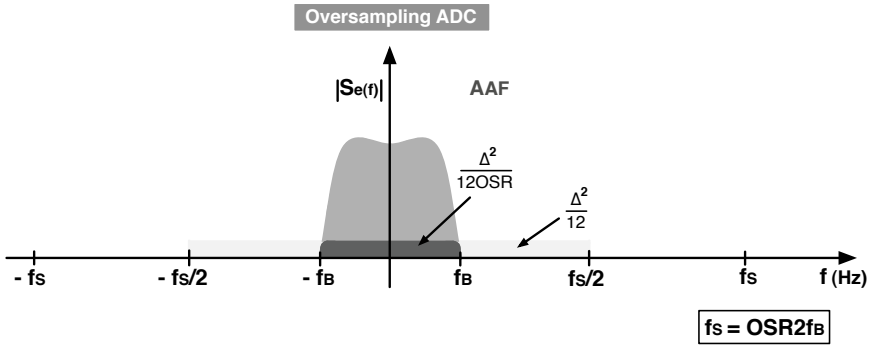

Figure 3.4: Benefit of the oversampling on the in-band noise power.

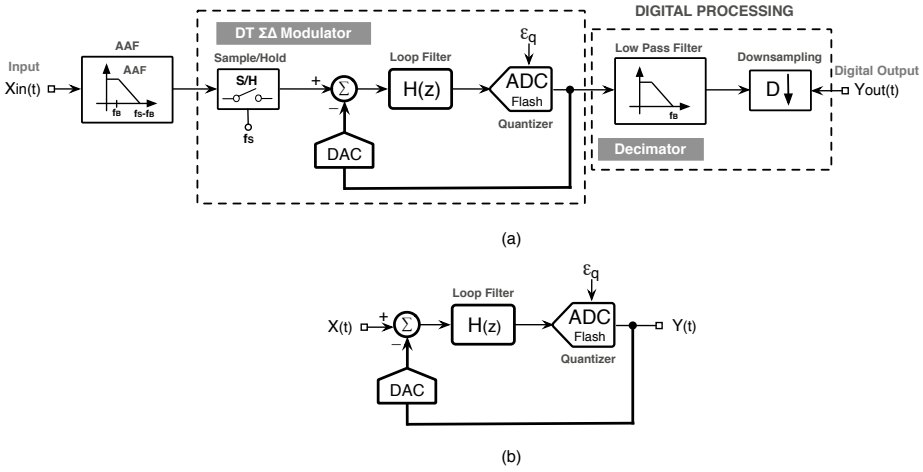

Figure 3.5: (a) Block diagram of a DT ΣΔ modulator (b) Conceptual block diagram of the ΣΔ modulator.

the filter H(z) is high enough in the signal bandwidth (f_B), the difference between the input X(t) e the output Y(t) properly filtered by H(z) and processed by the quantizer, gives rise to attenuation of the quantization error in the signal band, pushing the rest of the power at high frequency (Fig. 3.6).

The assumption of white additive noise model for ϵ_q, allows to model the modulator reported in Fig. 3.5 (b), as a two-input, X(t) and ϵ_q(t), one output Y(t) system. The resulting transfer function in the z domain is:

$$Y(z) = X(z)STF(z) + \epsilon_q(z)NTF(z) \tag{3.6}$$

where X(z) and ϵ_q(z) are the Z-transform of the input signal and quantization noise, respectively. STF(z) and NTF(z) play an important role in the definition of the final performance of the modulator; they stand for the signal transfer function and the noise transfer function, respectively given by:

$$STF(z) = \frac{H(z)}{1 + H(z)} \tag{3.7}$$

$$NTF(z) = \frac{1}{1 + H(z)} \tag{3.8}$$

Notice that, if the loop filter $|H(z)| \to \infty$ in the signal bandwidth, the input signal is transfered to the output ($|STF(z)| \to 1$), while the quantization error is ideally removed ($|NTF(z)| \to 0$). For a low pass ΣΔ modulator, STF should be low pass, while NTF high pass.

The basic architecture of ΣΔ modulator is the first order, as depicted in Fig. 3.7. The loop filter H(z) is realized with a delayed discrete time integrator (H(z)=z^{-1}/(1-z^{-1})). By inspection

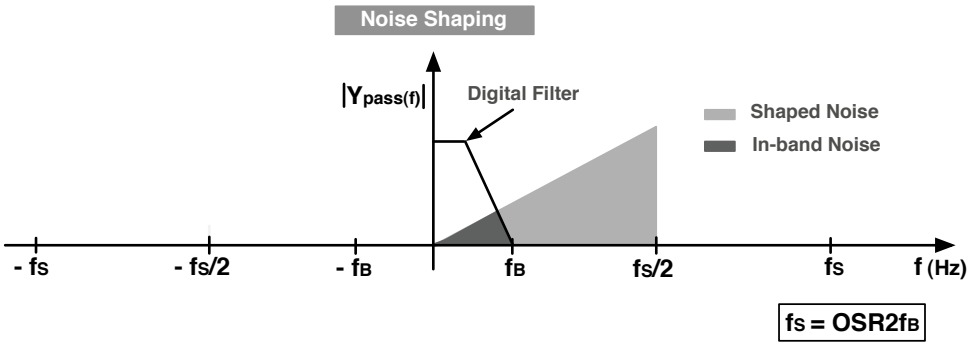

Figure 3.6: Processing of the signal in ΣΔ modulator.

of the scheme, the STF(z) is simply a delay z^{-1}, while NTF(z) is a first order differentiator filter (1-z^{-1}). The roll-off of the shaped noise spectrum is only -20 dB/decade. The scheme with a single bit, for both the quantizer and the DAC, has one important drawback associated with the presence of idle tones in the spectrum, due to the strong correlation existing between the input signal and the quantization error. The correlation makes the noise colored so that the assumption of white noise vanishes. The problem can be mitigated by increasing the order of the loop, introducing an additional discrete time integrator.

This concept can be extended towards L order filtering (where L is the order of the filter), increasing the numbers of integrators in the loop with distributed feedback paths. For example, in the case of low-pass oversampled signals, a high order loop allows to obtain high-order noise transfer functions,

$$NTF(z) = (1 - z^{-1})^L \tag{3.9}$$

with benefit in terms of increased resolution. However, the benefit is contrasted by the difficulty in the design of stable modulator with many integrators around the loop. The problem can be overcome by adopting MASH (multistage noise-shaping) architectures, which on the other

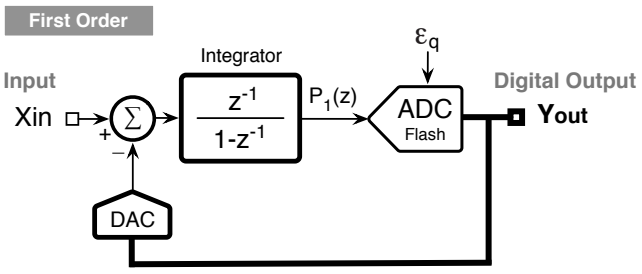

Figure 3.7: Block diagram of a First Order ΣΔ modulator.

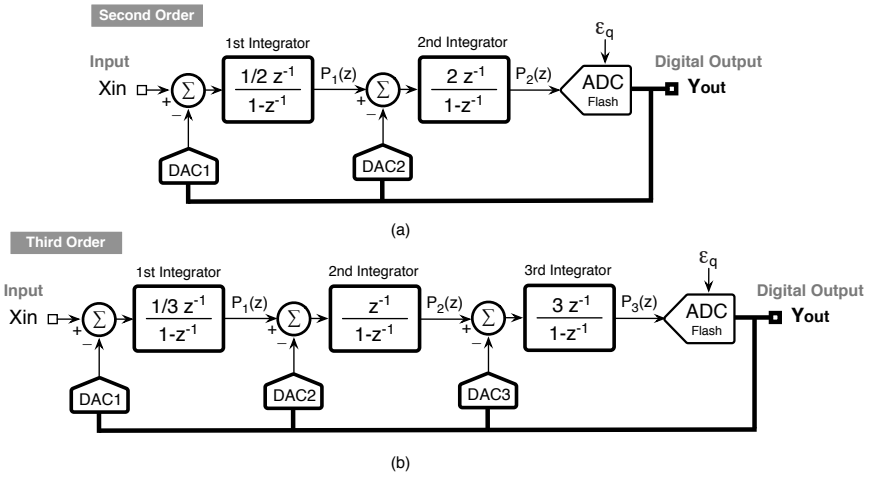

Figure 3.8: Block diagram of a conventional ΣΔ modulator: (a) Second Order. (b) Third Order.

hand, are very sensitive to mismatch of the paths, leading to an incomplete cancellation of the quantization error at the output.

Fig. 3.8 shows the block diagram of a conventional second and third-order with suitable coefficients for completely delayed integrator solutions. In these cases the transfer functions are

$$Y(z) = X(z)z^{-2} + \epsilon_q(z)(1 - z^{-1})^2 \tag{3.10}$$

$$Y(z) = X(z)z^{-3} + \epsilon_q(z)(1 - z^{-1})^3 \tag{3.11}$$

where e_{q2} and e_{q3} are the quantization noise of the second and third order respectively. The STFs are simple delay. A plot of these two NTFs is reported in Fig. 3.9. The use of high order architecture allows to push more effectively the in-band noise to high frequency, thereby increasing the performance. The slope of the NTF filtering is 20·L dB/decade. Additionally, as can be seen in Fig. 3.9, the out of band gain of the higher order NTF increases, leading to instability problem through overloading the quantizer.

In all ΣΔ modulators, as depicted in Fig. 3.5 (a), the output of the quantizer, is then processed by the decimator filter, which performs low-pass filtering and down sampling. The first operation allows to suppress all the noisy pushed to high frequency, while the latter reduces the output rate down to Nyquist frequency, shortening the width of the output word.

The ΣΔ architecture transfers most of the signal post-processing tasks to digital domain, because the digital word is dominated by DSP or digital specific μprocessor, which make easy to implement digital filtering and handling difficult mathematics operations.

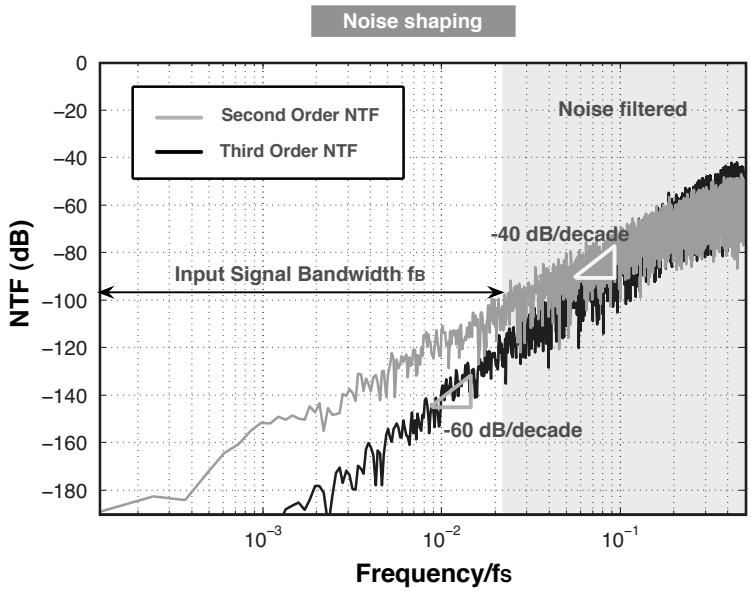

Figure 3.9: Noise transfer function (NTF) for a second and third order ΣΔ modulator.

3.3 Continuous-time ΣΔ modulator

Most of the research work done in the field of ΣΔ modulator has been focused on the development of discrete-time DT structures, mostly implemented with switched capacitor (SC) technique. The SC schemes offer more precision because the integrator gain is proportional to the ratio of capacitors, which can be integrated with high accuracy (the accuracy varies from 0.1 to 0.01% depending on layout and capacitor dimensions). Moreover, the circuits allow high linearity and the synthesis is very easy due to the low level of complication of the mathematics, that characterize these types of dicrete-time systems.

However, the increasing demand for very low power and faster ADCs has shifted the attention to the continuous-time (CT) implementation [16], [17], [18], [19], [14]. An illustrative schematic of a continuous-time ΣΔ modulator implementation is shown in Fig. 3.10.

The key difference between the CT modulator and its DT counterpart is that the sampling operation occurs inside the loop in front of the clocked quantizer, in contrast to DT modulator, where a sample and hold (S/H) circuit is placed at the input of the converter. Thus, each error (timing error in sampling process, linearity) that affects this critical block, is added directly to the input of modulator degrading the SNR performance. On the contrary, in the CT implementation, all non-idealities related to the sampling process are noise shaped. The shift of the sampling operation behind the continuous filters on the signal path, provides a further interesting feature, due to implicit antialiasing filtering. Indeed, it is not necessary the use of the antialiasing filter (AAF) in front of the modulator, as reported in Fig. 3.10. From

intuitive point of view, it is quite easy to understand this advantage: the input of the quantizer at the sampling time depends on the feedback path and on the integrated version of the input signal, over a sampling time period. Considering the integration, as a black block operator, it is possible to express the integration as the convolution of the input signal with a rectangular pulse (that lasts one sampling period). In the frequency domain, this step, corresponds to the multiplication of the input spectrum with a $sinc(\pi/f_S)$ function. This function attenuates the input spectrum exactly at the multiples of the sampling frequency f_S, realizing an intrinsic AFF filtering. As a consequence, higher order modulator and high loop-gain give rise to an increased antialiasing filtering.

The loop filter H(s) is performed using continuous-time filters, which can be active RC-filters realized using operational amplifier, operational transconductance amplifiers (OTA), g_mC schemes or even LC-resonator structures. However, the continuous-time nature of the signals around the loop allows to relax the speed and gain requirement of the active blocks, enabling the adoption of high sampling frequency. This feature is another advantage over DT implementation, where the maximum clock rate of the switched capacitor circuits is limited by the active blocks bandwidth, that affects the settling accuracy of the charge-transfer characteristic. Moreover, DT schemes are sensitive to signal-swing dependant on-resistance of the switches, glitch errors and digital switching noise.

Furthermore, continuous time implementation suffers from many problems related to large process dependent variations, that worse the final linearity of the modulator (due to harmonic distortion that appears at the output) and lead to high mismatch in the integrator gain, since it is dependent on RC or g_mC product.

3.3.1 DT-CT equivalence

The signals in a DT modulator are represented by charge pulses due to nature of charge transfer between switched capacitors, which are the basic elements of the converter. In this case, it is important to ensure the complete charge transfer between the feedback capacitors towards the integrating capacitor, in order that the finally settled valued of the signal presents a sufficient

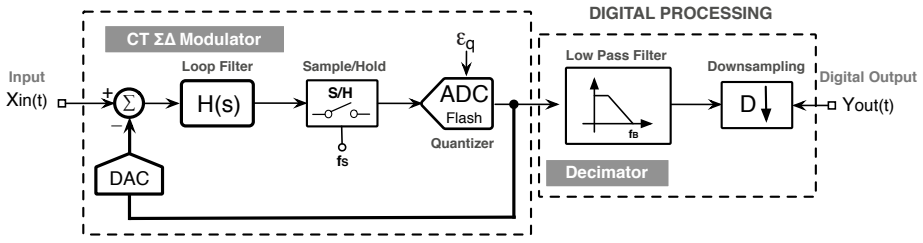

Figure 3.10: Block diagram of a CT ΣΔ modulator.

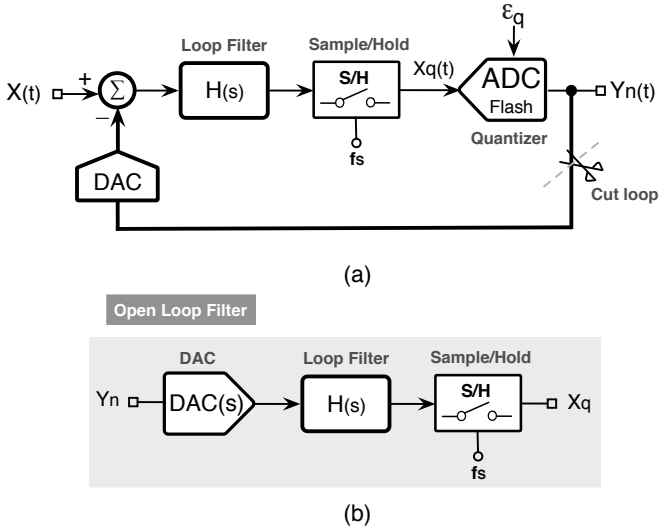

Figure 3.11: CT ΣΔ scheme: (a) Block diagram. (b) Open loop CT-DT equivalence.

accuracy. In contrast, in the CT implementation, the signals are continuous and permanently integrated over time, so that the modulator is sensitive to every change from the ideal behavior. The synthesis and the mathematical analysis of a CT ΣΔ modulator is more difficult and challenging than a DT, because the loop involves both continuous-time and discrete-time signals. However, the feedback signal in both CT and DT modulators is an analog signal, which is originated by the digital domain. In both cases, the feedback signal is processed by the respective loop filter, which is a linear system. At the end, the output of the linear system is quantized (in the CT implementation sampling and quantization occur simultaneously) and converted in digital domain. So, both modulators exhibit the same NTF, if at all the sampling times the CT and DT loops generate the same signal at the input of the quantizer for the same digital word fed at the input of their respective feedback DAC. In other words, this means to make equivalent the impulse response of both loops broken at digital output, as reported in Fig. 3.11(a) for the CT implementation. Fig. 3.12 shows a list of the most common DAC impulse responses used in the CT design. Among them, the list incorporates the non return to zero (NRZ) [3.12(a)], the return to zero (RZ) [3.12(b)], the switched resistance-capacitor discharge (SCR) [3.12(c)] and an example of arbitrary waveform [3.12(d)].

However, the shape of the feedback waveform generated by the CT DAC has a direct impact on the CT-DT equivalence. A common design approach for CT architecture normally starts with an already designed DT prototype targeted with the desired features in terms of NTF behavior. This allows to extend the design techniques and tools available for DT modulator to the design of CT counterpart.

More detailed informations about the procedure for obtaining DT-CT equivalence will be

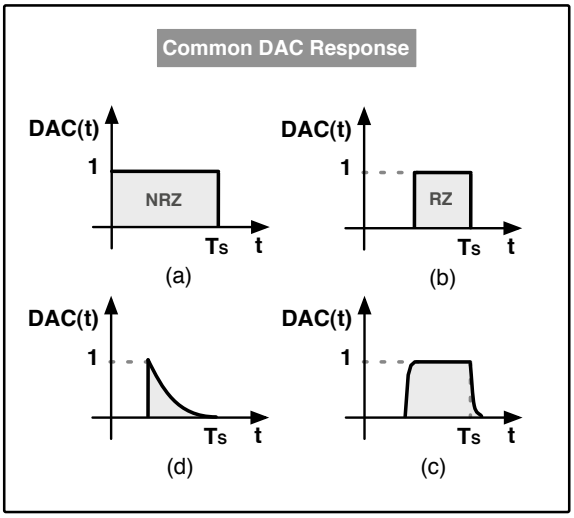

Figure 3.12: DAC impulse response. (a) NRZ. (b) RTZ. (c) SCR. (d) Arbitrary.

provided in Chapter 6.

3.3.2 Feedback DAC Error

The CT architecture is very sensitive to the non-ideal behavior of the feedback DAC, because the integration is done permanently, so any deviation from the ideal pulse shape deteriorates the quality of the noise shaping. Normally the source of non-idealities is attributable to finite GBW and slew-rate of operational amplifier, but CT implementation suffers also of timing errors of the feedback DAC's waveforms. These timing errors modify the time position and the duration of the charge injection of the feedback pulse over the sampling period. The two most important effects to be considered are the *clock jitter* and the *excess loop delay*.

- **Clock jitter**. Clock jitter is related with statistical variation of the sampling frequency due to spectral purity of the clock source [20], [21], [22]. This error affects both DT and CT modulator, but its effect is more dominant in the CT $\Sigma\Delta$. Normally in DT, the uncertainty of the sampling clock, at quantizer level, is not a real issue if the integrators settle with a given accuracy, while a jitter at sample and hold process translates in an equivalent amplitude error causing an increase of the noise floor. For the CT architecture, the error associated with the sampled internal quantizer is shaped because injected at the point of maximum error suppression. Otherwise, the dominant influence of the clock jitter in CT implementation is due to timing errors in feedback DAC, because a statistical variation of the charge injected by each DAC results in a statistical integration error and consequently in increased in-band noise. As illustrated in Fig. 3.13 (a), the statistical

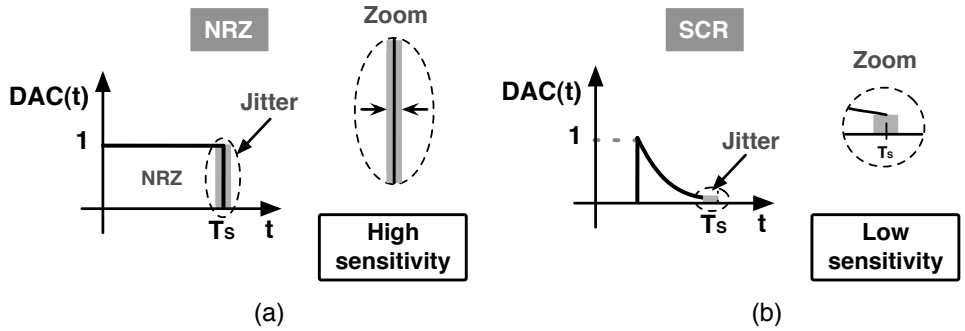

Figure 3.13: Clock jitter in CT ΣΔ: (a) Clock jitter in NRZ. (b) Decaying Pulse waveform.

variation of the charge of the feedback pulse modulates the amount of feedback injected charge over the sampling clock cycle. The error is directly proportional to the clock jitter variance, to the value of the feedback pulse at the instant of jitter occurrence and which feedback path with its scaling coefficient injects the jitter noise. The clock jitter effect is reduced by using multibit feedback DAC or as reported in Fig. 3.13 (b), by the adoption of decaying pulse shape in order to reduce the amount of injected charge at the end of the clock jitter.

- **Excess loop delay**. Excess loop delay is related to the intrinsic delay existing between the quantizer clocking edge time and the subsequent injection charge of the feedback DAC [23]. In worse case loop delay is so high that a portion of the DAC pulse is shifted into the next sampling period, leading a mismatch in the feedback CT coefficients and stability problem.

The table 3.1 presents a summary of the main benefits that characterize DT and CT ΣΔ modulators.

Advantages of CT ΣΔ	**Advantages of DT ΣΔ**
Implicit antialiasing filter	Low sensitivity to clock jitter
Allows to reach high sampling frequency	High definition of the integrator gains and transfer function
Less digital switching noise	Highly linear SC integrator
Relaxed operational amplifier requirements	Lower sensitivity to mismatch and process variations

Table 3.1: Comparison between benefits of CT and DT ΣΔ modulators.

3.4 Noise and power metrics for ΣΔ modulators

The analysis of the power spectral density of the ADC output signal is straightforward, because it is possible to extract all the informations about the features and limits of the converter. Especially for a noise shaping converter, like the case of ΣΔ modulators, the analysis in frequency domain is the best solution. The most popular specifications and their technical terms are explained as follows [12].

- **Oversampling ratio (OSR)**. This parameter is defined as:

$$OSR = \frac{f_S}{2f_B} \tag{3.12}$$

  where f_S is the sampling frequency, while f_B is the signal bandwitdh. Oversampling technique helps to relax the requirement of the antialiasing filter, improves resolution spreading the noise over a larger bandwidth, but on other hand increases the power consumption.

- **Signal to Noise Ratio (SNR)**. The SNR is very important because it quantifies how much an ADC corrupts the information of the input signal, by adding noise. This parameter is often expressed using the decibel scale (dB) and defined by:

$$SNR|_{dB} = 10 \cdot log\frac{P_{sig}}{P_{noise}} \tag{3.13}$$

  where P_{sig} and P_{noise} are the power of the signal and the power of the noise in the band of interest, respectively. Moreover the SNR depends on the frequency of the input signal and it decreases proportionally to the input amplitude.

- **Signal to Noise and Distortion Ratio (SNDR)**. The SNDR is an extension of the definition of SNR. It is defined as the ratio between the power of the signal and the sum of noise and all distortion power components. The spectra are obtained by applying an input signal with a frequency $f_{sig} \leqslant f_B/3$, in order to include at least the second and third harmonic in the band of interest.

- **Total Harmonic Distortion (THD)**. It is defined as the ratio of the sum of the signal power of all harmonics above the fundamental frequency to the power of the fundamental frequency.

- **Spurious-Free-Dynamic-Range (SFDR)**. This parameter is defined as the ratio of the signal power and the power of the strongest spectral tone in the Nyquist band. It dominates the resulting ADC linearity. Moreover, its influence depends on the application and, for example, it is very important in telecommunications systems because it represents the smallest value of input signal that can be discriminated from a large and close interfering signal.

- **Effective-Number-of-Bits (ENOB)**. The noise is a limit that affects an ADC and this parameter measures the signal to noise and distortion ratio using bits definition. It is expressed by:

$$ENOB = \frac{SNDR|_{dB} - 1.76}{6.02} \tag{3.14}$$

  where SNDR is the signal to noise and distortion ratio.

- **Dynamic-range (DR)**. It is defined as the ratio between the largest signal that the converter can handle and the noise level, expressed in dB. It determines the maximum achievable SNR. In other terms, it represents the value of the input signal at which the SNR is 0 dB.

- **Figure of Merit (FoM)**. This parameter measures the power effectiveness of the modulator and depends on architecture solution and technology used. In literature, different definition of FoM are used, but the most common is:

$$FoM = \frac{P}{2^{ENOB} \cdot 2 \cdot f_B} \tag{3.15}$$

  where P is the total power consumption, f_B is the signal bandwidth and ENOB is the effective number of bits, as described before. It is measured in Joules-by-conversion level (J/conv-level). Thus, the term is used to compare different modulator implementations with each other.

Chapter 4

Low Power Techniques: State of the Art

4.1 Introduction

The mobility request of the portable electronics demands more complex processing but with a limited power refueling. Nowadays, the major design concern is the optimum trade-off between power and performance, in order to minimize the power consumption, with benefits in terms of increased battery lifetime.

The power consumption, is simply given by the product of voltage to current, so lowering the supply voltage at constant current reduces power. However, the reduction of the available voltage headroom due to the shrinking of the CMOS processes, introduces severe constraint for achieving acceptable dynamic range. The consequence is the degradation of the signal to noise ratio (SNR) due to the increased relevance of the noise floor (ad example the KT/C noise or the thermal noise).

Indeed, in a KT/C limited design, the SNR is proportional to OSR$\cdot V_{FS}^2\cdot$C/(KT), so the reduction of the full scale voltage involves the increase of the sampling capacitance C, in order to reduce the noise floor. A given OSR requires a certain product gain bandwidth (GBW) for the op-amp, which as well know is proportional to the ratio g_m/C. The transconductance g_m, for a transistor in saturation region, is proportional to the square root of the current ($\propto \sqrt{I_D}$). Including these considerations, the SNR is proportional to OSR$\cdot V_{FS}^2\cdot\sqrt{I_D}$/(KTGBW). The last relationship shows that, the reducing by a factor α of the supply voltage (or equivalently of the full scale voltage range V_{FS}), requires to increase the current of factor α^4 in order to preserve the SNR. Therefore, the reduction of the supply voltage is not advisable to reduce power consumption. The challenge is further complicated when deeper technologies are used due the influence of short channel effects, such as velocity saturation, which diminish the transconductance and the dc gain effectiveness.

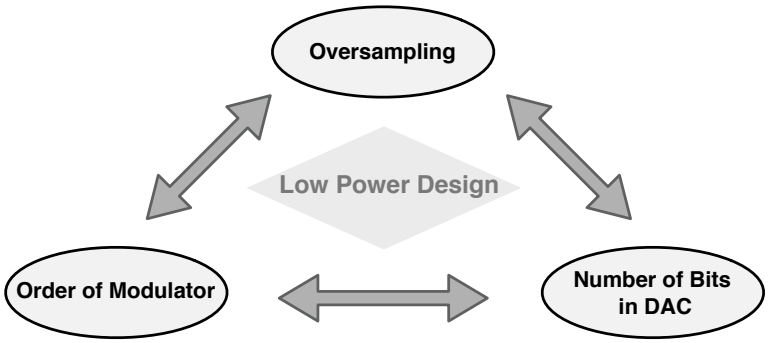

Figure 4.1: Trade-off for low power design.

However, the research of low power consumption in the design of ΣΔ modulator, must be achieved without affecting the final performance of resolution and linearity thank to the adoption of new design techniques. In a ΣΔ modulator design, the low power goal can be obtained by a proper choice of three design parameters that affect directly the resolution (as reported in Fig. 4.1): *the oversampling ratio* (OSR), *the order of the modulator* (L) and *the number of bits of the quantization* (n) [24], [25].

- The oversampling technique allows to increase the resolution by reducing the in-band noise, spreading the total noise over a larger bandwidth. On the contrary, this increases the sampling frequency and augments the need of high bandwidth (GBW) and high slew-rate operational amplifiers, thus affecting the power consumption. At first approximation, if the sampling frequency increase by a factor β, the power consumption of the operational amplifier increases of β^{α}, where α in general is around 2 and depends on technology. Moreover, the improvement in SNR due to oversampling depends on the order of modulator; for example in a second order low-pass ΣΔ modulator the resolution increases of 2.5 bit for every doubling of the OSR, while in the third order the improvement is 3.5, with the same number of bits in the quantizer. Therefore, any decision to increase the OSR must be well balanced between complexity of the structure, power consumption and simplicity of the anti-aliasing filter.

- The noise shaping order (L) coincides with the number of integrators used in the loop, so high-order noise shaping behavior demands for a large number of operational amplifiers, affecting the power consumption and the stability of the loop.

- The use of multi-bit quantizer increases the final resolution, because the SNR improvement is proportional to 6.02·n, where n is effectively the number of bits in the DAC. However, the use of multi bit DAC is source of harmonic distortion due to the mismatch between the unitary elements. Anyway, the problem can be mitigated using properly DEM (Dynamic

Element Matching) techniques [26], [27], that translates mismatch into noise, which is filtered (noise shaped) by the loop.

The following sections present several design techniques, that recently have been reported in literature. Anyway, the best choice is not fixed, but depends from many constraints (technology, complexity, area, ...) and from field of application (linearity, input signal bandwidth, ...), so the knowledge of all limits that affect the ΣΔ modulator family, is very important for the designer to optimize the power consumption without sacrificing the performance.

4.1.1 DAC resolution reduction

In a ΣΔ architecture the improvement in the SNR due to resolution of the feedback DAC is linear and proportional to 6.02·n (where n is the number of bit of the DAC). The use of a flash ADC limits the maximum number of bits, because for an added k comparators, the improvement in final resolution is equivalent to $log_2(k-1)$. An high number of comparators introduce more constraints in the circuit design in terms of sensitivity, noise and offset, making necessary the adoption of calibration circuits and DEM techniques for DAC in order to reduce harmonic distortion. A possible solution uses less levels for the DAC compared to the ADC ones, without losing resolution, thank to Leslie-Sing method ([28]) or truncation. The ΣΔ architecture uses a *m-bit* ADC and *n-bit* for the feedback DAC. The reduction of the resolution from m to n is simply realized by truncating the output digital word by discarding the last m-n LSB. The post processing of the completed digital word and its truncated version provides the output of the modulator ([29]).

Another promising technique reduces the number of bits by using a digital ΣΔ, as shown in Fig. 4.2. The truncation error modeled as additive white noise, is shaped by the digital modulator with its NTF, so that $Y_1 = Y + \epsilon_T(1-z^{-1})^k$, where k is the order of the auxiliary modulator. The term $\epsilon_T(1-z^{-1})^{k-1}$ cancels the effect of the shaped truncatin noise injected by the input DAC ([12]).

4.1.2 Parallelism

At the beginning the ΣΔ techniques have been widely used for low-bandwidth and high resolution application, but nowadays are being extended to new telecommunication fields, which require signal bandwidth in the megahertz range and sampling frequency in the order of 100 MHz. At these frequency, the design is complicated due to the onset of high-frequency limitation of the op-amps and switches. These problems can be overcome by adopting properly technique that allow to increase the oversampling ratio without speeding the analog building block; in the literature have been proposed two techniques: *double sampling* [30] and *time-interleaved* technique [31].

The double sampling technique is an efficient solution for DT ΣΔ architectures, which use switched capacitor circuits. It allows to speed up the processing by optimizing the operation

of the op-amp in the clock period. Generally, the clock period is dedicated for the 50% to the sampling of data and the remaining 50% to the active integration realized by the op-amp. The integration of the data lasts only half of the clock period, due to necessity to wait the quantization and sampling phases. The process can be improved if during the sampling phase of the actual data, the op-amp is used to realize the integration of the previous data. The operation is simply done by using an auxiliary switched capacitor network with properly phases. In this way, the final sampling frequency is double of the actual modulator clock frequency, without increase the speed of the op-amp, but augmenting in a little increasing of the slew-rate requirements. Moreover, in ΣΔ architecture the technique gives rise to an improvement of 3(2· L+1) dB, where L is the order of the modulator. However, this technique is affected by some limitations, that restrict its application. The main problem is related to the modulation of the input signal introduced by the mismatch between the two switched capacitor paths: the effect is the folding of the input near the $f_S/2$ of the spectrum [32]. The problem is resolved using a switched capacitor integrator with a fully floating input branch [32]. Another limit is related to the stringent timing constraint because the op-amp uses the full clock period and the quantization must be realized during the non-overlapping times of the clock. A simple solution is proposed in [33], that introduces two fully cycle delayed switched capacitor paths, which are summed in front of the quantizer.

Another technique is the time-interlevad (TI) solution, which allows to increase the oversampling rate of the modulator of M times, thank to M parallel processing path, whose effects are added at the output, in the digital domain. Therefore, the circuit implementation of the TI DT ΣΔ modulator, is limited by quantizer domino and channel mismatch effects. Quantizer domino effects occurs when a given quantizer output is connected directly to another quantizer input without any delay element. This effect can only be prevented for two channel structure by using a double sampling capacitor architecture. Anyway, the structure reported in Fig. 4.3, proposed a new predictive TI scheme, that is completely free of the quantizer domino and less

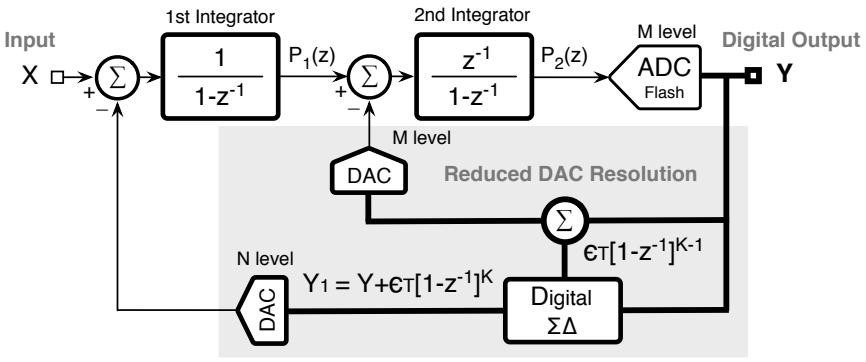

Figure 4.2: Second Order DT ΣΔ modulator with reduced DAC resolution.

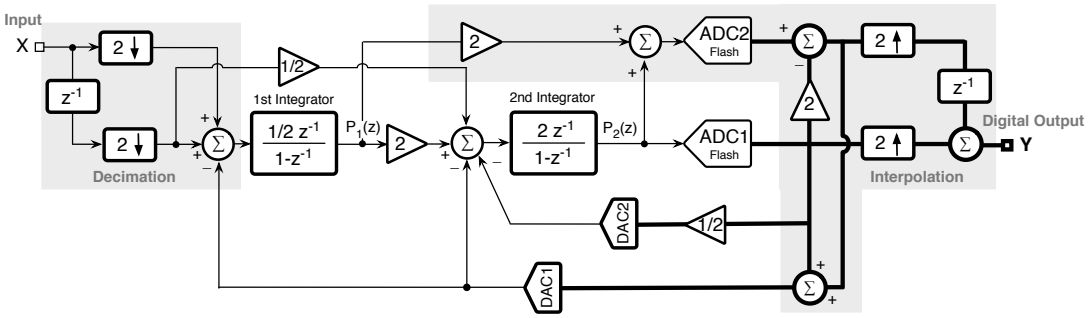

Figure 4.3: Second Order DT ΣΔ modulator: two channel interleaved structure.

sensitive to mismatch effect thank to the optimization of the feedback path [34].

4.1.3 Reduction of the numbers of operational amplifiers

The order of the ΣΔ modulator, which corresponds to the number of integrator used in the closed loop, determines the effectiveness of the noise shaping. However, the reduction of the number of op-amps is a good solution to increase the efficiency of the modulator and as consequence the reduction of the power consumption. The simplest way to reduce the number of integrator is the time-sharing technique, which consist in the rearrangement of the signal processing, in order to perform with a single op-amp multiple operations during the entire clock period, like presented in [35].

This solution has been effectively implemented with switched capacitor network, but the final benefits in terms of reduced power consumption is less than 50%, due to increased slew-rate performance. For example, the double sampling technique discussed before is an example of time-sharing approach, but its benefits is around 40%.

Another effective way for reducing the number of op-amp is the general solution proposed in [35] as an extension of the approach proposed in [36]. Consider the generic DT ΣΔ architecture

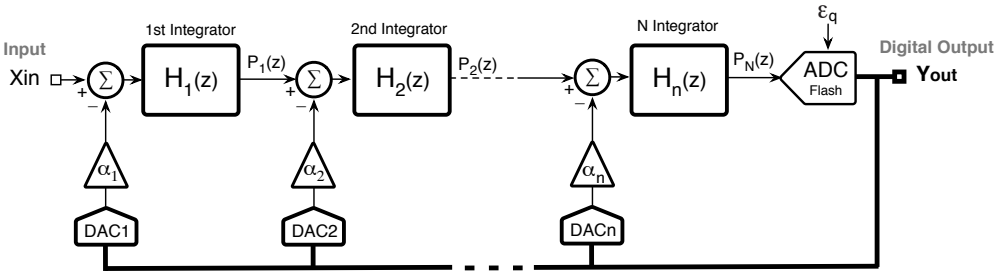

Figure 4.4: Block diagram of a generic n-order DT ΣΔ modulator with distributed n feedback.

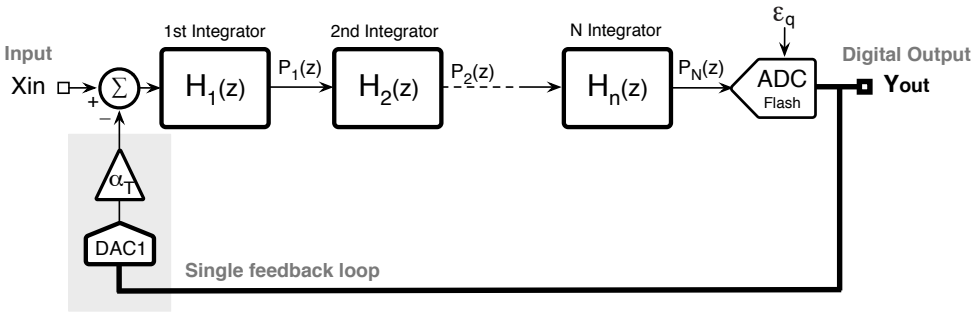

Figure 4.5: Second Order DT ΣΔ modulator with single feedback loop.

reported in Fig. 4.4: it is a cascade of n discrete integrator (delayed or not) with distributed n feedback. The technique, with a topological rearrangement, moves the feedback path, from the input of the *i-th* stage, to the input of the previous *(i-1)-th* by diving its contribution with the transfer function $H_{i-th}(z)$. At the end, when all the total feedback paths are moved to the first feedback position (Fig. 4.5), the resulted coefficient α_T is:

$$\alpha_T = k_1 + \frac{k_2}{H_1(z)} + ... + \frac{k_n}{\prod_{i=1}^{n-1} H_i(z)} \tag{4.1}$$

The cascade of the analog blocks $H_1(z), ..., H_n(z)$ can be replaced with a reduced number of operational amplifiers. The final integrator is:

$$H_T = \frac{z_p}{(1 - z^{-1})^n} \tag{4.2}$$

where n is the number of cascaded integrators and p is the delay around the loop.

4.1.4 Operational amplifier swing reduction

The reduction of the available power supply voltage due to the shrinking of the dimension of the transistor, introduces a lot of constraints in the design of ΣΔ modulators. The reduction of the headroom voltage involves the lowering of the available voltage swing at the output of the integrators, thus leading to a strong degradation of the dynamic range (because the noise floor remains unchanged). This problem can be resolved with two different approaches: using rail to rail analog block or develop new architecture of ΣΔ. The former solution consists to design operational amplifiers, that permit to extend the output swing very close to the supply limit, but typically they require additional circuitry, thus increasing the circuitry complexity and as consequence the power consumption. The latter solution requires topology modification of the architectures, able to reduce the swing of the output of the integrators. For example, a possible reduction of the swing can be obtained by simply scaling the gain of the integrators. However,

this solution is not suitable when the speed and the thermal noise (KT/C) are severe constraints. Indeed, in a DT ΣΔ modulator, the reduction of the gain is achieved by reducing the sampling capacitance (leading in a KT/C increasing) or by increasing the feedback capacitance (but the capacitance load that affects the operational amplifiers increases).

However, the last solution is the most effective, because the minimizing of the operational amplifiers output voltage swing offers several advantages:

- *the relaxing of the slew-rate and bandwidth requirements with benefits in terms of power consumption;*
- *ensures better linearity and consequently reduces the harmonic distortion;*
- *allows to use power efficient operational amplifier architecture, like the single stage telescopic scheme.*

The use of analog feedforward paths (AFF) on each amplifier output node reduces its voltage swing [37]. However, this technique is not power efficient, because it requires an analog adder block before the quantizer, as reported in the conventional architecture shown in Fig. 4.6 ([38], [39], [40]). The analog summa can be done by using another operational amplifier [41] or with a passive switched-capacitor network [42]. The former solution is usually implemented because it ensures high sufficient gain, but on the contrary introduces design complexity due to the large output swing of the summing operational and increases the final power consumption. The latter solution exploits the charge sharing of a passive switched capacitor network connected directly to the input of all comparators. Furthermore, the need to maintain the signal swing at the input of the ADC, requires to scale the reference voltage by a factor equal to the voltage drop across the passive network due to its intrinsic parasitics. This leads to higher sensitivity specification for comparators, resulting in increased power consumption and sensitivity to mismatch effects.

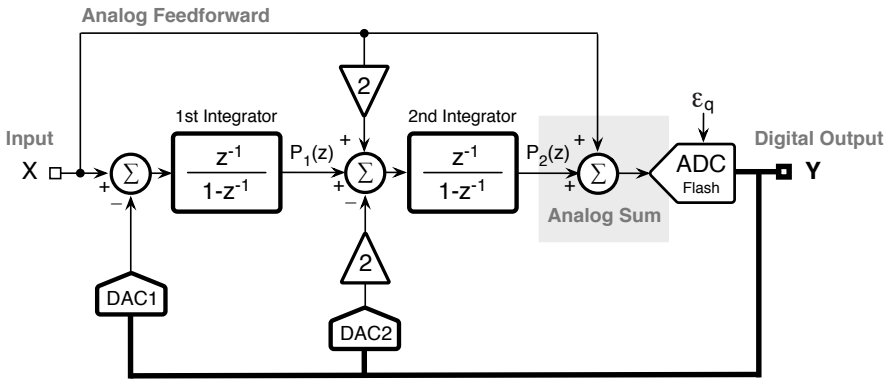

Figure 4.6: Swing reduction in a second order DT ΣΔ modulator with analog feedforward (AFF) paths.

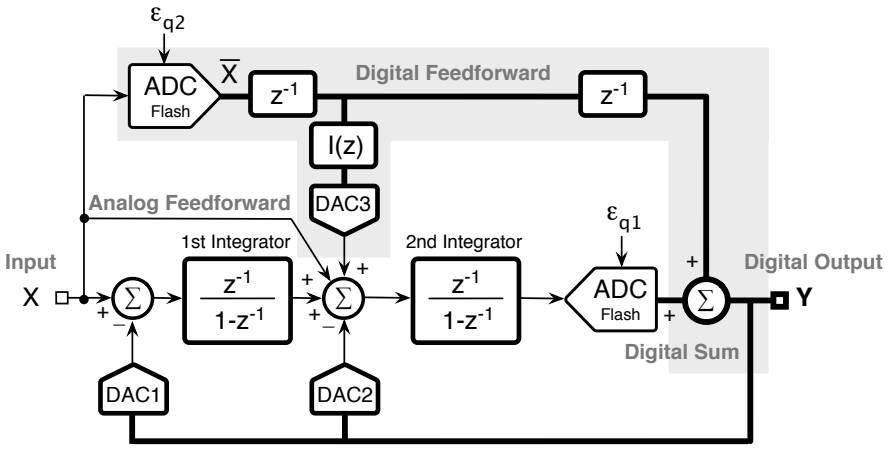

Figure 4.7: Swing reduction in a second order DT ΣΔ modulator with digital feedforward (DFF) path.

These limits can be attenuated using an additional compensation capacitance, as expressed in [43].

An improved solution realizes the input feedforward path in the digital domain [38], [44]. The digital feed-forward (DFF) signal, as shown in Fig. 4.7 [45], is a n-bit quantized version of the input signal. The method needs an extra second flash ADC but the total number of the comparators does not increase. Therefore, the additional branch I(z) at the in put of the second integrator compensates the effect of the quantization error ϵ_{q2}. The I block add an opposite contribution to the one given by DFF in the digital domain at the output of the modulator. The transfer function of I(z) block is given by:

$$I(z)\frac{g_2 z^{-1}}{1-z^{-1}} = -z^{-1} \Longleftrightarrow I(z) = -\frac{1-z^{-1}}{g_2} \tag{4.3}$$

where g_2 is the gain of the second integrator.

A fully digital feedforward solution is exposed in [40]. The method applied to a conventional second order ΣΔ architecture is depicted in Fig. 4.8. To preserve the same unity STF, the output of the auxiliary ADC (X + ϵ_{q2}) multiplied with $(1 - z^{-1})$ is subtracted in the digital domain from the output of the main flash ADC. Moreover, the effect of the quantization error ϵ_{q2} is deleted at the output of the modulator. Thus, the overall output of the ΣΔ modulator is designed to be

$$Y = X \cdot STF + \epsilon_{q1} \cdot NTF = X + \epsilon_{q1} \cdot (1 - z^{-1})^2 \tag{4.4}$$

The internal swing of the nodes are reduced and the effect of $\epsilon_{q2}(1 - z^{-1})$ is shaped at first-order in the feedback loop.

Another approach has been developed in [46]. The proposed architecture is an improved low-

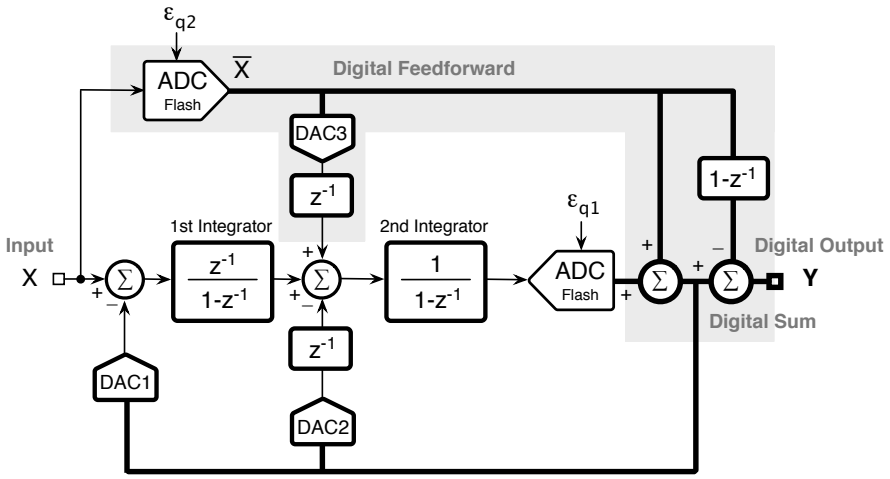

Figure 4.8: Swing reduction in a second order DT ΣΔ modulator with fully digital feedforward (DFF) path.

distortion DT ΣΔ modulator targeted for wide-band applications. It is based on quantization noise coupling that allows to boost the noise shaping performance from second to third order. This is achieved by an added injection of the quantization noise into the loop (Fig. 4.9), without changing the STF of the starting second order architecture. The method is also effective for integrators output swing reduction, but the need to use an auxiliary summing operational amplifier before the quantizer, reduce the final power-efficiency of the structure.

An alternative strategy that merges the reduction of the number of operational amplifiers technique with the output swing reduction, is shown in Fig. 4.10(a). The proposed structure

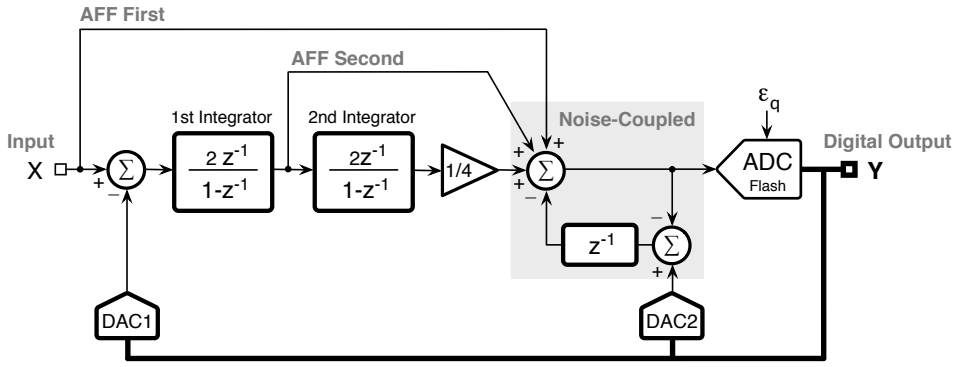

Figure 4.9: Third order DT ΣΔ modulator with shaped quantization noise injected via noise coupling.

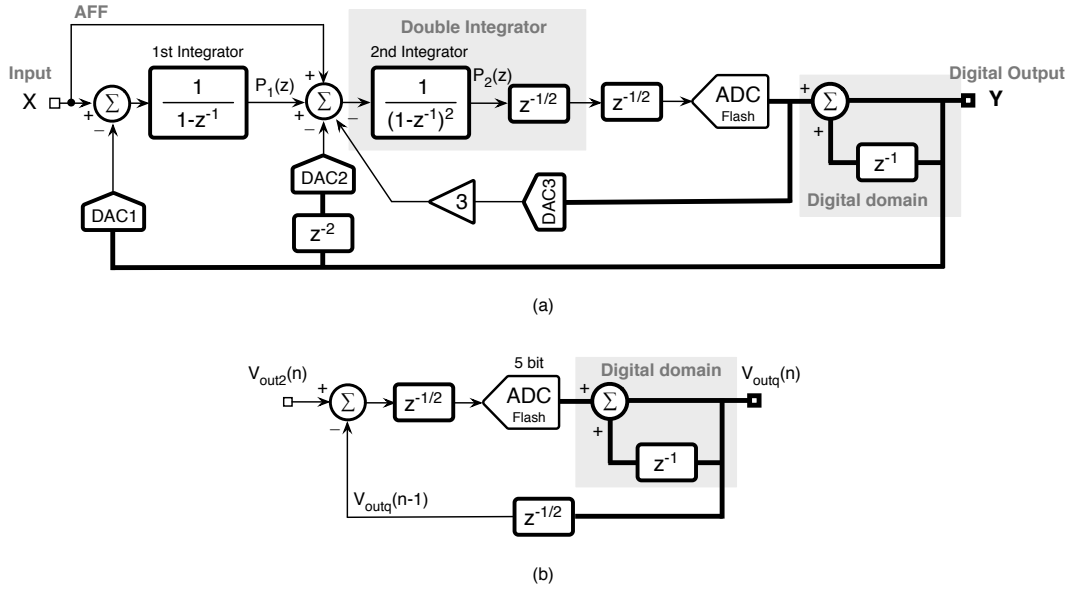

Figure 4.10: Third order DT ΣΔ modulator with two operational amplifiers.

obtains a third order noise shaping behavior, by using only two operational amplifiers. This interesting feature is realized thank to topological transformation, which replaces a double integrator block with transfer function $1/(1-z^{-1})^2$, with a single integrator closed in feedback with two auxiliary paths $+z^{-1}$ and $-z^{-2}$.

Regarding the reduction of the swing, the main idea of the architecture is based on the observation that, for a given OSR, there is some correlation between two successive inputs, [47]. The feature suggest the scheme of Fig. 4.10(b) which allows to reduce the flash input signal amplitude. In particular, the input of the flash ADC is the difference between the output of the last operational amplifier (Vout2(n)) and its delayed and quantized version (V$outq$(n-1)). The reconstruction of the information is realized retrospectively in the digital domain, by adding the previous subtracted part. The reduction of the input swing of the flash, permits to reduce the required number of the comparators. The use of high resolution ADC (flash) guarantees a low level quantization noise that helps to increase the effectiveness of the method. However, this technique is prone to potential instability due to the presence of the term $1/(1-z^{-1})$ in the loop, which leads to a positive recursive feedback in digital domain.

Finally, an aggressive low-power efficient solution is proposed in ([48], [49]). The novel DT ΣΔ architecture reported in Fig. 4.11, achieves a third-order noise shaping by using only one operational amplifier working in time sharing fashion. The synthesis of the NTF is realized by using the noise shaping enhancement technique. This technique allows to determines and injects the missing terms of the quantization error, that obtain the desired noise transfer function starting from a given one. These missing terms of the quantization error are processed by a

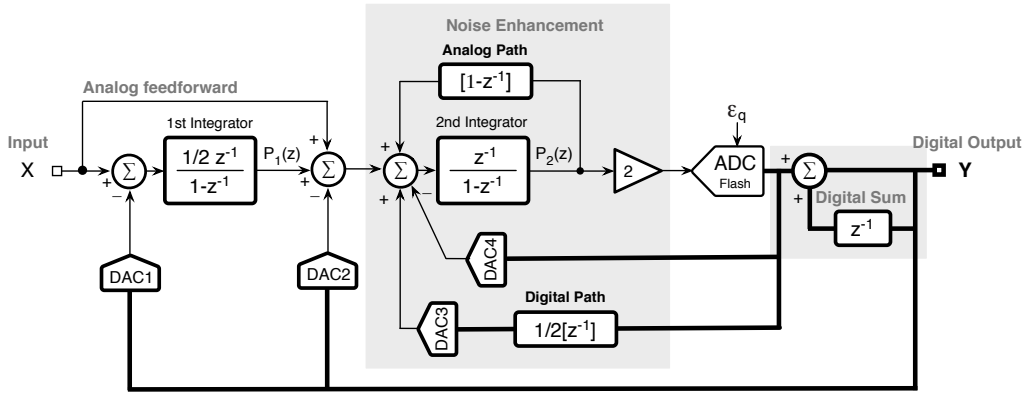

Figure 4.11: Third order DT ΣΔ modulator with single operational amplifier.

passive switched capacitor network. However, the increased load capacitance demands for an increased slew-rate specification, achieved with an auxiliary circuitry included in the operational amplifier. The added circuit senses the unbalance of the amplifier and helps to injects more current at the output in order to increase the slew-rate. The scheme also obtains the swing reduction of the output of operational amplifier by using a mix of analog feedforward path (AFF) and correlation technique, proposed in [47].

Chapter 5

Digitally Assisted Third-Order $\Sigma\Delta$ modulator with Two Operational Amplifier

The chapter explains the synthesis and the design of a low-power third order low-pass discrete time (DT) $\Sigma\Delta$ modulator targeted for WCDMA requirements in a 65 nm CMOS technology. The modulator achieves about 14 bit over 2.2 MHz input signal bandwidth. The proposed architecture obtains a third order noise shaping behavior with only two operational amplifier by using the noise shaping enhancement technique. Moreover, the structure integrates a new swing reduction technique that reduces the swing of the two integrators to a very small level comparable with the dynamics of a quantization noise. The last feature allows to implement a single telescopic stage operational amplifiers increasing the power efficiency. The integration of different power reduction techniques limits the power consumption to 2.3 mW, thus yielding an optimum FoM of only 43.8 fJ/conversion-level. Finally, experimental measurements confirm the effectiveness of the architecture.

5.1 ADC Specification for WCDMA standard

The rapid growing of the market of portable phone and the demand for new telecommunication services with high rates and different operating modes, have pusched the definition of new wireless communications standards. The transition from the second generation (2G) digital system toward the third generation (3G) is driven by the definition of the wide-band code division multiple access (WCDMA) standard, based on QPSK modulation.

Fig. 5.1 shows a simplified block diagram of a conventional Zero-IF or direct conversion WCDMA receiver. The incoming RF signal received by the antenna is filtered with a high

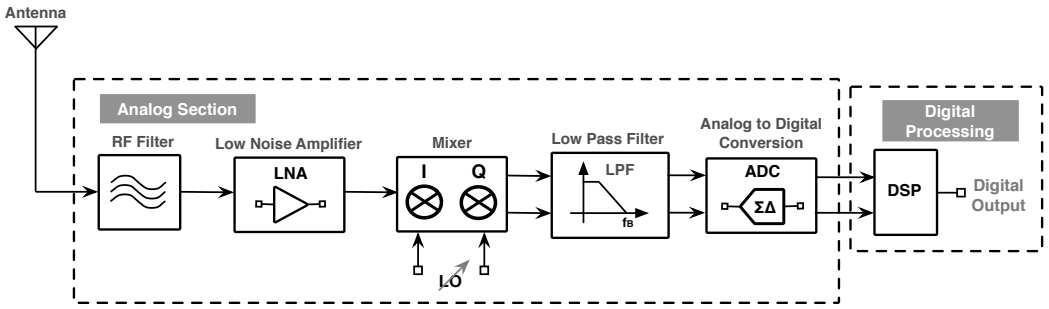

Figure 5.1: Block diagram of the direct conversion homodyne receiver architecture.

RF selectivity filtering stages and sends through a low noise amplifier (LNA). The following stage is a mixer (LO) that translates directly the RF signal to the base-band frequency without operations at intermediate frequencies. The architecture suffers of DC offset and 1/f noise that affects the information of the base-band signal. The base-band channel selection is performing by tuning the RF frequency of the mixer at the centre of the desired channel. This operation avoids the problem of image frequency, because the image and the channel in this case are equal. After the mixing, a low-pass filter (LPF) removes the nearby channels and interferers before the A/D processing. At the end, the digital post-processing realized with a specific DSP, allows further selectivity, demodulation and data decoding operation ensuring adaptability to different operating environment.

The architecture is suitable for higher integration solution and multi-standard, but limitation of the selectivity filters due to adjacent channel interference protection, shifts a lot of constraints on the ADC performance. In this challenging scenario, the best ADC converter topology is the $\Sigma\Delta$ architecture, which offers better linearity, robustness to low precision analog building block and presents intrinsic bandwidth resolution trade-off in the noise shaping characteristic. The required ADC performances for WCDMA application are reported in table 5.2.

Another important point to be considered is that nowadays the driving forces in the fields of portable electronics devices are the final cost and the battery life, so area and very low power consumption become fundamental aspects. In modern deep-submicron CMOS processes, the low cost is obtained by using a single chip solution, well known as System on a Chip (SoC), that integrates analog and digital circuitry on the same die. Otherwise, the nanometer CMOS technologies poses new hard challenges for analog circuit design due to new predominant physical effects such as low supply voltage, short-channel effects, increased sensitivity to process variation and leakage currents. This motivates the development of new design techniques that

Table 5.1: Specification targets for ADC

Standard Bandwidth	**SNR (dB)**	**SNDR (dB)**
WCDMA (1.92 MHz)	> 70	> 75

allows to relax the requirements of the analog circuit, so that the design of ADC still continue also with deeper technology.

The rest of the chapter will focus on the detailed study, design and realization of innovative very low power third order DT ΣΔ modulator targeted for WCDMA specification with a 65 nm CMOS process.

5.2 Synthesis of a Third-Order NTF with Two Operational Amplifiers

The order, L, of a ΣΔ modulator determines its noise shaping performance. Generally, a L-order loop filter requires the use of a chain of L operational amplifiers. An aggressive noise shaping is, therefore, power demanding and introduce stability problems of the loop. However, for portable applications that require medium-high resolution (12-14 bit) and bandwidth in the 2-4 MHz range, [50], [36], a multi-bit third order modulator with relatively low oversampling ratio (OSR) is a good architectural choice.

The new design strategy proposed in this work consists in determining those missing terms that obtain the desired noise transfer function starting from a given one. As mentioned, this study aims achieving a third-order NTF starting from a conventional second-order modulator, as shown in Fig. 5.2, but the method can be extended to more complex cases. The NTF of a second and of a third-order ΣΔ are respectively

$$\epsilon_q(1-z^{-1})^2 = \epsilon_q(1-2z^{-1}+z^{-2}) \tag{5.1}$$

$$\epsilon_q(1-z^{-1})^3 = \epsilon_q(1-3z^{-1}+3z^{-2}-z^{-3}) \tag{5.2}$$

where ϵ_q is the quantization error. The difference between (5.1) and (5.2) gives

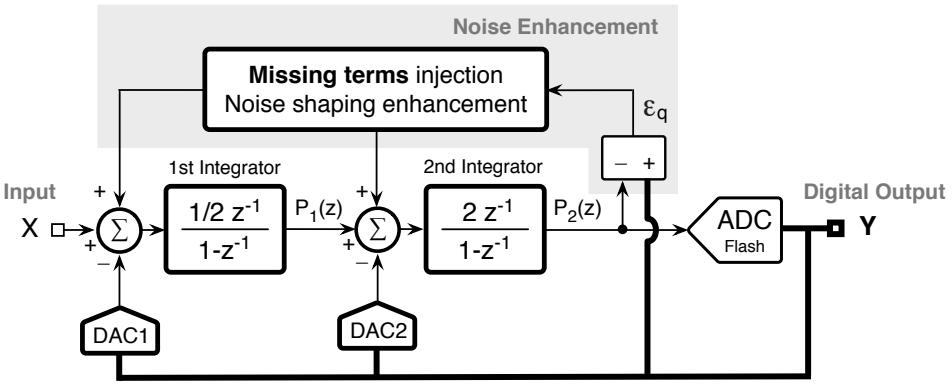

Figure 5.2: Enhancement of the NTF in a conventional second-order ΣΔ modulator.

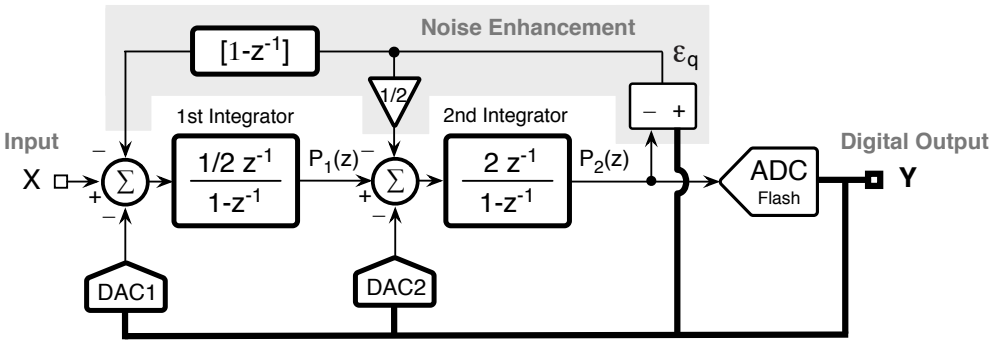

Figure 5.3: Third-order ΣΔ modulator with missing term injection in two integrators.

$$\epsilon_q(-z^{-1} + 2z^{-2} - z^{-3}) \tag{5.3}$$

which can be rearranged as follows

$$\underbrace{z^{-2}\epsilon_q(1 - z^{-1})}_{\text{First term}} - \underbrace{z^{-1}\epsilon_q(1 - z^{-1})}_{\text{Second term}} \tag{5.4}$$

The two terms highlighted in (5.4) have to be respectively injected at the first and second integrator inputs of Fig. 5.2. However, since the signal transfer function (STF) from the input to the output of the modulator is z^{-2}, the missing term to be injected at the first integrator input is $(1 - z^{-1})$, as shown in Fig. 5.3. The STF calculated from the input of the second integrator to the output of the modulator, STF_2, is $2z^{-1}(1 - z^{-1})$. The missing term to be injected at the second integrator input is therefore $-1/2$.

An equivalent, but more effective topology can be obtained by injecting the missing terms only at the input of the second integrator. Consider the following rearrangement of (5.4)

$$-z^{-1}\epsilon_q(1 - z^{-1})(1 - z^{-1}) \tag{5.5}$$

which can be more conveniently rewritten as

$$\underbrace{2z^{-1}\epsilon_q(1 - z^{-1})}_{\text{STF}_2}\underbrace{(-(1 - z^{-1})/2)}_{\text{Missing term}} \tag{5.6}$$

The injection of the missing term highlighted in (5.6) at the input of the second integrator leads to the scheme of Fig. 5.4. The effectiveness of solutions depends on the extra circuitry and the sensitivity on coefficients. Since the feedback terms coming from the DAC can be combined together in the digital domain, what matter for the increased complexity are the analog extra feedbacks. Obviously, obtaining third order with a second order basis worsens the feedback factors. The challenge is to obtain the best trade-off for achieving minimum power. For the

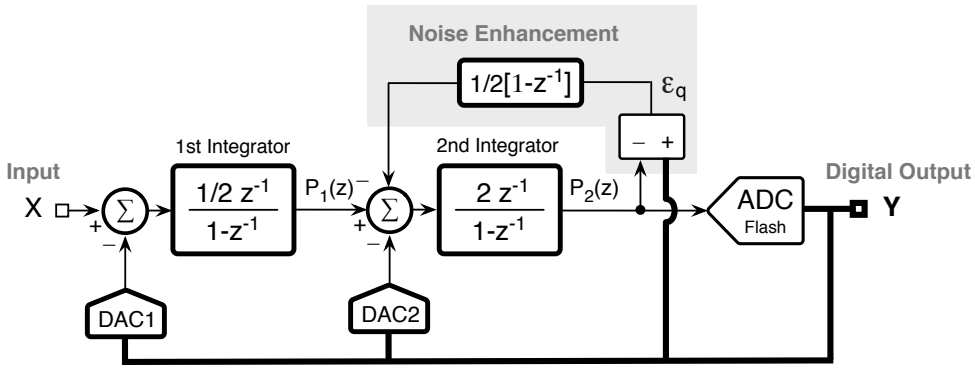

Figure 5.4: Improved third-order ΣΔ architecture with single missing term injection.

scheme of Fig. 5.3, a direct connection of a capacitor from output of the second op-amp to input of the first realizes the $(1 - z^{-1})$ term. This is not achievable for the extra term of Fig. 5.4 that requires an analog delay. Anyway, notice that the circuit implementation of the scheme of Fig. 5.4, compared to the one of Fig. 5.3, is more compact, uses favorable feedback coefficients and results in a simpler circuital implementation.

Both schemes of Figg. 5.3 and 5.4 require the use of switched capacitor networks to realize the missing terms injection. The effect of capacitors mismatch has to be carefully considered. To this end, the terms that make the third-order noise shaping in Fig. 5.3 are considered equal to $(\alpha_1 - \alpha_2 z^{-1})$ and $(-\alpha_3/2)$, being α_1, α_2, and α_3 coefficients that account for the capacitors mismatch. The same can be done for the missing terms in Fig. 5.4 that become $(\alpha_4 - \alpha_5 z^{-1})/2$. Considering these coefficients, the NTFs of the schemes of Figg. 5.3 and 5.4 are respectively

$$NTF_1 = 1-(2+\alpha_3)z^{-1}+(1+\alpha_1+\alpha_3)z^{-2}-\alpha_2 z^{-3} = NTF-\alpha_3 z^{-1}+(\alpha_1+\alpha_3)z^{-2}-\alpha_2 z^{-3} \quad (5.7)$$

$$NTF_2 = 1-(2+\alpha_4)z^{-1}+(1+\alpha_4+\alpha_5)z^{-2}-\alpha_5 z^{-3} = NTF+(1-z^{-1})(\alpha_4 z^{-1}+\alpha_5 z^{-2}) \quad (5.8)$$

Coefficients α_1, α_2, α_3, α_4, and α_5 move the original zeros placement. Typical modern CMOS technologies ensure good capacitor matching coefficients. Values of $0.2\,pF$ or higher provide accuracies as good as $\pm 0.02\%$ or better. Using that figure, a Montecarlo simulation (30 runs) spread the roots of (5.7) as shown in Fig. 5.5. The errors affect all the zeros. Two of them are complex conjugates and fall inside or outside the unity circle. The third zero is real inside or outside the unity circle. For (5.8) the errors move only two of the zeros while one remains at $z = 1$. The moved zeros are real or complex conjugates, as shown in Fig. 5.6.

The slight shift of zeros changes the NTF at low frequency. Therefore, its effect on the SNR is noticeable only for high oversampling ratios. However, we can observe that the same mismatch causes a lower spread (about 3 times less) of zeros for the scheme of Fig. 5.4 than the one of Fig. 5.3. Also, complex conjugates zeros close to the unity circle possibly enlarge the noise shaping bandwidth. Therefore, the reduced mismatch sensitivity and the possible to

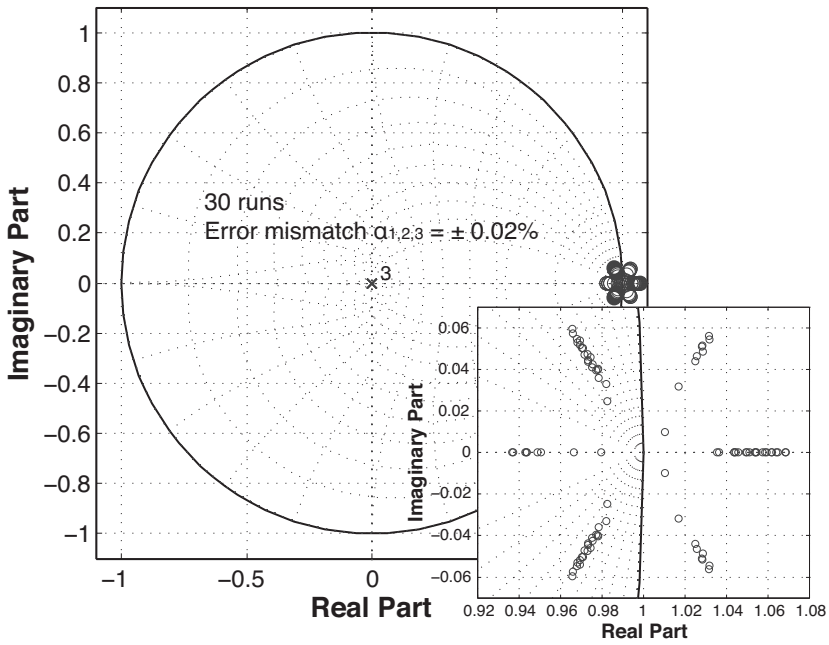

Figure 5.5: Capacitor mismatch effect on zeros placement in the structure of Fig. 5.3. The inset shows a zoom around z=1.

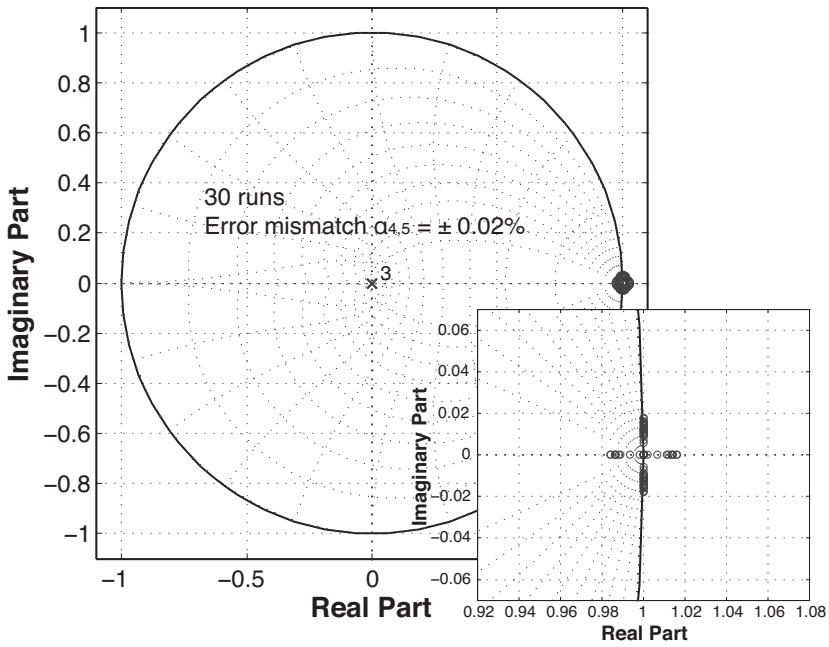

Figure 5.6: Capacitor mismatch effect on zeros placement in the structure of Fig. 5.4. The inset shows a zoom around z=1.

have beneficial complex zeros makes the scheme of Fig. 5.4 preferable.

A further montecarlo simulation, which considers an increased capacitors mismatch of ±0.2%, tests the mismatch sensitivity of the structures of Figg. 5.3 and 5.4 versus the expected ENOB. Fig. 5.7 shows the result with 200 runs. As expected, the architecture of Fig. 5.4 gives better results. The possibility to have complex conjugates zeros can even enhance the ideal resolution (14 bits), making this scheme preferable. Only this architecture is therefore considered hereinafter.

Fig. 5.8 shows the block diagram of the considered third-order solution in which analog and digital paths are highlighted. Fig. 5.9 depicts a possible switched capacitor implementation of the analog path around the second integrator together with the driving phases. The implementation of the analog path requires the use of only 3 capacitors. For sake of simplicity, Fig. 5.9 shows the single-ended solution.

5.3 Operational Amplifiers Swing Reduction

The reduction of the operational amplifiers output voltage swing further decreases the modulator power consumption. Indeed, output swing minimization leads not only to relaxed slew-rate request, but also ensures better performance in terms of harmonic distortion. In addition, it enables the use of lower supply voltages, thus allowing to implement single-stage op-amp architectures, such as telescopic cascode. The approach proposed in this project can belong to

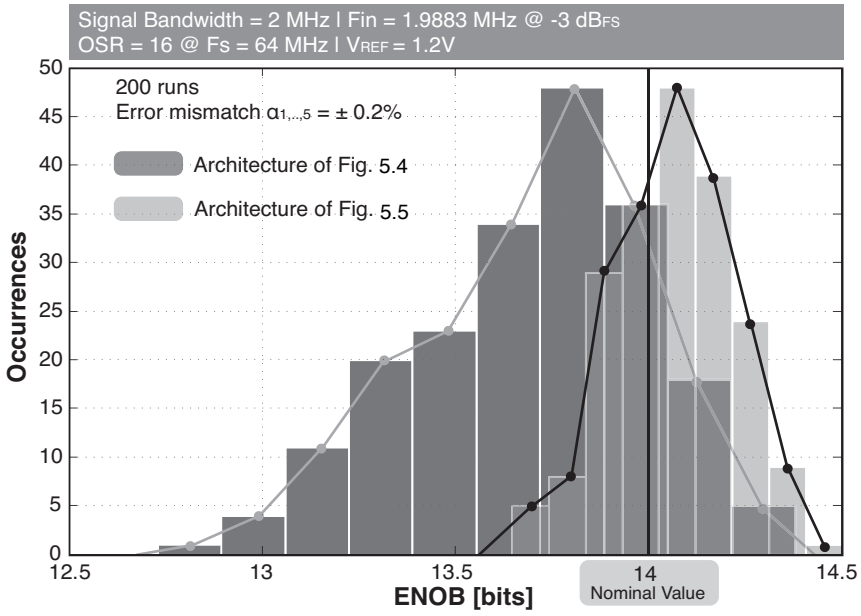

Figure 5.7: Capacitors mismatch effect on the resolutions.

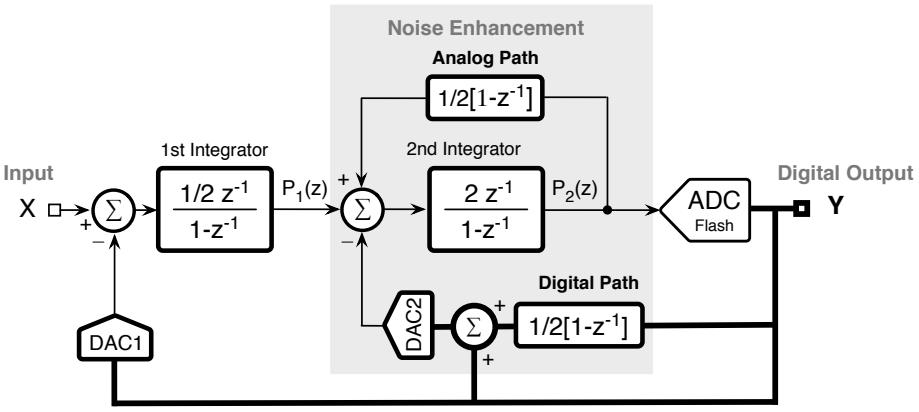

Figure 5.8: Third-order $\Sigma\Delta$ with detailed analog and digital paths.

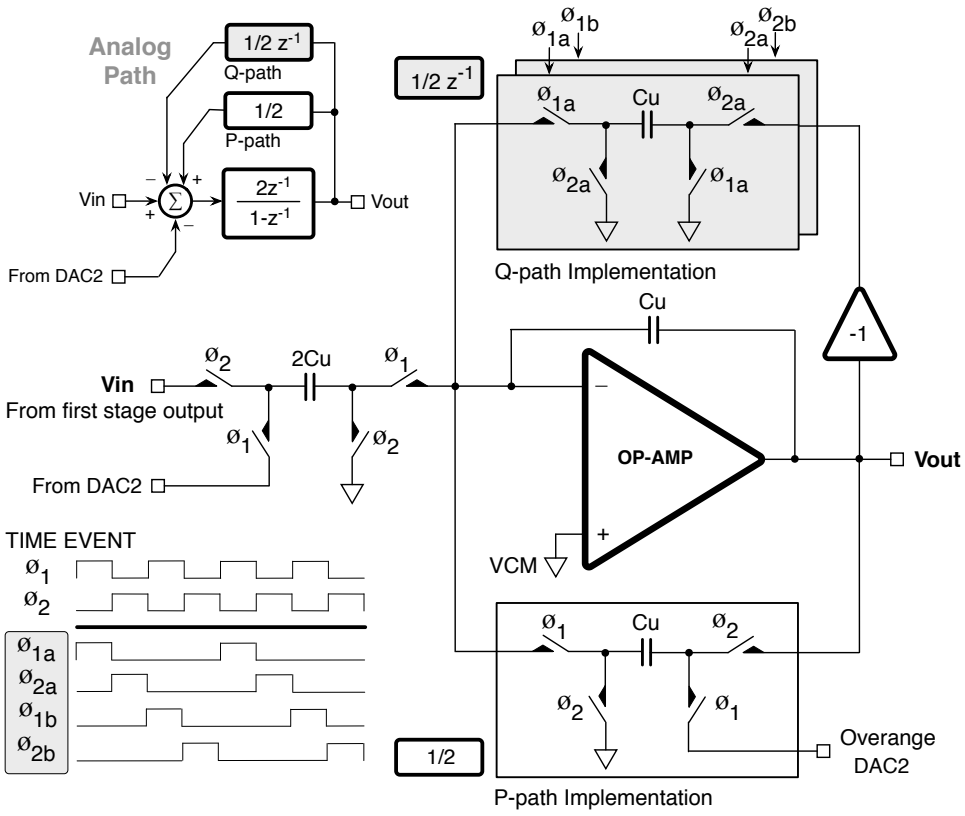

Figure 5.9: Switched capacitor implementation.

the family of digitally assisted analog technique (DAA) ([45], [51]), because uses an increased digital support for improving (or relax) the performance of the analog section, which is the critical point in deeper technology, like the case of used 65 nm CMOS technology.

The proposed approach grants the minimum swing of the output of both operational amplifiers by using a distributed digital feedforward paths without modifying the modulator STF and NTF. The cost of the method is an extra quantizer at the input of modulator.

The starting prototype is the noise shaping boosting architecture proposed in Fig. 5.4. The output is expressed by:

$$Y = X \cdot STF + \epsilon_q \cdot NTF = Xz^{-2} + \epsilon_q(1 - z^{-1})^3 \tag{5.9}$$

where ϵ_q is the quantization noise of the main quantizer. Note that the unity STF is only a two delay such as in a second order modulator, while the NTF is equivalent to the noise shaping behavior of a third order ΣΔ modulator. The output of the first integrator (Fig. 5.10(a)) is described by

$$P_1(z) = \frac{X}{2}z^{-1}(1 + z^{-1}) - \frac{\epsilon_q}{2}(1 - z^{-1})^2 = X \cdot H_1 - \frac{\epsilon_q}{2}(1 - z^{-1})^2 \tag{5.10}$$

where X is the input signal multiplied by the transfer function H_1. The main contribution to the swing of this node is due to the input, so in order to compensate its effect, it is possible to process its quantized version, indicated as $\overline{X}$. The quantization of the input signal $\overline{X}$ is equals to X+ϵ_{q1}, where ϵ_{q1} is the quantization noise of the added quantizer.

As shown in Fig. 5.10(b) the information doesn't change if the quantity $H_1\overline{X}$ is added and subtracted at the output $P_1(z)$. The term -$H_1\overline{X}$ is then shifted in front of the integrator dividing it by the integrator transfer function. The result as shown in Fig. 5.10(c), is an additional injection at the input of the first integrator equal to $H_2\overline{X}$, where H_2 is $(1 - z^{-2})$. However, the output $P_1(z)$ is given by:

$$P_1(z) = \frac{1}{2}z^{-1}[\epsilon_q(1 - z^{-1})^2 + \epsilon_{q1}(1 + z^{-1})] \tag{5.11}$$

The contribution of the output is dominated by quantization error ϵ_q shaped at second order, and auxiliary quantization error ϵ_{q1} multiplied by $(1+z^{-1})$. The use of multi-bit solution ensures low level swing. The procedure can be repeated also for the second integrator, which can be topologically rearranged, as illustrated in Fig. 5.11. The starting second delayed integrator of Fig. 5.11(a) is closed in feedback loop with the analog path $1/2(1 - z^{-1})$. The structure is equivalent to the block reported in Fig. 5.11(b) with transfer function equals to $2z^{-1}/(1-z^{-1})^2$. The output P_2 of the second integrator in the structure of Fig. 5.8 is:

$$P_2(z) = Xz^{-2} - \epsilon_q z^{-1}(3 - z^{-1})(1 - z^{-1}) = X \cdot H_3 - \epsilon_q z^{-1}(3 - 4z^{-1} + z^{-2}) \tag{5.12}$$

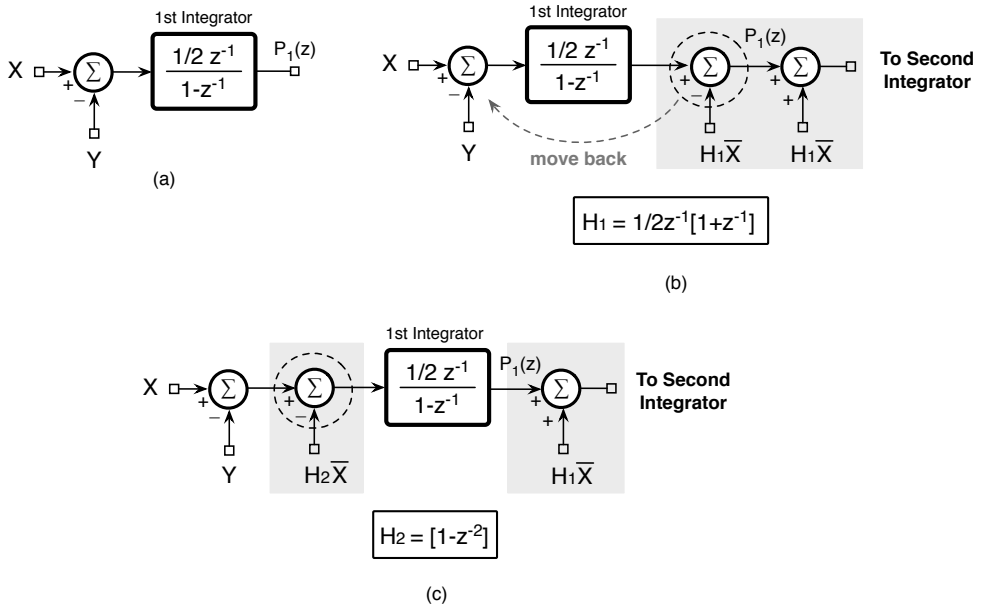

Figure 5.10: Block diagram of reduction swing technique applied to the first integrator.

The reduction of the swing of the second integrator, as reported for the case of the first one, is obtained by adding and subtracting the quantized version $\overline{X}$ of the input signal multiplied with the same transfer function of the main contribution of $P_2(z)$. The quantized input $\overline{X}$ is then multiplied with the transfer function H_3, and shifted in front of the equivalent second integrator, as illustrated in Fig. 5.12(b). The transfer function H_3 referred to the input of second integrator changes in H_4 (Fig. 5.12(c)) which is equal to $1/2z^{-1}(1-z^{-1})^2$. The reconstruction of the $P_2(z)$ due to the term $+H_3\overline{X}$ can be shifted in digital domain after the quantizer, as shown in Fig. 5.12(d). Fig. 5.13 shows the proposed structure with the additional switched ca-

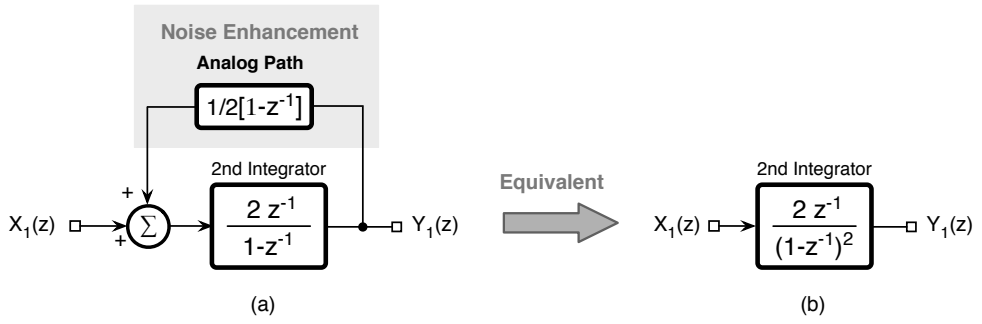

Figure 5.11: Second Integrator topology equivalence.

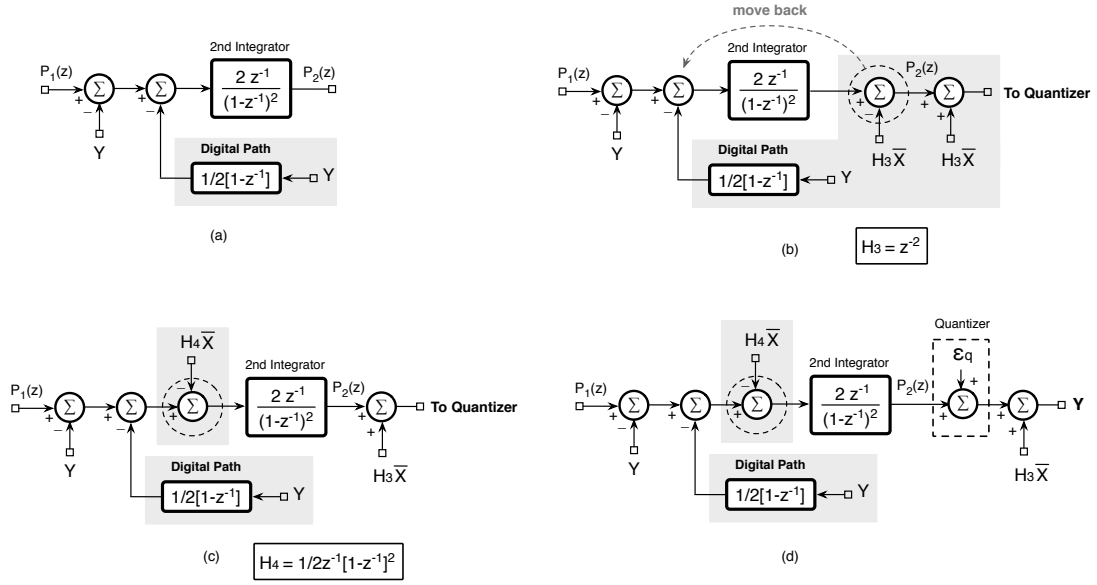

Figure 5.12: Block diagram of reduction swing technique applied to the second integrator.

pacitor paths that boosts the noise shaping behavior and all the distributed digital feedforward branches used to reduce the swing of the integrators. The methodology that allows to built the original STF and NTF directly after each integrator, requires the implementation of additional DACs that convert the digital quantized version of the input, filtered with the transfer function $H_1, H_2 and H_4$. Anyway the advantage to work in digital domain allows to simplify the architecture with properly topological modification, as illustrated in Fig. 5.14, where the digital paths

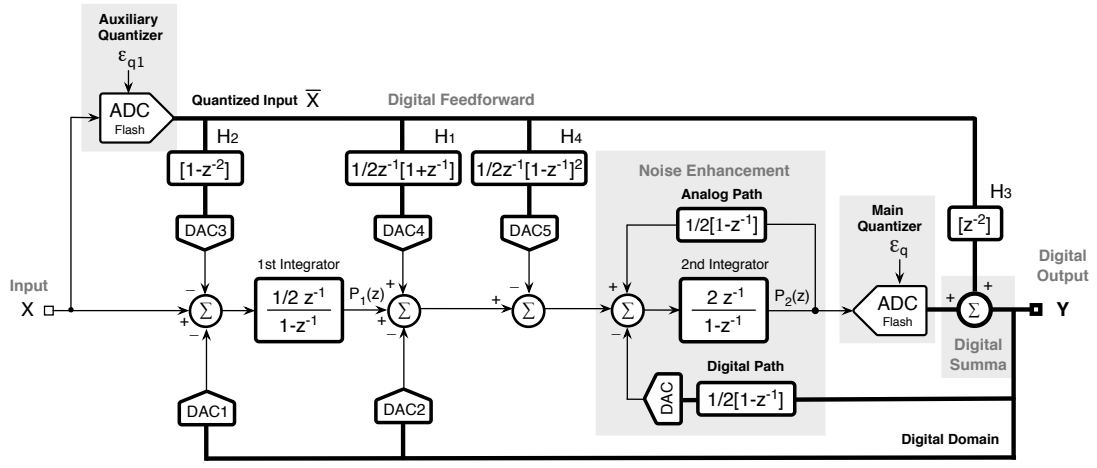

Figure 5.13: Complete third order ΣΔ architecture with all distributed digital feedforward branches

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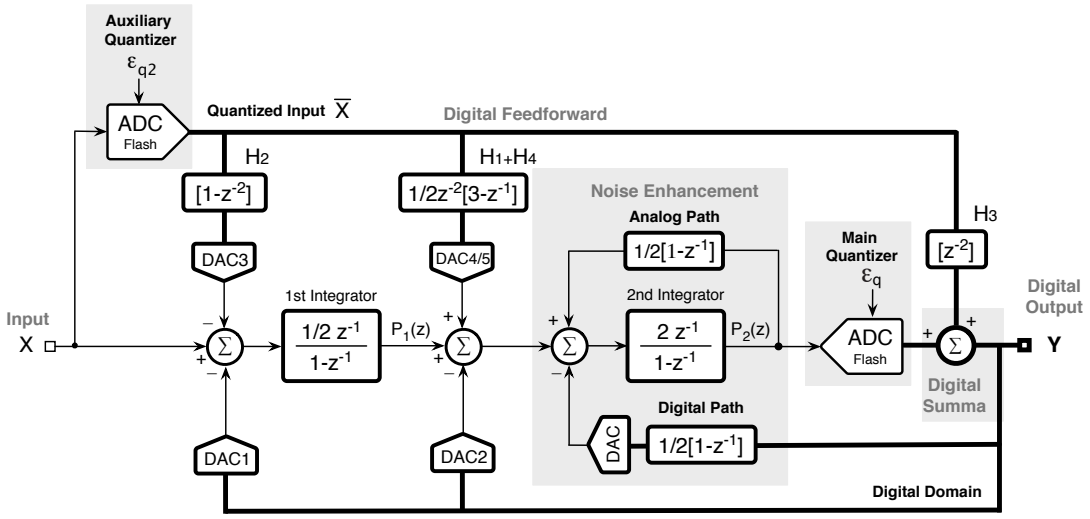

Figure 5.14: Topological modification: Digital processing combination of DAC4 and DAC5.

with transfer functions H_1, H_4 are merged together in a single path. Moreover, the feedback path that connects the modulator output to the first DAC1, is moved back to the output of the main quantizer because previously is subtracted with block H_2 at the input of the first quantizer and at the end summed with block H_3 at the output of the modulator (Fig. 5.15).

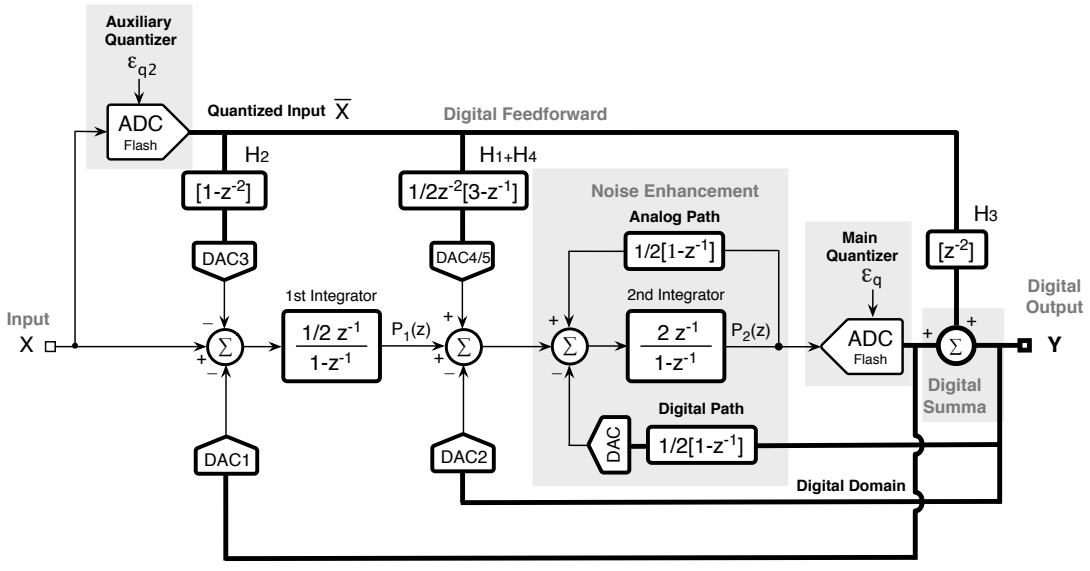

Figure 5.15: Topological modification: Moving the input of the DAC1 from output of the modulator to the output of main quantizer.

This movement is advantageous because thank to the reduced swing at the input of the main quantizer, also its output has a reduced number of levels, so that the required number of unity element of the DAC1 are limited with improvement in terms of linearity and consequently less harmonics distortion.

The final result is the third order ΣΔ architecture of Fig. 5.16. The gain by two of the second integrator is shifted inside the voltage reference of the main flash converter, in order to further reduce the swing of the second integrator at the cost of higher comparator sensitivity (Fig. 5.16). The gain of two translates in the halving of the voltage reference of the main converter and consequently the changing of the 1/2 feedback factor of the auxiliary analog path to unitary value. The reduction of the swing of both integrators to a very small dynamic comparable with the level of a quantization error, requires to use a 4 bit flash ADC for the auxiliary flash converter and 5 bit for the main flash converter, as the behavioral simulation will show in detailed in next section.

The trade-off between power consumption, area, number of DACs and complexity design imposes to implement DACs with shared Kelvin divider in order to increase the final power efficiency. In particular the 4 bit DACs ($DAC3$ and $DAC4/5$) share a single Kelvin divider which generates the needed 16 differential references voltages, while the 5 bit DACs (DAC,$DAC1$ and $DAC2$) uses a single Kelvin divider with 32 differential references voltages. The choice to generate differential levels allows to completely delete the error caused by gradient in the value of each resistors used in the resistive string. On the contrary, using resistive divider needs good matching accuracy, which could be obtained by increasing the dimension of each resistor and with very carefully layout. This allows to reduce the harmonic distortion and does not require

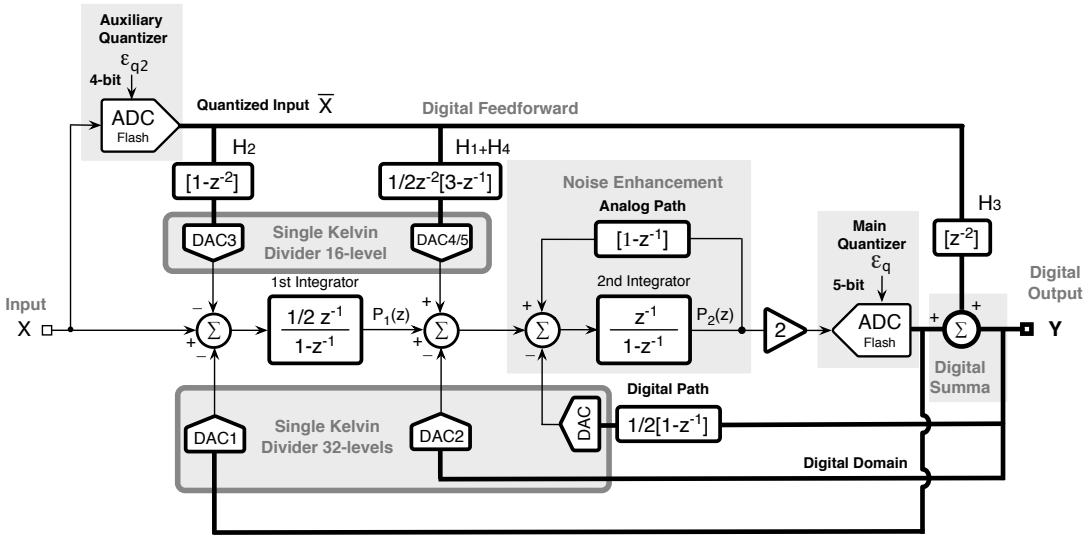

Figure 5.16: Proposed third-order DT ΣΔ modulator.

digital calibration or dynamic element matching (DEM) techniques.

5.3.1 Behavioral Simulation of the proposed third order ΣΔ architecture.

The effectiveness of the architecture proposed in Fig. 5.16 is proved with Matlab-Simulink^{TM} behavioral simulation by using the modeling of non-idealities (op-amp with finite GBW and limited slew-rate, KT/C noise) [52]. The simulation provide a comparison between the dynamic output swing with and without the digital assisted analog technique (DAA). The architecture is tested by applying an input sine wave of 2.18 MHz, which is close to the signal bandwidth limit of 2.2 MHz with an amplitude of -2 dB_{FS}. The oversampling ratio is 16 and consequently the sampling frequency is 70.4 MHz.

The best trade-off between swing reduction effectiveness, power consumption, resolution and complexity suggests to use 5 bit flash converter in the main quantizer and 4 bit flash converter for the auxiliary quantizer. The first integrator output swing goes down from ±0.504 V to ±0.065 V (respect to analog voltage, which is equal to the half of the supply voltage), which corresponds to a swing reduction of the 88%, as shown in Fig. 5.17. Therefore, for the second integrator, the benefit of the swing reduction is approximately 75%, from ±0.28 V to ±0.076 V, as shown in Fig. 5.18. Notice that for the second integrator, the originating swing without the DAA technique is already limited, due to the combination of the effects of the analog path used to boost the noise shaping and the shifting of the gain two inside the voltage reference of the main quantizer.

The reduction of the output swing of both integrators is significantly, as illustrated in Fig. 5.19, where the histogram of the outputs of integrators assumes a noise-like behavior typical of quantization error, thank to DAA technique, in contrast with the strong sinusoidal component obtained in the case of inactive DAA method.

Thank to the swing reduction at the output of second integrator, the number of quantization level and consequently, the number of comparators used in the main quantizer reduced from 31 to only 9. Thus, the implementation of the DAA technique requires performing the conversion of the input signal with an auxiliary quantizer, that at the maximum input voltage swing needs of 14 comparator. As a result, the performance is the same of the structure of Fig. 5.8 witch use only a single 5 bit flash converter in the loop, but thank to DAA method the total number of used comparator does not increase, but it is reduced from the original 31 to 23 (14+9) even if the structure of Fig. 5.16 use two different flash converters.

The penalty to pay is just an additional digital feed-forward circuitry and auxiliary DAC, but the combination of the noise enhancement and DAA techniques allow to fully compensate this limits thank to the relaxing requirement of dynamic range, slew-rate and linearity, that permit to implement single telescopic scheme with improvement in term of power efficiency and reduced harmonic distortion.

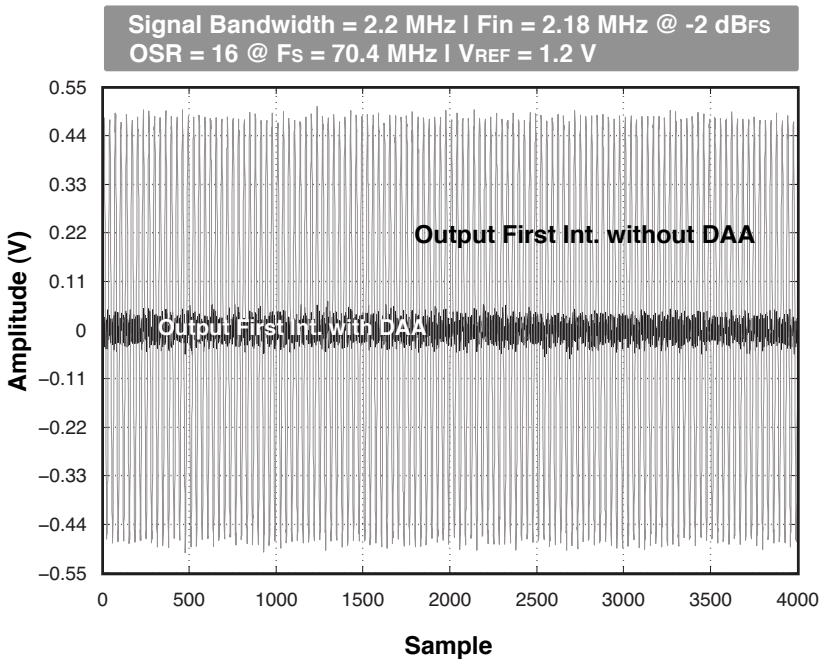

Figure 5.17: Output dynamic range of the first integrator with and without DAA technique.

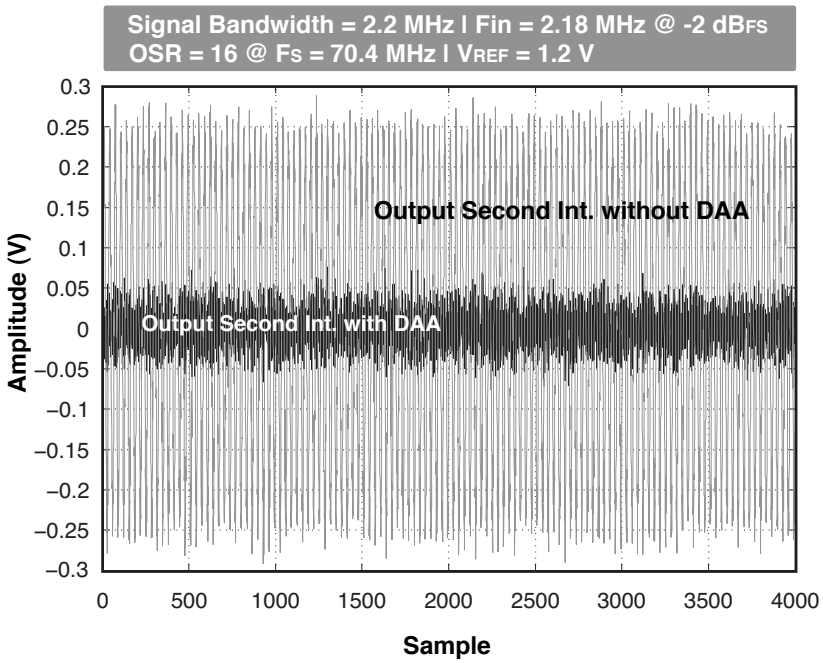

Figure 5.18: Output dynamic range of the second integrator with and without DAA technique.

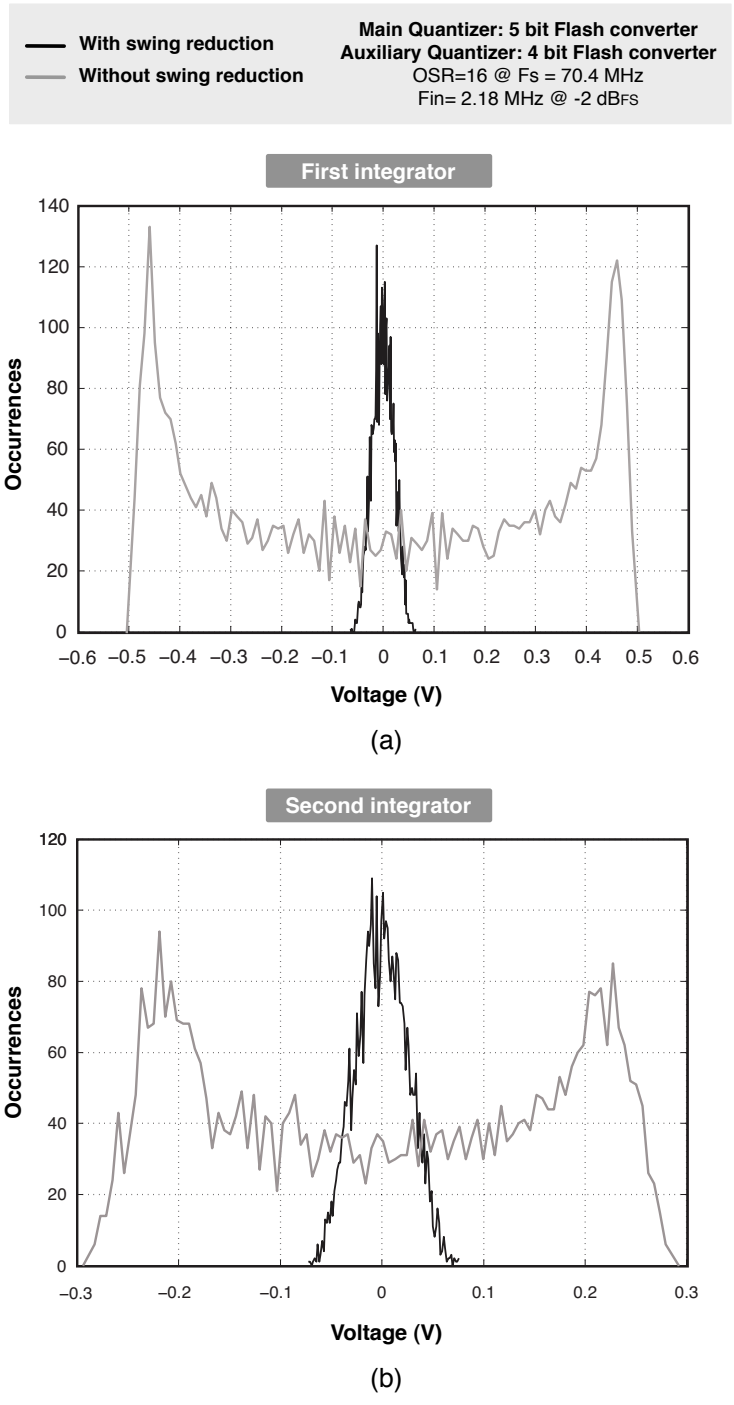

Figure 5.19: Noise-like swing dynamic: (a) First Integrator (b) Second Integrator.

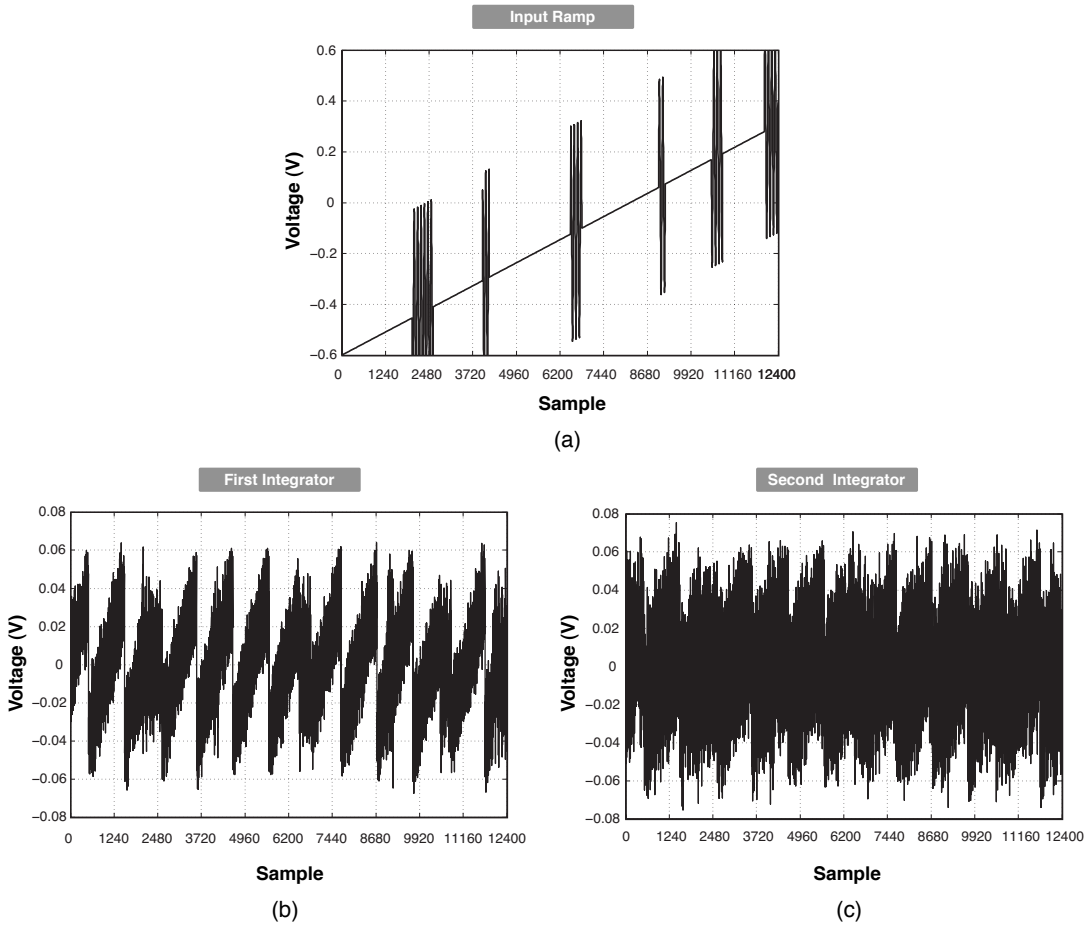

Figure 5.20: Stability in the proposed ΣΔ modulator: (a) input ramp with sinusoidal burst. (b) Output first integrator. (c) Output second integrator.

5.3.2 Stability Analysis

The study of stability in ΣΔ architecture is a must when the order of noise shaping behavior increases ([53],[54]). Structures with order L $\geq$ 3 are prone to instability. Stability problems occur when the internal nodes (such as input quantizer) are bounded to a fixed value permanently for many clock periods or start to oscillate at low frequency, leading to tones located in the signal band. In the literature have been proposed several stability criteria to study the behavior of the ΣΔ modulator with the increasing of the input amplitude. Anyway, a large amount of these methods, based on the definition of quantizer "gain", are not so effective and the best solution is using a more practical approach based on extensive time-domain simulations with different amplitudes and frequencies input sine wave.

Therefore, the stability of the proposed modulator was tested by time-domain simulations

using a slowly increasing input ramp with arbitrary multiple burst. As reported in Fig. 5.20, the DAA technique allows to increase the stability of the modulator because the injection of the quantized input reduces the swing of both integrators. The outputs of the integrators are always limited so that also the bursts at the input are not able to create oscillations or saturation of the internal nodes.

5.4 Circuit implementation of the ΣΔ Architecture.

The alleviate integrators output swing requirements allows to use single-stage telescopic operational amplifier, witch is the best power efficiency solution in terms of gain and bandwidth, but suffers of limited slew-rate. Anyway, the small swing allows to relax also the slew-rate requirement, making the telescopic scheme the best candidate. Moreover the solution ensures better linearity and consequently less harmonic distortion.

As explained in the previous sections, the proposed architecture realized a third order noise shaping behavior with only two operational amplifier thank to an auxiliary switched capacitor network closed in feedback with the second integrator (indicated as analog and digital path), that boosts the order of the noise shaping. Fig. 5.21 illustrates the fully differential switched capacitor implementation of the structure and the phases scheme used to control the switches.

For limiting the KT/C noise in order to obtain the resolution of 14 bit, the value of Cu capacitor connected to the first integrator is equal to 800 fF, while for the capacitors connected to the second integrators the value is less (160 fF), because all the errors injected at the input of the second integrator are noise shaped. This also helps to reduce the capacitor load of the second operational amplifier. The choice to use telescopic stage for the operational amplifiers introduce one constraint related to the necessity to use different common mode voltage between the input ($V_{CMIN} = 0.5$ V) and output ($V_{CMOUT} = 0.65$ V). Moreover, all capacitor are realized with MOM (metal-oxide-metal) structures which offer an intrinsic high linearity and accuracy which are necessary for high performance ΣΔ architecture.

The phase diagram shows that the duration of the two phases is not equally distributed, but Φ_1 lasts for the 75% of the clock period in order to guarantee sufficient time for the settling of the integrated charge. The Φ_2 is shorter than the one used for the injection, because the passive charging is faster than the virtual ground injection being only limited by the on resistance of the switches and by equivalence resistance of the kelvin divider.

The switched capacitors network connected to the second integrator realize the different transfer functions of the noise shaping boosting and of all digital feedforward paths. The single delay is realized with two switched capacitor structure operating in a ping-pong fashion thank to the controlling phases ϕ_{1a} and ϕ_{1b} (or ϕ_{2a} and ϕ_{2b}). Thus, the different coefficients are simply realized with capacitor ratio, so it is sufficient to size correctly the feedback capacitors, as depicted in Fig. 5.21. The digital data at the input of the DAC4/5 is previously double delayed in digital domain with a cascade of two class D flip-flop.

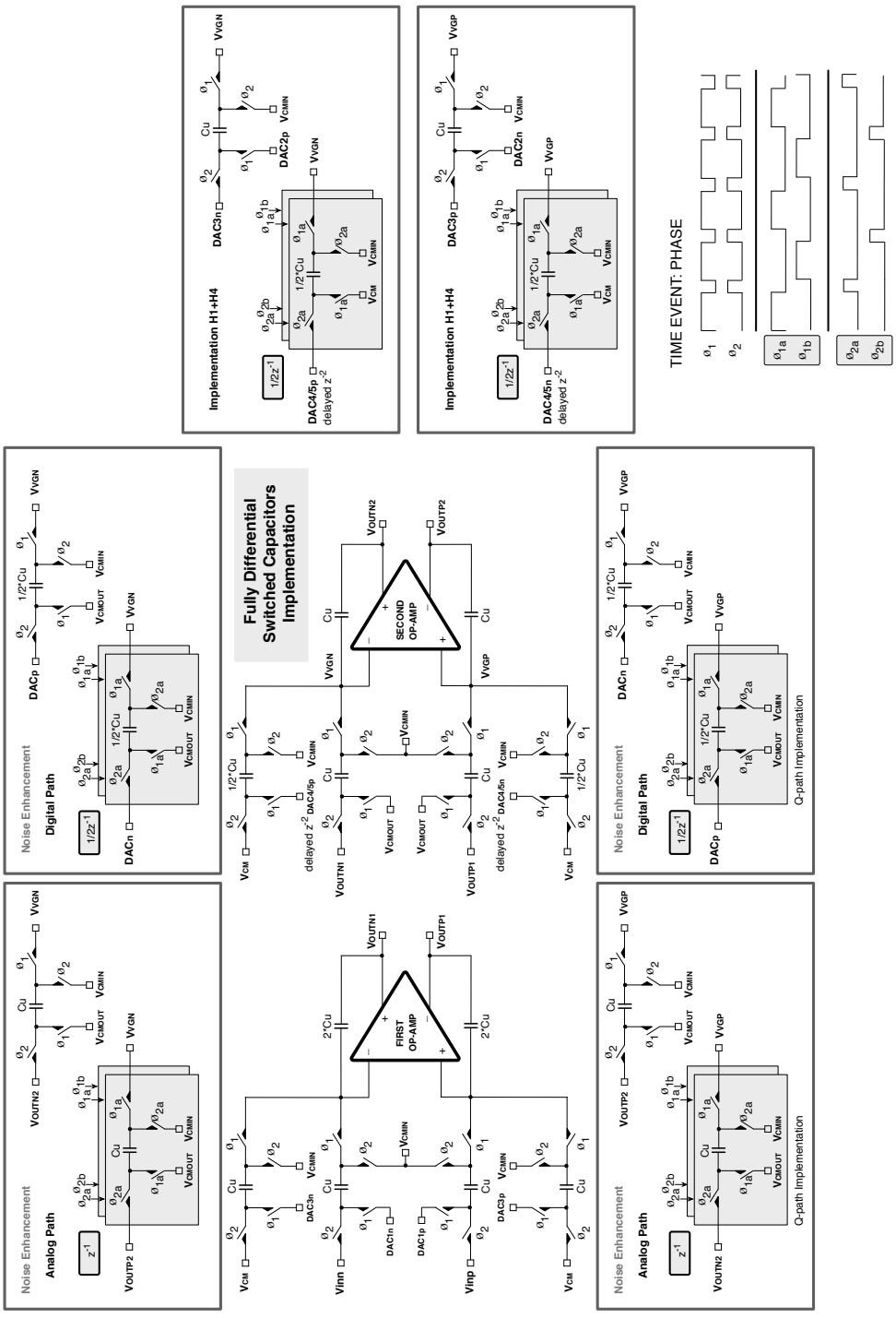

Figure 5.21: Fully differential switched capacitor implementation of the modulator.

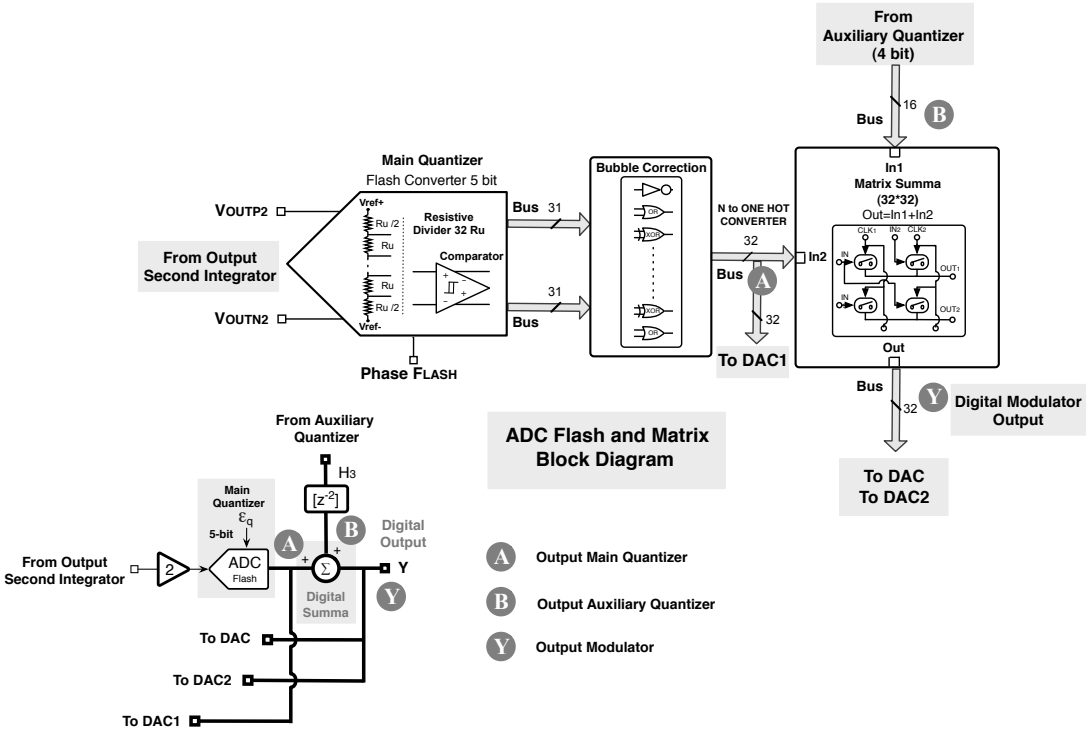

Figure 5.22: Block diagram of the main quantizer and digital processing.

The differential output of the second integrator is than processed by the main flash converter as shown in more detailed in Fig. 5.22. The main quantizer uses only 9 comparators thank to the swing reduction of the second integrator. Anyway the structure implements all the 31 comparator in order to avoids settling problems at the start-up: after the settling of the internal nodes all the useless comparators are completely turned off. The thermometric code generated by the main flash is simultaneously converted to one-out-of-N code and corrected of possible bubble errors ([55], [56]) by a digital circuit, named bubble correction, realized with simple logic gates. The same circuits is also used after the auxiliary quantizer properly resized for the case of 4-bit flash converter.

The digital bus (indicated with the digit A) drives the switches, that select the needed reference voltages of the Kelvin divider of DAC1 and one input of the matrix array, used to realized the digital sum at the output of the modulator. The second digital bus (indicated with the digit B) injected at the second input of the matrix is the double delayed (with H_3) quantized version of the input voltage, realized by the 4-bit auxiliary flash converter at the input of the modulator.

The operation of addition is realized in digital domain without the use of digital logic gates, but using an array of 32×32 switches, implemented with a simple NMOS transistor, as reported

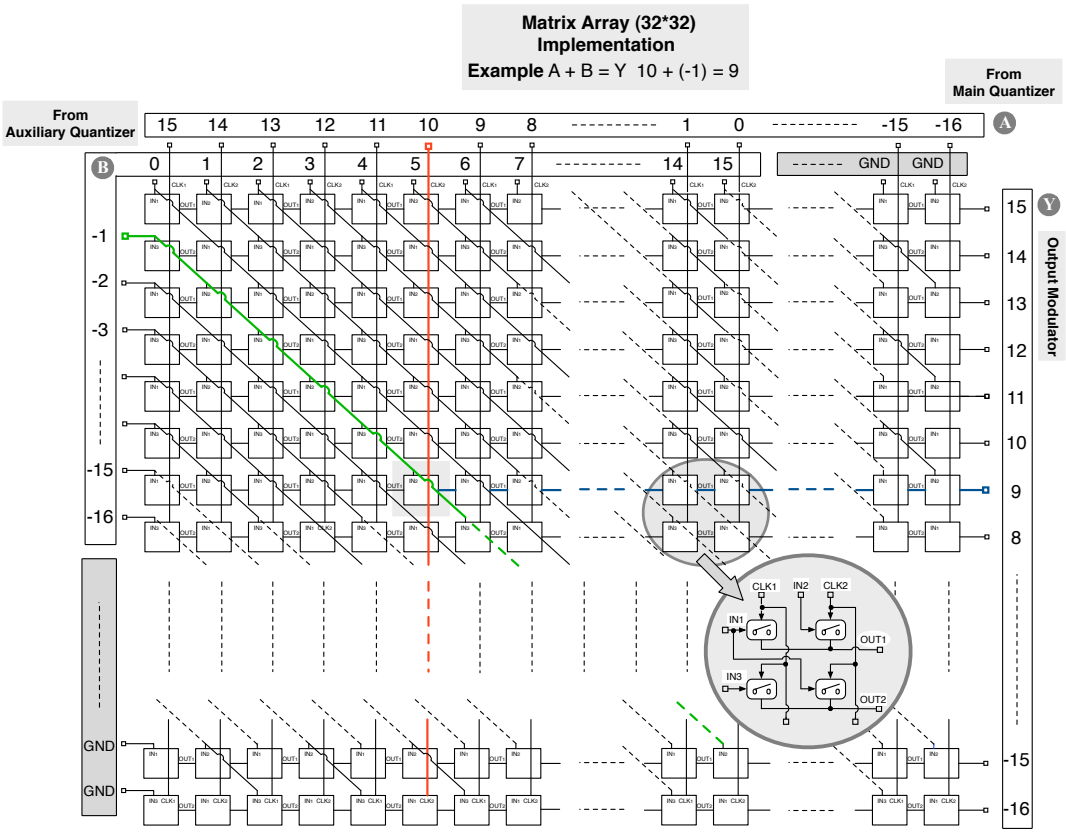

Figure 5.23: Schematic implementation of the matrix array.

in Fig. 5.23. The operating principle is very simple: the input bus A encoded in one-out-of-N code with 32 level has only one active bit for each data, so it is able to select only one possible column (from circuit point of view set the voltage gate of all the switches of the column to the supply voltage), while in turn, the input bus B selecting only one row, allowing to define a single switch and consequently only one output. In other words, providing an appropriate placing for the data of the inputs bus it possible to select only one output, which correspond to the logic sum of the encoded data applied at the inputs. Notice that the input bus B has only 16 levels, so it is sufficient to connect alternately 16 of the 32 available input switches. For each input Fig. 5.23 shows the equivalent decimal coding of the data expressed in the one-out-of-N code. The code of both inputs and output is represented in decimal range from -16 to 15. Fig. 5.23 illustrates an example of addition operation between the data 10 (from A in red) and -1 (from B in green). The output result is 9, as highlighted in blue.

Thus, the matrix ensure intrinsic speed and benefits in terms of power consumption, but adds the penalty of increased area and complexity layout, even if it is composed of modular blocks. The result of the summing matrix represents the digital output code of the modulator,

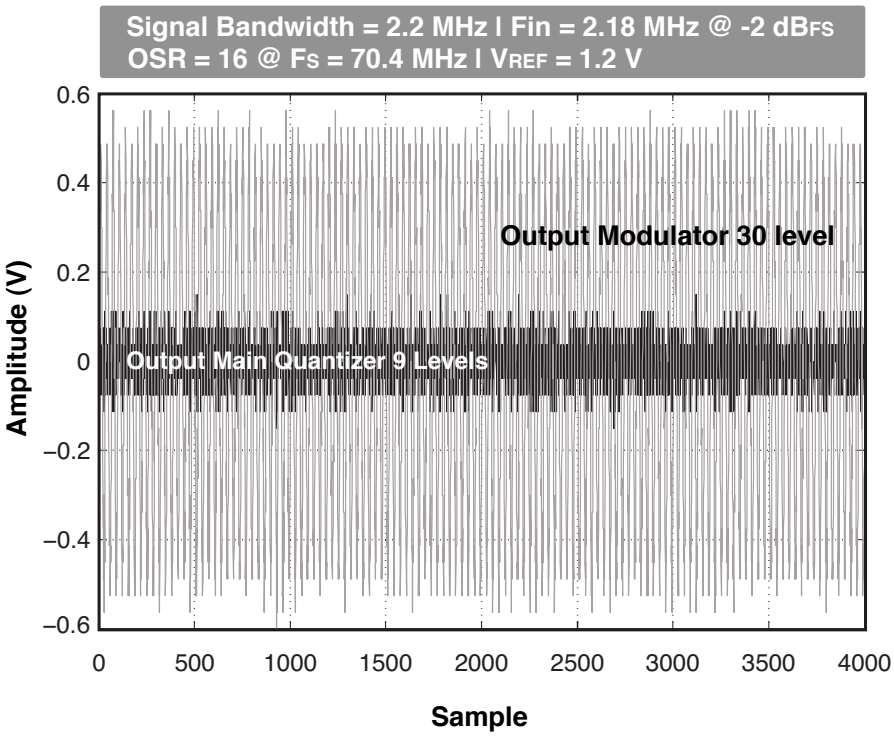

Figure 5.24: Swing comparison between the output of the main quantizer and the output of the modulator.

used to control the selection of the reference of DAC and DAC2. Fig. 5.24 shows the comparison between the swing of the output of the main quantizer and the output of the modulator.

The need to use a large number of DACs makes difficult to implement switched capacitor solution, because the high resolution target, imposes to use high value for unity capacitor element in order to meet KT/C noise limit and demands for calibration or DEM techniques. The uses of large capacitances involve more power consumption, while calibration techniques require more area and complexity. This design adopts the string resistive DAC scheme, that on the contrary presents the problem of the matching. Anyway, this limits could be resolved enlarging the unity value of the resistance, without affecting the final power consumption. Moreover, the processing of differential voltages generate with the same resistive string allows to cancels the gradient error, at least at first order. To prove this feature, suppose that the generic i-th resistor R_i is subjected to a linear gradient δ_R (due to process and temperature variation); the corrected value is $R_i = R_{unit} + \mathrm{i}\delta_R$. The differential voltage between symmetric voltage references, results to be independent from δ_R, as expressed below ([48], [49]):

$$V_{differential} = V_{ref} \frac{(N-i)R_i + \delta_R(N-i)(N-i+1) - iR_i + \delta_R i(i+1)}{NR_i + \delta_R N(N+1)} \tag{5.13}$$

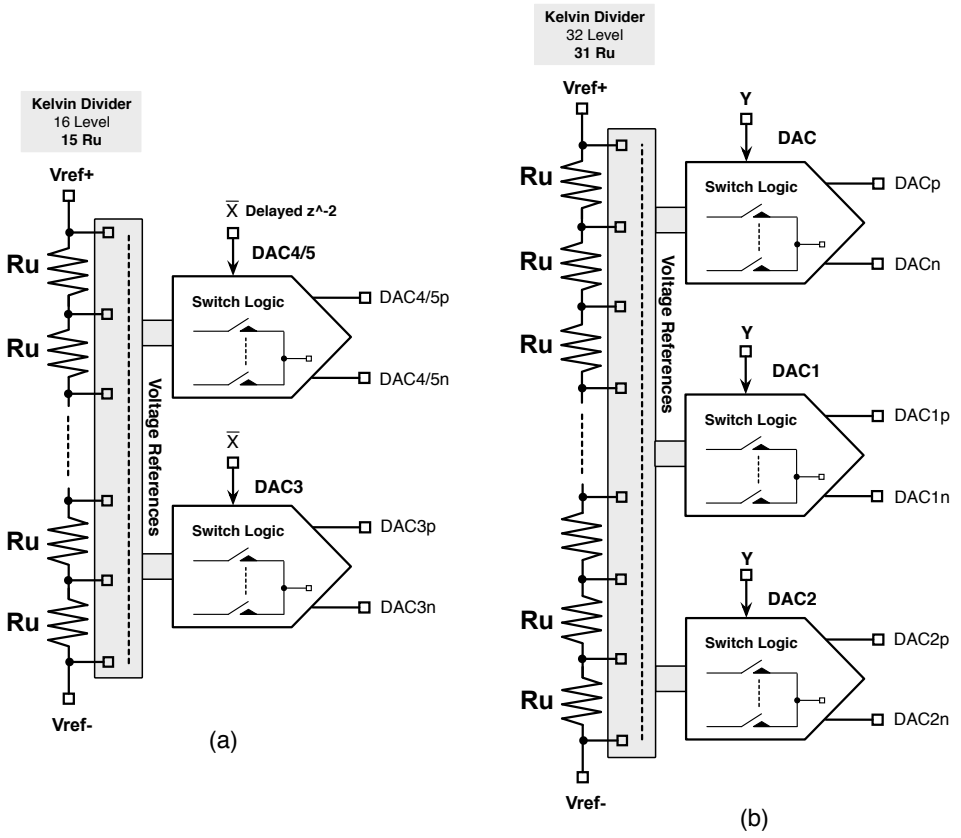

Figure 5.25: Block diagram of the string resistor implementation: (a) Case 4-bit (b) Case 5-bit.

Fig. 5.25 shows the block diagram of the DACs implemented in the architecture. The reference voltage for both DACs are fixed between $V_{ref}+$ and -V_{ref}, which conventionally correspond to the supply voltage (V_{DD}) and analog ground (V_{SS}). In the case of Fig. 5.25(a) the value of $V_{ref}+$ must by reduced of LSB/2 ($V_{DD}/16$) in order to guarantee consistency in the digital summa between a two data with different full scale value. Indeed, for Fig. 5.25(b), the shift of gain two of the second integrator imposes to halve the nominal voltage reference around the output common mode of the second operational amplifier. The digital selection of the differential voltages at the output is realized with the one-out-of-N data received at the input. The 5-bit resistor string used for DAC, DAC1 and DAC2, is realized with 31 poly resistance of 100 Ω, while the 4-bit version (DAC3 and DAC4/5) implements 15 poly resistance of 200 Ω, in order to maintain the same power consumption. The expected matching between unitary resistance is around 0.1%, leading to harmonic distortion of more than 85 dB without any digital calibration or DEM technique.

5.4.1 Operational amplifier scheme

The alleviate operational amplifier output swing requirements allow to use single-stage conventional telescopic scheme reported in Fig. 5.26. The use of 65 nm technology with intrinsic low gain imposes the adoption of the gain boosting technique in order to enhance the final gain as shown in Fig. 5.27. The high gain and low output swing imposes to use a continuous-time common mode feedback, that control the current in the branches by using two transistors in triode region on the p-side of all stages, as explain in [12]. The auxiliary amplifiers (op-amp1 and op-amp2) are folded cascode schemes with complementary configuration. The third branch of the input stage, that is biased with the voltage V_X or V_Y, determines the voltage of the source of $M_{35} - M_{36}$ and $M_{33} - M_{34}$ respectively. Notice that in order to avoid stability problems, the additional stages must not be fast than the unity frequency of final operational amplifier, as explained in [57]. The use of telescopic stage ensures intrinsic stability (the system has only

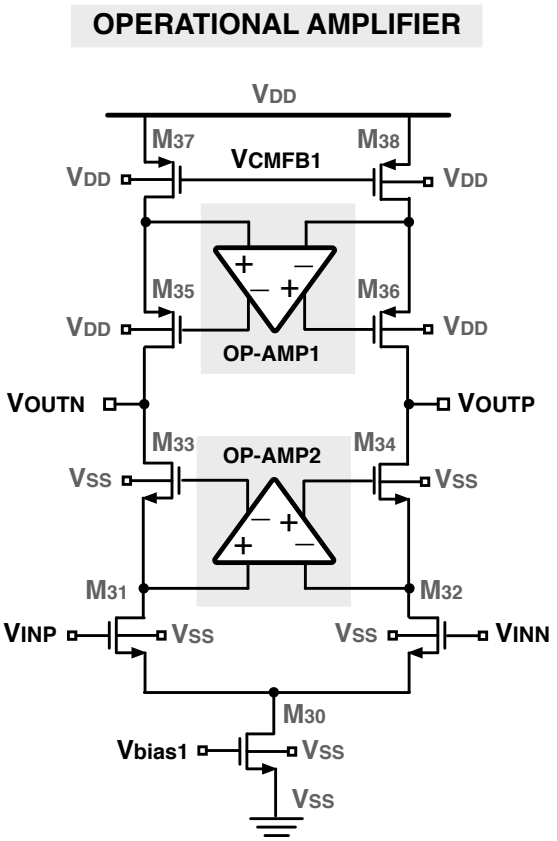

Figure 5.26: Gain boosted telescopic operational amplifier.

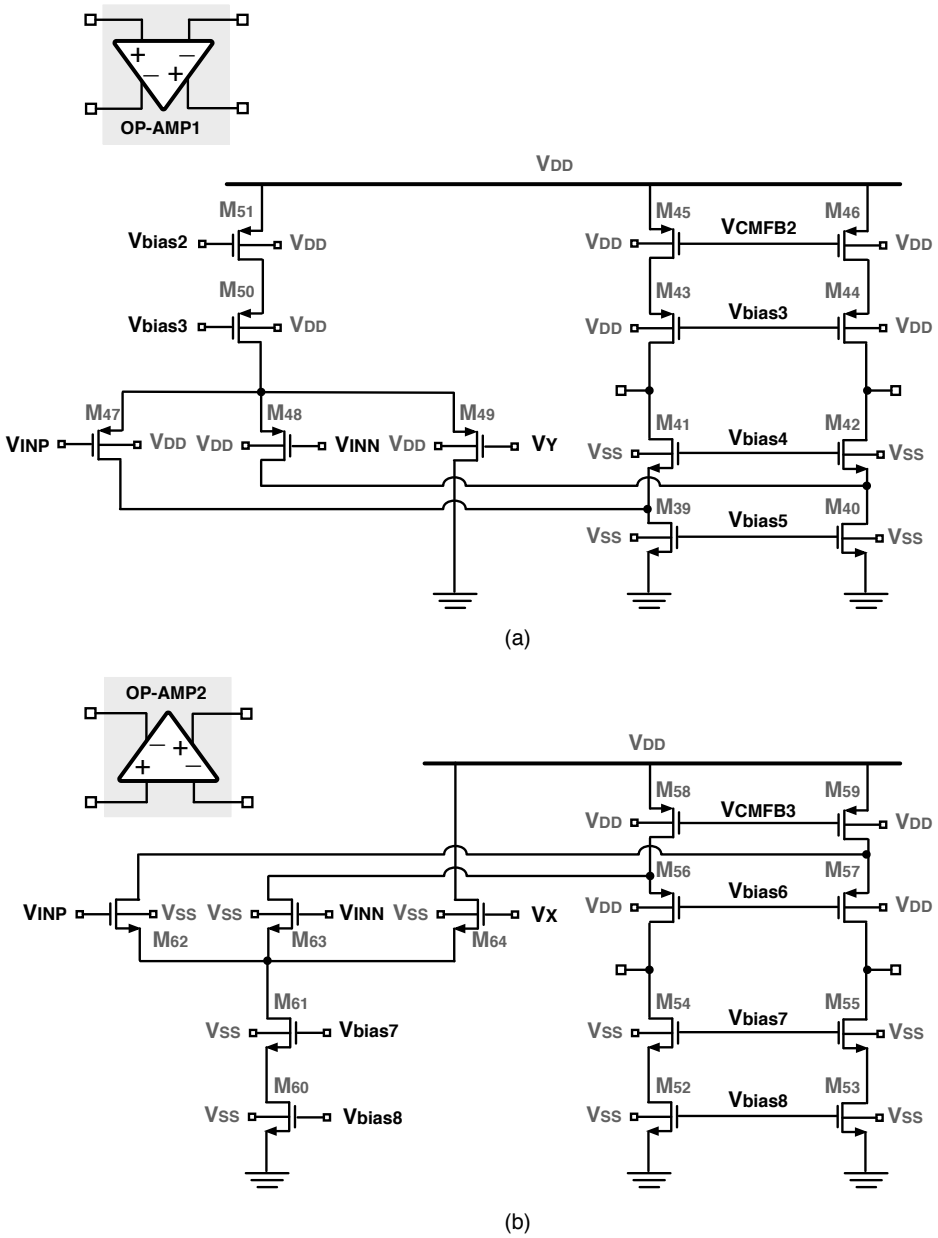

Figure 5.27: Auxiliary operational telescopic stages: (a) P-side. (b) N-side.

one dominant pole), power efficiency but reduced slew-rate, which is not a real problem due to the reduced output swing.

The input common mode voltage is 0.5 V, while the output common mode voltage is 0.65 V. The bias current of the auxiliary amplifiers is 13 μA. Simulation at transistor level, ensures

Parameter	First telescopic stage	Second telescopic stage
Bias Current	250 μA	280 μA
DC Gain (with gain boost)	94 dB	90 dB
Unit Frequency (C_{LOAD}=1.2 pF)	240 MHz	270MHz

Table 5.2: Performance of the telescopic stages

that the gain of the telescopic stage is always $\geqslant$ of 78 dB for all the output swing range of $\pm$ 65 mV around the output common mode voltage. The op-amps use the same scheme with different bias currents to meet the DC gain, slew-rate and bandwidth requirements as summarized in Table 5.3.

5.4.2 Comparator scheme

The design of comparator especially for flash ADC, is affected by the kickback noise [58], which disturbing the input voltage, introduces errors in the conversion from analog to digital domain. The disturb is related with the large variation of the regenerative nodes, that are coupled back to the input of comparator, through the parasitic capacitances of the transistors. The stage placed before the comparator has not a zero output impedance, so the coupling back creates disturbance on the input voltage. The problem is esacherbates in this architecture where the high gain of the telescopic stage associated with the noise-like swing of the output of the second operational amplifier, impose to have a very small kickback noise. The new proposed architecture of comparator isolates the preamplifier stage (Fig. 5.28) from the regeneration

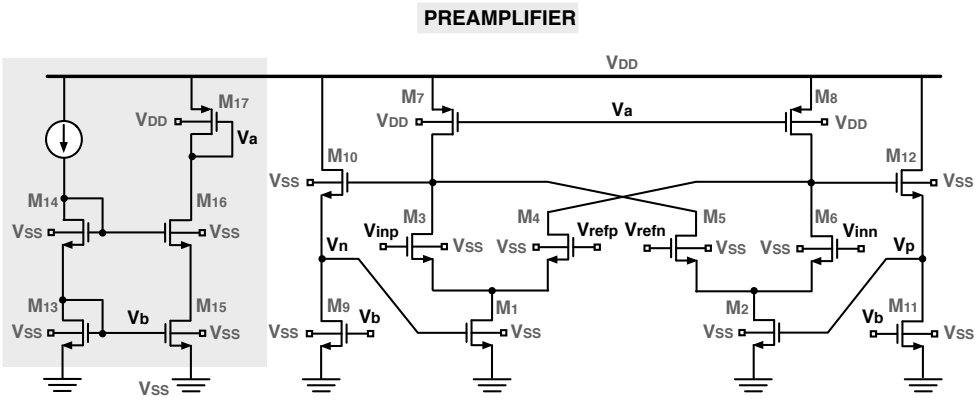

Figure 5.28: Schematic diagram of the preamplifier stage of the comparator.

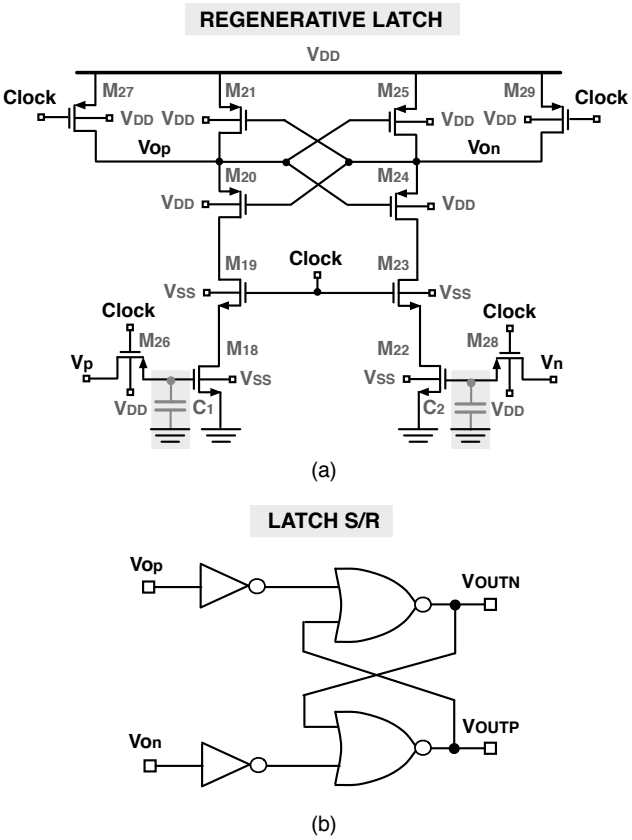

Figure 5.29: Schematic diagram of the regenerative latch and of the S-R latch.

nodes using switches (Fig. 5.29), which are opened during the regeneration phase (C_{LOCK} high). In the reset phase (C_{LOCK} low), the preamplifier stage uses a 2 NMOS input differential pairs to amplifies the unbalance between the input voltages and the different references. The unbalanced voltage on the active load is than shifted of one V_{GS} to the gate of bias generator (M_1 and M_2) through two source follower stages (M_{10} and M_{12} respectively). This configuration helps to limit the voltage swing of the drain of the input differential pairs. The p-type switches M_{26} and M_{28} are close and allow to charge the parasitics capacitance C_1 and C_2 to the voltages V_n and V_p.

When the C_{LOCK} goes high, immediately the switches to the output latch are opened and the output latch is started. This latch has a very small regenerative time constant due to presence of two back to back CMOS inverters that regenerate the output voltage presents at the gate of M_{18} and M_{22} to full scale digital levels. The set-rest latch allow to memorize the digital data for the entire clock period.

The comparator is designed to have, in the reset phase, an output voltage that is interpreted as the high logic value, due to presence of the transistors M_{27} and M_{29}. The overall current consumption is 12 μA, distributed in this way: each input differential pair draws 5 μA , while the branch with the source follower stage requires 1 μA. The sensitivity of the comparator is equal to 1 mV, while the time to conversion is only 200 ps.

The reference of both flash ADCs are generated by a resistive strings consuming 50 μW.

5.4.3 Switch Design with low voltage supply

The design of MOS switch in analog sampled data systems (ΣΔ modulator, switched capacitor circuits, filters,...) operating at low supply voltages becomes a difficult task. In general, the on-resistance of a conventional switch realized with a pair of complementary transistor, is proportional to:

$$R_{ON} \propto \frac{L}{W \cdot (V_{GS} - V_{TH})} \propto \frac{L}{W \cdot V_{OV}} \tag{5.14}$$

The reduction of the overdrive voltage V_{OV} of a transistor gives rise to a large variations of

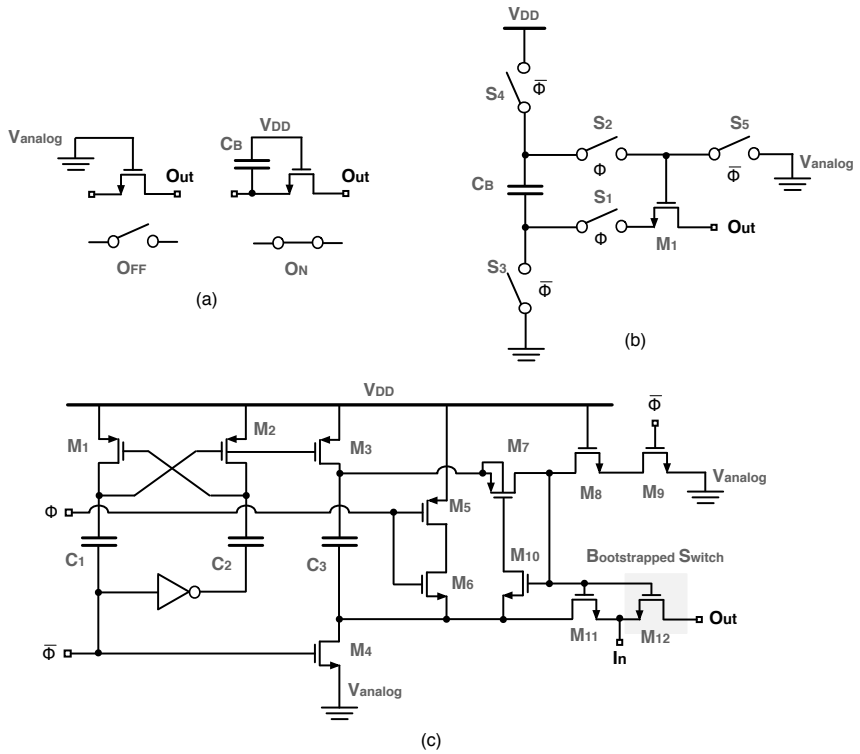

Figure 5.30: Bootstrapped Switch: (a) Conceptual scheme. (b) Basic implementation. (c) Circuit realization.

the on-resistance, that results to be signal dependent. This changing in settling behavior, leads to distortion in output spectrum. Thus, this effect at first approximation can be compensated with the design of large devices, but this adds significant parasitic capacitance that lowering the final speed. In general, the design of a full signal transmission switch, with low and acceptable resistance, can be done or by increasing the gate voltage or with the reduction of the threshold voltage. The former solution uses the conventional bootstrapped switch structure, while the second solution requires further technological steps that allow to have different transistor with high and low threshold voltage V_{TH}. Fig. 5.30(a) illustrates the basic conceptual scheme of the booststrapped technique [12]. The basic idea is that, when the switch is turned on (phase ϕ close in Fig. 5.30(b)), the gate voltage equals its source voltage increased of V_{DD}, guaranteeing a constant overdrive voltage and as a consequence a fixed on-resistance. This is obtained with an auxiliary capacitance C_B (precharged at V_{DD} during the off state) connected between source and gate when the transistor has to be turned on. Fig. 5.30(c) shows the most popular circuit implementation, which results to be complex in terms of area, power consumption and reliability

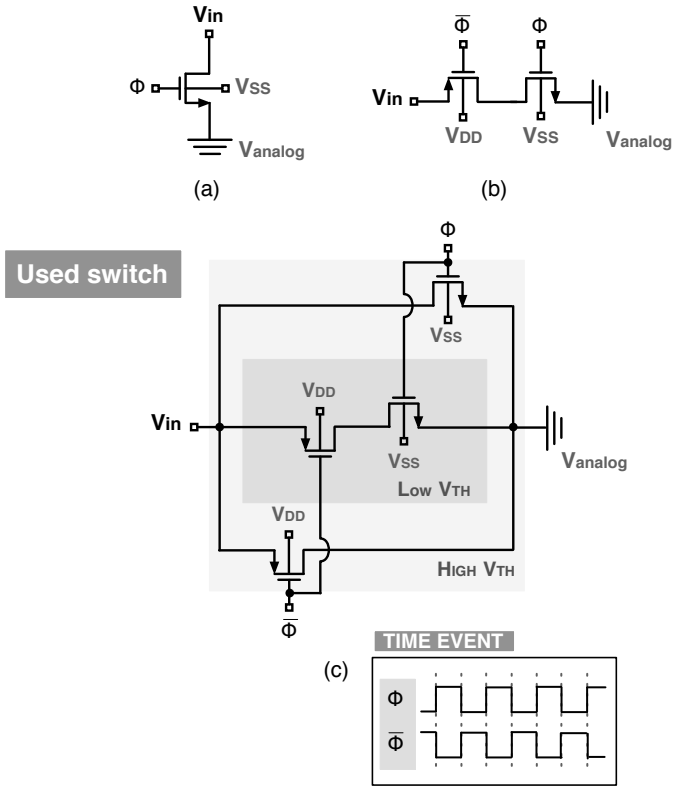

Figure 5.31: Reduction of leakage current in switch design : (a) Simple n-type switch. (b) Series transmission gate. (c) Full swing composite switch.

issues. A novel symmetrical bootstrapped switch circuit design is presented in [4]. It is based on a dynamic comparator that distinguishes which side of the switch must be used to boost the gate voltage in order to ensure reliability. Anyway, the structure increases the complexity of the design and the final power consumption.

The adoption of scaled technology poses another big problem in switched capacitor circuits due to the effect of subthreshold leakage off-currents, that change the charge across capacitors, leading to nonlinear error and consequently distortion, as explained in [59]. A first approach that permits to reduce the influence of these leakage current is the reduction of the signal swing on both side of the switch. In this case the reduction of the subthreshold leakage off-current is proportional to the ratio between the swing reduction and the subthreshold swing.

Consider the simple turned off (ϕ is low) n-type switch reported in Fig. 5.31(a). For the drain voltage V_{in} close to V_{DD} the leakage current is low, but it increases exponentially when V_{in} reaches the V_{SS}. A very low leakage switch is obtained using the series transmission gate switch proposed in Fig. 5.31(b). At first approximation, during off state, the inverse polarity of the leakage currents helps to partial compensation between the two terms, as explained in [59]. However, the transmission gate scheme suffers of limited input signal swing. Another interesting solution is proposed in Fig. 5.31(c) that ensures rail to rail operation. The scheme requires the use of transistor with low and high threshold voltage. In particular it is a composite switch, where a two high V_{TH} complementary transistor are used in parallel with a series transmission gate. The high gate ensures good conduction when the input signal V_{in} is close to the rails, while at middle rail series transmission gate conducts well. The implementation demands for multi-threshold process, but the solution is very promising in terms of leakage current reduction and it is also very simple without any problem related with reliability issues.

5.5 Simulation and Transistor Results.

The proposed architecture of third-order $\Sigma\Delta$ modulator has been fully simulated at transistor level by using a 65 nm CMOS technology. The nominal supply voltage is 1.2 V. A completely fully differential structure is chosen in order to minimize supplies and substrate noise injection and reducing distortion due to even-order harmonics.

Fig. 5.32 shows the simulated power spectral density of the modulator. The input signal is at -2 dBFS and its frequency is 2.18 MHz, closest to the Nyquist limit of 2.2 MHz. Considering an oversampling ratio of 16, the simulated modulator achieves a signal to noise ratio (SNR) of 85.9 dB (13.98 bits) over a signal bandwidth of 2.2 MHz.

Fig. 5.33 shows the measured power spectrum with a 326 kHz input signal at -2 dBFS. The accomplished SNDR is 83.27 dB, corresponding to an effective number of bits equal to 13.54. Third and fifth harmonic distortion tones are at -94 dBFS and -100 dBFS, respectively.

Fig. 5.34 compares the simulated performance of the proposed architecture with other state of the art ADCs converters presented in the last years. The structure is promising compared

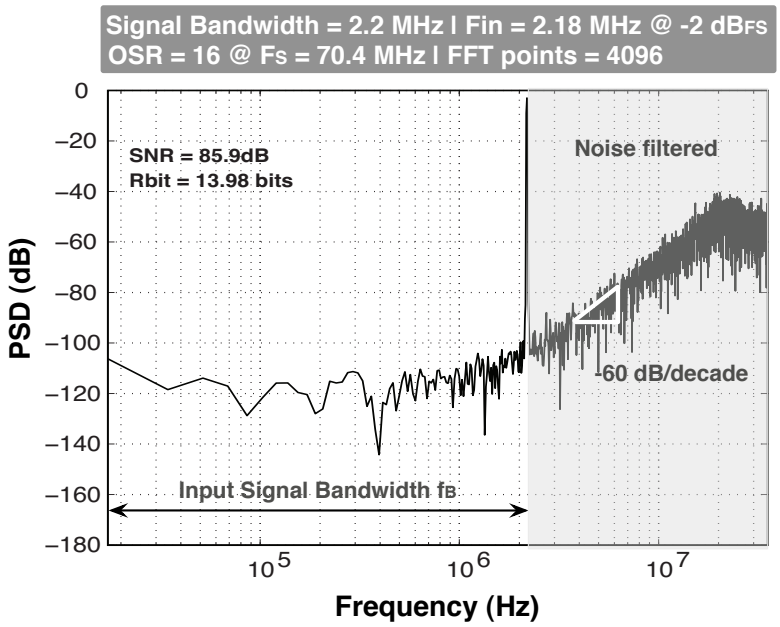

Figure 5.32: Simulated SNR of the proposed third order DT ΣΔ modulator.

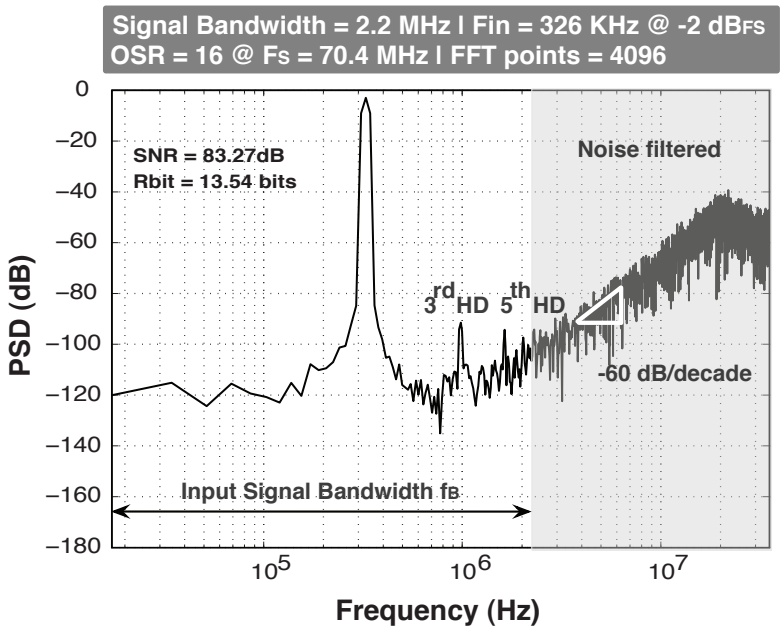

Figure 5.33: Simulated SNDR of the proposed third order DT ΣΔ modulator.

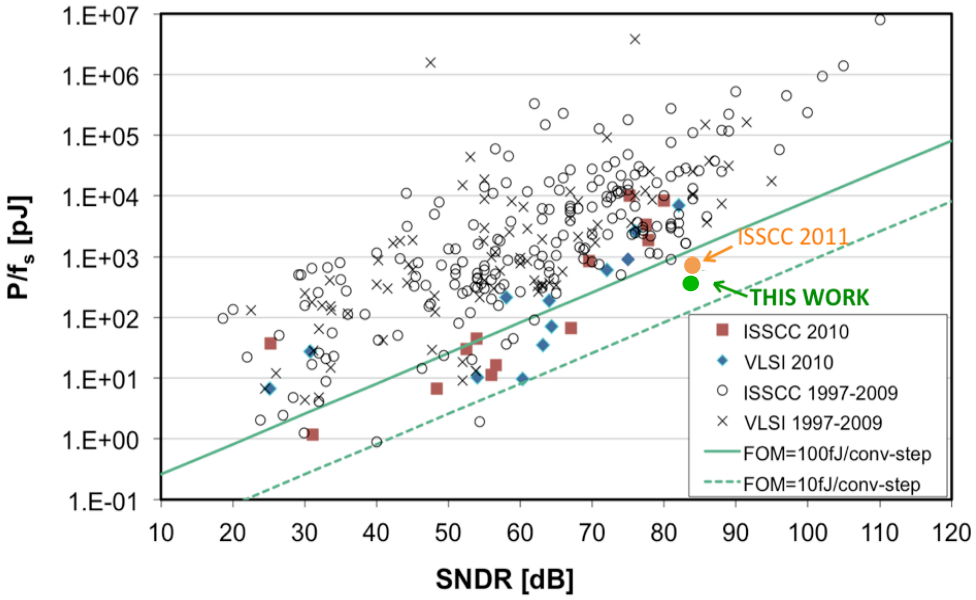

Figure 5.34: Comparison between the proposed power efficiency modulator with other state of the art ADCs presented in the last years. B. Murmann, "ADC Performance Survey 1997-2011," http://www.stanford.edu/∼murmann/adcsurvey.html.

with the last best result obtained at the ISSCC conference of 2011. The total power consumption of the modulator sampled at 70.4 MHz is 2.3 mW. The partial contribution are: first operational amplifier 300 μW (13.04%), second operational amplifier 336 μW (14.61%), 23 comparators 331 μW (14.39%), resistive DACs consume 929 μW (40.39%) and the digital logic 404 μW (17.57%).

Parameter	Value
Signal bandwidth b_w	2.2 MHz
Oversampling ratio	16
Sampling Frequency f_S	70.4 MHz
SNDR	83.27 dB
ENOB	13.54 bits
Dynamic Range	88 dB
Power Consumption	2.3 mW
FoM	43.8 fJ/(conversion-level)

Table 5.3: Summary of the performance of the third order DT modulator.

The total count excludes the power consumption of the output digital buffers that drive the output pad to realize the 5-bit encoder that transform the output modulator data from the one-out-of-N code to binary digital code. The achieved Figure of Merit (FoM) is consequently 43.8 fJ/(conversion-level). The performance summary of the simulated third order DT ΣΔ modulator is given in Table 5.4.

5.5.1 Layout Design

The realization of a good layout is a very important aspect in the design process of a ΣΔ modulator, due to the complexity of the structure, that integrated a mix of analog and digital circuitry. Normally a good design rule imposes to separate physically the analog circuitry from the digital blocks in order to prevent disruptive cross-talk effects that affect the final performance. On-chip, analog and digital blocks uses separate power supplies and grounds.

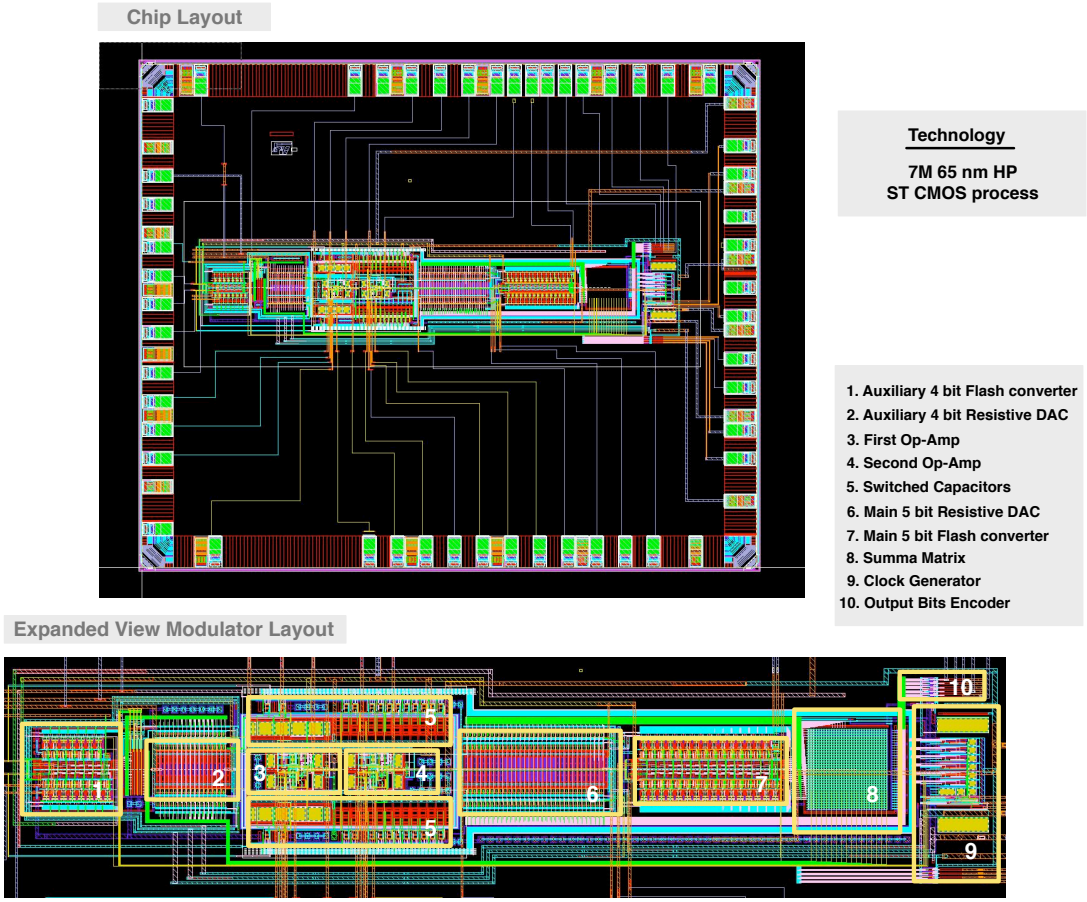

Figure 5.35: Top level of the third order DT ΣΔ modulator.

Long and wide guard ring were routed with the lower resistive metal in order to capture the noise coupled in the substrate and preserve signal integrity.

The proposed third order DT ΣΔ modulator has been integrated using a 65 nm, 7-metal, HP (high-performance for mixed signal design) step, CMOS technology, courtesy offered by ST Microelectronics from Castelletto, Milan (Italy). The active chip area is $1770 \times 400\ \mu m^2$, while

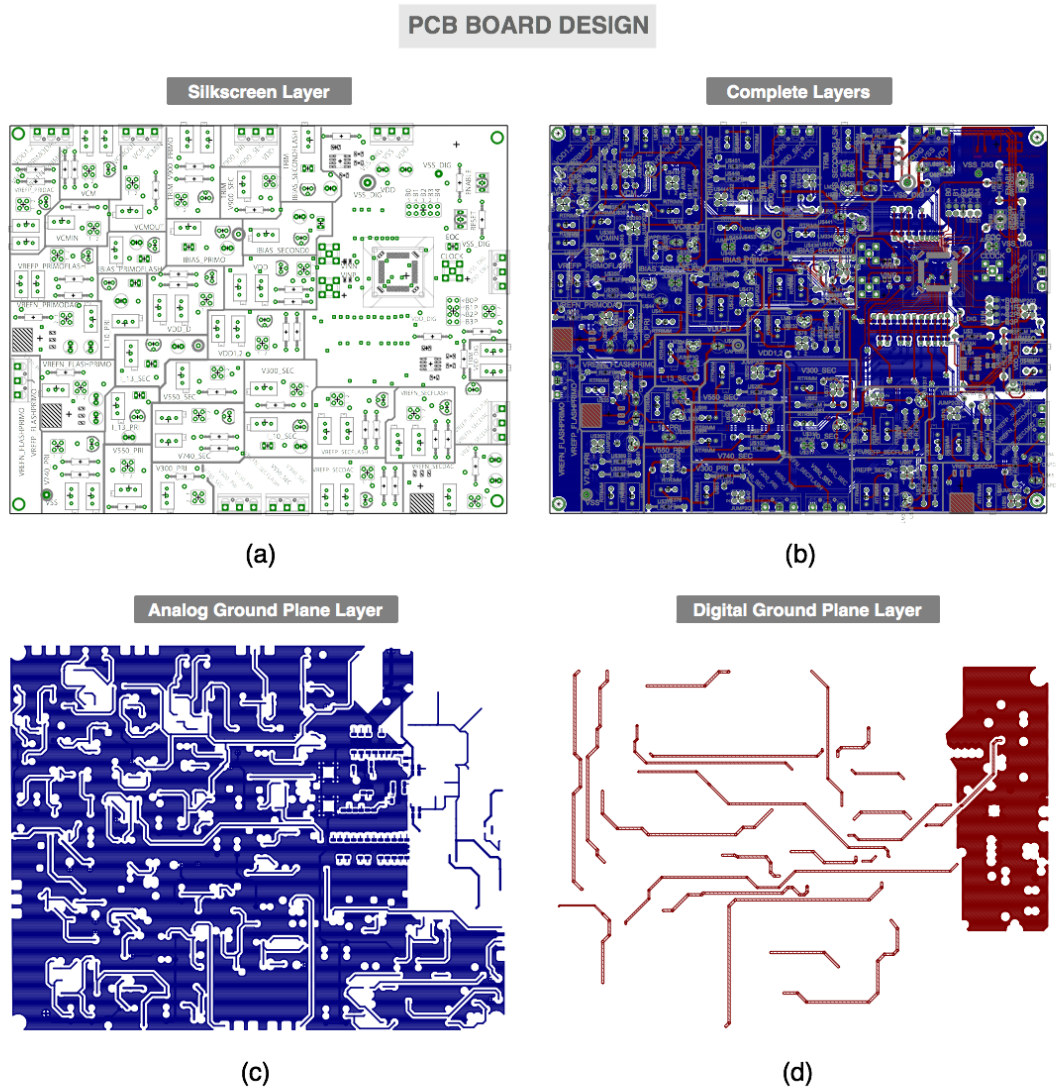

Figure 5.36: Board design for the third order ΣΔ modulator: (a) Silkscreen layer and all layers. (b) Analog ground layer. (c) Digital ground layer.

the total area with padring is $2200 \times 1800\ \mu m^2$. Fig. 5.35 shows the ΣΔ modulator floor plane with a zoom of the active area and the numbered list of the building block.

From above consideration, the clock tree is arranged at the bottom of the device and all generated clock phases and digital control signals run along the borders of the analog core. The heart of the core has been reserved to the two operational amplifiers, the switches capacitors network and the two string resistive DACs. The flash converters are positioned near the respectively DAC, while the addition matrix is placed in front the clock generator. The layout of a 65 nm analog block requires very carefully attention on the placement of dummies in order to mitigate the WPE and STI issues (as explained in Chapter 1) and increase the final symmetry of the structure.

5.5.2 Board Design

For a proper testing of the modulator performance a four layer board (Fig. 5.36 (a) and (b)) has been designed with Eagle software, by using the design guidelines presented in the appendix A. Analog and digital power supplies and grounds are separated into distinct planes (Fig. 5.36 (c) and (d)), while all the supplies line and the voltage reference lines of the chip are decoupled with SMD capacitor. As explained in Appendix A, all the decoupling capacitance must be placed as close as possible to the package pin in order to reduce the inductance of the lines. The voltage reference of the DACs and flash converters and all the currents bias are generated and decoupled off chip. This allows to study how the performance of the modulator integrated in the test chip, can change in order to optimize the power consumption.

Chapter 6

An Improved Design Methodology for Continuous-Time $\Sigma\Delta$ Modulators

The continuous-time CT $\Sigma\Delta$ modulators have received an increased attention over the last years as an alternative to their discrete-time DT counterpart. The CT architecture presents a better power efficiency, implicit antialiasing filtering and it allows to realize very high rate sampling rate, but in spite of these benefits, its synthesis is much more difficult compared to the DT counterpart, because the performance depends on the chosen typology of feedback DAC ([16], [17], [18], [19], [14]). Normally the CT design is obtained by starting from a DT prototype thank to many mathematical approach, like invariant impulse response, modified $\mathcal{Z}$ transform, and so on. Traditionally, all these methods are based on the assumption that the feedback signal in the CT implementation assumes ideal simple shapes, like non return to zero, return to zero or switched capacitor discharge on resistor, but real imperfections associated with real analog circuit, cause deviation from the ideal shape degrading the final performance. The chapter introduces a new general design methodology for all structure of $\Sigma\Delta$ modulator without any limitation about the shape and number of different typology of the feedback signal paths in the same modulator. This feature allows the system level compensation of nonidealities associated with the implementation of the real analog block. The key point of the proposed methodology is its simplicity because the procedure allows hand calculation also for complex modulator and is circuits oriented, so could be simply implemented with circuit simulator directly at transistor level, during the design step.

6.1 Introduction

In the past a lot of attention was focused to the development of new and innovative DT ΣΔ architecture, but nowadays the demand for increasingly performance with the stringent constraint of very low power consumption, changes the scenario. Continuous-Time (CT) ΣΔ modulators have become effective alternatives to Discrete-Time (DT) schemes for medium resolution, large signal bandwidth and low power. The key difference between a CT and a DT architecture is the shifting of the interface between continuous-time and discrete-time domain, as shown in Fig. 6.1.

The sampling in DT scheme is done at the beginning of the modulator, leading to its sampled-data nature. On the contrary, in the CT scheme sampling and quantization operations are done simultaneously inside the loop, offering an intrinsic antialiasing filtering feature. Despite this difference, the feedback signal in both CT and DT modulator is an analog signal converted from digital output domain thank to DAC and then processed through the respectively loop filter, which is a linear system. At the end, the output of the feedback linear system is sampled and quantized. Therefore, the equivalence between the CT and DT loop is realized if the respective feedback loop generate the same value at the input of the quantizer for identical digital codes present at the modulator output. In this way, both modulator exhibits the same NTF. Anyway, the continuos time nature of feedback waveforms generated in CT modulator affects the CT-DT equivalence, because it depends on the details of the transients. This makes the analysis and the synthesis of a CT modulator more difficult and challenging compared to its DT counterpart.

The design of the CT modulator is normally done by using an already designed DT prototype targeted with the expected performance. Assume that the loop transfer function of the linear discrete-time model shown in Fig. 6.1(a) is $H_D(z)$. In the case of the CT design (Fig. 6.1(b)), the loop transfer function also includes the response of the DAC, $H_{DAC}(s)$. The final CT loop

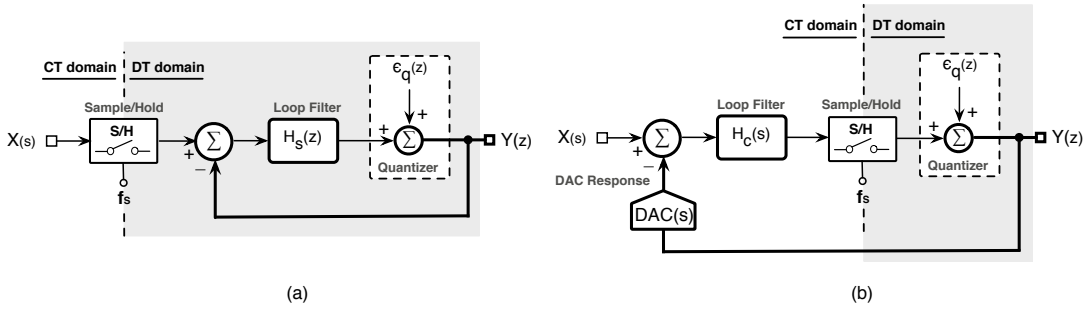

Figure 6.1: Linear model of a Discrete-Time ΣΔ (a) and of a Continuous-Time (b) ΣΔ modulator.

transfer function in the Laplace domain is:

$$G_C(s) = H_C(s) \cdot H_{DAC}(s) \tag{6.1}$$

The above condition about the equivalence at the input of the quantizer translates directly into:

$$\mathcal{Z}^{-1}\{H_D(z)\} = \mathcal{L}^{-1}\{G_C(s)\}|_{t=nTs} = \mathcal{L}^{-1}\{H_C(s) \cdot H_{DAC}(s)\}|_{t=nTs}. \tag{6.2}$$

Therefore the coefficients of CT structure can be calculated by discretizing its linear loop filter and matching it with the loop filter of the DT counterpart.

Early publications resolve (6.2) with different mathematical approaches, like the modified $\mathcal{Z}$ transform [23], the impulse invariant method ([17], [21]), the state-space approach ([60], [61]), the s-domain approach ([62]) or numerical optimization ([63]). The methods typically use for the DAC response a zero-order interpolator or a rectangle lasting a fraction of the clock period. Other more complex DAC responses and limits like the finite gain bandwidth of active blocks are difficult to study. The most common methods for the DT-CT transformation are:

- **Impulse Invariant Transform**.

  The corresponding time domain expression of (6.2), leads to the condition:

  $$h_{DT}(n) = [h_{DAC}(t) * h_{CT}(t)]|_{t=nTs} = \int_{-\infty}^{\infty} h_{DAC}(\tau)h_{CT}(t-\tau)d\tau|_{t=nTs} \tag{6.3}$$

  where $h_{DT}(n)$ is the impulse response of DT loop, $h_{CT}(t)$ is the impulse response of CT loop and $h_{DAC}(t)$ is the impulse response of the feedback CT DAC. This transformation allows the design of CT loop filter $H_C(s)$, which in combination with a chosen DAC transfer function DAC(s) results in the same impulse response of the DT loop filter $H_D(z)$ counterpart. The equivalence between the open loop responses, as explained above, ensures same NTF. The adoption of basic DAC responses like NTZ, RZ or SCR simplifies the design procedure, because in literature are available tables that present directly the result of the transformation (6.3) for this basic loop filter poles with closed-form expression. However, the procedure for calculating the CT coefficients, requires to dividing the DT loop filter into its partial fractions and applying the basic equivalents given by specific table for each kind of CT feedback DAC. The study of real DAC response affected by circuit limitation, complicates the calculus and requires the support of symbolic math program.

- **Modified $\mathcal{Z}$ Transform**.

  This approach is an extension of a general $\mathcal{Z}$ transformation, because allows to calculate the value of a discrete time system at all sampling time, also in the case of delayed and multirate systems. The procedure starts with the evaluation of the $G_C(s)$ loop filter and

the consequent conversion to the $\mathcal{Z}$ domain by using the modified $\mathcal{Z}$ transform, as follow:

$$H_m(z) = \sum_i \mathcal{Z}_{m_i}\{H_C(s) \cdot H_{DAC}(s)\} \tag{6.4}$$

The calculated transfer function $H_m(z)$ is than compared with the starting DT loop filter in order to obtain the equivalent CT coefficient. The variable m is a delay factor normalized to the sampling period T_S. It is bounded between 0 (corresponding to the previous sampling instant) and 1 (corresponding to next). As reported for the impulse invariant response, also for this case in literature are available tables that realize this transformation for the basic filter loops. The limit of the method is its not accurately modeling of the excess loop delay.

- **State-Space Approach**.

  The method proposed in [60], allows the calculation of the coefficients of the CT modulator using extensive exponential matrix calculation, leading to cumbersome algebra. The complexity of calculations rises up rapidly when include the effect of the circuit level non-idealities, because require the calculus of the residues. The operation can be done only by using symbolic calculation software in which the residues are efficiently calculated from a Laurent series or using Padé approximation.

Other methods, like numerical optimization [63] or direct filter synthesis with Matlab tools [62], are rather uncommon because are afflicted with some restrictions for a general use.

6.2 Limits of CT Design Methods

A DT prototype gives rise to a CT equivalent by replacing sampled data integrators with continuous-time integrators. The time constants on the signal path are unchanged while the coefficients in the branches that feed back the digital output change depending on the impulse DAC responses ($h_i(t)$). The reason is that differences in the operation of a DT and a CT integrator propagate through the cascade making it necessary to perform correcting actions along the architecture.

Consider, for example, Fig. 6.2. It is a multiple chain of k discrete integrators with distributed feedback. Conceptual schemes use a single DAC and local amplification to realize the β_i design coefficients. Real implementations use separate DACs typically made by binary weighted or unary capacitors with suitable unity value.

The design methods that transform the DT prototype into a CT equivalent determine the feedback coefficients $\omega_{i,j}$. The first index refers to the position of the DAC in the DT scheme. The second index indicates the injection position in the CT counterpart. The $\omega_{i,j}$ coefficients depend on the impulse response of the DAC. The conventional DT-CT transformation methods proposed in the literature suppose to use a DAC with equal impulse response along the cascade.

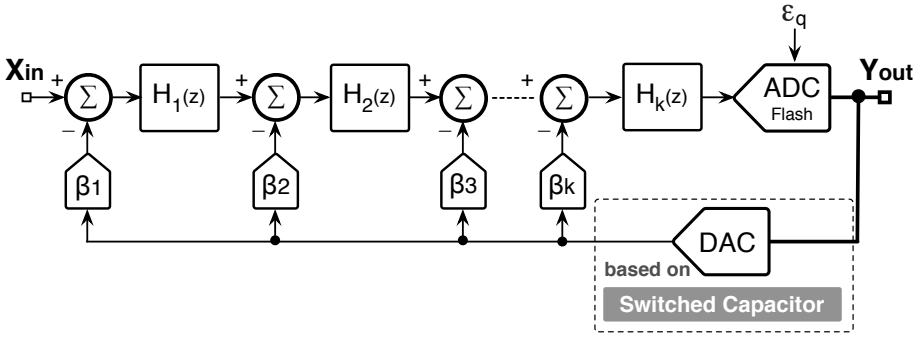

Figure 6.2: Generic k-th order Discrete Time ΣΔ modulator.

Therefore, in the case of different DAC impulse responses, the correct implementation of a multi-feedback scheme is the one of Fig. 6.3. The injection in the position 2 is the superposition of the impulse response of DAC1 multiplied by $\omega_{1,2}$ with the impulse response of DAC2 multiplied by $\omega_{2,2}$. For the injection in the position 3 there are three terms injected with the impulse response of the first second and third DAC and so forth for the successive inputs.

Since the use of many DACs as required by Fig. 6.3 is unpractical, real implementations normally superpose the design coefficients and realize them with a single DAC response. This is an evident limits, because poses constraint on the degrees of freedom in designing: for example, the total noise contribution from the feedback DACs is dominated by the noise of the DAC that inject at the first integrator, because the PSD of the noise from the other DACs is noise shaped. Thus, the optimization of noise performance imposes particular attention on a proper design of only first DAC in terms of noise and linearity contribution. Finally, the possibility to choose different DAC allows to maximize noise and also power performance, as proposed in [64] for a second order ΣΔ modulator. Anyway, the synthesis process in [64], is based on

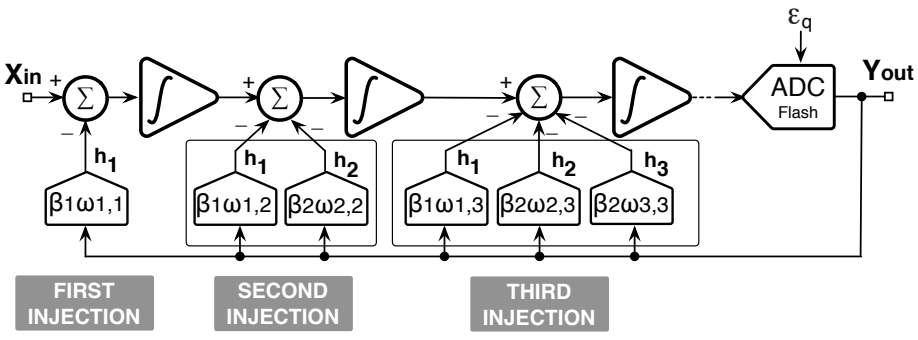

Figure 6.3: Equivalent CT ΣΔ modulator with multiple DAC responses.

the calculus of the CT feedback coefficients with manually repetitive response simulation. This limits is overcome thank to the improved design methodology proposed in this chapter, that illustrates the steps to follow in order to calculate directly the value of the CT coefficients.

6.3 Basic level Approach

In this paragraph is proposed a first approach that permits to realize the complete STF and NTF CT-DT equivalence. The method works entirely in time domain and allows to synthesize CT feedback loop with different feedback DAC in the same scheme. Moreover, this method permits to compensate the influence of real analog components by tuning properly the feedback coefficients. For sake of simplicity, without any loss of generality, the theory will be introduced with the design of a second and a third order $\Sigma\Delta$ modulator.

6.3.1 Second Order Continuous-Time

Let us consider the design of a second order modulator using the DT prototype of Fig. 6.4(a). It has a delay in the last integrator. Fig. 6.4(b) shows the equivalent CT scheme. For NRZ DAC the use of the method described in [17] obtains the coefficients

$$\alpha_1 = \frac{a_1}{T} \quad and \quad \beta_1 = 1.5 \cdot \frac{b_1}{T} \tag{6.5}$$

The NTFs are equal but the STFs differ. However, extensive computer simulations verified that it is possible to obtain equal STFs. For this, it is necessary to add an input feedforward branch β_2, as shown in Fig. 3. The exact equivalence holds if the input signal passes through a S&H (NRZ). This is clearly a limitation, but the error introduced does not corrupt the result if the sampling rate is higher than the bandwidth of the input signal. A comparison of Fig. 6.4(b) and Fig. 6.5 allow us to verify that

$$\beta_2 \cdot T = \beta_1 \cdot T - b_1 \tag{6.6}$$

Therefore, the path that ensures exact equivalence corresponds to the amount needed to increase $\beta_1 \cdot T$ with respect to b_1.

If the DAC responses (Fig. 6.5) become RTZ with Δ_1 and Δ_2 duty cycle, the amplitude of the pulse at the input of the first integrator must increase as prescribed by

$$\Delta_1 \cdot \alpha_1 \cdot T = a_1 \tag{6.7}$$

that ensures an equal charge injected in the first integrator as for the NRZ case. For the second integrator, a proper relation is found to be

$$\beta_1 \cdot \Delta_2 \cdot T = (2 - \frac{\Delta_1}{2}) \cdot b_1 \tag{6.8}$$

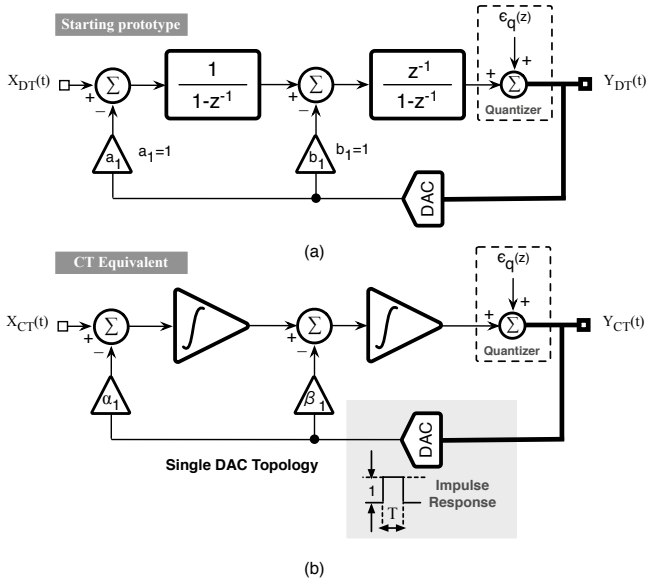

Figure 6.4: (a) Second Order of Discrete-Time ΣΔ modulator. (b) Equivalent Continuous-Time ΣΔ modulator.

that becomes $1.5 \cdot b_1$ for NTZ ($\Delta = 1$). The RTZ changes the coefficients α_1 and β_1 but not β_2 because it compensate for the signal at the input. Equations (6.7) and (6.8) have been verified by behavioral simulations for various values of Δ.

Suppose now that the two DACs have generic impulse responses $h_{DAC1}(t)$ and $h_{DAC2}(t)$. The value of α_1 must such that

$$a_1 = \alpha_1 \int_0^T h_{DAC1}(t)dt \tag{6.9}$$

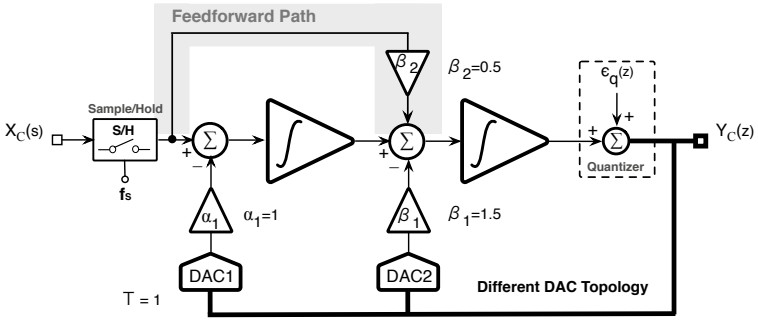

Figure 6.5: Continuous-Time Second Order ΣΔ modulator with NRZ DAC response.

A generalization of (6.8) is

$$\beta_1 \int_0^T h_{DAC2}(t)dt = \{K_1 - H_{DAC1}\} \cdot b_1 \tag{6.10}$$

where K_1 and H_{DAC1} are coefficients that depend on the generic responses $h_{DAC1}(t)$ and $h_{DAC2}(t)$. Therefore, the coefficient β_1 depends on the responses of both DACs.

6.3.2 Benefit of the Exact Equivalence

The transformation of a DT prototype into an exactly equivalent CT scheme is not beneficial only because the STFs are equal but mainly because the exact equivalence offers a powerful way to compensate the effect of real analog DAC. Moreover, computer simulations enable us to trim the design and to compensate for non ideal effects.

The method used is the search of the value of β_1 that makes equal the CT and the DT designs and, in particular, the output spectra, or better the FFTs of the outputs, $S_{CT}(f_i)$ and $S_{DT}(f_i)$. Since it is necessary to estimate only one parameter we define the quantity

$$S(\beta_1) = \sum_{f_i=1}^{fi=N} [S_{CT}(f_i) - S_{DT}(f_i)] \tag{6.11}$$

The relationship (6.9) determines the value of α_1. The value of β_1 that makes zero (6.11) provides the second parameter. Since (6.11) is non linear, it is necessary to use a numerical successive approximation method to zero, like the Newton-Raphson.

Suppose to consider the two real DAC responses of Fig. 6.6. The coefficient α_1 calculated by using relation (6.9) is α_1= 2.5974 supposing $T = 1$. The plot of (6.11) versus β_1 is not

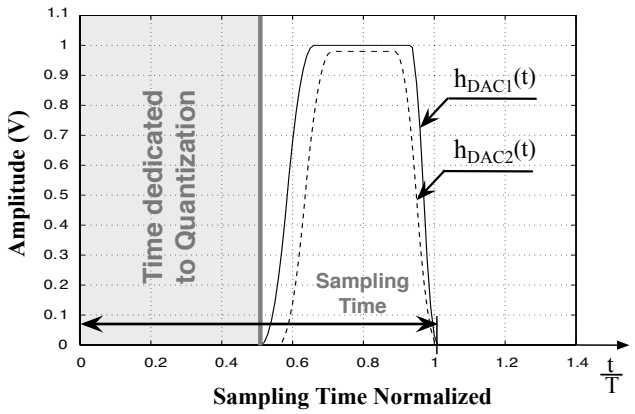

Figure 6.6: Example of two possibile real RTZ DAC impulse response.

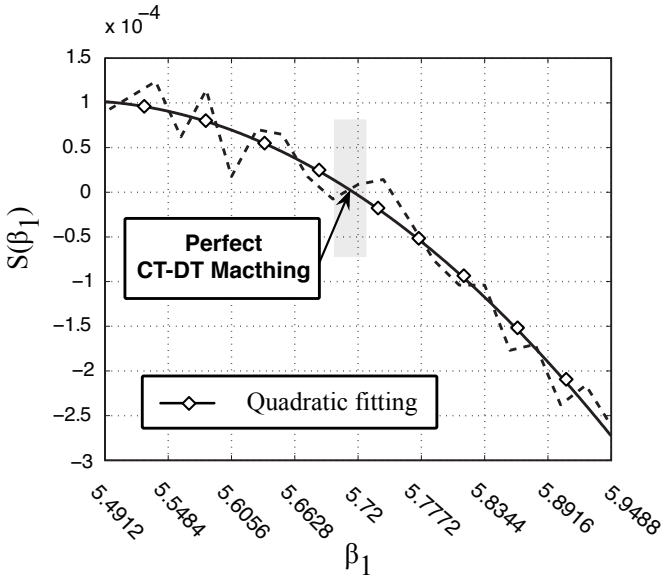

Figure 6.7: S(β_1) versus β_1

smooth, as shown in Fig. 6.7. The reason is that the modulator is a non-linear block. In order to facilitate the zero search we use a quadratic fitting of the estimated values. The zero occurs at $\beta_1 = 5.720$.

6.3.3 Third Order CT Equivalent Scheme

Let us consider the DT third order modulator shown in Fig. 6.8. The first two DT integrators are without delay, the last integrator is with delay. Fig. 6.9 shows the equivalent CT scheme with separate DACs serving each single feedback path. Moreover, Fig. 6.9 shows the values of the coefficients for NRZ DACs.

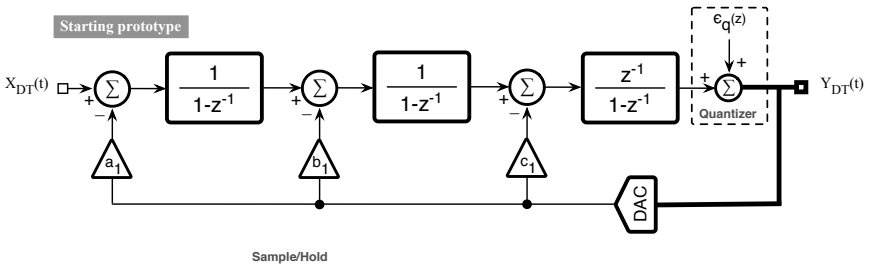

Figure 6.8: Third Order Discrete-Time ΣΔ modulator.

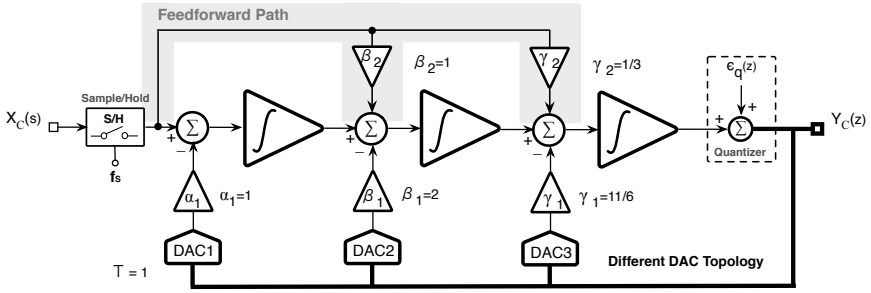

Figure 6.9: Third Order Continuous-Time ΣΔ modulator with additional paths in the case of NRZ DAC response.

In order to obtain the exact time equivalence two extra paths from the input to the two intermediate summing nodes are necessary. They are named β_2 and γ_2 in the diagram. The needed values of the coefficients have been determined by successive approach using fractional values. The search was facilitated by the fractional value γ_1. The use of multiples of 1/6 obtained the exact equivalence for $\beta_2 = 6/6$ and $\gamma_2 = 2/6$.

The use of RTZ DACs or DACs with generic responses changes the values of coefficients α_1, β_1 and γ_1 only. The ones that achieve exact equivalence are estimated by a procedure that is more complex than the one of a second order scheme. However, for α_1 the request to inject the same charge for CT and DT leads to the same condition (6.9).

The values of β_1 and γ_1 are estimated by the search of the condition of exact equivalence. However, since there are two coefficients it is necessary to use a nulling function different from (6.11). If one of the parameters is kept constant, changing the other it is possible to find a zero of (6.11), but that value cannot be the true solution. A more convenient nulling function is

$$S_2(\beta_1, \gamma_1) = \sum_{f_i=1}^{f_i=N} (S_{CT}(f_i) - S_{DT}(f_i))^2 \tag{6.12}$$

that is always positive and becomes zero at the pair β_1 and γ_1 that achieve the exact equivalence.

The non-linear nature of S_2 imposes a computer zero nulling search. The zero search will end when the pair of coefficients obtain S_2 near zero within a defined acceptable limit. When using real blocks the simulation of the modulator must include the behavioral description of real limits.

6.3.4 Effect of Real Blocks

The use of real op-amps or OTAs in the CT implementation alters the integrator response. This effect can be studied together the real DAC response. As proposed in [65] a real integrator must be simulated at system level. Then, the integrator is modeled as the cascade of an ideal

integrator and a correcting CT block whose response is low-pass like. For example, the finite GBW gives rise to an integrator gain error (GE) and a parasitic pole ω_p.

With a suitable topological transformation the correcting CT blocks can be incorporated in the DAC responses to obtain a scheme with ideal integrators, real DAC and a block in front of the modulator $k_{(S)}$, as depicted in Fig. 6.10, that accounts for the correcting functions of the three real integrators. Its effect on the signal transfer function is negligible because the three poles are far away from the signal band.

The topological transformation that incorporate the limit of the integrator limit into the DAC causes an equivalent extra loop delay [65].

Table 6.1: Duty Cycle Parameter for Third Order of Fig. 6.10

Case	Δ_1	Δ_2	Δ_3	α_1	β_1	γ_1
1	1	1	1	1	2	1.8336 (11/6)
2	1	1	0.61	1	2	3.0056
3	1	0.54	0.61	1	3.7038	3.7596
4	0.44	0.53	0.6	2.2727	4.3019	3.9392

6.3.5 Computer Simulations Strategy

As well known there is a defined region of stability in the parameter's space for any high order modulator. Therefore, the search of the coefficients that lead to an exact equivalence must be kept away from instable regions. This is obtained with a suitable design strategy that achieves the result by successive changing of the coefficient one by one, as indicated by Table 6.1. The

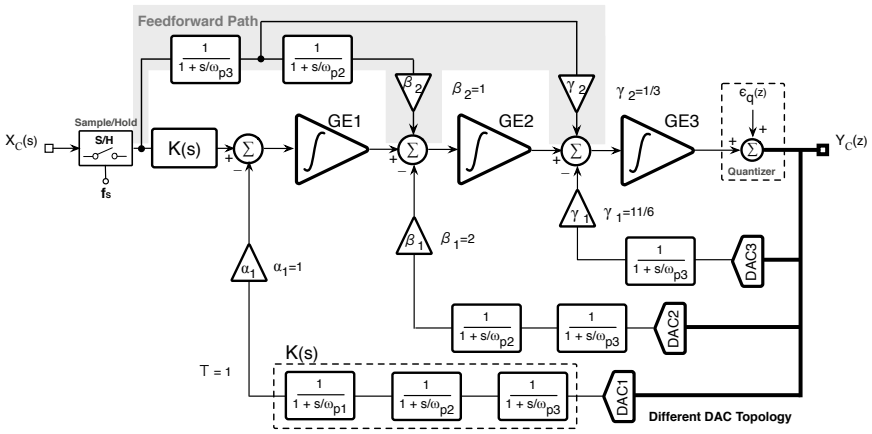

Figure 6.10: Complete model for Third Order CT with finite GBW modulator.

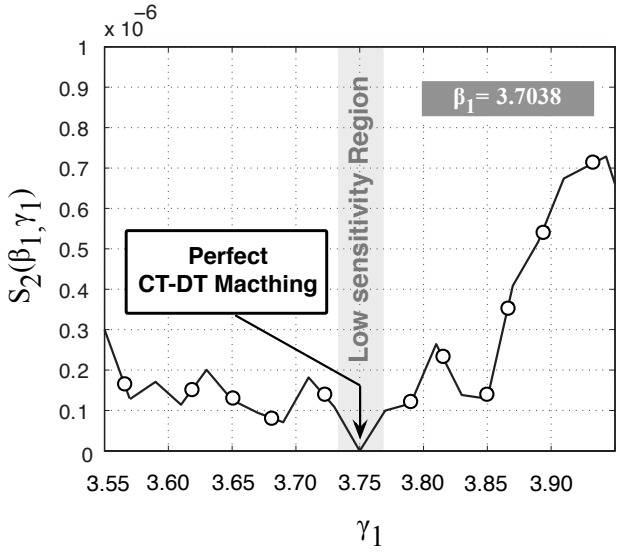

Figure 6.11: Third Order CT modulator: $S_2(\beta_1,\gamma_1)$ versus γ_1 in the case of Δ_1=1 Δ_2=0.54 and Δ_3=0.61.

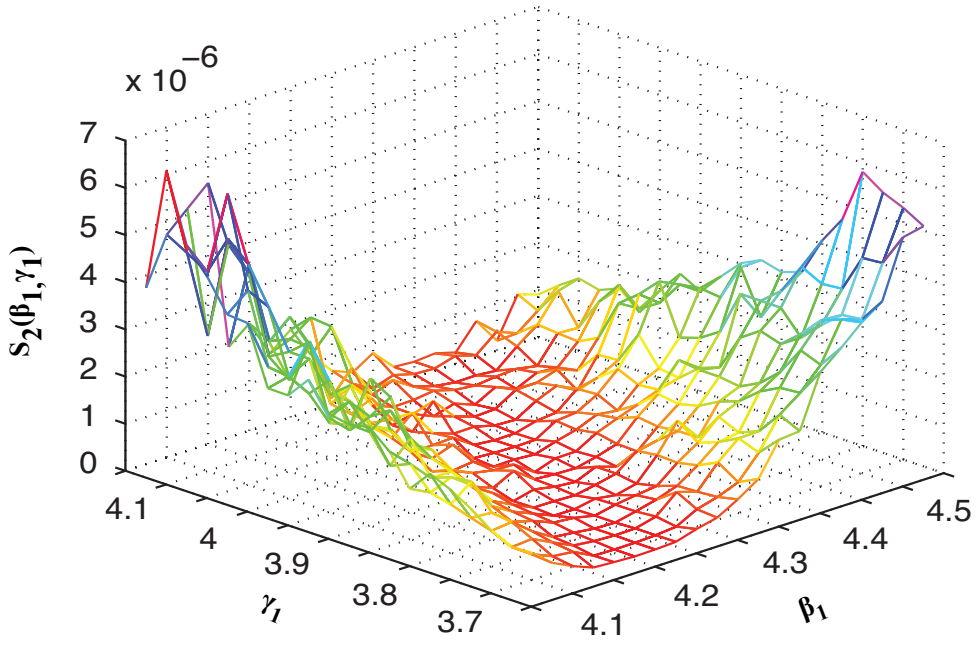

Figure 6.12: Third Order Continuous-Time ΣΔ modulator: $S_2(\beta_1,\gamma_1)$ versus pair (β_1,γ_1) in the case of Δ_1=0.44 Δ_2=0.53 and Δ_3=0.6.

initial design assumes ideal blocks and NRZ DACs. The next step uses a real DAC in the third stage that corresponds to the use of an equivalent duty cycle $\Delta_3 = 0.61$. The use of the condition (6.9) gives $\gamma_1 = 3.0056$. The third step supposes real the second DAC and again, condition (6.9) determines β_1. The value of γ_1 is determined by a zero search of S_2 (even S_1 works), starting from the value of the previous step. Fig. 6.11 shows the function S_2 versus γ_1 with DAC_2 and DAC_3 real.

The last step considers real the first DAC and all the integrators. Equation (6.9) estimates the value of α_1. The zero search of S_2 yields β_1 and γ_1. Fig. 6.12 shows the 3D plot of S_2 versus β_1,γ_1. The figure, in addition to identifying the solution also indicates a region of low sensitivity. Fig. 6.13 is a magnification of the 3D plot of Fig. 6.12. It identifies the pair $\beta_1 = 4.3019$ and

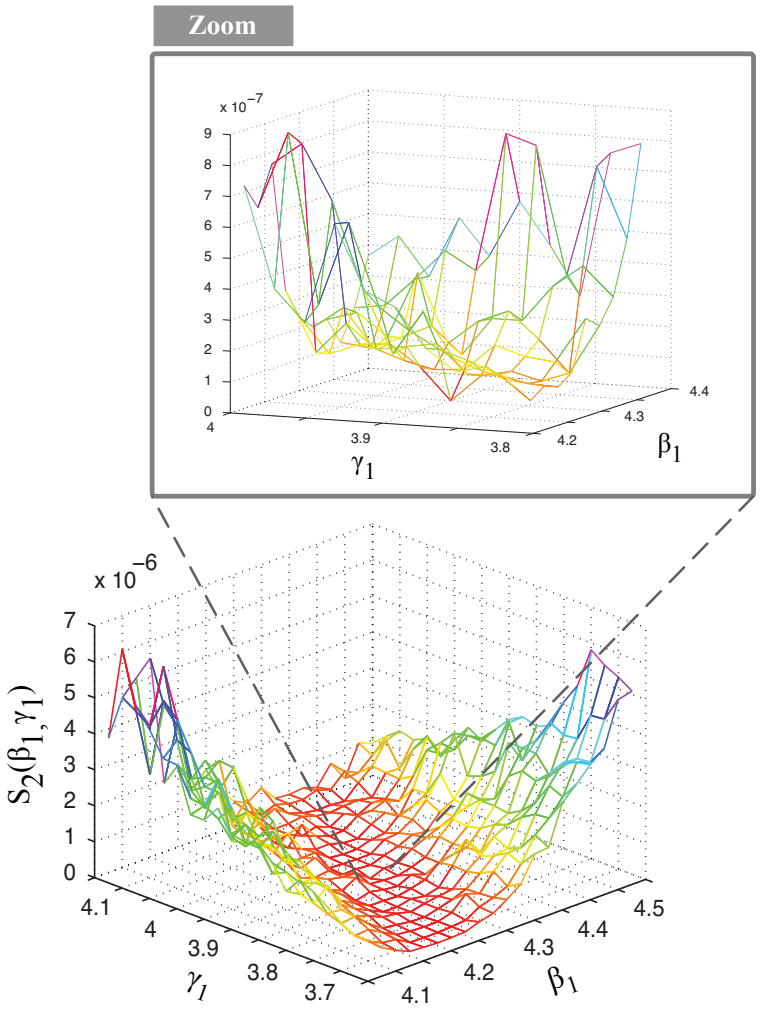

Figure 6.13: Magnification $S_2(\beta_1,\gamma_1)$ in the case of Δ_1=0.44 Δ_2=0.53 and Δ_3=0.6.

$\gamma_1 = 3.9392$ that zero S_2. This is the point of exact equivalence between the CT scheme and the DT prototype.

6.4 Improved design methodology

The goal of this study is to investigate an improved design methodology that makes the NTF of the continuous time scheme equal to the one of the DT prototype. Having equal STFs is not particularly relevant, being enough to have the same signal responses in the signal band and alike responses outside signal band.

The method studied here states that equal NTFs result from a CT and a DT schemes that are exact equivalents, a property for which all the samples at the input of the CT and DT analog to digital converters (ADCs) have the same values for any DAC input sequence and zero input signal. If the circuits are exactly equivalent, the processing of the quantization noise within the quantization loop gives rise to the same sampled data responses.

The design of exactly equivalent modulators is conveniently done in the time domain. For the sake of simplicity, we illustrate the method starting from a third order low-pass DT prototype, as shown in Fig. 6.14. The extension to higher order or other architectures is not difficult. The DT integrators are accumulators (A_{CCU_i}) with impulse response $h_i(nT)$. The accumulators could be with or without delay, but in every feedback loop it is necessary to have at least one delay. The feedback coefficients, β_1, β_2, β_3 and the possible delay of the sampled-data integrator produce the DT signal and noise transfer functions. How to derive coefficients and how to possibly assign delay to integrators is known but not discussed here.

The first step of the procedure is to expand the scheme into branches made of the cascades of integrators. The result is shown in Fig. 6.15. The second and the third integrators are duplicated to give rise to separate processing; the outputs of the branches are summed up to determine the input of the quantizer. Notice that each branch processes only signals coming from the DAC, the input of the modulator being set to zero. The linear property of the scheme ensures the correspondence between Fig. 6.14 and Fig. 6.15. Therefore, $P_Q(nT)$, the input of

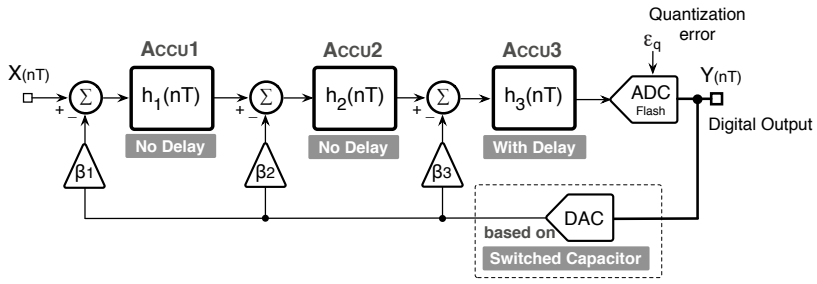

Figure 6.14: Discrete time third order low pass ΣΔ modulator.

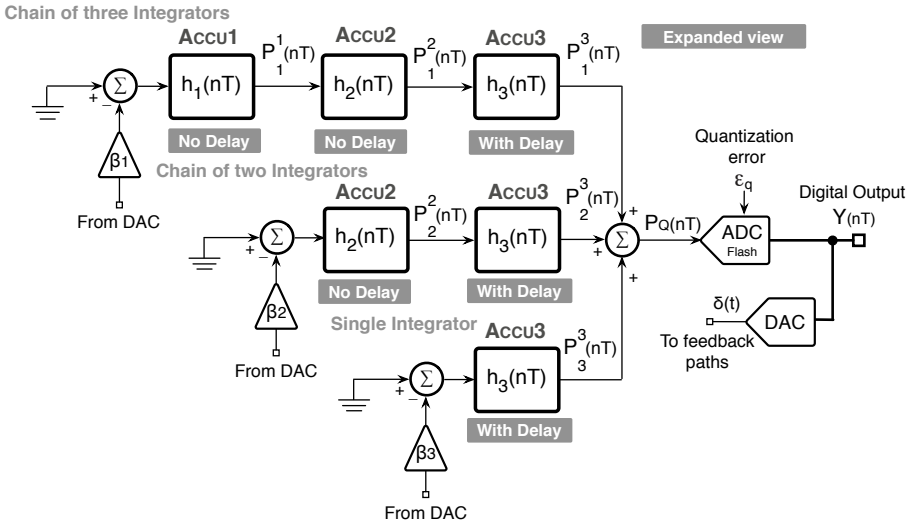

Figure 6.15: Expanded view of a discrete time third order low pass ΣΔ modulator.

the quantizer, is $P_Q(nT) = P_1^3(nT) + P_2^3(nT) + P_3^3(nT)$.

Thanks to the linear property, the exact CT equivalent of Fig. 6.14 must be also the exact equivalence of Fig. 6.15. Therefore, it is required to find the exact equivalence of each branch of the expanded scheme. We will see that the CT exact equivalent of a branch with multiple integrators needs extra injection of CT signals. This must be done through DACs whose impulse response is the one of the converter used on that intermediate input.

The superposition of exact equivalent branches gives rise to the overall CT architecture. The result has the same architecture as in Fig. 6.14, with CT integrators replacing the sampled data counterpart but, obviously, the CT feedback coefficients are different. The study assumes, as normally done in CT designs, that CT integrators have a time constant equal to the sampling period.

The exact equivalence must hold for any waveform delivered by the flash; however, since the system is linear, it is possible to focus the study on a delta pulse driving the DT and the CT DACs. For the DT scheme, the DACs have delta at output. The CT schemes use the impulse responses of the DACs. As already mentioned, they can have any waveform, but it is assumed they go to zero at the end of the sampling period. Otherwise, the impulse response should be divided into two sections with the second one entered during the next clock period. That would correspond to the presence of a transversal filter in the DT prototype.

6.4.1 Single Integrator Exact Equivalence

Fig. 6.16 shows the bottom DT branch of Fig. 6.15 and its CT counterpart. The sampled data accumulator is with delay because it is the only block around the loop, just before the

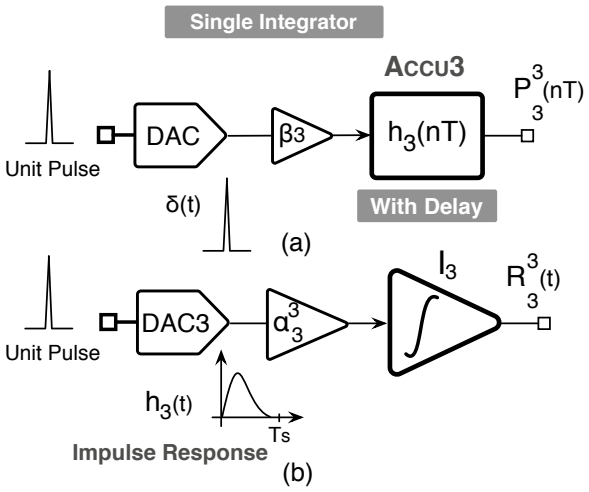

Figure 6.16: Discrete (a) and (b) Continuous time single integrator branch.

quantizer. For the CT architecture the input of the integrator is the impulse response of the DAC. Notice that, at the beginning of the clock period, a small fraction of time-slot is dedicated to the quantization process.

Normalizing the time of the sampling period to 1, the output of the DT integrator is

$$P_3^3(n) = \beta_3 step(n-1) \tag{6.13}$$

The output of the CT integrator is

$$\begin{cases} R_3^3(1) = \alpha_3^3 \int_0^1 h_3(\tau)d\tau & t \leq 1 \\ R_3^3(n) = \alpha_3^3 \int_0^1 h_3(\tau)d\tau & n > 1. \end{cases} \tag{6.14}$$

where $h_3(t)$ is the impulse response of DAC3.

The time equivalence conditions lead to

$$\beta_3 = \alpha_3^3 \int_0^1 h_3(\tau)d\tau \ = \alpha_3^3 h_{int,3}^1 \tag{6.15}$$

that defines $h_{int,3}^1$, the first integral of the DAC3 response, $h_3(t)$, over the sampling period.

Notice that the shape of the waveform of the CT outputs within the $[0, 1]$ period is irrelevant; what matters is its value at the sampling times $t = n$. Moreover, since the DAC control is a single pulse $\delta(t)$, the DT and CT outputs remain constant for $n > 1$. Having equal outputs at $t = 1$ ensures that the outputs are equal for any time $t = n > 1$.

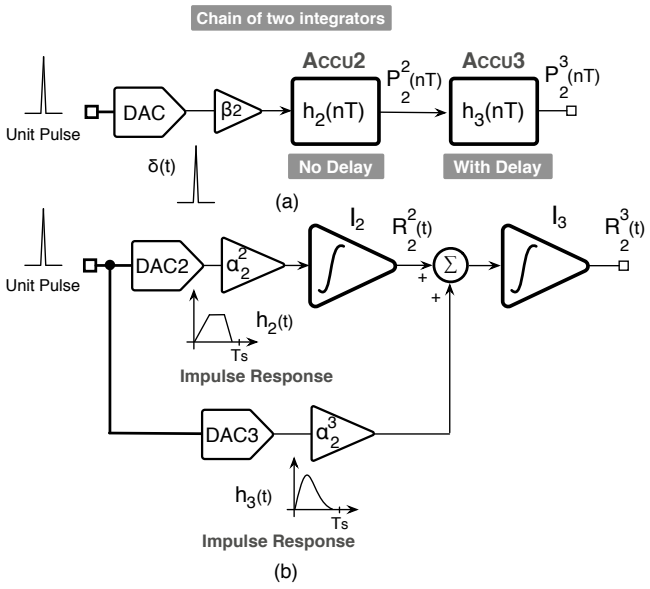

Figure 6.17: Chain of two integrators: Discrete (a) and (b) Continuous time version.

6.4.2 Double Integrator Exact Equivalence

For the cascade of two DT integrators there are two different options: first integrator without delay, as shown in Fig. 6.17 (a) or first integrator with delay. Let us consider the former case first. With a $\delta(t)$ pulse at input the output of the first integrator is a step and that of the second integrator is a staircase with values at the sampling times $t = n$ given by

$$\begin{cases} P_2^2(n) = \beta_2 step(n); \\ P_2^3(n) = \beta_2 \cdot n \quad n > 0. \end{cases} \tag{6.16}$$

The CT counterpart must be able to generate the same amplitude at the output of the second integrator at time $t=1$ and give rise to a ramp with the same slope for $t>1$. Since the slope depends on the output of the first integrator at $t=1$ it is necessary to meet two conditions and this, according to a simple verification, cannot be realized with one parameter.

It is necessary to plan for two injections at the input of the first and the second integrator. The injection onto the second integrator must match the impulse response of DAC3. The request on equal slopes determines the gain factor, α_2^2. The condition on equal outputs gives rise to the coefficient α_2^3, of Fig. 6.17 (b).

The exact equivalent conditions are

$$\begin{cases} P_2^2(1) = R_2^2(1);\ \beta_2 = \alpha_2^2\, h_{int,2}^1; \\ P_2^3(1) = R_2^3(1);\ \beta_2 = \alpha_2^2\, h_{int,2}^2 + \alpha_2^3 h_{int,3}^1 \end{cases} \tag{6.17}$$

where

$$h_{int,2}^1 = \int_0^1 h_2(\tau)d\tau \tag{6.18}$$

$$h_{int,2}^2 = \int_0^1 h_{int,2}^1(\tau)d\tau, \tag{6.19}$$

are the first and the second integral of the DAC2 response over the $[0, 1]$ time interval.

The case of two DT integrators with delay determines the following DT impulse responses

$$\begin{cases} P_2^2(n) = \beta_2 step(n-1); \\ P_2^3(n) = \beta_2 \cdot n \quad n > 1. \end{cases} \tag{6.20}$$

The condition on the slope remains unchanged because it holds for $t > 1$. The exact equivalent conditions are

$$\begin{cases} P_2^2(1) = R_2^2(1);\ \beta_2 = \alpha_2^2\, h_{int,2}^1; \\ P_2^3(1) = R_2^3(1);\ 0 = \alpha_2^2\, h_{int,2}^2 + \alpha_2^3 h_{int,3}^1 \end{cases} \tag{6.21}$$

which, again, together with the impulse response of the CT scheme, determine the parameters α_2^2 and α_2^3 which ensure exact equivalence. Another procedure that gives rise to exact equivalence is to use the conditions that are verified if values and slopes are equal at t=1. Their extensions are more convenient conditions for high order schemes.

$$\begin{cases} P_2^3(1) = R_2^3(1) \\ P_2^3(2) = R_2^3(2), \end{cases} \tag{6.22}$$

6.4.3 Triple Integrator Exact Equivalence

The branch of three DT integrators with or without delay has β_1 as input multiplier of the input DAC. The injection of a pulse gives rise to DT second order ramps with the delay established by the architecture at the output. For example, three integrators and only one delay in the last stage, like the one shown in Fig. 6.18 (a), and a pulse at input give rise to

$$P_3^3(n) = \beta_3 \sum_1^n \sum_0^n 1. \tag{6.23}$$

The CT architecture that enables exact equivalence is the one in Fig. 6.18 (b). The outputs

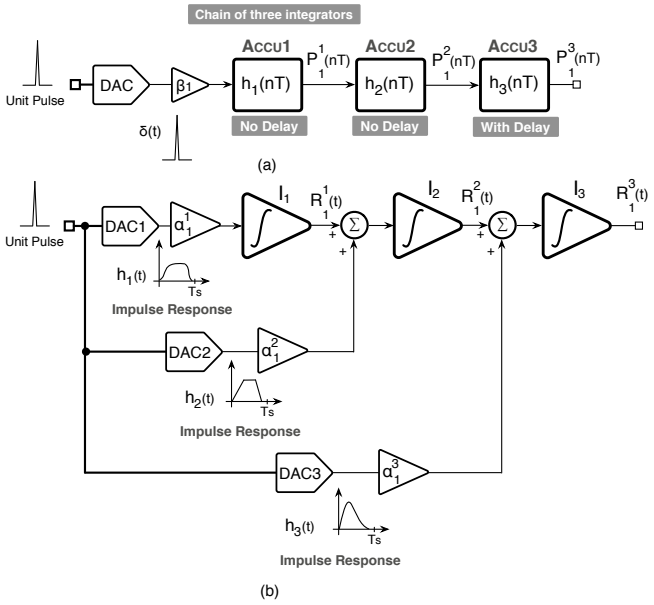

Figure 6.18: Chain of three integrators: Discrete (a) and (b) Continuous time version.

$R_3^3(n)$ at times $t = 1, 2, 3$ are

$$\begin{cases} R_3^3(1) = \alpha_1^1\, h_{int,1}^3 + \alpha_1^2\, h_{int,2}^2 + \alpha_1^3 h_{int,3}^1 \\ R_3^3(2) = R_3^3(1) + \alpha_1^1\, h_{int,1}^2 + \alpha_1^2\, h_{int,2}^2 \\ R_3^3(3) = R_3^3(2) + \alpha_1^1\, (h_{int,1}^1 + h_{int,1}^2) + \alpha_1^2\, h_{int,2}^2. \end{cases} \tag{6.24}$$

The exact design condition requires $P_3^3(1) = R_3^3(1)$, equal slope and equal second order derivative or, equivalently

$$\begin{cases} P_3^3(1) = R_3^3(1) \\ P_3^3(2) = R_3^3(2) \\ P_3^3(3) = R_3^3(3); \end{cases} \tag{6.25}$$

that make a linear system of three equations needed for estimating the design parameters α_1^3, α_2^3 and α_3^3.

6.4.4 Superposition of results

The exact equivalences of the three branches of Fig. 6.15 determine three schemes that involve one DAC injection at the input of the first integrator, two DAC injections at the input of the second integrator and three DAC injections at the input of the last integrator. Since the DACs of the CT exact equivalent have the same impulse response it is possible to superpose their

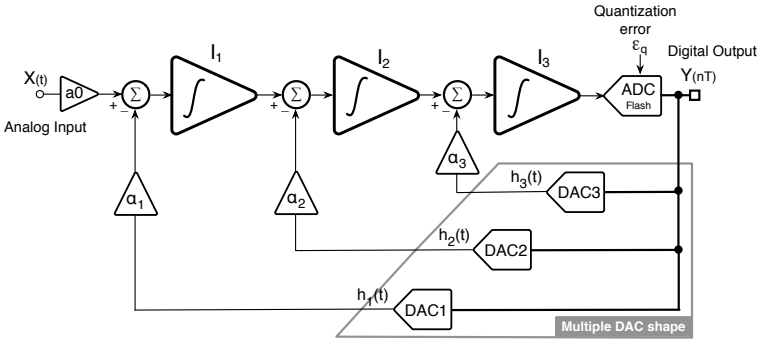

Figure 6.19: Continuous time final block diagram.

effects, leading to the scheme of Fig. 8.7. The α_i coefficients are

$$\begin{cases} \alpha_1 = \alpha_1^1 \\ \alpha_2 = \alpha_2^1 + \alpha_2^2 \\ \alpha_3 = \alpha_3^1 + \alpha_3^2 + \alpha_3^3. \end{cases} \tag{6.26}$$

Thus obtaining the exact equivalence in the time domain allows one to equal the input at the quantizer in both modulators at each sampling time. This provides the same processing as the feedback loop and consequently the same NTF for both modulators.

6.4.5 Extension to higher order

The design methodology developed for the third order scheme can be extended to higher order modulators with low-pass or band-pass response. The design steps are the same. They are summarized as follows:

- Define the DT prototype and consider only the paths from the ADC.
- Expand the DT prototype into parallel processing. Duplicating the DT integrator gives the quantizer input as the superposition of paths made by a cascade of integrators without intermediate inputs.
- Obtain the DT-CT exact equivalence of each branch by estimating the output responses of a DT and a CT counterpart with multiple intermediate inputs. The DAC of the intermediate input must have the impulse response of the DAC used in the final scheme in that position.
- Resolve the system of linear equations that make the outputs of the DT and CT branches equal at times $t = 1, 2, \cdots N$, where N is the number of integrators of the branch.

- Superpose the exact equivalent of branches to produce the final architecture.

6.5 Non-idealities in CT ΣΔ Modulators

The loop filter of a CT ΣΔ modulator determines the noise transfer function and thereby the quantization noise-shaping behavior. However, any source of non-idealities directly affect the performance of the CT modulator by increasing the integrated in-band noise which causes a degradation in the final SNR.

Among these non-idealities there is the finite operational amplifier's gain A_{dc}. This limit affects both low-pass CT and DT modulators since the zeros of the NTF are pushed inside the unity circle, thus reducing quantization noise attenuation in the signal band. Fortunately, for medium resolution the required gain is well affordable so that the limit is not normally a real concern. Other sources of errors are the finite gain-bandwidth product (GBW) and the slew-rate of active blocks used for the integrators. The slew-rate limit mainly affects the DT modulators. Indeed, low slew-rate sensitivity mainly motivates the choice of CT architectures; the signal injected at the feedback input lasts for a large fraction of the sampling period, thus reducing the op-amp peak output current and its derivative. The finite GBW is the most critical limit for the CT schemes because it delays the transfer of the input signal to the output of single or multiple real integrators [65].

Consider, for example the cascade of a DAC with one and two integrators as shown in Fig. 6.20. The outputs with real op-amps obviously differ from the ones with ideal op-amps and this degrades performance. However, it is possible to incorporate the bandwidth limit into the DAC

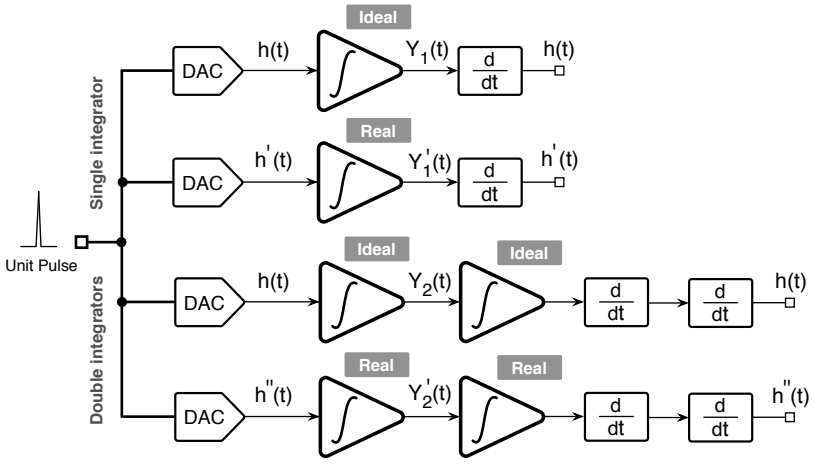

Figure 6.20: Procedure that permits to determine the input referred equivalent DAC impulse response for single and double integrators.

response. For this it is necessary to pass the output waveform of the real integrator(s) through one or more derivations (ideal). The result of the operation is an input referred equivalent DAC impulse response ($h'(t)$ or $h''(t)$) that, used with ideal integrators, would determine the same output of the real integrator counterpart. Fig. 6.21 shows a possible DAC input response and its input referred equivalents for the cascade of one or two integrators and two different op-amp bandwidths ($GBW_1 = 2f_S$ and $GBW_2 = 3f_S$) . Notice that there is a delay that increases as

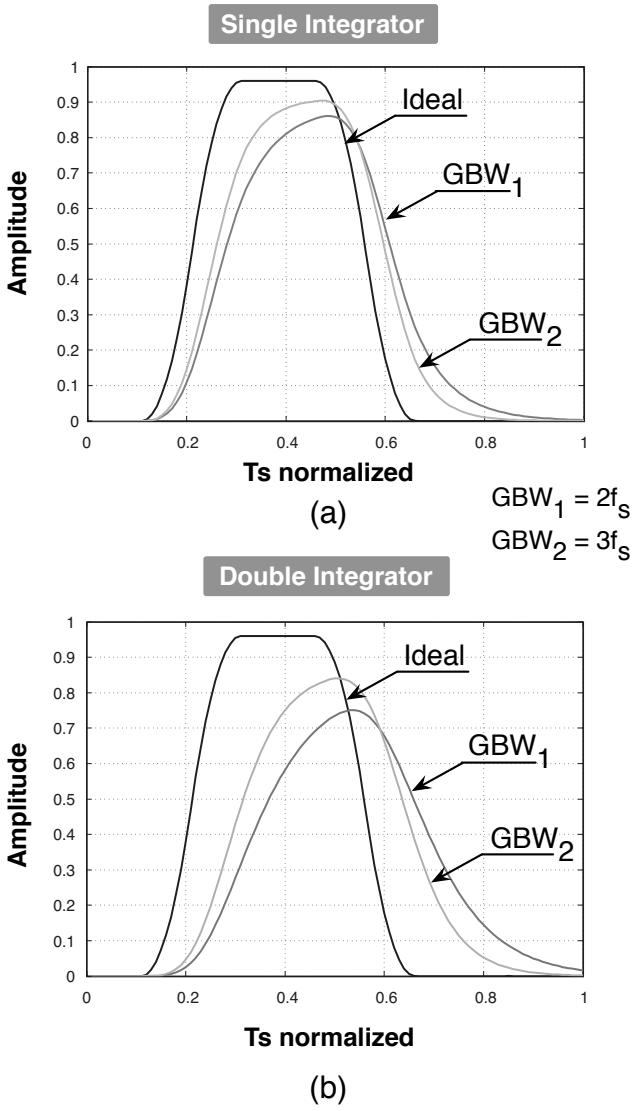

Figure 6.21: Effects of finite GBW on input referred DAC response: a) Single integrator and b) Double integrators.

the bandwidth decreases and is larger for a cascade of multiple integrators.

The results depicted in Fig. 6.21 recommend anticipating the fall time of the DAC responses injected at the beginning of integrator chain in order to avoid a tail in the next clock period. This method obviously requires accounting for different DAC impulse responses as with the method discussed in this paper.

Remember that the design procedure requires estimating multiple integrals of the DAC response. For a real integrator it would be necessary to estimate the input referred DAC response before and to pass that waveform through a single or a multiple ideal integration. Since the estimation of the input referred DAC response includes derivatives, the following ideal integrations compensate for them. Therefore, the needed parameters $h^j_{int,i}$ are conveniently estimated by passing the actual DAC response through real integrators instead of taking the mathematical integration of the input referred impulse response. The operation can be done with a circuit simulator that uses the transistor-level description of the used op-amp.

6.6 Design example

The design method is verified with the multi-bit (4 bit) third order prototype of Fig. 6.14 with all coefficients equal to one. For the equivalent CT architecture, let us use the DAC responses $h_{DAC1}(t)$, $h_{DAC2}(t)$ and $h_{DAC3}(t)$, as shown in Fig. 6.22.

The shape of the DAC was suggested by the consideration made in the previous section. This ensures enough time to avoid injection in the next sampling time and helps in increasing robustness against clock jitter [20], [22], [64].

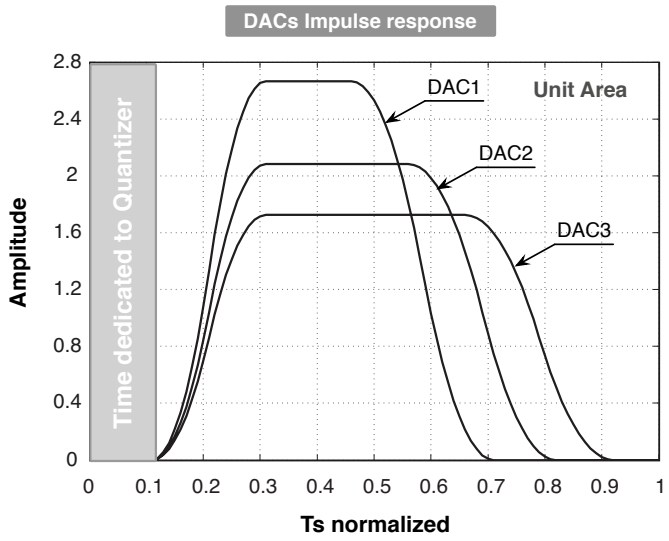

Figure 6.22: DACs impulse responses.

The integral in time domain of each DAC response must be 1, as required by the design conditions. Therefore, we need to verify

$$\begin{cases} \int_0^{Ts} h_1(\tau)d\tau = h^1_{int,1} = 1 \\ \int_0^{Ts} h_2(\tau)d\tau = h^1_{int,2} = 1 \\ \int_0^{Ts} h_3(\tau)d\tau = h^1_{int,3} = 1 \end{cases} \tag{6.27}$$

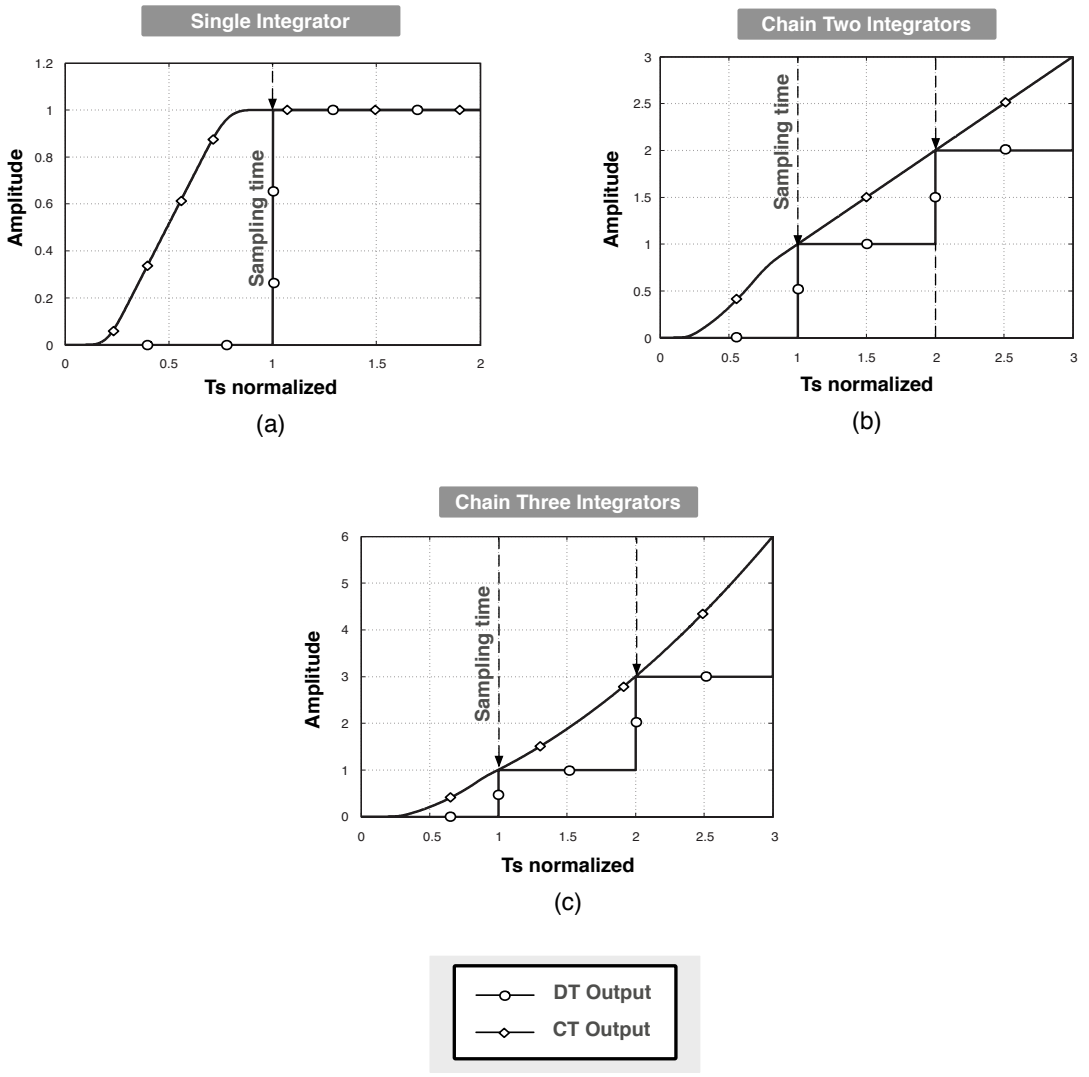

Figure 6.23: Impulse response DT-CT equivalence: a) Single integrator. b) Chain of two integrators. c) Chain of three integrators.

The equivalence of the single integrator branches leads to equation (5) to determine the coefficient α_3^3. Equations (6.20), (6.21) and (6.22) yield the coefficients α_2^2 and α_2^3. We estimate the parameter $h_{int,2}^2$ with its mathematical definition for ideal active elements or by a circuit simulation that uses the DAC2 cascaded with two real integrators for real active elements. For the chain of three integrators it is necessary to use coefficients and equations (6.24) and (6.25). Also in this case real active elements require us to estimate $h_{int,1}^3$, $h_{int,1}^2$ and $h_{int,2}^2$ with circuit simulations.

The resulting waveforms of the CT circuit in the time domain perfectly equal the DT counterparts with zero analog input as required to have equal NTFs, as shown in Fig. 6.23. The obtained coefficients are α_1=*2.777*, α_2= *4.058* and α_3= *3.112*. Using the coefficients provided gives rise to the same NTF and noise spectrum as CT and its DT prototype.

Chapter 7

A Second Order Hybrid CT $\Sigma\Delta$ Modulator with Multi-rate Injections

The chapter explains the synthesis and the design of a new second-order low-pass multi-bit multi-rate hybrid continuous-time (CT) $\Sigma\Delta$ modulator targeting for IEEE 802.15.4 standard. The modulator is implemented with a general purpose 65-nm CMOS technology. The circuit ensures jitter immunity granted by the use of multi-rate switched-capacitor (SC) DACs that further reduce the requirement of the operational amplifier in term of gain, bandwidth and slew-rate. A combination of analog and digital feedforward paths allows to reduces integrators output swing. The modulator provides a measured 10.8 bits of resolution over a signal bandwidth of 1.1 MHz and a spurious free dynamic range (SFDR) of 78 dB. The chip draws 1.1 mW from a 1-V supply, leading to a Figure of Merit (FoM) equal to 280 fJ/conversion-level. Finally, experimental measurements confirm the effectiveness of the architecture.

7.1 ADC Specification for IEEE 802.15.4 standard

A wireless personal area network (WPAN) is a low-range wireless network which covers an area of only a few ten metres. This sort of network is generally used for linking very low cost and low power peripheral devices (like sensors and home appliances) to a main computer, without using a hard-wired connection. The requirements of ultra-low complexity, cost and power for low-data rate wireless communication motivated the definition of the standard IEEE 802.15.4. This standard is designed to be used in a wide range of applications, including home automation (temperature, humidity and monitoring), public safety, automotive sensing (pressure tire monitoring, exhaust gas analysis, etc.), smart badges and all the application that

Table 7.1: Specification targets for ADC

Standard Bandwidth	SNR (dB)	DR (dB)
IEEE 802.15.4 working at 2.4 GHz (1 MHz)	> 60	> 60

requires to sense analog signal (pH level, concentrations of substances, etc.)

The standard allocates 16 channel with a transmission rate of 250Kb/s in the range between 2.4 and 2.4835 GHz, which is the industrial, scientific and medical (ISM) worldwide availability band. The receiver architecture used in this low cost peripheral devices is the direct conversion receiver (DCR), which structure is explained in detailed at the beginning of Chapter 5. The $\Sigma\Delta$ architecture has become very attractive for low-rate low-power CMOS radio receiver, because allow to relax the requirement of the analog building block by transferring a significant part of the signal processing into the digital domain. In this work it is proposed an innovative CT $\Sigma\Delta$ architecture realized in a general purpose 65 nm technology, that targets the IEEE 802.15.4 standard specification. The required performance of ADC are reported in table 7.1.

7.2 Introduction

Continuous-time (CT) $\Sigma\Delta$ modulators ensure implicit anti-aliasing filtering action and, for a given sampling frequency, grant lower power consumption with respect to their discrete-time (DT) counterparts. Since the sample and hold (S/H) in CT schemes is within the loop, the noise transfer function (NTF) filters the S/H inaccuracies, [14]. Unfortunately, the mix of continuous and discrete time elements makes the CT modulators difficult to design and simulate. Furthermore, CT schemes are sensitive to many non-idealities, such as digital-to-analog (DAC) non linearity and clock jitter [20]. The non-linear limit, dominated by the first integrator, is normally solved by using an active RC integrator as first stage, possibly followed by g_mC stages and by using DEM or digital calibration techniques for the linearization of the DACs. The clock jitter sensitivity is resolved by the use of DACs with decaying pulses, like the exponentially shaped waveform generated by a modified switched capacitor circuit (SC-DAC), [22], [66], [67]. If the exponential goes to zero the charge injected by the DAC is jitter independent.

Fig. 7.1 compare how a RTZ pulse and exponential SC DAC pulse, are affected by pulse-width jitter. In this case the resistance is represented by the on-resistance of the switch, like in the case of pure SC, very common in DT $\Sigma\Delta$ modulator. As reported in SCR DAC case, the induced error depends on the settling behavior of the current and consequently by the finite settling speed of integrators due to finite GBW of the OTA. The SNR limitations due to the pulse-width jitter for RTZ and SC DACs, respectively, are expressed as:

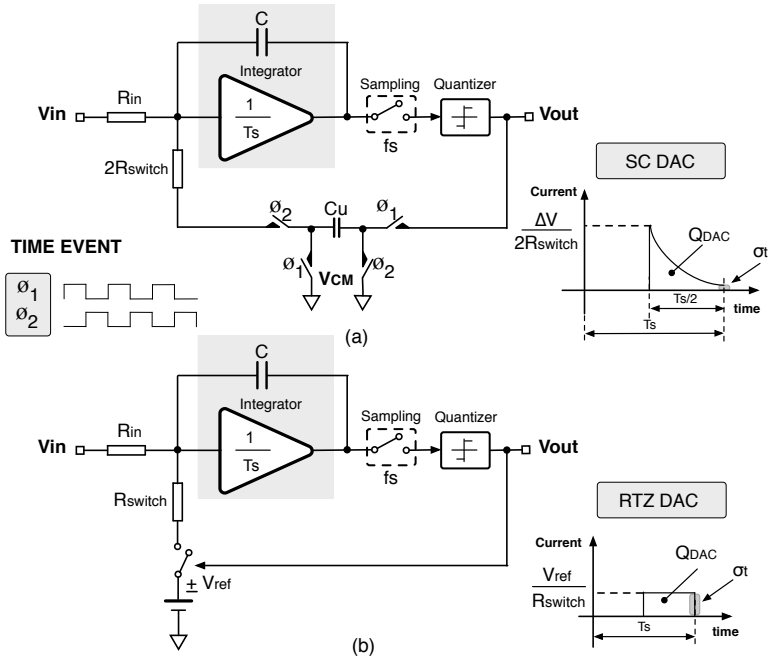

Figure 7.1: Illustrative schematic of clock jitter effect for a single bit CT modulator: (a) with SC feedback DAC. (b) with RTZ feedback DAC

$$S/N_{JitterRTZ} = 10log\left(\frac{\delta OSR}{4 \cdot f_S^2 \cdot \sigma_t^2}\right) \tag{7.1}$$

$$S/N_{JitterSC} = 10log\left(\frac{\delta \cdot OSR}{4 \cdot f_S^2 \cdot \sigma_t^2} \cdot \left(\frac{1 - e^{\delta \cdot \alpha}}{\delta \cdot \alpha}\right)^2\right) \tag{7.2}$$

where $\delta$is the duty-cycle of the DAC,σ_t is the rms jitter, while α is related to the settling-time of the current (α=$T_S/(2R_{SWITCH} \cdot C_U)$). The term $\left(\frac{1-e^{\delta \cdot \alpha}}{\delta \cdot \alpha}\right)^2$ represents the jitter sensitivity improvement from RTZ to a SC feedback DAC [67].

The use of an hybrid integrator with a resistance on the signal path and a SC scheme for realizing the DAC avoids jitter dependency but causes errors if the op-amp bandwidth is finite and the slew-rate limited. The two real dependencies give rise to a linear and a non-linear error. Since a linear error is equivalent to integrator gain error, the main concern is for the non-linear term. This chapter analyzes the limit that causes non-linearity and proposes method for its reduction or cancellation. The most effective solution is the use of a multi-rate hybrid scheme.

7.3 Hybrid Continuous-Time ΣΔ Modulator

Fig. 7.2 shows a hybrid continuous-time ΣΔ modulator. The continuous-time path made by the resistance R_1 gives rise to the integration of the input signal, V_{in}. The feedback path is

a switched-capacitor (SC) network made by switches with on-resistance R_{on}. Let us suppose $C_1 = C_2$ and gain of the integrator equal to 1. It results $R_1 C_1 = T_S$. The capacitance C_L accounts for the capacitive load of the next stage and the compensation capacitance of the op-amp. Immediately after phase Φ_2 rises, the op-amp does not react and the virtual ground and output voltages change just because of the capacitive coupling established by C_2, C_1 and C_L. The virtual ground and output voltage become

$$V_{vg} = V_{DAC} \frac{C_2}{C_2 + C_1 C_L/(C_1 + C_L)} = \alpha V_{DAC} \tag{7.3}$$

$$V_{out} = V_{DAC} \frac{C_1 C_2/(C_1 + C_2)}{C_L + C_1 C_2/(C_1 + C_2)} = \beta V_{DAC} \tag{7.4}$$

where V_{DAC} is the voltage of the DAC.

After there is a transient of output and virtual ground voltages associated to the integration of the charge of C_2 into C_1. If the input voltage is zero, the virtual ground goes to zero, otherwise it settle to about $V_{vg}(\infty) \approx V_{in}/(g_m R_1)$ (g_m is the transconductance gain of the op-amp).

The transients depend whether the operational amplifier is in slew-rate or not. When the input differential voltage is higher than $\sqrt{2}V_{ov}$ (V_{ov} is the overdrive voltage of the input differential pair), the input stage is completely unbalanced and the output current and the bias conditions and the used scheme determine the current at output of the op-amp. Typically the current is less than a given value, I_{SR}. If V_{vg} is lower than $\sqrt{2}V_{ov}$, the waveforms change

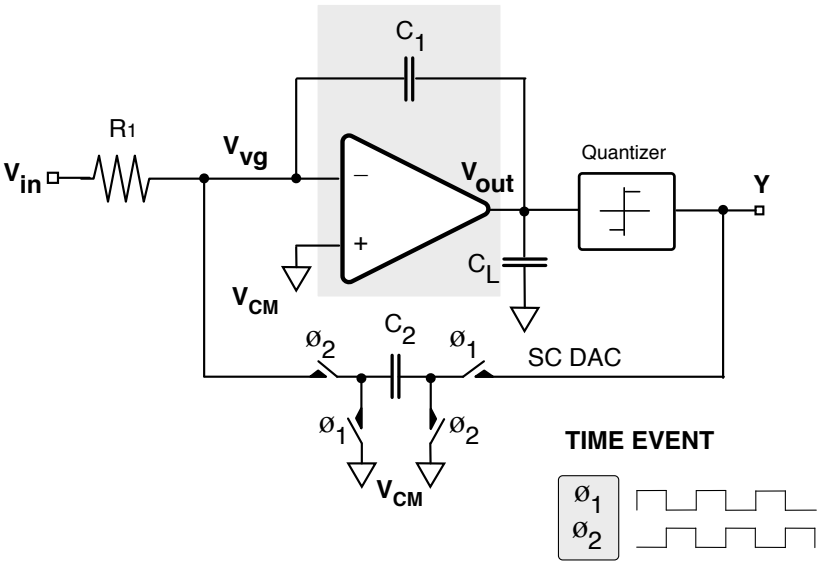

Figure 7.2: Block diagram of a hybrid CT modulator.

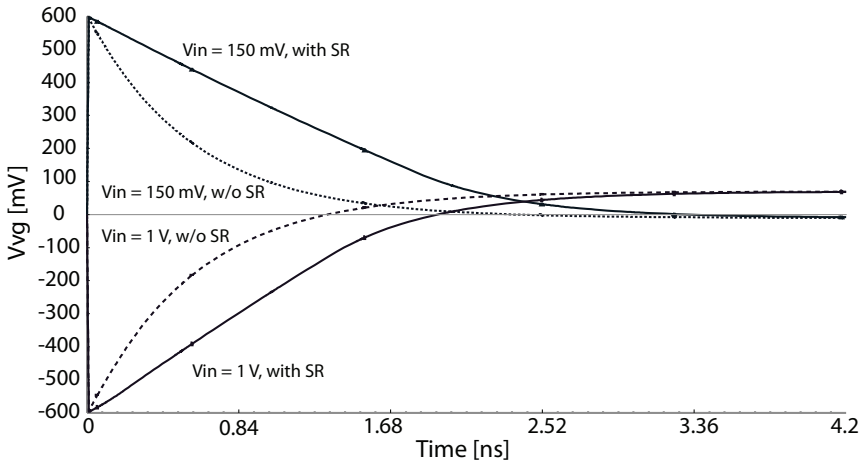

Figure 7.3: Simulated virtual ground waveforms with and without slew-rate limitation for two input voltage values.

exponentially (supposing to model the op-amp with a single pole model). If V_{vg} exceeds $\sqrt{2}V_{ov}$, the op-amp goes in slewing until the input difference becomes lower than $\sqrt{2}V_{ov}$. Until then, the waveforms change almost linearly, then they decrease exponentially.

In the slew-rate condition $|I_{out}| > I_{SR}$. Accounting for the current from resistance R_1, the discharge current of the SC capacitor C_2 is approximated by

$$I_{C_2} = \frac{V_{in} - V_{vg}}{R_1} - C_L \frac{dV_{out}}{dt} - I_{SR}; \tag{7.5}$$

that, together with other equations, describes the transient during slewing. Fig. 7.3 shows the virtual ground waveform for two values of input voltage (V_{in} = 1 V and V_{in} = 150 mV), supposed constant, and a positive or negative DAC output ($|V_{DAC}|$ = 1 V). The figure also shows waveforms for the case of infinite slewing. They are exponentials that approximately settle to $V_{vg}(\infty)$. For finite slew-rate, the linear part ends at a time that depends on the value of the input voltage.

What is relevant for the study is that the virtual ground does not remain at a constant level, Ort2, and this changes the current of the input resistance by $(V_{in} - V_{vg})/R_1$. The consequence is an extra fraction of injected charge, ΔQ, inversely proportional to the the input resistance, R_1.

Supposing $t = 0$ the beginning Φ_2 and $\bar{t}$ the time at which the op-amp exits from the slewing condition, the lost charge is

$$\Delta Q_{SR} = \int_0^{\bar{t}} \frac{V_{vg}(t)}{R_1} dt. \tag{7.6}$$

When the op-amp is in the linear region the virtual ground settles to $V_{vg}(\infty)$ exponentially with a time constant, τ_1, that depends on capacitances and transconductance gain of the op-

amp. To be precise, we should also account for the on resistance of the switches. If the period of phase 2 is long enough, the virtual ground voltage reaches its asymptotical value. ΔQ in the interval $(\bar{t} \cdots T_S/2)$ can be calculated as

$$\Delta Q_{exp} = \int_{\bar{t}}^{\infty} \frac{V_{vg}(t) e^{-(t-\bar{t})/\tau_1}}{R_1} dt = \frac{\sqrt{2} V_{ov} \cdot \tau_1}{R_1} \tag{7.7}$$

being $V_{vg}(\bar{t}) = \sqrt{2} V_{ov}$. If the virtual ground voltage does not settle to zero, the integral of equation (5) further depends on V_{in} because $\bar{t}$ affects the integral (5). The total extra charge injected into the virtual ground becomes

$$\Delta Q_{slew}(V_{in}) = \Delta Q_{SR}(V_{in}) + \Delta Q_{exp}(V_{in}) \tag{7.8}$$

If the value of $V_{vg}(0)$ established by equation (1) is lower than the slew-rate limit, the virtual ground voltage starts immediately an exponential decrease, giving rise to a lost charge equal to

$$\Delta Q_{no\text{–}slew} = \int_{0}^{\infty} \frac{V_{vg}(0) e^{-t/\tau_1}}{R_1} dt = \frac{\alpha V_{DAC} \tau_1}{R_1}. \tag{7.9}$$

Since $\Delta Q_{no\text{–}slew}$ does not depend on the input voltage, the error corresponds to a DAC gain error. Even if the virtual ground does not settle to zero $\Delta Q_{no\text{–}slew}$ is constant. Moreover, the SC capacitor C_2 is not completely discharged. The error is constant and can be incorporated in a DAC gain error and it can be easily compensated for by tuning the injection coefficient.

From the above, we notice that what is relevant is the non-linear part caused by slewing and input voltage. It is zero if the op-amp does not slew and is

$$\Delta Q_{n-lin} = \Delta Q_{slew}(V_{in}) - \Delta Q_{slew}(0) \tag{7.10}$$

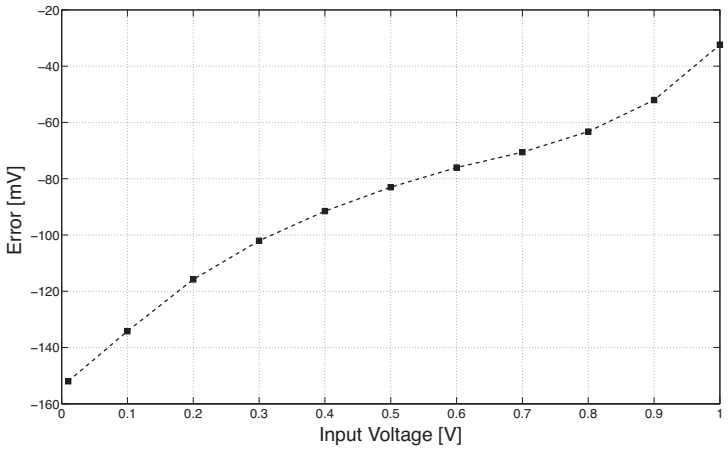

Figure 7.4: Simulated error as a function of the input voltage.

in case of slewing.

The error becomes strongly non-linear when the slewing period becomes a significant fraction of the injection phase and depends on design parameters and clock frequency. Moreover, the transition from "off" to "on" determined by switches made by MOS transistors smooth the waveforms and reduces the peak value of the virtual ground swing. The behavior, studied at the transistor simulation level, gives rise to the non-linear error as a function of V_{in} of Fig. 7.4, obtained with $f_s = 100$ MHz, $g_m = 250$ μS, $I_{SR} = 50$ μA, $C_1 = C_2 = 0.5$ pF, $C_L = 1$ pF, $R_{switch} = 100$ Ω, and $V_{DAC} = -1$ V. The error is calculated as the difference at the end of the injection between waveform with infinite and finite slew-rate. For negative values of the input voltage, the behavior is symmetrical.

7.4 Design Solution: Multi Rate DAC

The use of a SC-DAC limits the error due to the clock jitter ([22], [20]), but the simple theory of the previuos paragraph indicates a non-linear error when the op-amp goes in the slewing conditions. Therefore, a generic design guideline is to avoid slewing even if this is obtained at the expenses of a reduction of the op-amp bandwidth. To overcome the above drawbacks, in this architecture is proposed a new method called multi-rate injection. This approach, in the case

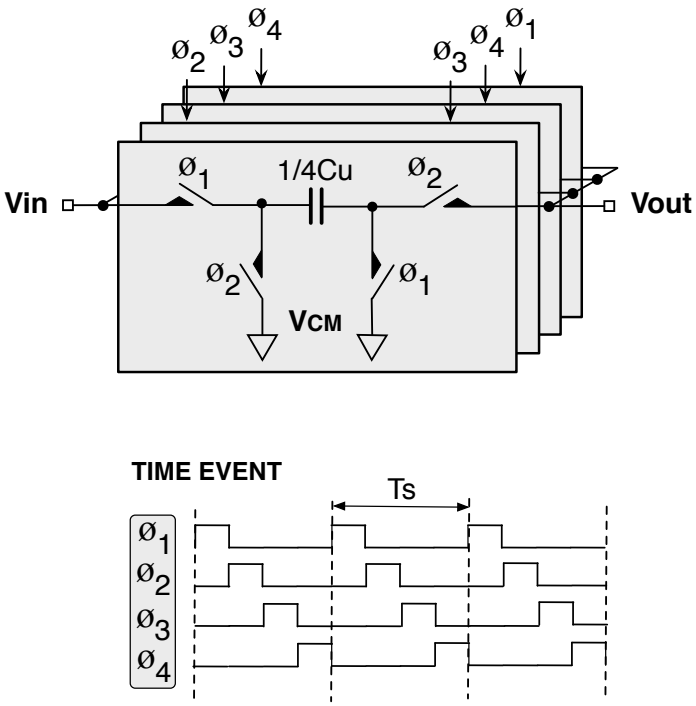

Figure 7.5: Scheme of the multi-rate DAC.

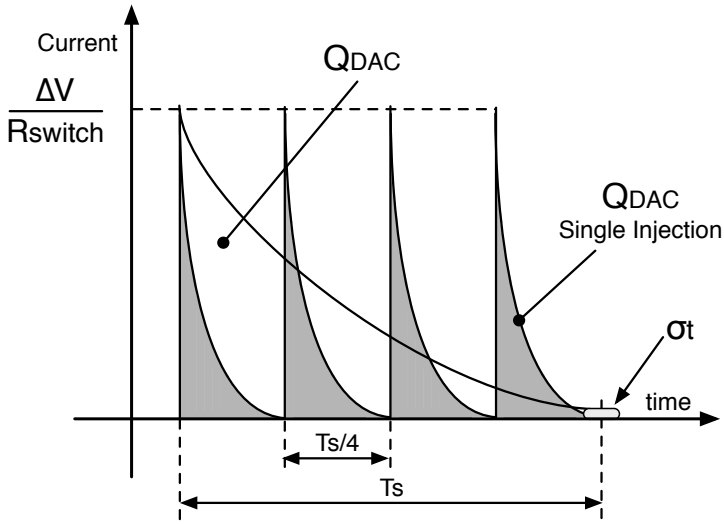

Figure 7.6: Conceptual diagram of the mutli-rate injections.

of switched capacitor DAC consists in injecting the foreseen charge in N equal time slots within a single sampling period, as conceptually shown in Fig. 7.5 for the case of four injections. The sharing of the charge related to a single feedback pulse in successive four weighted packages, like shown in Fig. 7.6, allows to relax the effect of finite gain due to limited charge injection required at each step.

Since the injecting capacitor is C_2/N (where N is the number of multiple injection), replacing this value in eq. 7.3 leads to a significant reduction of the virtual ground swing. Depending on the op-amp performance, it is possible to choose the number of injections that keep the op-amp off of slewing. The optimum number of injections depends on the DAC signal and available op-amp overdrive voltage. The number of required injections can dynamically diminish if the DAC is multi-bit. Fig. 7.7 shows the simulated error, calculated with the same parameters used for Fig. 7.4 (but with double transconductance), as a function of the input voltage. The simulation uses a number of injections equal to 4. The non-linearity is significantly reduced.

The small variation of the virtual ground is beneficial in the CT modulator, where the permanent integration of continuously changing waveforms requires high linearity for all time. In the DT counterpart the large glitches in the virtual ground due to the switched capacitor injections are not a real issue, because what matter is the settled value, while in CT modulator each movement of the virtual ground affects the final integration.

As well known, the dynamic response of an analog integrator to an input step (charge injection from a SC DAC) is limited by the slew-rate SR and the gain-bandwidth product GBW of the operational amplifier. For example, a large step gives a long slewing period and reduce the time left for the esponential settling. On the contrary, a small step leads to a

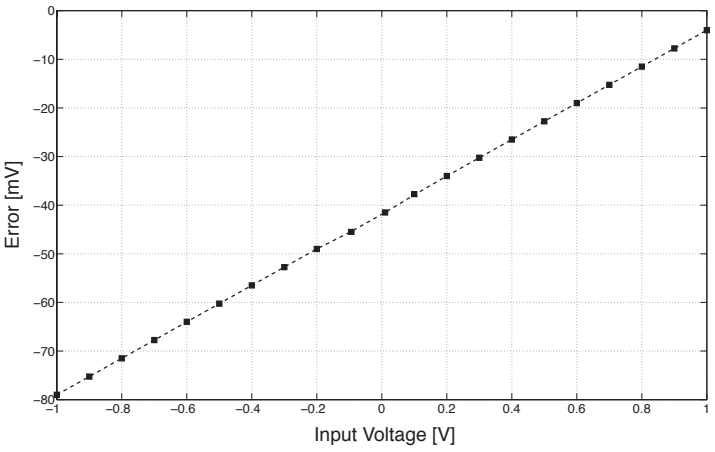

Figure 7.7: Simulated error of the multi-rate DAC (4 injections).

minimum slewing time and a longer period for settling. The integrated error during the slewing period (area A of Fig. 7.8) is $\frac{\Delta V_{in}^2}{SR} - SR \cdot \tau^2$, in which τ equals $\frac{1}{\beta \cdot 2\pi \cdot f_T}$ where β is the feedback factor and f_T the gain-bandwidth product. The integrated error during the settling period (area B of Fig. 7.8) is $\Delta V \cdot \tau$. If $\Delta V_{in} < \Delta V$ there is no slewing phase and the integrated error is proportional to the step size, while for large step, the error increases with the square of the step.

In this way, avoiding the slew-rate step response, the charge injection could be corrected simply by tuning properly the feedback coefficient to compensate the loss of charge compared

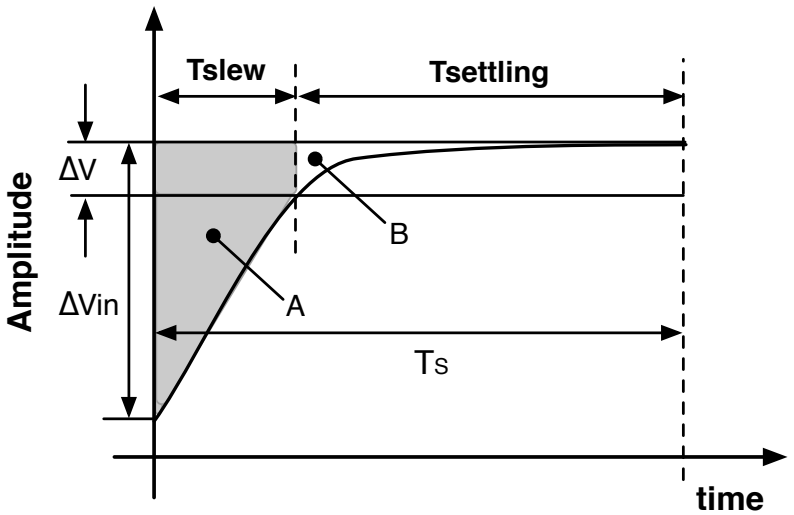

Figure 7.8: Scheme of the DAC with controlled rise time.

to the ideal SC case. This technique ensures low sensitivity to clock jitter and reduces the effect of the finite gain of OTA and limited slew-rate, with benefit in terms of improved linearity.

7.5 Chip Architecture

The design of a continuous-time ΣΔ modulator is normally done starting from a discrete-time prototype. Fig. 7.9 shows the discrete-time scheme used to design this continuous-time modulator: a multi-bit second-order ΣΔ. The key feature of this design consists in reducing the output swing of both integrators. The use of analog input feedforward keeps low the swing of the first integrator output node, P_1. A digital assistance network, which processes the quantized version of the input signal, diminishes the swing of P_2. The digitally assisted technique applied to a discrete-time ΣΔ modulator (Fig. 7.9) is proposed in [45]. The method enables the use of low supply voltage and allows decreasing the number of comparators in the quantizer, thus relaxing the second integrators requirements and saving its power. Neglecting the terms related to the quantization noise, ϵ_q, P_2 is equal to Xz^{-1}. To reduce the output of the second integrator, this term needs to be deleted. Therefore, $H_1(z)$ holds $0.5(1 - z^{-1})$. To keep the modulator signal transfer function (STF) unchanged, $H_2(z)$ is a simple delay. The compensation is realized in the digital domain after the quantizer. Notice that this operation cancels also the effect of the quantization noise of the extra quantizer, ϵ_{q1}.

The transformation of the scheme in Fig. 7.9 in its continuous-time version uses hybrid integrators with a resistance on the signal path and SC feedback DACs. The method, normally,

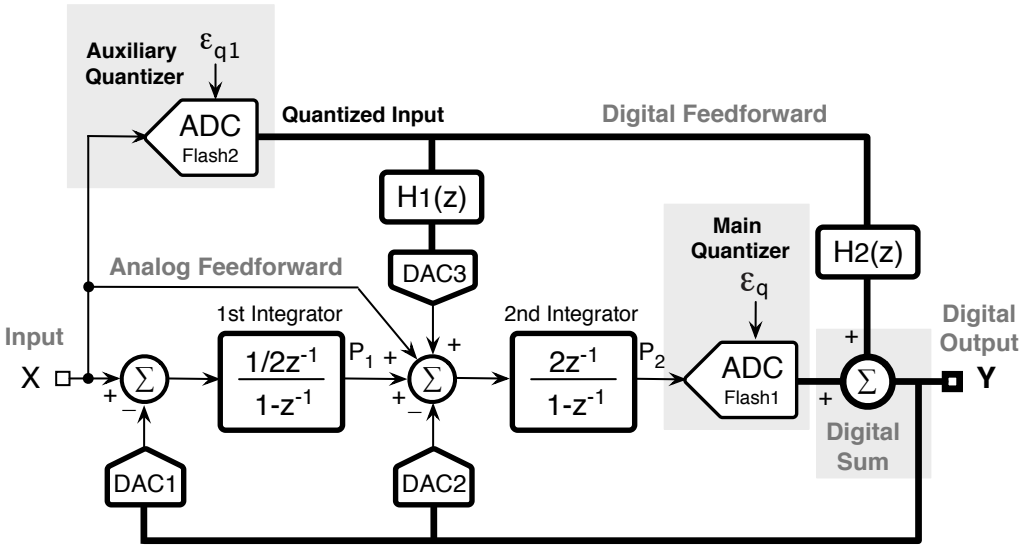

Figure 7.9: Block diagram of the second order DT ΣΔ prototype.

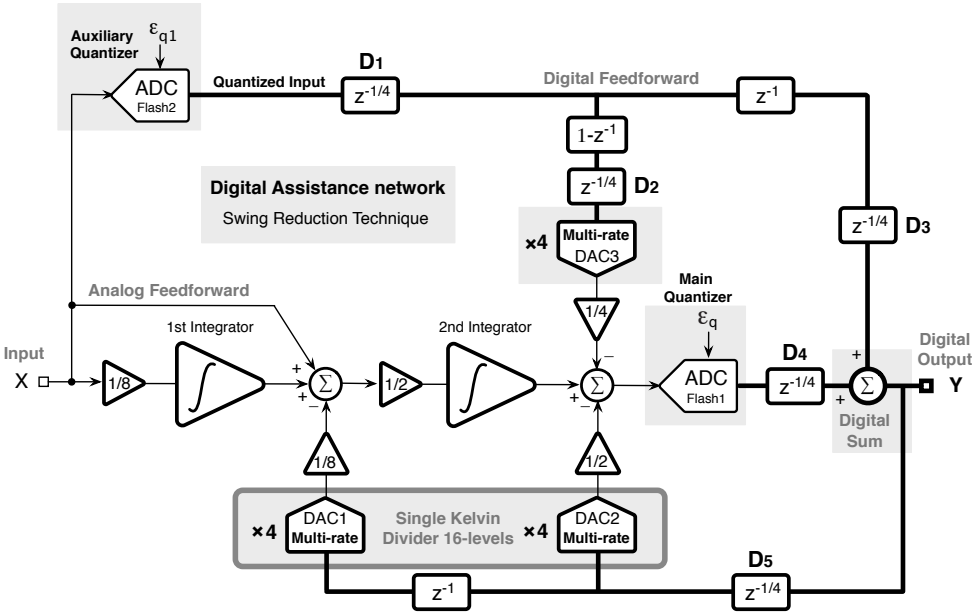

Figure 7.10: Block diagram of the proposed CT ΣΔ modulator.

causes errors because the op-amp goes in slewing condition. Indeed, it is the combination of finite gain and limited slew-rate that gives rise to a linear and a non-linear error. Since a linear error is equivalent to integrator gain error, the main concern is for the non-linear term which arises when the op-amp goes in slewing mode. To overcome the non-linear error associated with the slewing mode of the operational amplifier, this design uses multi-rate DACs.

Fig. 7.10 shows the block diagram of the CT modulator. The presence of a digital assistance network in a continuous-time modulator is not conventional and this makes not straightforward the DT-CT transformation. Extensive simulations at the behavioral level allow optimizing the coefficients values. Having, as mentioned above, 4 DAC injections leads to the availability of $z^{-1/4}$ delays. D_1 and D_4 account for the conversion time needed by the two flash ADC, while delays D_2 and D_3 provide the time required for the digital subtraction in the block $(1 - z^{-1})$ and the digital addition at the modulator output, respectively. Notice from Fig. 7.10 that the injections of the DACs start after half sampling period the flash conversion. This means that the first two injections of the multi-rate DACs belong to the actual sampling period while the remaining two are shifted in the following one. This is not a limit due the reduced value of the feedback coefficients, as extensive simulations verify the stability of the modulator in any operational conditions.

The best trade-off between swing reduction effectiveness, power consumption, resolution and complexity suggests to use 4 bit ash converter for both quantizers, realized with FLASH converters architecture. Fig. 7.11 shows the simulated (at transistor level) output voltage swings

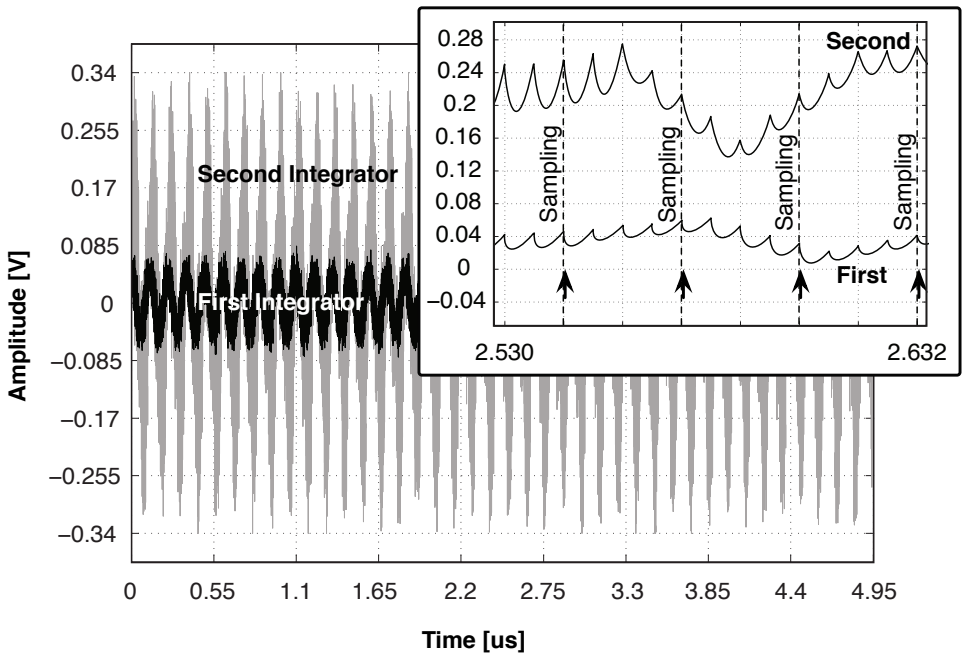

Figure 7.11: Simulated output voltages of both integrators.

of both first and second integrator with a full scale input signal of -1 dB_{FS}, (the voltage full scale is $V_{FS} = 1$ V). The analog feedforward and the digital assistance network keep the two nodes within ±0.08 V and ±0.34 V with respect to the common mode voltage. The inset shows a detail of the two waveforms where the 4 injections due to the multi-rate DACs are visible. The reduced swing outlines the benefit of the digital assistance network that allows us to diminish the number of comparators of the main 4-bit FLASH converter from 15 to 8. Moreover, the trade-off between power consumption, area, number of DACs and complexity design imposes to implement DACs with shared Kelvin divider in order to increase the final power efficiency. In particular the 4 bit DACs (DAC 1 and DAC 2) share a single Kelvin divider which generates the needed 16 differential references voltages, while the 4 bit DAC3 uses another single Kelvin in order to avoid cross-talk effect between the input and the output of the modulator (with a reasonable penalty of increased power consumption).

The choice to generate differential levels allows to completely delete the error caused by gradient in the value of each resistors used in the resistive string, as explained in Chapter 5. The use of resistive divider needs good matching accuracy, which could be obtained by increasing the dimension of each resistor and with very carefully layout. This allows to reduce the harmonic distortion and does not require digital calibration or dynamic element matching (DEM) techniques.

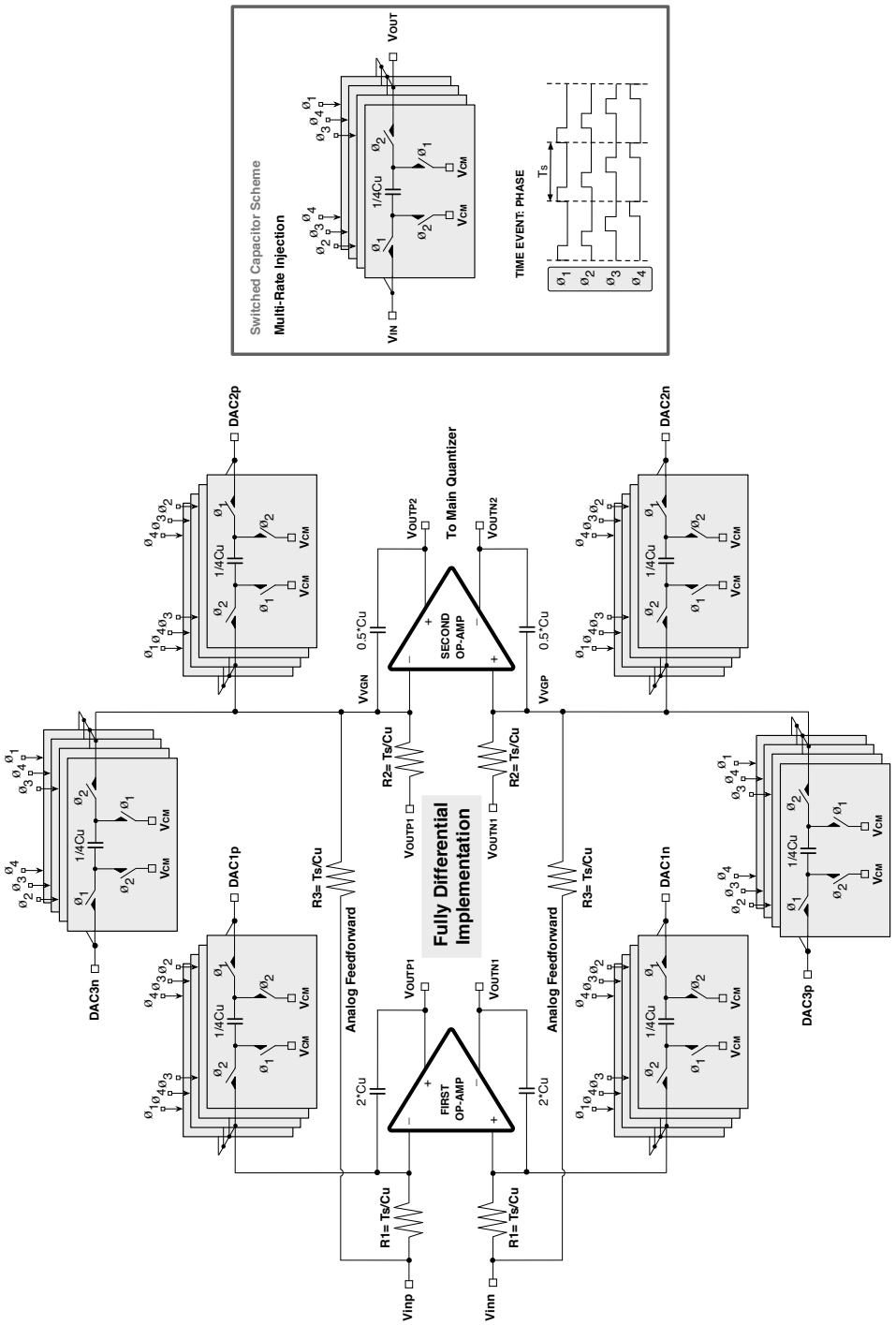

Figure 7.12: Fully differential implementation of the CT modulator.

7.6 Circuit Implementation of the ΣΔ architecture

The fully differential circuit implementation of the structure designed with a 65-nm 1 V general purpose CMOS technology is shown in Fig. 7.12. The integration of the signal path is realized with active RC Integrators due to better linearity and parasitic insensitivity. The input resistor R performs a linear V/I conversion if the virtual ground is fixed. Otherwise, in real implementation the finite amplifier's gain gives rise to small residual voltage fluctuation of the virtual ground that influence the integration, degrading the final linearity. The adoption of the multi-rate technique with 4 injection realizes two benefits: avoids the slewing conditions of the operational amplifier and relaxes the movement of the virtual ground also with limited DC gain of operational amplifier realized with a 65 nm technology. Moreover, performance enhancements can be achieved by increasing the area of integrated polysilicon resistors and by ensuring the matching between input resistors. The use of MOM capacitor as integration

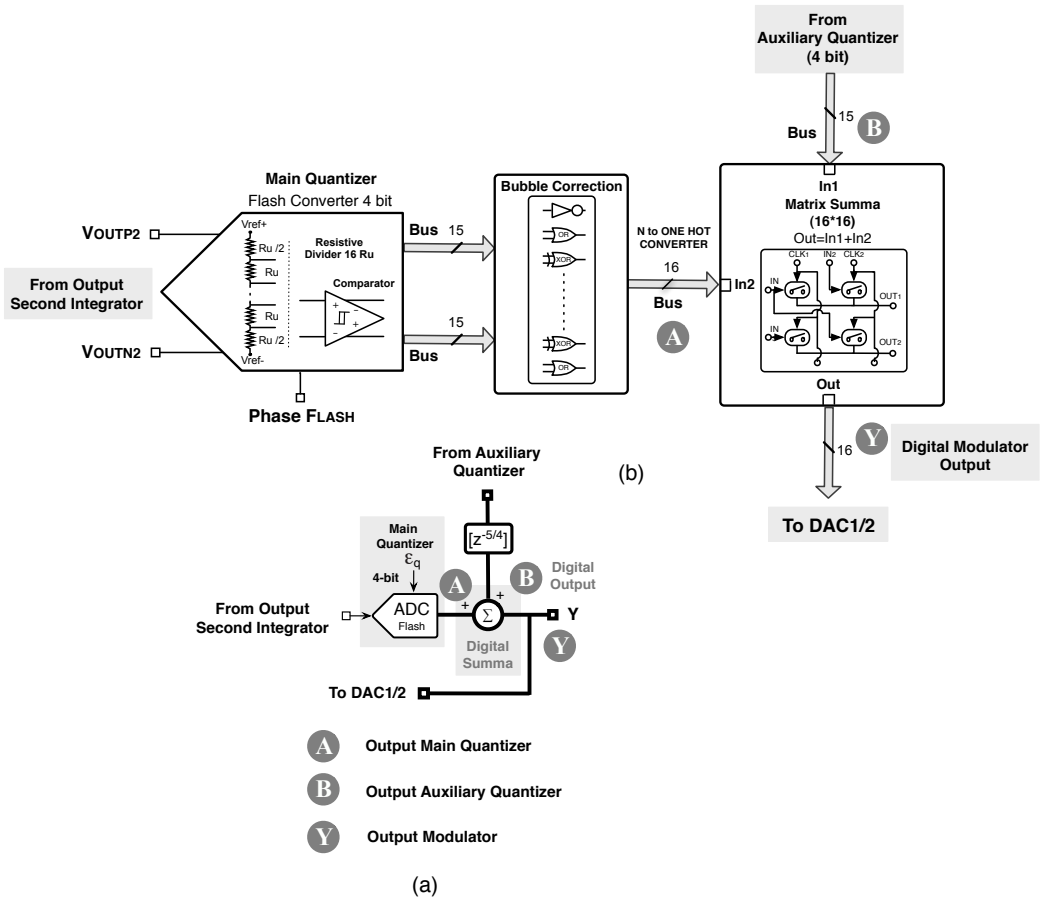

Figure 7.13: Block diagram of the main quantizer and digital processing of the addition.

capacitor is not critical due the presence of the negative feedback loop and inherent linearity of MOM capacitors. The thermal noise limit determines the resistances on the signal path, 47.35 kΩ (from theoretical calculation the value of Cu is equal to 600 fF). The integration capacitors of the first and second op-amp are 1.2 pF and 0.3 pF, respectively (Fig. 7.12). The unity capacitance of the SC circuits is equal to 75 fF.

The multi-rate injection technique is realized with the switched capacitor network reported on the right side of Fig. 7.12. It use four equal capacitor of value Cu/4 (150 fF) operating in a ping-pong fashion thanks to the controlling phases ϕ_1, ϕ_2, ϕ_3 and ϕ_4. Each phase lasts a quarter of the sampling period.

The differential output of the second integrator is than processed by the main flash converter as shown in more detailed in Fig. 7.12. The main quantizer uses only 8 comparators thanks to the swing reduction of the second integrator. Anyway the structure implements all the 15 comparator in order to avoids settling problems at the start-up: after the settling of the

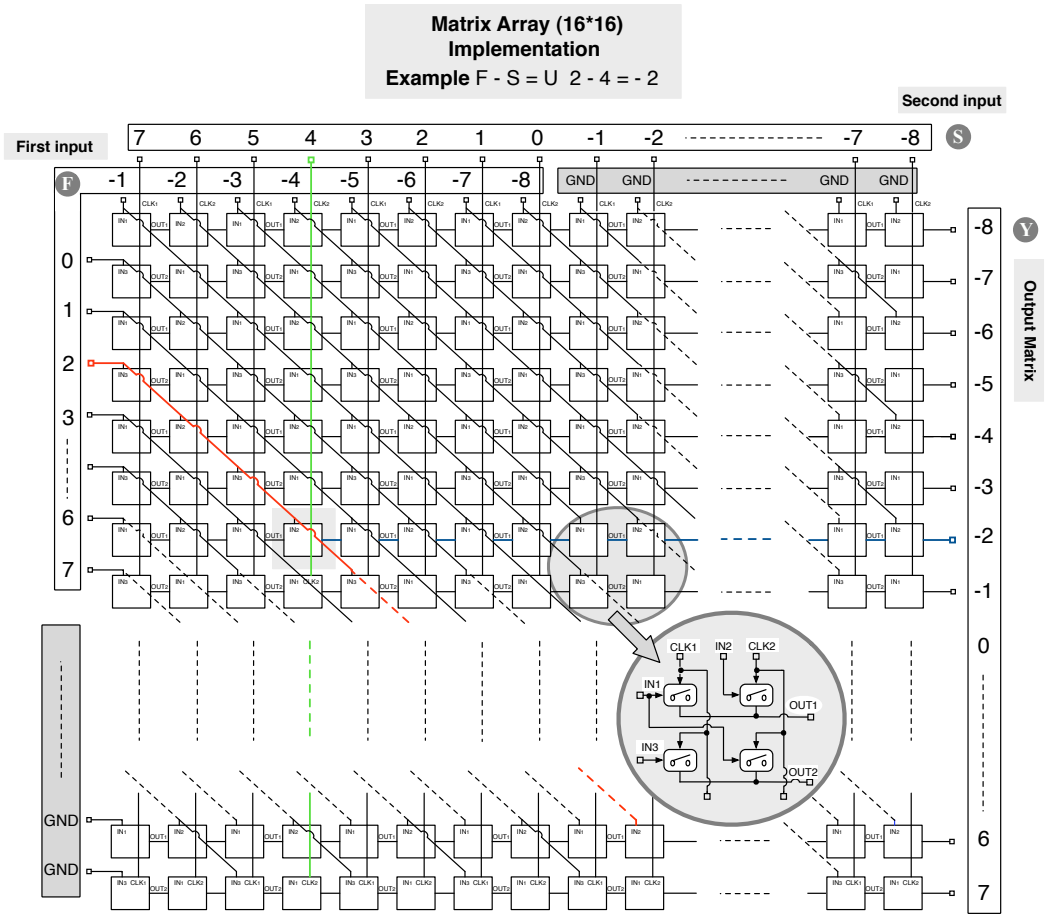

Figure 7.14: Block diagram of the matrix used for the digital subtraction.

internal nodes all the useless comparators are completely turned off. The thermometric code generated by the main flash is simultaneously converted to one-out-of-N code and corrected of possible bubble errors ([55], [56]) by a digital circuit, named bubble correction, realized with simple logic gates. The same circuits is also used for the 4-bit auxiliary quantizer. The digital output bus of the main quantizer (indicated with the digit A) and the delayed quantized one of the input voltage due to the auxiliary quantizer (indicated with the digit B) are summed in digital domain with an array of 16×16 switches as reported in the ΣΔ architecture discussed in Chapter 5 (Fig 7.13). The output data of the matrix is the output of the modulator, used to that select the needed reference voltages of the Kelvin divider shared by DAC1 and DAC2.

The reduction of the output swing of the second integrator and the cancellation of the quantization error e_{q1} demand the implementation of the digital filter with transfer function $H_1(z)$. The operation could be done efficiently by using the same switched array matrix used to obtain the summa, but rearranged for subtraction operation, as shown in Fig 7.14. In Fig 7.15, the digital output bus of the auxiliary quantizer (indicated with the digit B) is send to both input of the subtraction matrix. The path with delay z^{-1} is simply realized with two register of flip-flop D, working in opposite phase. The output data of the subtraction matrix is used to

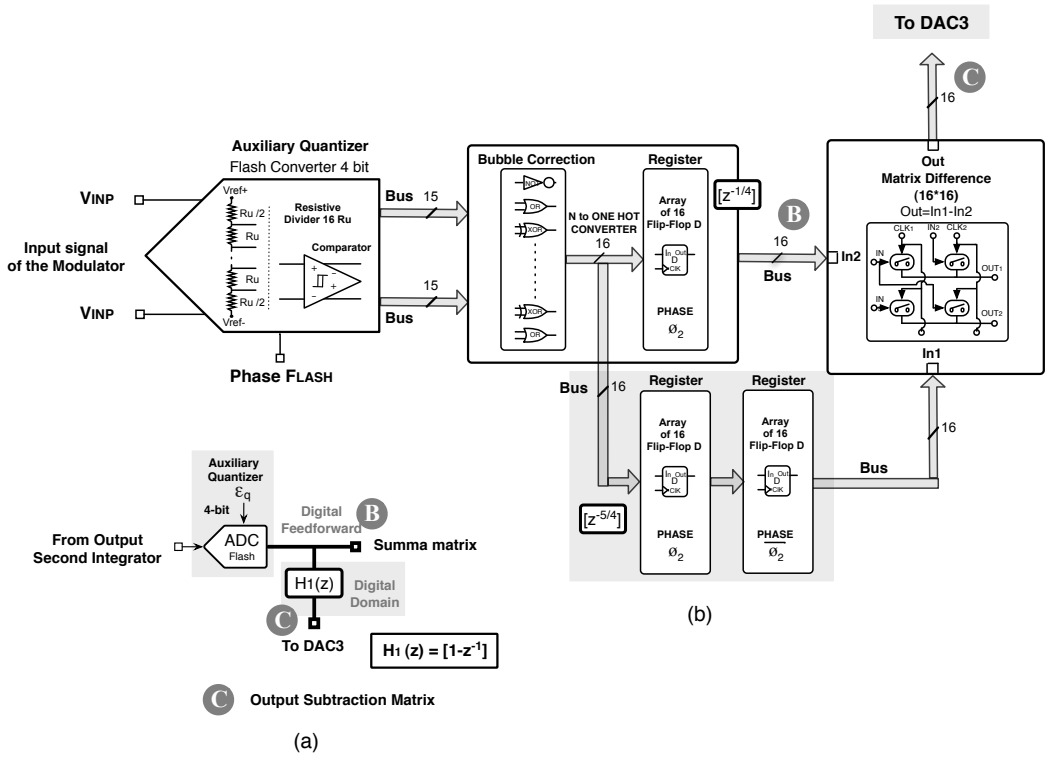

Figure 7.15: Block diagram of the auxiliary quantizer and digital processing of the subtraction.

that select the needed reference voltages of the Kelvin divider of DAC3.

Resistive Kelvin dividers that use 15 nominally equal resistances realize the two DACs. Unity resistances of 440 Ω with increased area achieve the required matching accuracy without the need of trimming or calibration ([48], [49]). Thus, the power consumed by the DAC depends on the value of the unity resistance and not on the area. Since the converter uses a single resistive divider to generate the differential voltages, first order gradients error are compensated for, as explained in Chapter 5.

7.6.1 Operational amplifier scheme

The dynamic response of an analog integrator to an input step is limited by the slew-rate SR and the gain-bandwidth product GBW of the operational amplifier. For example, a large step gives a long slewing period and reduce the time left for the esponential settling. Slewing effect divides the op-amp output settling (t_s) into large signal response (t_{slew}) and small-signal response ($t_{settling}$). Considering both region, the relationship between GBW and t_s results [68]:

$$GBW = \left(\frac{n}{\beta} + \frac{V_{swing}}{V_{OV}}\right)\frac{1}{t_s} \tag{7.11}$$

where β id the feedback factor, while V_{swing} and V_{OV} are the maximum output voltage swing and the overdrive voltage of the input differential pair, respectively. The value n is a time-constant coefficient, defined as the number of required time constants in which the final settling error due to finite bandwidth is less the required e_{rr}. This parameter could be expressed as:

$$n = \frac{t_{settling}}{1/(\beta GBW)} = ln\frac{1}{e_{rr}} \tag{7.12}$$

The relationship 7.11, valid for a single stage operational amplifier, predict that the reduction of the output swing needs less GBW for a given settling time. Anyway, eq. 7.11 is still valid also for more complex operational structure, like two o three stage operational [68]. The overdrive voltage of differential input pair of the first operational amplifier is 85 mV, while for the second stage is 76 mV. The first and second integrator op-amp have the same scheme (Fig. 7.16), but use different bias currents to meet the slew-rate and bandwidth requirements. The structures were implemented with a general purpose low threshold voltage 65 nm technology suitable for digital application but not for analog one, because very sensitive to short channel effects and (but cheaper compared to the technology used for the modulator of Chapter 5). A PMOS cascode stage (M_4 and M_5) increases the output resistance of the first stage and allows to reduce the effect of channel length modulation on the input differential pair while a level shifter (M_9 and M_{14}) drives the output stage. The transistors M_9 and M_{14} have the body connected to the source in order to reduce "body effects". A conventional $R_C C_C$ (zero nulling resistor with capacitor) compensation ensures stability. Both first and second stage use a continuous-time common mode feedback network: in the first stage V_{CMFB1} is realized by using a current

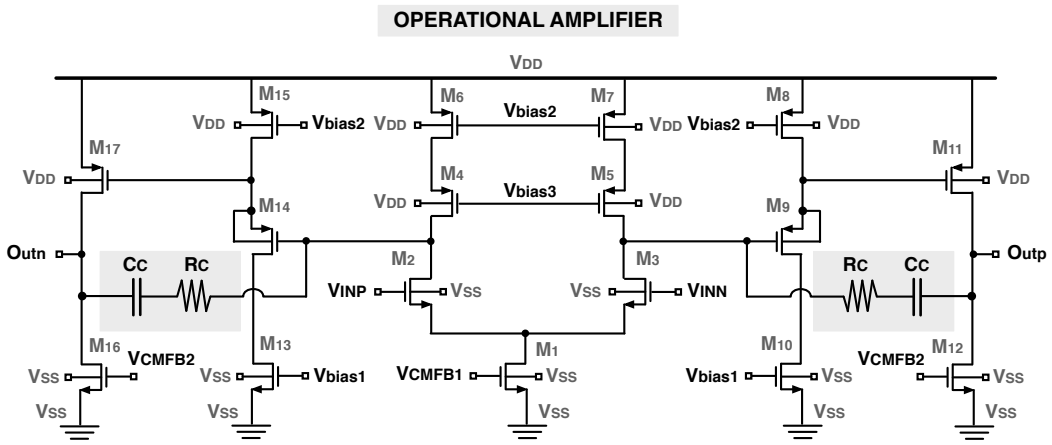

Figure 7.16: Schematic diagram of the two stages Miller compensated operational amplifier.

mirror with adjustable mirror factor thanks to a pair of transistors working in triode region, as illustrated in [69]. In the second stage the difference between the common mode of the outputs (sensed with two high value resistors) and a fixed voltage equal to $V_{DD}/2$ is amplified with an additional amplifier and connected to the gate of transistors M_{12} and M_{16} (V_{CMFB2}): this allows to control the quiescent current of the output stages. The additional amplifier has a gain of 20 dB and a bandwidth of 600MHz. Table 7.2 summarizes the op-amps key features. Notice that the digital assistance network branch on the second op-amp requires slightly augmented bandwidth and not demanding slew-rate. The low gains match the architecture low sensitivity to the finite gain granted by the low voltage swing of integrators. The feature was verified with simulations.

Feature	First Op-Amp	Second Op-Amp
Supply Voltage	1 V	1 V
Bandwidth	180 MHz	195 MHz
Phase margin	62 deg	61 deg
Slew-Rate	14 V/μs	17 V/μs
Gain	36 dB	34 dB

Table 7.2: Summary of the performance of operational amplifiers used in the second order CT ΣΔ modulator.

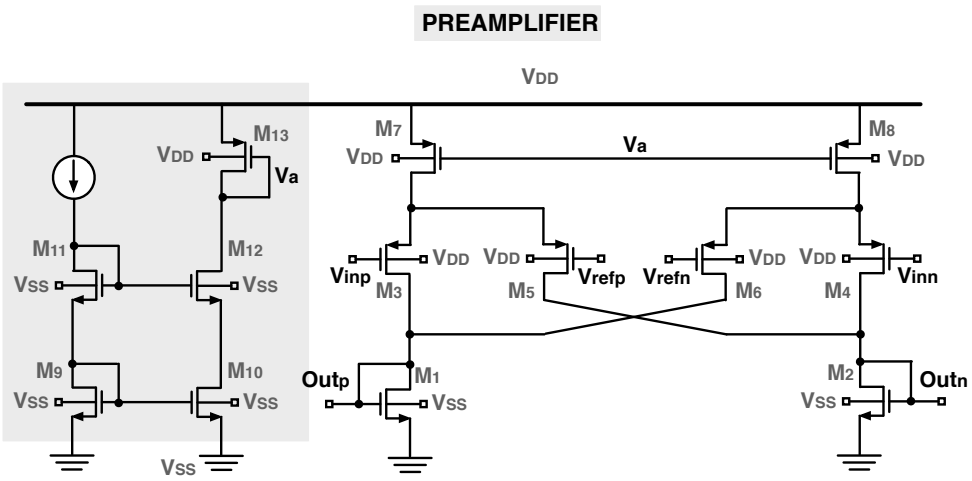

Figure 7.17: Schematic diagram of the preamplifier stage of the comparator.

7.6.2 Comparator scheme

The implemented comparator is a conventional static latched comparator, composed of a differential preamplifier (Fig 7.17) with low gain followed by a regenerative latch circuit (Fig 7.18). The regenerative latch presented in Fig. 7.18 is similar to the one used in the previous modula-

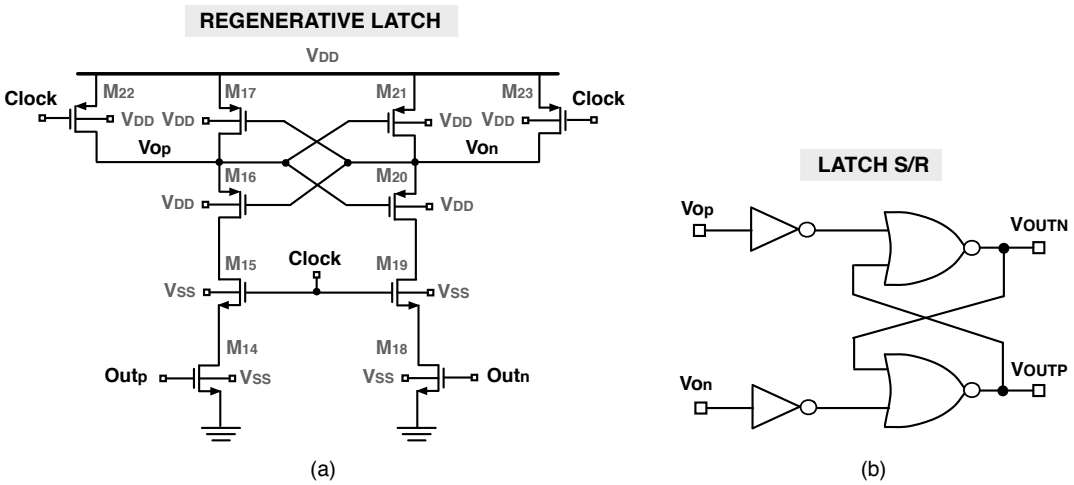

Figure 7.18: Schematic diagram of the regenerative latch and of the S-R latch.

tor presented in Chapter 5. When the C_{LOCK} is low transistors M_{15} and M_{19} are opened and the output of the latch are closed to V_{DD} through transistors M_{22} and M_{23}.

When the C_{LOCK} goes high, immediately the switches connected to the output latch are opened (M_{22} and M_{23} are off, while M_{15} and $M_{19}$are on) and the regeneration phase starts. The differential currents come from differential amplifier input stage (M_3-M_5 and M_4-M_6) with active load (M_1/M_2) are mirrored to the output nodes through current mirrors (M_{14}/M_{18}). This latch has a very small regenerative time constant due to presence of two back to back CMOS inverters that regenerate the output voltage to full scale digital levels thanks to positive loop. The set-rest latch allow to memorize the digital data for the entire clock period. The presence of transistors (M_{14}/M_{18}) isolate the input stage from the transitions of the regeneration nodes reducing the kickback noise.

The comparator is designed to have, in the reset phase (C_{LOCK} low), an output voltage that is interpreted as the high logic value, due to presence of the transistors M_{27} and M_{29}. The overall current consumption is 3 μA. The sensitivity of the comparator is equal to 1 mV, while the time to conversion is only 500ps. The reference of both flash ADCs are generated by a resistive strings consuming 30 μW.

7.6.3 Switch Design

For switched capacitor circuits at low voltages, the carefully design of switch is mandatory. Two problems afflict the design of switch: channel charge injection and clock feedthrough. The first

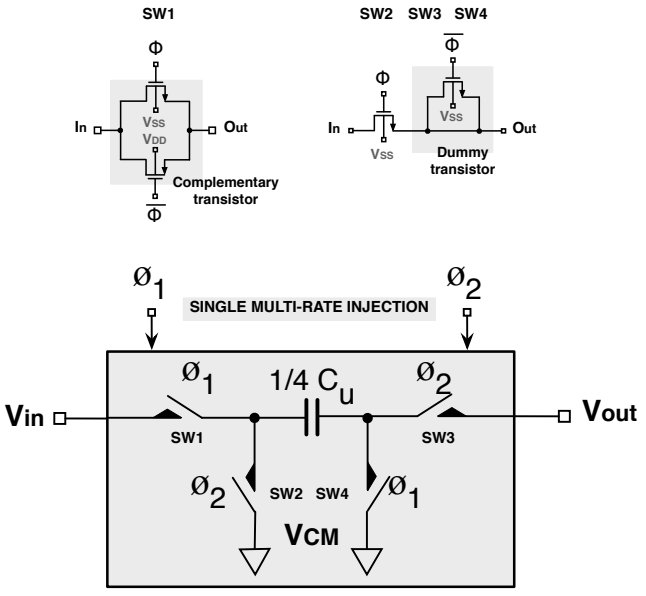

Figure 7.19: Switch implementation in multi-rate injections technique.

is related with the stored channel charge dissipated when the switch turned off [70]. The charge injection contributes three types of errors in sampling ciruicts: gain error, dc offset and non-linearity due the dependence between input voltage and charge injected. The first two terms are not a real problem because can be corrected and the third is relaxed due the reduced swing. The charge injection could be mitigated with the use of dummy transistor, which driven by the delayed and complemented phase can absorb this charge. Normally the dummy transistor has the same length but half width of the main switch (the effectiveness of the approach is around 80 % [12]). SW2, SW3 and SW4 (Fig. 7.19) are implemented with dummy solution that also allows to suppress the effect of the clock feedthrough, due to capacitive coupling between clock transitions and gate-drain or gate-source overlap capacitance. The trade-off between speed and precision resulting from charge injection is independent of the switch width and of the sampling capacitor but is inversely proportional to the square of the channel length, so the deep submicron technology helps to improve this figure of merit.

The input switch SW1 is realized with complementary transistor in order to reduce the value of resistance and removes the constant offset. The problem of clock feed-through is also compensated with the bottom plate sampling technique, as explained in [12].

7.6.4 Layout Design

The realization of the layout follows the same guidelines explained in Chapter 5. Thus, the clock tree is placed at the bottom of the device and all generated clock phases and digital control signals run along the borders of the analog core. The heart of the core has been reserved to analog circuitry, including the two operational amplifiers, the resistance of integrators, the feedback switches capacitors network and the two string resistive DACs. The flash converters are positioned near the respectively DACs, while the switching summa and subtraction matrix are placed closet the ADCs. The layout of a 65 nm analog block requires very carefully attention on the placement of dummies in order to mitigate the WPE and STI issues (as explained in Chapter 1) and increase the final symmetry of the structure.

The proposed third order CT ΣΔ modulator has been integrated using a 65 nm, 7-metal, GP (general purpose for digital design) step, CMOS technology, courtesy offered by ST Microelectronics from Castelletto, Milan (Italy). The active chip area is $904 \times 360\ \mu m^2$. Fig. 7.20 shows the ΣΔ modulator floor plane with a zoom of the active area and the numbered list of the building block.

7.6.5 Board Design

For a proper testing of the modulator performance a four layer board (Fig. 7.21 (a) and (b)) has been designed with Eagle software, by using the design guidelines presented in the appendix A. Analog and digital power supplies and grounds are separated into distinct planes (Fig. 7.21 (c) and (d)), while all the supplies line and the voltage reference lines of the chip are decoupled

with SMD capacitor. As explained in Appendix A, all the decoupling capacitance must be placed as close as possible to the package pin in order to reduce the inductance of the lines.

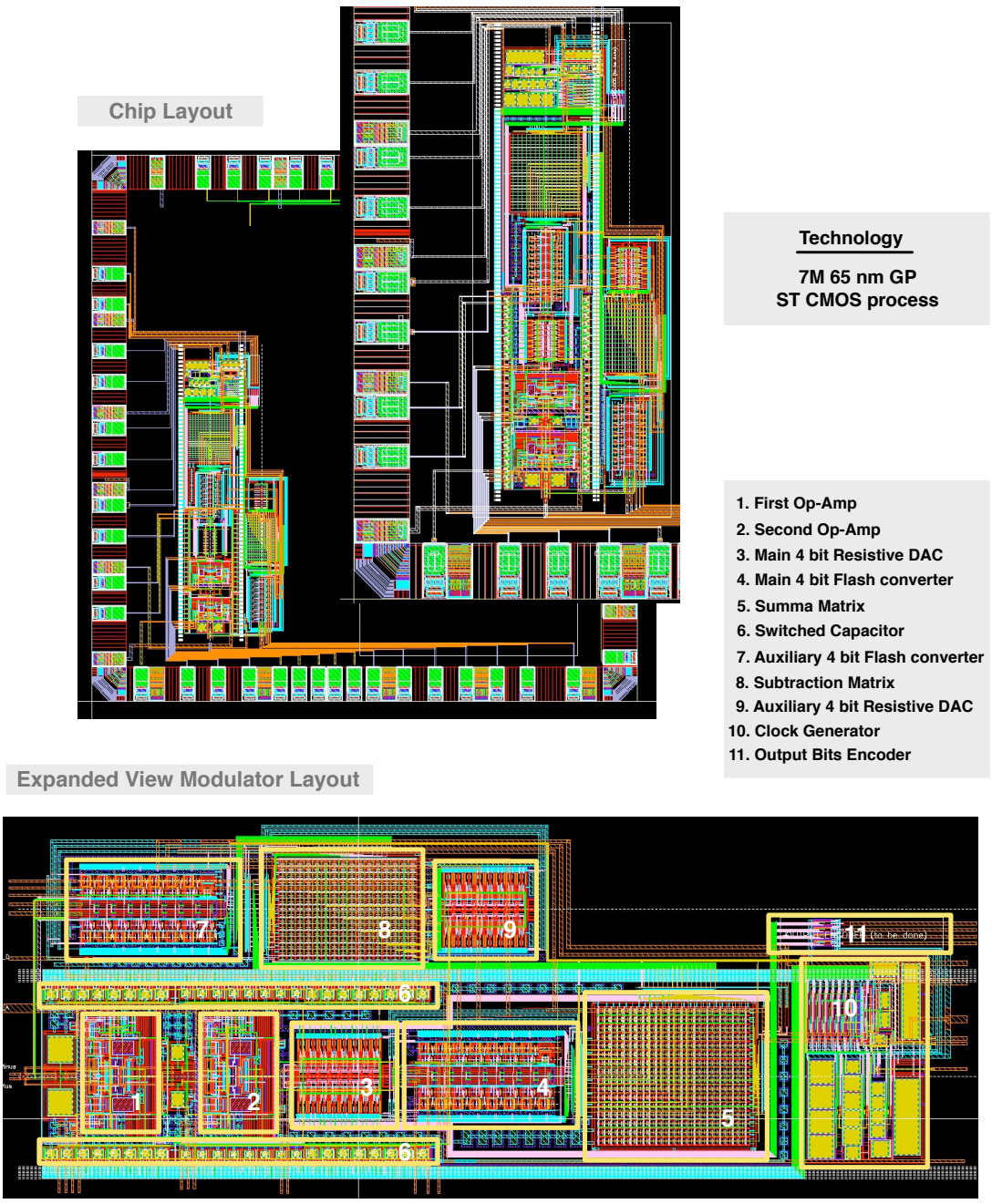

Figure 7.20: Top level of the second order CT ΣΔ modulator.

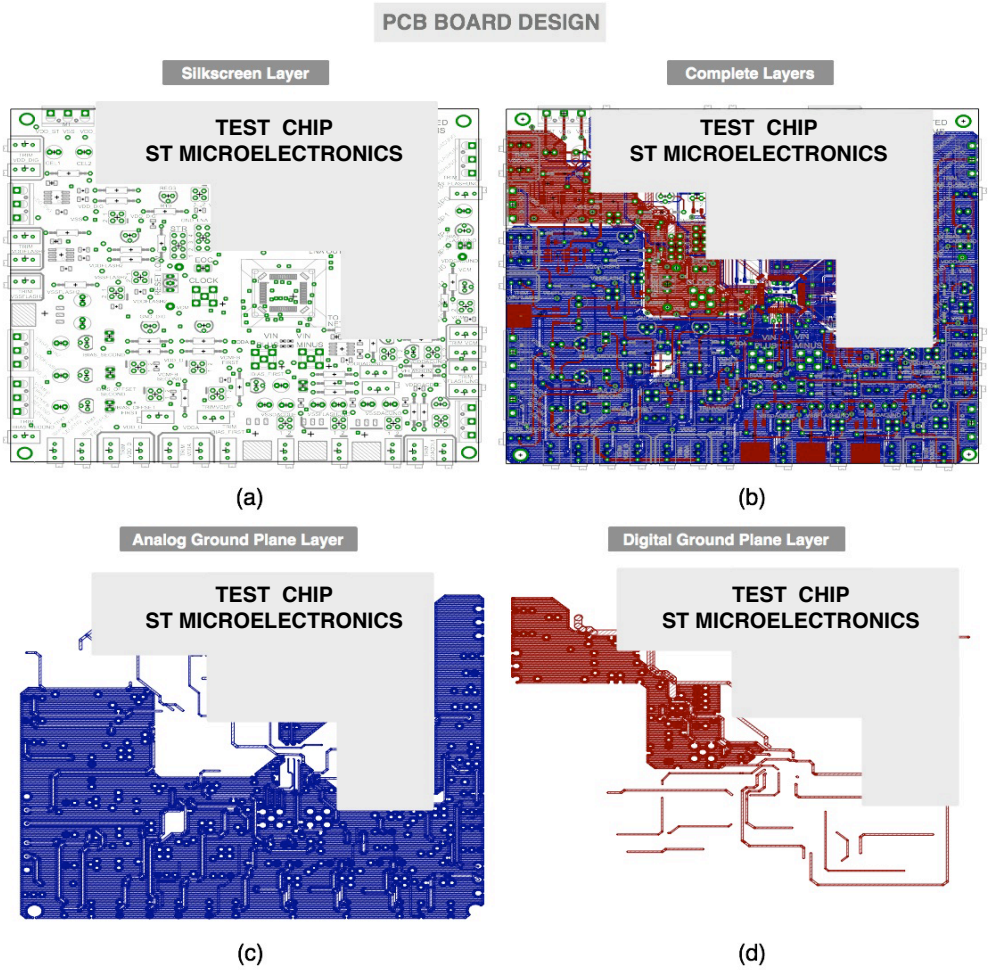

Figure 7.21: Board design for the second order ΣΔ modulator: (a) Silkscreen layer and all layers. (b) Analog ground layer. (c) Digital ground layer.

The voltage reference of the DACs and flash converters and all the currents bias are generated and decoupled off chip. This allows to study how the performance of the modulator integrated in the test chip, can change in order to optimize the power consumption. The covered part is related to the biasing network of the test-chip part developed by STMicroelectronics, which is integrated on the same die of the proposed modulator. Input signals and clock signal were generated with an external generator. Digital output bit stream is captured by a mixed-signal oscilloscope and post-processed with Matlab to elaborate the spectrum.

7.7 Experimental Results

The second-order CT ΣΔ modulator has been integrated using a 65-nm CMOS technology with 7 metal levels and metal-oxide-metal (MOM) capacitors. The die, whose microphotograph with layout in the background, is shown in Fig. 7.22, has an active area equal to 904μm × 360μm.

The reference voltages are external to the circuit; no internal buffer is used to enforce the strength of the references. The nominal supply voltage is 1 V.

The nominal sampling frequency, f_S, is 35.2 MHz. With an OSR = 16, the signal bandwidth is 1.1 MHz. Fig. 7.23 shows the measured SNDR as a function of the input signal frequency. The peak of the SNDR is 67 dB and it is almost flat over the entire signal bandwidth. Fig. 7.24 shows the output spectrum with a 652.61-kHz input signal at -0.75 dB_{FS} (FFT with 8192 points). No spurious tones are visible. However, reducing the input frequency down to 83.2 kHz reveals a third and a fifth harmonic whose amplitudes are -79 and -85 dB_{FS}, respectively. The measured SFDR is, hence, 78 dB. Fig. 7.25 shows the measured SNDR as a function of the input signal amplitude. The use of the digital assistance network extends the input signal range up to -0.75 dB_{FS}. The dynamic range is 70 dB. The total power consumption of the modulator is 1.1 mW. The partial contribution are: first operational amplifier 290 μW (26.36%), second operational amplifier 325 μW (29.55%), 22 comparators 85 μW (7.73%), resistive DACs

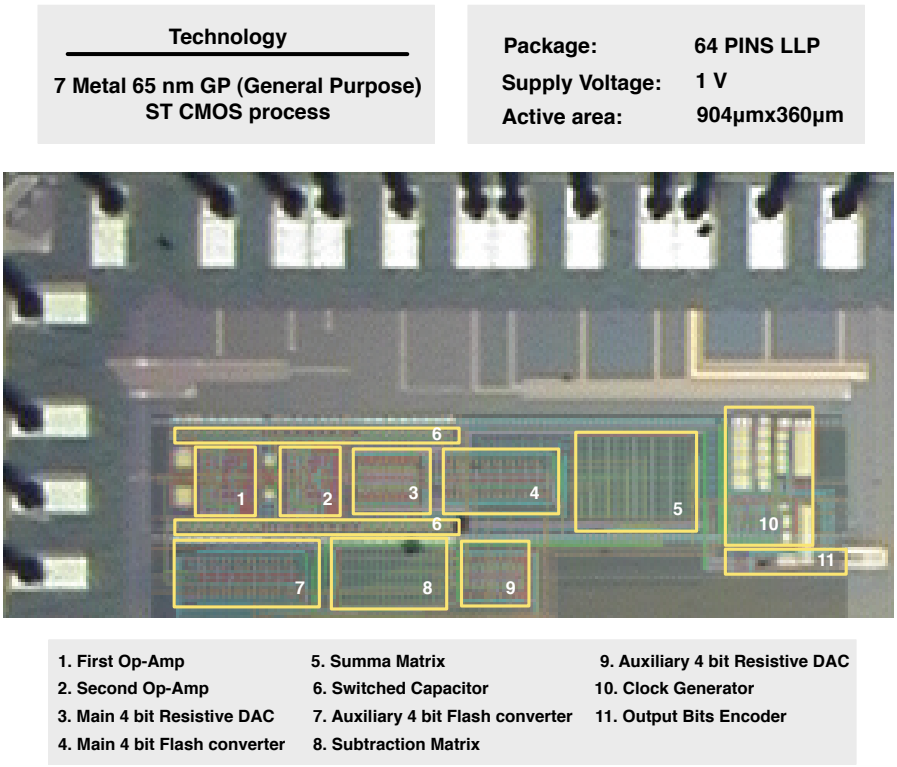

Figure 7.22: Chip microphotograph of the second order CT ΣΔ modulator.

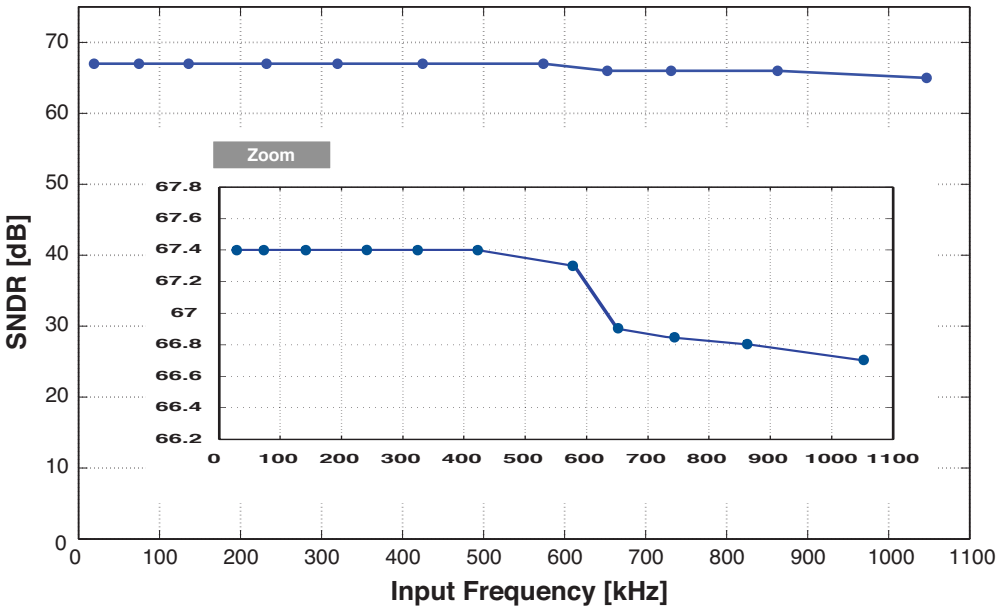

Figure 7.23: SNDR as a function of the input signal frequency.

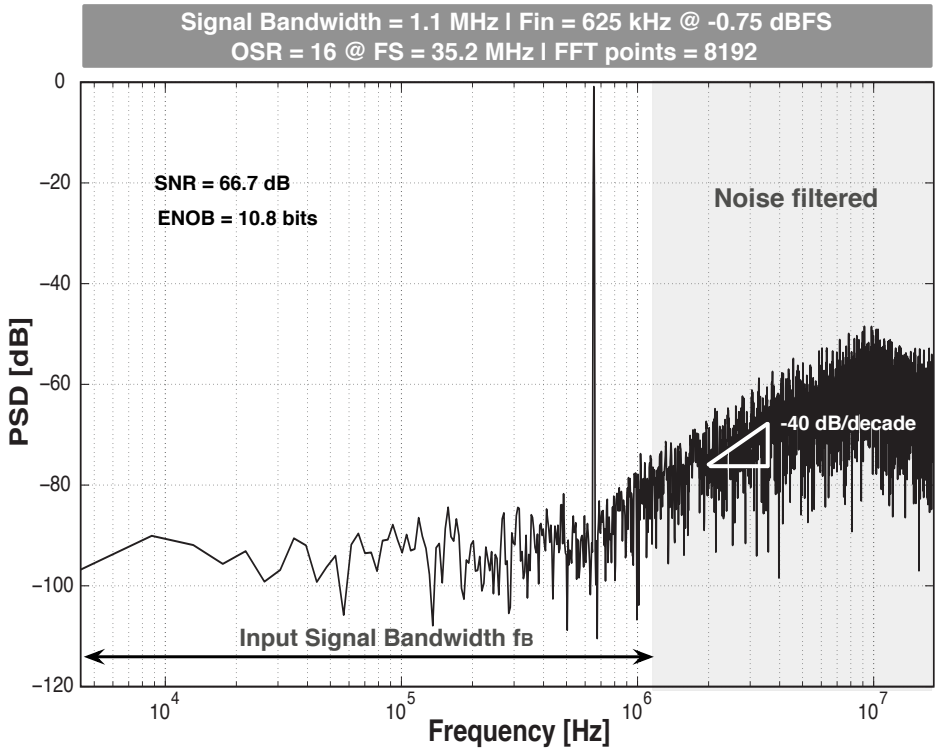

Figure 7.24: Measured power spectral density of the proposed modulator.

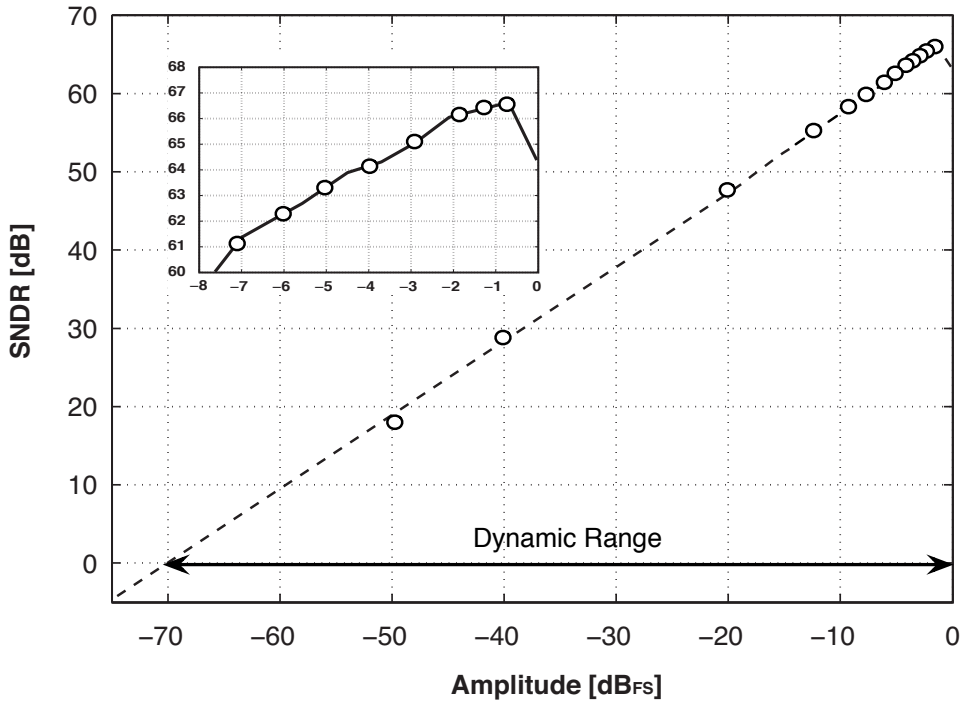

Figure 7.25: Measured SNDR versus signal amplitude for OSR=16.

consume 300 μW (27.27%) and the digital logic 100 μW (9.09%). The total count excludes the power consumption of the output digital buffers that drive the output pad to realize the 4-bit encoder that transform the output modulator data from the one out of N code to binary digital code. The achieved Figure of Merit (FoM) is consequently 280 fJ/(conversion-level).

The experimental results are in line with the recently published performances as reported in Table 7.3, but the SFDR is 10 dB better. The power efficiency of the proposed second order CT $\Sigma\Delta$ modulator verifies the effectiveness of the architecture. The performance summary of the modulator is given in Table 7.4.

Parameter	**unit**	**This** Work	**Texas In.** 2010 [1]	**ISSCC** 2009 [71]	**ESSCIRC** 2009 [4]	**CICC** 2009 [3]
CMOS technology	nm	65	65	65	65	65
Supply Voltage	V	1	1.4	1.22	1	1.1
Signal bandwidth b_w	MHz	1.1	1.2	2	1	3.125
Oversampling ratio	OSR	16	125	32	56	16
Sampling Frequency f_S	MHz	35.2	300	128	108	100
Order	L	2	2	3	3-1	3
Number of bit in DAC	N	4	1	3	1	3
SNDR	dB	66.7	69	79.07	75.4	64
ENOB	bits	10.8	11.1	12.84	12.23	10.33
Active Area	mm^2	0.27	0.1875	0.084	0.4	0.6
Power Consumption	mW	1.1	1.16	4.52	17	11
FoM	$\frac{fJ}{con-lev.}$	280	200	153	1760	1369

Table 7.3: Comparison of the proposed modulator with other state of the art A/D converters reported in recent years.

Parameter	**Value**
Signal bandwidth b_w	1.1 MHz
Oversampling ratio	16
Sampling Frequency f_S	35.2 MHz
SNDR	66.7 dB
ENOB	10.8 bits
Dynamic Range	70 dB
Power Consumption	1.1 mW
FoM	280 fJ/(conversion-level)

Table 7.4: Summary of the performance of the second order CT ΣΔ modulator.

Chapter 8

High Performance Techniques

8.1 Introduction

This chapter presents the analysis of two new low-power ΣΔ modulator architectures. The first one present the design of a third order modulator realized with only two operational amplifiers. The modulator achieves complex conjugate zeros that allow to increase the signal bandwidth and to obtain a SNR improvement of about 8 dB. Moreover, the design uses a fully digital technique to reduce both amplifiers output swings in order to relax the analog requirements, as discussed in the chapters before. Behavioral level simulations, considering the slew-rate, bandwidth and DC gain limits of the amplifiers, demonstrate the effectiveness of the proposed solution.

The second architecture exhibits a new smart technique that virtually doubles the oversampling ratio of a conventional second order ΣΔ modulator. Accounting for a limited cost, the resolution increases by about 2-bit while power just increases by few percents. Therefore, the FoM diminishes by a factor close to 3.5. Simulation at the behavioral level of the proposed method verifies the operation. Circuit level schemes indicates that the architecture does not requires higher op-amp bandwidth. The method can be used with multi-bit quantizer without requiring additional efforts for the DEM.

8.2 Third-Order ΣΔ Modulator with Complex Conjugate NTF zeros

Today portable communications market demands for high speed and high resolution analog-to-digital converters (ADCs) with severe requirements on power consumption, in order to maintain a longer battery life. Sigma-Delta (ΣΔ) modulators, used for high resolution in audio applications, are more and more addressed when medium resolutions (12-14 bits) and signal bandwidth in the MHz or tens of MHz range are required. To meet specifications multi-bit third-order

modulators are good and efficient architectural choice. Low oversampling ratio (OSR) and the use of low voltage swing operational amplifiers keep low the power consumption.

A third-oder ΣΔ modulator typically uses three integrators. However, lower power consumption results by architectures that obtain third-order noise shaping with only two integrators. Suitable topological modifications of a conventional third-order scheme, [47], can obtain the result. An alternative solution is the noise coupling technique, [46], which, however, requires an additional active block.

Low op-amps swings enable relaxed slew-rate requirements, better linearity, lower power consumption, and allows operation at lower power supply voltages. Various methods for reducing the op-amps output voltage swings have been proposed, [42], [38], [51]. A further benefit for high order schemes is to have complex conjugate zeros, [72]. For medium resolutions, the signal-to-noise (SNR) ratio can be about 8 dB better than having all the zeros at $z = 1$. This project obtains all the above features. It realizes with two op-amps a third-order ΣΔ modulator; a fully digital solution reduces the amplifiers output swings and achieves complex conjugate zeros.

8.2.1 Third-Order Modulator with Two Op-Amps and Complex Conjugate Zeros

Suitable topological changes of a third-order architecture obtains a scheme with two integrators, [47]. This proposed architecture obtains the result with complex conjugate zeros in the noise transfer function (NTF) by the direct cascade of two blocks, shown in Fig. 8.1, that realizes a zero at $z = 1$ and two complex ones with imaginary part $\alpha/2$.

The block K before DAC1 serves to avoid denominator in the signal and noise transfer functions. By inspection of the scheme, the denominator is:

$$D = NTF + z^{-1}[1 + (1 - z^{-1})K] \tag{8.1}$$

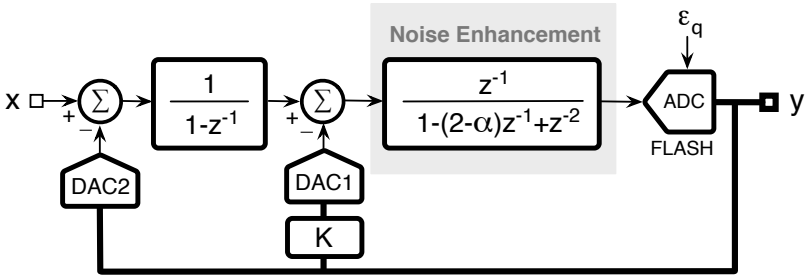

Figure 8.1: Block diagram of a third-order ΣΔ modulator with complex conjugate zeros.

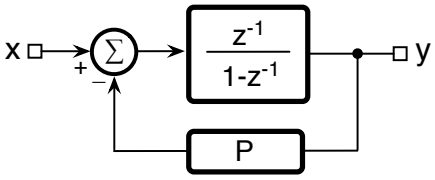

Figure 8.2: Block diagram of the second block of Fig. 8.1.

where

$$NTF = (1 - z^{-1})(1 - (2 - \alpha)z^{-1} + z^{-2}) \tag{8.2}$$

is the expected noise transfer function. The denominator becomes one if

$$K = (2 - \alpha) - z^{-1} \tag{8.3}$$

Thus, we achieve the NTF and the signal transfer function (STF) becomes z^{-1}.

The scheme of Fig. 8.2 implements the second block of the architecture of Fig. 8.1. Its transfer function is obtained by

$$\frac{(x - Py)z^{-1}}{1 - z^{-1}} = y \tag{8.4}$$

that results in

$$H(z) = \frac{z^{-1}}{(1 - z^{-1}) + Pz^{-1}} \tag{8.5}$$

Therefore, it is necessary to have

$$P = z^{-1} - (1 - \alpha) \tag{8.6}$$

that requires to use an analog delay, obtainable with two capacitors working in interleaved fashion. Fig. 8.3 shows a possible single-ended SC implementation.

8.2.2 Swing Reduction

Several methods, [42], [38], [51], obtain op-amps output ranges reduction in multi-bit architectures. This design uses digital methods to avoid extra branches at the input of the op-amps.

Fig. 8.4 shows the technique used to reduce the swing at the first integrator. An additional ADC converts the input signal and obtains an input feedforward toward the input of the second block.

By inspection of the circuit, the output of FLASH-1 is:

$$y^{'} = xz^{-1} + \overline{x}z^{-1}(1 - z^{-1}) + NTF\epsilon_q \tag{8.7}$$

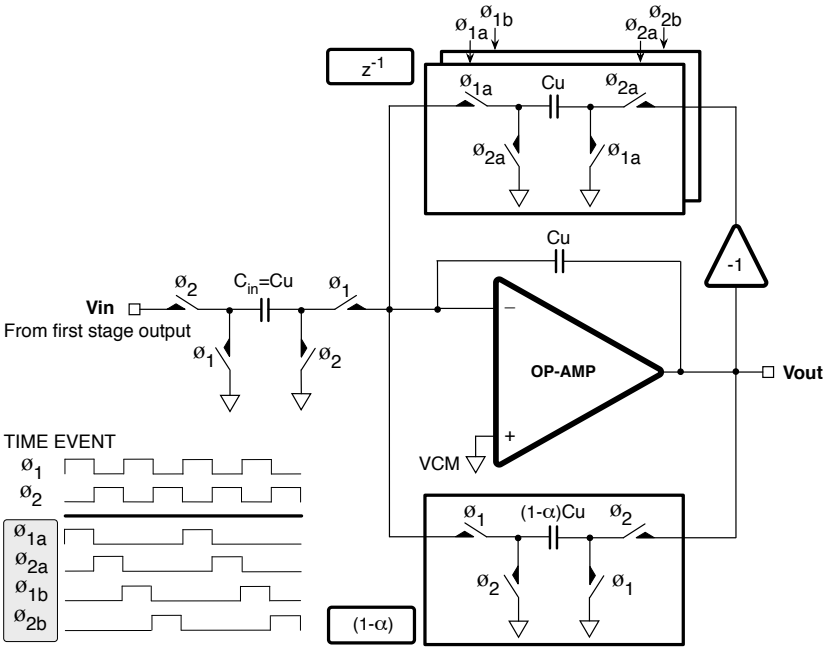

Figure 8.3: Possible single-ended SC implementation of the block diagram of Fig. 8.2.

where ϵ_q is the quantization error and $\overline{x}$ is the quantized version of the input signal, x. Therefore, we can eliminate in the digital domain the term $P_1(z)\overline{x} = \overline{x}z^{-1}(1-z^{-1})$, as shown in Fig. 8.4, to obtain the original response.

For the swing reduction of the second block, we observe that its output is

$$O_2 = xz^{-1} + \overline{x}z^{-1}(1-z^{-1}) + \epsilon_q(NTF-1) \tag{8.8}$$

With a suitable number of bits in FLASH-1 and FLASH-2, the dominant part of O_2 is

$$\overline{x}P_2(z) = \overline{x}z^{-1}(2-z^{-1}) \tag{8.9}$$

Suppose to add and subtract that term to O_2, as shown in Fig. 8.6. This operation does not change O_2. Then, we move the addition in the digital section to obtain $(O_2 - P_2)$. The final step is to move the subtraction to the input of the second block, as depicted in Fig. 8.5. The output of the block becomes $(O_2 - P_2)$.

Obviously, moving $-P_2(z)$ at the input of the block requires to divide $-P_2(z)$ by the block transfer function. Thus, the reduction of the swing of the second block requires a second extra injection at its input (Fig. 8.6)

$$\overline{x}E(z) = \overline{x}[1-(2-\alpha)z^{-1}+z^{-2}](2-z^{-1}) \tag{8.10}$$

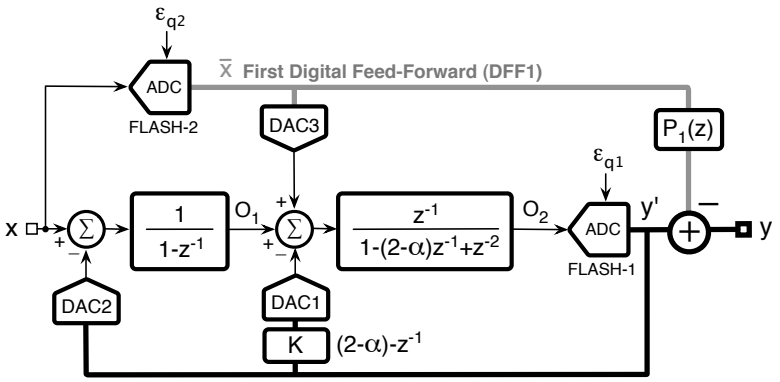

Figure 8.4: Swing reduction of the first integrator output.

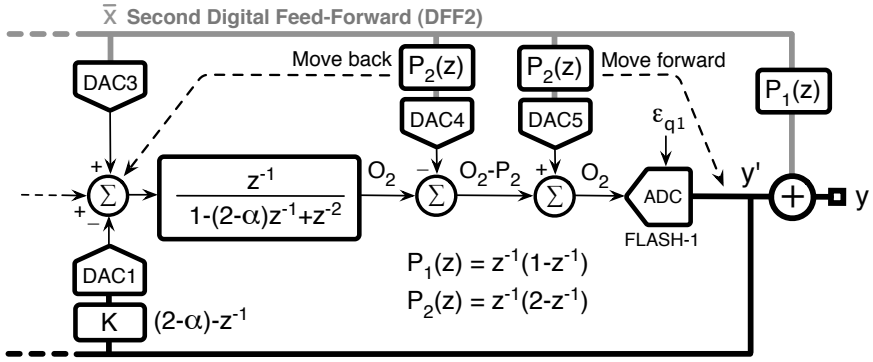

Figure 8.5: Swing reduction at the output of the second amplifier.

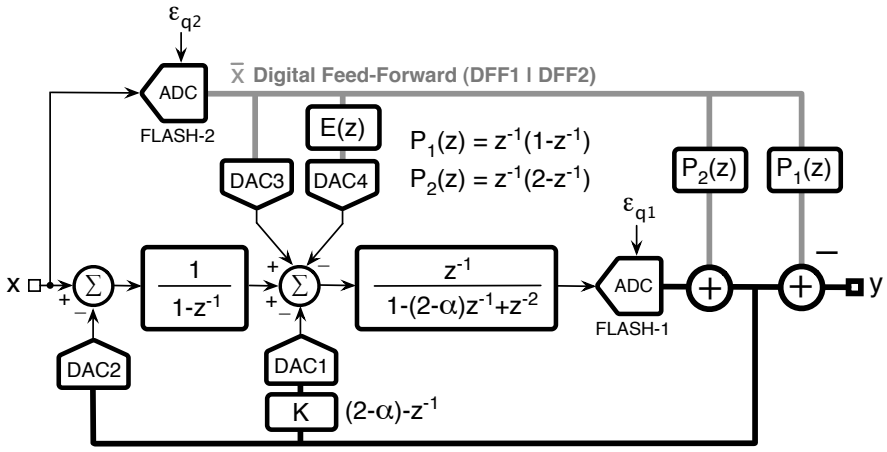

Figure 8.6: Third-order ΣΔ modulator with fully digital swing reduction.

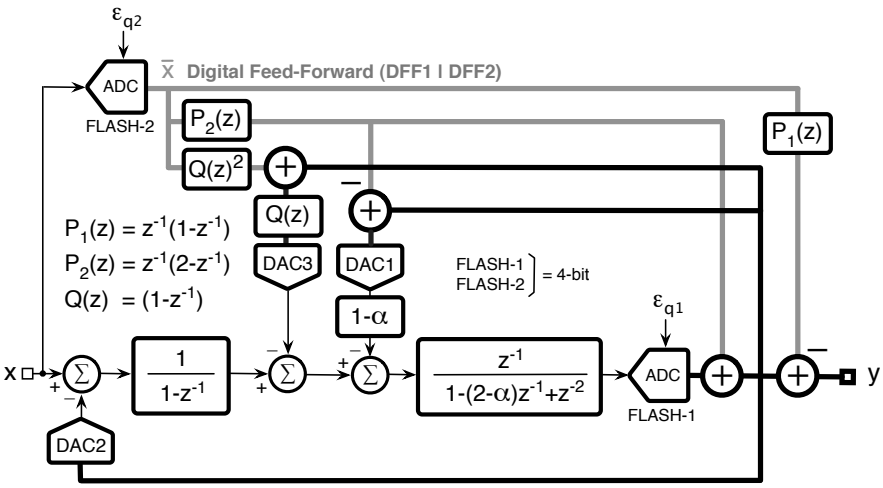

Figure 8.7: Proposed third-order modulator scheme.

Suitable combinations of digital terms lead to the scheme of Fig. 8.7. The term $(1-\alpha)$ is distinguished from the rest because it can be realized using the capacitor $(1-\alpha)C_u$ of Fig. 8.3 that obtains the second term of (8.6). Moreover, to implement DAC3, we can use C_{in} of Fig. 8.3, whose left terminal is available during Φ_1.

8.2.3 Simulation Results

The proposed third-order ΣΔ modulator with reduced amplifiers output swing and complex conjugate zeros has been simulated at the behavioral level in Matlab-Simulink^{TM}. With 4-bit flash and OSR = 8, the SNR with all NTF zeros at $z = 1$ is 64.9 dB. Making complex conjugate two zeros with $\alpha = 1/11$ optimizes the SNR that becomes 72.8 dB. The zeros placement depends on the accuracy of the capacitor that realizes this coefficient. Typical modern CMOS technologies ensure capacitors matching within ±0.02%. Montecarlo simulations (50 runs) obtain the root locus of (8.2), shown in Fig. 8.8. The mismatch minimally affects the position of the complex conjugate zeros.

Fig. 8.9 and Fig. 8.10 show the output voltage swing of the first integrator and the following block, respectively, when applying an input signal at -3 dB$_{FS}$ at the upper limit of the bandwidth with and without swings reduction. The first and second output swings are reduced by about 43% and 56%, thus demonstrating the effectiveness of the approach. Notice that the circuit implementation grants $z^{-1/2}$ delay for FLASH-2 operation. Moreover, since the swing of the second block is 53% of the full scale, the number of comparators of FLASH-1 goes down from 15 to 8.

The overall consumed power is reduced despite the need of 8 more comparators. The architecture spares the third op-amp (whose power need is about 50% of the first op-amp)

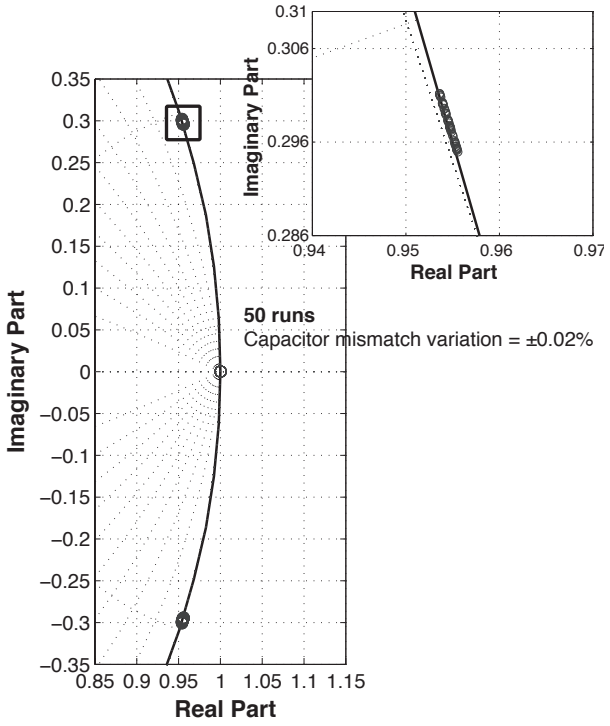

Figure 8.8: NTF zeros placement.

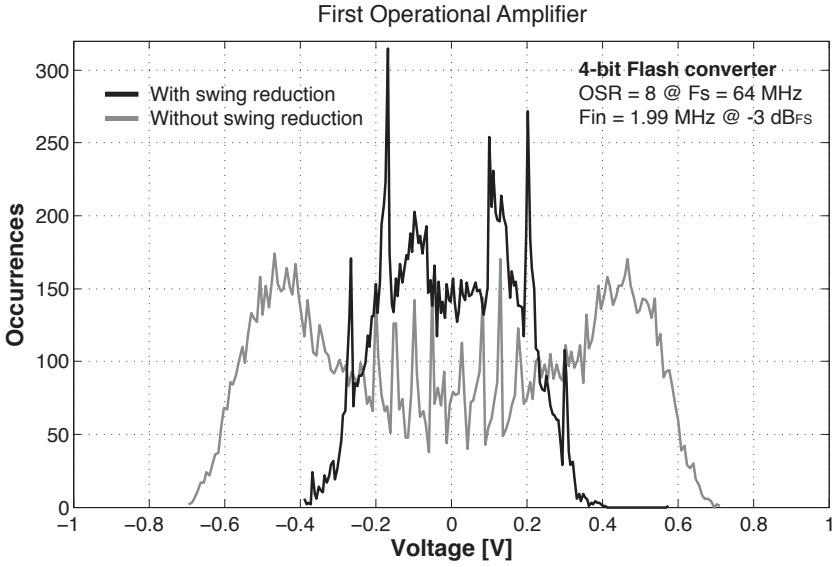

Figure 8.9: Simulated output voltage with and without digital swing reduction: First integrator.

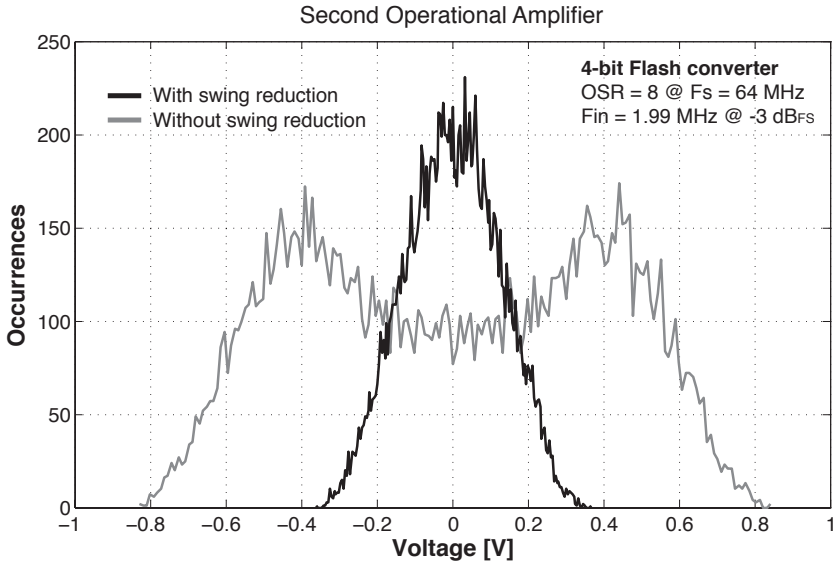

Figure 8.10: Simulated output voltage with and without digital swing reduction: Second integrator.

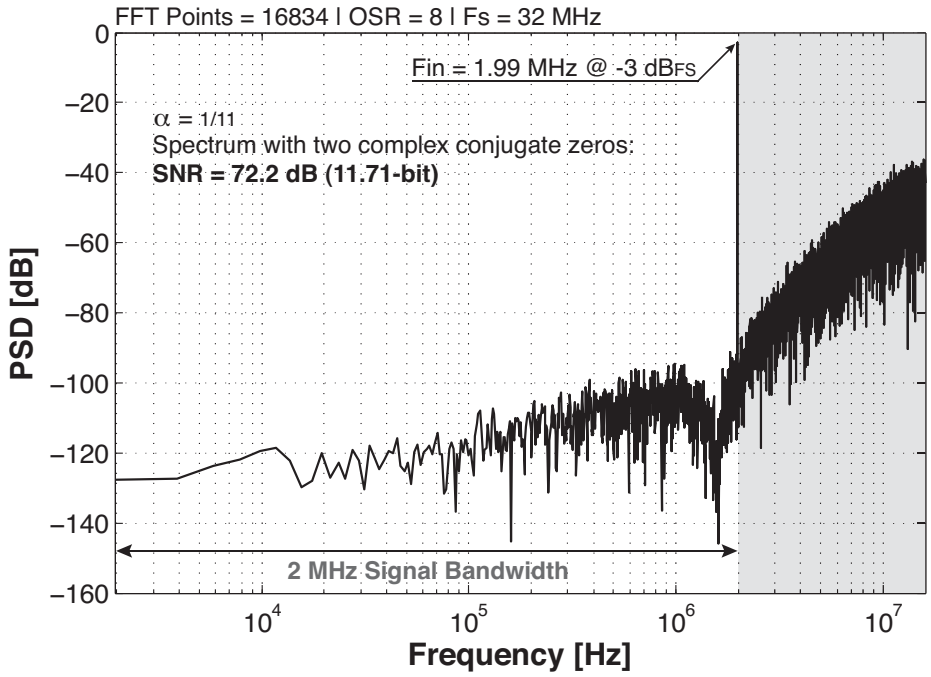

Figure 8.11: Simulated output spectrum.

and does not need more power on the second block. Simulation results show that the use of op-amp with bandwidth and slew-rate equal to the ones of the first and second op-amps of a conventional counterpart obtains the noise spectrum of Fig. 8.11. The SNR is 72.2, just 0.6 dB less than the ideal case. The simulation supposes a signal bandwidth of 2 MHz and amplifier unity gain frequency $f_{t1} = f_{t2} = 64$ MHz.

8.3 Oversampling Enhancement in ΣΔ Modulators

Data converters for portable communications must generate medium resolutions (in the range 10-12 bit) but must consume very low power. The parameter that measure the power effectiveness is the Figure of Merit, defined by

$$FoM = \frac{P}{2^{ENOB}\, 2f_B} \tag{8.11}$$

where P is the power, $ENOB$ is the equivalent number of bit and f_B is the signal band.

State-of-the-art ΣΔ modulators achieve FoMs lower than $0.2\,pJ/conv-lev$ but further reductions of the power level is increasingly required because of the needs of autonomous systems.

The methods that gives rise to optimal power consumption operate on three parameters: order of the modulator, oversampling ratio and number of bit of the quantizer [13]. The choice is typically for second order schemes (unless higher order are obtained with two op-amps), low oversampling and medium-high number of bit. The latter parameter depends on two factors: the power consumption that increases exponentially with the resolution and the number of unity elements that the DEM must average [27]. A common choice is to use a 3-bit quantizer but for medium resolution even 4-bit quantizer is a good choice.

This paper uses as starting prototype a second order modulator with 3-bit quantizer. However, more bit are also usable with the proposed method. Since the described technique virtually doubles the oversampling ratio (OSR) the scheme operates with a given clock frequency but the output digital data is at a double rate. The result, like the time-interleaved schemes reported in [34] and [73], gives rise, ideally to 2.5 extra bit. The benefit, as shown in the following sections, is fully granted with an analog solution. A digital realization looses 0.5 bit but requires less additional power.

8.3.1 Oversampling Enhancement Concept

Increasing the oversampling ratio means using more samples of the analog input signal. There are two possibilities, using a faster sampling rate or interpolating the input signal with zero or held replica of the input. Interpolation is common with digital signal but not used for analog. This paper supposes to use an interpolation by 2 to enhance the OSR by 2.

Fig. 8.12 shows the second order prototype. It uses two delayed integrators with gain 1/2

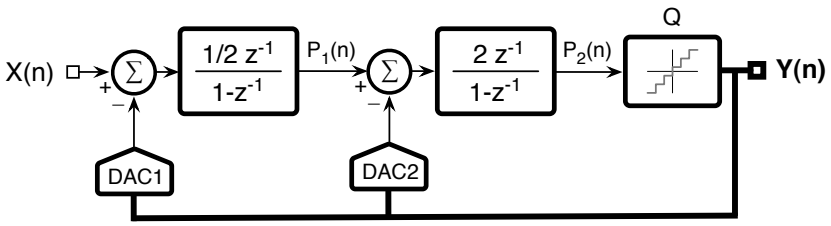

Figure 8.12: Conventional second-order ΣΔ modulator.

and 2 for the first and the second stage respectively. The choice accommodates half clock period for the settling of the two integrators, enables half clock period for the flash and the remaining half for DEM and D/A conversion.

The time-domain analysis of the modulator yields, for the first integrator

$$P_1(n+1) = P_1(n) + \frac{1}{2}\left[X(n) - Y(n)\right] \tag{8.12}$$

$$P_1(n+2) = P_1(n) + \frac{1}{2}\left[X(n) + X(n+1) - Y(n) - Y(n+1)\right] \tag{8.13}$$

Where n is supposed an even number. For the second integrator, it results

$$P_2(n+1) = P_2(n) + 2\left[P_1(n) - Y(n)\right] \tag{8.14}$$

$$P_2(n+2) = P_2(n) + 2\left[P_1(n) + P_1(n+1) - Y(n) - Y(n+1)\right] \tag{8.15}$$

therefore, the output of the first integrator at even times is the output at the previous even time plus the input minus the modulator output passed through the z-transfer function $(1 + z^{-1})$. Supposing that $X(n) = X(n+1)$ the input term is just twice the input at even times. The output of the second integrator at even times is given by the previous even plus output of first integrator minus the output passed through the z-transfer function $(1 + z^{-1})$.

Similarly, we can write equations that describe the output of integrators at odd times (again we suppose n an even number)

$$P_1(n) = P_1(n-1) + \frac{1}{2}\left[X(n-1) - Y(n-1)\right] \tag{8.16}$$

$$P_1(n+1) = P_1(n-1) + \frac{1}{2}\left[X(n-1) + X(n) - Y(n-1) - Y(n)\right] \tag{8.17}$$

and, for the second integrator

$$P_2(n) = P_2(n-1) + 2\left[P_1(n-1) - Y(n-1)\right] \tag{8.18}$$

$$P_2(n+1) = P_2(n-1) + 2\left[P_1(n-1) + P_1(n) - Y(n-1) - Y(n)\right]. \tag{8.19}$$

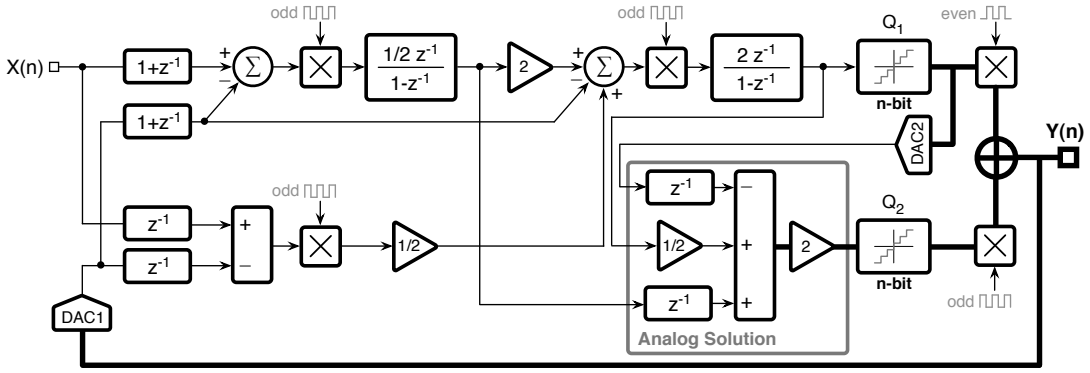

Figure 8.13: Second-order ΣΔ modulator with analog oversampling enhancement.

Supposing again that $X(n) = X(n+1)$ the input term uses one of the equal input pair and the previous one. Therefore, even if almost equivalent, when representing even samples the system looks ahead. When representing odd samples, the system recovers for the sample left behind.

The direct translation of the above equations is given by the analog implementation of Fig. 8.13. The inputs of the first integrator are the actual inputs plus the recovery term that gives rise to the analog and DAC input multiplied by $(1 + z^{-1})$ as equation (8.13) describes. The output of the first integrator is then available for two clock periods. The output of the second integrator is also available from even times (injection at $n + 1$ times) and lasts for two clock periods. It as prescribed by equation (8.15) is $P_2(n)$ added with twice $P_1(n)+P_1(n+1) = 2P_1(n) + 1/2\,[X(n) - Y(n)]$ and subtracted from twice $Y(n) + Y(n+1)$. The quantization of the output of the second integrator gives the digital output at even times. The circuit inside the block "Analog Solution" generates the next odd signal at the output of the second integrator as defined by equation (8.19). The block requires additions and subtractions that can be performed with a passive network. However, the operation must occur after the even quantization (Q_1). This requires to borrow a significant fraction of the full period.

There are other possible analog architectures that anticipate the generation of the even signal. The cost of the benefit is an extra op-amp that limits the power benefit Kye04a.

8.3.2 Digital Virtual Oversampling

The problem of the cascade of two quantizer and the need of using an extra DAC, as illustrated by Fig. 8.13, is resolved by the digital solution of Fig. 8.14. The scheme is formally the same but the "Digital Solution" block replaces the "Analog Solution" block by the use of a second quantizer (Q_2) that converts the output of the first integrator. The foreseen delay of the analog scheme provides the time needed for the A/D conversion. Moreover, the digital output replaces the analog output of the second integrator.

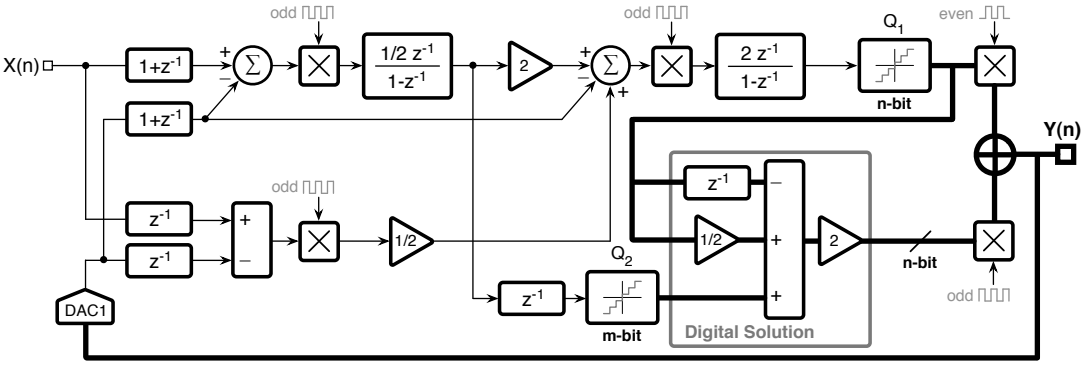

Figure 8.14: Second-order ΣΔ modulator with digital virtual oversampling enhancement.

The given solution is a trade-off between many possible schemes. Indeed the use of higher resolution in the digital paths that replace the analog signals would improve the result. The scheme of Fig. 8.14 uses the same number of bit, n, for the P_2 path and $m \geq n$ for the P_1 path.

The architecture of Fig. 8.14 can be improved because the signals at relevant nodes of the quantizer are the input plus shaped quantization noise. For a multi-bit scheme the noise term is small and because of oversampling there is some correlation between successive input samples [47]. The proposed scheme of Fig. 8.15 exploits that property. The input of Q_2 is the signal P_1 subtracted to a suitable processing of the digital output. The result is that the input range of the quantize is halved. Therefore, even if the quantization step remains the same the effective number of bit diminishes by one. Fig. 8.16 shows the output P_1 and the input of Q_2 with a $-3\,dB_{FS}$ signal and frequency at the limit of the band ($OSR = 16$).

The architecture of Fig. 8.15 has been simulated at the behavioral level. As shown in Fig. 8.17

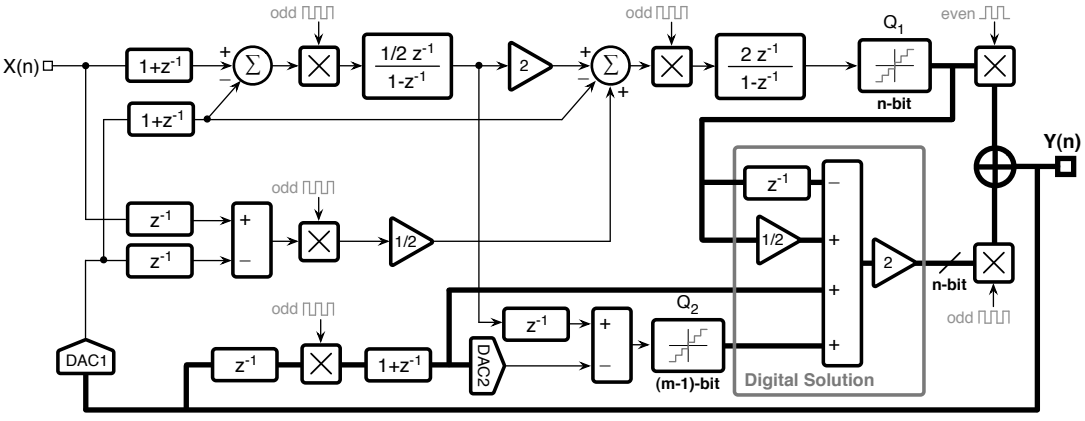

Figure 8.15: Proposed second-order ΣΔ modulator with digital virtual oversampling enhancement.

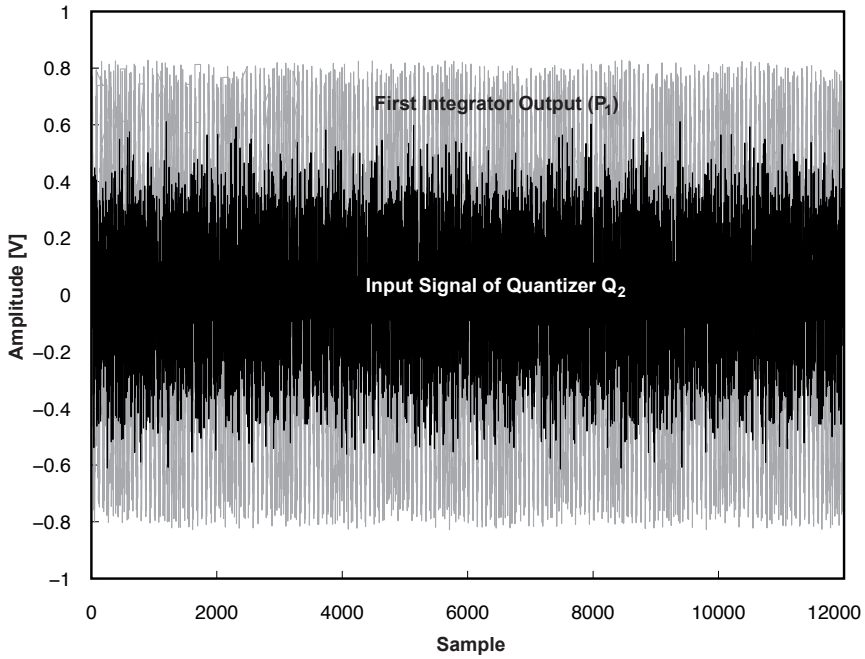

Figure 8.16: First integrator output signal and input signal of quantizer Q_2.

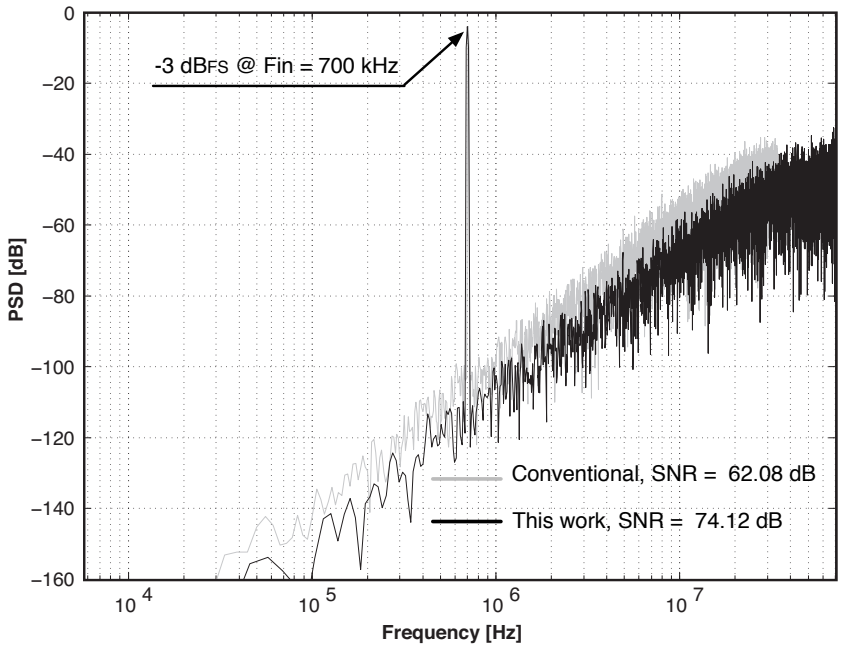

Figure 8.17: Simulated power spectrum density. FFT points=8192.

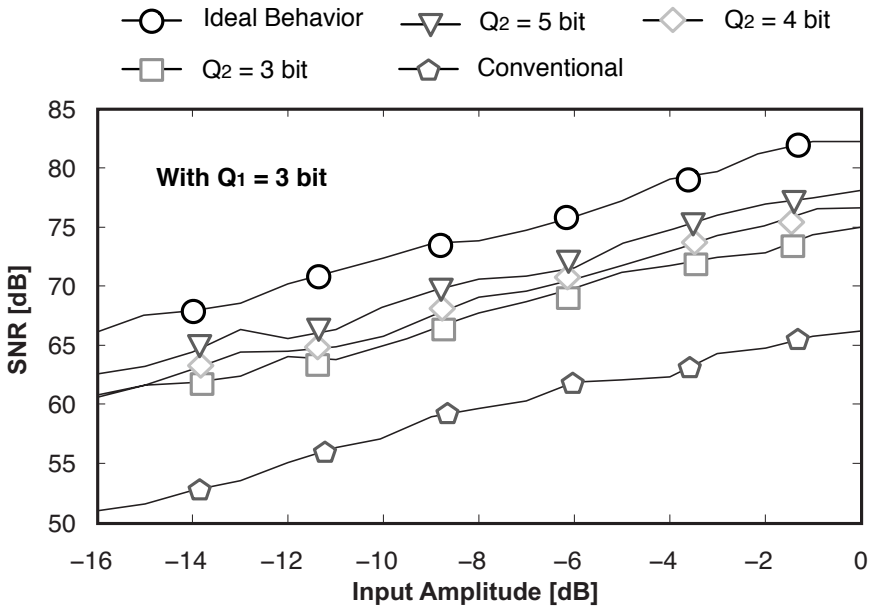

Figure 8.18: Simulated SNR vs input amplitude.

the conventional ΣΔ modulator of Fig. 8.12 with $OSR = 16$ and 3-bit quantizer achieves a $SNR = 62.08\,dB$. The proposed scheme of Fig. 8.15 with digital OSR enhancement grants about $12\,dB$ equivalent to 2-bit. The result is for a 4-bit Q_2 quantizer. The 0.5-bit loss respect to the ideal 2.5-bit (determined by a doubling of the OSR) is because of the performed digital approximation.

Fig. 8.18 shows the SNR at different input amplitudes and various Q_2 resolutions. Notice that the use of a 3-bit quantizer determines only $9\,dB$ improvement; the use of 4-bit grants about $12\,dB$ with a limited additional benefit for higher resolution. The use of 4-bit on both P_1 and P_2 paths gives rise to about an overall $13.5\,dB$ benefit.

8.3.3 Circuit Implementation

The implementation of the scheme of Fig. 8.15 must realize an additional transfer functions equal to $(1 + z^{-1})$ at the input of the first integrator. Moreover the input of the second integrator needs an equal transfer on the digital path, added to the multiplication by two P_1 plus an extra term given by the combination of an analog and digital converted term.

The design goal is to realize the functions with the minimum number of unity capacitors and to favor, when necessary a proper dynamic matching of unity elements. For the optimal circuit implementation it is worth nothing that:

- The outputs of the two integrators last for two clock periods.

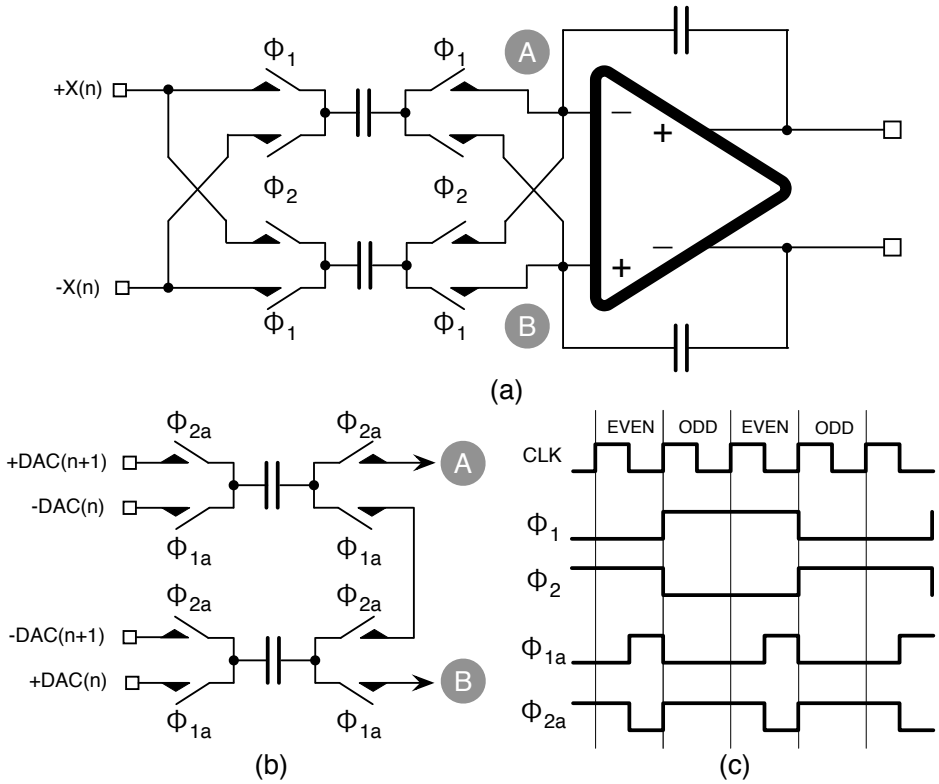

Figure 8.19: Possible fully differential SC implementation.

- The circuit generates the digital signals with short delay. The first is the even output followed by the odd by the delay established by the digital processing of the digital section.
- The input signals are possibly the result of an interpolation by two with the odd value equal to the previous even.

The above point suggest to use, in fully differential implementation, input structures like the ones of Fig. 8.19. The one on Fig. 8.19(a) can be used for the input signal. The driving phases are depicted in Fig. 8.19(c). Phase Φ_1 and Φ_2 last for two entire clock periods to ensure the longest time for the input injection. The scheme operates like a biquad parasitic insensitive SC structure. During phase Φ_1, the top capacitor injects the signal at odd times being pre-charged to the inverse of the input at the even times. The same does the bottom capacitor during phase Φ_2.

The scheme of Fig. 8.19(b) serves for the injection of the DAC signals. The capacitors are pre-charged at the proper value with a phase that is shorter than the one used for the injection. The reason is that passive charging is faster than the virtual ground injection being only limited by the on resistance of the switches. Similar strategy are used for the injection at the input of the second integrator.

An interesting feature of the solution proposed in Fig. 8.19 is that for multi-bit DAC the switched capacitor is divided into unity elements. They are used for both conversion of the digital signal of the even and the odd phases. This gives rise to the two conversions without using twice unity elements. Moreover, if DEM is needed the circuit must use two n-bit DEM, one for the even conversion, the other for the odd conversion.

Chapter 9

Conclusion

This thesis work has been focused on the design of two different topologies of low voltage low power $\Sigma\Delta$ modulators integrated with a 65 nm CMOS technology. The goal of this research was to explore efficient digital assistance techniques that allowing to relax the performance of the analog circuitry, making possible to mitigate the intrinsic limits of the deep submicron technology, which are not attractive for the analog design.

The rapid scaling of CMOS technology provides a bottleneck for analog circuit performance and poses a hard challenge for achieving an acceptable dynamic range due to the reduction of the supply voltage. At the same time, the threshold voltage is not scaling linearly with supply voltage, thus leading to a further strong degradation of the useful dynamic range, makeing difficult to drive CMOS switches and enhancing the leakage dissipation.

The aim of this thesis was to investigate the effectiveness of techniques that allow to reduce the swing of the output of the operational ampliers in order to relax slew-rate and GBW requirements with benets in terms of reduced power consumption and reduced harmonic distortion (better linearity). Moreover, these swing reduction techniques, allow to work with limited headroom voltage without affecting the final STF and NTF, thanks to the reconstruction of the information in digital domain.

The swing reduction technique is included in a new second order low-pass multi-bit multi-rate hybrid continuous-time (CT) $\Sigma\Delta$ modulator implemented with a general purpose 65-nm CMOS technology. The circuit ensures jitter immunity granted by the use of multi-rate switched-capacitor (SC) DACs that further reduce the requirement of the operational amplifier in term of gain, bandwidth and slew-rate. A combination of analog and digital feedforward paths allows to reduces integrators output swing. The modulator provides a measured 10.8 bits of resolution over a signal bandwidth of 1.1 MHz and a spurious free dynamic range (SFDR) of 78 dB. The chip draws 1.1 mW from a 1-V supply, leading to a Figure of Merit (FoM) equal to 280 fJ/conversion-level at the state of the art compared with other 65 nm chip operating in the same frequency range ([1], [2] ,[3], [4]).

The development of this innovative CT architecture suggests the study of new design

methodology that allowing to obtains a CT modulator with same noise shaping of a Discrete-Time (DT) prototype without any constraint about the shape of the feedback DAC. The new proposed methodology operates entirely in the time domain and accounts for any non-idealities of real implementations. Moreover, the procedure can be effectively implemented directly with circuit simulators during the design step, ensuring the exact design with transistor level blocks.

The second chip realization proposed a new third-order low-pass multi-bit discrete-time (DT) $\Sigma\Delta$ modulator implemented with a 65-nm CMOS technology. The proposed architecture obtains a third order noise shaping behavior with only two operational ampliers by boosting the noise shaping behavior from second to third order. Moreover, the implementation of a fully digital feedforward paths ensures a noise-like swing at the output of the operational amplifier, allowing the use of the telescopic scheme with gain boost. The modulator provides a simulated 14 bits of resolution over a signal bandwidth of 2.2 MHz and a signal to noise and distortion ratio (SNDR) of 83.27 dB. The chip draws 2.3 mW from a 1.2-V supply, leading to a Figure of Merit (FoM) equal to 43.8 fJ/conversion-level, the best of the state of the art in this frequency range.

Additionally, the work includes the analysis of two new low-power DT $\Sigma\Delta$ modulator architectures. The first one present the design of a third order modulator realized with only two operational ampliers, that achieves complex conjugate zeros allowing to increase the signal bandwidth and to obtain a SNR improvement of about 8 dB. The second architecture exhibits a new smart technique that virtually double the oversampling ratio of a conventional second order $\Sigma\Delta$ modulator. Accounting for a limited cost, the resolution increases by about 2-bit and power just increases by few percents. Therefore, the FoM diminishes by a factor close to 3.5.

The future work demands the measurement of the third order DT $\Sigma\Delta$ modulator and the chip realization of the last two ideas for very low power $\Sigma\Delta$ modulator.

Appendix A

PCB Design Guidelines

A.1 Board Layout

The layout of the board is the first step of the characterization of integrated circuit. High performance circuit not only requires a lot of care to the details of the circuit schematic, but also careful layout of final board plays a key role in order to obtain an optimum result. Thus careful routing and decoupling of the power lines and signal paths on board are very important. The optimal distribution of the ground on board and the decoupling between digital and analog part allow to reduce noise, interference and EMI generation [74].

Therefore, it is fundamental to follow some guidelines for obtaining optimal performance from a printed circuit board layout that involves analog and digital part. In general, for academic purposes, the design of a single board is sufficient, so the problem is limited to the realization of a single board ground (for example in equipment design is more critical, because all the boards or modules in the system have own ground all connected in a star fashion).

A.2 Ground Plane and Pin Rules

In a printed circuit board each input signals that feed the circuit generate a return current back to the source. This current follows the path with the least resistance and length. Then, the optimum return path is not a single trace, but a wide plane, that is, a plate coated with copper in order to reduce the overall impedance and increase EMI/RFI performance.

A basic layout consideration (it's a must) is that the analog and digital ground planes never should be overlapped in order to avoid cross-talking effect and induced noise. This suggests to place analog and digital parts at the opposite ends of a circuit board avoiding to surround analog region with digital ones and vice versa. Thus, both analog and digital circuitry have

their own separated ground planes.

Normally, it's better to place power supply circuits in a centralized area near the edge of the board; this permits to:

- easily reach all points of digital and analog power;
- any return currents generated in this edge area can return directly to the main supply with low impedance path without passing through the rest of the board.

The analog and digital ground planes should be connected together at only one point as close as possible to the main ground supply, as shown in Fig. A.1. This essentially creates the system star ground at the mixed-signal device. There are two possible solutions: using a simple via or a zero ohm SMD resistor. The last solution is preferable because offers low capacitance and low forward voltage drop. The low capacitance of the SMD resistor prevents ac coupling between the analog and digital ground planes. A good design rule indicates to have analog power planes that perfectly overlap the analog ground; the same applies to digital power planes

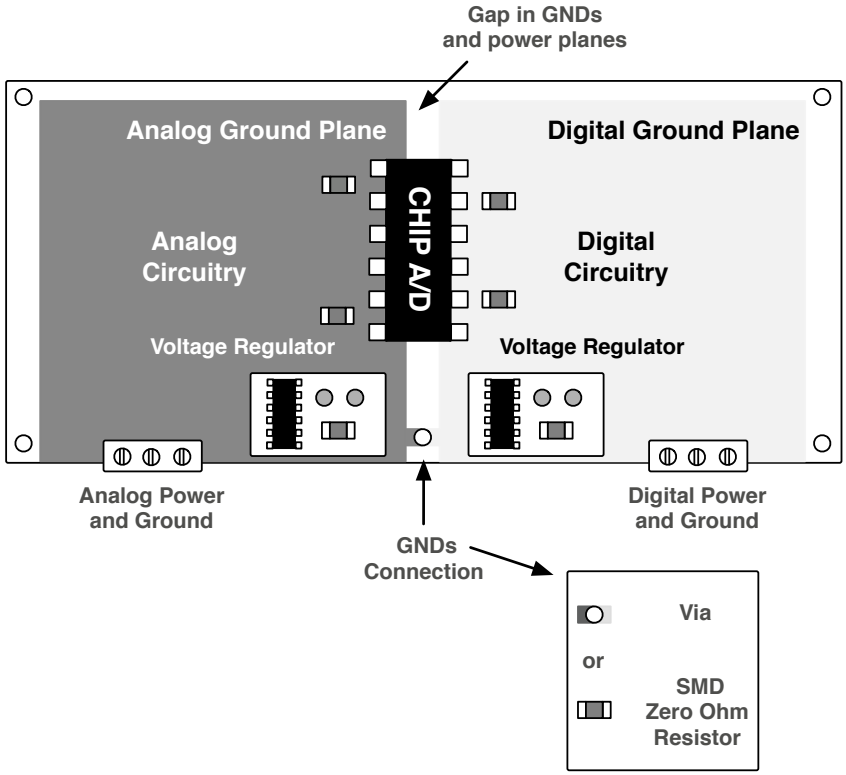

Figure A.1: Ground planes connection: the analog ground and digital ground planes are connected at that same point.

and its analog ground counterpart. Anyway there should be no overlap between analog and digital planes. The large overlap area of these power and the corresponding ground planes, with their close spacing, realize a distributed capacitance, which help to reduce high frequency noise and keep analog power voltage and ground plane voltage as flat as possible.

In order to maintain a low-impedance ground connection, it is usually a good choise increase the number of pins dedicated for ground and spread them among other connector pins. All additional ground pins provide parallel path that further reduce the impedance to the ground supply.

A.3 Supply and IC Decoupling

All analog circuit needs decoupling on its power pins to shunt both high frequency and low-frequency noise directly to ground. In that way, all return current thank to decoupling component return directly to supply leads without flowing in the rest of circuits. It is generally recommended to use larger value for electrolytic capacitor (in the range from $10\mu F$ and $47\mu F$) in parallel with a ceramic capacitor (in the range from $0.1\mu F$ and $0.01\mu F$). In particular, a good compromise for layout is placing for each supply leads, a decoupling capacitor directly to ground.

For a specific application, such as high performance A/D and D/A converters, it is recommended to use dedicated supply regulators and decoupling, for analog and digital parts, as close as possible to ICs in order to reduce the noise coupling with the rest of circuitry. Normally, the A/D should straddle the split between the two ground planes (Fig. A.1), in order to avoid any kind of cross-talking effect.

As said before, the ground connection is very important and must be wider. The smaller decoupling capacitor should be placed as close as possible to the IC on the same layer, as shown

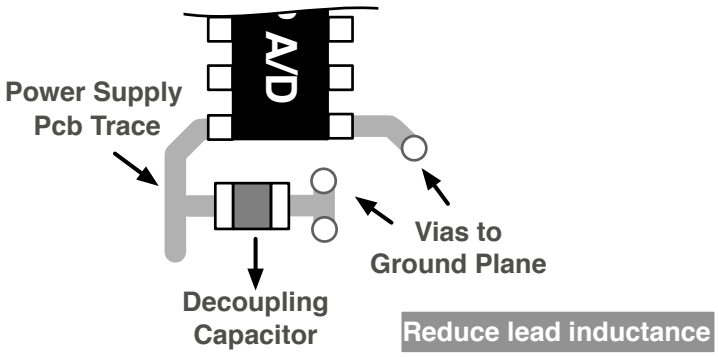

Figure A.2: Decoupling of IC power pins.

in Fig. A.2. The ground connection is realized with multiple vias: in this way the inductances of these vias are connected in parallel in order to reduce the total PCB trace inductance. Furthermore, the placement is facilitated by the presence of surface-mount capacitors which are the best solution, because their connection pads have almost no lead inductance and has very low ESR (equivalence series resistance).

A.4 PCB Layers

For high performance A/D characterization a good trade-off between complexity, cost and testability is a four-layer board (Fig. A.3). A general rule that simplifies the prototyping step, suggests to track the signal runs on the top and bottom layers and placing the power and ground planes on the inner layers. In general boards, the isolation (core) between layers 2 and 3 is thinner in order to increase the value of the distributed capacitance, which as well known is inversely proportional to this distance. The inner planes also helps to provide a low-impedance surface region that guarantee additional shielding between the external signal layers. Thus in order to reduce the radiation from high switching signal into analog circuits, it is recommended to fill with copper all the free areas among signal paths. The copper fill must be connected to ground.

An other recommendation, that allows to reduce the crosstalk, regards the routing of high speed digital signal traces (like digital clock) well away from all the sensitive analog traces.

At the end, the use of differential circuits in the generating of the analog inputs, gives rise to many benefits, due to differential circuit's balanced properties. Indeed, a differential circuit, permits to reject common-mode interference (including ground noise), reduces non-linearities, EMI generation and magnetically-induced interferences.

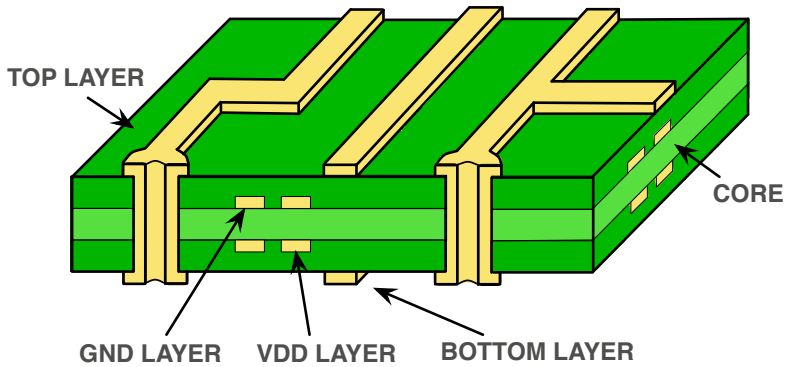

Figure A.3: Cross-section of a four layer board.

Appendix B

Pubblications

The primary technical contributions of this thesis are in the area of exploring efficient design techniques for the design of low voltage and low power ΣΔ ADC, that based on the increased support of digital assistance, allow to relax the performance of the analog circuitry, which present the worst features with deeper submicron technology. This thesis has been focused on proving the effectiveness of techniques that allow to reduce the swing of the operational amplifier used in the design of ΣΔ architectures targeted for low power consumption and low voltage applications in advanced 65 nm CMOS technology. The used design strategies, namely reduction of the number of op-amps and as well as integrators output swing reduction, further reduce the overall power consumption of the modulators but keeping the desired noise shaping performance in both CT and DT architecture.

Additionally, an investigative study was conducted to develop a new design methodology for CT ΣΔ ADC, that overcomes the limits of the conventional approaches and permits to obtain a CT modulator with same noise shaping behavior of the DT prototype without any constraint about the shape of the feedback DAC. The method works entirely in time domain and allows to model and compensate for any non-idealities of real implementations.

The main contributions and the papers on which they are based are listed below.

1. **Oscar Belotti** and Franco Maloberti "Design of Continuous Time ΣΔ Modulators with real analog blocks", IEEE PhD Research in Microelectronics and Electronics (Prime), Berlin, July 2010.

2. **Oscar Belotti** and Franco Maloberti "Time Domain Equivalent Design of Continuous Time ΣΔ Modulators", IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Athens, Dec. 2010.

3. Aldo Pena Perez, **Oscar Belotti** and Franco Maloberti "A two Op-amps Third Order ΣΔ Modulators with complex conjugate NTF zeros", IEEE International Conference on

Electronics Circuits and Systems (ICECS), Athens, Dec. 2010.

4. **Oscar Belotti** and Franco Maloberti "Mono-Rate and Multi-Rate Hybrid Continuous-Time Modulators with SC Feedback DAC" IEEE Internetional Symposium on Signals Systems and Circuit (ISSCS), Yasi, June 2011.

5. **Oscar Belotti**, Aldo Pena Perez and Franco Maloberti "Oversampling Enhancement in Sigma Delta Modulators", IEEE PhD Research in Microelectronics and Electronics (Prime), Madonna di Campiglio, July. 2011.

6. **Oscar Belotti**, Edoardo Bonizzoni and Franco Maloberti "A 1-V 1.1-MHz BW Digitally Assisted Multi-Bit Multi-Rate Hybrid CT $\Sigma\Delta$ with 78-dB SFDR", IEEE International Symposium on Circuits and Systems (ISCAS) (**Submitted**).

7. **Oscar Belotti**, Edoardo Bonizzoni and Franco Maloberti "Exact Design of Continuous Time Sigma-Delta Modulators with multiple feedback DACs", Journal of Analog Integrated Circuits and Signal Processing (**Submitted**).

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