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XXIII CICLO

Design of Band Pass ΣΔ Modulators with High Performances in 0.18-μm CMOS technology

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Preface

This Ph.D. thesis presents the research activity developed by Hervé Caracciolo concerning the study and the design at transistor level of a band pass ΣΔ modulator for Wide-Band Code Division Multiple Access (WCDMA) applications and a complex band pass ΣΔ modulator for Body Area Network applications. The activity involves the analysis at the behavioral level in Matlab-Simulink^{TM}environment, the transistor level design, and the layout of the two modulators. For the first project there is also the description of the PCB design and the test chip results. The thesis reports also the study of non-conventional architectures for the design of ΣΔ modulators. The activity is carried out in the IMS Lab of the University of Pavia, under the supervision of Prof. F. Maloberti.

The first project is the design of a MASH band pass ΣΔ modulator for Wide-band Code Division Multiple Access (WCDMA) applications. The signal bandwidth of the proposed modulator is 10 MHz, centered around an intermediate frequency (IF) of 70 MHz. The target is to have four complex conjugate zeros around the IF and a resolution of 13 bit in a 10 MHz bandwidth. To obtain this goal it's designed a MASH bandpass modulator to obtain multiple zeros: the MASH architecture is made by two band pass ΣΔ modulators. The principle of a MASH ΣΔ A/D converter consists in the quantization noise injection of the first ΣΔ modulator into the second one. A digital filter receives the two modulator digital outputs, and removes the quantization noise of the first modulator by an opportune digital processing, obtaining the desired noise transfer function. Each modulator in the MASH structure is based on a two-path architecture, which allow to obtain the desired in-band noise shaping zeros and reduce the power consumption. The ΣΔ modulator is implemented using a 0.18-μm CMOS technology and a sampling frequency of 180 MHz. The simulations at transistor level show a resolution of about 13 bit, with a bandwidth of 10 MHz, and a power consumption of about 90 mW, with a supply voltage of 1.8 V, resulting in a figure of merit as low as about 0.16 pJ/conversion-level. The mesurement results show a resolution of 11.7 bit with a bandwidth of 10 MHz. The power consumption is 95 mW, and the resulting figure of merit is equal to 0.42 pJ /conversion-level. The project was in collaboration with National Semiconductor.

The second project is the design of a complex band pass ΣΔ modulator for Body Area Network Applications. The proposed novel architecture is based on a method that constrains the zero positioning but allows to obtain simple approach in the design at transistor level. The principle of the architecture is to use cross-coupled feedback of the real path and the quadrature path, and the injection of the quantization noise coming from both path. In this way the noise transfer function has two zeros around the IF and no zeros in the image.

The target is to have a resolution of 6 - 7 bit resolution with a bandwidth of 2.6 Mz, and 8 - 10 bit resolution with a bandwidth of 100 kHz. The intermediate frequency (IF) is 2.5 MHz. The ΣΔ modulator is implemented using a 0.18-μm CMOS technology and a sampling frequency of 20 MHz. The simulations at transistor level show a resolution of about 8 bit, with a bandwidth of 2.6 MHz, and a resolution of 10 bit, with a bandwidth of 100 kHz. The power consumption is 1.95 mW, with a supply voltage of 1.8 V. The project was in collaboration with Analog Devices.
Chapter 1 describes the motivations, the main design features and the results of the two projects. This chapter gives a brief introduction to the Ph.D activity concerning the two band pass ΣΔ modulators design.
Chapter 2 presents in details the design of a band pass ΣΔ modulator for Wide-band Code Division Multiple Access (WCDMA) applications. It's described the motivations, the proposed architectures, the behavioral analysis, the transistor level design, the simulations results and the measurement.
Chapter 3 illustrates the design of a complex band pass ΣΔ modulator for Body Area Network Applications. It's presented the motivations, the study of architectures for band pass ΣΔ modulator, the proposed solution, the behavioral analysis, the transistor level design, and the simulations results.
Chapter 4 is a presentation of two non-conventional solutions for solving problems concerning the design of ΣΔ modulator. The two main thematics developed are: digitally assisted ΣΔ modulator, and the DAC linearization for multi-bit ΣΔ modulator without the use of dynamic elements matching. Each section illustrates the motivations, the proposed solutions and the results. Both techniques are simulated at the behavioral level in Matlab-Simulink^{TM}environment, introducing real parameter in the structures, and coefficient errors to investigate the mismatch sensitivity and demonstrate the effectiveness of the approach.
Appendix A and Appendix B give some information about Wide-Band Code Division Multiple Access, and Body Area Network, respectively.
Appendix C shows the Ph.D. publications.

Contents

Chapter 1

Motivations, Design, and Results

This Ph.D. thesis presents the research activity developed by Hervé Caracciolo and concerning the study and the design of a band pass ΣΔ modulator for Wide-band Code Division Multiple Access (WCDMA) applications and a complex band pass ΣΔ modulator for body area network applications. The activity involves the analysis at the behavioral level, the transistor level design, and the layout of the two modulators. Both architectures are novel and obtain performances at the state of the art. Informations about WCDMA and about body area network are available, respectively, in Appendix A, and Appendix B. This chapter explains the main features of the design activity. Both projects will be described in details in Chapter 2 and Chapter 3.

1.1 Band Pass Modulator for WCDMA Applications

In modern communication systems, the standards foresee wide signal bands ($1 \div 10$ MHz), while requiring medium-high resolution ($10 \div 14$ bit). To convert into digital an intermediary frequency (IF), often in the range of $40 \div 100$ MHz it's possible to use a high-resolution Nyquist-rate ADC or a band pass ΣΔ modulator. Since high-resolution Nyquist-rate A/D converters with sampling-rate embracing the IF interval consume significant power, band pass ΣΔ modulators are in general preferable because they consume low power either in continuous-time and sampled-data implementations. To achieve the standard specifications (wide signal bands ($1 \div 10$ MHz) and medium-high resolution ($10 \div 14$ bit)), it is necessary to design a band pass with multiple zeros around the IF. In this project is designed a A/D converter for WCDMA applications with the following specifications:

- IF around 70 MHz;
- Signal bandwidth 10 MHz;
- Minimum SNR 80 dB;
- Power consumption less than 100 mW;
- WCDMA Applications.

The proposed architecture is a MASH band pass ΣΔ modulator, made by two fourth order band pass ΣΔ modulators, Fig. 1.1.

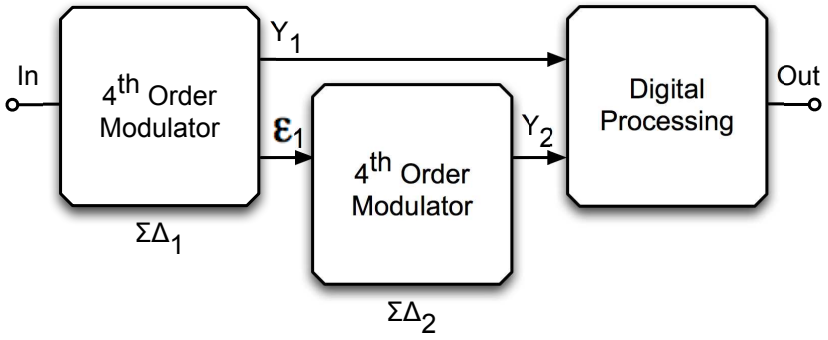

Figure 1.1: Block diagram of the designed MASH band pass ΣΔ modulator.

The target is to realize an *NTF* given by

$$NTF = \prod_{i=1}^{4} \left(1 + a_i z^{-1} + z^{-2}\right), \tag{1.1}$$

Fig. 1.2 shows the zeros positions around the unity circle, with the chosen values of coefficients a_i: $a_1 = 12/8$, $a_2 = 13/8$, $a_3 = 14/8$, $a_4 = 15/8$.

With these values, the zeros are very close to the edge of the first Nyquist band. The principle of a MASH ΣΔ A/D converter consists in the quantization noise (ϵ_1) injection of the first ΣΔ modulator into the second one. A digital filter receives the two modulator digital outputs, and removes the quantization noise of the first modulator by a suitable digital processing, obtaining the desired noise transfer function.

By inspection of the circuit in Fig. 1.1, the outputs of the first and second modulator are given by

$$\begin{cases} Y_1 = In \cdot STF_1 + \epsilon_1 \cdot NTF_1 \\ Y_2 = \epsilon_1 \cdot STF_2 + \epsilon_2 \cdot NTF_2 \end{cases}, \tag{1.2}$$

where $STF_1 = STF_2 = z^{-2}$ are the signal transfer functions of each modulator. The digital filter implements the function

$$Out = Y_1 \cdot z^{-2} - Y_2 \cdot NTF_1, \tag{1.3}$$

thus canceling the quantization error of the first modulator shaped by NTF_1 and leading to the desired output, given by

$$Out = In \cdot z^{-4} + \epsilon_2 \cdot \prod_{i=1}^{4} \left(1 + a_i z^{-1} + z^{-2}\right). \tag{1.4}$$

Each modulator introduces two couples of complex conjugate zeros around the intermediary frequency, and is based on a two-path architecture, Fig. 1.3, which allows to obtain the desired in-band noise shaping zeros and reducing the power consumption.

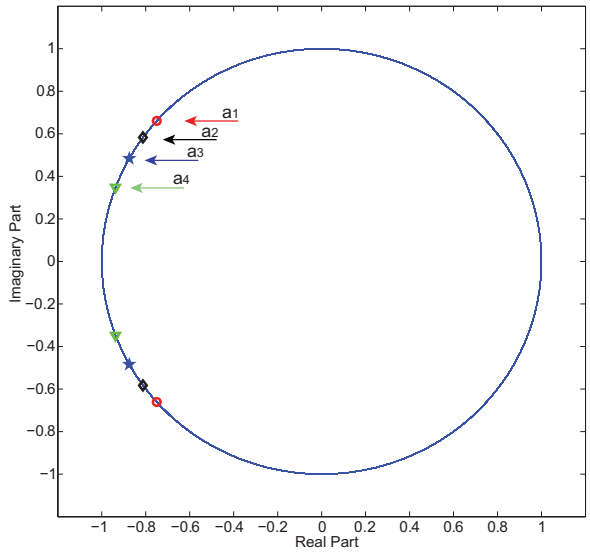

Figure 1.2: Desired position of the *NTF* zeros around the unity circle.

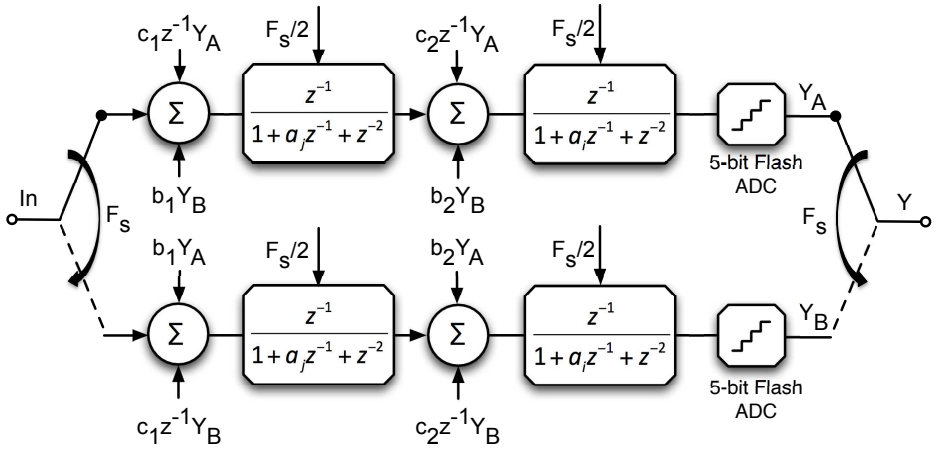

Figure 1.3: Band pass ΣΔ modulator implemented with two-path architecture.

The scheme in Fig. 1.3 uses resonators with transfer function $z^{-1}/\left(1+a_{i,j}z^{-1}+z^{-2}\right)$, with $-2 < a_{i,j} < 2$, in order to have complex conjugate zeros. In the two paths approach, the resonators can be implemented using the structure illustrated in Fig. 1.4. The two-path architecture, indeed, allows to easily realize a $z \rightarrow z^2$ transformation ($F_s \rightarrow F_s/2$) and a $z \rightarrow -z$ transformation using a square wave modulation at $F_s/4$ at the input and at the output of a conventional integrator, in order to obtain $z^{-1}/\left(1+z^{-2}\right)$ from a conventional integrator, $z^{-1/2}/\left(1-z^{-1}\right)$. The use of two-path reduces the power consumption, since multiple analog blocks running at a fraction of the speed require much less power than the power consumed by the single path counterparts. Benefit ensured by the two-path solution is about 50% of the total power. Moreover, suitable cross-coupled feedback paths in the integrators allow to obtain the $a_{j,i}z^{-1}$ terms in the resonator transfer function.

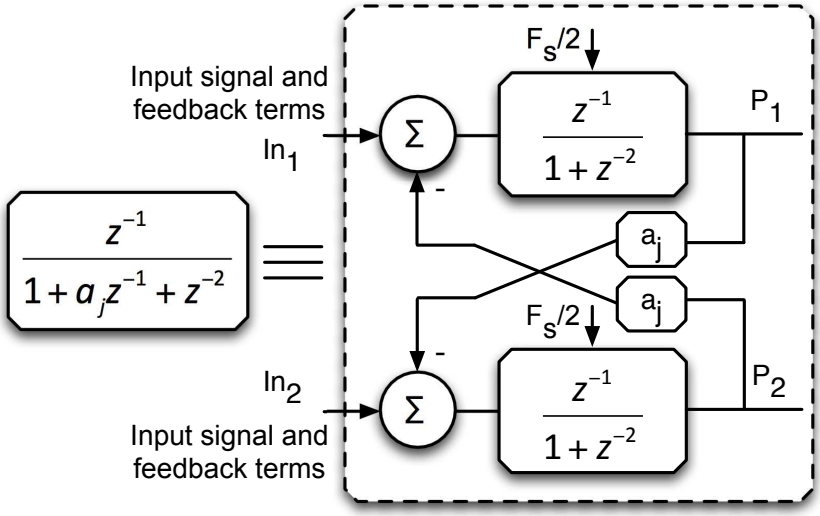

Figure 1.4: Resonator implementation in two-path architecture.

The MASH structure is, hence, analyzed using real integrators by a specific Matlab toolbox. The used integrators parameters are: DC gain around 1000, slew-rate of 500 V/µs, unity gain frequency equal to 1 GHz, and sampling capacitance (which is used for modeling the kT/C noise) equal to 1.2 pF. The resulting simulated output spectrum, reported in Fig. 1.5, shows that it is possible to achieve a resolution of about 13.7 bit with a signal bandwidth of 10 MHz. The noise floor present in the signal band is mainly due to the kT/C noise contribution.

The ΣΔ modulator is implemented using a 0.18-µm CMOS technology and a sampling frequency of 180 MHz. The simulations at transistor level show a resolution of about 13 bit, with a bandwidth of 10 MHz around an IF of 73.74 MHz, and a power consumption of about 90 mW, with a supply voltage of 1.8 V. Considering a typical figure of merit used for band pass ΣΔ modulator, the *FoM* is about 0.16 pJ/conversion-level, which is a value at the state of the art. Fig. 1.6 shows the simulated output spectrum with an IF of 73.74 MHz

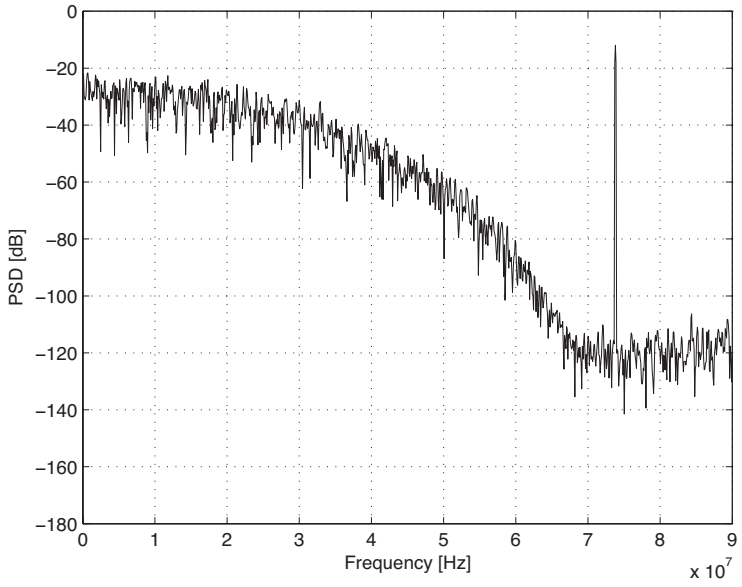

Figure 1.5: Output spectrum of the proposed ΣΔ modulator with real integrators.

and a sampling frequency of 180 MHz.

The layout converter is realized with a 0.18-μm CMOS technology and the chip area is 1.84 mm X 1.84 mm, including the pad-ring. The package is a LLP64 package with 64 pins. The research activity deals also in the PCB design and layout to test the chip. The mesurement results show a resolution of 11.7 bit in a bandwidth of 10 MHz. The power consumption is 95 mW, and the resulting figure of merit is equal to 0.42 pJ /conversion-level. Fig. 1.7 shows the measured spectrum: the input frequency is 70.5 MHz, the sampling frequency is equal to 180 MHz, and the FFT has 2^{17} points. The project was in collaboration with National Semiconductor.

1.2 Complex Band Pass Modulator for Body Area Network Applications

Quadrature band pass sigma-delta (ΣΔ) modulators are important building blocks for communication systems. Often zero IF solutions are unattractive because of the demanding image rejection requirements. Even low-IF, for which the DC offset and the 1/f noise fall outside the signal band, can be problematic for low power applications: the architecture must use wide-band A/D converters that are power hungry. The solution is to use quadrature or complex ΣΔ modulators that suppress the quantization noise only in the signal band and not in the image band.

In this project is designed a complex A/D band pass converter for body area network

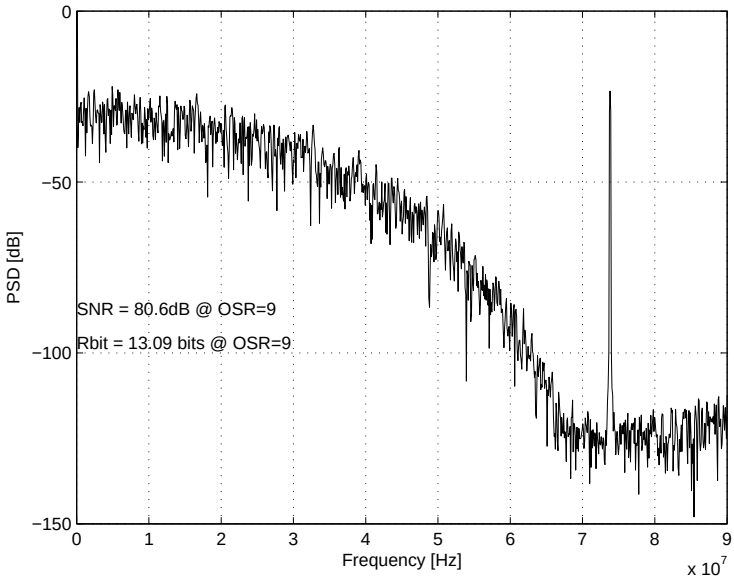

Figure 1.6: Output spectrum of the proposed ΣΔ modulator obtained with transistor-level simulation.

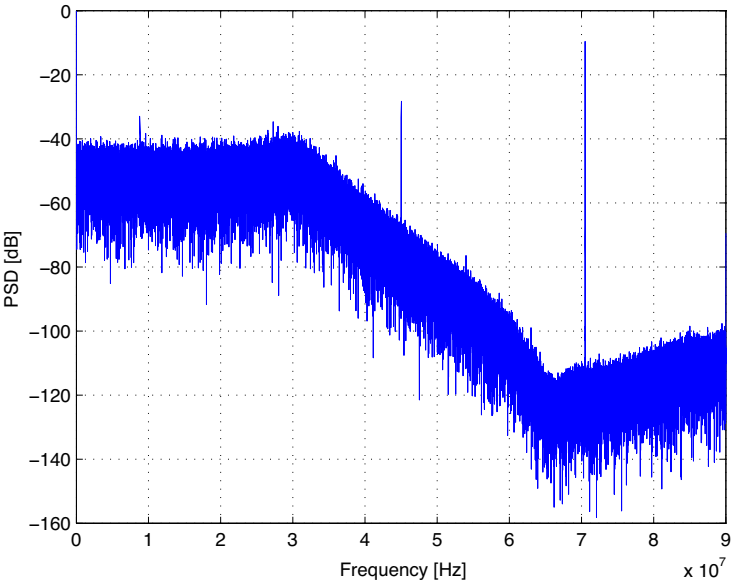

Figure 1.7: Output measured spectrum of the proposed ΣΔ modulator.

applications with the following specifications:

- IF 2.5 MHz;
- 6 - 7 bit resolution with a bandwidth of 2.6 MHz;
- 8 - 10 bit resolution with a bandwidth of 100 kHz;
- Power consumption less than 2 mW;
- Body Area Network Application.

The design of quadrature band pass ΣΔ normally assumes that the IF frequency is not locked to the sampling frequency. The possible degree of freedom is not a real advantage but on the contrary can be a limit because it is necessary to ensure accuracy in the coefficients of the complex filter that give rise to the notch.
The proposed method limits the possible transfer functions to a sub-set of possibilities. However, the resulting architectures allows to obtain simple circuital implementation. The NTF zeros placement is straightforward with the possibility to avoid using zeros in the conjugate position.

A complex *NTF* is in general expressed by

$$NTF = \prod_{1}^{n}\left[1 - \frac{e^{j\phi_i}}{z}\right] = 1 + \frac{a_1}{z} + ... + \frac{e^{j\sum_i^n \phi_i}}{z^n}. \tag{1.5}$$

The developed method limits the zero positioning to situations for which $\sum_i^n j\phi_i = 0, \pi, \pi/2, 3\pi/2$ or correspondingly the last coefficient of (1.5) is 1, j, -1 or -j. The reason of the choice is to simplify the architecture implementation, as depicted in Fig. 1.8.

The block diagrams of Fig. 1.8 (a) and (b) determine the noise transfer functions

$$NTF = (1 \pm z^{-n}) \quad or \quad NTF = (1 \pm jz^{-n}), \tag{1.6}$$

Notice that the block diagram inside the dotted lines of Fig. 1.8 is a generalization of the one used in a conventional quadrature modulator, shown in Fig. 1.9. It allows to obtain the complex transfer function $z^{-1}/(1 \pm jz^{-1})$.

In this design is implemented the following *NTF*:

$$NTF = 1 - \left(e^{j\phi_1} + e^{j\phi_2}\right)z^{-1} - jz^{-2} = 1 - \alpha z^{-1} - jz^{-2}, \tag{1.7}$$

where α is a complex number whose module is less than $\sqrt{2}$. Considering the possible *NTF* achievable using the scheme in Fig. 1.8, the missing term to obtain (1.7) is $-\alpha z^{-1}$. The realization of this term requires the injection of two quantization noise components one from the real path, the other from the imaginary one. The proposed resulting architecture is shown in Fig. 1.10: the two delays are distinguished into single delay, while the addition of the two quantization errors amplified by k is injected into the intermediate point with positive and negative sign.

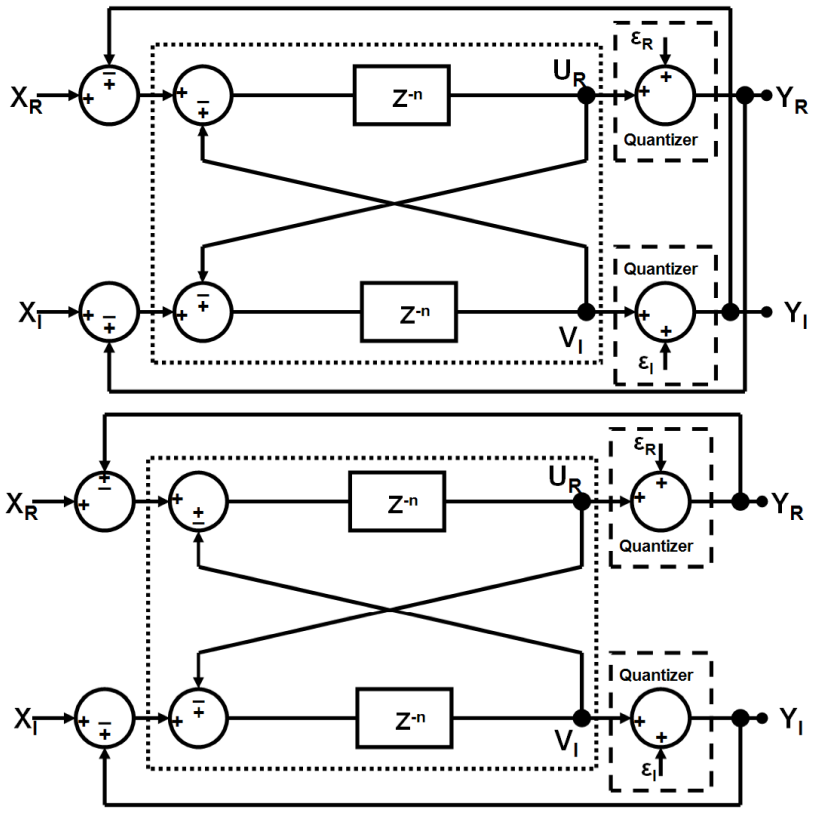

Figure 1.8: Generalized architecture for *NTF* with top ±j term, bottom with ±1 term.

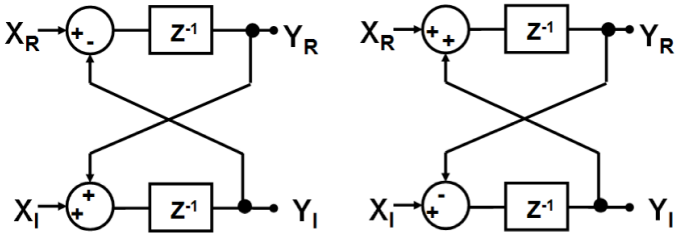

Figure 1.9: Basic building blocks for complex integrators.

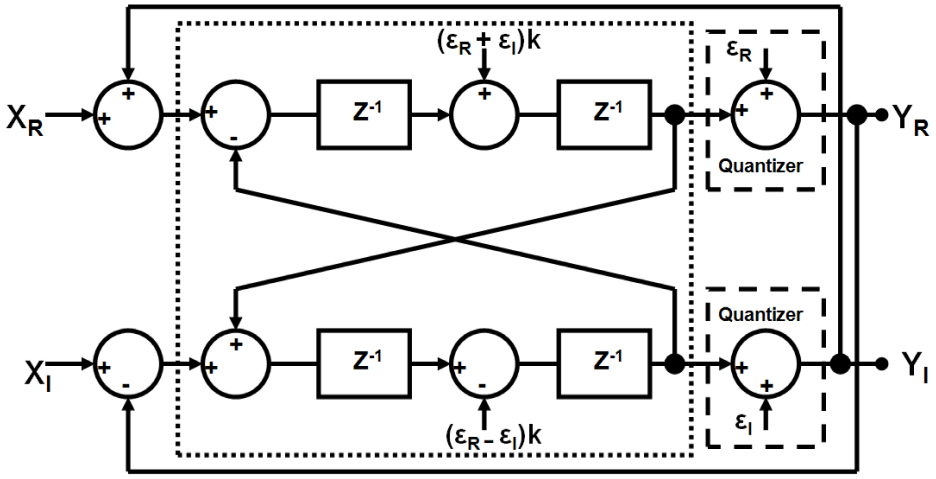

Figure 1.10: Block diagram of the designed complex band pass modulator with k=11/8.

In this project it's designed a complex band pass ΣΔ modulator using the architecture in Fig. 1.10 with k=11/8. The target is to obtain a *SNR* of about 48 dB with a signal bandwidth of 2.6 MHz, and a *SNR* of 66 dB with a signal bandwidth of 100 kHz. The *IF* is 2.5 MHz. Fig. 1.11 shows the zeros positions on the unity circle using k=11/8. The poles are all in the origin.

The modulator is studied introducing non-ideal parameter in the integrators and errors in the k-coefficient. Fig. 1.12 shows the spectrum with real integrators: the resolution is 8.8 bit with a 2.6 MHz bandwidth and 10.5 bit with 100 kHz bandwidth. Finite gain, op-amp finite bandwidth and slew-rate are considered in this simulation. Tab. 1.1 shows the parameters used into the analysis.

Table 1.1: Finite integrators parameters.

gain[dB]	**F**$_s$[MHz]	**bandwidth**[MHz]	**slew-rate**[μV/s]	**C input for kT/C**[fF]
60	20	100	30	800

The modulator is implemented using a 0.18-μm CMOS technology and a sampling frequency of 20 MHz. The simulations at transistor level show a resolution of about 8 bit, with a bandwidth of 2.6 MHz, and a resolution of 10 bit with a bandwidth of 100 kHz, considering an IF equal to 2.5 MHz. The power consumption is 1.95 mW with a supply voltage of 1.8 V. The resulting figure of merit is about 1.7 pJ/conversion-level. The obtained performances are at the state of the art. The layout converter is realized with a 0.18-μm CMOS technology and the chip area is 1.2 mm X 1.2 mm, including the pad-ring. The package is ceramic with 28 pin. At the moment the chip is not fabricated yet, so there are not chip measurement available. Fig. 1.13 shows the output spectrum obtained by post layout simulation, using an IF of 2.5 MHz, a sampling frequency of 20 MHz, and an FFT

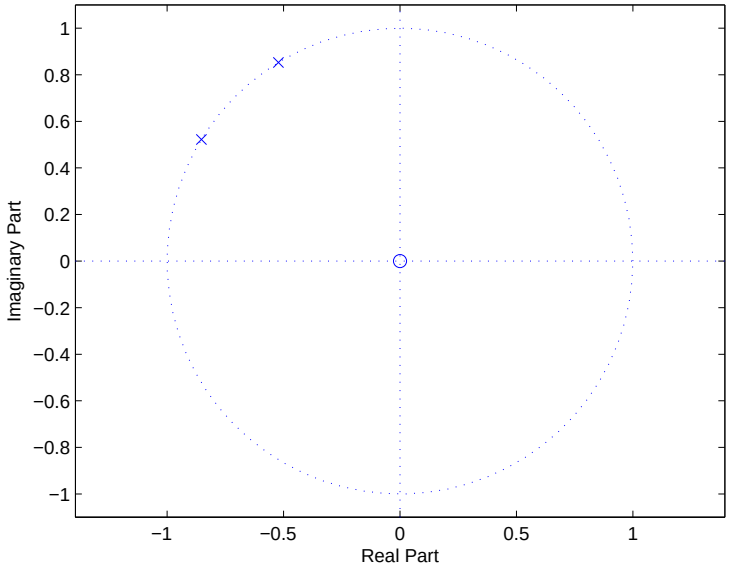

Figure 1.11: Zeros positions in the designed complex modulator.

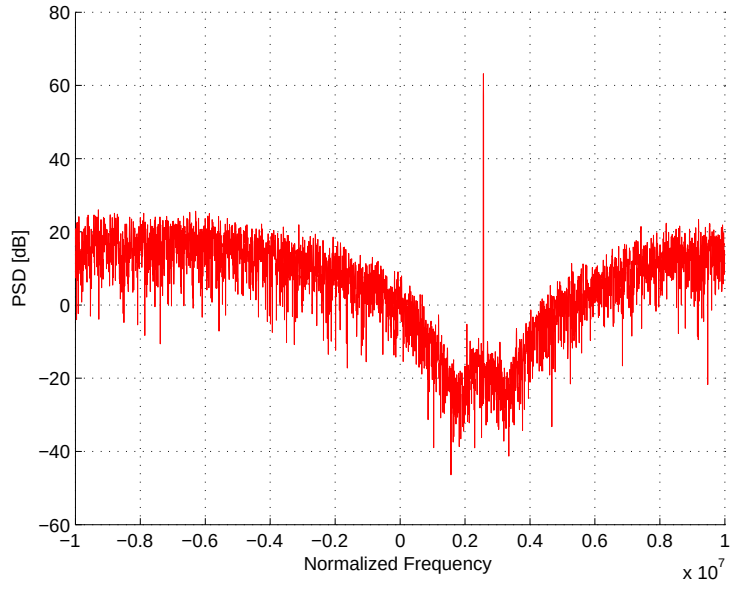

Figure 1.12: Spectrum of the designed second order complex modulator with real integrators.

of 2048 points. The project was in collaboration with Analog Devices.

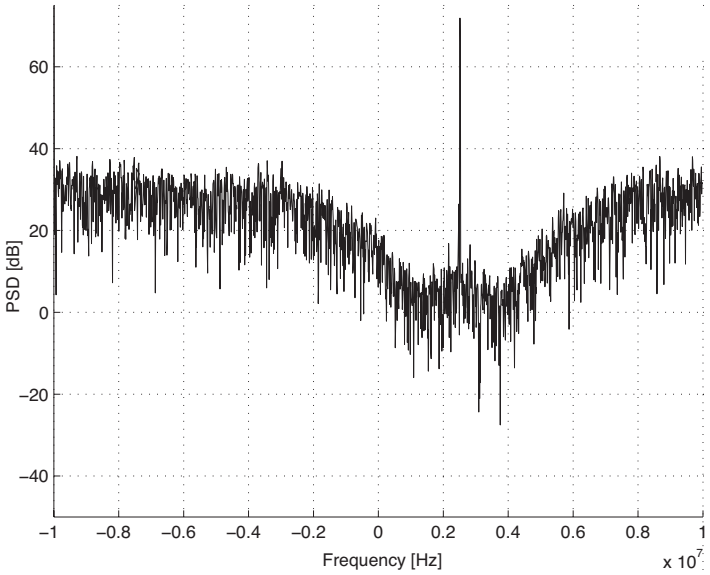

Figure 1.13: Simulated post layout output spectrum.

Chapter 2

Band Pass ΣΔ Modulator for WCDMA Applications

This chapter presents the design of a MASH band pass ΣΔ modulator for Wide-Band Code Division Multiple Access (WCDMA) applications. The signal bandwidth of the proposed modulator is 10 MHz, centered around an intermediate frequency (IF) of 70 MHz. The MASH architecture is made by two forth order band pass ΣΔ modulators. Each modulator in the MASH structure is based on a two-path architecture, which allow to obtain the desired in-band noise shaping zeros and reduce the power consumption. The ΣΔ modulator is implemented using a 0.18-μm CMOS technology and a sampling frequency of 180 MHz. The simulations at transistor level show a resolution of about 13 bit, with a bandwidth of 10 MHz, and a power consumption of about 90 mW, with a supply voltage of 1.8 V, resulting in a figure of merit (FoM) of 0.55 pJ/conversion-level. Considering a specific figure of merit for band pass ΣΔ modulator (FoM_{BP}), the modulator reaches a performance low as about 0.16 pJ/conversion-level. The mesurement results show a resolution of 11.7 bit with a bandwidth of 10 MHz. The power consumption is 95 mW, and the resulting figure of merit is equal to 0.42 pJ /conversion-level. The project was in collaboration with National Semiconductor.

2.1 Introduction, Motivations, and Results

In modern communication systems, the direct conversion into the digital domain of an intermediate frequency (IF), typically in the range $40 \div 100$ MHz, is becoming quite popular. The target is to match the communication standards specifications: wide signal bands ($1 \div 10$ MHz), and medium-high resolution ($10 \div 14$ bit). Tab. 2.1 shows the state of the art of band pass ΣΔ modulator.

In this chapter the design of a band pass ΣΔ modulator for WCDMA (Wideband Code Division Multiple Access) applications is presented. The considered IF is 70 MHz, the signal bandwidth is 10 MHz, and the signal-to-noise ratio (*SNR*) target is more than 80 dB. The proposed band pass ΣΔ modulator is based on a MASH (multi-stage noise shaping) architecture, which realizes a noise transfer function (*NTF*) with four couple of complex

Table 2.1: State of the art of band pass ΣΔ modulator.

P[mW] @ V_{dd}[V]	**F_s[MHz]**	**IF**[MHz]	**bw[MHz]**	**SNR**[dB]	**Ref.**
150 @ 1.8	120	40	2.5	69	[4]
88 @ 1.8	37.5	10.7	0.2	71	[17]
37 @ 3.3	240	60	0.2	72	[18]
47.5 @ 3.3	92	23	0.27	80	[19]
16 @ 1.8	120	40	1	65.1	[21]

conjugate zeros around the unity circle. The principle of a MASH ΣΔ A/D converter consists in the quantization noise injection of the first ΣΔ modulator into the second one. A digital filter receives the two modulator digital outputs, and removes the quantization noise of the first modulator by an opportune digital processing, obtaining the desired noise transfer function. The MASH structure consists of two fourth order band pass ΣΔ modulators, each implemented with a two-path architecture with cross-coupled integrators. The two-path structure allows to reduce the power consumption and easily implement the desired *NTF* zeros. The ΣΔ modulator works with a sampling frequency of 180 MHz, so that each path runs at 90 MHz. The proposed ΣΔ modulator is implemented at the transistor level using a 0.18-μm CMOS technology, a voltage supply of 1.8 V, and a sampling frequency of 180 MHz. The simulations at transistor level show a resolution of about 13 bit, with a bandwidth of 10 MHz around an IF of 73.74 MHz, and a power consumption of about 90 mW, with a supply voltage of 1.8 V. Considering a typical figure of merit used for band pass ΣΔ modulator, the *FoM* is about 0.16 pJ/conversion-level, which is a value at the state of the art.

2.2 Band Pass ΣΔ Architectures with Single and Two Parallel Paths

The proposed design strategies for band pass ΣΔ modulators are discussed. This section explains two different approaches: the use of resonators and the synthesis of the noise transfer function (*NTF*) starting from a closer function. The use of a MASH configuration to obtain multiple zeros or splitting the complex zeros of the *NTF* is also discussed. The sensitivity to components mismatch of the proposed solutions is studied to identify advantages and limits in various presented architectures. Results show that mismatch errors in the fraction of percent range do not degrade the *SNR* significantly. Two possible design strategies that achieve multiple complex pairs of zeros in the noise transfer function (*NTF*) are proposed. The resulting architectures can be implemented by using a single-path conventional scheme or by the parallel action of two-path modulators that work at half the clock frequency. The use of two-path simplifies the realization of the required basic functions and, at the same time, reduces the power consumption, since multiple analog blocks running at a fraction of the speed require much less power than the power consumed by the single path counterparts. The benefit ensured by the two-path solution is about 50% of

the total power.

2.2.1 Design Methods

The noise transfer function (*NTF*) of a band pass ΣΔ modulator can be generally expressed as follows:

$$NTF = \prod_{i=1}^{N} \left(1 + a_i z^{-1} + z^{-2}\right), \tag{2.1}$$

where each term contributes with a zeros pair located on the unity circle at the conjugate positions, under the condition $-2 < a_i < 2$:

$$z_{1,2,i} = \left[-a_i \pm j\sqrt{\left(4 - a_i^2\right)}\right]/2, \tag{2.2}$$

Moreover, the signal transfer function (*STF*) in the *IF* range must be flat with 0 dB gain. In the open literature, there are many circuit solutions that achieve such a result, [1], [2], [3]. Here the attention is focused on solutions based on a $z \rightarrow -z^2$ transformation applied to a low pass modulator or schemes with $z^{-\gamma}/(1 + az^{-1} + z^{-2})$ resonator. In the former case, the *STF* is flat, but the zeros of the *NTF* are fixed at $z = \pm j$. For the use of resonators, the *NTF* has zeros at the expected positions, but the *STF* may contain poles on the unity circle.

Second Order Band Pass Modulator

A transformation $z \rightarrow -z^2$ changes a first order *NTF*, $(1 - z^{-1})$, into a second order one, $(1 + z^{-2})$. The resulting *NTF* misses the term az^{-1} to achieve $(1 + az^{-1} + z^{-2})$. The missing term is generated by injecting at the modulator input the quantization error (ϵ) multiply by the coefficient a, as shown in Fig. 2.1(a), [4].

Another possible implementation is the use of resonator. A feedback loop that includes the quantizer and the resonator $z^{-1}/(1 + az^{-1} + z^{-2})$ allows to obtain the desired *NTF*, but the block P(z) used in the feedback loop, as shown in Fig. 2.1(b), can not be a simple delay. It can be easily verified that $P(z) = a + z^{-1}$ makes $STF = z^{-1}$. The operation of the above solutions can be verified at the behavioural level. Fig. 2.2 shows the simulated output spectrum generated by both architectures at the behavioural level in Matlab-Simulink^{TM}environment, using a coefficient equal to 14/8. The spectrum shows a zeros around the IF.

High Order Band Pass Modulator

The use of $z \rightarrow -z^2$ transformation on a second order low-pass modulator would produce $NTF = (1 + z^{-2})^2$, which has two zeros pairs at z= $\pm j$. If two pairs of complementary zeros at $z_{1,2} = \alpha_1 \pm j\beta_1$ and $z_{3,4} = \alpha_2 \pm j\beta_2$, respectively, are required, the noise transfer function becomes

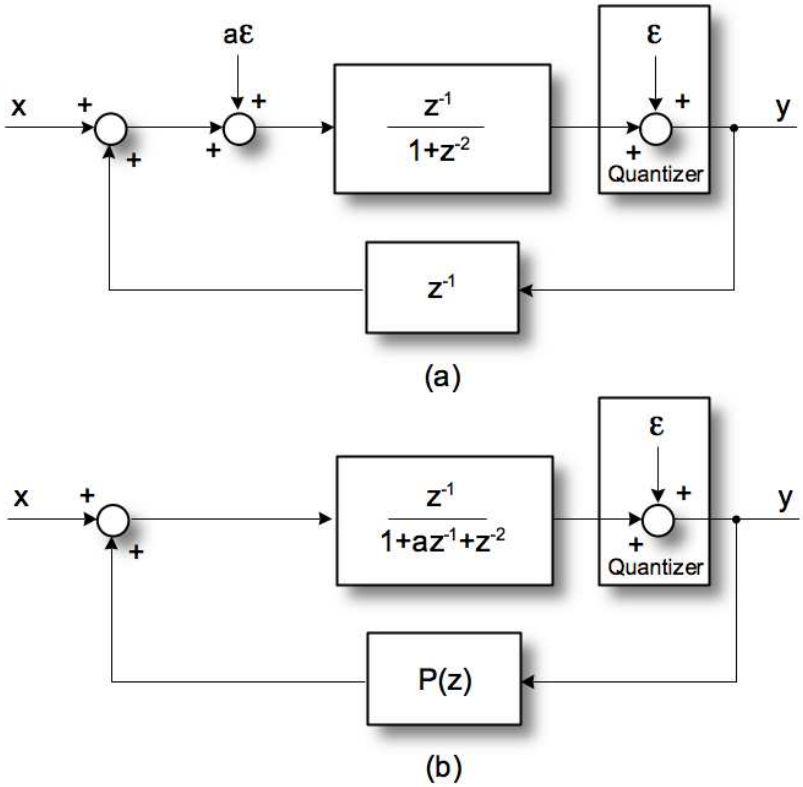

Figure 2.1: Second order band pass ΣΔ modulators with the injection of the quantization error (Fig. on top), and with the use of resonator (Fig. on bottom).

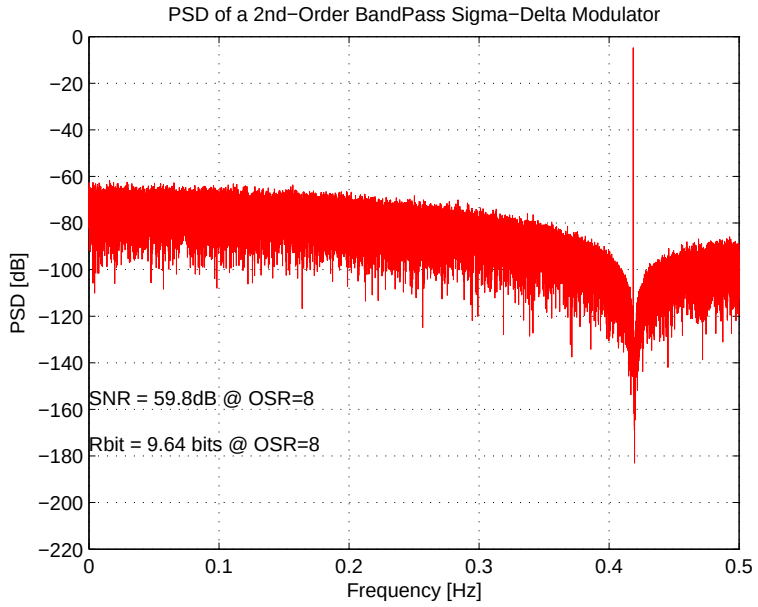

Figure 2.2: Spectrum of a second order band pass ΣΔ modulator. *FFT* with $N = 2^{17}$ points and $f_{in} = 0.418\ f_s$.

$$NTF = \left(1 + a_1 z^{-1} + z^{-2}\right)\left(1 + a_2 z^{-1} + z^{-2}\right) = \left(1 + z^{-2}\right)^2 + z^{-1}\left(a_1 + a_2\right)\left(1 + z^{-2}\right) + a_1 a_2 z^{-2} \tag{2.3}$$

Therefore, in order to obtain (2.3), it is necessary to synthesize the missing terms $z^{-1}(a_1 + a2)(1 + z^{-2})$ and $a_1 a_2 z^{-2}$. A second order scheme has two inputs that can be both used to synthesize terms of the *NTF*. Considering the scheme of Fig. 2.3(a), the injection of the quantization noise ϵ multiplied by K_1 and K_2 respectively yields

$$NTF = \left(1 + z^{-2}\right)^2 + K_1 STF + K_2 STF_1 \tag{2.4}$$

where $STF = z^{-1}$ and $STF_1 = z^{-1}(1+z^{-2})$ is the signal transfer function from the second input to the output. The two degrees of freedom, K_1 and K_2, enable multiple solutions, for example $K_1 = (a_1 + a_2)(1 + z^{-2}) + a_1 a_2 z^{-1}$, $K_2 = 0$. However, since the quantization error involves the subtraction of an analog quantity, it is worth using just a single delay. Therefore, a more convenient solution is using $K_1 = a_1 a_2 z^{-1}$ and $K_2 = a_1 + a_2$. Observe that the use of injecting paths worsens the feedback factor of the integrators used in the circuit and increases the load of the last stage. Therefore, it is necessary to increase the bandwidth and the slew-rate of the used op-amps or OTA to obtain the same performance.

The modulator of Fig. 2.3(b) uses two resonators with transfer function (2.5) to obtain the desired *NTF* zeros.

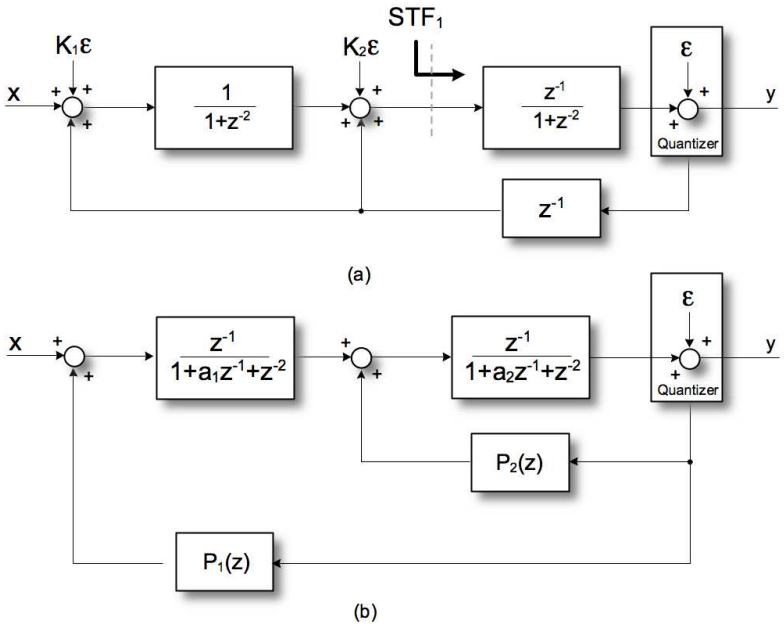

Figure 2.3: Fourth order band pass ΣΔ modulators with the injection of the quantization error (Fig. on top), and using resonators (Fig. on bottom).

$$H_{i,j}(z) = \frac{z^{-1}}{1 + a_{i,j}z^{-1} + z^{-2}}, \tag{2.5}$$

with i=1,2. However, the *STF* is

$$STF = \frac{z^{-2}}{D_1 D_2 - P_1 z^{-2} - P_2 z^{-1} D_1}, \tag{2.6}$$

where $D_{1,2} = 1 + a_{1,2}z^{-1} + z^{-2}$, with the same denominator in the NTF. Since the degree of the denominator of this *STF* is four, it is necessary to adjust the value of four parameters to make it equal to 1. Therefore, the feedback blocks $P_1(z)$ and $P_2(z)$ must of the form $P_1(z) = b_1 + c_1 z^{-1}$ and $P_2(z) = b_2 + c_2 z^{-1}$, respectively. The coefficients b_1, b_2, c_1, and c_2 that lead to $STF = z^{-2}$ are the solutions of the system of equations

$$\begin{cases} 1 - c_2 = 0 \\ 2 + a_j a_i - b_1 - b_2 a_j - c_2 = 0 \\ a_j + a_i - c_1 - b_2 - c_2 a_j = 0 \\ a_i + a_j - b_2 = 0 \end{cases}. \tag{2.7}$$

Both methods enable designing a band pass transfer function with a_1=13/8, a_2=14/8. The use of a 4-bit quantizer and OSR equal to 8 yields an SNR equal to 78.6 dB.

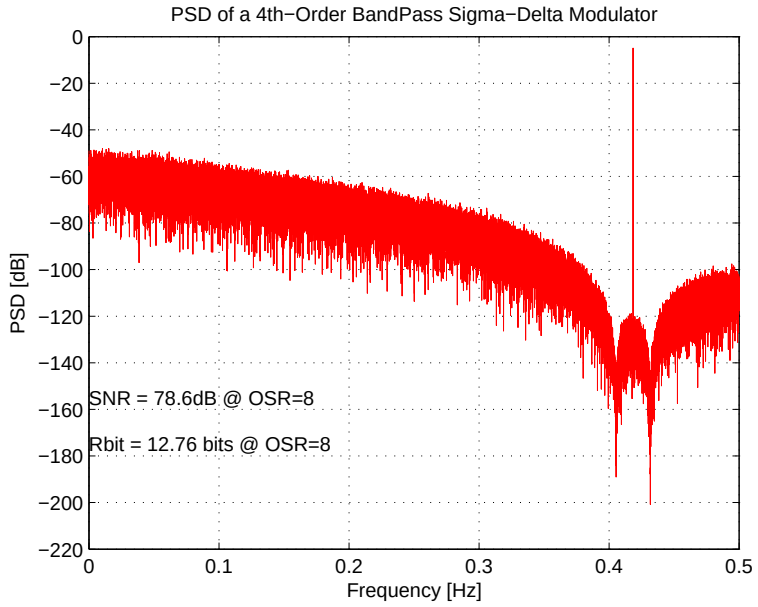

Figure 2.4: Spectrum of a fourth order band pass ΣΔ modulator. *FFT* with $N = 2^{17}$ points and $f_{in} = 0.418\ f_s$.

MASH Architecture

A method used to obtain high-order noise shaping is the multi-stage noise shaping (MASH) [5]. The same approach can be used in band pass architectures to achieve multiple pair of zeros [4]. However, for wide signal bands, instead of having multiple zeros in the *NTF*, it is better to distribute the zeros around the IF. The result is obtained by the cascade of a number of second order band pass modulator, as shown in Fig. 2.5. Each modulator gives rise to a term of equation (2.1) with its own coefficient a_i. The digital combination of outputs that cancels the quantization errors of the antecedent modulators is:

$$Y = y_1 z^{-(N-1)} - y_2 z^{-(N-2)} NTF_1 - y_3 z^{-(N-3)} NTF_1 NTF_2 - ... + y_N NTF_1 NTF_2 ... NTF_N, \quad (2.8)$$

where it is assumed that all the STF are z^{-1}. For three stages the result yields

$$Y = xz^{-3} + \epsilon_3 NTF_1 NTF_2 NTF_3, \quad (2.9)$$

Therefore, each stage of the MASH architecture defines a pair of complex zeros whose combination gives rise to an output spectrum like the one shown in Fig. 2.6 (case of three cascaded stages). The three stages use a_1=13/8, a_2=14/8, and a_3=15/8. With a 4-bit quantizer and OSR equal to 8, the resulting SNR is 95 dB.

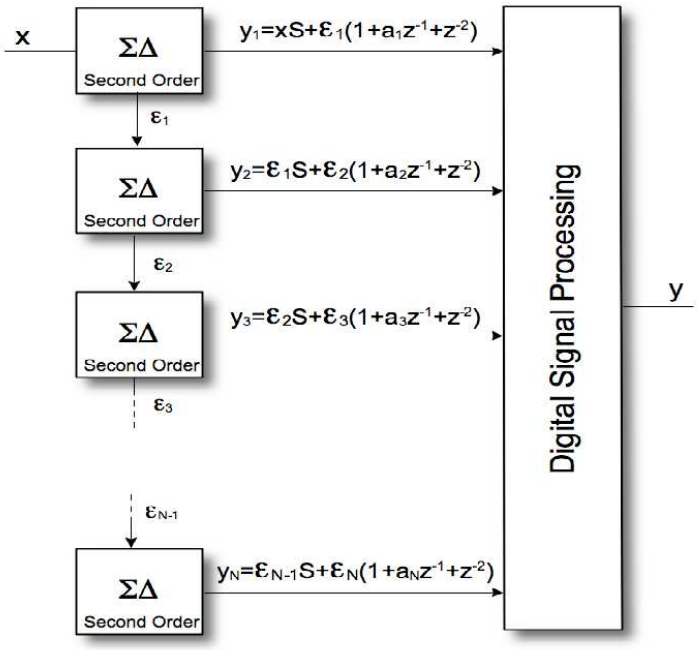

Figure 2.5: MASH architecture. $S = z^{-1}$ is the signal transfer function.

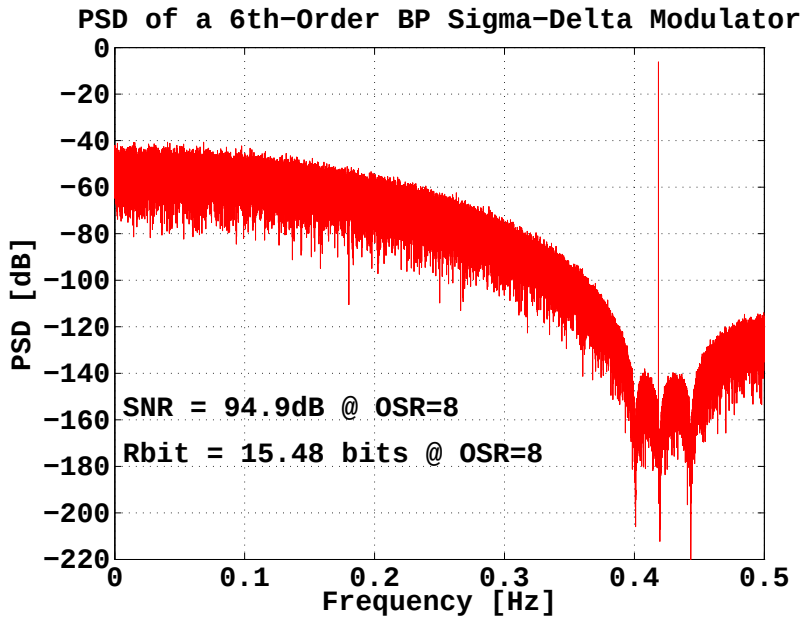

Figure 2.6: Spectrum of a sixth order MASH (2+2+2) 4-bit band pass ΣΔ modulator. *FFT* with $N = 2^{17}$ points and $f_{in} = 0.418\ f_s$.

2.2.2 Basic Block Design

The realization of a $z^{-1}/(1 + kz^{-1} + z^{-2})$ transfer function with $k < 1$ can be done with single path architecture using the resonator of Fig. 2.7.

It is difficult to obtain the transfer function with $k > 1$. However, this can be possibly achieved by replacing the integrators with pseudo-integrators $z^{-1}/(1 + z^{-1})$ or $(1 + z^{-1})$. In both cases two op amps switched at the sampling frequency are necessary. A more power effective method uses two-path architectures with twice the number of op-amps switched at half of the clock frequency. The power of each op-amp is almost divided by four and the overall power halved. The two-path scheme realizes the $z \rightarrow -z^2$ transformation, while suitable cross-coupled feedbacks give the kz^{-1} term, as shown in Fig. 2.8.

An $f_{ck}/4$ square wave modulation at input and output of conventional integrators running at $f_{ck}/4$ allows achieving $1/(1 + z^2)$. The phase control of the output interpolator provides a z^{-1} delay. The scheme of Fig. 2.1(a) can be realized with a two-path architecture. Fig. 2.9 shows how to achieve the result.

The architecture uses two feedback loops including a $z^{-1}/(1 + z^{-2})$ block and a quantizer. The quantization noise ϵ_1 and ϵ_2 are cross coupled and multiplied by k in order to obtain the missing term. Since quantization occurs with a z^{-1} delay synchronously with the injection in the complementary path, the $(1 + z^{-2})\epsilon_1$ noise will show up on the top output, while $k \cdot z^{-1}\epsilon_1$ appears on the bottom path and vice-versa for ϵ_2. Therefore the time interleaving of y_1 and y_2 gives

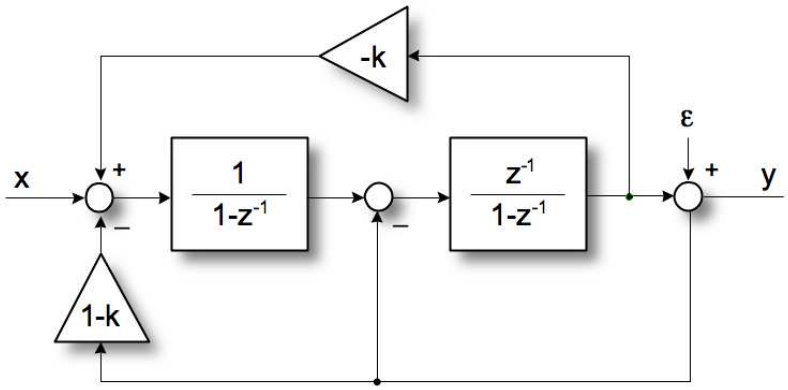

Figure 2.7: Single path resonator implementation.

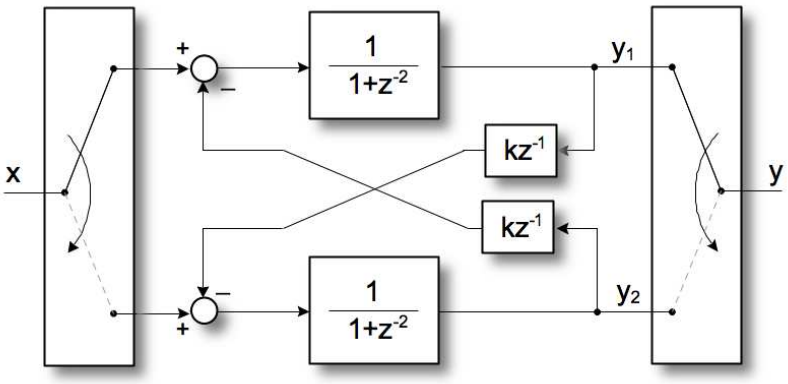

Figure 2.8: Band pass ΣΔ with Two-path resonators.

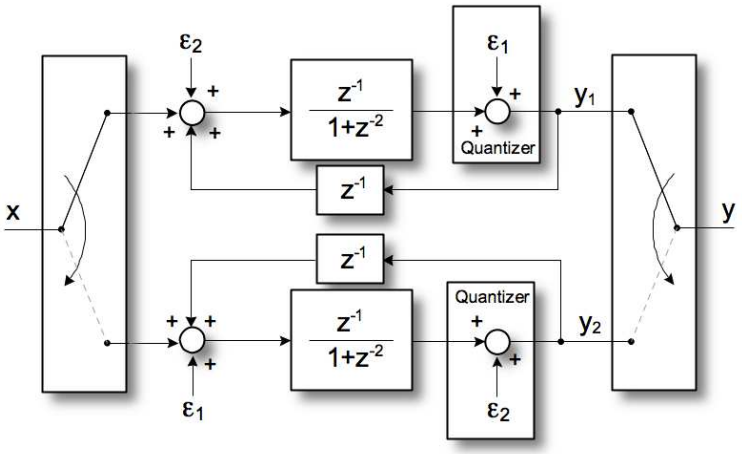

Figure 2.9: Two-path implementation of the architecture shown in Fig. 2.1(a).

$$y = x \cdot z^{-1} + \frac{\sqrt{\epsilon_1^2 + \epsilon_2^2}}{2}(1 + kz^{-1} + z^{-2}) \tag{2.10}$$

that accounts for the quadratic superposition of the quantization noises and the 50% duty cycle.

2.2.3 Sensitivity Analysis

The errors in implementing analog coefficients affect the signal and the noise transfer function. Assuming that the gain and the speed of op-amps are enough, the coefficient of z^p, with p the higher degree of the *NTF* polynomial, is equal to the product of the terms a_i contained in 2.1. If the zeros of the *NTF* are on the unity circle this coefficient is equal to one. So coefficients error can be admitted under the condition that zeros remain on the unity circle. Errors included in this range affect the position of *NTF* zeros, as shown in Fig. 2.10. Architectures of high order (Fig. 2.3 and Fig. 2.5) have been studied as a function of the a_i coefficients error, [6]. Fig. 2.10, on left, shows the zeros position of a fourth order *NTF* (a_1 = 13/8, a_2 = 15/8) with error Δ equal to 0 and 6.7%, respectively. When the error is as large as 6.7% a pair of zeros falls out of the unity circle, decreasing the modulator performance, and both zeros move from their original positions changing the implemented *NTF*. Fig. 2.10 on right, depicts the zeros position of a sixth order *NTF*. Also in this case, an error higher than 6.7% change the zeros position and cause the going out of a couple of zeros.

A statistical analysis estimates the *SNR* degradation caused by errors in a_i coefficients. The study of architectures in Figs. 2.3(a), 2.3(b) and 2.5 employed the Matlab-Simulink™environment, using a *FFT* with $N = 2^{17}$ points and $f_{in} = 0.418\ f_s$. All simulations use an error Δ equal to a normal distributed white random variable of zero mean,

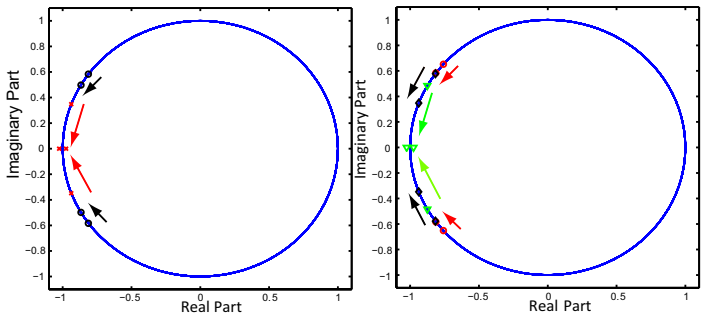

Figure 2.10: *NTF* zeros position (fourth order modulator on left; sixth order modulator on right) as a function of the error Δ.

with standard deviation (σ) equal to $2 \cdot 10^{-3}$. Simulation results are shown in Figs. 2.11 and 2.12.

With 1000 samples for each design, Fig. 2.11 shows that the *SNR* is higher than 74 dB in about 85% of total cases. Simulations on the MASH architecture for the fourth order shaping show a *SNR* higher than 74 dB in 83% of case; for a sixth order response, 87% of simulations gives a *SNR* higher than 90 dB. The results are in line with what obtained with special low sensitivity design techniques, [7].

2.3 Proposed Band Pass ΣΔ Modulator Architecture

The proposed ΣΔ modulator features a noise transfer function (*NTF*), given by

$$NTF = \prod_{i=1}^{4} \left(1 + a_i z^{-1} + z^{-2}\right), \tag{2.11}$$

where a_i ($i = 1, 2, 3, 4$) are real coefficients in the range $(-2, 2)$, in order to have complex conjugate zeros. Fig. 2.13 shows the zeros position around the unity circle, with the chosen coefficients values a_i: $a_1 = 12/8$, $a_2 = 13/8$, $a_3 = 14/8$, $a_4 = 15/8$. With these values, the zeros are very close to the the edge of the first Nyquist band.

The proposed ΣΔ modulator architecture, illustrated in Fig. 2.14, is based on a two-stage MASH structure: the first stage ($\Sigma\Delta_1$) realizes the external zeros, corresponding to $a_1 = 12/8$ and $a_4 = 15/8$, while the second stage ($\Sigma\Delta_2$) implements the zeros corresponding to $a_2 = 13/8$ and $a_3 = 14/8$. This leads to a first modulator *NTF* given by

$$NTF_1 = \left(1 + a_1 z^{-1} + z^{-2}\right)\left(1 + a_4 z^{-1} + z^{-2}\right), \tag{2.12}$$

while the *NTF* of the second modulator turns out to be

$$NTF_2 = \left(1 + a_2 z^{-1} + z^{-2}\right)\left(1 + a_3 z^{-1} + z^{-2}\right). \tag{2.13}$$

Being a MASH architecture, the second modulator receives as input the quantization error ϵ_1 of the first modulator, and the two digital outputs, Y_1 and Y_2, are processed by a digital

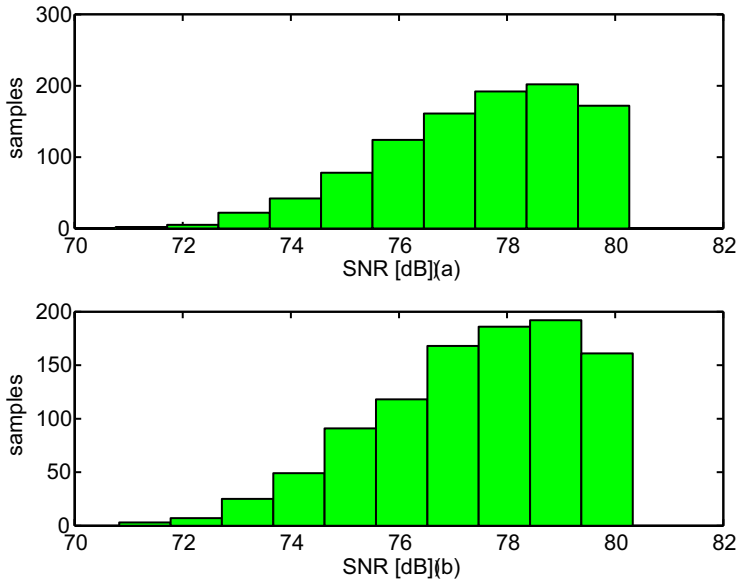

Figure 2.11: Simulated *SNR* of the fourth order modulator of Fig. 2.3(a) (top) and of the fourth order modulator of Fig. 2.3(b) (bottom).

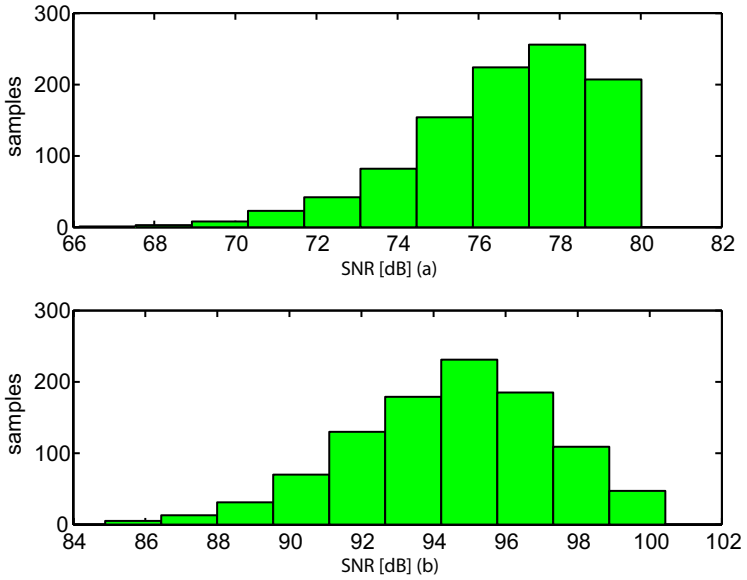

Figure 2.12: *SNR* of a fourth order (a) and a sixth order (b) MASH modulator (Fig. 2.5).

filter, to cancel the quantization error of the first modulator and realize the overall *NTF* given by (2.11).

By inspection of the circuit, the outputs of the first and second modulator are given by

$$\begin{cases} Y_1 = In \cdot STF_1 + \epsilon_1 \cdot NTF_1 \\ Y_2 = \epsilon_1 \cdot STF_2 + \epsilon_2 \cdot NTF_2 \end{cases}, \tag{2.14}$$

where $STF_1 = STF_2 = z^{-2}$ are the signal transfer functions of each modulator. The digital filter implements the function

$$Out = Y_1 \cdot z^{-2} - Y_2 \cdot NTF_1, \tag{2.15}$$

thus canceling the quantization error of the first modulator shaped by NTF_1 and leading to the desired output, given by

$$Out = In \cdot z^{-4} + \epsilon_2 \cdot \prod_{i=1}^{4} \left(1 + a_i z^{-1} + z^{-2}\right). \tag{2.16}$$

Both band pass ΣΔ modulators used in the MASH structure are based on the same architecture, whose block diagram is shown in Fig. 2.15. This modulator realizes a *NTF* with two couples of complex conjugate zeros. The coefficients values for the two modulators are different: for modulator $\Sigma\Delta_1$ it's used $a_j = 12/8 = a_1$ and $a_i = 15/8 = a_4$, while for modulator $\Sigma\Delta_2$ $a_j = 13/8 = a_2$ and $a_i = 14/8 = a_3$.

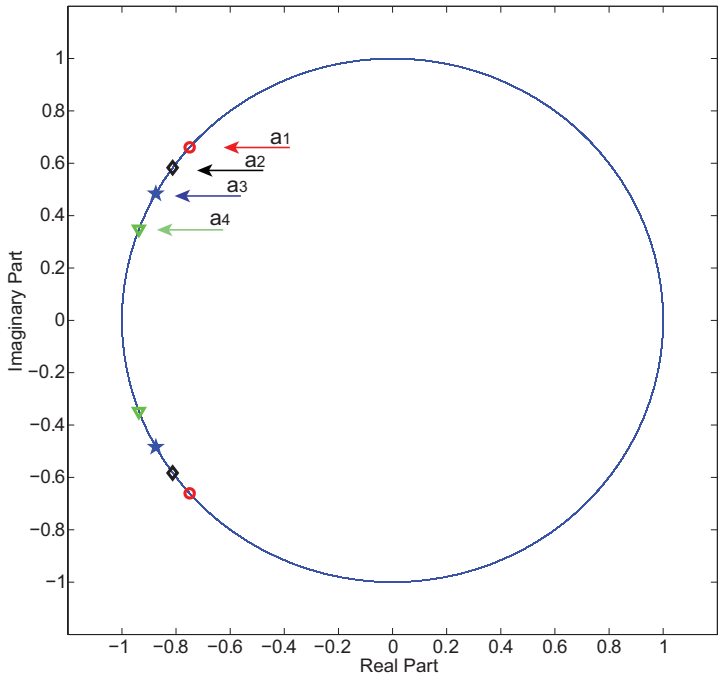

Figure 2.13: Desired position of the *NTF* zeros around the unity circle.

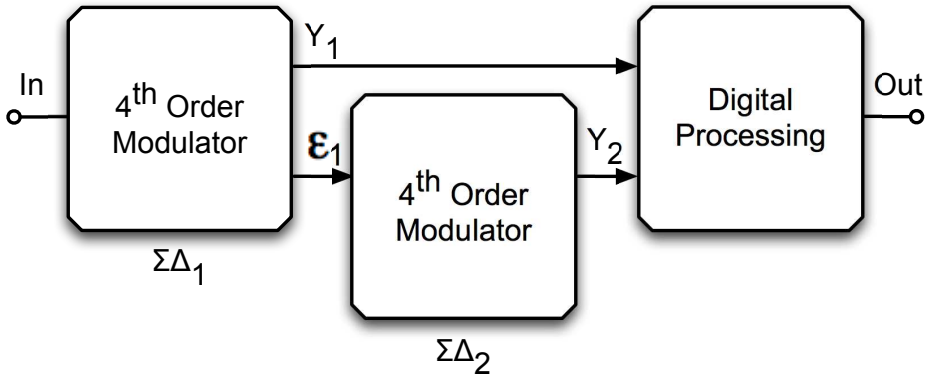

Figure 2.14: Block diagram of the proposed MASH band pass ΣΔ modulator.

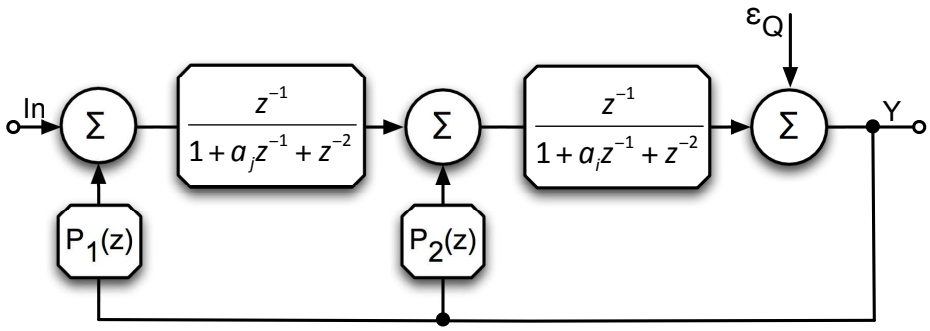

Figure 2.15: Block diagram of each band pass ΣΔ modulator.

To implement the desired *NTF*, each ΣΔ modulator requires two resonators with transfer function

$$H_{i,j}(z) = \frac{z^{-1}}{1 + a_{i,j}z^{-1} + z^{-2}}. \tag{2.17}$$

As a result, the *STF* is

$$STF = \frac{z^{-2}}{D_j D_i - P_1 z^{-2} - P_2 z^{-1} D_j}, \tag{2.18}$$

where $D_{i,j} = 1 + a_{i,j}z^{-1} + z^{-2}$. Since the degree of the denominator in this *STF* is four, it is necessary to adjust the value of four parameters to make it equal to 1. Therefore, the blocks $P_1(z)$ and $P_2(z)$ must of the form $P_1(z) = b_1 + c_1 z^{-1}$ and $P_2(z) = b_2 + c_2 z^{-1}$, respectively. The values of coefficients b_1, b_2, c_1, and c_2 that lead to $STF = z^{-2}$ are obtained by solving the system of equations

$$\begin{cases} 1 - c_2 = 0 \\ 2 + a_j a_i - b_1 - b_2 a_j - c_2 = 0 \\ a_j + a_i - c_1 - b_2 - c_2 a_j = 0 \\ a_i + a_j - b_2 = 0 \end{cases}. \tag{2.19}$$

2.3.1 Two-Path Approach

A power-effective method to implement the ΣΔ modulator in Fig. 2.15 is to use a two-path architecture, with twice the number of operational amplifiers, operated at half of the clock frequency ($F_s/2$ = 90 MHz). The power consumption of each opamp is almost divided by four and the overall power consumption is then halved. Fig. 2.16 shows the adopted solution to implement the band pass ΣΔ modulator of Fig. 2.15, using the two-path design approach.

The even and odd input samples are applied to the input of the top and bottom path, respectively, at the sampling rate (F_s). The feedback coefficients used to make the *STF* denominator equal to one are realized with direct (c_1 and c_2) or cross-coupled paths (b_1 and b_2). At the ΣΔ modulator output the digital data are taken alternatively from both paths

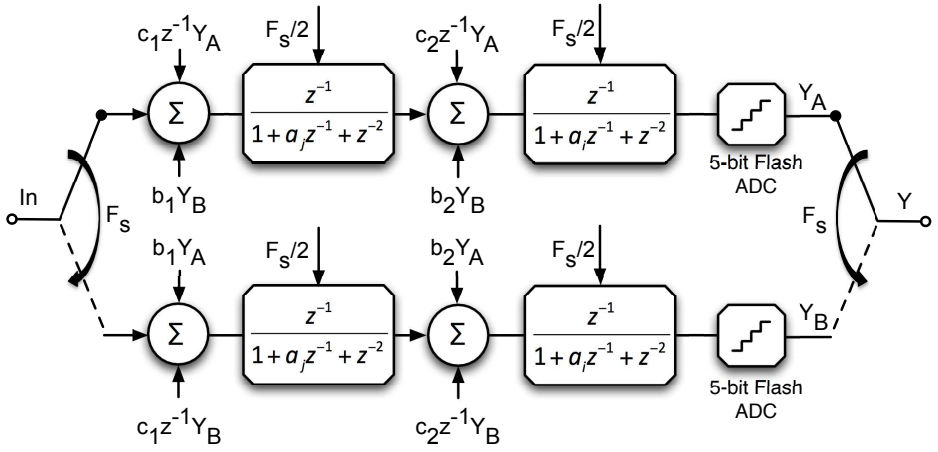

Figure 2.16: Band pass ΣΔ modulator implemented with two-path architecture.

at sampling frequency F_s. The modulator is realized using four switched-capacitor (SC) integrators and two 5-bit flash ADCs. Since the solutions of (2.19) are integer multiples of the fraction $1/8$, with the considered values of coefficients a_i ($i = 1, 2, 3, 4$), it is relatively easy to implement the feedback coefficients by capacitive ratios in the SC circuits. Considering the two-path ΣΔ modulator of Fig. 2.16, the resonators can be implemented using the structure illustrated in Fig. 2.17.

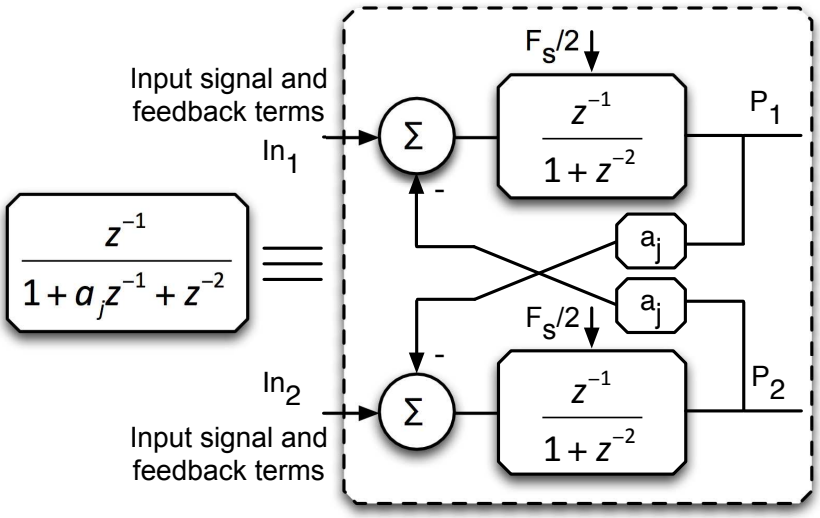

Figure 2.17: Resonator implementation in the two-path architecture.

The two-path architecture, indeed, allows to easily realize a $z \rightarrow z^2$ transformation ($F_s \rightarrow F_s/2$) and a $z \rightarrow -z$ transformation by a square wave modulation at $F_s/4$ [21] at

the input and at the output of a conventional integrator with transfer function

$$H(z) = \frac{z^{-1/2}}{1 - z^{-1}}, \tag{2.20}$$

as conceptually explained in Fig. 2.18, thus implementing the transfer function

$$\hat{H}(z) = \frac{z^{-1}}{1 + z^{-2}}. \tag{2.21}$$

Moreover, suitable cross-coupled feedback paths in the integrators allow to obtain the $a_{j,i}z^{-1}$ terms in the resonator transfer function.

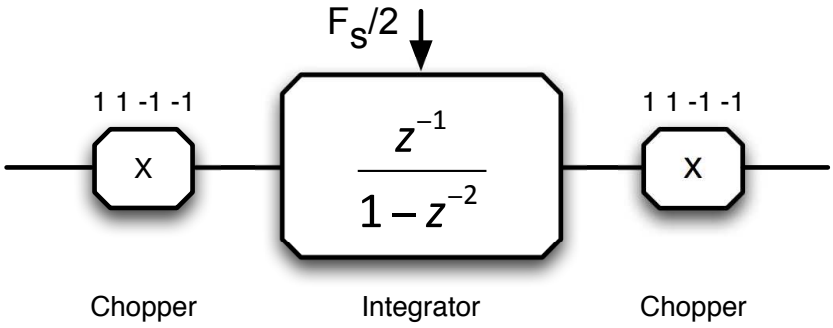

Figure 2.18: Implementation of the transfer function $\hat{H}(z)$, using a $z^2 \rightarrow -z^2$ transformation on a conventional integrator running at $F_s/2$.

Considering the block diagram of Fig. 2.17, the output signals P_1 and P_2 are given by

$$\begin{cases} P_1 = \left(In_1 - a_j P_2\right) \dfrac{z^{-1}}{1 + z^{-2}} \\ P_2 = \left(In_2 - a_j P_1\right) \dfrac{z^{-1}}{1 + z^{-2}} \end{cases}. \tag{2.22}$$

By adding the values of P_1 and P_2 given by (2.22), results

$$P_1 + P_2 = \frac{z^{-1}}{1 + a_j z^{-1} + z^{-2}} \left(In_1 + In_2\right), \tag{2.23}$$

leading to the desired expression of $H_{i,j}$, given by (2.17).

2.3.2 Behavioral Simulation Results

The proposed MASH band pass ΣΔ modulator architecture is verified at the behavioral level using Matlab-Simulink™. The simulations are carried-out with oversampling ratio (*OSR*) equal to 9 and input frequency around 73.74 MHz ($F_{in} = F_s \cdot N_{per}/N$, where F_s = 180 MHz is the sampling frequency, $N_{per} = 839$ is the prime number of periods of the input

signal considered, and $N = 2^{11}$ is the number of points used in the FFT). Fig. 2.19 shows the output spectrum under ideal conditions. In the spectrum it is possible to clearly note the four couples of complex zeros in the signal band. The obtained signal-to-quantization-noise ratio (*SQNR*) is higher than 116 dB.

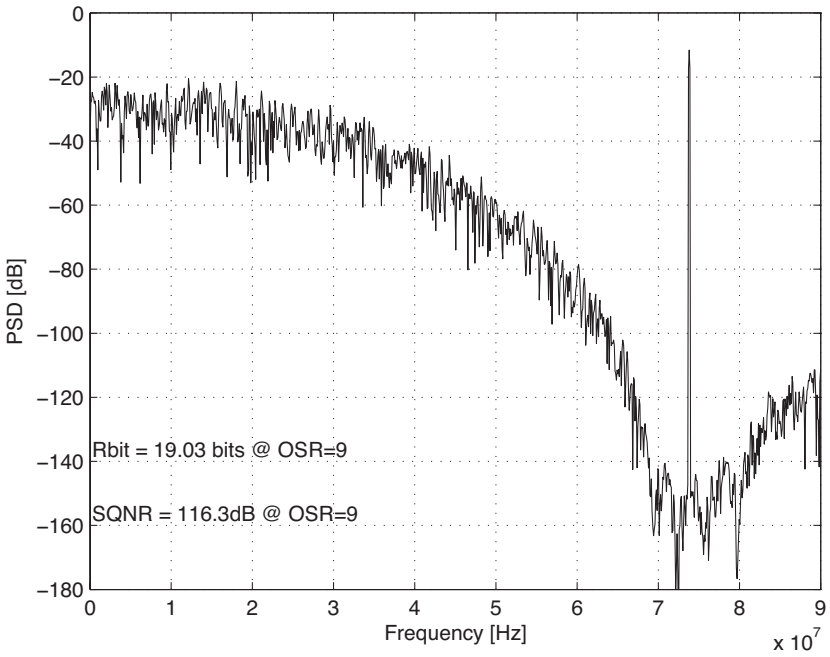

Figure 2.19: Output spectrum of the proposed ΣΔ modulator under ideal conditions.

The errors in coefficients values, caused by real integrators and capacitive mismatches, affect the *STF* and the *NTF* of both modulators of the MASH structure. In particular, in order to guarantee the stability of the modulator, it has to make sure that, in spite of any errors, the poles of the *NTF* do not fall outside the unity circle. Moreover, since the digital filter has to remove the first modulator quantization noise (shaped by its *NTF*), the implementation of the first modulator *NTF* has to be carefully considered. The MASH structure is, hence, analyzed using real integrators using a specific toolbox [12]. The used integrators parameters are: DC gain 1000 V/V, slew-rate of 500 V/µs, unity gain frequency of 1 GHz, and sampling capacitance (which is used for modeling the kT/C noise) equal to 1.2 pF. The resulting simulated output spectrum, reported in Fig. 2.20, shows that it is possible to achieve a resolution of 13.6 bit with a signal bandwidth of 10 MHz. The noise floor present in the signal band is mainly due to the kT/C noise contribution. In order to verify the effect of capacitive mismatches on the performances of the proposed ΣΔ modulator, a statistical analysis it's performed, introducing random normally distributed coefficient errors with zero mean and standard deviation $\sigma = 5 \cdot 10^{-3}$. The results achieved over 100 simulations, as shown in Fig. 2.21, demonstrate the robustness and the effectiveness of the

used topology and are in line with the performance of low-sensitivity, high-resolution band pass ΣΔ modulators.

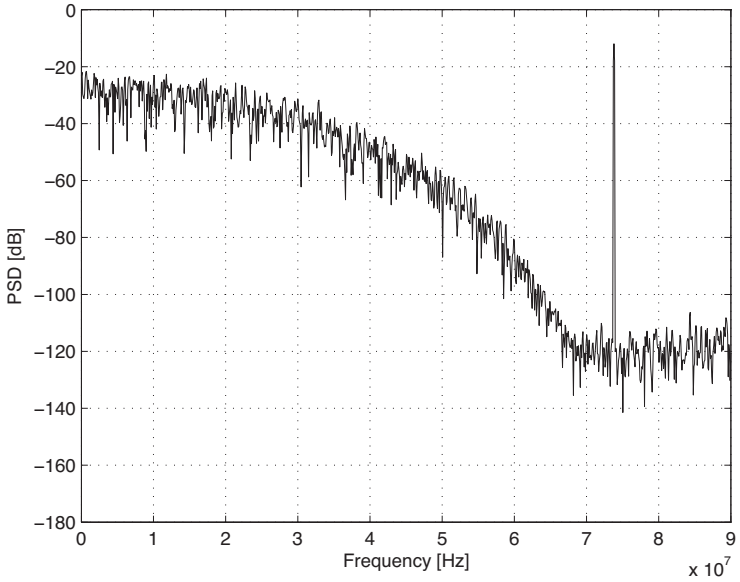

Figure 2.20: Output spectrum of the proposed ΣΔ modulator with real integrators.

2.4 Circuit Design

This section explains the circuit design at the transistor level for the blocks used in the modulator. There are the description of the operational amplifier, the comparator, the 5-bit flash and the integrators. Each block is illustrated with simulations at transistor level and Monte Carlo analysis. Corner simulations are not included because these models were not available.

2.4.1 Operational Amplifier

The operational amplifier is a fully differential two stage op-amp with RC compensation and discrete time common mode feedback. The first integrator in the first modulator has unity capacitor bigger than the ones in the other integrators to respect the kT/C noise limitation (see 3.3.4), so the op-amp in the first integrator of the first modulator has a different design respect the others. The op-amps performances are shown in Tab. 2.2, where the first line is referred to the op-amp for the first integrator of the first modulator, while the second line is referred to the other op-amp.

Fig. 2.22 shows the gain and the phase margin in standard conditions, of the op-amp for the first integrator in the first modulator.

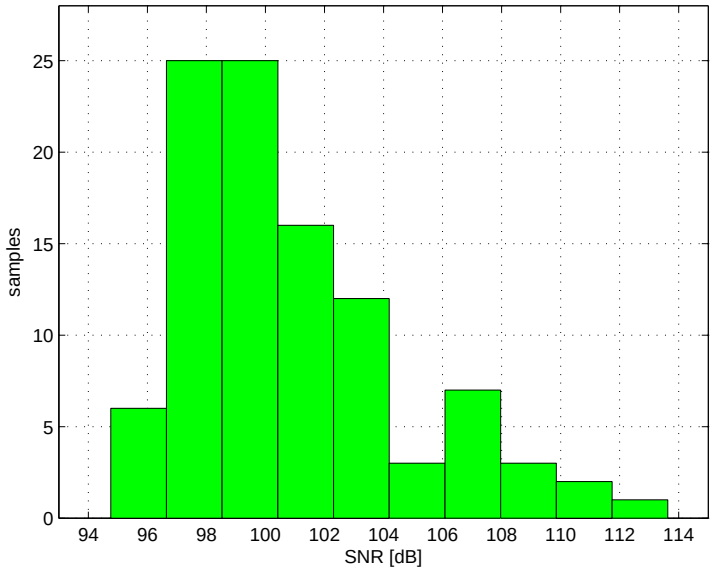

Figure 2.21: Simulated *SNR* (100 runs) considering errors in all the coefficient values ($\sigma = 5 \cdot 10^{-3}$).

Table 2.2: Op-amp performances.

	Gain	**Slew-rate**	**Bandwidth**	**Phase margin**	**Power consumption**
first op-amp	80 dB	480 μV/s	910 MHz	61 degree	10 mW & 1.8 V
other op-amp	65 dB	505 μV/s	890 MHz	65 degree	7.3 mW & 1.8 V

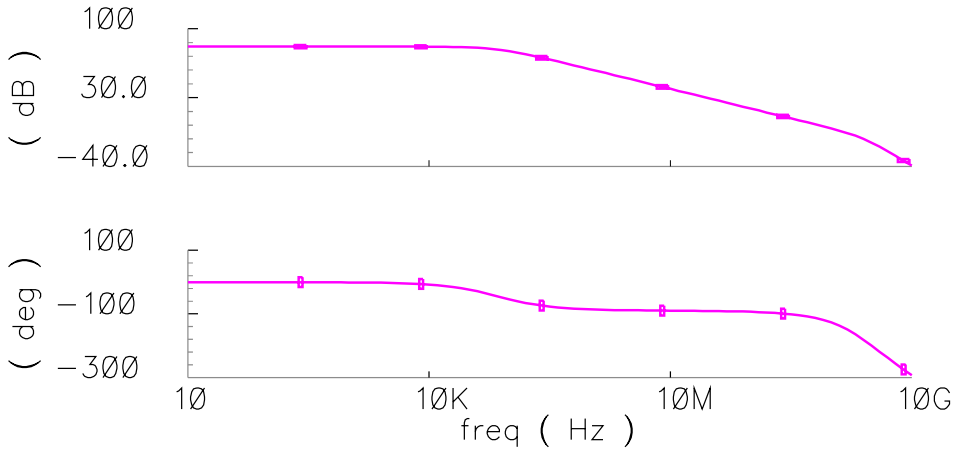

Figure 2.22: First op-amp gain and phase margin.

Fig. 2.23 shows the gain and the phase margin in standard conditions in the op-amp for the other integrators.

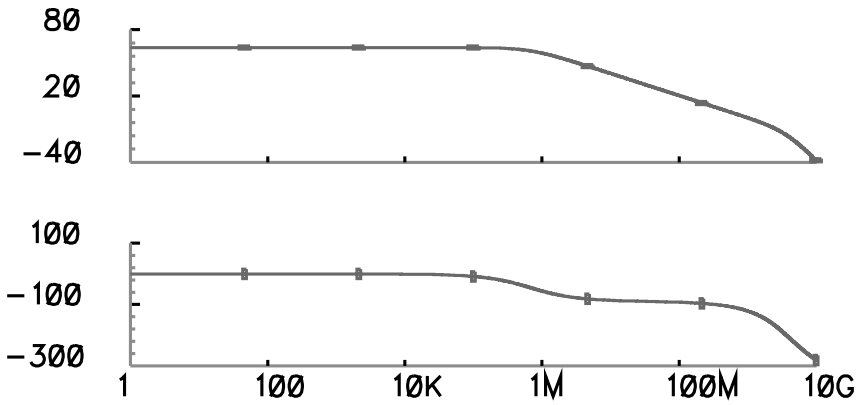

Figure 2.23: Second op-amp gain and phase margin.

Fig. 2.24 shows the time step response of the first op-amp.

Fig. 2.25 shows the time step response in the op-amp in other integrators.

Monte Carlo analysis with 100 runs shows that the gain is higher than 73 dB in the first op-amp and higher than 60 dB in the other one, in 93% of total cases. The layout, including the common-mode feedback circuit, is 400 μm X 60 μm in the first op-amp, and 360 μm X 60 μm in the other.

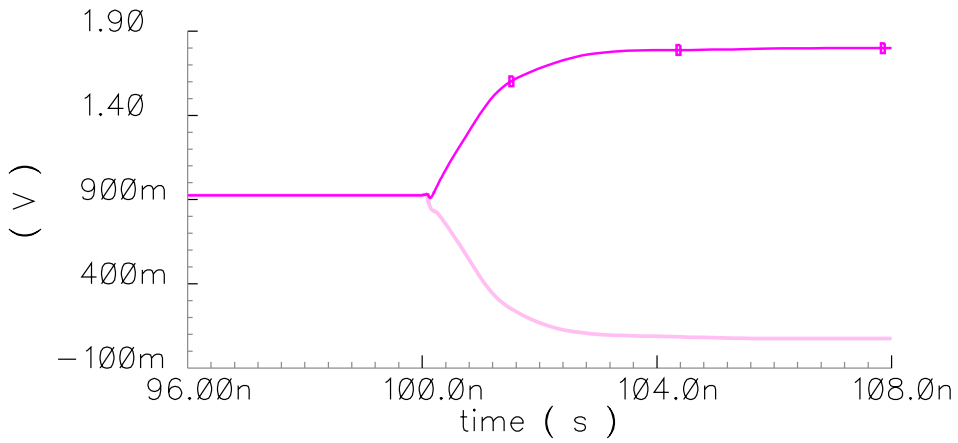

Figure 2.24: Step response of the first op-amp.

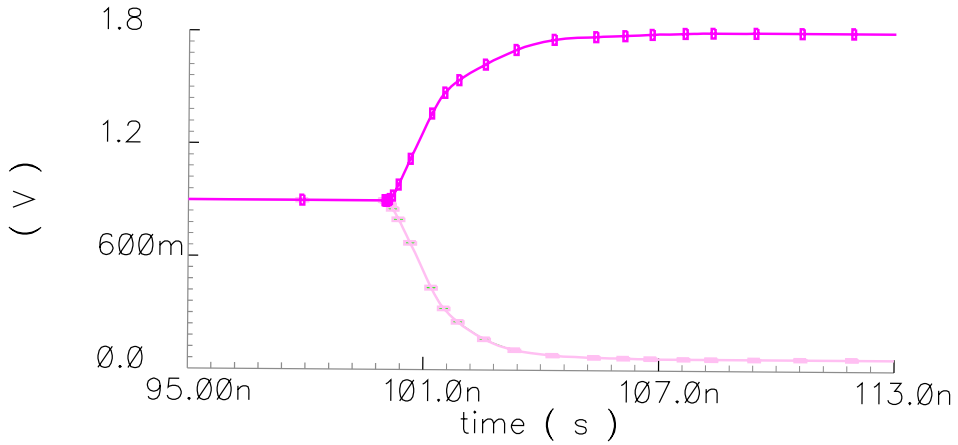

Figure 2.25: Step response of the second op-amp.

2.4.2 Comparator

Fig. 2.26 shows the scheme of the used comparator: it is composed by a pre-amplifier stage and a latch. The pre-amplifier is a fully differential structure made by two cross-coupled differential pairs. The latch uses a double positive feedback. The reset on NMOS ensures the reduction of the dynamic current consumption. The common mode feedback in the amplification stage is not shown in the picture and is made by two NMOS that realize a resistive degeneration under the current source of the differential pairs. The power consumption is 0.11 mW with a power supply of 1.8 V.

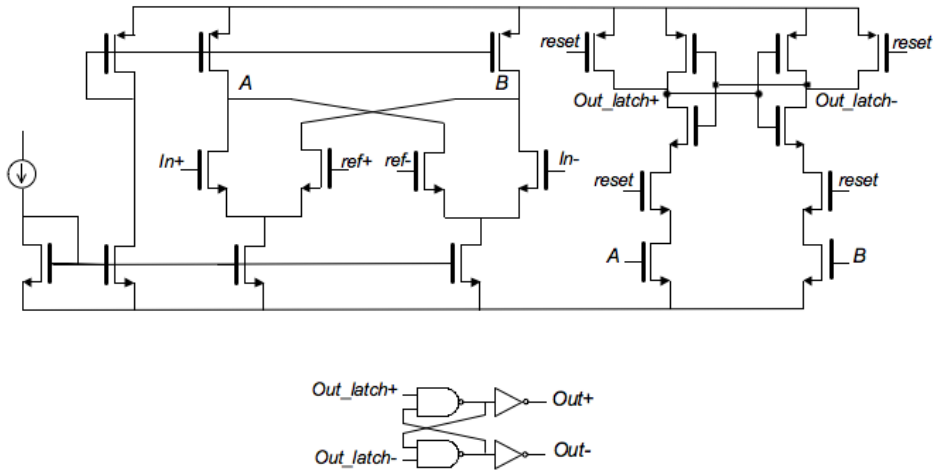

Figure 2.26: Comparator scheme.

Monte Carlo analysis with 100 runs shows that with a half LSB sensitivity, the outputs are correct in 95% of total cases. The layout is 45 μm X 60 μm.

2.4.3 5-bit Flash ADC

The 5-bit flash is made using the comparator shown in Fig. 2.26. Fig. 2.27 depicts the output spectrum of the implemented 5-bit flash: the resolution is 4.8 bit and the power consumption is 3.41 mW with a power supply of 1.8 V. The simulation is done with a sampling frequency of 90 MHz[1], input frequency of about 35 MHz, and FFT with 2048 points.

Fig. 2.28 shows the results of a Monte Carlo analysis with five runs on the designed 5-bit flash ADC. In all cases the resolution is higher than 4.55 bit.

The layout is 320 μm X 360 μm.

[1]Each path works at this frequency so the flash is tested at 90 MHz.

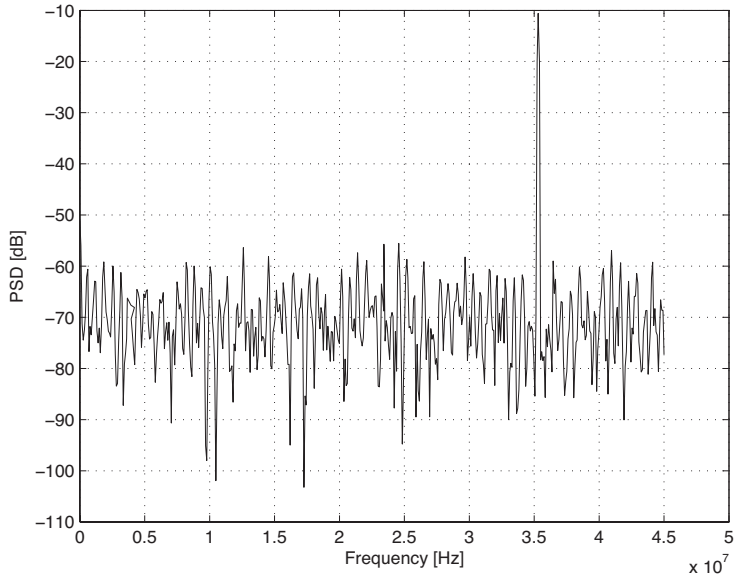

Figure 2.27: 5-bit ADC flash spectrum at the transistors level.

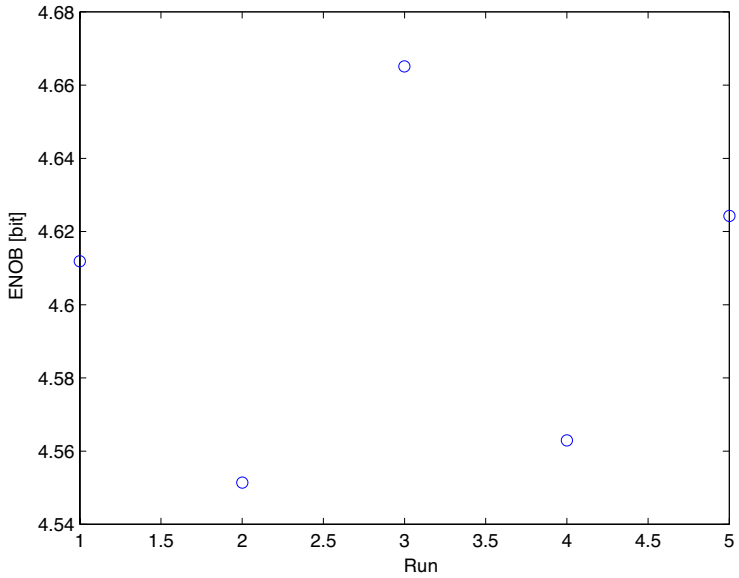

Figure 2.28: Statistical analysis of the 5-bit flash.

2.4.4 SC integrator

The eight integrators are implemented using a switched capacitor (SC) differential circuits approach. Each integrator has to realize function like the one depicted in Fig. 2.29.

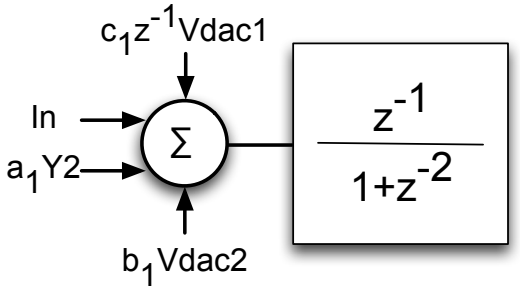

Figure 2.29: SC integrator scheme.

The different coefficients in the modulator are integer multiple of the fraction 1/8 so the integrator capacitors are made by eight unity capacitors. The first integrator capacitors in the first modulator has unity value of 150 fF to respect the kT/C noise limit. The other capacitors are chosen big enough to overcome drawback related to mismatch. The available poly-poly capacitors have a mismatch equal to $\frac{0.3\%}{\sqrt{WL}}$, where W and L are the capacitors dimensions, expressed in μm. Considering the mismatch limitations, capacitors in the other integrators are 50 fF. The kT/C noise is analyzed in 3.2.2 at the behavioral simulation. Considering the kT/C noise limit, it is possible to calculate the first integrator capacitors value by the analysis of the model in Fig. 2.30. This figure shows a conceptual view of the first integrator in the first modulator. The feedback capacitor is made by eight unity capacitances, while on the virtual ground there are twenty-two unity capacitances.

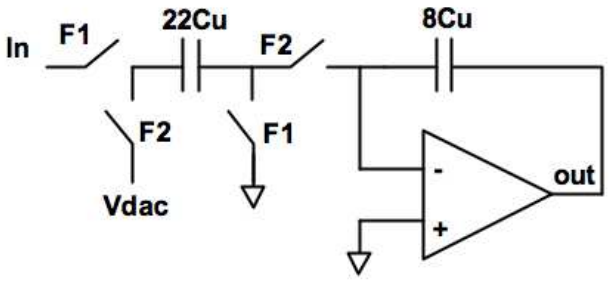

Figure 2.30: Model for the kT/C noise limit.

The contribution gives by the kT/C noise could be calculate considering the total noise charge Q^2_{nTOT}, given by:

$$Q_{nTOT}^2 = 22 \cdot 2 \cdot Q_n^2, \tag{2.24}$$

where twenty-two is the number of capacitors used to inject the charge into the integrator during a single clock period, $Q_n^2 = kT \cdot C_u$ is the noise charge of a singular capacitor, and the factor 2 is considered to taking in account the double injection in the integrator (term with and without delay, V_{dac} and In, respectively). T is the temperature expressed in Kelvin and k is the Boltzmann constant equal to 1.38 $10^{-23} \frac{J}{K}$. The total noise V_n^2 is equal to

$$V_n^2 = \frac{Q_{nTOT}^2}{C_{TOT}^2}, \tag{2.25}$$

where $C_{TOT} = 8C_u$ is the total integrator capacitance.

Considering a full scale of 1.1 V and a resolution target bigger than 13 bit, the LSB of the modulator is:

$$LSB = \frac{V_{FS}}{2^{ENoB}} = \frac{1.1\ V}{2^{13}} = 134\ \mu V. \tag{2.26}$$

The noise V_n must be less than the LSB,

$$V_n = \sqrt{44}\sqrt{\frac{kT \cdot C_u}{64 \cdot C_u^2}} < LSB = 134\ \mu V, \tag{2.27}$$

so the unity capacitor C_u must be higher than

$$C_u > \frac{44}{64}\frac{kT}{LSB^2} = 156\ fF. \tag{2.28}$$

Fig. 2.31 shows a possible arrangement of the integrators used in the modulator. Y_2 is the out of the other path integrator used to implement the resonator, and $V_{dac1,2}$ are use to generate the feedback coefficients.

The DACs used in the modulator are resistive string with poly resistance.

Fig. 2.32 shows the spectrum simulated at the transistor level and considering mismatch in capacitors and in resistors DACs. Capacitor mismatch is calculated by the previous, while resistors mismatch is $\frac{1.33\%}{\sqrt{WL}}$, where W and L are the resistors dimensions, expressed in μm.

The integrators layout in the first $\Sigma\Delta$ are: 490 μm X 380 μm in the first integrator, and 490 μm X 380 μm in the second one. In the second modulator the layout integrators are: 400 μm X 300 μm for the first SC, and 400 μm X 300 μm in the second one.

2.4.5 Layout

Fig. 2.33 represents the chip layout in 0.18-µm CMOS technology, with two poly and six metals. The chip area is 1.84 mm X 1.84 mm, including the pad-ring . In the layout picture are clearly visible the first and the second modulator, and four integrators and two

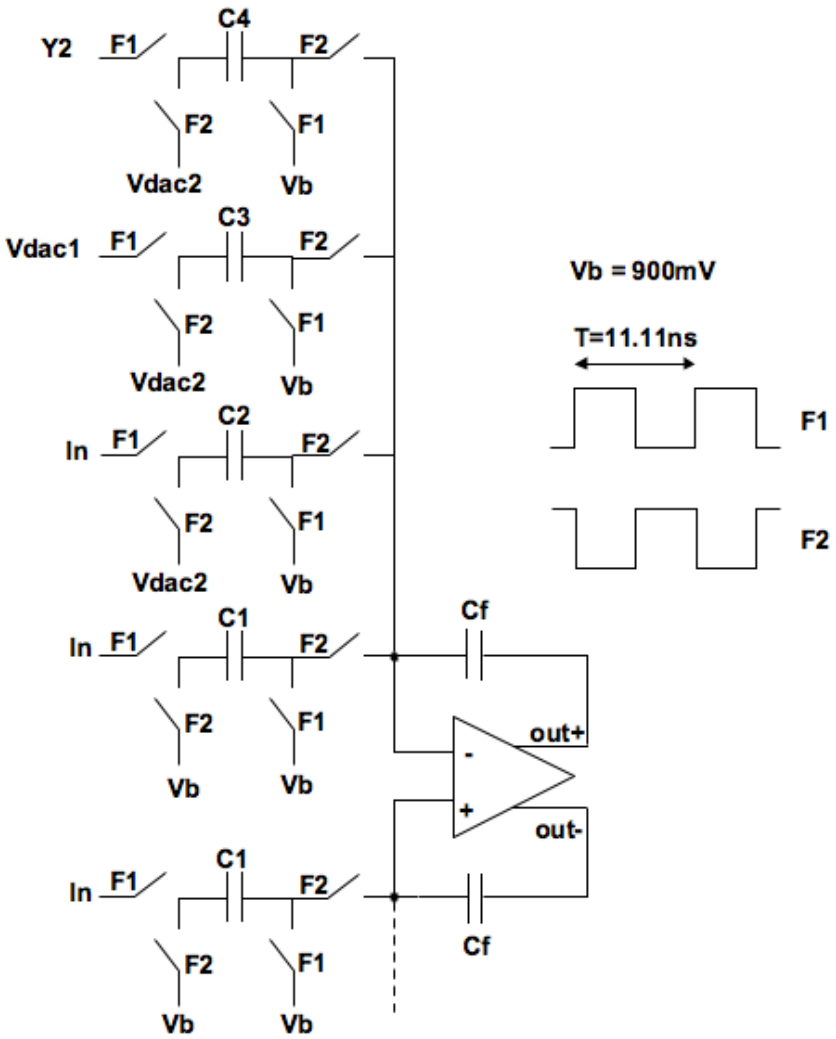

Figure 2.31: SC integrator scheme.

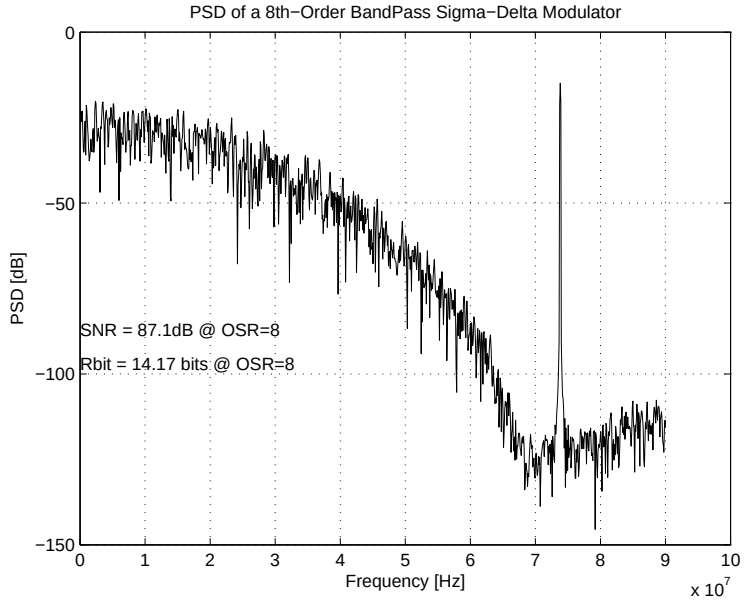

Figure 2.32: Output spectrum of the MASH introducing mismatches in the capacitors integrators.

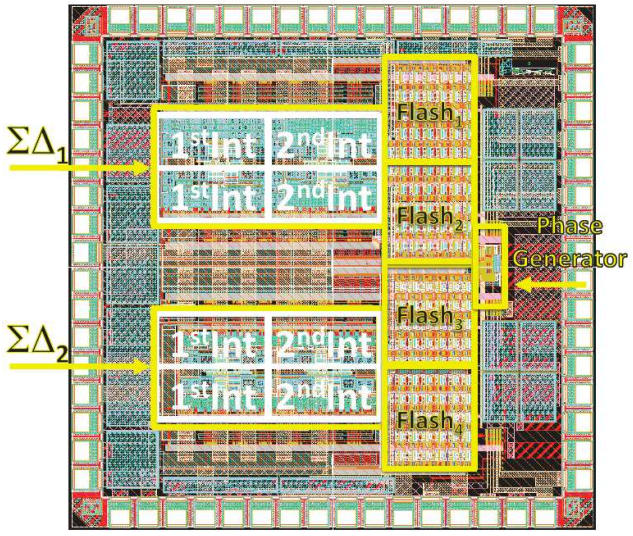

Figure 2.33: Band pass ΣΔ modulator layout in 0.18-µm CMOS technology.

5-bit flash ADC in each modulator. The chip is closed in a LLP64 package with 64 pins. The first modulator is 1.2 mm X 0.8 mm, while the second is 1 mm X 0.7 mm.

Fig. 3.23 shows the bonding diagram of the chip.

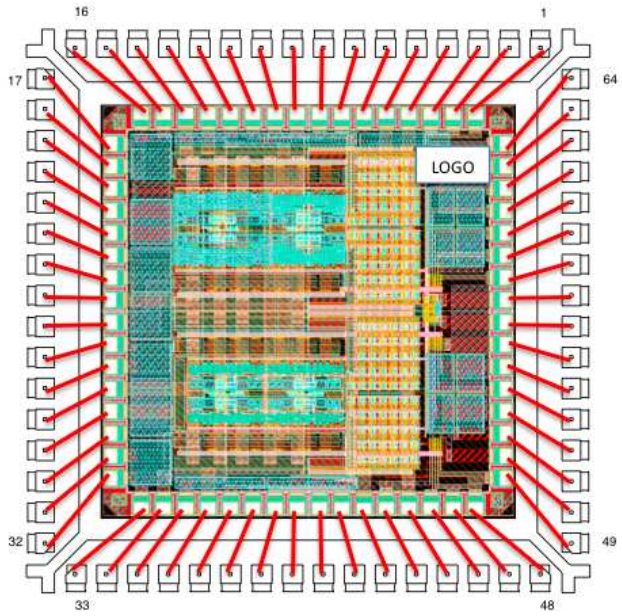

Figure 2.34: Chip bonding diagram.

2.5 Transistor-Level Simulation Results

The modulator is implemented at the transistor level using a 0.18-µm CMOS technology and a voltage supply of 1.8 V. The opamps are designed using a two stages architecture with *RC* compensation. The comparators consist in a pre-amplification stage and a latch, while the DACs are resistive strings. The flash has 5-bit resolution. The implemented opamps meet the specifications derived from the behavioral analysis. Fig. 2.35 shows the output spectrum of the MASH architecture implemented and simulated at transistor level, using an *OSR* equal to 9 and input frequency around 73.74 MHz ($F_{in} = F_s \cdot N_{per}/N$, where $F_s = 180$ MHz is the sampling frequency, $N_{per} = 839$ is the prime number of periods of the input signal considered, and $N = 2^{11}$ is the number of points used in the FFT). The obtained *SNR* is about 80 dB with a signal bandwidth of 10 MHz, leading to an effective number of bit (*ENOB*) equal to 13.09. The *SNR* degradation with respect to the value obtained in Fig. 2.20 is mainly due to switch and DAC non-idealities.

Tab. 3.7 summarizes the power consumption of the circuits used in the modulator.

The total power consumption is about 90 mW. The classical figure of merit *FoM* for ADC converter is:

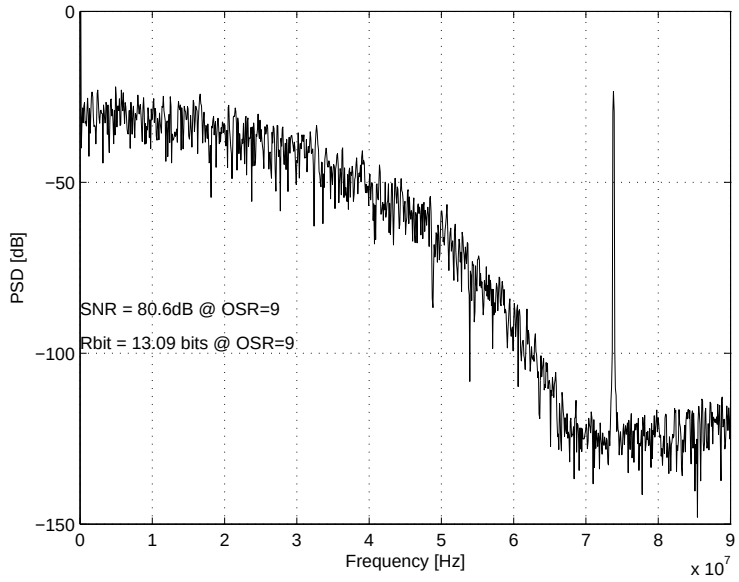

Figure 2.35: Output spectrum of the proposed ΣΔ modulator obtained with transistor-level simulation.

Table 2.3: Power consumption @ 1.8-V voltage supply.

Circuit	**Power**	**Number**	**Total**
Opamp1	10 mW	2	20 mW
Opamp2	7.3 mW	6	43.8 mW
Comparator	0.11 mW	124	13.64 mW
DAC	2 mW	4	8 mW
Logic	5 mW	1	5 mW
Total power consumption			90.44 mW

$$FoM_{BP} = \frac{P}{2 \cdot B \cdot 2^{ENOB}}, \tag{2.29}$$

where P is the power consumption, B is the signal bandwidth, and $ENOB$ the effective number of bit, giving a FoM of about 0.55 pJ/conversion-level.

A useful figure of merit for band pass ΣΔ modulators is defined as [21]

$$FoM_{BP} = \frac{P}{2^{ENOB} \cdot 2 \cdot B \cdot \left(1 + 3 \cdot \frac{IF}{f_N}\right)}, \tag{2.30}$$

where P is the power consumption, $ENOB$ the effective number of bit, B is the signal bandwidth, IF the intermediary frequency, and $f_N = F_s/2$. The above is just a reasonable definition that accounts for the extra power needed by very high signals speed. The resulting FoM_{BP} for the proposed ΣΔ modulator is 0.16 pJ/conversion-level, which is well below the state of the art.

Fig. 2.36 and Fig. 2.37 show the output spectra of the first and second modulator implemented and simulated at transistor level and simulated in the same conditions of Fig. 2.35.

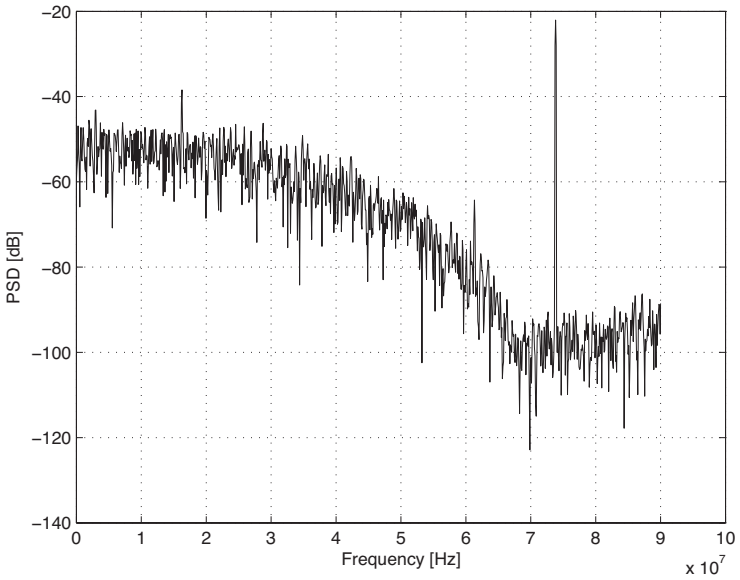

Figure 2.36: Output spectrum of the first ΣΔ modulator obtained with transistor-level simulation.

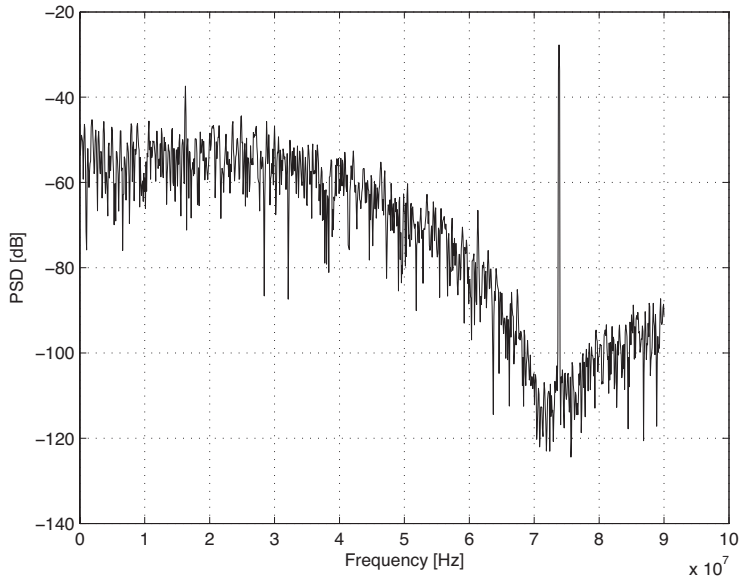

Figure 2.37: Output spectrum of the second ΣΔ modulator obtained with transistor-level simulation.

2.6 Measurement

The modulator is tested using a printed circuit board (PCB) designed using Eagle. The board has four layers and Fig. 2.38 shows the use of each layer:

- Layer Top is used for devices and connections;
- Layer 1 is the analog ground;
- Layer 2 is for connections;
- Layer Bottom is for digital ground, clock and digital outputs.

The use of multi-level board ensure high level of signal integrity. The analog ground and the digital ground are connected by a minimum via to avoid disturb from the digital part to the analog one. The input differential signal is generated by a wide-band rf transformer (Fig. 2.39): from an input sinewave, two differential sinewaves are generated. The central pin on right in Fig. 2.39 is the analog ground.

Voltage reference has three filter capacitor: one surface mounting device capacitor (100 pF) (very close to the chip), one ceramic capacitor (1 nF) and an electrolytic one (10 nF) for each reference. Current reference are generated using current regulator (LM334). The clock is direct connected with a BNC (there are inverters buffer on chip).
The mesurement results show a resolution of 11.7 bit in a bandwidth of 10 MHz. The

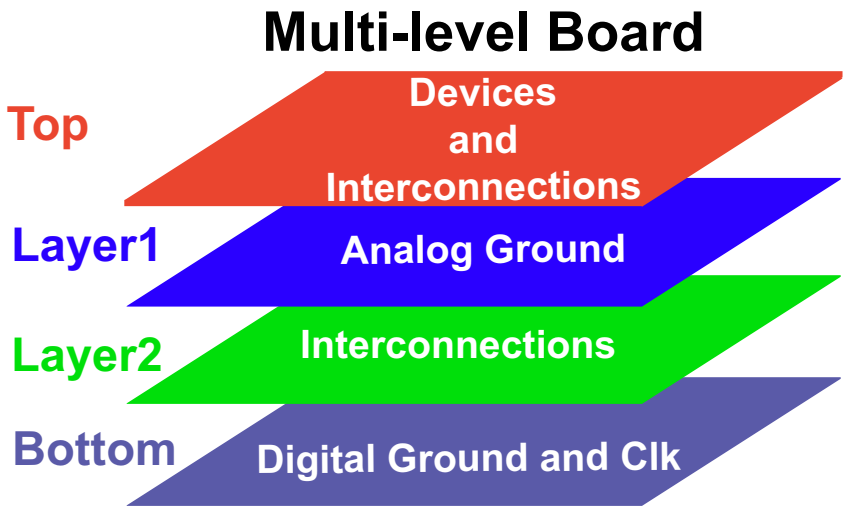

Figure 2.38: Conceptual scheme of the PCB for test chip.

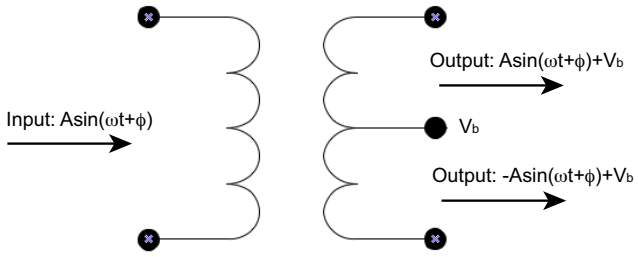

Figure 2.39: Wide-band RF transformer to generate the differential input signal.

loss of resolution, respect the simulation at transistor level, is due to the mismatch in the noise transfer function implemented by the first modulator and it cancellation in the digital domain. The measured power consumption is 95 mW, and the resulting figure of merit is equal to 0.42 pJ /conversion-level. Fig. 2.40 shows the measured spectrum: the input frequency is 70.5 MHz, the sampling frequency is equal to 180 MHz, and the FFT has 2^{17} points. The tone at $f_N/4$ is due to path mismatch.

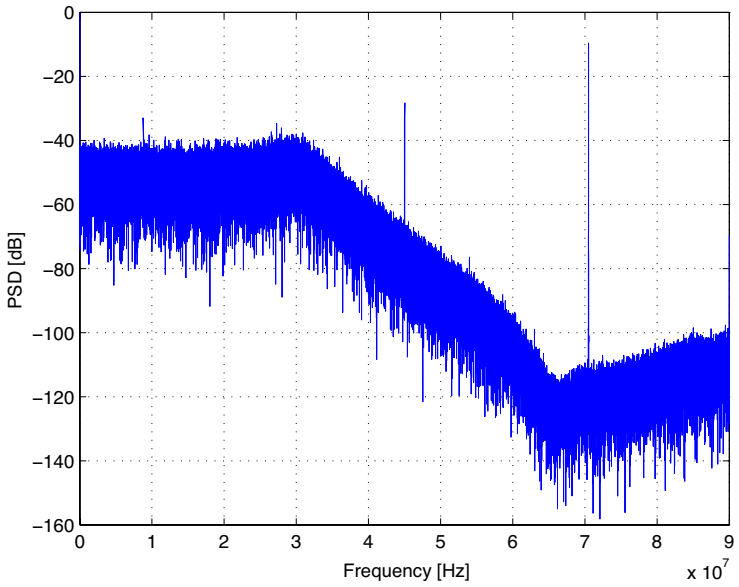

Figure 2.40: Output measured spectrum of the proposed ΣΔ modulator.

Chapter 3

Complex Band Pass ΣΔ Modulator for Body Area Network Applications

This chapter presents the design of a complex band pass ΣΔ modulator for Body Area Network Applications. The proposed architecture limits the zero positioning to situations for which the last coefficient in the NTF is 1, j, -1 or -j. The reason of the choice is that the first and the last term in the NTF can be implemented with an architecture with delay as basic blocks. The ΣΔ modulator is implemented using a 0.18-μm CMOS technology and a sampling frequency of 20 MHz. The simulations at transistor level show a resolution of about 8 bit with a bandwidth of 2.6 MHz, and a resolution of 10 bit with a bandwidth of 100 kHz. The intermediate frequency (IF) is 2.5 MHz. The power consumption is 1.95 mW with a supply voltage of 1.8 V. The project was in collaboration with Analog Devices.

3.1 Introduction, Motivations, and Results

Quadrature band pass sigma-delta (ΣΔ) modulators are important building blocks for communication systems. Superheterodyne receivers often use quadrature mixers with complex signals that must be transformed into digital form. Often zero IF solutions are unattractive because of the demanding image rejection requirements. Even low-IF for which the DC offset and the 1/f noise fall outside the signal band can be problematic for low power applications: the architecture must use wide-band A/D converters that are power hungry. The solution is to use quadrature or complex ΣΔ modulators that suppress the quantization noise only in the signal band and not the image band. The design of quadrature band pass ΣΔ normally assumes that the IF frequency is not locked to the sampling frequency. The possible degree of freedom is not a real advantage but on the contrary can be a limit because it is necessary to ensure accuracy in the coefficients of the complex filter that give rise to the notch. The state of the art of complex band pass ΣΔ is summed in Tab. 3.1.

This work proposes a novel approach by locking IF frequency to sampling frequency which may be considered as a disadvantage but actually, as shown in this text, it is vice versa. The proposed method of locking frequencies limits the possible transfer functions

Table 3.1: State of the art of complex band pass ΣΔ.

P[mW] @ V_{dd}[V]	**F_s[MHz]**	**IF**[MHz]	**bw[MHz]**	**SNR**[dB]	**Ref.**
375 @ 1.8	264	44	8.5	77	[25]
4.4 @ 1.8	64	0.5	1	75.5	[27]
10 @ 2.1	13	10	0.2	81	[28]
56 @ 1.2	340	10.5	20	71	[29]
43 @ 1.8	276	11.5	23	68.8	[30]

to a sub-set of possibilities. However, the resulting architectures that use unity delays and adders obtain a limited sensitivity to errors. The NTF zero placement is straightforward with the possibility to avoid using zeros in the conjugate position.
In this chapter the design of a complex band pass ΣΔ modulator for body area network applications is presented. The considered IF is 2.5 MHz, the signal-to-noise ratio (*SNR*) target is about 50 dB with a signal bandwidth of 2.6 MHz, and about 62 dB with a signal bandwidth of 100 kHz. The ΣΔ modulator works with a sampling frequency of 20 MHz, and the power consumption is 1.95 mW with a power supply of 1.8 V. The proposed ΣΔ modulator is implemented at the transistor level using a 0.18 μm CMOS technology and a voltage supply of 1.8 V.

3.2 Proposed Complex Band Pass ΣΔ Modulator

Low-IF has been used in many receiver architectures in which different A/D conversion approaches are possible. One of these uses two separate ADCs for I and Q channels [22] or shares one ADC for both channels [23]. These ADC's are often pipelined-type but also they may be ΣΔ ADC's. However, both the approaches consume significant power and area. Reducing the number of *NTF* zeros with a complex or quadrature type A/D converter [24]-[28], diminishes the power while keeping the benefit of the band pass noise shaping. The mismatch in quadrature A/D converters can be source of tones in the image position, problem overcame by placing a zero on the image [25] or by taking advantage of system specifications such as GSM [24]. The *IF* frequency of quadrature A/D converters is independent by the clock frequency, but in case of a mismatch, the independency becomes source of error requiring the possible use of calibration or trimming methods. Although it is possible to select *IF* frequency and clock frequency such that the performance degradation in case of mismatch error is limited.
This work foresees a generalization with multiple feedbacks and delay elements. Before studying possible block diagrams let us consider the noise transfer function of a system with a set of zeros on the unity circle at the positions $e^{j\phi_i}$, i = 1, 2, n. The *NTF* is

$$NTF = \prod_{1}^{n}\left[1 - \frac{e^{j\phi_i}}{z}\right] = 1 + \frac{a_1}{z} + ... + \frac{e^{j\sum_i^n \phi_i}}{z^n}, \tag{3.1}$$

Therefore, depending on the zero position the last term has module one and phase that

is the addition of the phase of all zeros.
The developed method limits the zero positioning to situations for which $\sum_i^n j\phi_i = 0, \pi, \pi/2, 3\pi/2$ or correspondingly the last coefficient of (3.1) is 1, j, -1 or -j. The reason of the choice is is totally from implementation perspective. The block diagrams of Fig. 3.1 (a) and (b) determine the noise transfer functions

$$NTF = (1 \pm z^{-n}) \quad or \quad NTF = (1 \pm jz^{-n}). \tag{3.2}$$

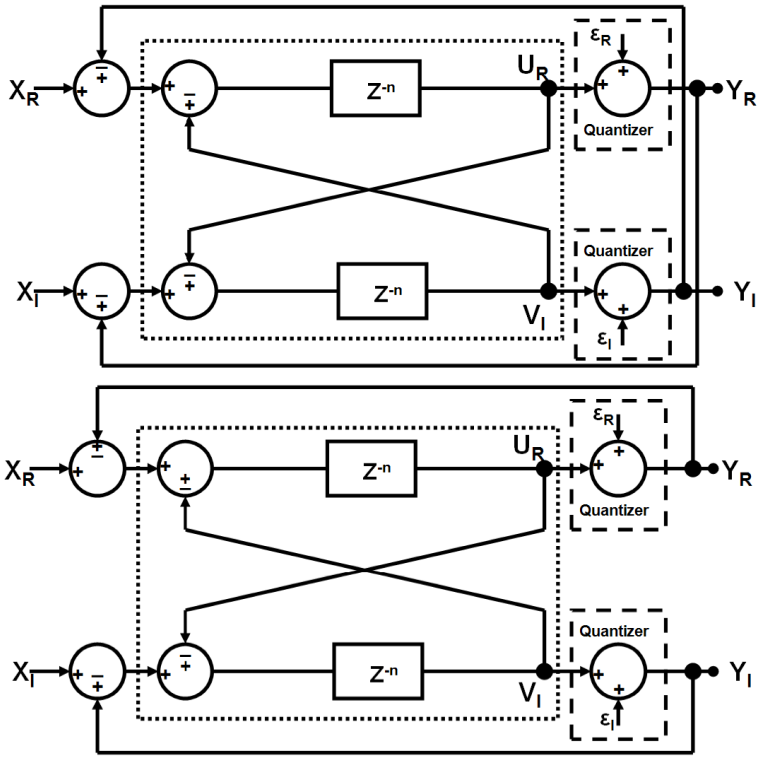

Figure 3.1: Generalized architecture for *NTF* with top ±j term, bottom ±1 term.

Notice that the block diagram inside the dotted lines of Fig. 3.1 is a generalization of the one used in a conventional quadrature modulator, shown in Fig. 3.2. It obtains the complex transfer function $z^{-1}/(1 \pm jz^{-1})$. The scheme of Fig. 3.1 realizes only two terms of the expected NTF; therefore, it is necessary to realize the inner terms of the equation 3.1. Suppose to design a modulator whose *NTF* has two zeros, and also assume that $\phi_1 + \phi_2 = 3\pi/2$.
Therefore it results:

$$NTF = 1 - \left(e^{j\phi_1} + e^{j\phi_2}\right) z^{-1} - jz^{-2} = 1 - \alpha z^{-1} - jz^{-2}, \tag{3.3}$$

where α is a complex number whose module is less than $\sqrt{2}$.

The missing term is $-\alpha z^{-1}$. If the phase of the zeros are symmetrical with respect to $3\pi/4$ ($\phi_{1,2} = 3\pi/4 \pm \delta$), then

$$\alpha = -(1 + j)\, k, \qquad \left(k < \sqrt{2}\right), \tag{3.4}$$

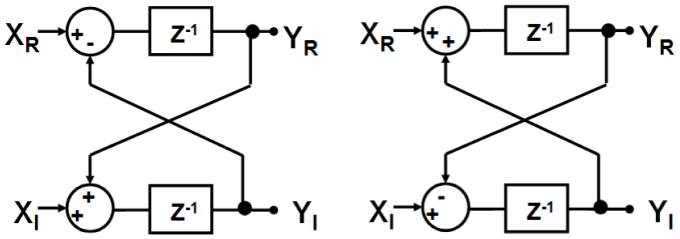

Figure 3.2: Basic building blocks for complex integrators.

Notice that if k=1, then $z_1 = 1$ ans $z_2 = -j$. Morover, for k= $\sqrt{2}$ the zeros are coincident. Indeed, the parameter k produces the root locus of Fig. 3.3; for $k < 1$ the zeros are in the fourth quadrant.

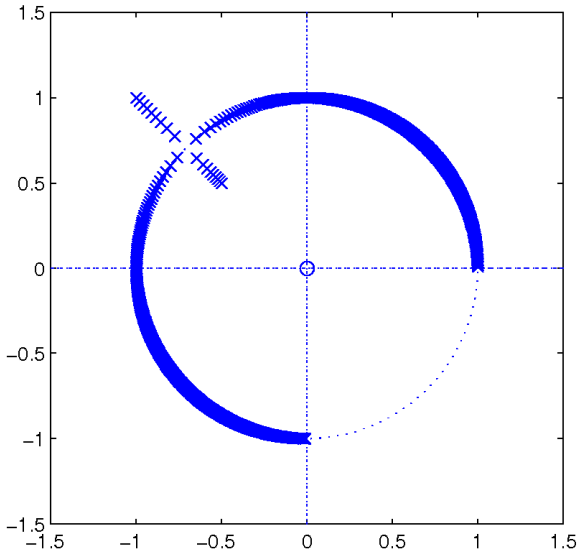

Figure 3.3: Root locus of two complex zeros.

The implementation of the missing term requires the injection of two quantization noise components one from the real path, the other from the imaginary one. This is done with the diagram of Fig. 3.4: the two delays are distinguished into single delay, while the addition

of the two quantization errors amplified by k is injected into the intermediate point with positive and negative sign. The accuracy of the result depends on the network used for the implementation of the missing term, however, an error on k causes a shift of the zeros proportional to the sensitivity of $\phi_{1,2}$ to k. If the zeros are apart enough the sensitivity is not very high and the effect of mismatches cause a negligible variation of the SNR. The same is for error affecting the addition of quantization errors.

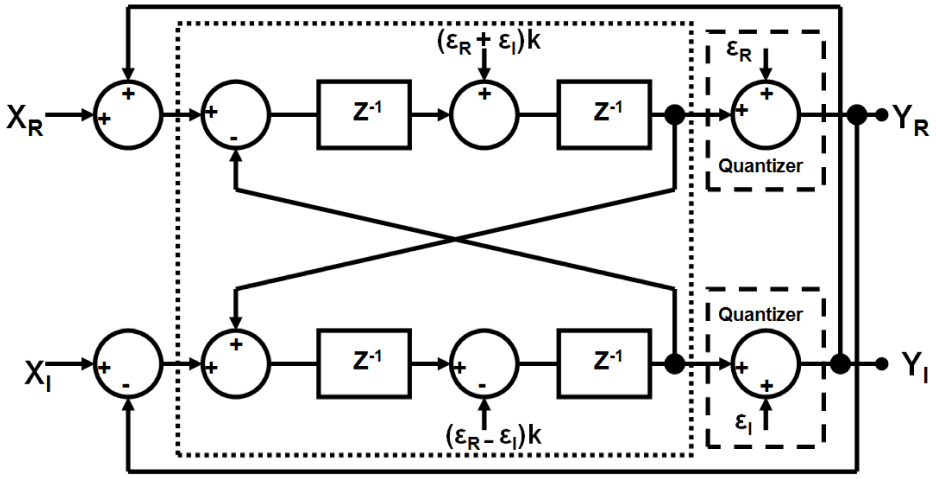

Figure 3.4: Block diagram for two complex zeros.

The above point is verified with an analytical study. By inspection of Fig. 3.4 and accounting for possible errors it results:

$$\begin{aligned} Y_R &= (X_R + Y_I - P_I) + k\epsilon_1 z^{-1} + \epsilon_R \\ Y_I &= (X_I + Y_R - P_R) + k\epsilon_2 z^{-1} + \epsilon_I \\ P_R &= Y_R - \epsilon_R; \qquad P_I = Y_I + \epsilon_I \\ \epsilon_{1,2} &= \epsilon\,(1 + \delta_{1,2}) + \epsilon_I \end{aligned} \tag{3.5}$$

that gives the following extra terms

$$\begin{aligned} &k\delta_R\,(\epsilon_R + \epsilon_I) + k\delta_1\,(\epsilon_R + \epsilon_I) \\ &k\delta_I\,(\epsilon_R + \epsilon_I) + k\delta_2\,(\epsilon_R - \epsilon_I) \end{aligned} \tag{3.6}$$

The left part of the extra terms moves the zeros from their original position. However, since the expected mismatch is in the order of 0.1%-0.4% then the deviation from the nominal placement is limited. The remaining part causes a leakage that gives rise to a slight increase of the noise in the signal band. Behavioral simulations show that the degradation of performances is negligible with expected values of mismatches.
The above described method for obtaining two complex zeros in the *NTF* can be extended to higher order. Assume that it is required to generate an *NTF* with three zeros on the unity

circle with phases ϕ, $(\phi + \delta)$ and $(\phi - \delta)$, moreover $3\phi = \pi/2, \pi, 3\pi/2$ or 2π, ... Then, it is necessary to use a basic scheme like the one of Fig. 3.1 with z^{-3} plus extra injections to generate the z^{-1} and z^{-2} terms. The results is the diagram of Fig. 3.5.

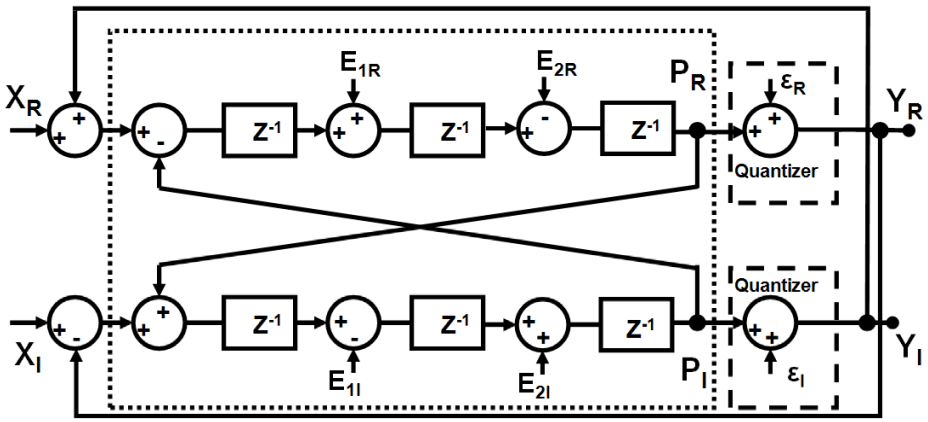

Figure 3.5: Third order architecture.

The additional injected terms are:

$$\begin{aligned} E_{i,R} &= \alpha_{i,R}\epsilon_R + \beta_{i,R}\epsilon_I \\ E_{i,I} &= \alpha_{i,I}\epsilon_R + \beta_{i,I}\epsilon_I \end{aligned} \tag{3.7}$$

where the coefficients α and β are possibly complex and are determined by the required transfer function. Again, it is possible to make a study of the sensitivity to the mismatch in a way similar to the one performed for the two zeros case.
Summing up the above study it's possible to summarize the proposed design method for a band pass quadrature modulator with the following steps.

1. Calculate the required SNR and bandwidth for achieving the desired specifications.
2. Calculate the order of the system regarding the SNR value calculated.
3. Decide where to place zeros of the system. If for image rejection another zero is required, then increase the order of the system.
4. After the calculation of number of zeros and their placement, select which *NTF* (with 1, j, -1 or -j) is suitable for covering these zeros.
5. Set the coefficients in the intermediate injection points for achieving the desired zero locations.
6. Perform behavioral simulation for verification.

3.2.1 Design Examples

The proposed method has been verified in the design of modulators with two, three or four zeros without complex conjugate counterparts. Fig. 3.6 shows the location of the complex zeros that have phase $3\pi/4 \pm \pi/20$. This design requires using k=1.4 in the extra injection point of Fig. 3.4. The obtained noise shaping with 4-bit quantizer is shown in Fig. 3.7. The *SNR* with $OSR = 8$ is as good as 74.5 dB.

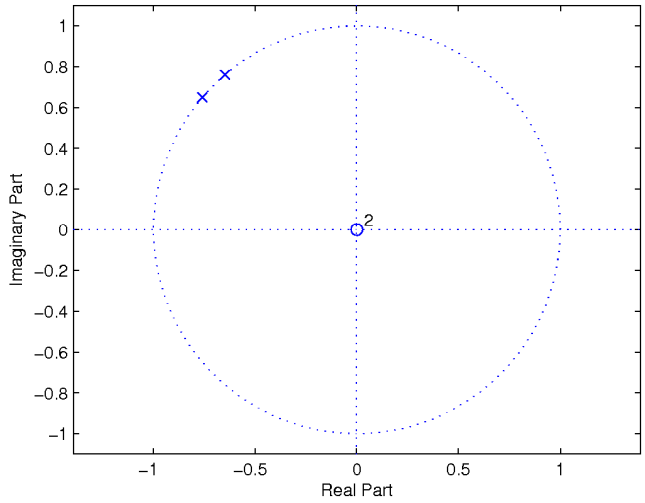

Figure 3.6: Zeros and poles locations of the second order complex modulator considered in the design example.

The scheme can be realized with a sampled-data or continuous time approach, [29] - [32]. The design example with three zeros uses $\phi_1 + \phi_2 + \phi_3 = \pi/2 + 4\pi$ that gives jz^{-3} as the higher order term of the *NTF*. The zeros with $\phi_1 = 17\pi/2$, $\phi_2 = 18\pi/2$ and $\phi_3 = 19\pi/2$ are shown in Fig. 3.8. Fig. 3.9 shows the noise shaping along with the signal tone. The chosen value of coefficients grants a wide signal band ($f_N/5$) with a significant *SNR*.

The last design example is with four zeros as shown in the noise shaping diagram of Fig. 3.10.

3.2.2 Behavioral Simulation Results

In this project it is designed a second complex band pass ΣΔ modulator using the architecture in Fig. 3.4 with k=11/8. The target is to obtain a *SNR* of about 48 dB with a signal bandwidth of 2.6 MHz, and 66 dB with a signal bandwidth of 100 kHz. The signal frequency is 2.5 MHz. Fig. 3.11 shows the zeros positions on the unity circle using k=11/8. The poles are all in the origin.

Fig. 3.12 depicts the spectrum of this architecture in ideal conditions using a 4-bit quantizer and a sampling frequency of 20 MHz: the two zeros are clearly visible around the

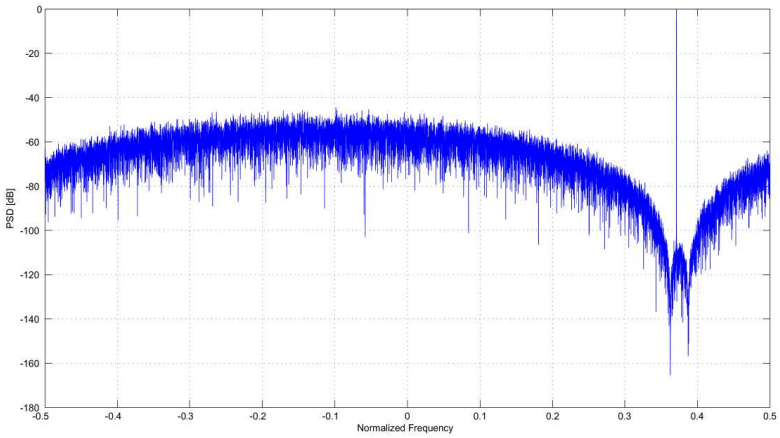

Figure 3.7: Spectrum of a second order complex modulator.

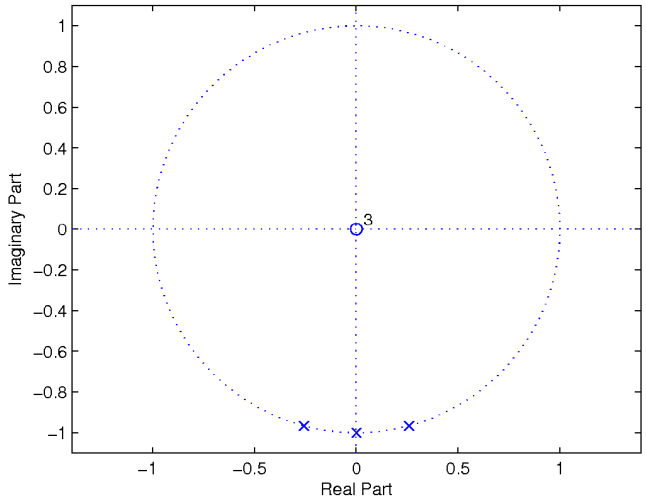

Figure 3.8: Zeros and poles locations of the third order complex modulator considered in the design example.

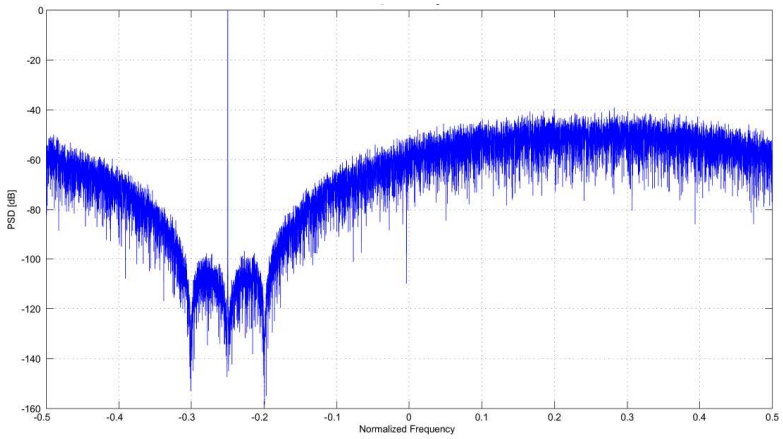

Figure 3.9: Spectrum of a third order complex modulator.

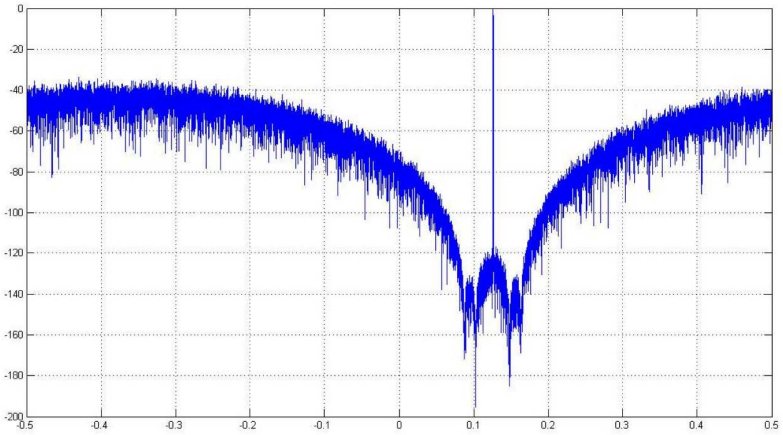

Figure 3.10: Spectrum of a four order complex modulator.

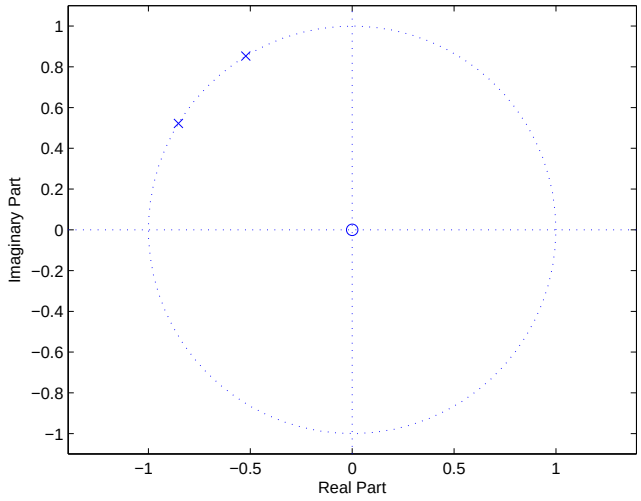

Figure 3.11: Zeros positions of the designed complex modulator.

IF. The simulation is performed in Matlab-Simulink^{TM}environment, with an IF at 2.5 MHz. The resolution is 11.1 bit on a bandwidth of 100 kHz, and 9.2 bit considering a bandwidth of 2.6 MHz.

The modulator is studied introducing non-ideal parameter in the integrators and errors in the coefficient k.

Fig. 3.13 shows the spectrum with real integrators: the resolution is 8.8 bit with a 2.6 MHz bandwidth and 10.5 bit with 100 kHz bandwidth. In this simulation are considered finite gain, op-amp finite bandwidth and slew-rate. Tab. 3.2 shows the parameters used into the analysis.

Table 3.2: Finite integrators parameters.

gain[dB]	**F**$_s$[MHz]	**bandwidth**[MHz]	**slew-rate**[μV/s]	**C input for kT/C**[fF]
60	20	100	30	800

The mismatches on coefficient k are studied by a statistical analysis, with 100 samples and introducing a random normally distributed coefficient errors with zero mean and standard deviation $\sigma = 5 \cdot 10^{-3}$. The results are illustrated in Fig. 3.14 and Fig. 3.15: the first one shows the SNR with a bandwidth of 100 kHz, the second the SNR with a bandwidth of 2.6 MHz. In both cases the desired SNR performances are in line with the target specifications.

The simulated image rejection is 60 dB, introducing a mismatch of 0.3% in the feedback DAC and in the different coefficients in the modulator.

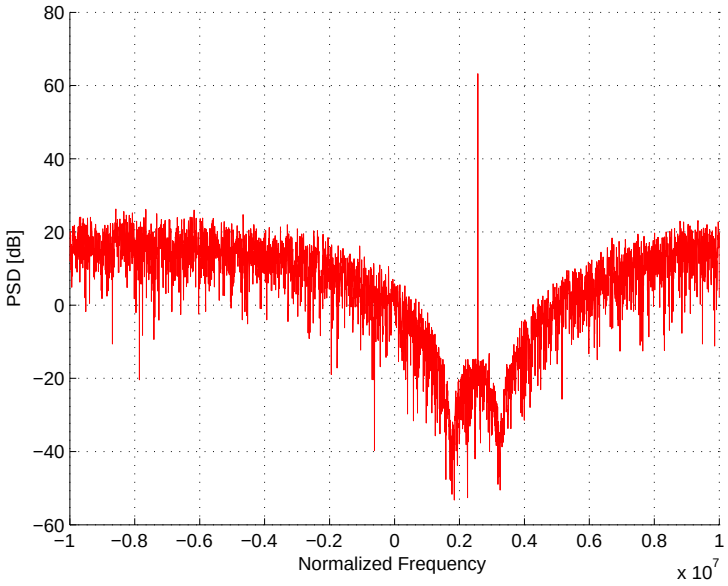

Figure 3.12: Spectrum of the designed second order complex modulator in ideal conditions.

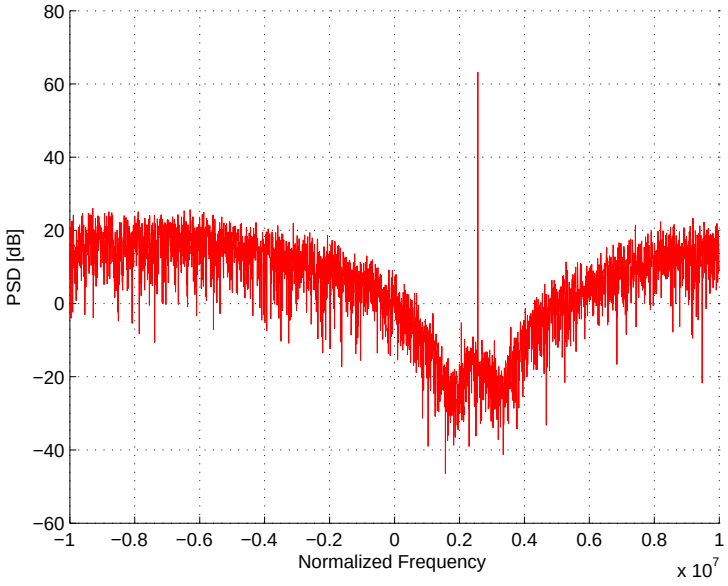

Figure 3.13: Spectrum of the designed second order complex modulator with real integrators.

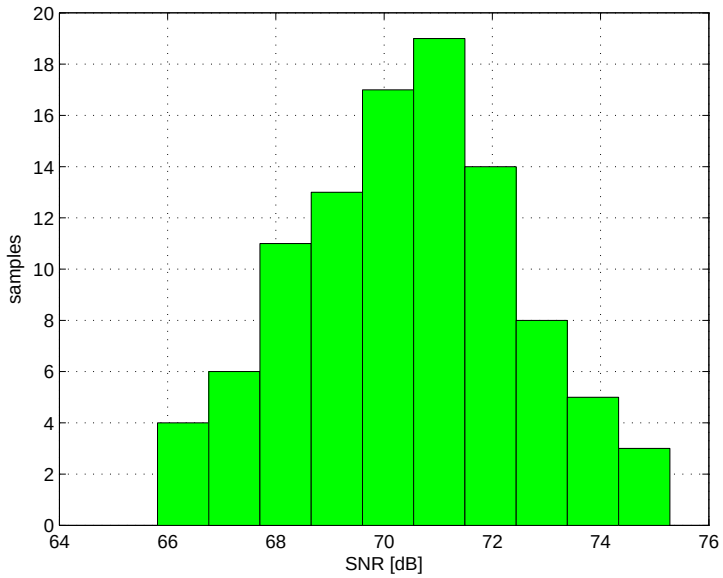

Figure 3.14: Simulated *SNR*, with a bandwidth of 100 kHz, and 100 runs considering errors in the k coefficient value ($\sigma = 5 \cdot 10^{-3}$).

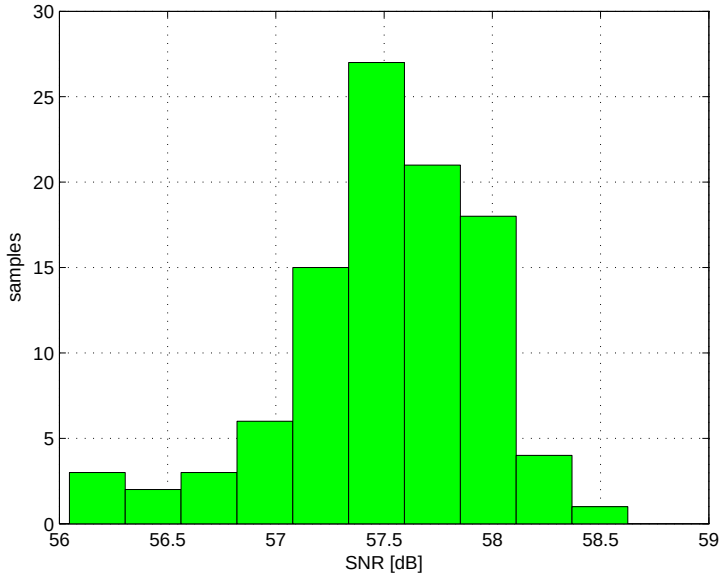

Figure 3.15: Simulated *SNR*, with a bandwidth of 2.6 MHz, and 100 runs considering errors in the k coefficient value ($\sigma = 5 \cdot 10^{-3}$).

3.3 Circuit Design

This section explains the circuit design at the transistor level with a 0.18 μm CMOS technology of the blocks used in the modulator. There are the description of the operational amplifier, the comparator, the 4-bit flash and the integrator. Each block is illustrated with simulations at transistor level, Monte Carlo analysis, and corner simulations.

3.3.1 Operational Amplifier

The operational amplifier is a fully differential two stage op-amp with RC compensation and discrete time common mode feedback. The op-amp performances are shown in Tab. 3.3.

Table 3.3: Op-amp performances.

Gain	Slew-rate	Bandwidth	Phase margin	Power consumption
69.5 dB	30 μV/s	100 MHz	60 degree	350 μW & 1.8 V

Fig. 3.16 shows the gain and the phase margin in standard conditions.

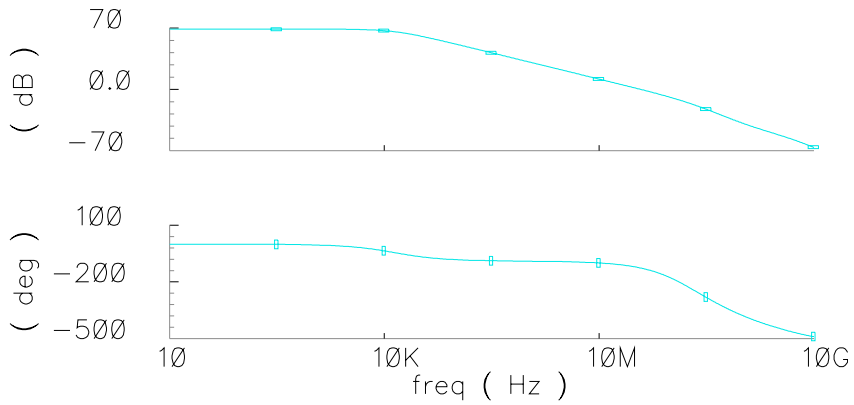

Figure 3.16: Op-Amp gain and phase margin.

Fig. 3.17 depicts the time step response of the op-amp in standard conditions.

Corner simulations results with temperature of 27°, -40°, and 85°are shown in Tab. 3.4, Tab. 3.5, Tab. 3.6, respectively. In the tables the first attribute (typical, fast or slow) is a parameter refer to the NMOS transistors while the second one is for the PMOS transistors.

Monte Carlo analysis with 100 runs shows that the gain is higher than 66.7 dB, with a loss of maximum 2.8 dB gain respect the standard conditions.

The layout, including the common mode feedback network, and the RC compensation, is 350 μm X 65 μm.

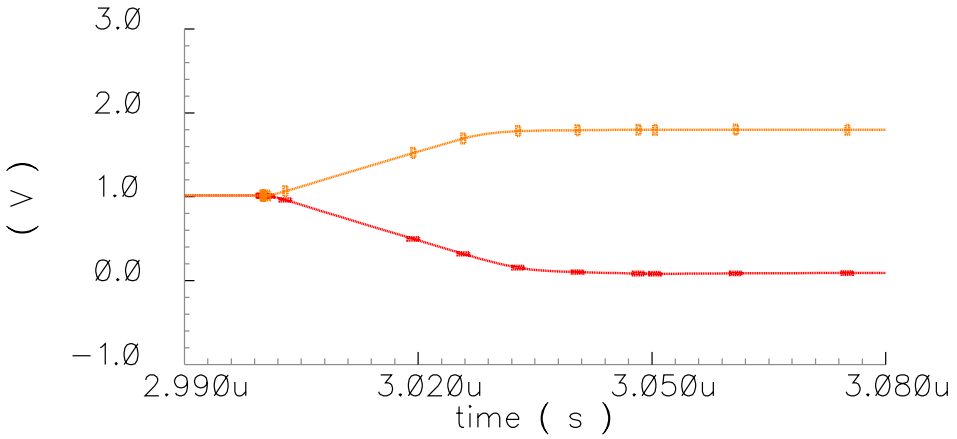

Figure 3.17: Step response of the op-amp.

Table 3.4: Gain Op-Amp corner simulations with 27°.

typical-typical	slow-slow	fast-fast	slow-fast	fast-slow
69.5 dB	69 dB	61 dB	64 dB	68 dB

Table 3.5: Gain Op-Amp corner simulations with -40°.

typical-typical	slow-slow	fast-fast	slow-fast	fast-slow
69 dB	68 dB	64 dB	64 dB	68 dB

Table 3.6: Gain Op-Amp corner simulations with 85°.

typical-typical	slow-slow	fast-fast	slow-fast	fast-slow
67 dB	69 dB	58 dB	63 dB	62 dB

3.3.2 Comparator

Fig. 3.18 shows the scheme of the used comparator: it is composed by a pre-amplifier stage and a latch. The pre-amplifier is a fully differential structure made by two cross-coupled differential pairs. The latch uses a double positive feedback. The reset of NMOS ensures the reduction of the dynamic current consumption. The common mode feedback in the amplification stage is not shown in the picture and is made by two NMOS that realize a resistive degeneration. The power consumption is 25μW with a power supply of 1.8 V.

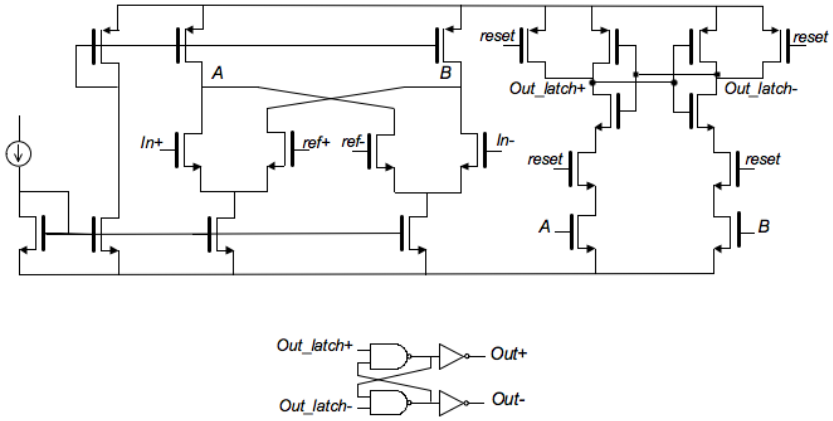

Figure 3.18: Comparator scheme.

Monte Carlo analysis with 100 runs shows that with a half LSB sensitivity, the outputs are correct in 97% of total cases. The layout is 35 μm X 45 μm.

3.3.3 4-bit Flash ADC

The 4-bit flash is made using the comparator shown in Fig. 3.18. Fig. 3.19 shows the output spectrum of the implemented 4-bit flash, obtained by a post layout simulation: the resolution is 3.88 bit and the power consumption is 0.375 mW with a power supply of 1.8 V. The simulation is done with a sampling frequency of 25 MHz, input frequency of about 5 MHz, and FFT with 2048 points.

Fig. 3.20 shows the results of a Monte Carlo analysis with five runs on the designed 4-bit flash ADC. In all cases the resolution is higher than 3.76 bit.

The layout is 150 μm X 190 μm.

3.3.4 SC integrators

The two integrators are implemented using a switched capacitor (SC) differential circuits approach. Considering the architecture of the designed modulator, Fig. 3.21, each integrator has these inputs,

- the two quadrature input signals (X_R or X_I);

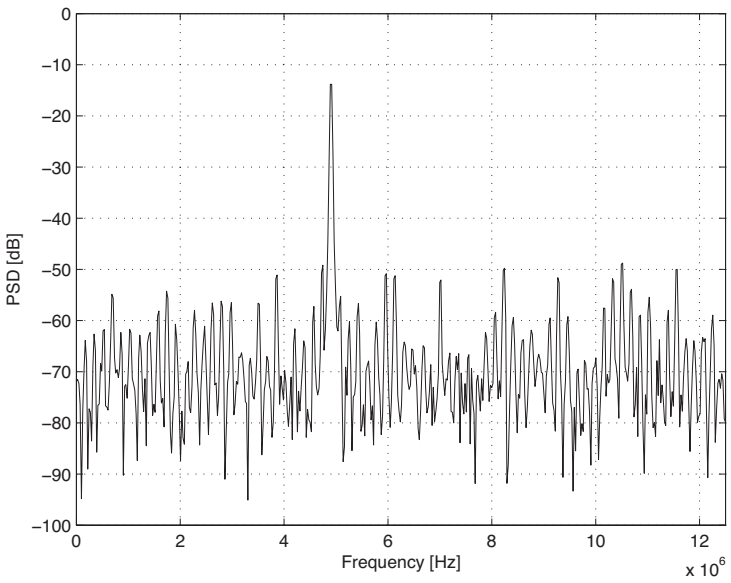

Figure 3.19: Simulated post layout 4-bit flash ADC output spectrum.

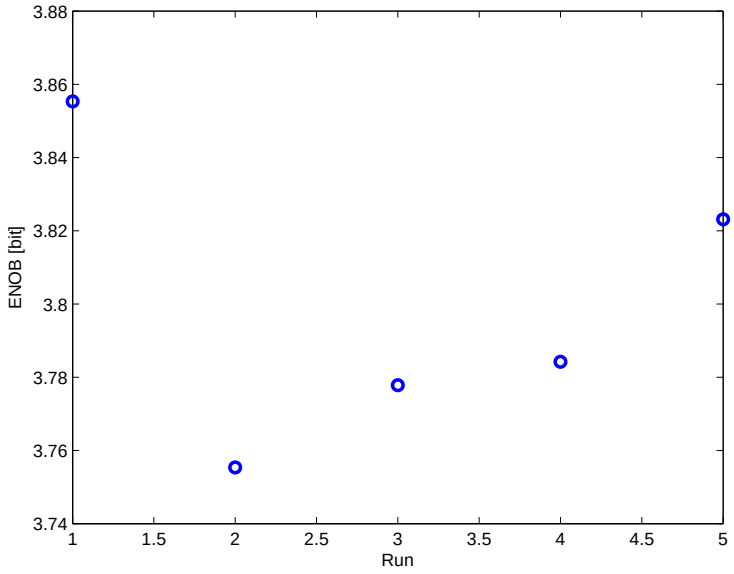

Figure 3.20: Statistical analysis of the 4-bit flash.

- the feedbacks coming from the DAC (Y_R or Y_I);
- the feedbacks coming from the output of the other integrator;
- the quantization errors ϵ_I and ϵ_R amplified by k=11/8.

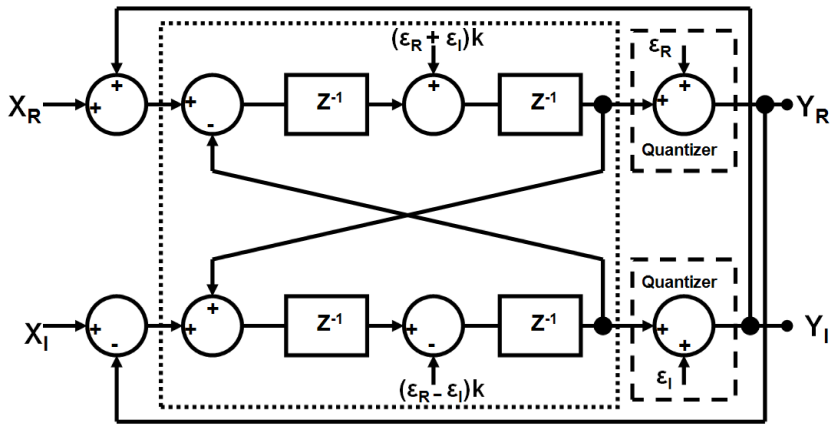

Figure 3.21: Diagram block of the designed modulator.

The different coefficients in the modulator are integer multiple of the fraction 1/8 (8/8 for inputs and feedbacks, and 11/8 for quantization error) so the integrator capacitors are made by eight unity capacitors. Integrator capacitors has unity value of 100 fF to respect the kT/C noise limit (the total input capacitance is 800 fF). The DACs used in the modulator are resistive string with poly resistance. Mismatches study is reported in 4.4. The integrator layout is 410 μm X 300 μm, including dummy capacitors.

3.3.5 Layout

Chip layout is realized with a 0.18 μm CMOS technology, with five metals, two poly, and MIM capacitor. The layout is illustrated in Fig. 3.22. The chip area is 1.2 mm X 1.2 mm, including the pad-ring. The chip has 28 pads and it will be closed into a ceramic package.

Fig. 3.23 shows the chip pad-ring.

Fig. 3.24 depicts the output spectrum obtained by a post layout simulation: the resolution is 7 bit with a bandwidth of 2.6 MHz, and 9.6 bit with a bandwidth of 100 kHz. The simulation is performed with an IF of 2.5 MHz, a sampling frequency of 20 MHz, and an FFT with 2048 points. The simulated power consumption is 1.95 mW with a power supply of 1.8 V.

The obtained performances are in line with the design specifications.

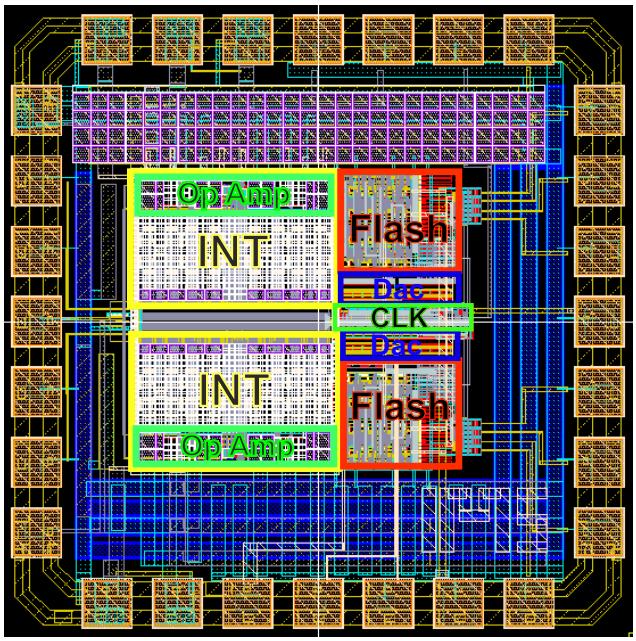

Figure 3.22: Complex band pass ΣΔ modulator layout in 0.18-µm CMOS technology.

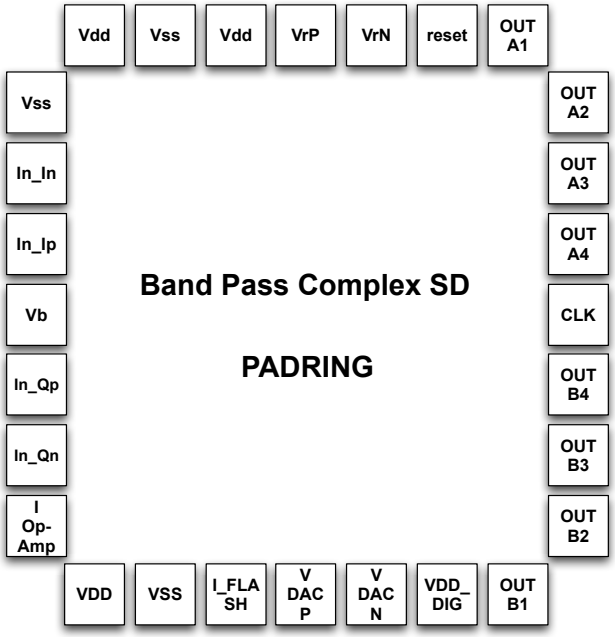

Figure 3.23: Pad-ring used in the designed chip.

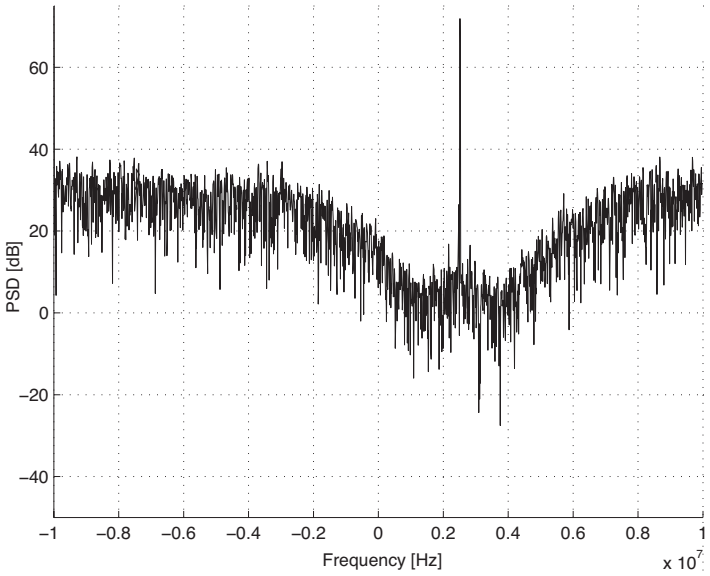

Figure 3.24: Simulated post layout output spectrum.

3.4 Transistor-level Simulations Results

The modulator is implemented at the transistor level using a 0.18-µm CMOS technology and a voltage supply of 1.8 V. The opamps are designed using a two stages architecture with *RC* compensation. The comparators consist of a pre-amplification stage and a latch, while the DACs are resistive strings. The flash has 4 bit resolution. The implemented opamps meet the specifications derived from the behavioral analysis. Fig. 3.25 shows the output spectrum of the complex modulator simulated at transistor level, and obtained, introducing mismatches in DAC resistors, using an input frequency of 2.5 MHz, a sampling frequency of 20 MHz, and a FFT with 2048 points. The introduced mismatch has a standard deviation from the nominal resistance of, respectively, 0.215% and 0.21%. The obtained *SNR* is about 55 dB with a signal bandwidth of 100 kHz, leading to an effective number of bit (*ENOB*) equal to 9 bit, and resolution of 7.5 bit with a bandwidth of 2.6 MHz. Its important to underline that, although the mismatches used in the simulation are high, the performances are in line with the design specifications.

Tab. 3.7 summarizes the power consumption of the circuits used in the modulator. The total power consumption is 1.95 mW.

Fig. 3.26 and Fig. 3.27 show the percentage variation from the nominal value of the used resistors during the simulation.

Considering the results of the post layout simulation, Fig. 3.24, the simulated *FoM* for the proposed ΣΔ modulator is 1.7 pJ/conversion-level, which is well below the state of the art of complex band pass ΣΔ modulator.

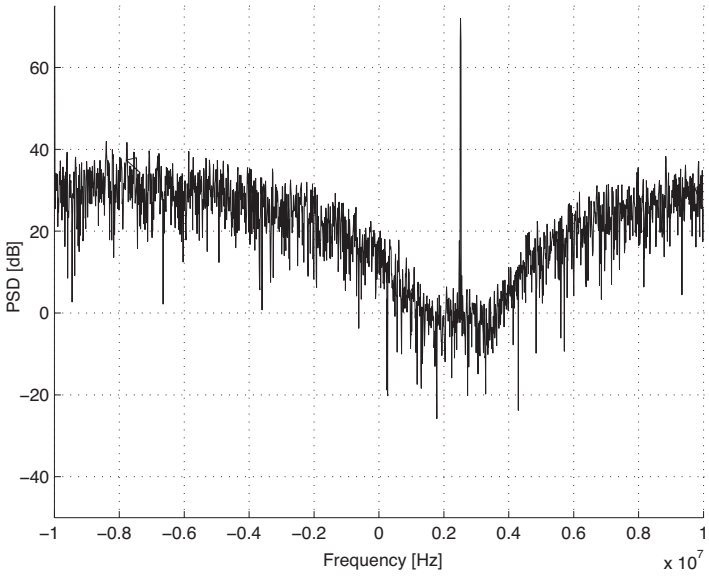

Figure 3.25: Output spectrum of the proposed ΣΔ modulator obtained with transistor-level simulation and mismatch in DAC resistors.

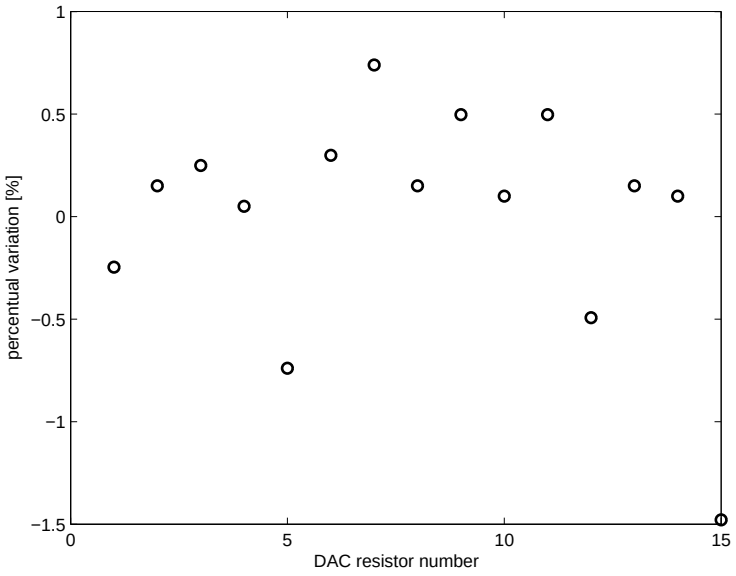

Figure 3.26: Percentage variations of the first DAC resistors string.

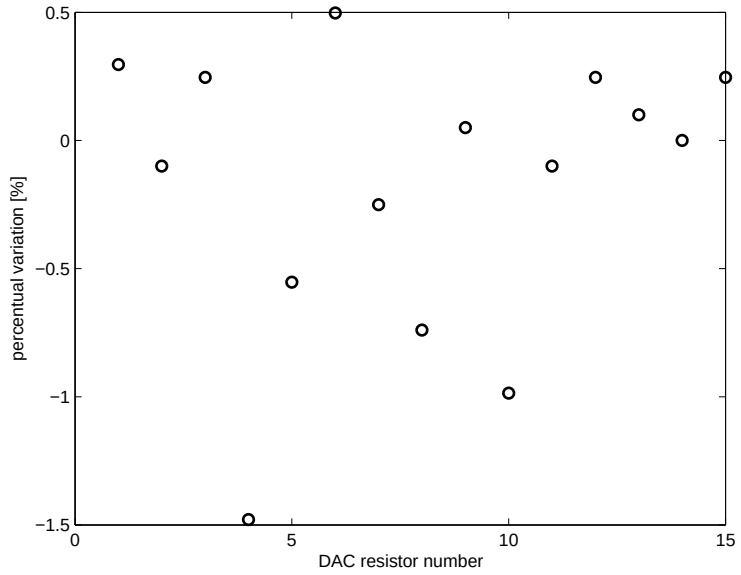

Figure 3.27: Percentage variations of the second DAC resistors string.

Table 3.7: Power consumption @ 1.8-V voltage supply.

Circuit	**Power**	**Number**	**Total**
Opamp	0.35 mW	2	0.7 mW
Comparator	25 μW	30	0.75 mW
DAC	0.2 mW	2	0.4 mW
Logic	0.1mW		0.1 mW
Total power consumption			1.95 mW

Chapter 4

Proposed Non-Conventional ΣΔ Architectures

The research in ADC ΣΔ modulators for telecommunication applications asking for new methods to achieve medium-high resolutions (10 - 14 bit) with medium-high bandwidth (1 - 10 MHz). This chapter presents the research activity results concerning the study of proposed non-conventional ΣΔ architectures. There are two main thematics developed: digitally assisted ΣΔ modulator, and the DAC linearization for multi-bit ΣΔ modulator without the use of dynamic elements matching. Each section illustrates the motivations, the proposed solutions and the results. All techniques are simulated at the behavioral level in Matlab-Simulink^{TM} environment, introducing real parameters in the structures, and coefficient errors to investigate the mismatch sensitivity and demonstrate the effectiveness of the approach.

4.1 Digitally Assisted ΣΔ Modulator

This section presents a design method to realize fully digital feedforward in ΣΔ modulators. The technique, here applied to a second order low-pass modulator, achieves a strong reduction in the operational amplifiers output swing, thus allowing the use of power efficient single stage architectures. The method ensures amplifiers reduced slew-rate requirements and allows operation at lower power supply voltages, preserving the modulator STF and NTF. The proposed technique is compared with the conventional both analog and digital feedforward solutions. The simulations at the behavioral level and the sensitivity analysis demonstrate the effectiveness of the approach.

4.1.1 Motivations, Proposed Method, and Results

The portable communications market requires high speed and high resolution analog-to-digital converters (ADCs) with severe requirements on power consumption, in order to maintain a longer battery life. To have high system integration and low fabrication costs, it is desirable to use nanometer CMOS technology. However, with these technologies,

the design of the analog circuits is complicated by the used low supply voltage. The ΣΔ technique, initially used to achieve high-resolution in the audio band, is now used for the communication applications that require medium-high resolution and wide signal bandwidth. The ΣΔ technique for broadband applications in the MHz or ten of MHz range cannot allow large oversampling ratio (OSR) and requires special care to keep the power consumption low. The goal is achieved with multi-bit architectures and low voltage swing of the used op-amps.

Various methods for limiting the op-amp voltage swing have been proposed. This section describes a design approach suitable for high-speed high-resolution ΣΔ ADCs with fully digital feedforwards. The solution ensures a low swing in the operational transconductance amplifier (OTA), thus allowing the use of single stage op-amps, such as telescopic cascode. Moreover, the digital feedforward does not requires additional branches at the input of the OTAs that worsen the feedback factor. In addition, swing reduction favors better linearity, lower power consumption, reduces the slew-rate requirements and allows operation at lower power supply voltages. Furthermore, the input signal can be at full scale, increasing the achievable signal to noise ratio (*SNR*).

4.1.2 Conventional Solutions

Previously published solutions use multi-bit architectures and analog or digital feedforward to reduce op-amps output range, [8]-[11]. In order to describe the method, consider the conventional second order modulator shown in Fig. 4.1. The voltage of P_1, the first

$$P_1 = X\frac{z^{-1}(1+z^{-1})}{2} - \epsilon_Q\frac{z^{-1}(1-z^{-1})}{2} \tag{4.1}$$

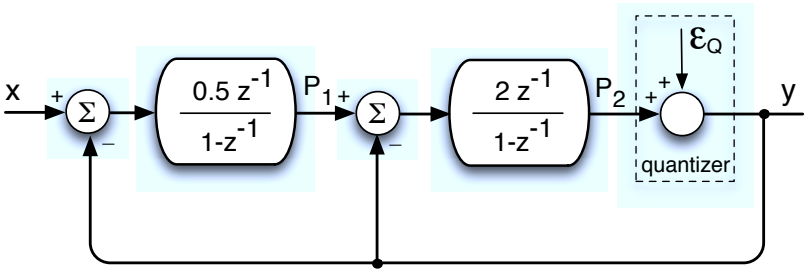

Figure 4.1: Block diagram of a conventional second order ΣΔ modulator.

integrator output, is large because even with a multi-bit quantizer, that gives a low quantization error, the amplitude of P_1 is dominated by the first term of (4.1). The swing of the first integrator diminishes with analog feedforward, [8]-[10], as shown in Fig. 4.2.

By inspection, P_1 becomes

$$P_1 = X\frac{z^{-1}(1-z^{-1})}{2} + \epsilon_Q\frac{z^{-1}(1-z^{-1})}{2} \tag{4.2}$$

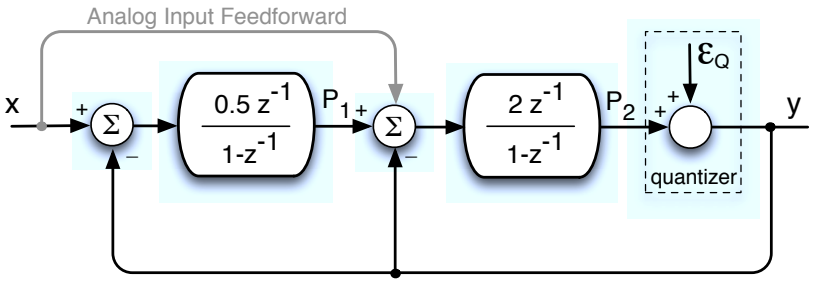

Figure 4.2: Second order ΣΔ modulator using analog input feedforward.

showing that the contribution of the signal is strongly reduced being passed through a high-pass filter $(1-z^{-1})$. However, the feedforward path referred to input is $2X(1-z^{-1})/z^{-1}$ that, multiplied by the signal transfer function ($STF = z^{-2}$), denotes a spur term in the *STF*. Therefore

$$STF = z^{-2} + 2z^{-1}(1 - z^{-1}) \tag{4.3}$$

Analog feedforwarding can be also applied to the second integrator, but the method would require an analog addition before the quantizer. This is unpractical because, even with a relatively low number of comparators, the adder requires an extra op-amp or OTA that consumes additional power, worsening the power effectiveness.

Instead of analog, it is possible to realize the feedforward paths in the digital domain, [11]. The method, shown in Fig. 4.3, uses a quantizer that digitizes the input. The quantized result, equal to input plus a quantization error ϵ_{IN}, is injected at the input of first and second integrator to reduce the output swing. The injections also involve ϵ_{IN} that is processed in the analog chain. The effect is compensated for with an additional digital processing, as shown in Fig. 4.3. By inspection of the quantizer output plus the feedforward, P_3 is given by

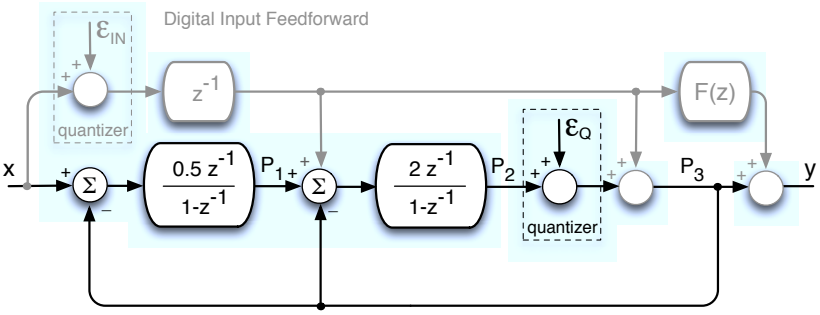

Figure 4.3: Second order ΣΔ modulator with digital input feedforward.

$$P_3 = Xz^{-2} + \epsilon_Q(1 - z^{-1})^2 + \overline{X}(1 - z^{-2}) \tag{4.4}$$

Therefore, the effect of the input signal quantization is removed in the digital domain by using $F(z) = -(1 - z^{-2})$. The result leads to the desired *STF* and *NTF* (noise transfer function). The cost of the method is the extra quantizer at the input, but, since the swing at the input of the ΣΔ quantizer is low, it only requires a few extra comparators.

Obviously, the operation of the methods, either analog or digital, relies on the accuracy and the matching of the extra elements used in the analog section. Possible inaccuracies give rise to noise leakage that reduce the *SNR*. Therefore, a key quality factor is the low sensitivity to components variations.

4.1.3 Proposed Method

Consider again the second order modulator of Fig. 4.1. The main contribution to the output of the first integrator, as given by (4.1), is the signal X multiplied by $H(z) = 0.5z^{-1}(1 + z^{-1})$. Therefore, to compensate for this term, it is possible to use the quantized version of X, $\overline{X} = X + \epsilon_{IN}$. Suppose to add and subtract the same quantity, $\overline{X}H(z)$, at the output of the integrator, which shouldn't change the overall result. This is illustrated in Fig. 4.4(a). To achieve the desired term cancellation, the quantity $-\overline{X}H(z)$ is then moved to the input of the integrator dividing it by the integrator transfer function, as shown in Fig. 4.4(b).

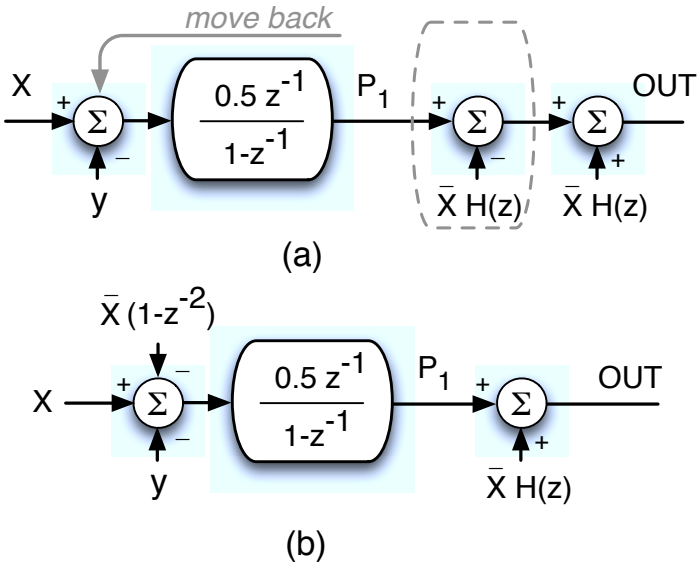

Figure 4.4: Basic idea for the proposed feedforward digital path.

The quantity added at the integrator input becomes $\overline{X}(1-z^{-2})$ and the output of the first integrator is

$$P_1 = -0.5z^{-1}[\epsilon_Q(1 - z^{-1}) + \epsilon_{IN}(1 + z^{-1})] \tag{4.5}$$

The output contains only the quantization error ϵ_Q, shaped at the first order, and ϵ_{IN} multiplied by $(1 + z^{-1})$. For a medium number of bit, the signal is low. The same process can be done for the second integrator (Fig. 4.5)..

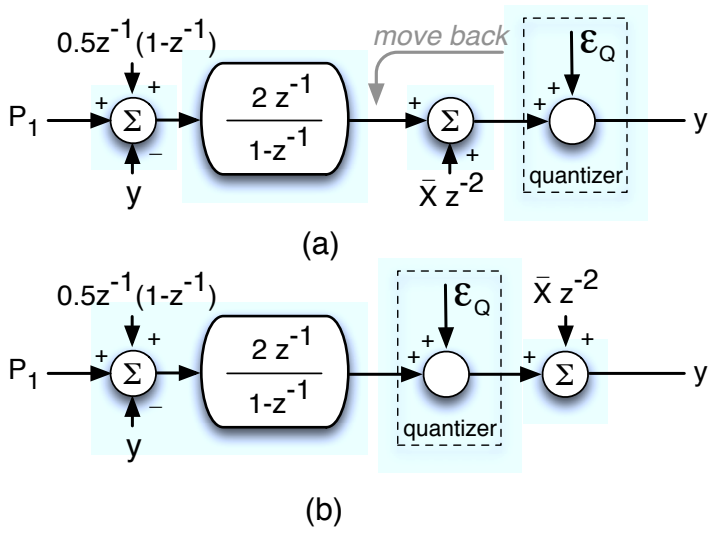

Figure 4.5: Proposed method applied to the second integrator.

Indeed, the output P_2 in a conventional second order (see Fig. 4.1) is

$$P_2 = Xz^{-2} + \epsilon_Q[(1 - z^{-2}) - 1] \tag{4.6}$$

To reduce the output of the second integrator, Xz^{-2} needs to be removed. Using the proposed approach, the transfer function $H(z)$ is z^{-2}, which, referred to the input, becomes $0.5z^{-1}(1 - z^{-1})$. The reconstruction at the output of the second integrator is realized in the digital domain after the quantizer (Fig. 4.5).
Fig. 4.6 shows the proposed second order ΣΔ modulator using the previous approach for both integrators. The injection at the input of the integrators are done using a DAC that converts the output of the digital filter that realizes the transfer functions used to reduce each integrator output dynamic range. Since the filters add a quantity proportional to the integrator denominator, $(1 - z^{-1})$, it is possible to inject this term on the op-amp virtual ground by using the amplifier in the inverting configuration.

The advantage of the proposed architecture is the use of a distributed digital feedforward that reduces the integrator outputs and reconstructs the original *STF* and *NTF* after each integrator. This avoids the quantization noise cancellation being done totally after the quantizer, before and after the loop as in the digital feedforward presented in Fig. 4.3.

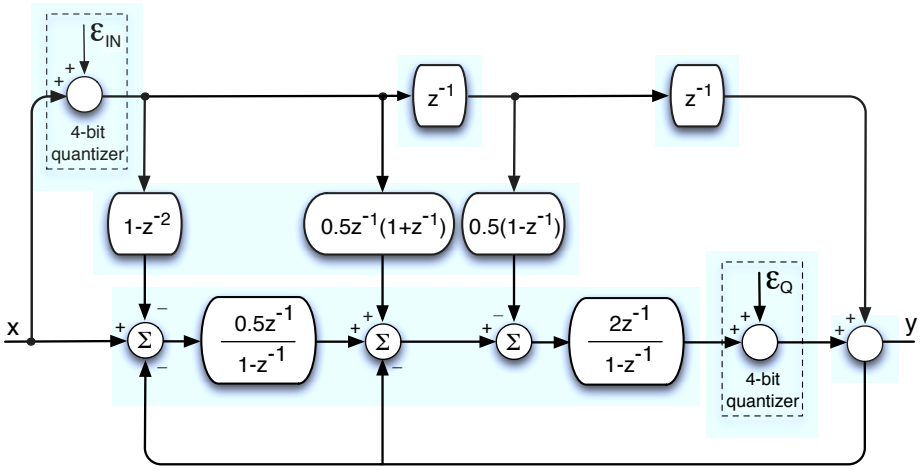

Figure 4.6: Proposed digitally assisted multi-bit modulator block diagram.

4.1.4 Simulation Results

The operation of the above solutions were verified at the behavioral level. The simulations are done using four bit quantizers, both for the input digital conversion and in the loop, an oversampling ratio (OSR) of 10, input amplitude equal to 0 dB and input frequency at the limit of the signal bandwidth ($F_{in} = F_s \cdot \text{nper}/N$, where F_s is the sampling frequency, $nper = 401$ and $N = 2^{13}$ is the number of points used in the FFT). Fig. 4.7 shows the first integrator outputs of three second order modulators, one with the analog feedforward, one using the previous solution shown in Fig. 3, and one with the proposed feedforward approach. The simulation shows that, using the proposed architecture, the dynamic range of the first integrator output is less than half (±0.048) that of the previous digital feedforward approach (±1.12) and a little smaller than the the analog approach (±0.05).

Fig. 4.8 illustrates the benefit at the second integrator output when using analog feedforward. It can be noted that, when using analog feedforward, the output swing is strongly reduced from ±0.45 down to ±0.07. However, as mentioned before, this result has to be paid in term of an increased power consumption, since analog feedforwarding on the second integrator requires an additional active circuit at the quantizer input. This makes this technique not practical.

Fig. 4.9 shows the improvement obtained at the second integrator output when using the proposed technique with respect to the previously presented digital feedforward one (see Fig. 3). Notice that with the proposed approach the swing is reduced from ±0.18 down to ±0.1, value which is comparable with the result obtained with the power hungry analog feedforward solution.

The architectures in Fig. 4.2 (with and without analog feedforward at the second integrator), Fig. 4.3, and Fig. 4.6 were also simulated using real integrators (gain = 1000, slew-rate = 25 $V/\mu s$, unity gain frequency = 400 MHz, saturation = ±0.5), [12], the same

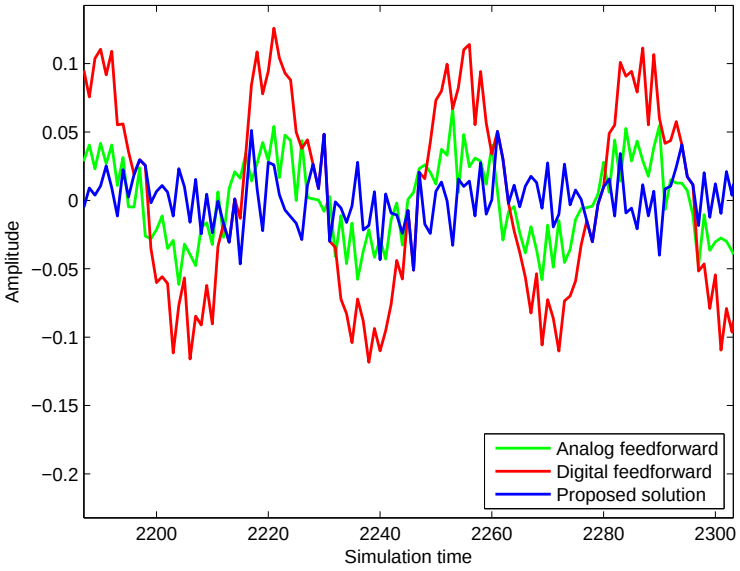

Figure 4.7: First integrator output with analog feedforward, previous digital feedforward, and proposed solution.

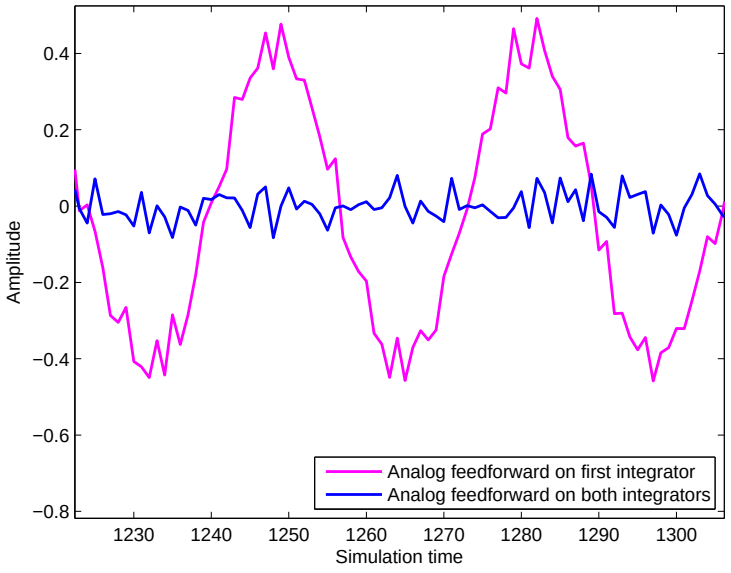

Figure 4.8: Second integrator output swing when using or not analog feedforward.

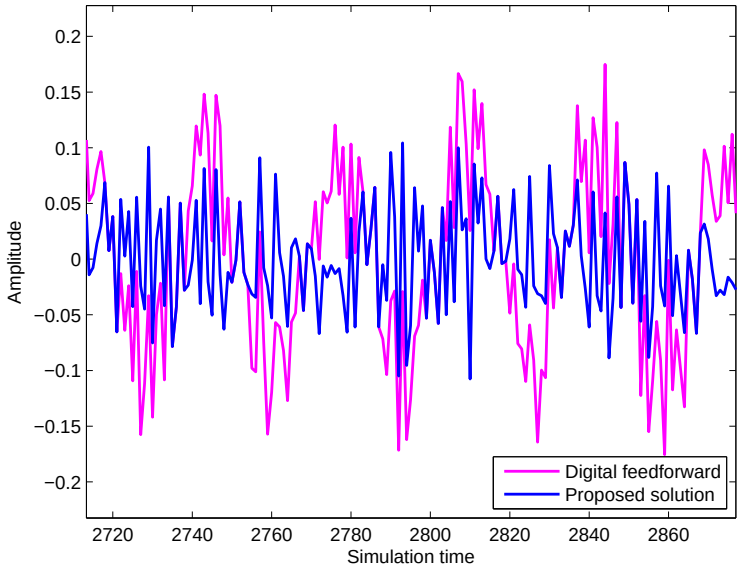

Figure 4.9: Second integrator output with previous digital feedforward path, and with proposed solution.

previous simulation conditions, and F_s = 200 MHz.

Fig. 4.10 shows the resulting output spectra. The SNR is 51 dB for architecture in Fig. 4.2 (without feedforward at the second integrator), 55 dB for the previous digital feedforward, and 60 dB in the proposed solution. Notice that the presented approach obtains about 1 bit and 2.5 bit more with respect to the previous digital feedforward and the analog feedforward (at the first integrator) approaches, respectively, and substantially the same resolution of the completely analog feedforward solution. With the proposed architecture, it is possible to have a medium-high resolution (10 bit) and high signal bandwidth (10 MHz) with a very low power consumption, since a slew rate of only $25V/\mu s$ is required to achieve this performance.

4.1.5 Sensitivity Analysis

Since both in analog and in digital feedforward, a capacitor is used to inject a signal into the loop, the errors in implementing analog coefficients affect both the signal and the noise transfer function. Also in digital feedforward designs, the non-ideality of the input conversion into the digital domain can lower the performance. A statistical analysis estimates the SNR degradation caused by errors in feedforward path coefficients and in comparators thresholds. The study of architectures of Fig. 4.2, Fig. 4.3, and Fig. 4.6 has been performed by using Matlab-Simulink^{TM}environment, using an OSR=10, ideal integrator, and four bit quantizers. All simulations use for each injection an error Δ_1 equal to

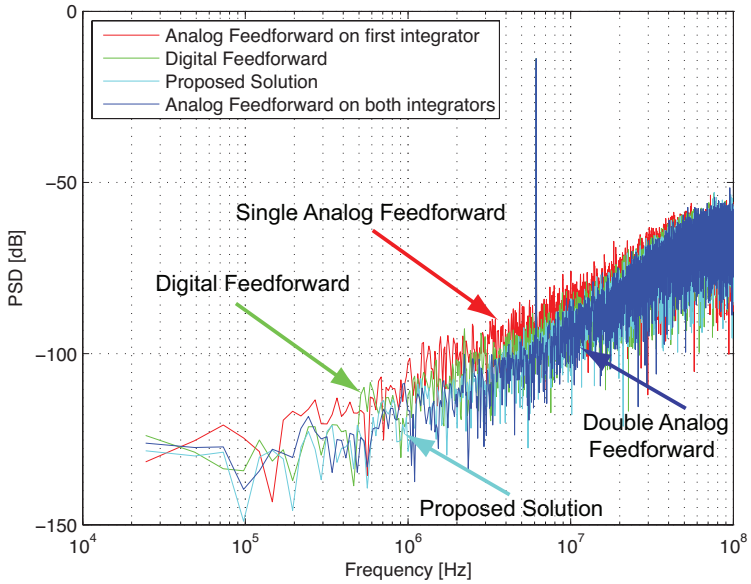

Figure 4.10: Output spectra for different architectures simulated with real integrators.

a normally distributed white random variable of zero mean, with standard deviation (σ) equal to $3 \cdot 10^{-3}$, and an error Δ_2 equal to a normally distributed white random variable of zero mean, with standard deviation (σ) equal to $3 \cdot 10^{-2}$ for the comparators thresholds. Simulation results are shown in Fig. 4.11 with 200 samples for each design. The *SNR* for the analog feedforward approach (both on first and second integrator) is higher than 59 dB in about 75% of total cases. The previous digital feedforward architecture of Fig. 4.3 gives a *SNR* higher than 60 dB in 85% of cases. The proposed approach obtains *SNR* higher than 62 dB in about 90% of total cases, demonstrating that the robustness and the effectiveness of the method. It is finally worth to point out that the presented design approach can be extended and applied to higher order $\Sigma\Delta$ modulators.

4.2 Optimum Selection of Capacitive Array for Multi-bit Sigma-Delta Modulators without DEM

A method for a smart selection and sequencing of unity capacitors in a multi-bit DAC is proposed. The approach, suitable for the DAC nonlinearity correction in Sigma-Delta modulators, obtains results that are better than the Dynamic Element Matching. Key of the technique is an off-line self-measurement of mismatches. The results significantly improve when the DAC capacitors are selected from a set that is larger than required. An affordable silicon area overhead avoids extra power consumption during the normal operation of the converter.

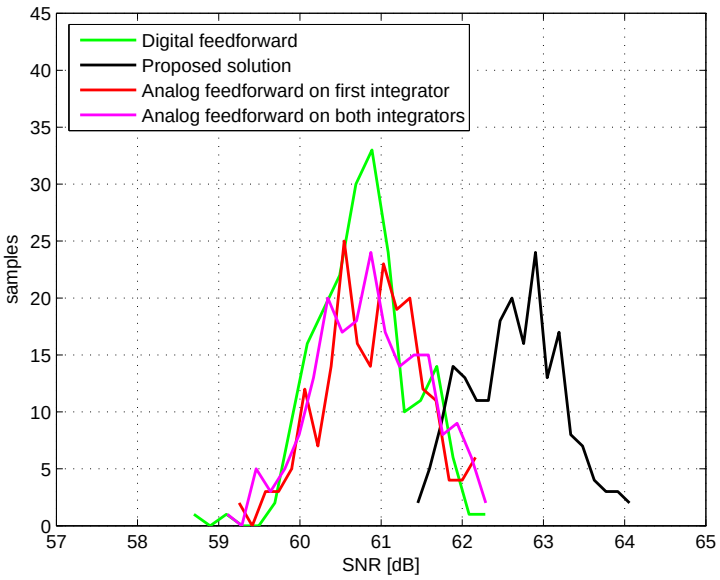

Figure 4.11: Simulated *SNR* for the architecture analyzed in this section, introducing errors in coefficients and in comparators thresholds.

4.2.1 Motivations, Solutions, and Results

Recent commercial applications in the telecommunication and sensor area utilize analog-to-digital converters (ADC) to ensure lower power and better processing. However, the challenges placed by those applications to ADC's push the ADC's to their performance limits, asking for new methods that obtain high performance but reduced power consumption. Recent applications aim at ADC's with medium-to-high resolution and very high operation speed. Since the use of digital technologies is another common constraint, the use of multi-bit Sigma-Delta ($\Sigma\Delta$) ADC's is a good choice. However, the linearity of the DAC in the ADC's is a general limitation. There are many design dimensions that increase resolution of $\Sigma\Delta$-ADC's. Among them the order of the modulator and the oversampling ratio, normally pushed to the limits for best performance. Also increasing the number of bit in the DAC increases resolution but, as mentioned, the linearity becomes a critical design parameter. Calibration and trimming methods were introduced for multi-bit solutions. However, these methods cost overhead to the system during conversion thus, increasing the power consumption. In addition, some of the methods use blind averaging which prevents from achieving the best solution. One well known approach is the Dynamic Elements Matching (DEM) [13] that scrambles or sequentially uses the unity elements of the DAC that, according to a given algorithm, eventually obtains noise shaping of the mismatch error. However, error is not reduced but it is only transformed into a pseudo-noise that is a possible source of tones in the signal band. Moreover, the required logic circuitry operates

at the oversampled frequency, increases the consumed power and reduces the effectiveness of the converter.

This solution exploit the possibility offered by the ΣΔ modulator to perform a preliminary measure of the unity elements value in the DAC and uses the information for a smart selection of elements, thus avoiding DEM, while obtaining excellent performances.

4.2.2 Proposed Method

The DAC used in ΣΔ modulator is made by a set of N unity capacitors, C_u, nominally equal. The mismatch among them makes each

$$C_i = C_u + \varepsilon_i. \tag{4.7}$$

The sequence of errors ε_i has a systematic and random component that cause a deviation of the transfer characteristic of the DAC from the linear behavior. The DEM technique transform the error to into a pseudo-noise whose input referred voltage power is

$$V_{n,\varepsilon}^2 = \frac{V_R^2}{C_{u^2}} \sum_{i=1}^{N} \varepsilon_i^2. \tag{4.8}$$

A random scrambling spreads that power uniformly over the Nyquist interval whereas other methods may obtain shaping. The result is normally suitable for a σ of mismatch well below 1% and resolution of 12-14 bit.

Suppose now to know the value of the sequence of errors, ε_i. Instead of dynamic use of elements it is possible to consider a "smart" use of elements that optimize the INL of the DAC. Assuming to have just a systematic error, the INL may look like the one of Figure 4.12 (a). A proper sequence of the unity elements can change the INL diagram into the one of Figure 4.12 (b) that has a lower maximum amplitude and a more busy behavior.

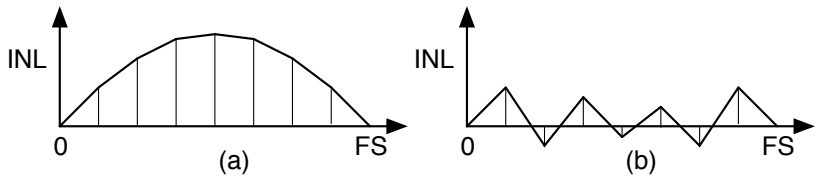

Figure 4.12: INL of a) a systematical error b) a proper sequence.

Notice that the INL of Fig. 4.12 (b) is not a good choice for small input amplitudes in a Nyquist rate DAC but is optimal when the DAC is used in a ΣΔ modulator. The digital output that controls the DAC is the input plus a shaped quantization noise, whose maximum amplitude is the quantization step. Therefore, the control of the DAC is inherently a dynamic averaging of the DAC levels corresponding to the input amplitude over two or more neighbor quantization intervals. The effect, as verified shortly by computer simulations, is to smooth the effect and to obtain negligible harmonic tones.

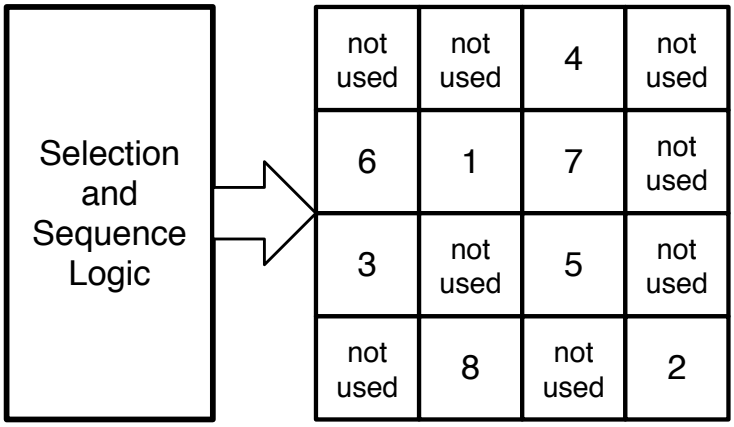

Figure 4.13: Layout diagram of a possible capacitor array.

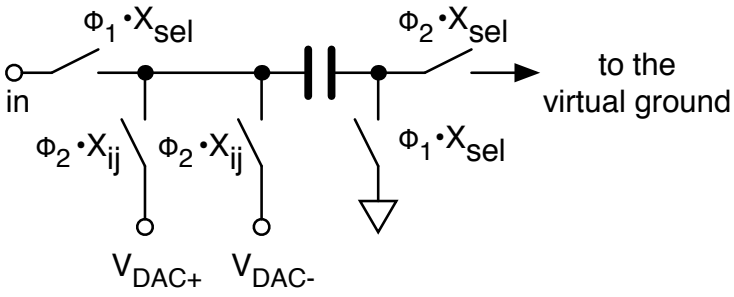

Figure 4.14: Switched capacitor scheme of the single unity element.

Suppose that the available number of elements is more than what is needed by the DAC. For example 9 or 16 when 8 are needed for a 3-bit DAC. Knowing the mismatches it is possible to choose the most favorable elements for the optimal sequence. This, as verified by simulations further improves the INL. Hence, the proposed approach provide different levels of accuracy depending on the silicon area that can be allocated for this capacitors and the control logic. For example, with a 3-bit DAC, 16 elements can be arranged in a square matrix and the smart selection can use the elements and the sequence of Fig. 4.13, where a suitable logic determines the capacitances to be used and the sequence.

The circuit implementation with more capacitors (i.e. 16) and 3-bit DAC can use separate elements or the same elements for the sampling of input and for the DAC. In the latter case, it is necessary to generate an extra logic signal that identifies the set of unity elements to be charged to the input, for avoiding an extra capacitive load to the input terminal. An elementary generic element and the used switches are shown in Fig. 4.14. It uses two controls signals one for the selection and the other for the DAC function.

4.2.3 Error measurement

The value measurement of the N capacitors of the array is performed off-line using the ΣΔ architecture itself. The scheme is re-configured as incremental [15], [16], i.e. the charge stored in two integrators is reseted. A fixed voltage, V_{Meas} lower than $Vref/N$ is applied to the input. The output of the modulator is a bit-stream that uses none or just one capacitor only, the one under measure, C_i. The use of a cascade of integrators (one more than the order of the modulator) provides the digital measure of the input voltage multiplied by the input gain

$$V_{out,i} = \frac{C_i}{C_f} V_{Meas} \tag{4.9}$$

since C_f, the feedback capacitance is $\sum_1^N C_i$, the digital output is the measure of C_i multiplied by an unknown ratio. If the same reference voltage is used for the measure with all the unity elements, the results are a relative measure of the values that enables to estimate the mismatches.

With a second order modulator the use of three cascades integrators for K clock periods obtain $K(K+1)(K+2)/6$ as full scale. Therefore, the accuracy of the measurement is approximately $1/(3log_2K - 3)$. Therefore by selecting $K = 2^8$ the relative value of each capacitor is measured with more than 20 bit of accuracy.

Once the measurement for a capacitor is performed, the set with the best matching is selected. Then, a suitable algorithm for having the minimum INL is performed.

4.2.4 Optimum Selection

The optimum selection of N elements out of M available corresponds to the set with minimum relative differences. A possible algorithm, used in the simulations described in the next section, employs the partial average value $\bar{C}_i$ taken from a set of $(K-1)$ elements that excludes C_i

$$\bar{C}_i = \frac{1}{K-1}\sum_{j\neq i} C_j. \tag{4.10}$$

The selection starts with $K = M$ and eliminates the element for which the distance D_i

$$D_i = (C_i - \bar{C}_i)^2 \tag{4.11}$$

is maximum. Then, $K = M - 1$ and the test continues with eliminations of one by one element until reaching the number of elements required by the DAC.

The choice of the optimal sequence of N elements, $C_1, C_2, \cdots, C_N$, whose average value is $\bar{C} = 1/N \sum C_i$, is done according to the following algorithm:

The first selected element, $C_{s,1}$ is the one that obtains the minimum value of

$$\Delta_1 = (C_i - \bar{C})^2. \tag{4.12}$$

The next element obtains the minimum

$$\Delta_2 = (C_i + C_{s,1} - 2\bar{C})^2, \tag{4.13}$$

and so forth. The selected elements and the optimal sequence control a switch matrix that uses the thermometric control of the DAC to provide the logic signals used in the switched capacitor scheme of Fig. 4.14. Fig. 4.15 gives an example of possible switch matrix with 16 unity elements for a 3-bit DAC. The measure of the elements value and the described algorithms select the first, third, fourth and so forth capacitors. The control of the others is grounded by the switches on the top. The first capacitor is used to convert the bit T6 of the thermometric signal, the third converts T3 and so forth. Therefore, the circuit overhead is the matrix of Fig. 4.15 and the memory that gives the static controls of switches. The handled signal is digital and the use of a switch does not affect, in practice, the speed.

4.2.5 Simulation Results

The proposed approach has been simulated at the behavioral level with various mismatches and signal amplitudes. The first study concerned the evaluation of the INL in different foreseen cases.

Fig. 4.16 shows the statistical distribution of the absolute value of the INL obtained with a 3-bit DAC made by unity capacitances with random mismatch with $\sigma = 0.01$. The distribution concerns 100 cases. The value of the INL ranges from 0.7 to 2.7%. The average loss for the SNR in a 3-bit second-order modulator with OSR=32 is 15 dB. Moreover a tone at -79 dB with $-6dB_{FS}$ appears. Starting from same mismatched cases, with only 8 elements the algorithm of optimum sequence obtains the histogram of Fig. 4.17. The distribution is strongly concentrated around 0.005 that is half the value of the used σ. Moreover, the proper sequence makes the INL plot suitable for smoothing thanks to the quantization noise random variation.

The histogram of Fig. 4.17 shows that a small number of cases are not properly brought to a low value of INL. They are caused by the mathematical tails of the statistic distribution

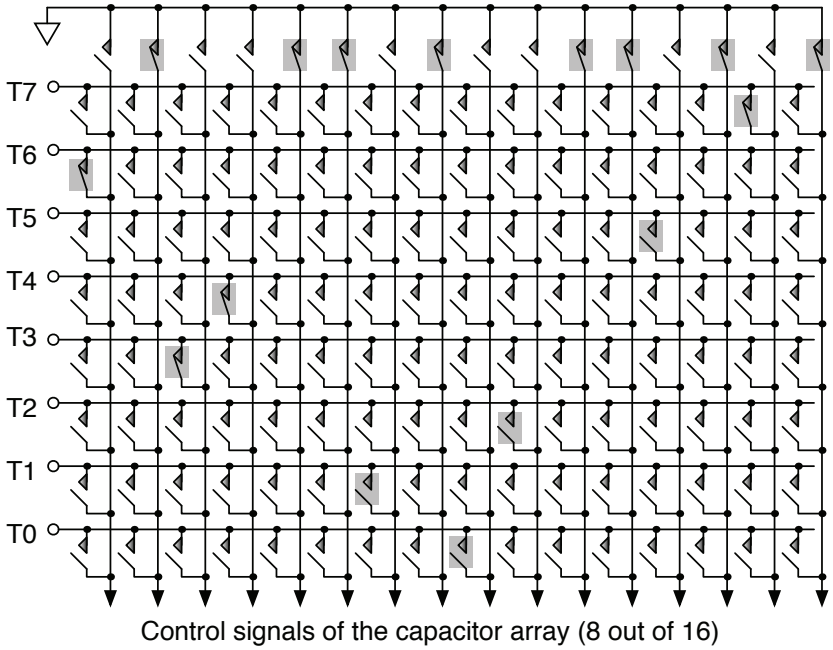

Figure 4.15: Matrix of switches suitable for the control of a DAC that uses 8 out of 16 unity elements.

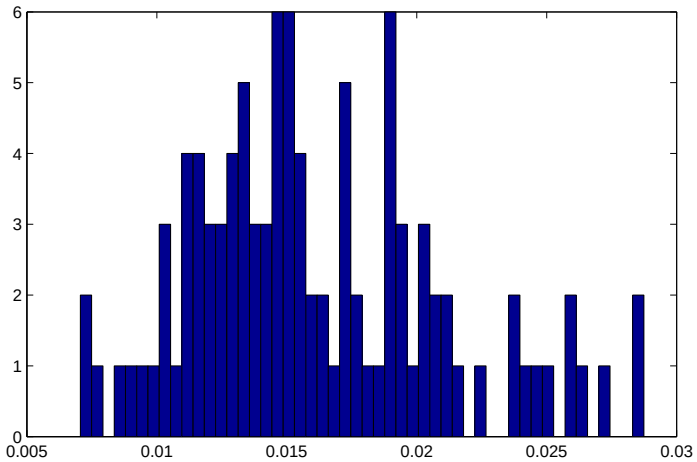

Figure 4.16: Maximum absolute value of the INL of a 3-bit DAC with a 0.01 σ error.

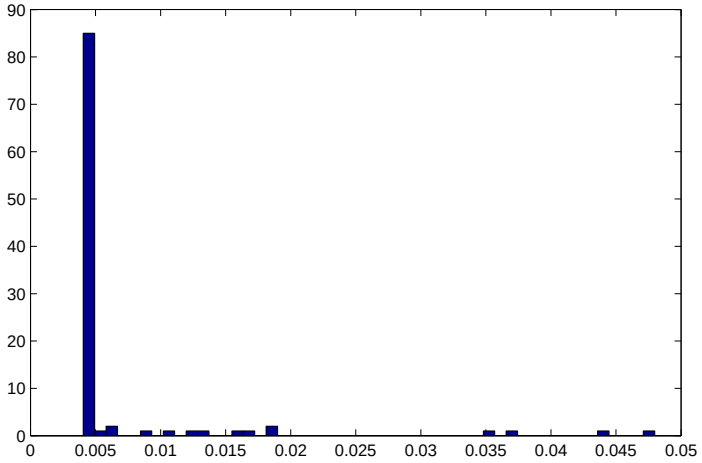

Figure 4.17: Maximum absolute value of the INL of a 3-bit DAC with a 0.01 σ error, after optimum selection.

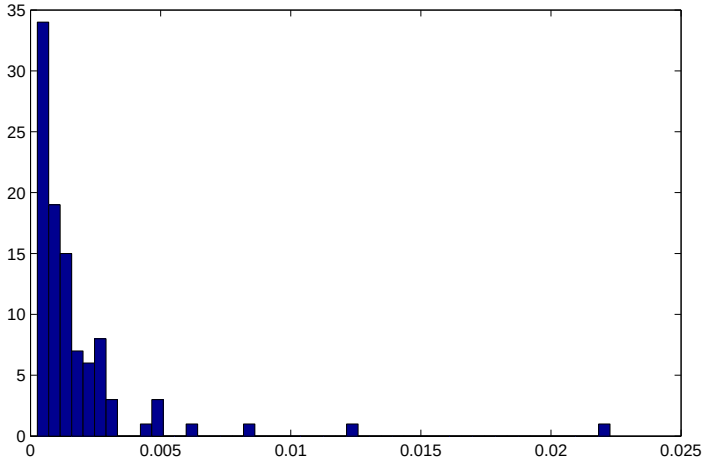

Figure 4.18: Maximum absolute value of the INL of a 3-bit DAC with a 0.01 σ error with optimum selection and 9 elements.

that foresee values of unity capacitances with a large error. Indeed, in real situations having a big error is not possible and the real statistical distribution is not with a fully random added term.

Notice that in order to obtain an INL curve like the one of Fig. 4.12 it is necessary to have pair of capacitors whose value are symmetrical with respect to the average. If, for example, the set of 8 capacitors is made by 5 elements bigger and 3 smaller than the average value the algorithm cannot pair a bigger and a smaller element. Consequently, the INL will show, somewhere, two consecutive increases. Obviously the situation is worst with a $6-2$ or a $7-1$ distribution around the average. These cases and the the effect of tails are the possible limit the yield even when considering the real statistical distribution.

A possible systematic error in the unity capacitor values is transformed into alternate fluctuations of the INL that, as mentioned is smoothed by the effect of the quantization error. Simulation results shows that the effect of systematic contributions is negligible until very large gradients that cause an overall change of unity elements as large as $10-15\%$.

The result of Fig. 4.17 denotes a good improvement but some worst cases make the possible yield non acceptable. In order to improve the effectiveness of the method the 8 elements are selected from a set with extra parts. The statistic distribution significantly improves with only one extra capacitor, as shown in Fig. 4.19. The value of the INL is often below 0.2% with few cases of values larger than 0.6%. The worst situations correspond to the $6-2$ distribution around the average because the probability to have $7-1$ is almost zero.

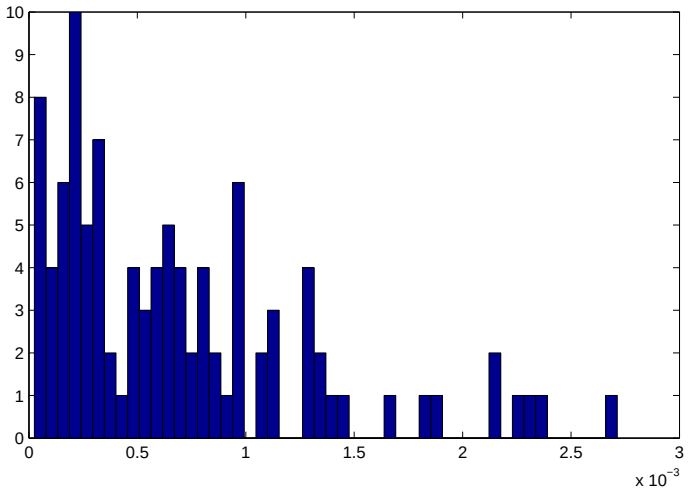

Figure 4.19: Maximum absolute value of the INL of a 3-bit DAC with a 0.01 σ error with optimum selection and 16 elements.

Obviously, the use of more element to perform the selection improves the INL histogram. Fig. 4.19 shows that with 16 elements and optimum sequence the INL improves by almost an order of magnitude with respect to the plain case.

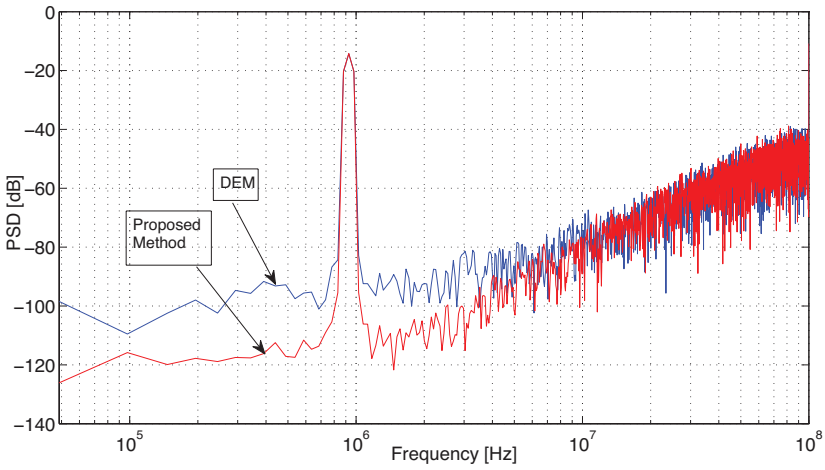

Figure 4.20: Output spectra obtained with the proposed method and DWA-DEM. The capacitor mismatch in the 3-bit DAC is $\sigma = 0.01$.

The improved INL and the optimum sequence obtain performances better than the DEM with a mismatch as large as 1%. Fig. 4.20 shows the output spectra the SNR of a second order fully differential modulator for the proposed method, that is unchanged with respect to the ideal case, and the spectrum of a modulator with DWA-DEM that starts deviating from the ideal response for OSR > 20. The average SNR loss with OSR = 32 is 7 dB.

The benefit of the method is unchanged for low input amplitudes. Fig. 4.21 shows that the spectra (with a different set of unity capacitors and $\sigma = 0.01$) have similar behavior. The one of the proposed method still follows the case without mismatch, thus demonstrating the smoothing effect of the quantization noise.

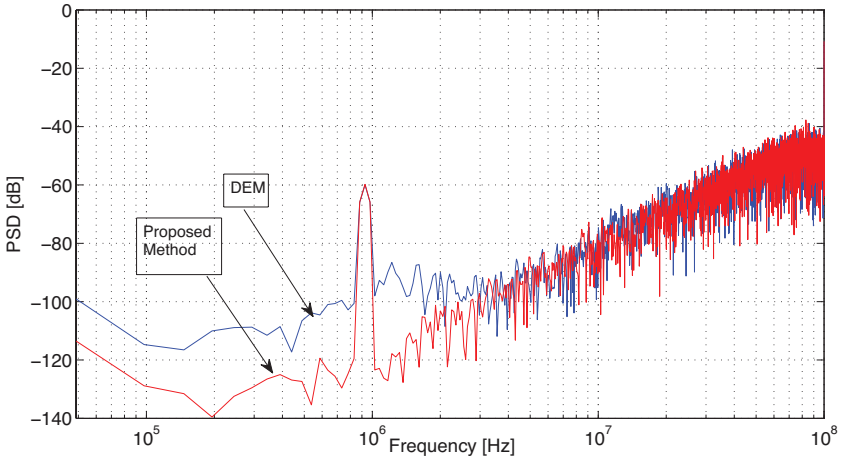

Figure 4.21: Output spectra of the case of Fig. 9 with -60 dB input amplitude.

Chapter 5

Conclusion

This Ph.D. thesis presents the study and the design at transistor level of a band pass ΣΔ modulator for Wide-Band Code Division Multiple Access (WCDMA) applications and a complex band pass ΣΔ modulator for Body Area Network applications. The activity involves the analysis at the behavioral level in Matlab-Simulink^{TM}environment, the transistor level design, and the layout of the two modulators. For the first project there is also the description of the PCB design and the test chip results. Both modulator are novel architectures and achieve results at the state of the art.
The first project is the design of a MASH band pass ΣΔ modulator for Wide-band Code Division Multiple Access (WCDMA) applications. The signal bandwidth of the proposed modulator is 10 MHz, centered around an intermediate frequency (IF) of 70 MHz. The target is to have four complex conjugate zeros around the IF and a resolution of 13 bit in a 10 MHz bandwidth. To obtain this goal it's designed a MASH bandpass modulator to obtain multiple zeros. The MASH architecture is made by two band pass ΣΔ modulators. Each modulator based on a two-path architecture, which allow to obtain the desired in-band noise shaping zeros and reduce the power consumption. The ΣΔ modulator is implemented using a 0.18-μm CMOS technology and a sampling frequency of 180 MHz. The simulations at transistor level show a resolution of about 13 bit, with a bandwidth of 10 MHz, and a power consumption of about 90 mW, with a supply voltage of 1.8 V. The resulting figure of merit is 0.16 pJ/conversion-level. The mesurement results shows a resolution of 11.7 bit in a bandwidth of 10 MHz. The power consumption is 95 mW, and the resulting figure of merit is equal to 0.42 pJ /conversion-level. The project was in collaboration with National Semiconductor.
The second project is the design of a complex band pass ΣΔ modulator for Body Area Network Applications. The proposed novel architecture is based on a method that limits the zero positioning but allows to obtain simple approach in the design at transistor level. The principle of the architecture is to use cross-coupled feedback of the real path and the quadrature path, and the injection of the quantization noise coming from both path. In this way is generated a noise transfer function with two zeros around the IF and with no zeros in the image. The target is to have a resolution of 6 - 7 bit resolution with a bandwidth of 2.6 Mz, and 8 - 10 bit resolution with a bandwidth of 100 kHz. The intermediate frequency

(IF) is 2.5 MHz. The ΣΔ modulator is implemented using a 0.18-μm CMOS technology and a sampling frequency of 20 MHz. The simulations at transistor level show a resolution of about 8 bit, with a bandwidth of 2.6 MHz, and a resolution of 10 bit, with a bandwidth of 100 kHz. The power consumption is 1.95 mW, with a supply voltage of 1.8 V. The resulting figure of merit is 1.7 pJ/conversion-level, which is at the state of the art for complex band pass ΣΔ modulator. The project was in collaboration with Analog Devices.
The thesis reports also the study of some non-conventional architectures for the design of ΣΔ modulators.

Appendix A

Information about Wide-Band Code Division Multiple Access

WCDMA is a kind of multiple access method used in telecommunication. Multiple access means the joint use by multiple users of a single resource represented by a bandwidth portion of the transmission medium, considering a preassigned distribution of its potential. There are several multiple access techniques: FDMA (Frequency Division Multiple Access), TDMA (Time Division Multiple Access), and CDMA (Code Division Multiple Access). The frequency division multiple access (FDMA) channel-access scheme is based on the frequency-division multiplex (FDM) scheme, which provides different frequency bands to different data-streams. In the FDMA case, the data streams are allocated to different users or nodes. An example of FDMA systems were the first-generation (1G) cell-phone systems. A related technique is wave-length division multiple access (WDMA), based on wavelength division multiplex (WDM), where different users get different colors in fiber-optical communication. The time division multiple access (TDMA) channel access scheme is based on the time division multiplex (TDM) scheme, which provides different time-slots to different data-streams (in the TDMA case to different transmitters) in a cyclically repetitive frame structure. For example, user 1 may use time slot 1, user 2 time slot 2, etc. until the last user. Then it starts all over again. Packet mode multiple-access is typically also based on time-domain multiplexing, but not in a cyclically repetitive frame structure, and therefore it is not considered as TDM or TDMA. Due to its random character it can be categorized as statistical multiplexing methods, making it possible to provide dynamic bandwidth allocation.
CDMA is a channel access method used by various radio communication technologies. CDMA employs spread-spectrum technology. A special coding scheme is assigned to each transmission to allow multiple users to be multiplexed over the same physical channel. By contrast, time division multiple access divides access by time, while frequency-division multiple access divides it by frequency. CDMA is a form of spread-spectrum signaling, since the modulated coded signal has a much higher data bandwidth than the data being communicated, because the code has frequency higher than the frequency signal. Each user in a CDMA system uses a different code to modulate their signal. Choosing the codes

used to modulate the signal is very important in the performance of CDMA systems. The best performance will occur when there is good separation between the signal of a desired user and the signals of other users. The separation of the signals is made by correlating the received signal with the locally generated code of the desired user. If the signal matches the desired user's code then the correlation function will be high and the system can extract that signal. If the desired user's code has nothing in common with the signal the correlation should be as close to zero as possible (thus eliminating the signal); this is referred to as cross correlation. If the code is correlated with the signal at any time offset other than zero, the correlation should be as close to zero as possible. An analogy to the problem of multiple access, see Fig. A.1, is a room (channel) in which people wish to communicate with each other. To avoid confusion, people could take turns speaking (time division), speak at different pitches (frequency division), or speak in different languages (code division). CDMA is analogous to the last example where people speaking the same language can understand each other, but not other people. Similarly, in radio CDMA, each group of users is given a shared code. Many codes occupy the same channel, but only users associated with a particular code can communicate.

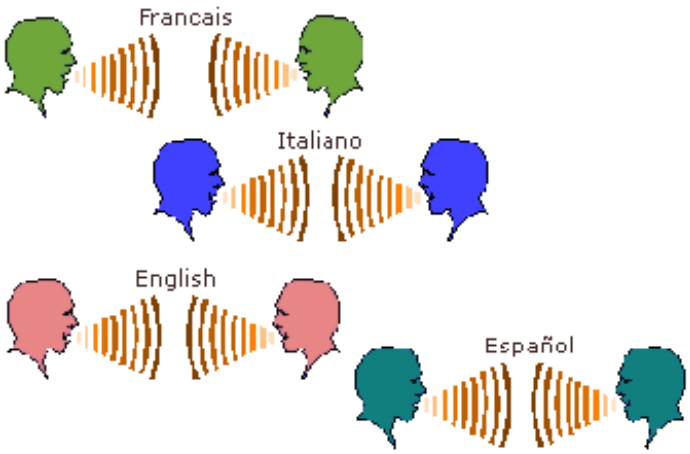

Figure A.1: Analogy to the problem of multiple acces.

In the late 1990s, W-CDMA was developed by NTT DoCoMo as the air interface for their 3G network FOMA. Later NTT DoCoMo submitted the specification to the International Telecommunication Union (ITU) as a candidate for the international 3G standard known as IMT-2000. The ITU eventually accepted W-CDMA as part of the IMT-2000 family of 3G standards, as an alternative to CDMA2000, EDGE, and the short range DECT system. Later, W-CDMA was selected as an air interface for UMTS. As NTT DoCoMo did not wait for the finalisation of the 3G Release 99 specification, their network was initially incompatible with UMTS. However, this has been resolved by NTT DoCoMo updating their network. Code Division Multiple Access communication networks have been developed by a number of companies over the years, but development of cell-phone networks

based on CDMA (prior to W-CDMA) was dominated by Qualcomm. Qualcomm was the first company to succeed in developing a practical and cost-effective CDMA implementation for consumer cell phones: its early IS-95 air interface standard, which has since evolved into the current CDMA2000 (IS-856/IS-2000) standard.

Appendix B

Information about Body Area Network

Body Area Network (BAN), Wireless Body Area Network (WBAN) or Body sensor network (BSN) are terms used to describe the application of wearable computing devices. This will enable wireless communication between several miniaturized Body Sensor Units (BSU) and a single Body Central Unit (BCU) worn at the human body. The rapid growth in physiological sensors, low power integrated circuits and wireless communication has enabled a new generation of wireless sensor networks. These wireless sensor networks are used to monitor traffic, crops, infrastructure and health. The Body Area Network field is an interdisciplinary area which could allow inexpensive and continuous health monitoring with real-time updates of medical records via internet. A number of intelligent physiological sensors can be integrated into a wearable wireless body area network, which can be used for computer assisted rehabilitation or early detection of medical conditions. This area relies on the feasibility of implanting very small bio-sensors inside the human body that are comfortable and that don't impair normal activities. The implanted sensors in the human body will collect various physiological changes in order to monitor the patient's health status no matter their location. The information will be transmitted wirelessly to an external processing unit. This device will instantly transmit all information in real time to the doctors throughout the world. If an emergency is detected, the physicians will immediately inform the patient through the computer system by sending appropriate messages or alarms. Currently the level of information provided and energy resources capable of powering the sensors are limiting. While the technology is still in its primitive stage it is being widely researched and once adopted, is expected to be a breakthrough invention in healthcare, leading to concepts like telemedicine and mHealth becoming real. Initial applications of BANs are expected to appear primarily in the healthcare domain, especially for continuous monitoring and logging vital parameters of patients suffering from chronic diseases such as diabetes, asthma and heart attacks. A BAN network in place on a patient can alert the hospital, even before he has a heart attack, through measuring changes in his vital signs. A BAN network on a diabetic patient could auto inject insulin though a pump, as soon as his insulin level declines, thus making the patient doctor-free and virtually healthy.

Other applications of this technology include sports, military, or security. Extending the technology to new areas could also assist communication by seamless exchanges of information between individuals, or between individual and machines. A typical BAN or BSN requires vital sign monitoring sensors, motion detectors (through accelerometers) to help identify the location of the monitored individual and some form of communication, to transmit vital sign and motion readings to medical practitioners or care givers. A typical Body Area Network kit will consist of sensors, a processor, a transceiver and a battery. Physiological sensors, such as ECG and SpO2 sensors, have been developed. Other sensors such as a blood pressure sensor, EEG sensor and a PDA for BSN interface are under development.
Fig. B.1 shows an example of BAN.

Figure B.1: Body Area Network example.

Problems with the use of this technology could include:

- Interoperability: WBAN systems would have to ensure seamless data transfer across standards such as Bluetooth, ZigBee etc. to promote information exchange, plug and play device interaction. Further, the systems would have to be scalable, ensure efficient migration across networks and offer uninterrupted connectivity.

- System Devices: sensors used in WBAN would have to be low on complexity, small in form factor, light in weight, power efficient, easy to use and reconfigurable. Further, the storage devices need to facilitate remote storage and viewing of patient data as well as access to external processing and analysis tools via internet.

- System and device-level security: Considerable effort would be required to make BAN transmission secure and accurate. It would have to be made sure that the patients data is only derived from each patients dedicated BAN system and is not

mixed up with other patients data. Further, the data generated from WBAN should have secure and limited access.

- Invasion of privacy: People might consider the WBAN technology as a potential threat to freedom, if the applications go beyond secure medical usage. Social acceptance would be key to this technology finding a wider application.

- Sensor validation: Pervasive sensing devices are subject to inherent communication and hardware constraints including unreliable wired/wireless network links, interference and limited power reserves. This may result in erroneous datasets being transmitted back to the end user. It is of the utmost importance especially within a healthcare domain that all sensor readings are validated. This helps to reduce false alarm generation and to identify possible weaknesses within the hardware and software design.

- Data consistency: Data residing on multiple mobile devices and wireless patient motes need to be collected and analysed in a seamless fashion. Within Body Area Networks, vital patient datasets may be fragmented over a number of nodes and across a number of networked PCs or laptops. If a medical practitioners mobile device does not contain all known information then the quality of patient care may degrade.

BAN is a promising technology which can revolutionize next generation healthcare and entertainment applications. BAN brings out a new set of challenges in terms of scalability, energy efficiency, antenna design, QoS, coexistence, interference mitigation,security and privacy. Developing a unifying BAN standard which addresses the core set of technical requirements is the quintessential step for unleashing the full potential of BANs, and is currently under discussion in the IEEE 802.15.6 Task Group. In the end several non-technical factors would also play crucial roles in the success of the BAN technology in mass marketing, such as affordability, legal, regulatory and ethical issues, and user friendliness, comfort and acceptance. BAN technology needs the widespread acceptance of key stakeholders in the healthcare domain, including the medical-electronics industry, patients, caregivers, policy makers, patient advocacy groups and ordinary consumers for it to become a truly pervasive technology.

Appendix C

Publications

1. H. Caracciolo, E. Bonizzoni and F. Maloberti, "Quasi-Second Order Sigma Delta Modulator Based on Phase Integration", IEEJ AVLSI 2007, November 2007, pp. 19 - 22.

2. H. Caracciolo, I. Galdi, E. Bonizzoni and F. Maloberti, Band-Pass ΣΔ Architectures with Single and Two Parallel Paths", IEEE Int. Symp. on Circuits and Systems (ISCAS), May 2008, pp. 1656 - 1659.

3. H. Caracciolo, S. Talay and F. Maloberti, "Optimum Selection of Capacitive Array for Multibit Sigma-Delta Modulators without DEM", IEEE Int. Conference on Electronics, Circuits, and Systems, (ICECS), December 2009, pp. 759 - 762.

4. H. Caracciolo, E. Bonizzoni, P. Malcovati, F. Maloberti, "Design of a 70-MHz IF 10-MHz Bandpass Sigma-Delta Modulator for WCDMA Applications", IEEE International Symposium on Circuits and Systems, ISCAS '10, May 30 - June 2 2010, pp. 2406 - 2409.

5. H. Caracciolo, E. Bonizzoni, F. Maloberti, G. S. La Rue, "Digitally Assisted Multi-Bit Sigma-Delta Modulator", IEEE International Symposium on Circuits and Systems, ISCAS '10, May 30 - June 2 2010, pp. 3993 - 3996.

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