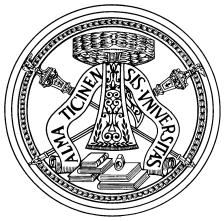

Università degli Studi di Pavia

Facoltà di Ingegneria

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Dottorato di Ricerca in Microelettronica
XXIV ciclo

STUDY, MODELING AND REALIZATION OF AN AUDIO CLASS-D POWER AMPLIFIER IN 0.18µm CMOS TECHNOLOGY

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Davide.

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Introduction

Since portable devices, such as as phones, MP3 readers, and laptops became more and more popular, microelectronic researchers have dealt with a strong request of high performance devices with very limited power consumption. This kind of request is more important today than in the past ten years, due to all the applications and features that a portable device is supposed to have. For example, the synergy between phones and last generation network services, like blogs or social networks, needs devices with a lot of functions and a computing power very close to the power of a PC.

One of the most popular functions in the today's market is the capability to record and to playback audio/video files, normally with HD quality. If advances in silicon technology reduced the power consumption of image sensors and displays, in the audio field the power levels that come in to play have remained unchanged over the past twenty years, due to the final transducers of the reproduction chain: the speakers. Most of these, in fact, although improved, show the same electro-mechanical operating principle that, to work properly, need high performance driver stages in terms of both noise and load current capability. For these reasons, new amplifier classes, such as Class-D or Class-G, also if more complex with respect to conventional Class-A or Class-AB, are becoming a standard in mobile applications, due to their capability to combine high audio quality (low harmonic distortion) with low power consumption (high efficiency).

In particular, in this thesis a study on Class-D audio amplifiers will be presented: starting from high level modeling and passing through synthesis, two versions of a power audio system used as the output stage of a pre-existing digital CODEC have been realized.

In Chapter 1 the general aspects of an audio signal and the main specifications that must be taken into account during the design of a generic audio system will be discussed. Chapter 2, starting with an overview and a comparison between the main amplifier classes used in audio applications, it is then focused on Class-D structures: advantages, disadvantages and main characteristics will be discussed and a design methodology will also be introduced. In Chapter 3 both the first version (Ver. 1 – Test chip) and the second version (Ver. 2 – Stereo chip) of the designed Class-D amplifier are presented. Modeling, schematics and design choices are reported for both amplifiers together with simulation results. Measurement results are reported only for Ver. 1, since Ver. 2 is presently being fabricated. The conclusions are discussed in Chapter 4.

Chapter 1

Audio signals: general properties and specifications

Few fields of technical endeavor are more plagued with errors, mis-statements and confusion than audio. In the last 20 years, the rise of controversial and non-rational audio hypotheses, gathered under the title "subjectivism", has deepened these difficulties. It is commonplace for hi-fi reviewers to claim that they have perceived subtle audio differences which cannot be related to electrical performance measurements. For a subjectivist, in fact, objective measurements of an amplifier performance are unimportant compared with the subjective impressions received in informal listening tests: in contrast with most technology fields, where improvements of defined and accepted performance measurements (e.g. km/h or km/l in the automotive field, or *MIPs* in computer manufacturing) are unequivocally considered a step forward, in the field of hi-fi, many people seem to have difficulties in deciding which is the forward direction [1].

A less irrational vision of the audio environment is given by psychoacoustic that, in contrast with subjectivism, is based on a vast amount of hard scientific information, obtained by subjective tests performed on human patients. Results, averaged over a large number of subjects, give an accurate idea of the features and responsivity that usually the human hearing apparatus has and, being by now very accurate and well modeled, they are often used to improve the design of audio systems. The main results of psychoacoustic may be briefly summarized as follows:

- the human ear can generally hear sounds with frequencies between 20 Hz and 20 kHz and the upper limit generally decreases with age;
- the smallest step-change in amplitude that can be detected is about 0.3 dB for a pure tone; in more realistic situations it is 0.5 to 1.0 dB, corresponding to about a 10% change [2];
- the smallest detectable change in frequency of a tone is about 0.2% in the band 500 Hz – 2 kHz; in terms of percentage this is the parameter for which the ear is most sensitive [3];
- the least detectable amount of harmonic distortion is not an easy figure to determine, as there are a multitude of variables involved, and in particular the continuously

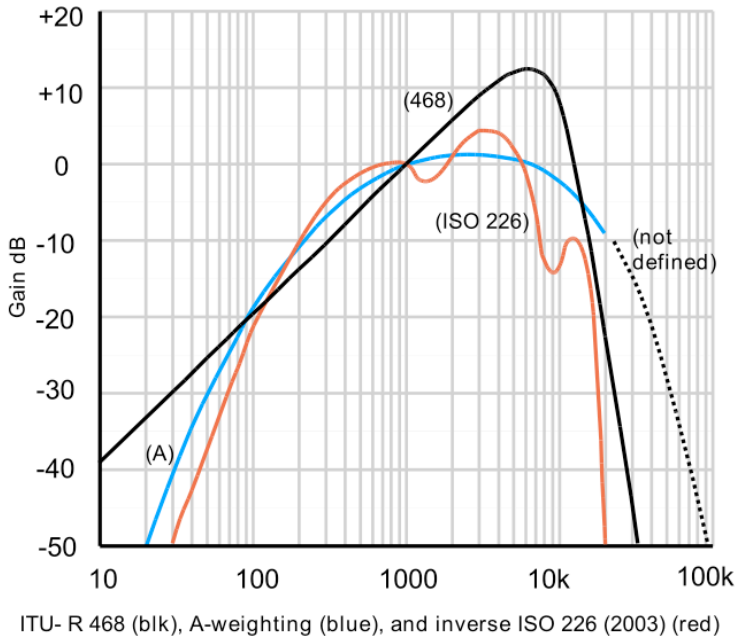

Figure 1.1: Weighting curves: ITU-R 468 in black, A-weighting in blue and inverse ISO 226 in red

varying level of signal means that the level of THD introduced is also dynamically changing; with mostly low-order harmonics present the just-detectable amount is about 1%, though crossover effects can be picked up at 0.3%, and probably lower; there is certainly no evidence that an amplifier producing 0.001% THD sounds any cleaner than one producing 0.005% [1];

- inter-channel crosstalk can obviously degrade stereo separation, but the effect is not detectable until it is worse than 20 dB, which would be a very bad amplifier indeed [1];
- phase and group delay have been an area of dispute for a long time, but a properly designed amplifier has its response roll-off points not too far outside the audio band, and these will have accompanying phase-shifts; there is no evidence that these are perceptible [1].

The picture of the ear that emerges from psychoacoustic and related fields is not that of a precision instrument. Its ultimate sensitivity, directional capabilities and dynamic range are far more impressive than its ability to measure small level changes or detect correlated low-level signals like distortion harmonics. This is unsurprising: from an evolutionary viewpoint the functions of the ear are to warn of approaching danger (sensitivity and direction-finding being paramount) and for speech. In speech perception the identification of formants (the bands of harmonics from vocal-chord pulse excitation, selectively emphasized by vocal-tract resonances) and vowel/consonant discriminations, are infinitely

more important than any hi-fi parameter. Presumably the whole existence of music as a source of pleasure is an accidental side-effect of our remarkable powers of speech perception: how it acts as a direct route to the emotions remains profoundly mysterious.

However, without a standardization of the various parameters that characterize an audio signal both in the physical and in the electrical behavior, no design activity would be possible. For this, in the course of the years, some standard scales and curves have been defined in order to take in account all together the hearing human limitations in the audio field. The most used is the A-weighting curve, belonging to a family of curves defined in the International Standard IEC 61672:2003 and various national standards relating to the measurement of sound pressure level [4]. This curve is today commonly used for the measurement of environmental noise and industrial noise, as well as when assessing potential hearing damage and other noise health effects at all sound levels and is characterized by an emphasis of frequencies around 3 – 6 kHz, where the human ear is most sensitive, while attenuating very high and very low frequencies to which the ear is insensitive. Figure 1.1 shows the A-weighting curve (blue) and other two very common weighting curves. In particular, the ITU-R 468 is commonly used in Europe.

1.1 Main characteristics of sound waves

Sound waves exist as variations of pressure in a medium such as air. They are created by the vibration of an object, which causes the air surrounding it to vibrate. When detected by the human ear, the vibrating air causes the eardrum to vibrate generating what is interpreted as sound. After an electronic acquisition, sounds can be mathematically represented as time-varying entities whose simplest form is the sine wave reported in Figure 1.2 and given by

$$V(t) = A \cdot \sin(2\pi f t) \tag{1.1}$$

characterized by an amplitude A, normally expressed in volt [V] and a frequency f measured in hertz [Hz]. From f, it is possible to obtain the period T, expressed in seconds [s]:

$$T = \frac{1}{f} \tag{1.2}$$

In Figure 1.2 the root mean square (rms) amplitude of the wave is reported. This is a very important parameter that comes in to play as soon as we consider the power associated to the signal. Actually rms amplitude, that considering a sine-wave can be expressed as

$$V_{rms} = \sqrt{\frac{1}{T}\int V(t)^2 dt} = \frac{A}{\sqrt{2}} \tag{1.3}$$

represent the DC voltage which would deliver the same average power to the same load as the sine-wave.

Of course a general audio signal is more complex than a simple sine-wave: first of all is not completely periodic and, second, it can contain more than one frequency. The

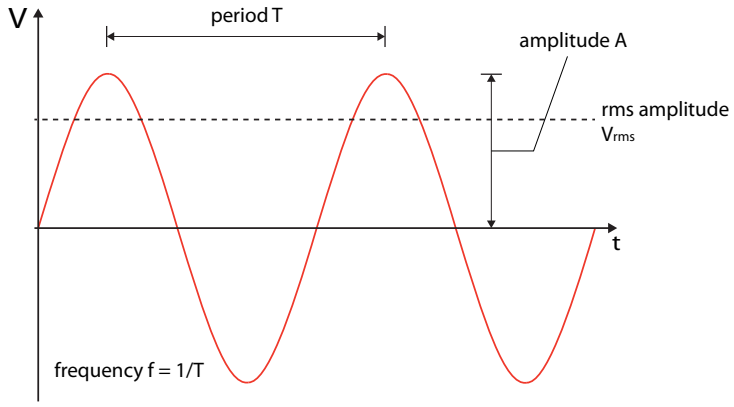

Figure 1.2: Sine-wave time behavior

two fundamental characterizing parameters are the *pitch* and the *timbre*. The pitch, in the musical field, is normally described as the position of a note in a musical scale: the higher is the pitch, the higher is the position of the note along the scale. In physical terms, instead, it represents the frequency of the fundamental harmonic of the sound that we are listening to. The timbre is used to describe the *quality* of the sound. Indeed, the sound of a trumpet is different from the sound of a clarinet for the same pitch. Physically the difference is related to the harmonic content and the envelope transients (*attack* and *decay*). Every sound is representable in the frequency domain using the Fourier transform that, giving the signal power distribution as a function of frequency, defines the signal spectrum $\hat{V}(\omega)$ as

$$\hat{V}(\omega) = \int V(t) \cdot e^{-j\omega t}\, dt \tag{1.4}$$

Time and spectral behavior of a generic audio signal are shown in Figure 1.3. Observing a signal like that, another important parameter called "crest factor" comes out. This parameter, also known as Peack-to-Average-Ratio (PAR), is defined as

$$PAR = 20 \log \left(\frac{V_{max}}{V_{rms}} \right) \tag{1.5}$$

where V_{max} is the amplitude of the maximum peak of the signal and V_{rms} is the amplitude defined by (1.3). The criticality introduced by the crest factor is that, due to the fast and large amplitude variations of a normal audio signal, any audio device has to deal with a very large range of signal amplitudes, implying a very large dynamic range.

Although in the normal use an audio amplifier deals with very complex signals, most of the tests performed to verify the performance of the system during the design are made using as input signal a simple sine-wave, in order to allow easier interpretation of the results. However, statistic standard tests, based on amplitude and frequency distribution of various normalized audio fragments, exist. These are used, in the final part of the design, to test the system under more general conditions [5].

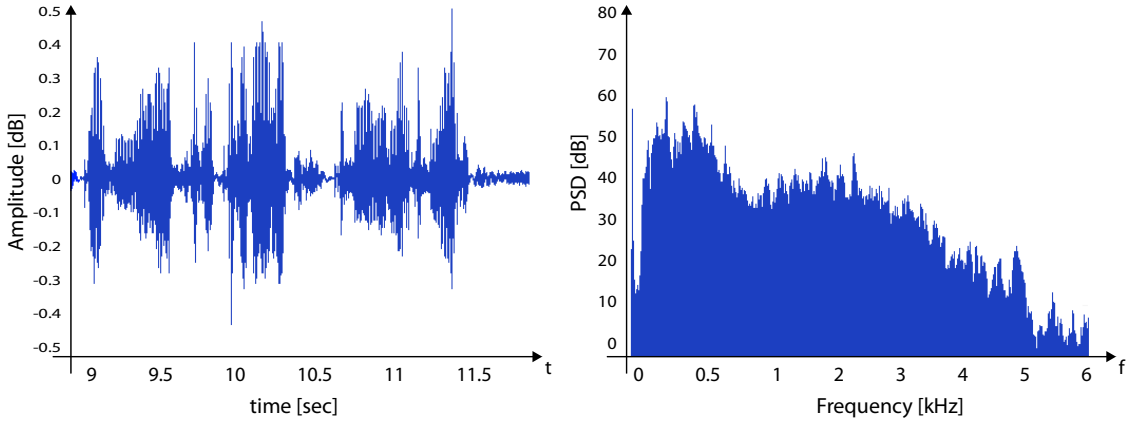

Figure 1.3: Generic audio signal: a – Time behavior, b – Spectral behavior

1.2 System requirements

Due to the popularity acquired by portable devices and the technological improvements of integrated circuits, power audio amplifiers have to deal on one side with high output power levels and linearity performance and on the other side with small area, high efficiency and cooling problems. In the following paragraphs will report the main critical aspects of an integrated audio system that will be taken in account during its design.

1.2.1 Output power and output stages

Essentially, an audio amplifier is a normal voltage amplifier optimized for the amplification of audio signals. If the first stage is normally critical in terms of noise performance, the output stage has to present the right characteristics to satisfy many critical aspects related to the load management.

The most important feature of the output stage is the output impedance (R_{out}). Considering that in audio systems the load is substantially the very low impedance of the speaker coil (4 – 16 Ω), the output stage impedance has to be extremely low as well (0.1 – 1 Ω) and the stage must be able to deal with a very large current level. Therefore, the output stage normally consists of very large transistors, even multiple stages in parallel, in order to obtain the lowest possible R_{out} and guarantee a correct thermal power dissipation that otherwise could damage the chip. However, large transistors involve the use of powerful output drivers that will affect the power consumption. Moreover, these large devices normally occupy most of the area of the chip and determine most of the amplifier cost.

Another important aspect about output power derives from the fact that it has to be increased very significantly to make the amplifier significantly louder [1]. We do not perceive acoustic power as such – there is no way we could possibly integrate the energy released in a room. Instead, we perceive pressure: the power radiated by a generic sound source results in a sound pressure (SP). The unit for SP is pascal (Pa), which is equal to

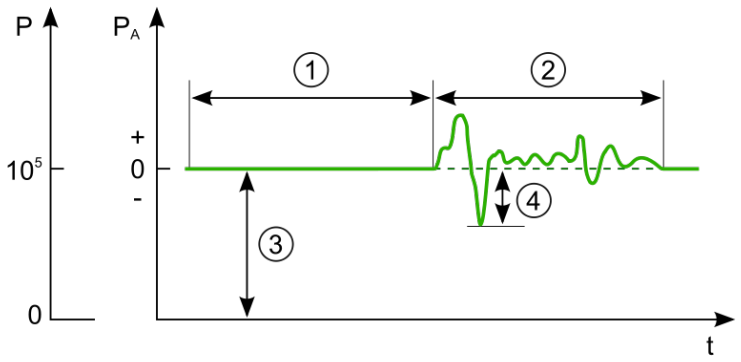

Figure 1.4: Sound pressure diagram: 1 – Silence, 2 – Audible sound, 3 – Atmospheric pressure, 4 – Instantaneous sound pressure

newton per square meter (N/m^2). However, what the ear perceives is the local pressure deviation from the ambient (average) pressure. For that, the sound pressure level (SPL) is normally defined as

$$L_p = 20 \log \left(\frac{P}{P_{ref}} \right) \tag{1.6}$$

in which P_{ref} is a reference value equal to 20 μPa. A pressure equal to the reference value is thus equal to 0 dB_{SPL} while 1 Pa equals 94 dB_{SPL}. The 0 dB_{SPL} value corresponds to the threshold of hearing at 1000 Hz for a young person with normal hearing ability. Figure 1.4 shows the sound pressure diagram for a generic audible sound. It is well known that power in watt must be quadrupled to double the sound pressure level, but this is not the same as doubling subjective loudness: some psychoacousticians have reported that doubling subjective loudness requires a 10-dB rather than 6-dB rise in SPL, implying that the amplifier power must be increased tenfold, rather than merely quadrupled [6].

Moreover, human ear has a very large dynamic range. To give an example: the ratio between the acoustic power of a rock concert and the sound of breathing can be as large as 10^{11}. Table 1.1 shows the sound pressure levels and the relative electrical power levels required to supply to a generic headphones systems (normally 32 Ω of impedance), in order to obtain the same loudness. As we can see, also excluding the first harmful high levels, the output power can involve a range including something like nine orders of magnitude (from 1 pW to 1 mW). For all these reasons, that imply quick variation of large load currents, it comes out that the output stage is one of the most critical blocks of an audio amplifier.

In order to take in account also the way in which the load current is provided to the load, and hence the linearity achieved, the output stage topology must be considered. In the first part of Chapter 2 an overview on the various existent output stages topologies is reported.

Source of sound in air	Sound pressure [Pa]	SPL [dB_{SPL}]	Power in Headphones [W]
Calculated Krakatoa explosion at 100 miles (160 km) in air	20000	180	–
Jet engine at 30 m	632	150	–
Hearing damage (ist.)	20	120	1
Jack hammer at 1 m	2	100	10 m
Traffic on a busy roadway at 10 m	$2 \cdot 10^{-1} - 6.32 \cdot 10^{-1}$	80 – 90	1 m
Hearing damage (over long-term exposure, not continuous)	0.356	85	0.3 m
Passenger car at 10 m	$2 \cdot 10^{-2} - 2 \cdot 10^{-1}$	60 – 80	30 µ
TV (set at home level) at 1 m	$2 \cdot 10^{-2}$	60	1 µ
Normal conversation at 1 m	$2 \cdot 10^{-3} - 2 \cdot 10^{-2}$	40 – 60	0.3 µ
Very calm room	$2 \cdot 10^{-4} - 6.32 \cdot 10^{-4}$	20 – 30	1 n
Auditory threshold at 1 kHz	$2 \cdot 10^{-5}$ (rms)	0	1 p

Table 1.1: Example of sound pressure level for different sources of sound and the equivalent power delivered to a 32-Ω headphones load with 90 dB/mW of sensitivity

1.2.2 Efficiency

In portable devices, power dissipation should be minimal both for achieving the longest possible battery life time and for minimizing heat generation that, as mentioned above, in the output stage could be so strong to destroy the device. Obviously, the less energy is lost during normal operation of a system, the better it is. The efficiency η of a generic system is defined as:

$$\eta = \frac{P_O}{P_{SUP}} = \frac{P_O}{P_O + P_{DISS}} \tag{1.7}$$

where P_O is the output power and P_{SUP} is the total power used by the system delivered by the supply source. In particular, we can specify more in details P_{SUP} as shown in (1.7), in which P_{DISS} includes all the power losses. The most critical issue in audio devices is that, besides the efficiency improvement due to the lower power supply levels needed by the new integration technologies, the output stage has to supply a fixed amount of power that depends on the application specifications. For this, in order to improve the efficiency of the whole device in which they are used, new architectural solutions that exploit in a different way the power stage, as Class-D or Class-G amplifiers, have been introduced.

Usually the efficiency is depicted as shown in Figure 1.5 as a function of the output power P_O. However, in these kind of plots, it is difficult to see how much the amplifier actually dissipates [7]. The dissipation of an amplifier in relation to the output power P_O and the efficiency η is:

$$P_{DISS} = P_O \left(\frac{1}{\eta} - 1 \right) \tag{1.8}$$

It not very easy to see that the amplifier on the right in Figure 1.5 dissipates 50% more than the one on the left at full power. In fact, since the efficiency is always zero at zero output power, the lower efficiency of the first case is not visible at all. A better representation of η is shown, for the previous two cases, in Figure 1.6. Here, thanks to the logarithmic x-axis that eliminates the case with $P_O = 0$ and emphasizes the efficiency values for low P_O level, it is easier to observe the correct η value for each operating point.

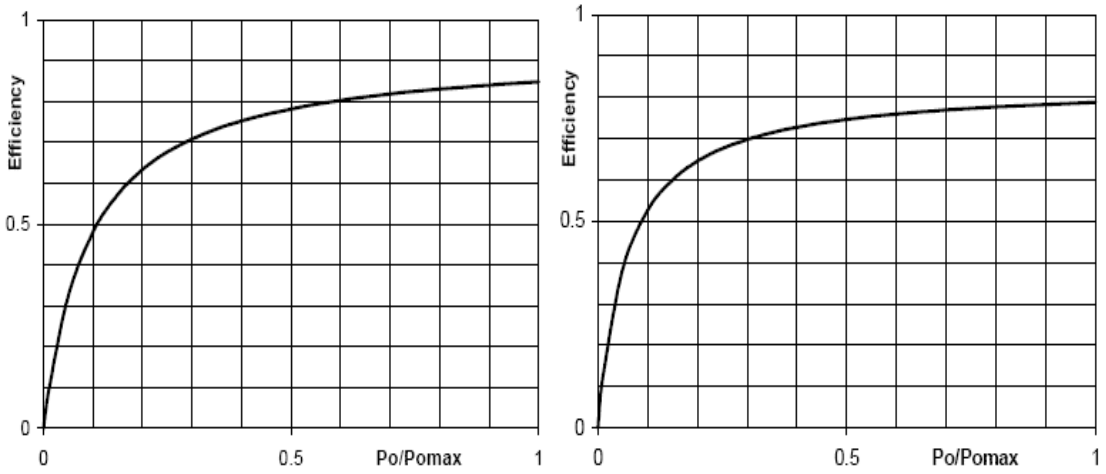

Figure 1.5: Simulated efficiency of two hypothetical audio amplifiers with different quiescent and maximum dissipations (linear scale)

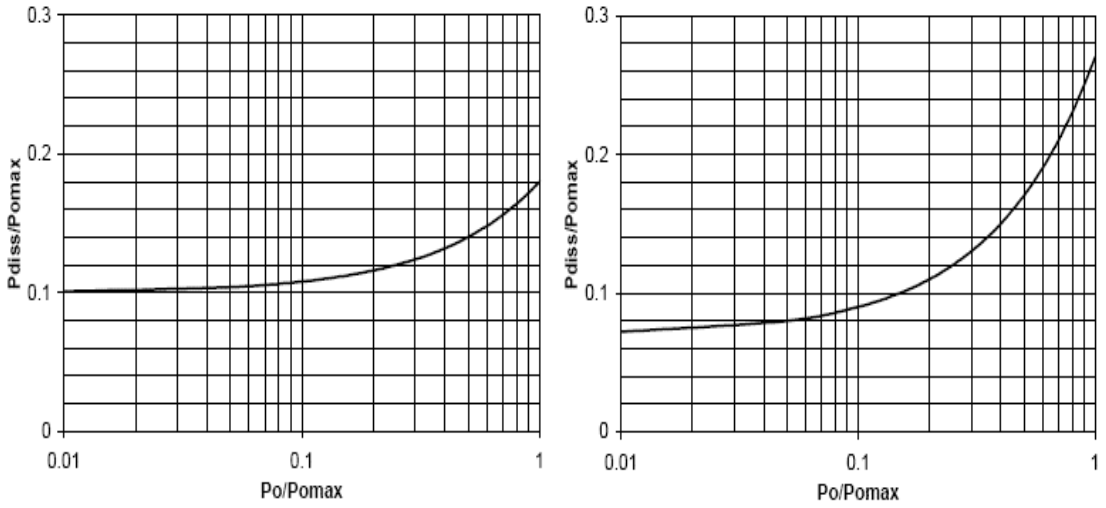

Figure 1.6: Simulated efficiency of two hypothetical audio amplifiers with different quiescent and maximum dissipations (logarithmic scale)

1.2.3 Distortion

Designing an audio system with very high efficiency could mean to have very low linearity. In most of today's application this aspect can not be tolerated. Therefore, parameters as Total Harmonic Distortion (THD) have become very important indexes to consider in the design phase.

Total harmonic distortion (THD)

When applying a sine-wave at the input of a non-linear amplifier, at the output we obtain an amplified sine-wave at the base frequency plus higher-order components with frequencies multiple of the base one. The THD is defined as:

$$THD = \frac{\sum_{n=2}^{\infty} P_n}{P_1} \tag{1.9}$$

where P_1 is the power of the fundamental harmonic having the frequency equal to the frequency of the input signal (base frequency) and $\sum_{n=2}^{\infty} P_n$ represents all the power lost in the higher-order harmonics. Considering also the noise floor of the system (P_{noise}), it is possible to define the THD+N as:

$$THD{+}N = \frac{\sum_{n=2}^{\infty} P_n + P_{noise}}{P_1} \tag{1.10}$$

Both indexes make sense only if calculated within an integration band that is usually equal to the operating band.

Intermodulation distortion (IMD)

When two sinusoids are summed and applied to a non-linear amplifier, the output contains tones at the base frequencies, at integer multiples of the base frequencies and at the difference between the base frequencies and their multiples. Two main standards exist. The first standard was defined by the SMPTE (Society of Motion Picture and Television Engineers). A 60-Hz tone and a 7-kHz tone in a 4:1 amplitude ratio are applied to the non-linear amplifier. The 60-Hz tone appears as sidebands of the 7-kHz tone. The Intermodulation Distortion (IMD) is the ratio between the power in the sidebands and the power of the 7-kHz tone. The second standard is defined by the CCITT (Comité Consultatif Internationale de Télégraphie et Téléphonie), and uses two tones of equal strength at 14 kHz and 15 kHz. This generates low frequency products and products around the two input frequencies, depending on the type (odd or even) of distortion.

Interface intermodulation distortion (IIMD)

In the Interface Intermodulation Distortion (IIMD) test, the second tone of an IMD measurement is not connected to the input, but to the output (in series with the load impedance) [7, 8].

Transient intermodulation distortion (TIMD)

In the Transient Intermodulation Distortion (TIMD) test, normally applied to a system with feedback, a sinusoid is added to a large square-wave and used as input signal. Due to the square-wave the input stage has to handle a large differential signal that probably pushes it in an operating region less linear than its quiescent operating point. The sine-wave, affected by this behavior, presents at the output the TIMD, also called transient distortion [9]. There are many ways of testing the TIMD and it remains unclear how much it adds to the existing measurement methods. If the maximum input signal frequency during normal operation of an amplifier is limited to 20 kHz, a 20 kHz full power sinusoid is the worst case situation. When that generates little distortion, TIMD will not occur [10].

Distortion summary

There is no consensus as to which distortion measurements are essential. Most of all, speaking about "sound" of an amplifier, because of subjectivism, it is not clear which distortion test is much close to the human perception of "good sound". With music, for instance, intermodulation effects are definitely more important than harmonics. However, THD tests have the unique advantage that visual inspection of the distortion residual gives an experienced observer a great deal of information about the root cause of the non-linearity and for that are the most used in both the design and the characterization of devices.

1.2.4 Power supply rejection ratio (PSRR)

Another important parameter in audio application is the Power Supply Rejection Ratio (PSRR). Due to the very high level of integration of microelectronic systems, electromagnetic coupling between power nets (very large metal paths) and any other signal present in the circuit is not so difficult. This can bring a lot of noise on the power supply and can affect the correct behavior of the system, for example, deteriorating the biasing levels, introducing undesired in band tones and intermodulations. The capability to be immune to these sources of noise and to limit the amount of these disturbances on the output signal is called PSRR and it is defined as

$$PSRR = \frac{\Delta V_{supply}}{\Delta V_{out}} \tag{1.11}$$

In particular, in mobile applications, a very strong specification is usually set about the level that the PSRR has to be (from -80 dB to -100 dB at 217 Hz). This specific frequency is actually due to the GSM standard electromagnetic coupling, that can induce noise as large as 600 mV.

1.2.5 Channel crosstalk

In stereo integrated amplifiers another important parameter is the channel crosstalk. This is a phenomenon by which a signal transmitted on one channel creates an undesired effect in the other channel of the stereo system [11]. In integrated circuit design, crosstalk normally refers to a signal affecting another nearby signal. Usually the coupling is capacitive and relative to the nearest neighbor, but other forms of coupling and effects on signals further away are sometimes important, especially in analog designs. For example a channel crosstalk could be conveyed through the integrated circuit substrate. There are a wide variety of possible fixes, with increased spacing, wire re-ordering, and shielding being the most common.

1.2.6 Noise

Considering that the dynamic range of an amplifier is given by the ratio, generally measured in dB, of its maximum undistorted output signal ($THD < 1\%$) to its noise floor, the noise level has to be maintained as low as possible without compromising other parameters. Today, high-performance audio amplifiers need a dynamic range up to 100 dB. Digital audio systems, such as CODEC or sigma-delta ($\Sigma\Delta$) modulators, face this increasing dynamic range by increasing their quantizer resolution. However, in analog devices things are different: once noise is added to a signal, it is essentially impossible to remove it without altering or degrading the original signal. Therefore, noise and interferences must be prevented along the entire signal path. Moreover, it is well known that the noise contributed by each stage of an amplifier decreases as the gain preceding the stage increases, implying that the first few stages in a cascade are the most critical [12]. Since the most common systems use feedback in order to stabilize the gain and to reduce distortion, the main noise sources will be the input and feedback resistors. Their value must be chosen as low as possible to maintain their thermal noise value under or at the same level of the amplifier noise floor.

1.2.7 Load impedance and filterless applications

The audio amplifiers load is substantially the impedance of the speaker they are bonded to. Two are the main parameters of the load to take in account during an amplifier design: the sensitivity, defined as the the speaker efficiency in dB_{SPL} per milliwatt of input signal power, and the load impedance. This last, especially in headphones applications, can vary in a wide range because of the possibility given to each user to use the amplifier with any kind of headphones. Different load impedance means different phase margin and loop gain, that bring the design of the headphones amplifiers stability to be pretty hard [5].

Filterless applications

The most common speaker structure consists of a voice coil rigidly connected to a diaphragm. The whole moving system has a certain mass and compliance that can be as-

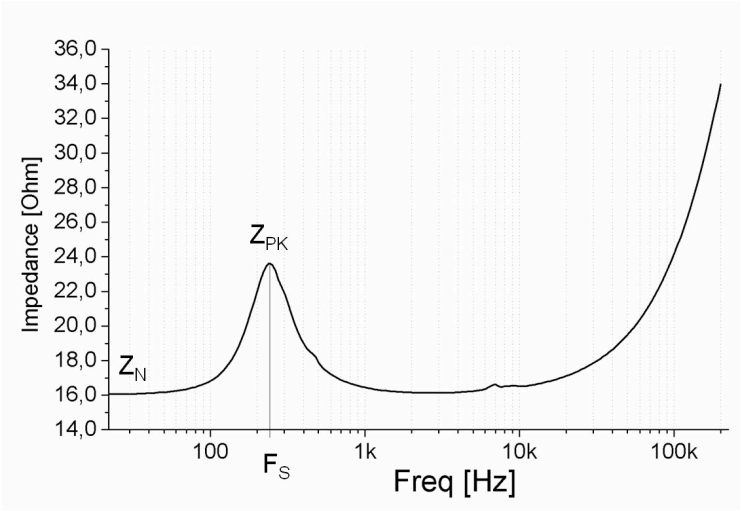

Figure 1.7: Module of the electrical impedance of a general speaker versus frequency

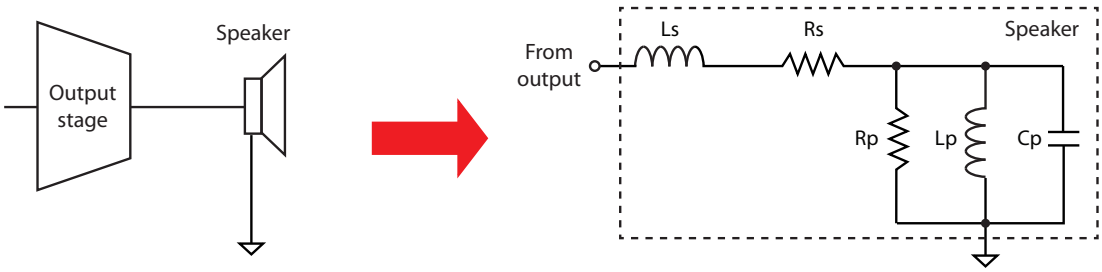

Figure 1.8: Model of a general speaker

sociated to a simple mass-spring-damper system with the relative resonance frequency, at which the impedance value shows its maximum, as shown in Figure 1.7. A simple electrical model of a general speaker is reported in Figure 1.8, where R_S and L_S include also the distributed resistances and inductances due to the connection from the amplifier output to the speaker: the interesting thing is that the net acts as a high-order low-pass filter. This property plays a fundamental role in switched applications, such as Class-D amplifiers. As it will explained in Chapter 2, in order to maximize the efficiency, this kind of structure takes advantage of a pulse-width modulation that, on the other side, can give some electromagnetic interference problems due to the high frequency carrier harmonics introduced on the output signal. Normally, this drawback is overcome by an output filter that, however, due to the low required cutoff frequency (about 30 kHz), it is generally bulky. It will be shown that particular modulations and structures can work properly without the external filter, using the intrinsic low-pass action of the speaker, saving area and making devices cheaper.

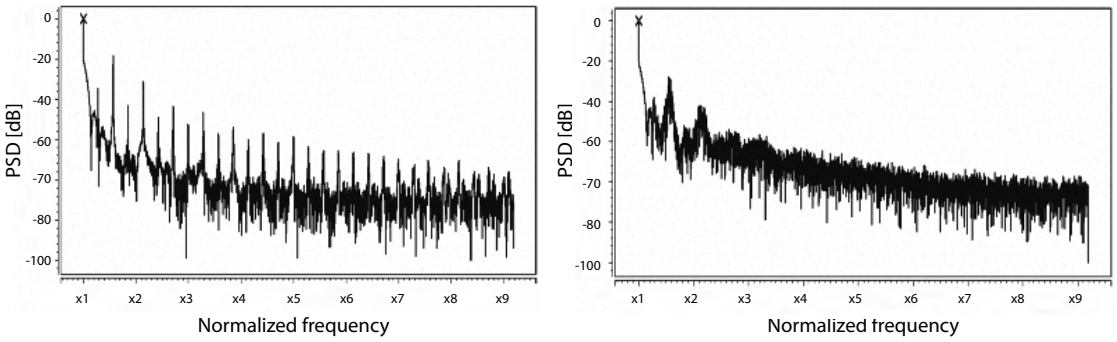

Figure 1.9: Example of a general Class-D spectrum at high frequencies: a – Without EMI control system, b – With EMI control system

1.2.8 Electromagnetic interference (EMI)

As briefly explained above, switched systems like Class-D amplifiers use an high-frequency carrier in order to modulate the audio signal and improve efficiency. Therefore, the output signal, besides the amplified audio information, contains also high-frequency components that, due to the relatively long connections from the output to the load, can produce electromagnetic emissions that can compromise the correct operation of other nearby devices. In order to avoid these problems, severe specifications have to be respected in the design of switching amplifiers and a lot of research has been done to limit as much as possible electromagnetic interference (EMI) problems and make the products marketable. Figure 1.9 shows an example of the output spectrum of a Class-D amplifier before and after the EMI limitation.

1.3 Conclusions

In this chapter we have seen all the main characteristics and specifications that an audio system has to satisfy in order to be marketable. Particular care has to be taken in the design of the output stage which, dealing with the highest power levels of the system, is the most delicate block of the amplifier. THD and dynamic range, although related to the output signal, are normally satisfied with a proper design of the first stage and the output drivers.

Chapter 2

Output stages, modeling and synthesis

After reviewing in Chapter 1 the general characteristics of audio amplifiers, in Chapter 2 we will show a comparison of all existing amplifier output stage classes with their operating principle and main proprieties. Particular attention will be dedicated to Class-D amplifiers, explaining in detail every critical point that needs to be taken into account during the design. Finally, we will introduce the modeling techniques for this kind of amplifiers and a new design methodology that can help the Class-D amplifier design.

2.1 Amplifier architectures

The vast majority of audio amplifiers use the conventional architecture shown in Figure 2.1. There are three stages: the first one being a transconductance stage (differential voltage input, current output), the second a transimpedance stage (current input, voltage output) and the third a unity-voltage-gain output stage. The first stage provides the needed SNR, the second stage has to provide all the voltage gain and the third one is used to ensure a sufficiently low output impedance in order to drive the load. Depending both on the topology of the third stage and on how it delivers the power to the load, it is possible to draw a classification of power amplifiers: each category is called Class and features different characteristics, especially in terms of THD and efficiency. For a long time the only amplifier classes relevant to high-quality audio were Class-A and Class-AB, due to the low distortion that they can achieve. However, due to recent market requests, also other amplifier classes have become popular and are now commercially exploited [13].

2.1.1 Class-A amplifier

Amplifying devices operating in Class-A are conducting over the whole input signal period. As shown in Figure 2.3, the input signal is applied to the gate of transistor $M1$ that is biased by the current source I_0. At the output node V_0 we obtain as output signal an inverted and scaled replica of the input signal (Figure 2.2a). Even in the absence of input signal, current I_0 is always absorbed by the supply voltage V_A, producing a fixed and

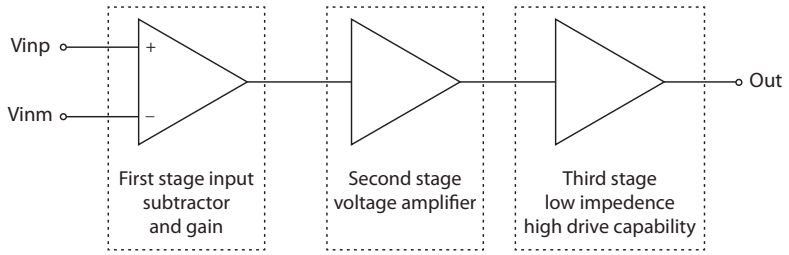

Figure 2.1: A general three-stage amplifier structure

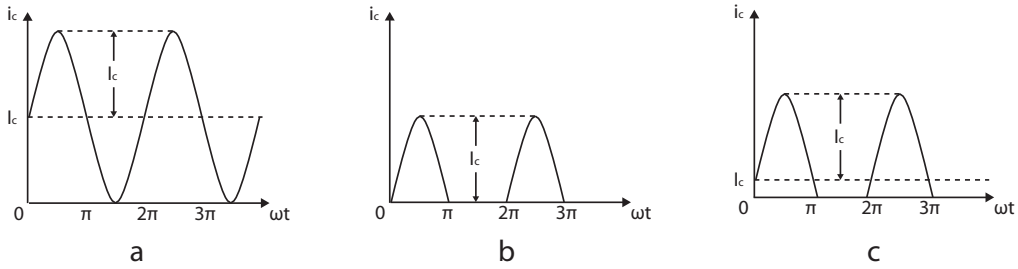

Figure 2.2: Bias current of transistor operating in: a – Class-A, b – Class-B, c – Class-AB amplifier stages

significant power loss. Considering a sinusoidal input signal (1.1) we can calculate the maximum theoretical efficiency of this kind of structure using (1.7).

Defining the load power as

$$P_L = R \cdot {I_{Leff}}^2 = R \cdot \frac{{V_0}^2}{(2 \cdot R^2)} = \frac{{V_0}^2}{2 \cdot R} \tag{2.1}$$

and the power delivered by the supply as

$$P_A = 2 \cdot \frac{{V_A}^2}{R} \tag{2.2}$$

the efficiency becomes

$$\eta = \frac{P_L}{P_A} = 0.25 \cdot \frac{V_0^2}{V_A} \rightarrow \eta_{max} = 25\% \tag{2.3}$$

As it can be seen the theoretical efficiency is very poor and, therefore, the use of Class-A amplifiers can be tolerated only in cases where neither power consumption nor thermal dissipation are a problem. Nevertheless, this class of amplifiers features a very high linearity and it is easy to design due to the small number of components, thus making this configuration very popular in many non portable applications.

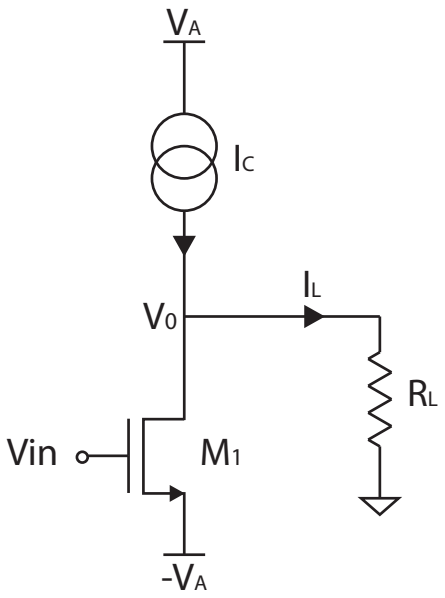

Figure 2.3: General Class-A amplifier

2.1.2 Class-B amplifier

The general schematic of a Class-B amplifier is reported in Figure 2.4. In this case no fixed bias current exist and the load current I_L is supplied by $M1$ or $M2$ for negative or positive signals, respectively. Figure 2.2b shows the drain current of $M2$ with a sinusoidal input signal.

The main characteristic of this configuration is that with zero input signal both power transistors are off and no current flows through the output branch. Therefore, considering also in this case a sinusoidal input signal, the efficiency of this structure is given by

$$\eta = \frac{P_L}{P_A} = \frac{\pi}{4} \cdot \frac{V_0}{V_A} = 0.785 \cdot \frac{V_0}{V_A} \rightarrow \eta_{max} = 78.5\% \tag{2.4}$$

The theoretical efficiency is much larger than in Class-A amplifiers, but it is still not sufficient for the targets set for the most recent devices on the market, that normally require $\eta \approx 90\%$. Moreover, due to the on/off behavior of the transistors, a large crossover distortion appears: for small signals both transistors are off, or in a non linear region, and the output does not follow the input anymore, presenting a large in band harmonic content. For this reason Class-B amplifiers are not suitable for audio applications.

2.1.3 Class-AB amplifier

The Class-B amplifier crossover distortion is solved with the Class-AB architecture (Figure 2.5). Here two "batteries" connected to the gates of $M1$ and $M2$ maintain both tran-

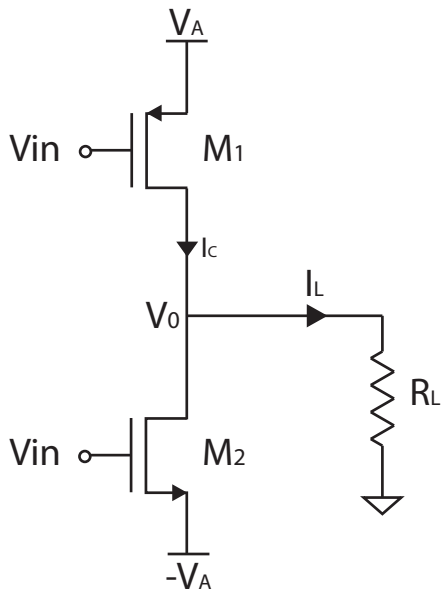

Figure 2.4: General Class-B schematic

sistors on also for small input signals, thus improving the linearity almost as in the large signal case.

As suggested by the name, the behavior and hence the efficiency of this configuration is a trade-off between Class-A and Class-B, depending on the output signal level. Figure 2.6 shows a comparison between the three classes considered so far. Looking at the Class-AB efficiency curve, it is possible to note that, for small signals, the quiescent bias current is comparable with the signal itself and the efficiency is similar as with a Class-A amplifier, while at higher signal level η tends toward the Class-B curve.

Thanks to the technological improvements and in order to get even better performance, other classes of power stages are being introduced in audio applications. Among these new configurations, the most relevant are Class-G and Class-D amplifiers, in which, at the expense of higher complexity, larger efficiency and linearity performance can be obtained, reaching values that could never be reached using conventional amplifier classes.

2.1.4 Class-G amplifier

A Class-G device is a high-efficiency analog amplifier, fundamentally based on a Class-AB structure, but working with two different levels of supply voltage. This structure takes advantage of the fact that musical and voice signals have a high crest factor (1.4), with most of the signal content at lower amplitudes. In practice, the system switches from one supply voltage to the other, according to the instantaneous output voltage level, obtaining a great reduction of power dissipation for most of the typical musical or voice sources.

The core of a Class-G amplifier is the switching circuitry that has to enable a smooth

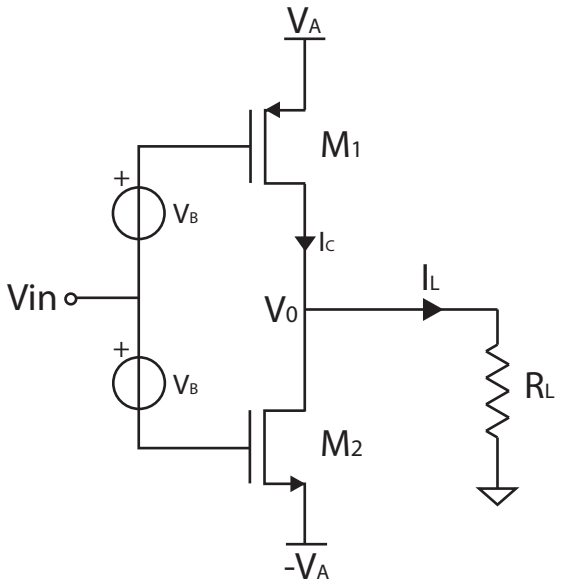

Figure 2.5: General Class-AB schematic

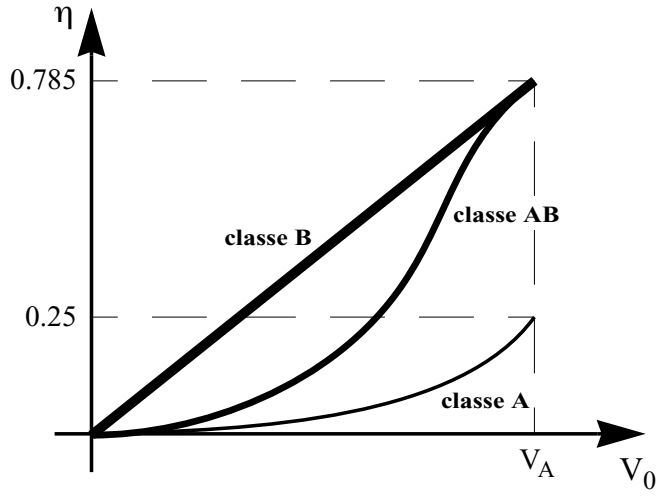

Figure 2.6: Comparison between theoretical efficiency curves

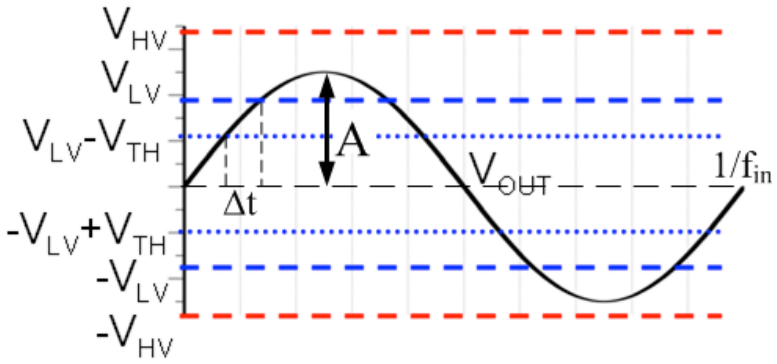

Figure 2.7: Output voltage versus time: supply voltage rails and switching point levels

handover of the load driving during the teansition from the lower supply to the higher one and viceversa. As shown in Figure 2.7, it is possible to define two switching point levels called $V_{LV} - V_{TH}$ and $-V_{LV} + V_{TH}$, where V_{LV} is the value of the amplifier low voltage supply and V_{TH} is a threshold voltage [5].

Figure 2.8 reports two possible solutions for realizing a Class-G topology: the *series* implementation (shown in Figure 2.8a) and the *parallel* implementation (shown in Figure 2.8b). Thanks to its simpler switching circuit, the series solution is the most common. In this case, when the output voltage lays between the two thresholds ($-V_{LV}+V_{TH} < V_{in} < V_{LV} - V_{TH}$), the switches are open and the amplifier is connected only to the low voltage supply through the diodes. When the output voltage exceeds the switching points, the switches are closed and the push-pull output stage is supplied by the high voltage rails. The diodes, that are used only to prevent current from flowing between the high and low voltage supply rails, represent the main limitation of this topology: the threshold voltage of the diodes strongly limits both the minimum value of V_{LV} and the switching point distance from V_{LV}, thus making this implementation unsuitable for low voltage applications. On the other hand, in the parallel topology, there are two output stages working in parallel and there is nothing between the power transistors and the supplies. This fact, although leading to more area consumption, poses no constraints on the minimum value of V_{LV} and allows placing the switching point very close to V_{LV}, thus achieving higher efficiency.

An example of Class-G output voltage behavior in the time domain is reported in Figure 2.9. It is possible to note how, with a high-crest-factor signal, the efficiency of the system is improved with respect to a Class-AB amplifier. Considering a rail-to-rail output sine-wave as input signal and defining the conduction angle α during which the load current is supplied by the low supply voltage as

$$\alpha = \arcsin\left(\frac{V_{LV} - V_{TH}}{A}\right) \tag{2.5}$$

where A is the peak amplitude of the sinusoid, it is possible to describe the efficiency η in

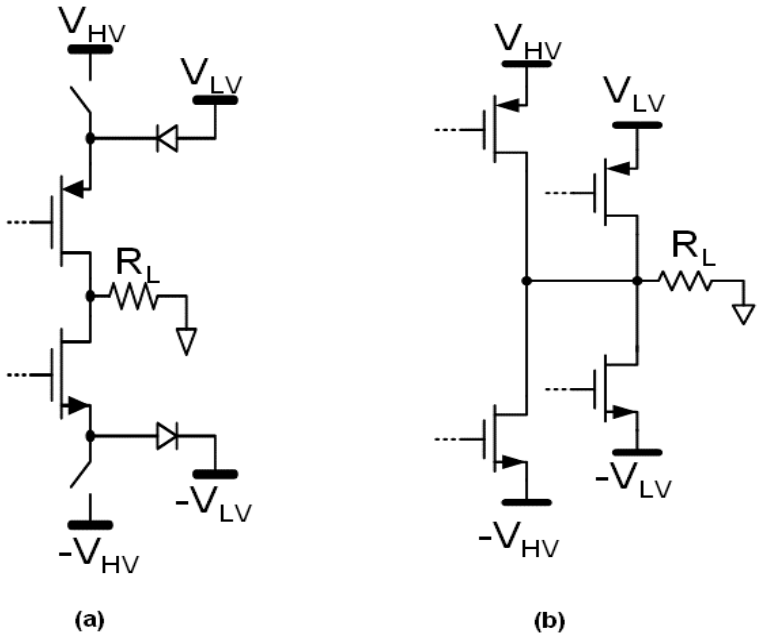

Figure 2.8: Class G topologies: a – Serial and b – Parallel

terms of the output power P_0 as

$$\eta = \frac{\pi \cdot \sqrt{2P_0R_L}}{4V_{LV}(1-\cos\alpha) + 4V_{HV}\cos\alpha} \tag{2.6}$$

where V_{HV} and V_{LV} are the voltage levels defined in Figure 2.7 and R_L is the load resistance.

As shown in Figure 2.10a, comparing the efficiency of Class-G and Class-AB amplifier, it is possible to note that η for a Class-G structure grows rapidly for low signals but falls down, tending to the Class-AB efficiency values, as soon as the output signal exceeds the threshold value and the higher supply voltage is used.

In practice, using a Class-G configuration instead of a Class-AB structure supplied with the Class-G highest supply voltage, the theoretical maximum advantage in terms of efficiency is given by the ratio between the high and low supply voltages. This value decreases every time the output signal exceeds the threshold value.

However, Class-G structures present also some critical drawbacks. First of all the worsening of the linearity, that in this case depends heavily on the switching point choice and on the input signal morphology. A second disadvantage of Class-G amplifiers is that they need two voltage supply rails. In most cases, it is necessary to generate those additional supply voltages and, for this purpose, buck converters and inverting charge pumps are normally used to generate the positive low voltage supply starting from the high voltage supply and the negative low voltage supply, respectively. This aspect and the modest

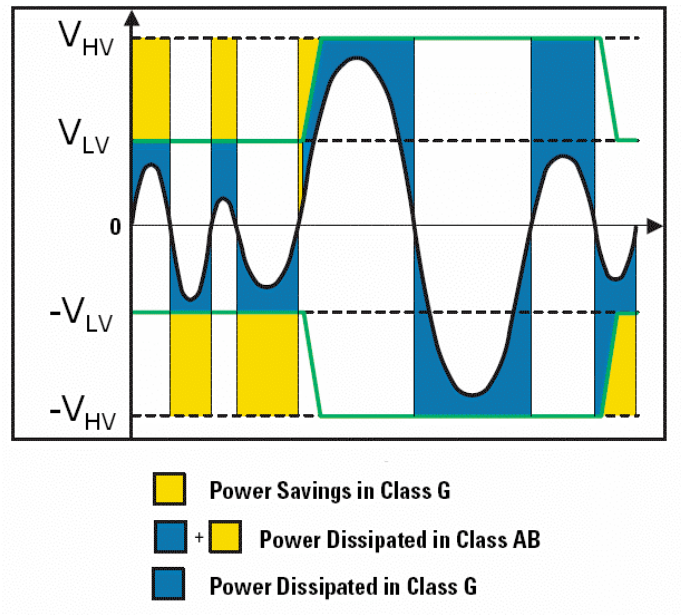

Figure 2.9: Intuitive view of the Class-G efficiency improvement with music as input signal

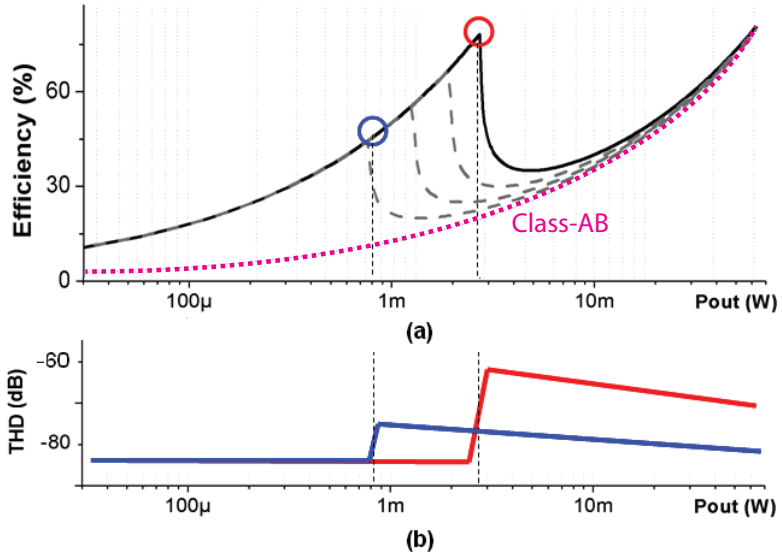

Figure 2.10: Class-G amplifier: a – Efficiency, b – THD versus output power at different switching point level

Figure 2.11: Block diagram of a basic switching amplifier

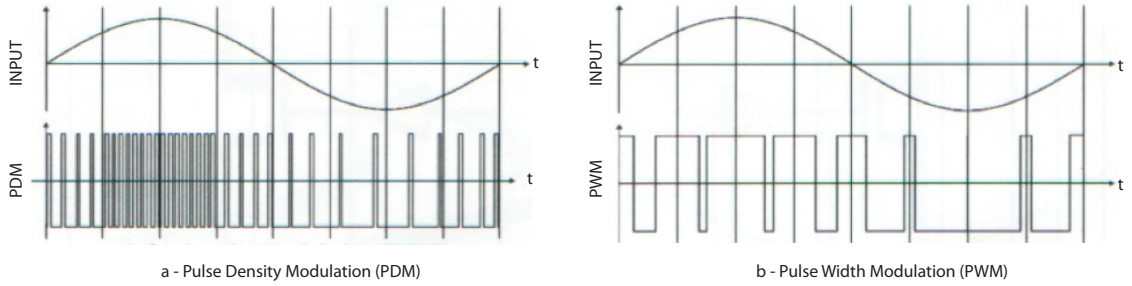

Figure 2.12: Pulse modulations examples: a – PDM, b – PWM

improvement of efficiency restrict the use of Class-G amplifiers to few applications.

2.1.5 Class-D amplifier

The simplest structure of a Class-D amplifier is illustrated in Figure 2.11. If in Class-G structures, the key role is played by the power supply switching circuitry, the core of a Class-D amplifier is the pulse code modulator, which transforms the input signal in a rail-to-rail switching square-wave that can drive in a very efficient way the output power stage. An output filter is then inserted in order to demodulate the amplified signal and filter out all the high frequency spurs introduced by the modulation. Hereafter, the main Class-D characteristics will be reported in order to create a well defined model to use during the design.

Pulse code modulations

Pulse code modulation is the key feature of a Class-D system. Two are the main existing pulse code modulations: the Pulse Density Modulation (PDM) and the Pulse Width Modulation (PWM). For both modulations the output signal consist of trains of pulses with variable density (PDM, Figure 2.12a) or width (PWM, Figure 2.12b) in the time domain, respectively. In a Class-D system, the output stage is directly driven by the modulated signal. With PDM, especially for large input signal amplitudes, the output transistors are switched on and off quite often, thus introducing significant switching losses. Moreover, PDM requires a more complex modulator implementation with respect to PWM, which normally requires just a comparator. For these reasons Class-D amplifiers normally use PWM modulation, which can be implemented in two main versions.

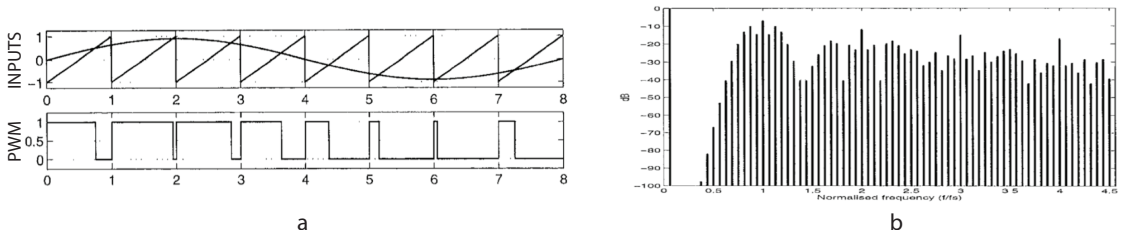

Figure 2.13: Natural sampling implementation: a – Time behavior, b – Frequency behavior

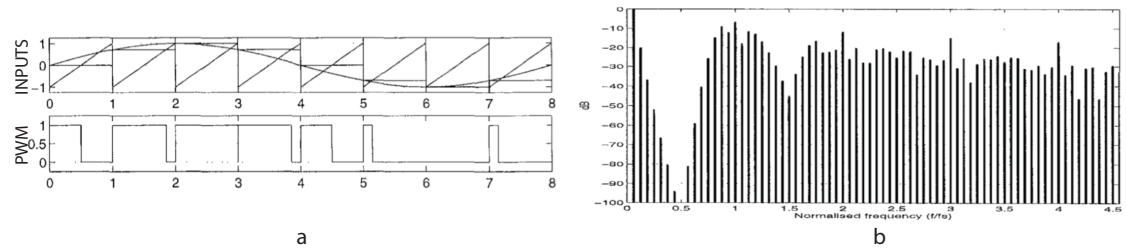

Figure 2.14: Uniform sampling implementation: a – Time behavior, b – Frequency behavior

The first version is called Natural Sampling (NS) and is obtained from the comparison between the modulating signal and a periodical carrier, that usually is a triangular or sawtooth wave. Figure 2.13a shows an example of NS signal behavior: due to the absence of any form of sampling, this modulation is completely analog and features an ideally null distortion, as can be seen in Figure 2.13b. The second version is called Uniform Sampling (US) and it is represented in Figure 2.14a. In this case a sample-and-hold circuit is inserted in front of the comparator in order compare the carrier with a fixed input value. This kind of modulation introduces many in band harmonics due to the sampling (Figure 2.14b), but is often used in mixed analog-digital systems, where a very good interface between digital part (input) and analog part (power output) is needed. In these cases PWM with US does not worsen the system linearity performance, since the digital input signals are already sampled, while the performance mainly depends on quantization and sampling frequency. Moreover, many interpolating techniques have been developed in order to achieve reasonable THD performance in these cases [14].

Power bridge types and filterless applications

The output stage of a Class-D amplifier can be composed of one or two output branches. In the first case (Figure 2.15a), called half-bridge, the load is connected in a Single-Ended (SE) way to the amplifier. The main advantages of this structure are the jack compatibility (the two stereo channels can share the ground contact) and the use of only two transistors,

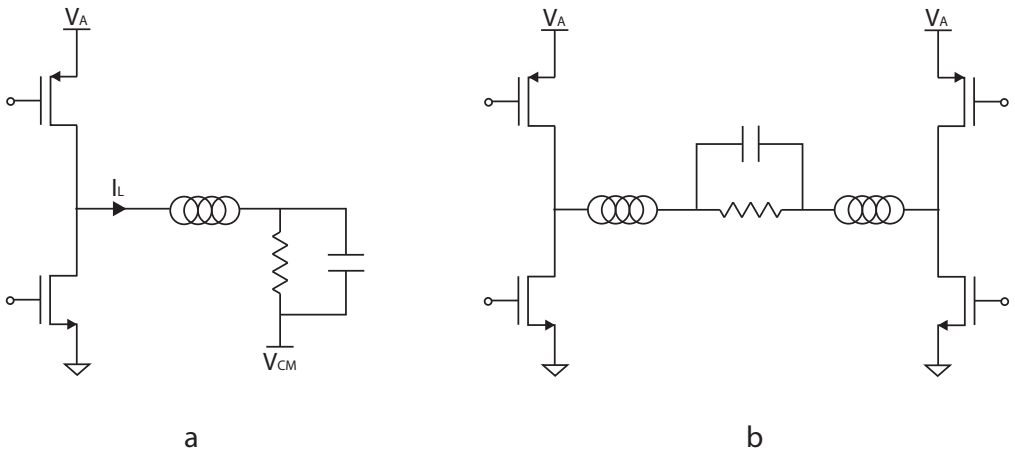

Figure 2.15: Possible output power stage architectures: a – Half-bridge, b – Full-bridge (BTL)

that makes it a cheap solution in terms of area. The solution with two branches is shown in Figure 2.15b and is called full-bridge or BTL (Bridge Tied Load) configuration. This is a Fully-Differential (FD) structure and, also if it needs twice the number of transistors, it is the most popular solution. In fact, working in a fully-differential way, all the common mode signals are canceled, increasing the Power Supply Rejection Ratio (PSRR), and all the even harmonics, carrier included, are suppressed, making easier the output filtering operation. Moreover, this structure doubles the output swing, delivering a maximum output power four times larger with respect to SE solutions for the same power supply voltage.

Another important aspect that arises when using the BTL configuration is the possibility to improve efficiency at the modulation algorithm level. In fact, due to the SE nature, half-bridge structures can deal only with the two-level PWM. By contrast, with the full-bridge power stage, the phase of the carrier for either bridge branch can be chosen independently and both two-level and three-level PWM modulations are allowed. Figure 2.16a shows how, modulating the same signal in counter phase with the same carrier, a three-level PWM signal can be generated. The name of this kind of modulation arises from the resulting signal on the load: each branch switches from 0 to $+V_{DD}$, leading, due to the subtraction due to the differential connection, to a signal that switches between $+V_{DD}$, $-V_{DD}$ and 0, where 0 is ground and V_{DD} is the supply voltage. Actually, $-V_{DD}$ is not a real negative supply voltage, it is simply obtained by the differential subtraction: this represents one of the advantages of Class-D amplifiers with respect to Class-G structures, which instead have to use charge pumps to create negative supply voltages.

The main property of the three-level PWM modulation is the effective doubling of the carrier frequency (Figure 2.16c) and, hence, the possibility to push at higher frequency the spur components present in the output signal due to the modulation. This behavior

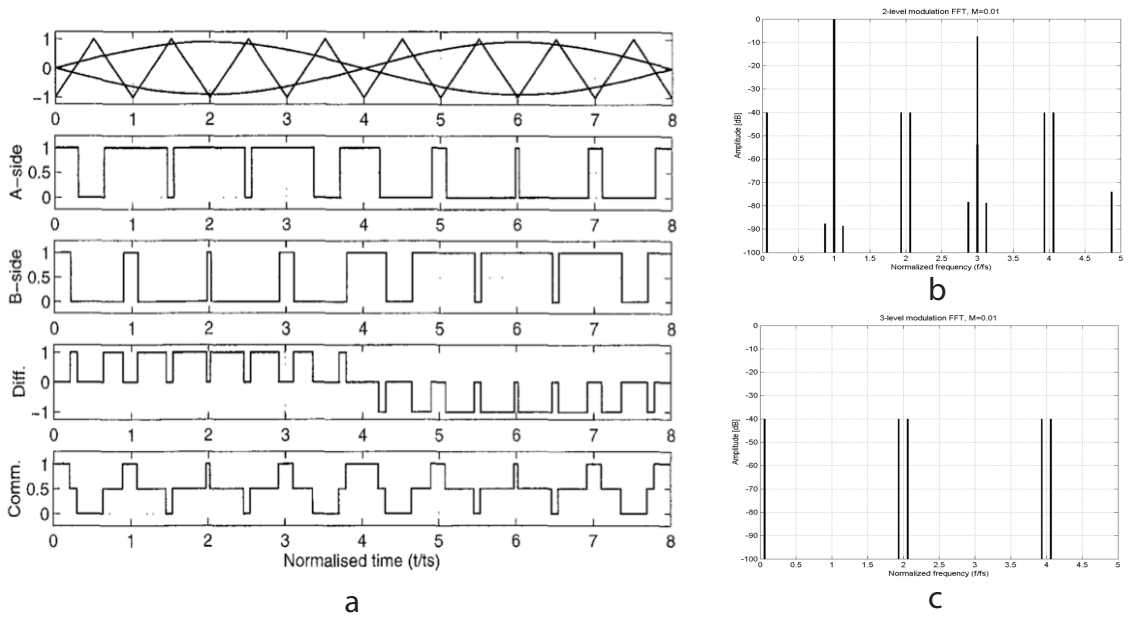

Figure 2.16: Three level PWM: a – Signals behavior, b – Two-level PWM spectrum, c – Three-level PWM spectrum

allows us to directly exploit the filtering action of the speaker, instead of introducing a dedicated output filter after the power stage, thus saving area and achieving the so called filterless configuration, which is a must for portable devices.

Efficiency

Theoretically, due to the switching behavior of Class-D amplifiers, no power stage bias current is needed. All the power drained from the supply is delivered without losses to the load, leading ideally to 100% efficiency. In the real world, however, there are anyway sources of power loss.

First of all the on-resistances of the bridge power transistors, typically in a range from 10 mΩ to 1 Ω, dissipate energy (losses due to Joule effect, P_j), especially with large output signal levels. This is also the main heat source of the amplifier that, if not well handled, can destroy the device. Therefore, especially in solid-state systems, the power bridge is implemented using very large transistors, while control and cooling systems are normally used to monitor and stabilize the chip temperature.

Another important aspect are the switching losses (P_{sw}) that occur any time the PWM output signal changes polarity. These losses depend mainly on two factors:

- parasitic capacitors;
- cross-conduction.

During each commutation, indeed, all the parasitic capacitors of the output stage have to be charged or discharged, respectively, depending if the power transistors have to be

switched on and off. Moreover, for each commutation there is an time interval in which both transistors of the same branch are concurrently on. This creates, also if for a short time, a direct path from the power supply to ground (cross-conduction), that can causes large current spikes, which degrade the efficiency.

The efficiency for a Class-D amplifier is given by:

$$\eta = \frac{P_{audio}}{P_{audio} + P_q + P_j + P_{sw} + P_{harm}} \tag{2.7}$$

Besides P_{sw} and P_j defined above, other two loss terms are present in (2.7): P_q, which represents the quiescent power dissipated by all the circuitry within the Class-D system (active filters, drivers, controls) and P_{harm}, which instead takes in account the power of the high frequency harmonics that, from the sound point of view, represent lost power, since they cannot be perceived by the human ear. However, this last term affects only the acoustic efficiency and has not to be taken in account to calculate electrical efficiency. Indeed, the electrical power on the load is $P_L = P_{audio} + P_{harm}$ and the electrical efficiency is:

$$\eta = \frac{P_L}{P_L + P_q + P_j + P_{sw}} = \frac{P_{audio} + P_{harm}}{P_{audio} + P_q + P_j + P_{sw} + P_{harm}} \tag{2.8}$$

Usual Class-D amplifier efficiency values range from 80% to 90%, depending on the technology and on the design.

Linearity

As mentioned in Chapter 1, THD is the most important index for high audio quality design. In Class-D amplifiers many are the sources of distortion and, unlike the other linear amplifier classes, they involve both non-linear transfer functions and timing errors components. As a matter of fact, after the PWM modulator the input signal information is transferred from the voltage domain to the time domain (pulse width), where, unfortunately, it can be easily affected (distorted) by uncorrelated delays introduced by the different system blocks. The main contribution in this sense is introduced by the so called "dead-time" control. Such control is introduced to overcome the cross-conduction problem: basically a suitable digital logic within the Class-D amplifier output drivers, ensures that each transistor of a branch is turned on only when the other if completely off, as illustrated in Figure 2.17.

In practice, during a certain time interval (the dead-time), both transistors of the output branch are off thus preventing cross-conduction. However, although the dead-time introduction improves significantly the efficiency, it also worsens the linearity because, changing the PWM timing, it affects the input signal information. For this reason, a trade-off between efficiency and THD has always to be considered during the design of the dead-time control circuit.

Another very important aspect, always related to the PWM timing, is the carrier linearity. As shown in Figure 2.18, the use of a non linear carrier introduces time errors on each

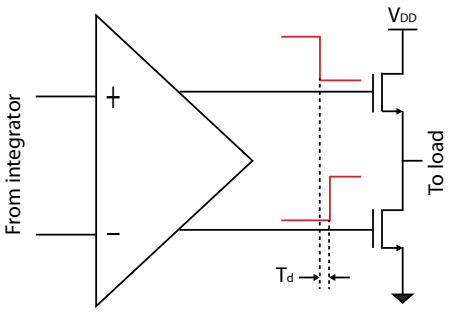

Figure 2.17: Dead-time control in power bridge driver signals

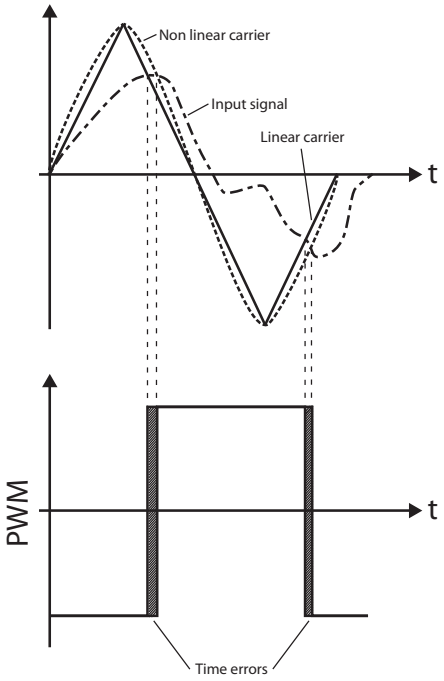

Figure 2.18: Time errors due to carrier non-linearity

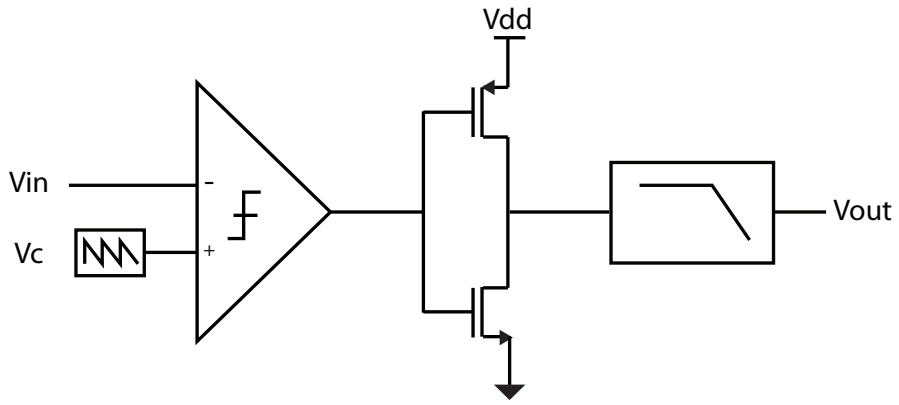

Figure 2.19: Single-ended open-loop Class-D amplifier implementation

switching edge, with respect to the linear case, thus producing distortion contributions observable as in-band harmonics after the demodulation.

Other non-linearity contributions are due to asymmetries in rise/fall time of the power transistor driving signals, hysteresis behavior, delays of the PWM comparators, non-idealities in the bridge drivers (e. g. saturation), and mismatches among the power bridge transistors.

Open-loop and closed-loop structures

A simple example of a Class-D amplifier is shown in Figure 2.19. This structure is very easy to implement, features high input impedance and, being delay independent, is intrinsically stable. However, considering the required high-quality in audio systems, this open-loop solution has several practical drawbacks, which limit its application. First of all, the overall gain depends on the supply voltage which has to be accurate and, secondly, the half-bridge (or the full-bridge in the differential configuration) is directly connected to the power supply. Therefore, any noise or disturbance on the power rails is transferred to the load, leading to a degradation of the PSRR. Furthermore, every non ideality introduced by modulator, drivers or output stage pass undisturbed through the chain, affecting the quality of the output signal.

To overcome these limitations, most class-D amplifiers are used in a closed-loop configuration [15]. A simple example is shown in Figure 2.20. Due to the closed-loop operation with a large loop gain, all the non-idealities occurring after the first integrator (like distortion, and PSRR) are referred to the input divided by the integrator gain in the signal band and their importance is then strongly reduced. Moreover, the overall (closed-loop) gain is well determined by the resistor ratio ($A \cdot R_{in}/R_{in}$).

Being a very non-linear system, also closing the loop, the achievable THD values are not very impressive ($THD \approx 65-70$ dB) and, hence, for a long time Class-D systems have been used in low-end applications only. Recently, a lot of research has been performed

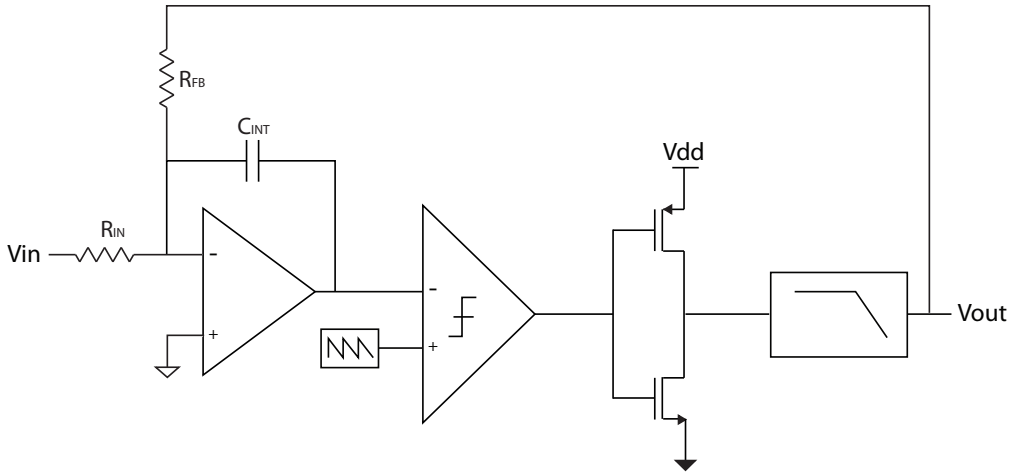

Figure 2.20: Single-ended closed-loop Class-D amplifier implementation

in order to find new solutions able to achieve the usual Class-D high efficiency together with a linearity suitable for Hi-Fi applications. Many solutions have been tried in order to improve performance [16–18], but among all these attempts the best solution seems to be the loop order increasing [19,20]. In fact, the higher is the order of the loop, the higher are the loop-gain and the non-ideality attenuation. However, increasing the order of the loop increases also circuit complexity and introduces critical stability issues. Therefore, a very well defined design methodology is needed for designing Class-D amplifiers with loop order higher than two and, as usual, depending on the specifications, a trade-off between order, circuit complexity and achievable linearity has to be considered.

2.2 Modeling and synthesis of Class-D amplifiers

Modeling and synthesis of Class-D amplifiers are important aspects in the design of such systems. It is therefore important to introduce at this stage a few concepts that have been widely used during the design of the two Class-D amplifiers reported in this work.

2.2.1 Simulink modeling

To better understand behavior and characteristics of a system, modeling is of paramount importance. In the initial design stage, indeed, ideal simplified blocks are used in place of the real and more complex components, in order to allow studying and understanding the main features and trade-offs in the system under analysis.

Among all the available simulation environments, for this work we chose Simulink that, basing its operation on the Matlab environment, allows us to simply assemble and simulate both continuous-time and discrete-time systems, with a level of abstraction that depend on the model created.

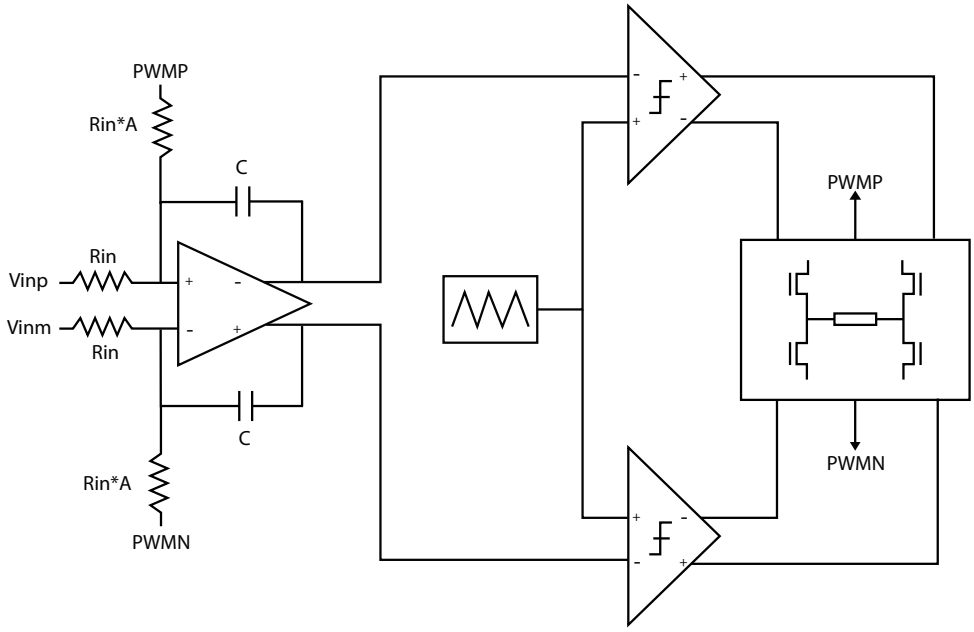

Figure 2.21: Fully-differential closed-loop Class-D amplifier implementation with BTL power stage

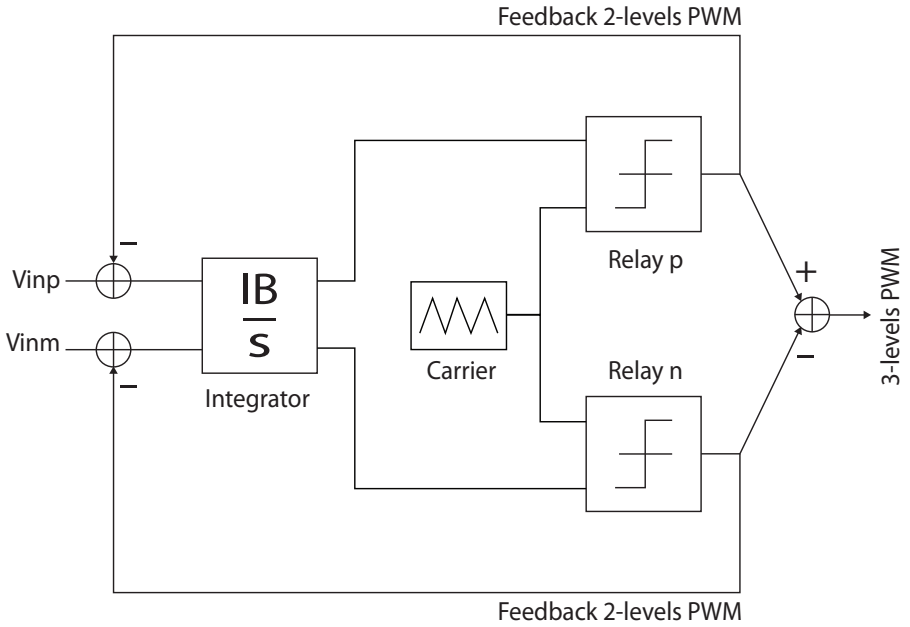

Figure 2.22: Fully-differential closed-loop Class-D amplifier model

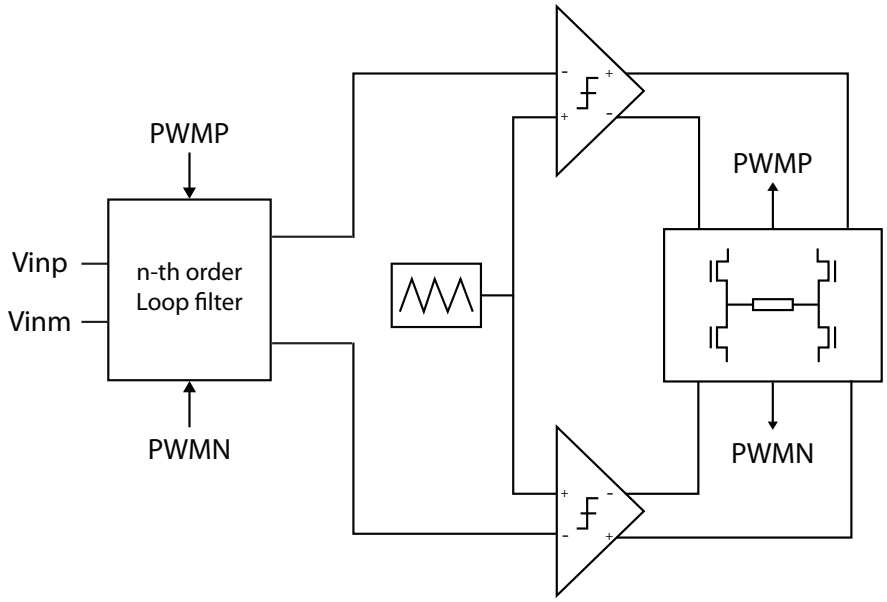

Figure 2.23: High-order fully-differential closed-loop Class-D amplifier implementation

The first prototype developed in this work starts from a pre-existent first-order fully differential Class-D amplifier, based on three-level PWM with a BTL bridge. The block diagram of the system is shown in Figure 2.21, while its model in Simulink environment is illustrated in Figure 2.22. It is a continuous-time system including a fully-differential integrator, two comparators and the power bridge. The integrator consists of a $1/s$ with a gain IB that models the Unity Gain Frequency (UGF) of the integrator. The comparators and the fully-differential power bridge are modeled by two relay blocks and a subtractor block, respectively: the relay blocks generate two complementary two-level PWM signals, while the subtractor produces the differential output signal implementing the three-level PWM. From model point of view at this abstraction level, the function of the power bridge is only to rise the output voltage level from the low voltage supply (3.3 V) to the high voltage supply (5 V) used to drive the bridge. For this reason, the comparator output swing has been increased to 5 V, in order to obtain, without additional blocks, the right voltage level to be sent back to the input through the feedback. Starting from this model, it is possible to replace the single integrator with a more complex circuit (n^{th}-order filter), thus achieving a higher-order loop, increasing the loop gain and improving the linearity of the Class-D amplifier. as shown in Figure 2.23. This circuit, however, must follow some strict stability rules.

2.2.2 High-order Class-D amplifiers

In order to find stability criteria for high-order Class-D structures, we can start from a useful observation: a closed-loop Class-D amplifier is quite similar to a sigma-delta ($\Sigma\Delta$)

modulator. Both are based on a feedback loop with a number of integrators as large as their order, both contain a non-linear element (the PWM modulator in the Class-D amplifier and the quantizer in the ΣΔ modulator), and both have zeros and poles introduced by feedback and feedforward loops. On the other hand, it is clear what makes them different: a Class-D amplifier, using an analog PWM, is ideally able to represent an infinite number of levels by changing the duty cycle of the carrier in each period, while a ΣΔ modulator, because of the quantizer can represent only a finite number of states ("0" and "1" for a single-bit quantizer, with 50% duty-cycle), as summarized in Figure 2.24.

In other words, a class-D amplifier, being an analog system, does not perform any quantization of the signal unlike a ΣΔ modulator that can provide only a given number of output levels, depending on the resolution of the quantizer used. In practice, the loop filter in a ΣΔ modulator suppresses the in-band quantization noise, whereas the loop filter in a Class-D amplifier attenuates spurs and errors (mainly harmonic distortion), introduced by the PWM modulator and the power stage. For a given order, the linearized equivalent model of a ΣΔ modulator is the same as that of a Class-D amplifier, as shown in Figure 2.25, where ϵ is the quantization error in a ΣΔ modulator or the PWM and power transistor bridge errors in a Class-D amplifier. The output voltage V_{out} is given by:

$$V_{out} = V_{in}\frac{H(s)}{1+H(s)} + \epsilon\frac{1}{1+H(s)} \tag{2.9}$$

where, with a proper choice of $H(s)$, the contribution of ϵ can be attenuated as required, while leaving V_{in} unchanged [21]. The higher is the order of $H(s)$, the higher is the attenuation of the spurs.

Based on these considerations, we can use the theory and the tools developed for the design of ΣΔ modulators to design the loop filter of a Class-D amplifier. Indeed, the ΣΔ modulator theory is well established and many toolboxes for ΣΔ modulator design are available. In particular, the *DelSig* toolbox [22] allows the definition of the coefficients of the loop filter, independently of the order, starting from some basic parameters. For how the tool is made, the output coefficients are defined for a discrete-time filter but, considering the well known *Backward-Euler* transformation between $\mathcal{L}$-transform and $\mathcal{Z}$-transform:

$$\frac{1}{z-1} \rightarrow \frac{1}{sT_s} \tag{2.10}$$

where T_s is the carrier period, it is possible to apply them also to the continuos-time counterpart and directly realize a stable continuous-time loop filter [23].

2.2.3 Design methodology for high-order Class-D amplifiers

Once identified the similarity between Class-D amplifiers and ΣΔ modulators, it is straightforward to introduce the practical design flow used during the design activity reported in this work.

The first step is the choice of the filter structure. The *DelSig* toolbox allows selecting the topology of the filter between cascade of integrators with feedback (CIFB), shown

	$Duty - Cycle$	$CarrierPeriod(Ts)$	$OutputValues$
$\Sigma\Delta$	50%	Ts	0, 1
$Class - D$	$0 \div 100\%$	Ts	0, 1

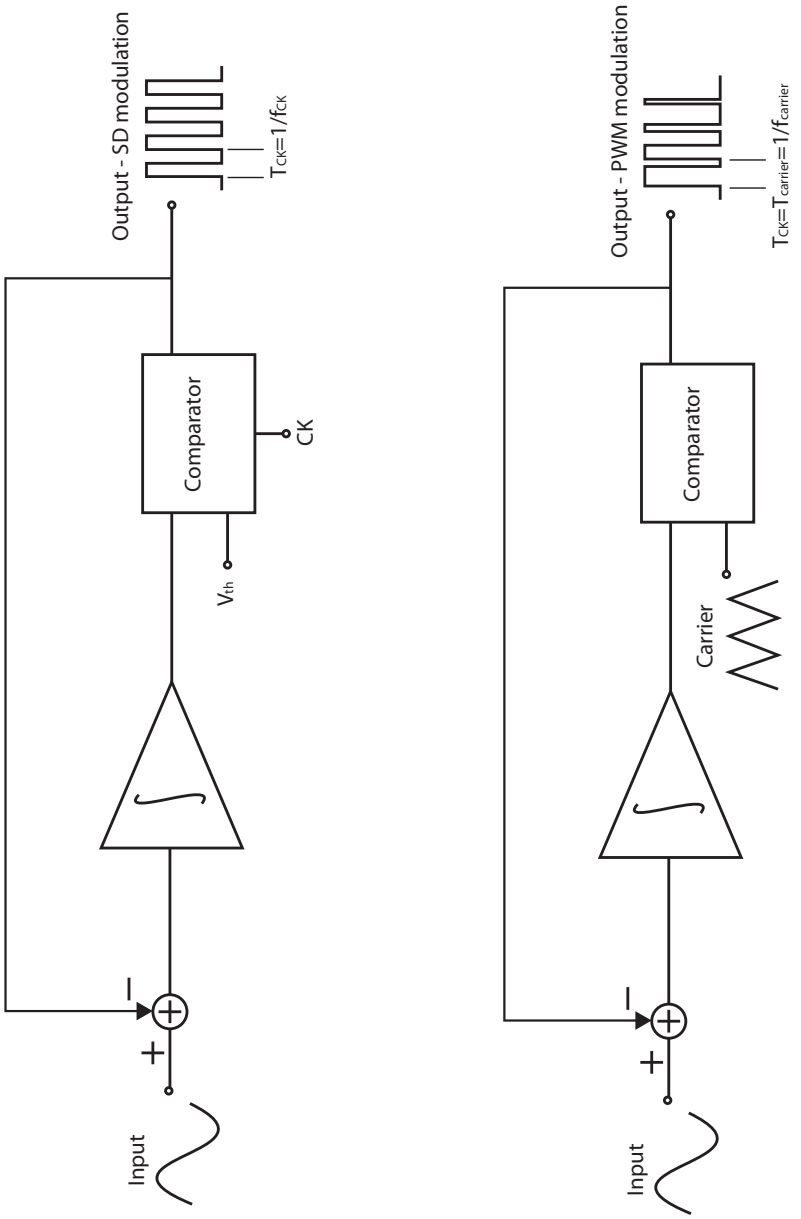

Figure 2.24: $\Sigma\Delta$ modulator versus Class-D amplifier

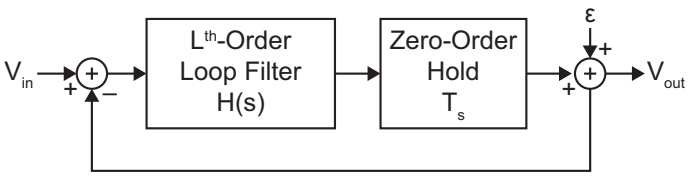

Figure 2.25: Linearized equivalent circuit of a ΣΔ modulator or a class-D amplifier

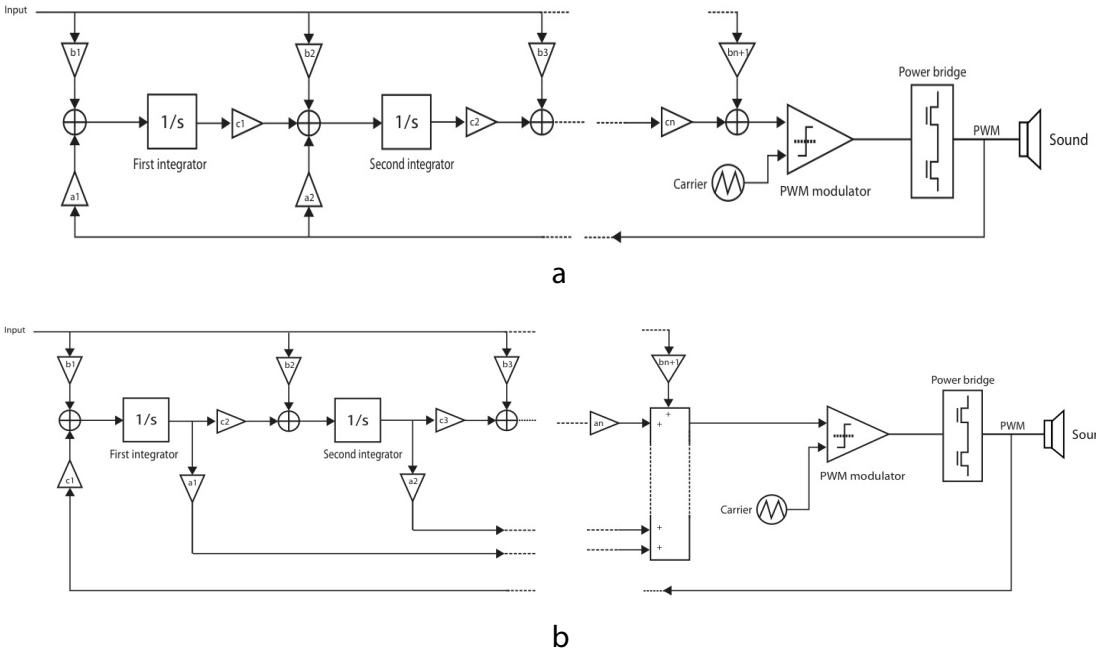

Figure 2.26: Basic CIFB and CIFF structures

in Figure 2.26a and cascade of integrators with feedforward (CIFF), reported in Figure 2.26b. Actually, this choice is not so relevant to the stability performance of the whole system, but it changes the required integrator specifications. In a CIFF structure, thanks to the feedforward paths, the input signal is not flowing through the integrators, thus allowing more relaxed operational amplifier specifications than in CIFB structures. On the other hand, the filtering action of the loop filter in CIFF structures is less effective and an adder is required to combine the different feedforward paths.

Once the filter topology is selected, the filter order L of the Class-D amplifier and the oversampling ratio (OSR) should be provided to the *DelSig* toolbox along with some flags for optimizing the pole and zero placement. The OSR is given by the ratio of the equivalent carrier frequency ($f_c = 2/T_s$ for three-level PWM or $f_c = 1/T_s$ for two-levels PWM) and twice the input signal band ($2 \cdot B$).

After that, we obtain the coefficients that guarantee system stability, but the spurs

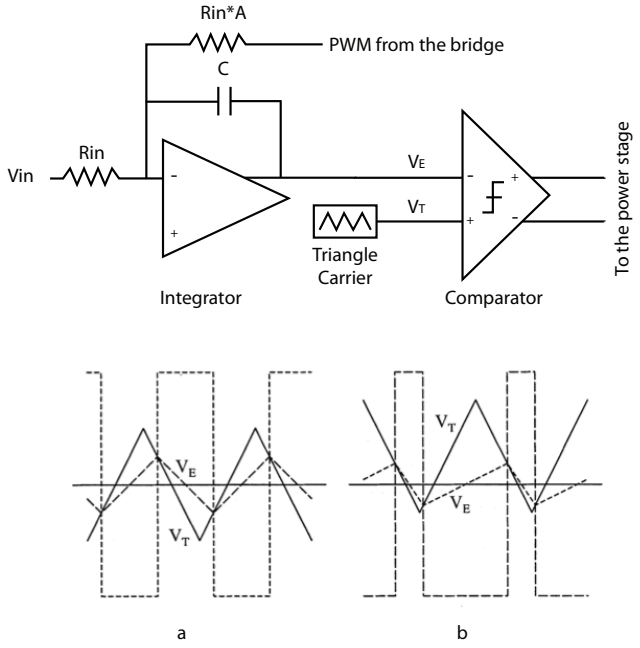

Figure 2.27: Internal loop signals: a – Zero input, b – Positive input

suppression effect could be quite poor. Indeed, the carrier frequency of a common Class-D amplifier is normally lower than 400 kHz and the *OSR* is very limited considering the 20-kHz audio band. To overcome this issue the designer have to tune the coefficients, in order to obtain the THD level requested by specifications, trying to maintain enough loop-filter phase margin to ensure system stability.

A very useful technique is to increase the c_n coefficients, which represent the forward gain of the filter and consist, as shown in Figure 2.26, of gain blocks connected between each integrator output and the next integrator input. In this way, the loop gain increases and, accordingly, also the suppression of the in-band harmonics increases, improving the THD. However, increasing these coefficients too much makes the system stumble into some drawbacks:

- degradation of the efficiency;
- degradation of the PWM;
- saturation of the system.

The first drawback is caused by the increased power consumption of the operational amplifiers due to the increased integrator UGB because of the larger c_n coefficients. Indeed, being a linear system, the gain introduced by the single c_n block can be seen also as a multiplication of IB for the same value and, as a consequence, the need of a wider band operational amplifier. In the real world, this leads to increasing of the operational amplifier bias current that, increasing the system quiescent power, worsens the efficiency.

The second drawback can be understood by considering the condition for proper op-

eration of the PWM generator [24]. As illustrated in Figure 2.27, the following general rule should be satisfied to perform PWM without saturation:

$$\textit{Carrier Slope} > \textit{Integrator Output Slope} \tag{2.11}$$

The general time-domain rule expressed in (2.11) is translated into the well-known frequency-domain rule for the loop to maintain the PWM correct:

$$\omega_{UG} < \frac{\omega_c}{\pi} \tag{2.12}$$

where ω_c is the carrier angular frequency and ω_{UG} is the unity gain band of the loop transfer function of the Class-D amplifier. The value of ω_{UG} is approximately given by:

$$\omega_{UG} = G_{PWM} \cdot \omega_{LPF} \tag{2.13}$$

where ω_{LPF} is the unity gain frequency of the Class-D filter and G_{PWM} is the PWM modulator gain, defined as

$$G_{PWM} = \frac{V_P}{V_c} \tag{2.14}$$

in which V_P is the PWM amplitude and V_c is the triangular carrier amplitude. When coefficients c_n are increased too much, ω_{LPF} becomes too large, violating the condition given by (2.12). Under this operating condition, the PWM starts to show multiple pulses per carrier period, increasing the switching losses. However, the loop acts to maintain a correct modulation up to a critical point where the third drawback comes into play: instability and saturation of the system.

At this point of the design, in order to pass from the model to a stable schematic circuit, it is only necessary to respect the relations imposed by the coefficients previously established, determining resistance and capacitance values according to these numbers. As an example, for a third-order structure, $b_1 = 0.044$. Choosing 50 kΩ as input resistance and setting the IB to be 400 kHz, the first integrator capacitance turns out:

$$C = \frac{1}{IB \cdot R} = \frac{1}{400\ \text{kHz} \cdot 50\ \text{k}\Omega} = 50\ \text{pF} \tag{2.15}$$

while the input resistance of the first stage is:

$$R = \frac{50\ \text{k}\Omega}{0.044} = 1.136\ \text{M}\Omega \tag{2.16}$$

As a matter of fact, especially using a CIFB structure, when using directly these theoretical values of the components, the SNR can be very poor because the noise produced by the resistors is too large. Therefore, the coefficients have to be scaled again in order to obtain a good trade-off between noise, operational amplifier output swing and area (typically dominated by the large value of the integrator capacitors).

2.3 Class-D toolbox

During the design activity, many Matlab scripts have been realized. At the end of the work the most important have been revised, optimized and grouped in a dedicated toolbox, which implements the design methodology explained above, oriented to the Class-D design. A brief description of this toolbox and of its main functions are reported in Appendix A.

2.4 Conclusions

In this chapter we described the most important output amplifier classes, with their main characteristics and behavior. In particular, Class-D amplifiers have been analyzed, defining the main parameters that need to be taken into account during the design. In the last part of the chapter a new methodology to design Class-D amplifier, starting from the $\Sigma\Delta$ modulator theory has been described. In the following chapter we will present the detailed design of two different third-order Class-D amplifiers, starting from the models to the silicon realization.

Chapter 3

Third-order Class-D amplifiers

Taking as reference the general circuit of Figure 2.20, it is possible to note that the power bridge is characterized by a conceptually much simpler structure than the integrator and the PWM modulator: just using two complementary transistors it is possible to transform the relatively high impedance of the PWM modulator in a low impedance and improve the drive capability of the system. However, if the design of the rest of the circuit implies the consideration of many more parameters, from the performance of the single operational amplifier (opamp) to the phase margin of the entire system, the implementation of a good power bridge is quite complicated, due to the non-idealities that can show up in the real structures. In fact, second-order effect, such as as temperature changes or leakage, that normally can be neglected, due to the high power levels managed by the output stage, can lead to the incorrect operation of the stage and, in some case, to the breakdown of the chip.

Due to the difficulties involved in modeling these characteristics under extreme working conditions, a power bridge good design can be performed only merging simulation and measurement results from some test-chip, basically after collecting some experience directly on the field. Therefore, starting from an already existing Class-D amplifier with a well tested and characterized power bridge, after modeling the whole system, we focused our work only on the feedback loop, searching for solutions able to improve the linearity performance, reducing the distortion contributions of the already available power bridge.

In this way, we realized two Class-D amplifiers with very high linearity performance, which verify and validate the design methodology described in Chapter 2. In fact, leaving all the other circuital blocks unchanged, at least in the first of the two realized chip, but changing only the structure of the loop filter, a very useful and coherent comparison between a first and a third-order Class-D amplifier, can be done, thus highlighting the real benefits of the new design.

3.1 First version (Ver. 1) – Test chip

Starting from the model illustrated in Figure 2.22, the behavior of the first-order Class-D amplifier have been deeply analyzed: delay time, dead time, carrier non-linearity, power

Order	THD [dB]
1^{st}-order	−70
2^{nd}-order	−80.5
3^{rd}-order	−93.5
4^{th}-order	−103

Table 3.1: THD values varying the loop filter order (test signal: V_{in} = 500 mV, f_{in} = 1 kHz, 1% of 3^{rd} harmonic distortion)

switch on-resistance and other non-idealities, have been introduced one by one, leaving the rest of the circuit completely ideal, in order to create parametric simulations and understand the distortion contribution of each non-ideality.

From this study it is clear that no large improvements could be achieved on the loop filter components: the non-linearity contribution introduced by the different blocks, such as the comparator or the operational amplifier, which were already optimized in the first-order design, are negligible with respect to the distortion terms related to the switching behavior of the system (most of all the power bridge driver dead time control), that, in order to preserve the efficiency, has to be leaved unchanged. Therefore, a higher-order loop-filter turned out to be the only viable way to improve the Class-D amplifier performance.

3.1.1 Architecture and design procedure

According to the methodology described in Chapter 2, the amplifier design started with the choice of the filter topology. Since we wanted a sharp out-of-band filtering action, in order to obtain a very effective noise shaping function, a CIFB structure has been chosen. Considering the requirement of a very low THD (under −90 dB) as the main target specification, a linearity study changing the order of the loop filter in the model of Figure 2.22 has been carried-out. Inserting a fixed amount of distortion by adding a 3^{rd} harmonic before the comparators on both signal paths, it has been possible to quantify the THD improvement that each order can achieve. Table 3.1 summarizes the main results of this analysis: it is possible to see that, if we want to reach the THD value requested by the specifications, at least a third-order loop filter has to be implemented.

Once selected the order and the topology of the filter, a set of stable coefficients has been calculated with the *DelSig* toolbox. Due to the three-level PWM, the effective carrier frequency (384 kHz) doubles and, in order to use correctly the toolbox, both the *OSR* and the parameter *IB* have to be doubled as well. The obtained Simulink model is shown in its single ended form (although the circuit is actually fully-differential) in Figure 3.1: also in this case, a 3^{rd} harmonic generator is inserted before the comparator in order to measure the THD variations changing the filter parameters.

As explained in Chapter 2, the obtained ideal set of coefficients did not satisfy the THD specifications due to the low *OSR*. Therefore, a tuning of these values has been done. First

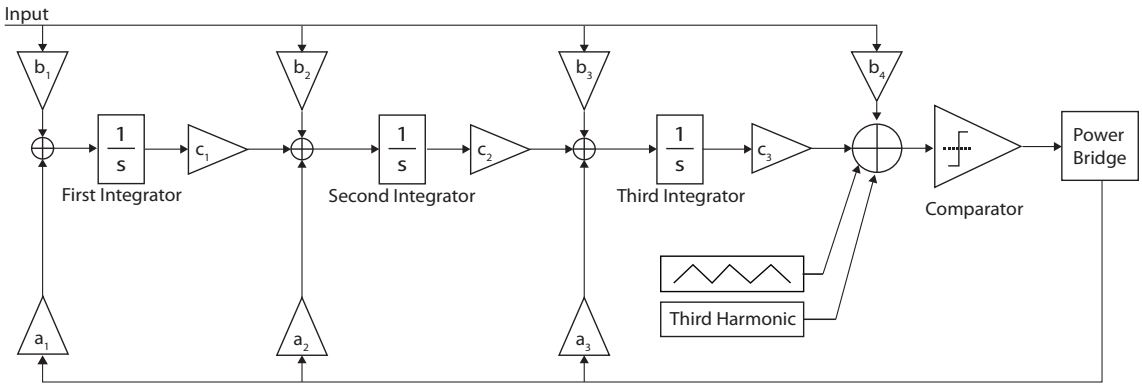

Figure 3.1: Third-order Class-D amplifier model

Coefficient (original/scaled)	1	2	3	4
a	0.044/0.044	0.2881/0.2881	0.7997/0.7997	–
b	0.044/0.044	0.2881/0	0.7997/0	1/0
c	1/2	1/4	1/1	–

Table 3.2: Original and scaled coefficients of the Ver. 1 Class-D loop filter

of all, in order to obtain a very high filtering action of the CIFB structure, all feed-forward paths from the input to the various integration stages have been eliminated. Moreover, the forward gain has been increased (c_n coefficients), considering a trade off between increasing the loop filter and keeping the phase margin needed to maintain stability. The ideal and final sets of scaled coefficients are reported in Table 3.2.

Once obtained a model achieving the required THD, the migration to the transistor-level design has been possible. Always following the procedure, a fully differential active *RC* structure, shown in Figure 3.2, has been realized, dimensioning all the components proportionally to the previously calculated coefficients.

At this point the specification of SNR had to be satisfied by modifying the first integrator stage components, while maintaining unchanged the *RC* product. Considering that most of the noise is aused by the first-stage resistors and opamp, the equations used to calculate the input referred noise contributions are the following:

- input resistance R_{in}:

$$V^2_{n(R_{in})} = 4kTBR_{in} \tag{3.1}$$

- feedback resistance R_{fb}:

$$V^2_{n(R_{fb})} = \frac{4kTBR_{fb}}{G^2} \tag{3.2}$$

- opamp:

$$V^2_{n(OP)} = V^2_{n(op)} \cdot \frac{1+G^2}{G^2} \tag{3.3}$$

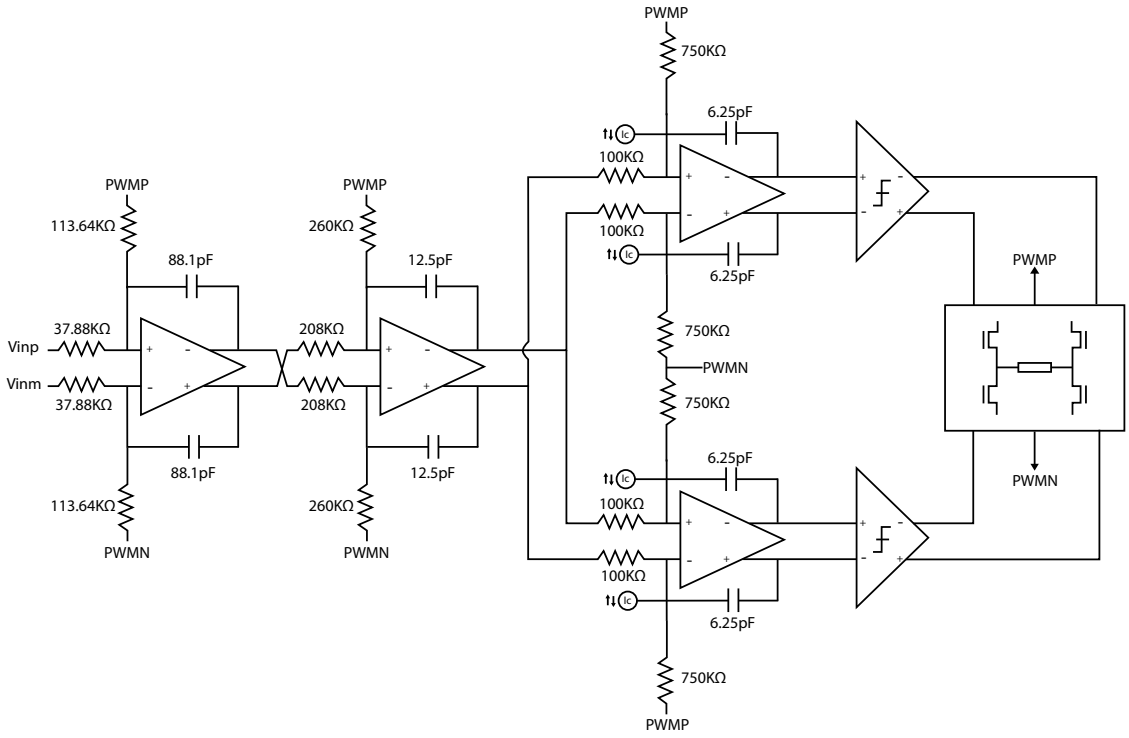

Figure 3.2: Third-order Class-D amplifier schematic

in which R_{in} and R_{fb} are the input and the feedback resistors, respectively, $V_{n(OP)}$ is the total noise voltage of the operational amplifier used in the first integrator, G is the gain of the Class-D amplifier equal to 3, B is the signal bandwidth, k is the Boltzmann constant and T is the temperature. The total input referred noise of the Class-D amplifier can be expressed as:

$$V_{CDn} = \sqrt{[V^2_{n(R_{in})} + V^2_{n(R_{fb})}] \cdot 2 + V^2_{n(OP)}} \tag{3.4}$$

where the factor 2 is introduced to account for the fully differential structure.

Having a fixed $V_{n(OP)}$ given by the existing opamp and wanting to maintain an SNR of about 103 dB with a maximum output power of 2 W over a 4-Ω resistive load, it has been possible to obtain all the first-stage resistance values by solving (3.4). Finally, considering the output swing of each opamp, also the capacitance values has been defined.

Being a test chip, in this first amplifier many control bits have been included to program different parameters. In order to test the THD variations and to test the Class-D amplifier stability varying the forward gain of the loop, three possible settings for each integrator have been included: for each stage nominal capacitor and input resistance values can be changed independently by programmable switches. Table 3.3 reports all the component values used in the designed loop filter.

First Integrator		
Component	**Value**	**# of instances**
R_{in}	37.88 kΩ	1
R_{fb}	113.64 kΩ	1
C_{1000}	1.175 pF	60
C_{900}	1.3 pF	6
C_{800}	1.225 pF	8
Second Integrator		
Component	**Value**	**# of instances**
$R_{in-20\%}$	156 kΩ	1
R_{in}	52 kΩ	1
$R_{in+20\%}$	52 kΩ	1
R_{fb}	260 kΩ	2
C_{1000}	2.5 pF	4
C_{900}	1.11 pF	1
C_{800}	1.39 pF	1
Third Integrator		
Component	**Value**	**# of instances**
$R_{in-20\%}$	80 kΩ	1
R_{in}	20 kΩ	1
$R_{in+20\%}$	20 kΩ	1
R_{fb}	(400 + 350) kΩ	2
C_{1000}	2.5 pF	2
C_{900}	0.55 pF	1
C_{800}	0.69 pF	1

Table 3.3: Capacitor and resistor values used in the test chip design

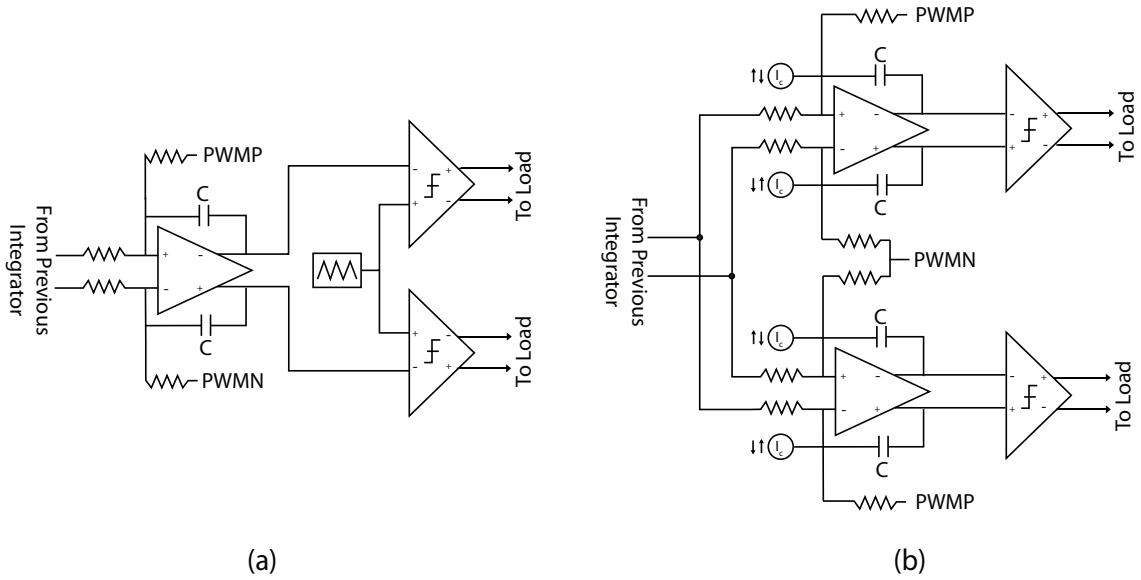

Figure 3.3: Carrier insertion: a – Stand alone generator, b – Square wave injection

3.1.2 Carrier generator

The carrier signal injection method in a Class-D amplifier is one of the most important design issues. As mentioned in Section 2.1.5, PWM carrier can be either a saw-tooth or a triangular wave signal. However, in order to obtain the three-level PWM required in filterless applications, it is necessary to use a triangular wave. Generally, Class-D amplifiers exploit a stand-alone trianglular carrier generator that has to produce a highly linear carrier, using minimum amounts of area and power. The carrier is then applied to the same input of two comparators, in order to create the three-level PWM (Figure 3.3a). Although very common, this solution introduces a series of problems related mostly to the linearity of the carrier and to the performance of the comparators, which have to operate with variable common-mode input signal.

In this design, instead, the triangular carrier signal is obtained by integrating a square wave along with the input signal in the last integration stage and its linearity depends mostly on the linearity of the integrator capacitor (the input signal and the injected square wave undergo the same non-linearity, thus reducing its effect). Moreover, with this solution all the carrier non-idealities are suppressed by the loop gain and the comparators operate with constant common-mode signal.

To realize the three-level PWM, it is necessary that one of the two following conditions is fulfilled:

- both comparators must compare the same carrier with two equal signals in counter-phase;
- both comparators must compare two equal in-phase signals with two equal carriers in counter-phase.

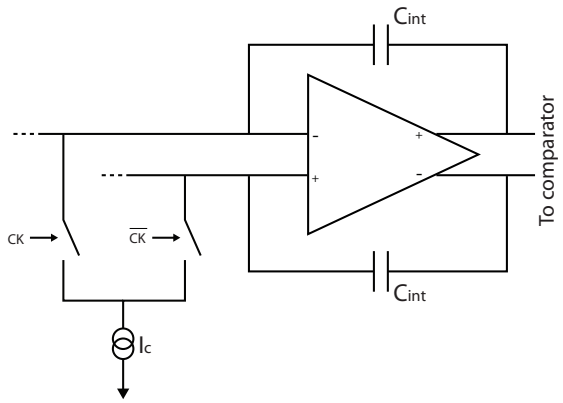

Figure 3.4: Carrier insertion circuit

In a fully-differential structure, each integrator deals with two equal signals in counter-phase, but cannot work with a common-mode carrier, due to the intrinsic common-mode rejection of the fully-differential topology. To overcome this problem, we adopted the solution shown in Figure 3.3b, where the third stage of the loop filter is duplicated and the same carrier is injected into both integrators, while the opposite phase differential input signal from the second integrator output is routed to the two third integrators, respectively. This corresponds to the first condition mentioned above.

Cascode current mirror

In order to inject a current signal in the last integrator and generate the carrier signal, a stable switching current generator have been designed. Its operating principle is summarized in Figure 3.4. A fixed DC current is routed alternatively to one opamp input or to the other by two switches driven by the clock of the system. Therefore, basically a current square wave is added to the audio information, obtaining at the integrator output the correct signal needed by the comparator to implement the PWM modulation.

This switching current generator has to be highly insensitive to the fluctuations of the opamp virtual ground. In fact, because of the direct feedback path coming from the BTL bridge, the opamp virtual ground of all the integration stages presents fluctuations under any operating condition. Therefore, a cascode current source has been implemented: the cascode structure, by increasing the current source output impedance, maintains constant both the DC operating point and the current mirror factor, independently of the visual ground voltage.

Figure 3.5 shows the schematic of the cascode switching current mirror. In order to route the current to either branch of the fully-differential structure, two small switches, $M1$ and $M2$, have been introduced. With this solution, the injected square wave ranges from zero to a fixed DC value set by the current mirror: this introduces a DC common-mode signal, that, being applied to the integrator virtual ground, affects the input common-mode voltage of the opamp, worsening the linearity . To avoid this, a secondary cascode current

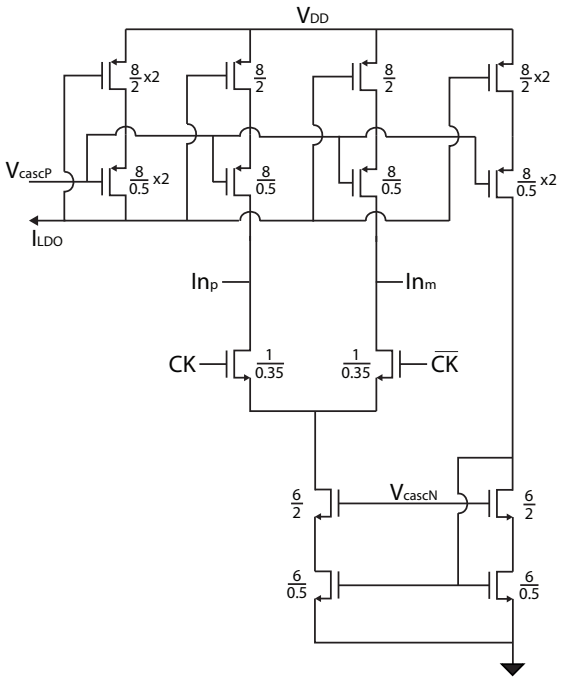

Figure 3.5: Carrier insertion circuit detailed schematic

mirror has been introduced, which, by mirroring a fixed DC current equal to half the square wave current in the opposite direction, removes the common-mode of the square wave and allows proper system operation.

The carrier frequency depends directly on the clock frequency, which is fixed. By contrast, the carrier amplitude can be programmed thanks to a set of four control bits, which act on a Low Dropout voltage regulator (LDO). The LDO, shown in Figure 3.6a, sets very precisely the current produced by the cascode current mirror. Indeed, due to the virtual ground of the opamp, the voltage across the programmable resistor is fixed to a value corresponding to input voltage of the LDO and. As a consequence, we obtain a current proportional to this voltage divided by the programmable resistance value. Figure 3.6b shows the scheme used to implement the programmable resistance used.

A critical aspect of this current/carrier generator is the offset that can be generated at its output by transistors mismatch or other non-idealities. For example, also a non precise switching of the current mirror, introducing a duty-cycle different from 50%, would bring the system to the saturation, since the Class-D system would see a DC differential information that would be integrated in the loop filter. This problem cannot be corrected neither by the output common-mode feedback of the single integrators nor by the global differential feedback loop of the filter, because both differential outputs of both integrators of the third stage drift away from the fixed common-mode voltage by the same quantity, as shown in Figure 3.7. In this situation the average value of the differential signal is always fixed, also when the system reaches saturation.

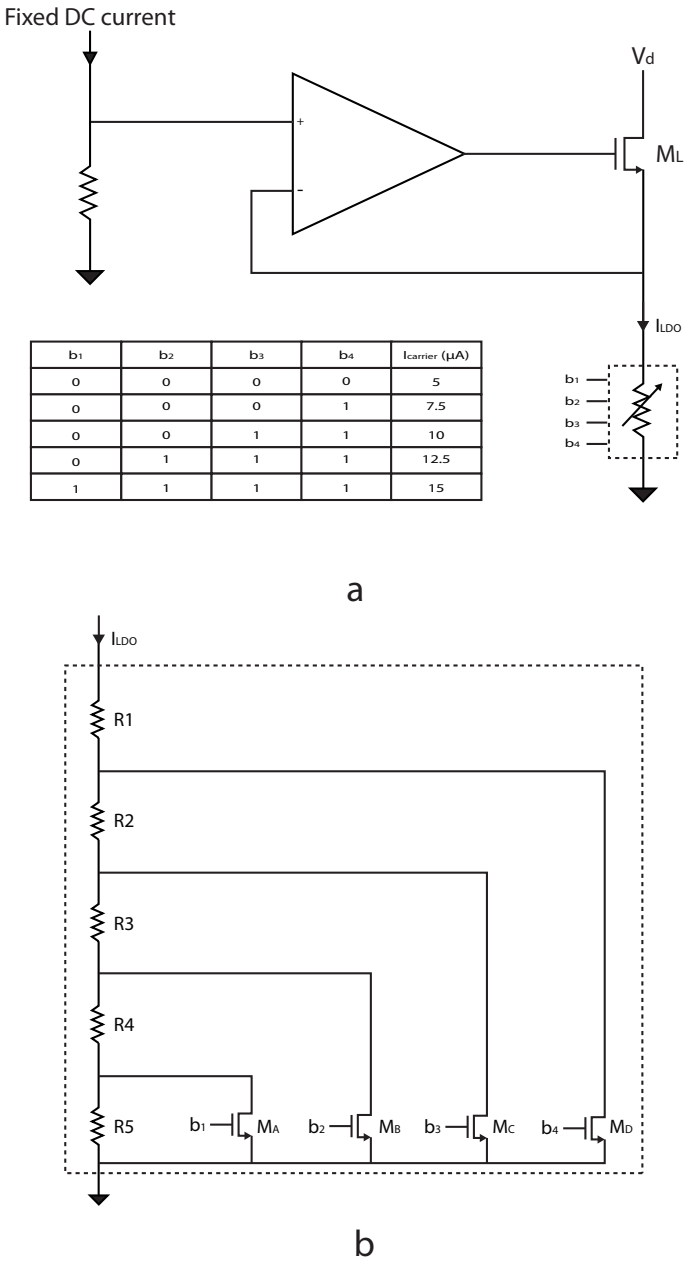

Figure 3.6: Carrier setting LDO system: a – LDO regulator system, b – LDO variable resistor

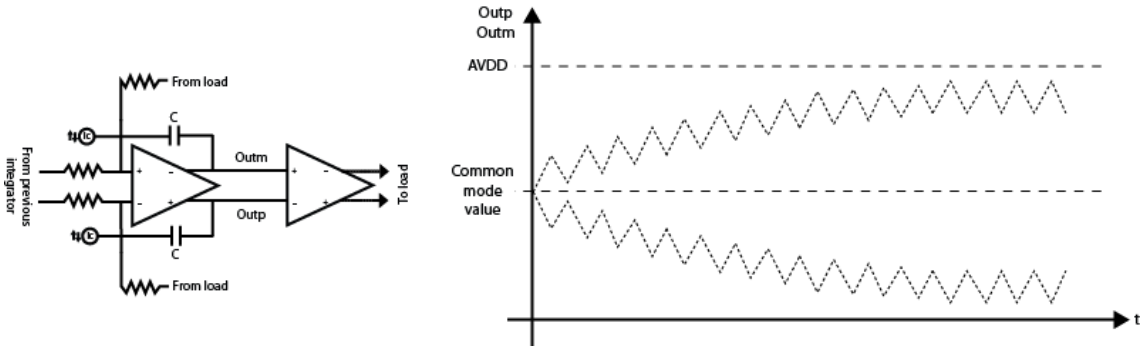

Figure 3.7: Integrator output behavior in the presence of carrier offset

A possible solution to this problem is the offset control circuit shown in Figure 3.8. A local feedback is introduced between the virtual ground and the output of both integrators of the third stage. The control circuit, including an additional gain stage, implements the function:

$$V_{dc2} = -V_{dc1} = (V_{p1} + V_{p2}) - (V_{n1} + V_{n2}) \tag{3.5}$$

The obtained signals V_{dc1} and V_{dc2} are injected in the virtual ground of both integrators of the third stage to compensate the carrier offset and keep the system out of saturation. Basically, the offset control circuit forces the common-mode levels of the both integrators to be equal, independently of the carrier offset.

Due to the signal phase inversion between the two integrators of the third stage, ideally, according to (3.5), the differential audio signal does not affect voltages V_{dc1} and V_{dc2}. However, since the control circuit has to compensate only the offset of the carrier, which is a DC voltage, we introduced in the control loop also a low-pass filter, in order to remove from V_{dc1} and V_{dc2} all possible contributions from the differential signal, even in the presence of mismatches. Actually, a pure integrator would theoretically be the best choice, but for stability reasons, we opted for a damped integrator, which guarantees an adequate phase margin, leading to a stable control-loop. The component dimension can be calculated considering a trade-off between the slew-rate of the splitted stag opamps and the additional thermal noise introduced by the resistors. However, considering that the offset control circuit acts on the final integration stage of the loop filter, the added resistors noise is referred to the input attenuated by the loop gain, thus allowing pretty large resistors to be used. Due to the finite gain of the offset control circuit, a fraction of the carrier offset voltage remains at the outputs of the integrators. However, since the carrier is generated using a very precise clock with a duty-cycle very close to 50%, also a contained gain (two in this case) is enough to make the residual offset negligible (comparable with the common-mode control error of the integrator opamp). The effect of the offset control circuit is illustrated in Figure 3.9.

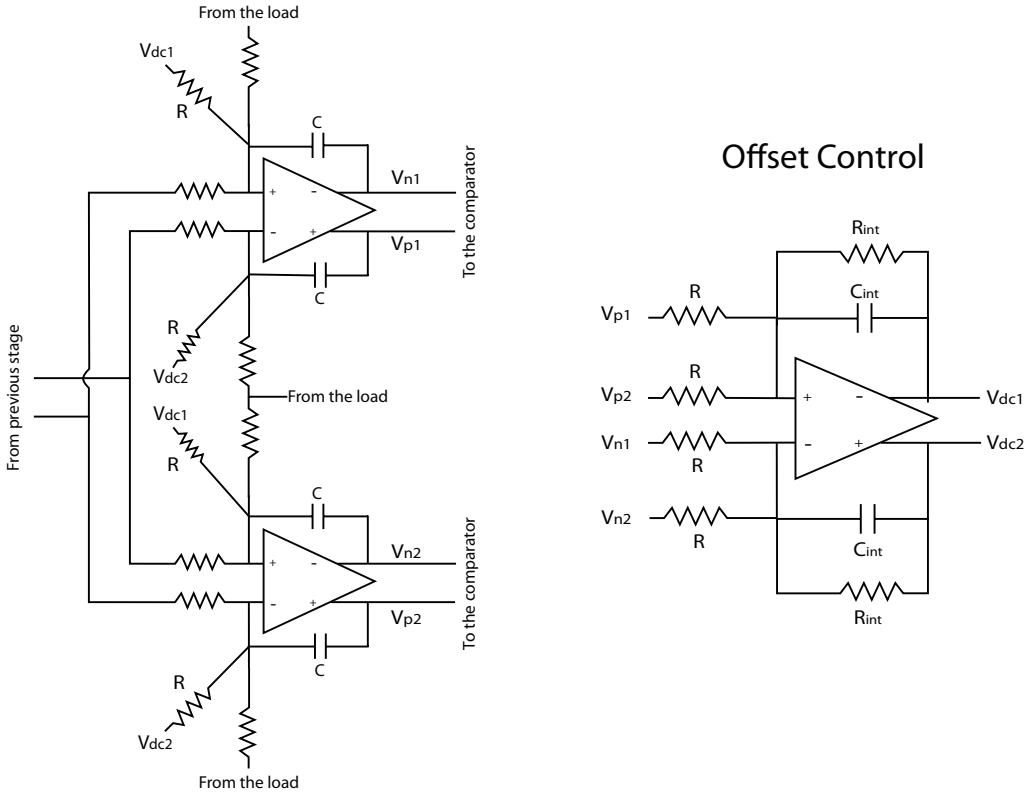

Figure 3.8: Carrier offset control circuit schematic

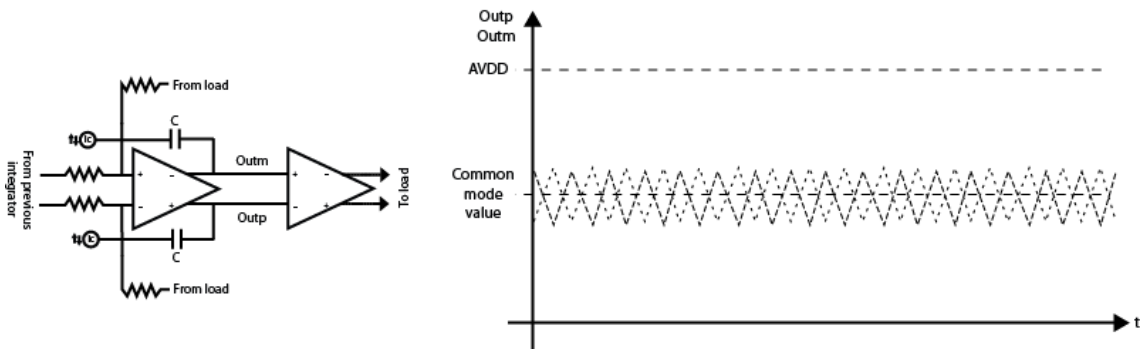

Figure 3.9: Integrator output behavior in the presence of carrier offset with the offset control circuit

3.1.3 Simulation and measurement results

In order to make a coherent comparison between the already existing first-order and the designed third-order Class-D amplifiers, many circuital blocks of the existing device have been reused in the designed one. The complete power stage, including the drivers, have been left unchanged, as explained at the beginning of Chapter 3, but also the comparators and the opamp have been used again without any customization. In particular, the opamp was originally optimized for the first stage of the first-order architecture and, therefore, it features low noise and large current consumption. In this test chip, we decided to use the same opamp for all the three integration stages, in order to be sure to obtain a very linear loop filter and prove the design methodology, do not taking in account resulting degradation of the efficiency. The opamp, whose schematic is shown in Figure 3.10, is based on a Class-A two-stage folded cascode structure with a total current consumption of about 2.7 mA. The amplifier achieves a DC gain of 120 dB and a phase margin of 65° with f_t = 90 MHz.

The third-order Class-D amplifier, together with the digital audio CODEC, have been integrated in the same chip, in order to be able to test the new design under the same conditions of the existing first-order amplifier. Figure 3.11 shows the layout of the Class-D amplifier only. The layout is not very symmetric and the power bridge overhang only half of the circuit. This is due to the fact that, in order to have enough area to introduce the two additional stages of the third-order amplifier, while maintaining the same shape for the digital part of the CODEC, one the two channels forming the stereo output has been completely removed. Moreover, most of the area is occupied by the first-stage integrator capacitor. This is due to the very low input coefficients of the CIFB structure and represents, together with the efficiency, one of the main aspects that have to be improved in the second version of the chip.

The fabricated chip has been tested in the Conexant laboratories, exploiting an Audio Precision equipment to ensure sufficient accuracy to verify the high linearity performance achieved with the device. The whole system has been tested with power supply and digital input signal provided by an high precision PC audio board. Measurements, considering 2 W as full-scale output power, have been performed in three different cases: without load and with a load consisting of the series of a resistor and an inductor with values equal to 8 Ω/22 μH and 4 Ω/22 μH, respectively, in order to simulate the impedance of a general speaker.

Figure 3.12a and Figure 3.12b show the spectra of the first and third-order amplifier output signals with $V_{in} = -3$ dB_{FS}, respectively. As it is possible to note, all the harmonics that are present in the first-order amplifier spectrum are strongly reduced in the third-order case: the harmonics average value shows an improvement of 25 dB, resulting in a very low THD.

Figure 3.13 shows the THD performance of the first and third-order devices as a function of the input signal amplitude. In general, the third-order system THD decreases more linearly with respect to the first-order device, which shows a corner around $V_{in} = -35$ dB_{FS}. In particular the curve can be divided in three regions according to the input

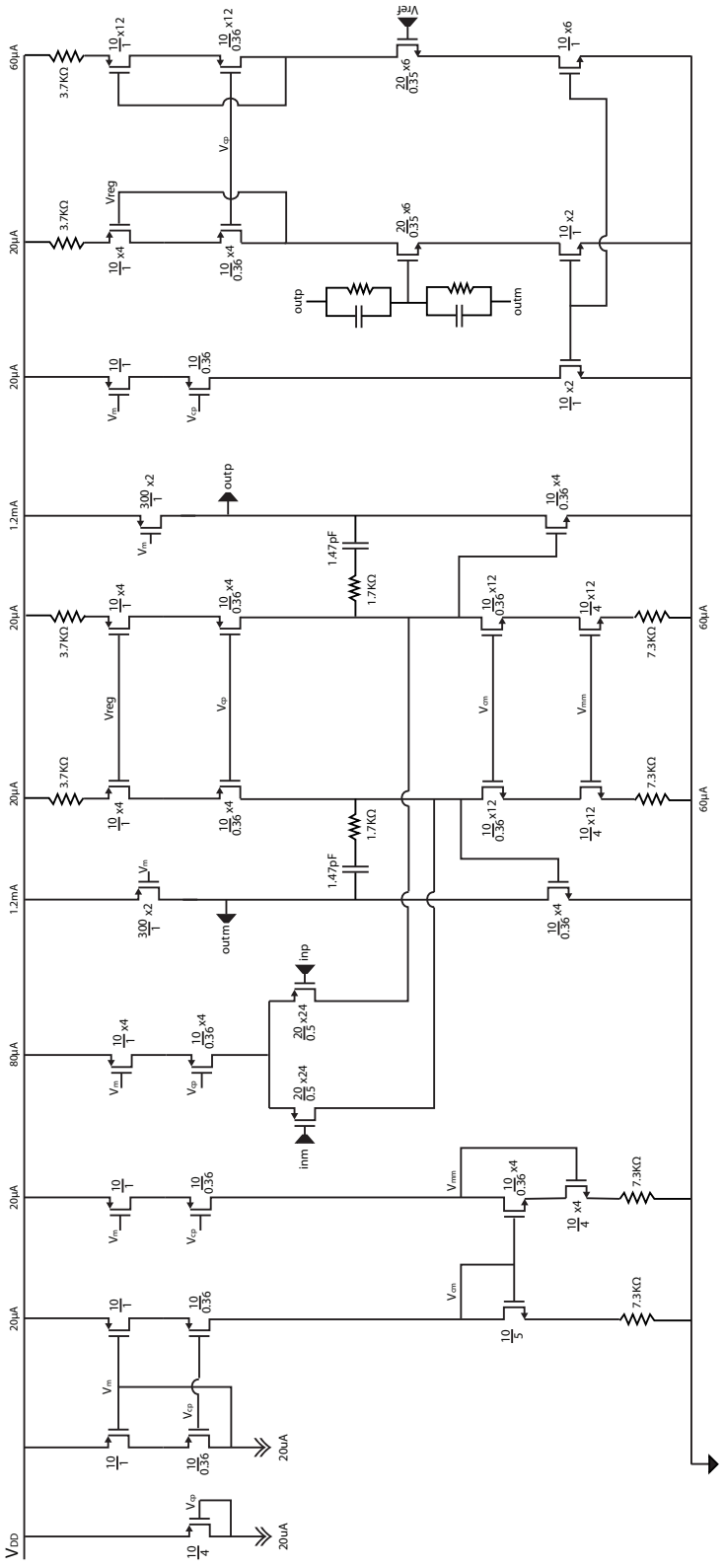

Figure 3.10: Operational amplifier used for all third-order integration stages

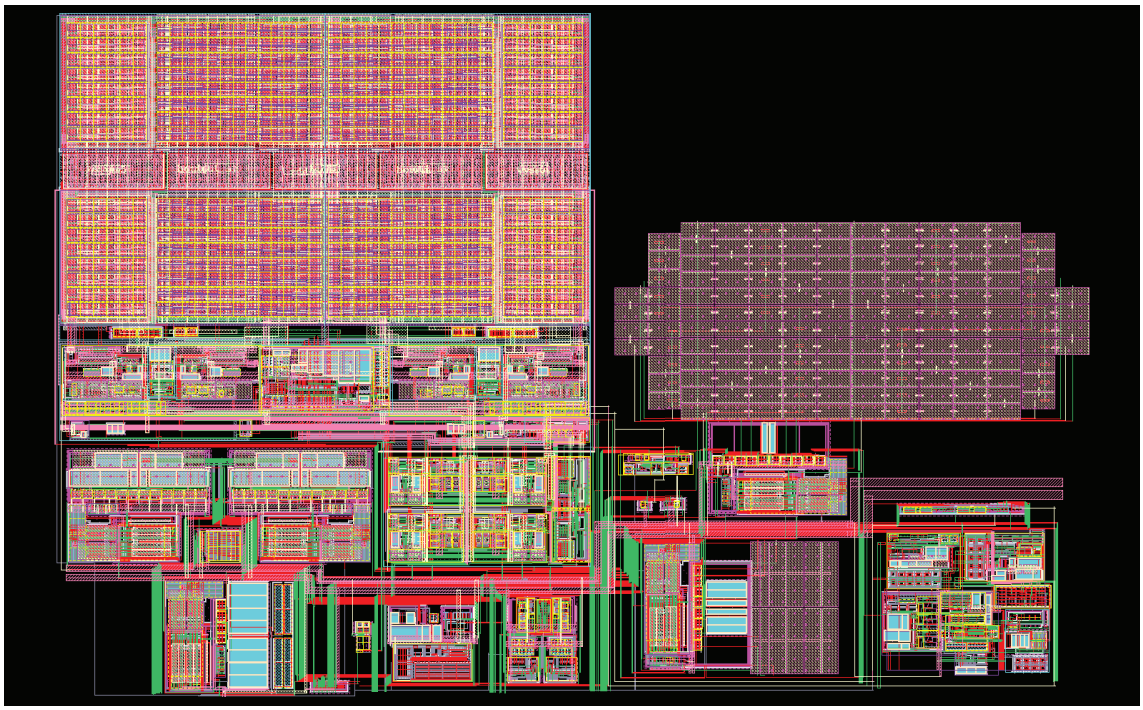

Figure 3.11: Third-order Class-D amplifier layout

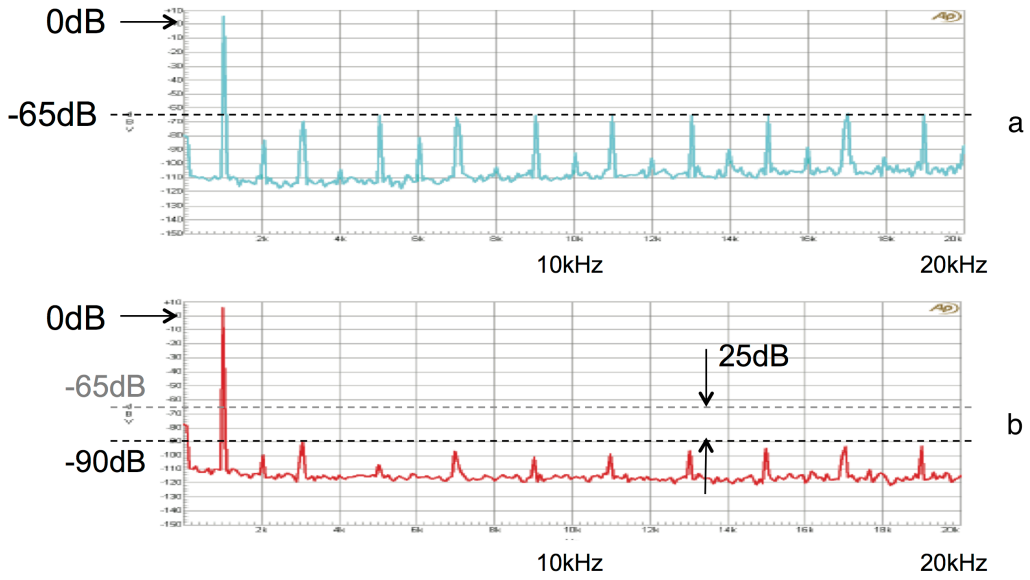

Figure 3.12: Comparison between output spectra with $V_{in} = -3$ dB_{FS} of: a – First-order amplifier, b – Third-order amplifier

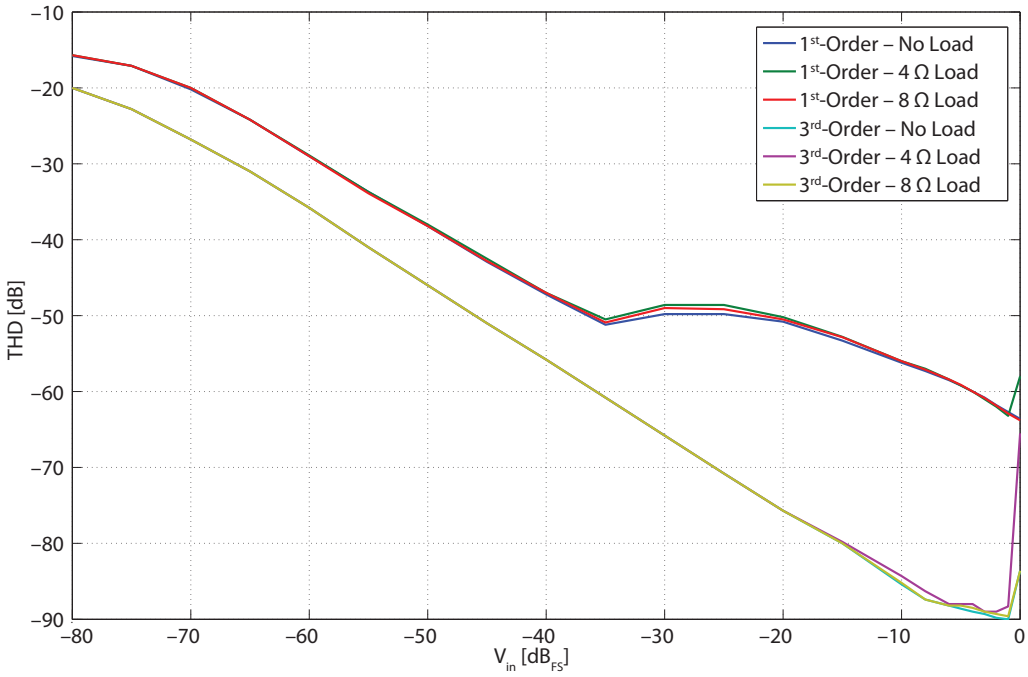

Figure 3.13: THD as a function of input signal level: comparison between first and third-order Class-D amplifier

signal amplitude. For very small input signals the improvement gave by the third-order filter is about 7 dB. Instead, a larger improvement can be seen from $V_{in} = -35$ dB_{FS} to the saturation region ($V_{in} > -3$ dB_{FS}): here the increased noise shaping of the third-order structure suppresses more efficiently the power bridge non-linearities, leading to a better THD. The root cause of the corner that can be observed in the THD curve of the first-order amplifier is not very clear: if for very small input signals the THD is dominated by the power bridge dead-time contribution, after $V_{in} = -35$ dB_{FS} other contributions become significant and, due to the modest first-order loop gain, they lead to a deterioration of the linearity. Most likely, after $V_{in} = -35$ dB_{FS} the main distortion contribution is introduced by the stand-alone carrier generator, that in the third-order amplifier has been eliminated. For high output power, as expected, the lower is the load resistance, the lower is the input signal value at which the system saturates. This is due to the increased output current delivered by the bridge, which produces a larger voltage drop on the on-resistance of the power transistors. Moreover, in this condition the THD is lower in the third-order structure, leading to an improvement for the 4-Ω load of about 8 dB.

Considering the whole transmission chain, from CODEC to class-D amplifier output, an SNR equal to 100 dB has been achieved, due to the optimization of the first-stage components. Since, as already mentioned, all the opamps have been maintained equal to the first-stage opamp of the first-order design, efficiency measurements would be meaningless and, hence, they have not been carried out.

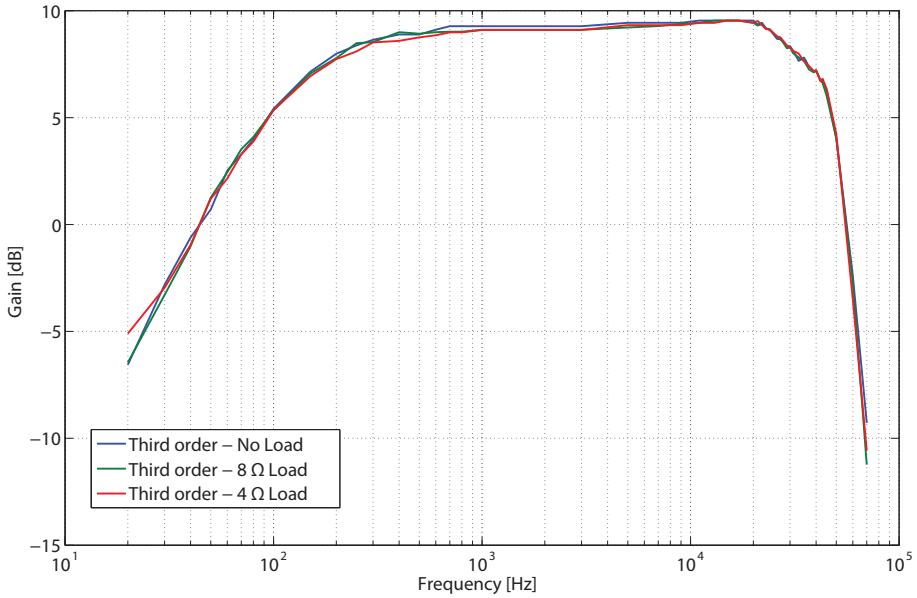

Figure 3.14: AC-coupled transfer function of third-order Class-D amplifier

Figure 3.14 shows the transfer function of the amplifier: at low-frequency the curve shows the AC coupling characteristics and the gain reaches its nominal value (9.5 dB) at 300 Hz. Beyond the audio band, the curve shows the expected low-pass filter behavior [25].

3.2 Optimized version (Ver. 2) – Stereo chip

In the first version of the realized third-order Class-D amplifier a large THD improvement has been achieved with respect to the first-order device, but the optimization of all the other system parameters, such as efficiency or area, has been disregarded. In the second version of the chip (Ver. 2), a general optimization of the system has been carried-out, customizing the opamp current consumption for each stage and reducing the first-stage integrator capacitor. Therefore, efficiency has been improved and layout area has been reduced, allowing the realization of a two-channel stereo Class-D amplifier, which shows competitive performance with respect to the most recent market products.

3.2.1 Coefficients and area optimization

In terms of area, the most critical aspect of Ver. 1 Class-D amplifier was the size of the first integrator capacitor. In fact, due to the adopted CIFB topology, the first-stage input and feedback coefficients were very small, resulting in very large resistor values, that had to be scaled down, in order to achieve the required SNR (about 103 dB). Since it is mandatory to maintain the *RC* product, defined by the integrator unity-gain bandwidth

(IB), in turn determined by the carrier frequency, the reduction of the resistances leads to a corresponding increase of the integrator capacitance.

Furthermore, the linearity of the first-stage integrator capacitor is quite important, since any non-linear contribution introduced in the first stage is not attenuated by the third-order loop filter, worsening significantly the THD performance. To ensure the maximum linearity, all the loop filter capacitors have been realized with Metal/Metal (MiM) structures. These capacitors exploit both vertical and horizontal electric field between two or more metal levels (in our case the fourth and the fifth metal layers), separated by a dielectric layer, thus achieving higher linearity with respect to the capacitors obtained exploiting polysilicon or silicon layers. Unfortunately, the specific capacitance achieved by MiM structures is about three times smaller than the value obtained with polysilicon capacitors (about 1 fF/μm^2). Moreover, in order to avoid crosstalk and intermodulation, it is not possible to overlap the MiM capacitors with any other part of the system. For all these reasons, the first integrator capacitors are the largest component of the whole Ver. 1 system and have to be reduced.

Starting from the Simulink model reported in Figure 3.1, we tried to find a solution for reducing the integrator capacitor area while maintaining the same THD performance achieved by Ver. 1 amplifier. As already mentioned, in order to obtain a very sharp out-of-band filtering action and a stronger non-linearity suppression, all the feed-forward paths from the input to the integration stages had been removed. Indeed, the injection of a fraction of the input signal after an integration stage worsens the filtering action of the integrator itself, due to the introduction of a direct path toward the output. However, at the same time, exactly for the same reason, the feed-forward path removes the input signal from the integrator output, reducing the opamp output swing. This effect can definitely be used to alleviate the opamp specifications [26], but it can also be exploited to reduce the integrator capacitance value. Indeed, a reduction of the integrator capacitance leads to an increase of the integrator IB and, consequently, to an increase of the integrator output swing, which can be compensated by the corresponding reduction granted by the feed-forward paths, actually maintaining the same opamp output swing as in Ver. 1 design, but with smaller capacitors.

The coefficients of the solution adopted are reported in Table 3.4. With this configuration, without loosing in THD performance and system stability, we reduced the first integrator capacitance by a factor three. Moreover, with this solution, the second stage deals only with the error signal (no useful signal is present at the output of the first integrator), thus relaxing significantly its output swing requirement.

3.2.2 Opamp architecture

The other important drawback of Ver. 1 Class-D amplifier, was the excess power consumption due to the fact that the same opamp designed for the first-order circuit was used for all the integration stages in the third-order design. This amplifier is very performant. It features a very high DC gain, a very large bandwidth, low noise, and a very large load current driving capability, thus requiring a bias current as large as 2.4 mA. All this fea-

Coefficient	1	2	3	4
a	0.044	0.2881	0.7997	–
b	0.044	2/3	1	0
c	2	4	1	–

Table 3.4: Scaled coefficients for optimizing the THD performance and the integrator capacitance area

tures, needed in the first-order amplifier to guarantee sufficient linearity with a first-order loop filter, are definitely excessive for the third-order structure.

In order to optimize the efficiency of the amplifier, we carried-out a trade-off study, exploiting a VerilogA model in the Cadence environment. The third-order loop filter has been modeled using ideal amplifiers with programmable dominant pole and DC gain. By varying these two parameters we found out that for all the stages after the first, modest values of DC gain (around 60 dB) and bandwidth (around 20 MHz) are sufficient to achieve full performance, without any degradation in the THD. Therefore, we designed two new opamps: one for the first stage and the other for the remaining integration stages. A different opamp is required for the first stage in order to optimize the SNR of the Class-D amplifier. The new opamps are more relaxed in terms of performance and feature a lower power consumption than the original one.

For the first integrator, the opamp available from the first-order design has been modified, introducing a Class-AB output stage. As explained in Chapter 2, thanks to the battery inserted between the two complementary transistors of the output push-pull stage, the quiescent current of the Class-AB output stage can be reduced a lot, while maintaining large slew-rate, gain and bandwidth. The Class-AB amplifier schematic is reported in Figure 3.15. By comparing it with the schematic of the original amplifier of Figure 3.10, it is possible to note that the first folded cascode stage is unchanged, thus maintaining the input referred noise performance and hence the system SNR. Moreover, only adding few biasing branches and the battery, the quiescent current of the two differential output branches has been reduced from 1.2 mA to 200 μA each. This last aspect, besides representing a large benefit in terms of efficiency, leads to the reduction of the opamp bandwidth, since it requires a double frequency compensation net in order to maintain a reasonable phase margin. As a result, however, a good trade-off between the reduction of the bandwidth and of the current consumption has been achieved. Indeed, the opamp bandwidth is half of the original one, while the total current consumption is one quarter.

For all the other integrators, the two-stage Class-A operational amplifier shown in Figure 3.16 has been used. Having even more relaxed gain and bandwidth requirements than the opamp of the first stage, this opamp can achieve a very low current consumption. In order to optimize the efficiency, the differential pair input transistors are biased to work in sub-threshold region, giving the maximum obtainable transconductance with the available current level (50 μA). Moreover, the cascode load decreases the equivalent input capacitance seen from the input, increasing at the same time the phase margin of the

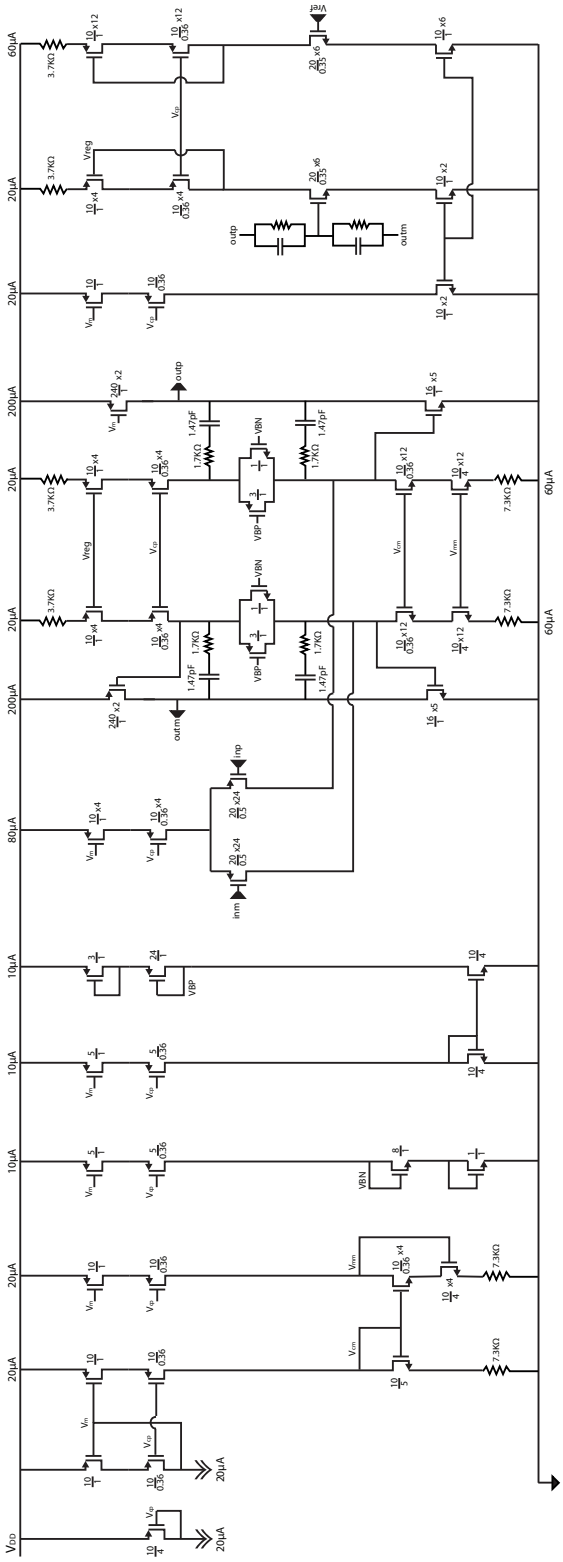

Figure 3.15: Ver. 2 opamp for the first integration stage based on a fully differential Class-AB folded cascode architecture

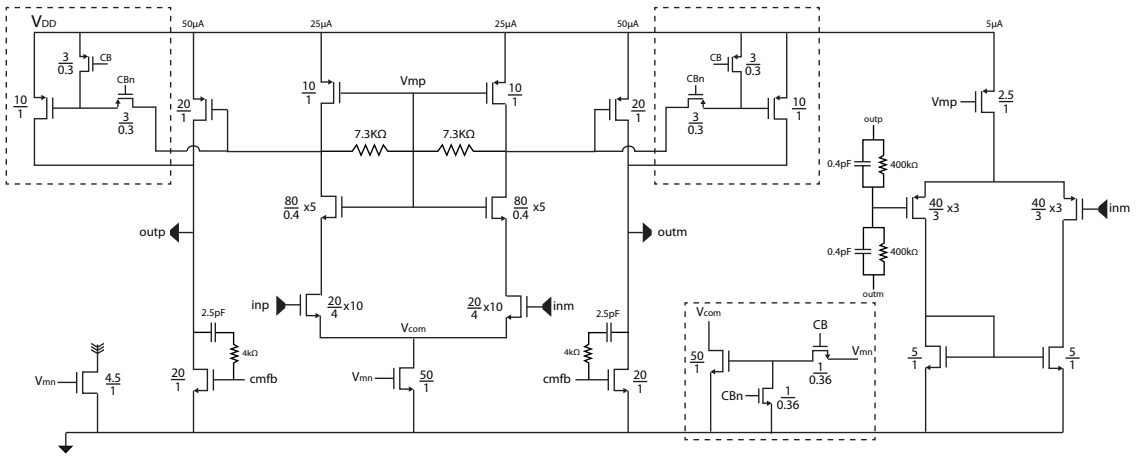

Figure 3.16: Ver. 2 opamp for the second and third integration stages, based on a fully differential Class-A architecture

Opamp	DC Gain [dB]	Phase Margin [°]	f_t [MHz]	Input Referred Noise [µV]	Current [µA]
Old Class-A	120	65	90	1.8	2700
Class-AB	130	60	45	1.8	700
New Class-A	65/80*	55/60*	20/31*	5.9/5.8*	150/400*

Table 3.5: Opamp performance comparison (values with star are with current boost on)

integrator once the feedback loop is closed. A particular solution has been adopted for the third-stage opamp. Indeed, since the third stage is producing the triangle carrier by integration of a square wave, its linearity is quite important. If the power consumption of the opamp is reduced too much, the carrier linearity starts to degrade. Therefore, a selectable current boost (CB) has been added to the third-stage opamp, allowing us to increase the current from 150 µA to 400 µA, thus increasing gain and bandwidth. The CB circuit is shown in Figure 3.16 inside the dotted rectangle.

Table 3.5 reports a comparison between the performance and the current consumption of the two newly designed operational amplifiers with respect to the first-order, first-stage opamp.

3.2.3 Saturation release control

A common requirement for audio amplifiers is that the output has to be driven rail-to-rail. It is customary to specify the maximum output power of an audio amplifiers as the output power level for which distortion becomes 10%, meaning that the output signal is clipping about 40% of the time. Clipping occurs when the input current of the first stage exceed the feedback current through the feedback resistor: in this condition the integrator

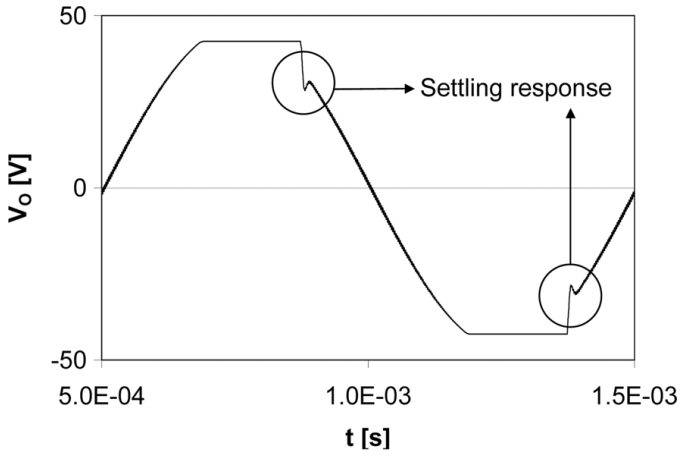

Figure 3.17: Second-order filter "sticking" response

outputs drift away from the normal operating level and reach saturation. When the input current returns to normal levels again, the integrator outputs need some time to return to their normal operating levels and show a transient that depends on the order of the loop filter. Figure 3.17 shows the output signal of a second-order Class-D amplifier during a clipping period. It is possible to note the second-order signal ringing behavior during the saturation release. This saturation recovery transient represents a problem in audio applications because it is clearly audible as a "ticking" noise, different from the "normal" distortion that results from clipping [27].

Many solutions have been developed to avoid this kind of problem and make the saturation release as linear as possible. Being an aspect very correlated to the system architecture, each solution has to be customized in order to limit the problem, while maintaining all the original features of the system under normal operating conditions. Considering that, during saturation, the PWM duty-cycle reaches 100%, a first solution can be the introduction of a logic block that, monitoring the PWM signal, avoids the system clipping by forcing a maximum/minimum PWM duty-cycle in case of saturation. However, in this way, also the maximum output power level is limited, reducing the application field of the amplifier.

Another approach for alleviating saturation recovery transients is reducing the loop filter order. Indeed, the higher is the loop filter order, the more critical and slower is the settling after clipping, due to the "memory" of the system, that stores saturation energy and requires time to resume. By reducing the filter order also the energy stored in the loop is reduced, the saturation release becomes faster, and the output signal behavior shows a limited "sticking" response or does not show it at all.

In our chip Ver. 2 this last approach has been used: a damping resistor is connected in parallel to the second integrator stage feedback capacitor with a switch that transforms the stage in an inverting unitary gain buffer, when saturation is detected, as shown in Figure 3.18. Ideally, the best solution would be to damp all the integrators, transforming

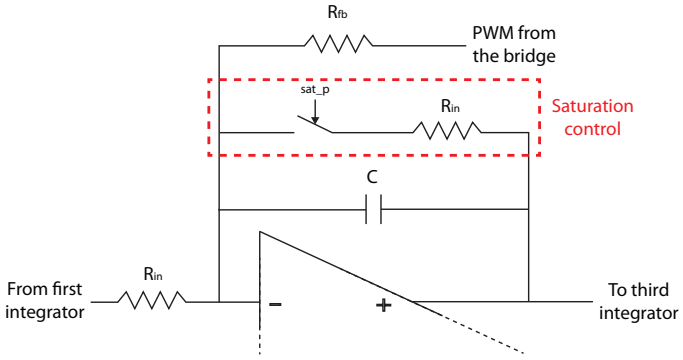

Figure 3.18: Saturation control implementation on the second integrator

them in simple gain stages as soon as the output signal shows clamping. In this way, the system "memory" would be reset, the loop filter order would become zero and all the previous benefits would appear. However, damping the first stage would imply changing the Class-D amplifier input impedance, thus introducing several problems in terms of input signal source compatibility and system stability. Moreover, since the carrier signal flows through the third integrator, it is not possible to damp it without switching off the PWM modulator and, hence, the whole Class-D amplifier. For these reasons, we damped the second stage only, that, thanks to the feed-forward structure adopted in this second version of the chip, has its output close to the common-mode value even when the Class-D output signal is close to saturation.

The implemented control logic block is shown in Figure 3.19. The circuit monitors the state of the PWM signal, checking for the presence of at least one PWM pulse per clock period. During saturation, the duty-cycle of the PWM becomes 100% and PWM pulses are not occurring any longer. Signal sat_p is, therefore, set to one, thus turning on the switches of Figure 3.18.The second integration stage, then, becomes a gain stage and the order of the filter is reduced from third to second. In practice, since we are using a triangular carrier and the PWM pulses are synchronous with the clock edges, two delay flip-flops, triggered on the positive and negative edges of the clock (CK and $\overline{CK}$), respectively, sense and store the PWM value exactly in the middle of each PWM pulse. During normal operation, both flip-flops always see the PWM signal low and, hence, sat_p, being the logic OR of the two flip-flop outputs, is zero. When saturation occurs, depending on the sign of the signal, one of the two flip-flops starts to see a high value and, hence, after a clock period sat_p becomes also high, turning on the switches. One clock cycle after the end of the saturation, sat_p returns low, resuming normal operation.

3.2.4 Simulation results

This second version of the Class-D amplifier is being presently fabricated. Therefore, experimental results are not yet available. However, since the used CMOS 0.18 µm technology is very mature and well modeled, the results obtained in simulation are quite reliable

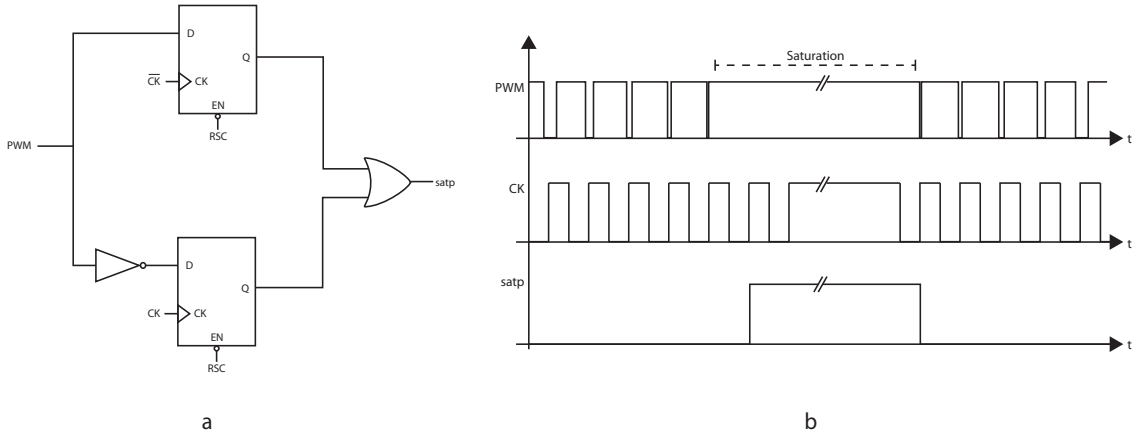

Figure 3.19: Saturation control logic: a – Schematic, b – Signal behavior

and we expect good agreement with the measurements, as for the first version of the chip.

Figure 3.20 shows a comparison between the THD performance of Ver. 1 and Ver. 2 designs, as a function of the input signal level. As it possible to note, in spite of the significative reduction of the opamp current consumption, the THD at low input levels is better in Ver. 2. This is probably due to the added feed-forward paths that, as mentioned, avoids the integration of the input signal in the second stage, eliminating all its non-linearity contributions.

Figure 3.21 shows the behavior in the time domain of integrator and system outputs without (Figure 3.21a) and with (Figure 3.21b) saturation control. As it can be seen, the saturation release causes fewer oscillations with the control system, as expected. Indeed, the sticking problem is strongly reduced. However, as for all the parameters characterizing an audio device, the improvement due to the saturation release control has to be evaluated also by listening to the amplifier play-back, according to subjectivism and psychoacoustic.

Figure 3.22 shows the layout of Ver. 2 Class-D amplifier. Thanks to the area optimization, it was possible to realize a better floor-plan than for Ver. 1. Increasing only the height of the device, while maintaining the layout width constant with respect to the original first-order Class-D amplifier, we realized a complete two-channel stereo system that could be inserted in the original CODEC layout. Realizing a stereo structure at this point is extremely important, since it will then be possible to test the overall system and to evaluate also the crosstalk between the two stereo channels.

3.3 Conclusions

In this chapter, the design and the realization of two different versions of a fully-differential third-order Class-D amplifier have been presented.

The first version of the design (Ver. 1) has been based on an already existing first-order Class-D amplifier with the target of improving the amplifier performance, especially in

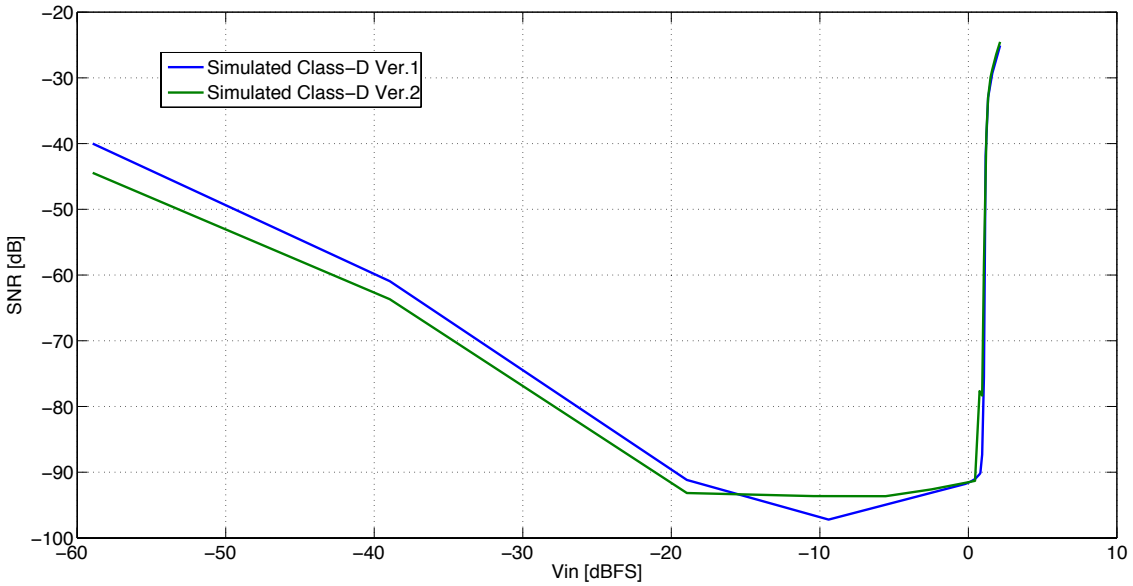

Figure 3.20: Comparison between the THD performance of Ver. 1 and Ver. 2 third-order Class-D amplifiers (input signal full-scale = 1.32 V)

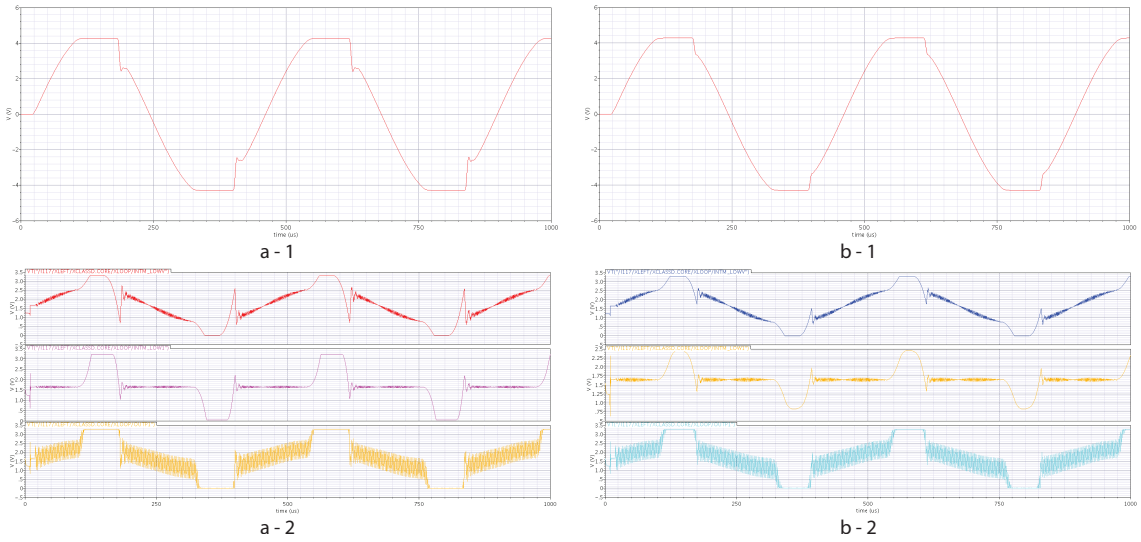

Figure 3.21: Third-order Class-D amplifier outputs: a – Saturation control off, b – Saturation control on; 1 – Main output, 2 – Integrator output

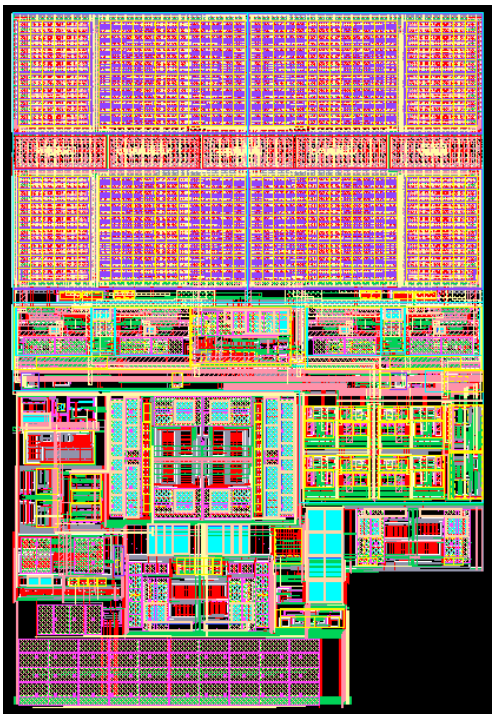

Figure 3.22: Layout of the third-order Class-D amplifier Ver. 2

terms of linearity. Since we wanted to demonstrate that, by increasing the loop filter order, the non-linearity suppression is improved, the first chip design was focused on the loop filter architecture only. Following the methodology presented in Chapter 2 and reusing unchanged all the existing building blocks blocks, we validated the methodology, through a very coherent comparison between the first and the third-order structure, achieving a THD improvement of about 25 dB.

In the second version of the chip (Ver. 2) all the system parameters not considered in the first version, such as efficiency and area, have been optimized along with the building blocks, in order to realize a complete stereo audio chip. By modifying the Ver. 1 loop filter structure and customizing the opamps for each stage, we implemented a very efficient Class-D amplifier, showing a very low THD value.

Chapter 4

Conclusions

Following the strong request from the consumer electronic market of high performance audio devices, in this thesis the modeling, the design and the realization of two different versions of a high linearity Class-D audio amplifier have been presented. Chapter 1 is focused on some general considerations on audio signals and on the main specifications that must be taken in account during the design of an audio system. In Chapter 2, after an overview and a comparison between the main amplifier classes used in audio applications, the Class-D structure has been explained in detail, introducing, in the last part of the chapter, a design methodology for high-order Class-D amplifiers. This methodology, exploiting the similarities between Class-D amplifiers and $\Sigma\Delta$ modulators, easily provides the correct loop filter coefficients for any high-order (larger than one) structure, making the design easier and faster. The methodology has been validated in Chapter 3, where the design and the realization of two fully-differential third-order Class-D amplifiers is reported. The first version of the chip has been realized starting from an already existing fully-differential first-order Class-D amplifier, with the goal of improving the THD performance. Experimental results from the prototype chip show a THD improvement of about 25 dB with respect to the existing design. In the second version of the chip, we optimized all the parameters, such as efficiency and area, that were not considered in the first version. Therefore, we redesigned the loop filter as well as the opamps for each stage, achieving a very efficient Class-D amplifier, showing very low THD. The second version of the chip is presently being fabricated.

Appendix A

Class-D toolbox

During any design activity, modeling is one of the most important parts, since it allows us to verify the performance of the system we are working on using simplified and fast simulations. Moreover it permits to isolate one specific non-ideality and, with the so called parametric simulations, to evaluate how and in which way that non-ideality worsens the behavior of the entire system.

In Chapter 2 a design methodology to implement high-order Class-D amplifiers has been presented. The methodology is based on the observation that $\Sigma\Delta$ modulators are structurally very similar to Class-D amplifiers. Starting from this consideration and imposing few conditions on both the $\Sigma\Delta$ modulators sampling frequency and the bandwidth of the integrators, it is possible to use the well defined $\Sigma\Delta$ modulator theory and toolboxes to design a stable Class-D amplifier. In particular, in this thesis, *DelSig* toolbox and Matlab/Simulink environment have been exploited to calculate stable loop-filter coefficients and ideally characterize the realized structures, respectively. Doing this, many Matlab scripts have been realized and, at the end of the work, the most important have been revised, optimized and grouped in a dedicated toolbox which, implementing the same design methodology, it can help during Class-D amplifier design. A description of this toolbox and of its main functions is reported in this Appendix A.

A.1 Class-D toolbox overview

The implemented Class-D toolbox (CLDTLBX) gives to the user the possibility of easily synthesizing and quickly evaluating at behavioral level a specific Class-D structure, starting from very general specification data. In fact, besides an automatic procedure to generate the Class-D model, the CLDTLBX directly evaluates some of the most important performance parameters for Class-D amplifiers: Total Harmonic Distortion (THD), Power Supply Rejection Ratio (PSRR), Transfer Function (TF) and Signal to Noise Ratio (SNR), thus allowing us to perform a complete characterization of the system under analysis. Once determined the topology of the amplifier and the coefficient values, the CLDTLBX gives also the possibility to calculate the passive component values that have to be used to implement the amplifier using an active *RC* architecture. For each analysis

the toolbox produces spectra and plots of the most important signals, in order to highlight and easily understand the behavior of the amplifier. All these data are also saved in the Matlab workspace, thus allowing any further data processing by the user.

A.1.1 Toolbox library

In order to leave to the designer the maximum flexibility, the toolbox library includes all the blocks used by the toolbox during the automatic generation of the model, plus other blocks modeling the opamp with real components. These blocks can be used by the designer to manually create any other Simulink model that can not be automatically created by the toolbox. The CLDTLBX library is shown in Figure A.1. As it is possible to see, the library is divided in four categories:

- Inputs, carrier and power block;
- CIFB components coefficients values;
- CIFF components coefficients values;
- Real components values.

The first category includes multiple input signal generator, multiple carrier generator and power bridge block, consisting of PWM modulator and SE power bridge. The second and third categories, instead, include all the circuital blocks needed to realize a CIFB and a CIFF loop-filter, respectively, using the *DelSig* toolbox's coefficients, modeling resistors by coefficient ratios. Finally, the fourth category includes actual circuital blocks: this part of the library allows us to model any structure of which the designer already has the components values. This, maybe not very important in a preliminary phase of the design, can be fundamental to understand and fix the problems of an already existent structure.

A.1.2 Model creation

In order to be in line with the market requests, this toolbox was created to deal mainly with filter-less Class-D amplifiers. In this kind of systems the loop filter feedback paths derive directly from the power stage, the output filter is eliminated and the output PWM signal is demodulated by the low-pass filtering action of the speaker. However, once the toolbox finishes the synthesis procedure, every model is saved in the CLDTLBX folder, allowing manual customization by the designer.

Once launched, CLDTLBX will make show the menu reported in Figure A.2. In this menu, the user can introduce the main design specifications that normally have to be satisfied in a Class-D amplifier.

The possibility to introduce the order, the bandwidth, the amplifier gain and the type of loop filter structure, choosing between Cascade of Integrators with Feedforward (CIFF) and Cascade of Integrators with Feedback (CIFB), leaves to the designer a pretty wide flexibility in terms of architecture.

In order to implement the PWM modulation, a carrier generator is inserted in each model just before the comparator: with this first menu the user can choose the carrier signal type (saw-tooth or triangular) and customize it, setting its amplitude and frequency.

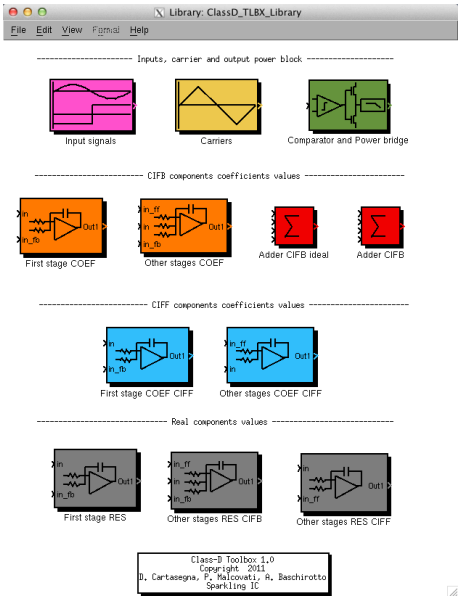

Figure A.1: Class-D toolbox library

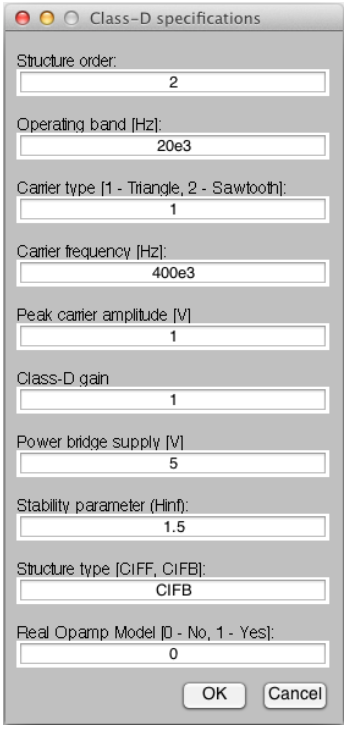

Figure A.2: Specification input menu

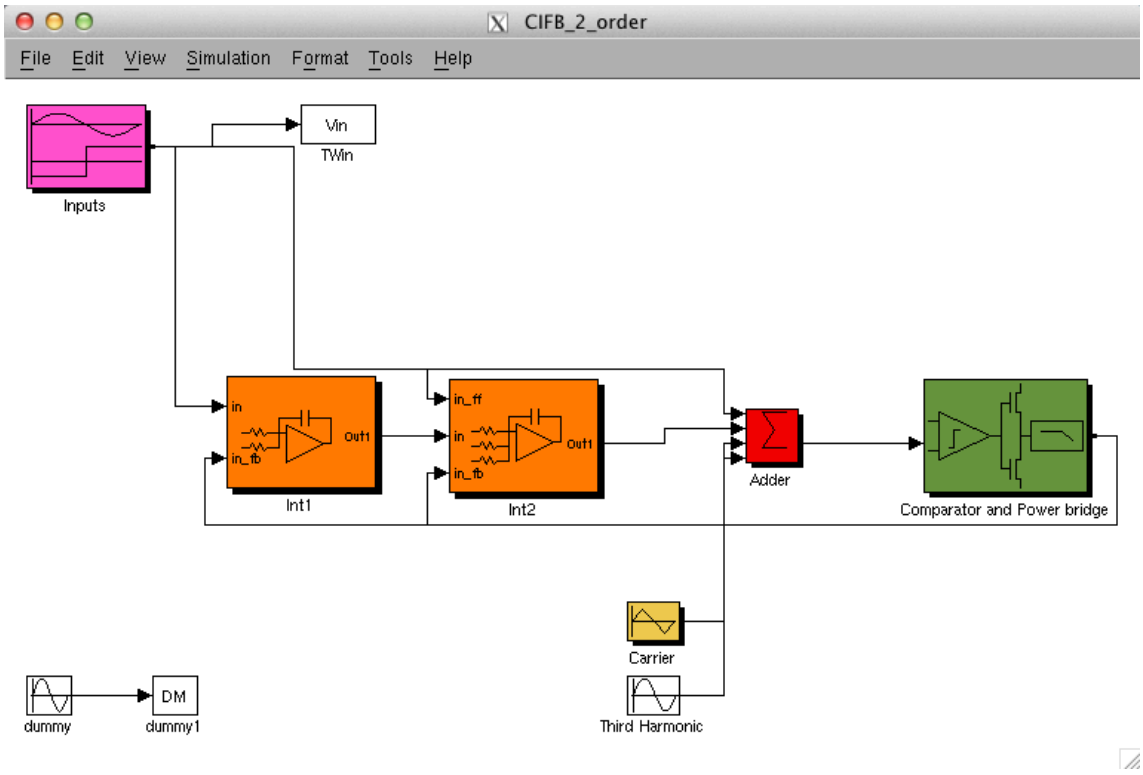

Figure A.3: Example of auto-generated model

Moreover, it is also possible to define the power bridge voltage supply level and the opamp models: the first choice is important to define the feedback signal levels and their effect on the system, while the second one allows us to introduce opamp models which include limited gain-bandwidth product and input referred noise. At least for a preliminary analysis, it is, however, advisable the use of a completely ideal opamp, in order to observe the limitations of the structure under analysis.

The last step is the choice of the output filter: being a square wave generated by a completely ideal continuous-time system, the PWM output signal includes infinite harmonic components. In order to correctly calculate the output signal spectrum, avoiding aliasing, a low-pass filter is needed. The parameters of this filter (filter type, corner frequency, order) can be set using a secondary menu that appears as soon as the toolbox finishes to elaborate the data of the first menu.

Once realized, the model is ready to be analyzed through the simulations present in the main menu. As an example, Figure A.3 shows the model that can be realized using unchanged all the default values present in the menus: it is a second order CIFB Class-D amplifier. Some defaults blocks, such as the 'Third Harmonic' or the 'Dummy Generator' blocks, are added automatically: the user can not avoid the insertion of these blocks, due to their importance during the model simulations, but their nominal values can be set before starting any CLDTLBX analysis.

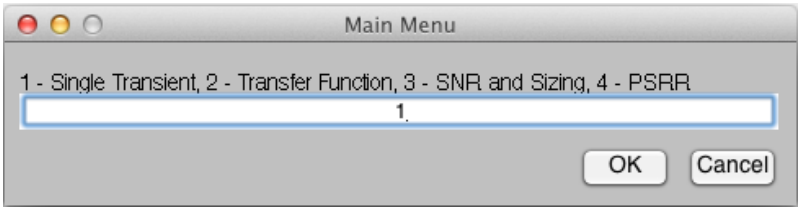

Figure A.4: Main analysis menu

A.1.3 Main analysis menu

The aspect of the main analysis menu is reported in Figure A.4. As it is possible to see, the user can choose between four different analyses:

- Single transient;
- Transfer function;
- SNR and sizing;
- PSRR.

All the analyses are explained here together with input menus and results for the default model of Figure A.3.

Single transient

In single transient analysis, the time-domain behavior of the model can be simulated for a duration specified by the user. Two are the menus to fill-out: the first one, shown in Figure A.5, allows us to set all the input signal parameters, while the second one regards non-idealities and other simulation parameters.

With the first menu it is possible to select and customize all the desired input signals: for each type of signal there is an on/off checkbox and the possibility to set amplitude and frequency. In this way, each signal with the on/off checkbox set on will be present at the system input, giving the possibility to run simulations with single or multiple inputs. For example, it is possible to simulate the model stimulating the system with only a single sine wave simply by setting on the "Sinusoid input signal" checkbox and leaving all the other checkboxes off. If the desired input signal is instead a couple of tones, it is necessary to set on also the "Second tone input" checkbox.

The last checkbox is dedicated to the insertion of a custom input file: in order to simulate with this input signal type, the user has to load the specific data file in the workspace by a dedicated menu that appears after the first menu is completed, only if the "Custom input" checkbox is set to on. The format of this file must be a two column data array, in which the first column represents the sampling instants while the other represents the sample amplitude of the desired input.

With the second menu it is possible to set some system non-idealities, such as carrier non-linearity, third-harmonic distortion, power bridge delay time and noise. In particular, it is possible to change the frequency, the amplitude and the type of carrier that was

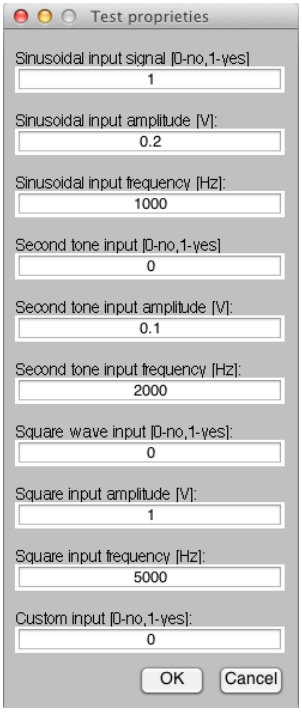

Figure A.5: Transient analysis – Input settings menu

already set in the main menu of the toolbox. This is not a redundant procedure, but derives from the recursive structure of CLDTLBX: the toolbox allows us to change also some fundamental filter parameters, in order to simulate the behavior of the amplifier under different working conditions, without exiting from the toolbox routine. Therefore, it can happen that doing two different analyses on the same model, the toolbox asks to set the same variables more than once. However, the variable value, once inserted, remains unchanged until the next user variation and will be reported as default value in every successive analysis menu.

The third harmonic parameter is the amplitude of the third harmonic generator added in front of the PWM modulator, as shown in Figure A.3, while delay time of the power bridge is intended as the time that elapses between the commutation of the PWM modulator and the proper setting of the output/feedback signal. These two parameters allow us to monitor the system THD, while varying the loop-filter coefficients.

The noise simulation on/off checkbox enables all the thermal noise sources that would be present in the real version of the modeled system, allowing us to analyze the SNR of the structure. However, this kind of simulation can be run only after the third toolbox analysis (SNR and sizing), when the real component values have been already determined.

The other parameters in this menu are the duration of the transient, the simulation time-step and the integration band for the THD calculation. This last parameter can also be different from the system bandwidt. The time-step has to be selected carefully: the

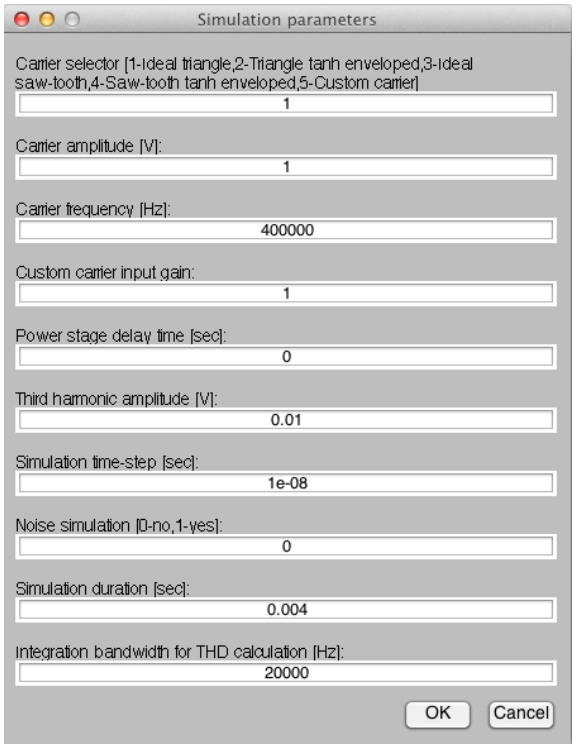

Figure A.6: Transient analysis – Non-idealities menu

larger is the time-step, the shorter is the simulation, but the worse is the achieved accuracy. Therefore, a trade off between these two aspects has to be considered.

After the analysis, the CLDTLBX processes the acquired data for input, PWM and filtered output signals and shows their spectra together with the used output filter transfer function, as reported in Figure A.7. Here a transient signal with a single tone as input and 10% of third-harmonic distortion has been used. As can be seen, printed on the filtered output spectrum there is the THD value relative to the ratio between the input signal and the spurious harmonic power. Moreover, the time-domain data of input, PWM and filtered PWM are saved in the Matlab workspace and available for plotting or further processing.

Transfer function

The transfer function analysis allows us to evaluate the transfer function of the modeled Class-D amplifier. The requested parameters are reported in the menu shown in Figure A.8. Besides the input signal amplitude, the simulation time-step, the THD integration band and some non-idealities, as in the single transient simulation, here the analysis bandwidth can be set, choosing the start and the stop input frequency values. Simulation frequencies are obtained dividing the analysis band by the number of points desired by the user. The division is done in a logarithmic way.

During this analysis the toolbox runs a number of single transient simulations equal to

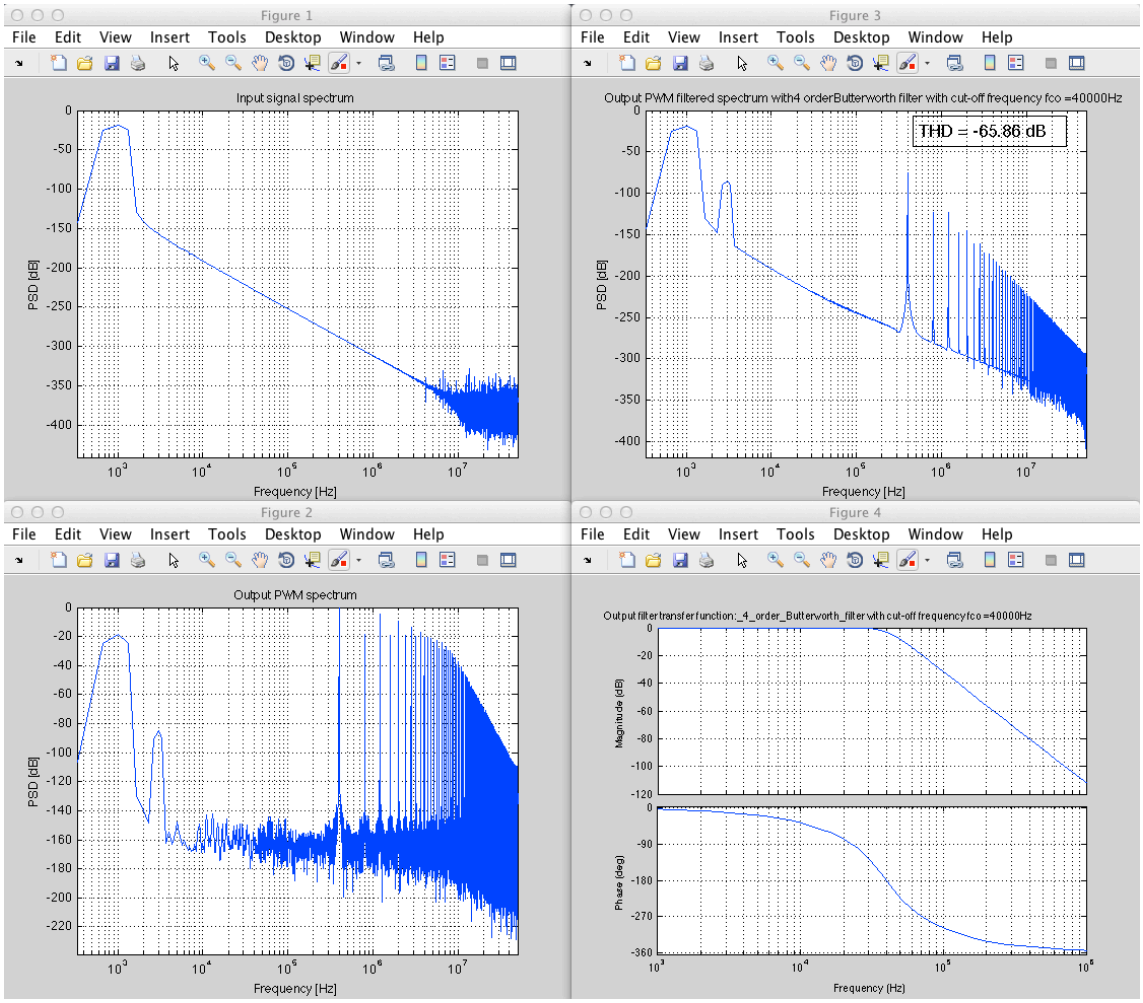

Figure A.7: Transient analysis – Output signal spectra

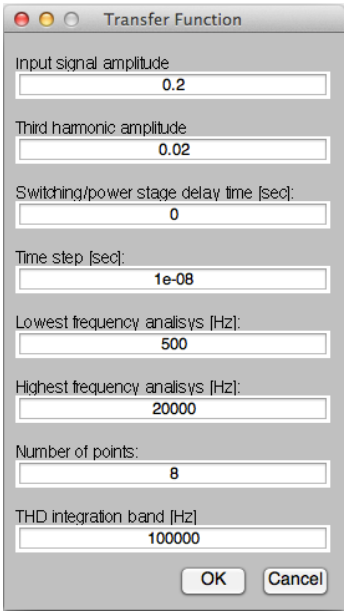

Figure A.8: Transfer function analysis – Input settings menu

the number of points of the transient response curve set by the user. For each simulation SNR and Class-D amplifier gain are calculated and saved in a matrix.

Since it is running a series of single transient simulations, this analysis can take a long time, especially choosing an analysis band which starts at low frequency (e. g. audio band 20 Hz - 20 kHz): the lower is the starting frequency of the analysis band and the longer the first simulations will be, in order to calculate correctly and with a consistent number of points the output signal spectrum for each simulation.

At the end of the simulations all the output data are processed and the two curves reported in Figure A.9 are plotted. The first one represents the amplifier transfer function in the band specified by the user, while the second one reports the THD as a function of the input signal frequency in the same range. In the example is possible to see the starting point of the second order CIFB structure low-pass filtering response and its SNR behavior considering a third harmonic distortion of 10% with respect to the input signal.

SNR and sizing

The SNR and sizing analysis can be done following two different paths:

- Evaluation of amplifier SNR from the calculated amplifier real component values;
- Definition of the first stage real component values starting from a SNR imposed by the user.

In the first case the user can choose to set one value between R and C as default parameter. From that value the toolbox will define all the real component values, starting from the integrator bandwidth, chosen as explained in Chapter 2, and the coefficients obtained from

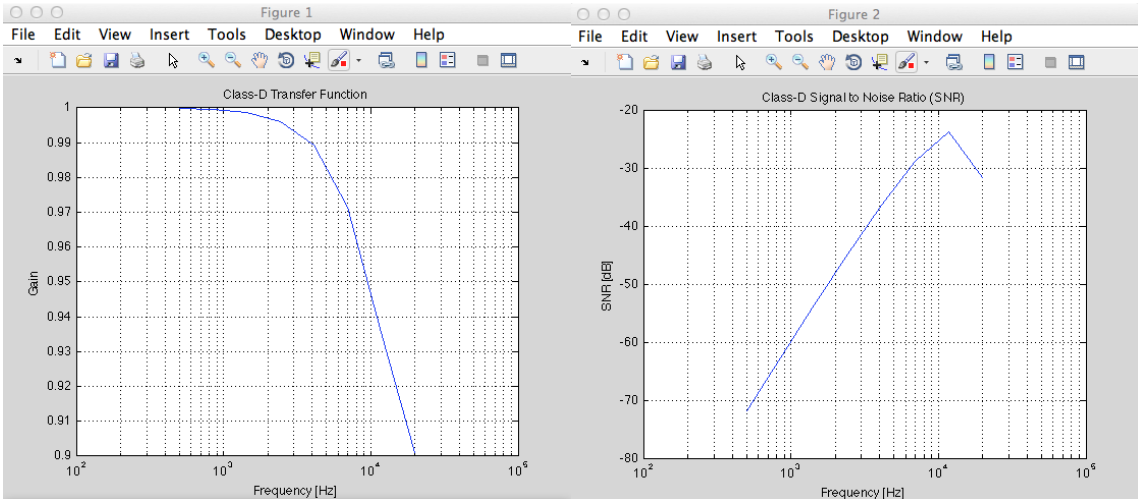

Figure A.9: Transfer function analysis – Output data: transfer function and THD vs. frequency

the *DelSig* toolbox. In this way no optimization is done and the SNR can be very poor, especially using CIFB structures.

In the second case, instead, the first stage sizing, that is normally the most critical in terms of noise, is obtained allowing the user to impose the desired SNR value and then calculating the component values accordingly. The component values for the stages after the first are determined as in the previous case. The results are saved in a matrix (RES) and plotted in the Matlab Command Window.

At the end of this analysis the toolbox automatically asks the permission to run a single transient simulation including the thermal noise components deriving from the calculated component values. Once terminated this operation, the usual results of a single transient simulation will be plotted on the screen (Figure A.10) and the toolbox will return to the main menu.

PSRR

Having the power bridge directly connected to the load, also when considering closed-loop structures, the noise present on the supply voltage can heavily affect the Class-D amplifier output signal behavior. Therefore, it is quite important to analyze the Power Supply Rejection Ratio during Class-D amplifier design. CLDTLBX toolbox faces this aspect in two different ways:

- PSRR transfer function;
- PSRR single transient.

In the first case, a number of single transient simulations set by the user are run as in the transfer function analysis. In this case the input signal of the system is set to zero and a tone is instead inserted on the voltage supply of the power bridge. Varying the

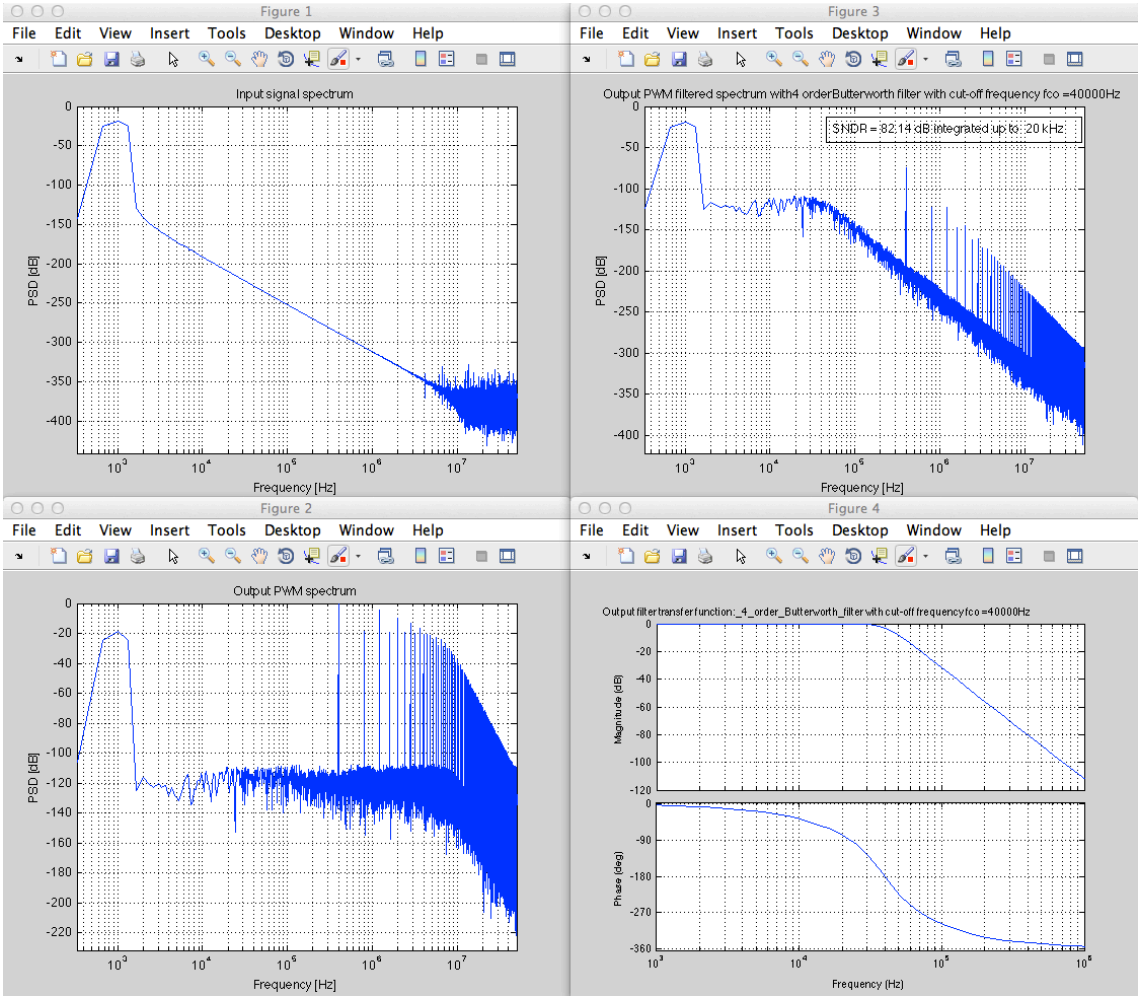

Figure A.10: SNR and sizing – Output data

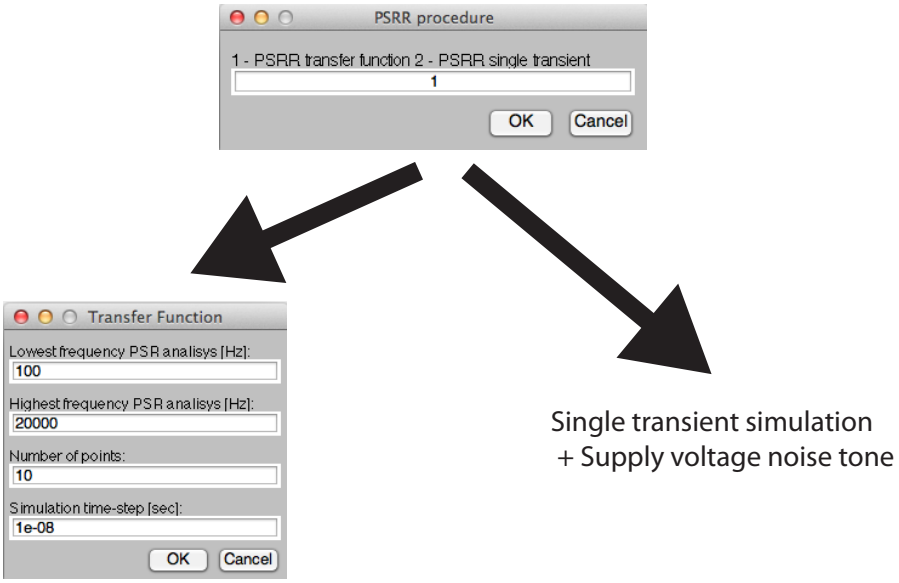

Figure A.11: PSRR analysis – Input settings menu

frequency of the tone, the trend of the supply noise attenuation with respect to frequency can be evaluated. The second case allows us to run a simulation including both the input signal and the supply noise tone, in order to evaluate the general behavior of the system including potential intermodulations. The PSRR input menu is reported in Figure A.11.

As an example, Figure A.12 reports the output spectrum of the usual default second order CIFB Class-D amplifier, stimulated by a sine wave with an amplitude of 200 mV and a frequency equal to 1 kHz at the amplifier input and a tone at 400 Hz with an amplitude of 600 mV added to the power bridge voltage supply. The value of the PSRR is reported on the filtered output spectrum in which both the signals (input and power supply noise) are plotted.

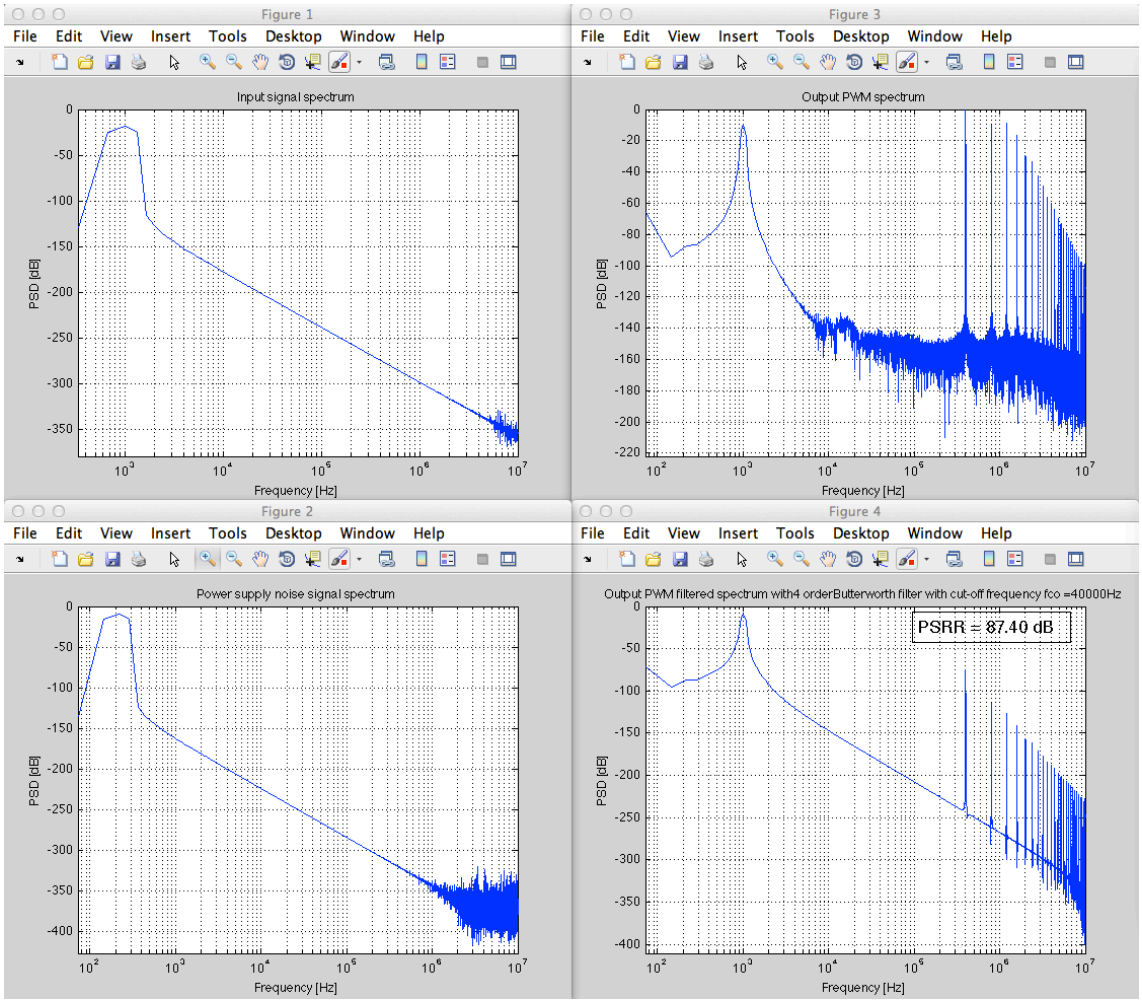

Figure A.12: PSRR analysis – Output data

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