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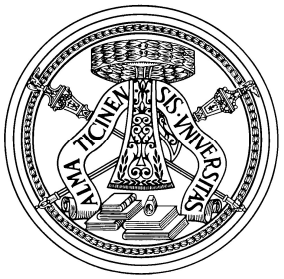

Ph.D. Thesis in Microelectronics
XXVI Cycle

Adaptive Transmitters for Mobile Communications

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Introduction

The role of the back-end of a transceiver is to transmit a very large signal (compared to a received one), localized in a precise frequency range and it must not interfere with other communication channels, unrelated to the transmitted one, but surrounding it in the frequency domain. In fact, since the world is analog and not digital, it is not possible to make the signal power drop to zero beyond the defined channel, but some out-of-band emission will leak in other bandwidth channels. The risk is corrupting other signal's reception and recovery.

In particular, the risk is more higher for the receiver (RX) that is integrated on the same chip of the transmitter (TX) and is working in a Frequency Division Duplex (FDD) mode: the TX out-of-band leakage is directly coupled to the RX path through the duplexer attenuation, corrupting the received signal. Hence, this leakage must be very low, since the attenuation is not infinite.

In traditional implementations, the out-of-band emission was lowered through the use of an external, expensive and bulky SAW (Surface Acoustic Wave) Filter placed between the integrated transceiver and the external Power Amplifier that drives the duplexer before the antenna. However, during the years, reasearch efforts in TX design and CMOS technology improvements were able to eliminate the use of the SAW filter in the 2G, 2.5G and 3G standards.

The introduction of the LTE 4G standard has again raised the need to reuse the SAW filters to counteract the worsening of out-of-band performances due to the enlargement of the Radio Frequency (RF) signal bandwidths and, hence, the reduction of the frequency distances between the RX and the TX channel (RX-TX frequency offset). Besides the larger bandwidths, the power consumption necessary to process the signal has also become more demanding in 4G, being a crucial problem for devices that are supposed to run on battery.

To solve the power consumption problem, we have to concentrate the efforts in the analog section of the transmitter, since it is the one that delivers the actual transmitted power to the antenna. Moreover, since out-of-band emission is intrinsically an analog issue, it's the analog section that must be optimized to lower this leakage. In this Thesis, the design of baseband sections for multistandard transmitters has been investigated.

In Chapter 1, a general overview of the new standard LTE is given, together with considerations about the out-of-band emission and contributors. An overview of recent multistandard transmitters from the State-of-the-Art closes the Chapter.

In Chapter 2, an improvement in terms of power consumption is given by a Class A/B approach in the active mixer of a transmitter working in voltage and current domain. The basic building blocks and design guidelines are described from a high-level point of view and the measurements of a realized prototype are discussed at the end of the Chapter.

In Chapter 3, a complete baseband working with a current approach from the DAC to the upconversion is described. The architecture and design of the main building blocks are highlighted. The last part of the Chapter is dedicated to the prototyping and measurements of the transmitter.

In Chapter 4, the benefits of pushing toward the theoretical limit the transmitter's building blocks is explained and demonstrated through simulations on two proposed "minimal" transmitters, oriented toward a $28nm$ and $55nm$ CMOS technology, working both entirely in Class A/B from the DAC to the upconversion.

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Chapter 1

State-of-the-Art of Transmitters for Mobile Communications

The introduction of the new standard LTE for mobile communications, besides 2G and 3G, needs an improvement on many performances of modern transceivers. In this first Chapter, a basic description of the features of the 4G standard is given, together with the challenging aspects and the introduced issues. The characteristics of modern integrated transmitters for mobile applications and their design are then discussed, focusing in particular on the problem of out-of-band emission when removing the external SAW filter placed before the external Power Amplifier. An overview of the major contributors to out-of-band emission is stated, along with the key figure of merit describing linearity, modulation accuracy and noise in transmitters. Finally, a summary of the State-of-the-Art of transmitters for mobile communications closes the Chapter.

1.1 An introduction to the Long-Term Evolution

The Long-Term Evolution, marked as 4G LTE, is the new standard for wireless communication of high-speed data for mobile phones and data terminals [1, 2]. Based on the GSM/EDGE and UMTS/HSPA network technologies, it increases the capacity and speed using a different radio interface together with enhancements in the core network. The standard has been developed by the 3GPP (3^{rd} Generation Partnership Project) like the previous standards and it is fully specified in his Release 8 documents.

LTE Release 8 was frozen in December 2008 and it has been the basis for the first wave of LTE equipment. The specifications are very stable and the motivations for the introduction of the new standard have been several:

- the need to ensure the continuity of competitiveness of the 3G system for the future;
- higher data rates and quality of service needed by the user;
- optimization of the Packet Switch system;
- cost reduction of the devices and services;
- the need for low complexity.

1.1.1 LTE Overview

The access part of LTE (or the E-UTRAN, Evolved Universal Terrestrial Access Network) is called the Evolved Packet System (EPS). High spectral efficiency, high peak data rates, short round trip time and frequency flexibility are the new and main requirements for the EPS.

During the '90s, GSM was studied to carry real time services, with data services only possible over a circuit switched modem connection, with very low data rates. The first step towards an IP based packet switched solution was made with the evolution from GSM to GPRS, using the same air interface and access method, TDMA (Time Division Multiple Access).

Finally, the Universal Mobile Telecommunications System (UMTS) was developed with a new access network, based on CDMA (Code Division Multiple Access), to reach higher data rates and data volume. The circuit switched connection and a packet switched connection for datacom services are emulated in the access network in UMTS for real time services. Moreover, the IP address is allocated when a datacom service is established and released when the service is released. However, incoming datacom services are still relying upon the circuit switched core for paging.

The core network is also prepared to be compatible with other access technologies not introduced by 3GPP, like WiMAX and WiFi. Non-3GPP developed access solutions are separeted in trusted and non-trusted: this division is not based merely on the technical solution, but only on the business relation/agreement between the operators.

The new Evolved Packet System is purely IP based: real time services and datacom services are carried by the IP protocol. The IP address is allocated when the mobile is switched on and released when switched off. LTE is able to reach even higher data rates and data volumes compared to the previous standards. High order modulation (up to 64QAM), large bandwidth (up to $20MHz$, starting from $1.4MHz$) and Multiple Input Multiple Output (MIMO) transmission in the downlink is also a part of the solution. The highest theoretical data rate is $170Mbps$ in uplink and, with MIMO approach, the rate can reach $300Mbps$ in the downlink.

The 3GPP chose a multicarrier approach for multiple access to achieve very high spectral efficiency. Orthogonal Frequency Division Multiple Access (OFDMA) was selected for the downlink. OFDM, a multicarrier technology that subdivides the available signal bandwidth into many mutual orthogonal narrowband subcarriers, also shares these subcarriers with multiple users. With this solution, it is possible to exploit variations in both frequency and time domains, achieving very high spectral efficiency, but requiring fast processors. Furthermore, OFDMA solution leads to high Peak-to-Average Power Ratio (PAR), up to $9dB$, requiring expensive and demanding power amplifiers with severe requirements on linearity, increasing the battery consumption. This would lead to very expensive handsets. To compensate for these problems, the uplink of LTE uses OFDMA and the Single-Carrier Frequency-Division Multiple Access (SC-FDMA), a precoded version of OFDM, also known as Discrete Fourier Transform (DFT) spread OFDMA, depending on the channel.

To allow possible deployment around the globe and to support as many regulatory requirements as possible, LTE is developed for many frequency bands, ranging from $800MHz$ up to $3.5GHz$ and numbered from Band1 to Band44. The available bandwidths are also very flexible, starting with $1.4MHz$ up to $20MHz$. As an example, in Fig. 1.1 is reported an RF LTE20 spectrum, taken from a spectrum analyzer. As we can see, the bandwidth is very well defined ($20MHz$) and the signal power is flat inside the band.

LTE supports both Frequency-division duplex (FDD) and Time-division duplex (TDD) modes: FDD uses paired spectra for uplink and downlink transmission separated by a duplex frequency gap and TDD separates one frequency carrier into alternating time periods for transmission from the base stations to the terminals and viceversa. The two modes have their own frame structure and these are aligned with each other, i.e. similar hardware can be used in the base stations and terminals to allow the scaling-down approach. These days, a single chipset can support both TDD-LTE and FDD-LTE operating modes.

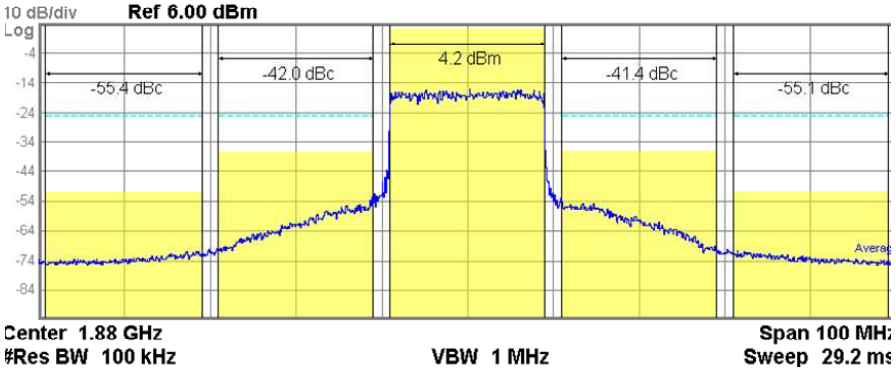

FIGURE 1.1: *LTE20 signal spectrum, taken from a Spectrum Analyzer.*

In the time domain, the LTE transmission is structured in radio frames. Each of these radio frames is $10ms$ long and consists of 10 subframes of $1ms$ each. In the frequency domain, the OFDM subcarrier spacing is $15kHz$. Twelve of these subcarriers together are called a Resource Block (RB): e.g., LTE10 full spectrum consists of 50 RB while LTE20 of 100 RB. However, in the downlink or uplink channel a minimum of 1 Resource Block during 1 subframe can be allocated.

Given that LTE provides high spectral efficiency with high data rates and a flexible access architecture, it will become a success among operators as well as customers.

1.2 Out-of-Band emission and modern transmitter parameters

1.2.1 General considerations

Integrated terminals for the new standard 4G are very demanding, since they also have to be compatible with all the pre-existing communication standards and, moreover, with many other wireless standards (WiMAX, WLAN, GPS etc...): nowadays, this is the trend in smartphone design. The most critical situation of coexistance is always the one of a receiver and a transmitter that are working in a FDD operation on the same mobile device. In fact, if we look to a typical mask of interferers for mobile communications FDD standards when designing a front-end, we can see that one of the most critical interferer is given from the transmitter itself.

3G and 4G standards, that require receiver (RX) and transmitter (TX) working at the same time on different bands, suffer from this issue. A partial isolation between the two paths is given by the duplexer: the two inputs have different passband transfer functions toward the ouput, so the RX and the TX can work at the same time, while the path between them is isolated. This property protect the most sensitive part of a transceiver, i.e. the analog front-end, from the emission in the RX signal band coming from the transmitter. Anyway, the isolation is not infinite, and leakage from the transmitter propagates in the RX-path.

There are two type of problem arising from this leakage and, with the use of large signal bandwidths as the ones of the 4G, these problems become even more critical:

- linearity: the wanted small received signal has to cohabitate with many interferers and the biggest one is coming from the transmitter itself, even if attenuated: the analog processing of the RX-path can create non-linearities and intermodulations that can fall in the received bandwidth, corrupting the wanted signal or saturating the receiver. Dealing with these interferences issues is, however, the duty of the receiver;
- out-of-band emission (see Fig. 1.2) : the transmitted signal and his leakage will be attenuated by the duplexer, but the leakage residuals that lie in the RX-band directly impact the performances of the receiver, since it is added

to the noise floor given from the the antenna and the noise figure. Moreover, out-of-band noise is also an important concern for coexistence of cellular transmitters with standards like GPS, WLAN and/or WiMAX on the same smartphone, a very common scenario nowadays. Finally, attention must be paid also to linearity issues (i.e. out-of-band intermodulations) that can impact other radio systems around the device.

This last problem is traditionally resolved using a SAW filter at the ouput of the integrated transmitter and before the Power Amplifier (PA) as shown in Fig. 1.2. The drawback is that the SAW filter is a bulky, external and expensive element on the cellular phone board. Furthermore, among the 44 working Bands mentioned before, each SAW filter can handle only some of them since they are manufactured to be effective only for narrowbands: hence, many of them, centered at different frequencies, are placed on the board.

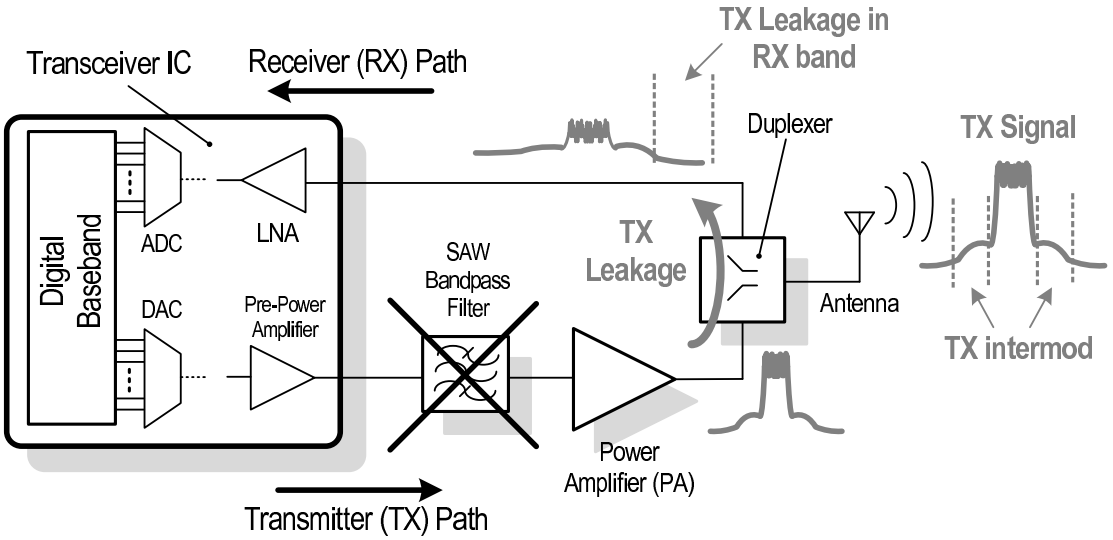

FIGURE 1.2: *A typical block diagram of a transceiver.*

Nowadays, since the mobile hand-set must move toward an entire reconfigurable and integrated radio transceiver, the trend is to eliminate this blocks, not reconfigurable and not integrable: with this goal, the transmitter must provide a very low out-of-band emission. In fact, with the 3G, it was possible to eliminate the SAW filters. However, the introduction of LTE forced the designers to re-introduce the SAW filter for some critical working bands, where the signal bandwidth is large and hence the frequency distance between the RX-band and the TX-band is very small. Beside the issues with the receiver, the low emissions are also necessary

because the transmitted signal must cohabitate with other standards that exist at other frequencies without interfere with them.

Three elements coming from the baseband of a transmitter are the principal contributors to the out-of-band emission: the DAC replicas, out-of-band noise and non-linearity. In the following sections, we're gonna discuss these elements and, in general, the main parameters of a transmitter for mobile communications.

1.2.2 DAC Replicas

The analog section of a transceiver is the part that interface the signal with the world. The baseband processing of the signal is, instead, entirely digital. Hence, an Analog to Digital Converter (ADC) is necessary in the receiver chain while a Digital to Analog Converter (DAC) is the interface of the transmitter chain (see Fig. 1.2).

In the transmitter, the band-limited signal $x(t)$ with spectral components beyond a frequency f_{max} equal to zero (like the one in Fig. 1.3) can be completely reconstructed from a set of uniformely spaced discrete-time samples, given from the digital baseband to the DAC, if the samples are taken with a sampling rate f_s,

$$f_s \geq 2f_{max}. \tag{1.1}$$

This is known as the uniform sampling theorem and the sampling rate $f_s = 2f_{max}$ is called the Nyquist rate [4].

Suppose an analog waveform $x(t)$ with a Fourier Transform $X(f)$ equal to zero for $|f| > f_{max}$ (Fig. 1.3) and sampled in the time domain. Ideally, sampling $x(t)$

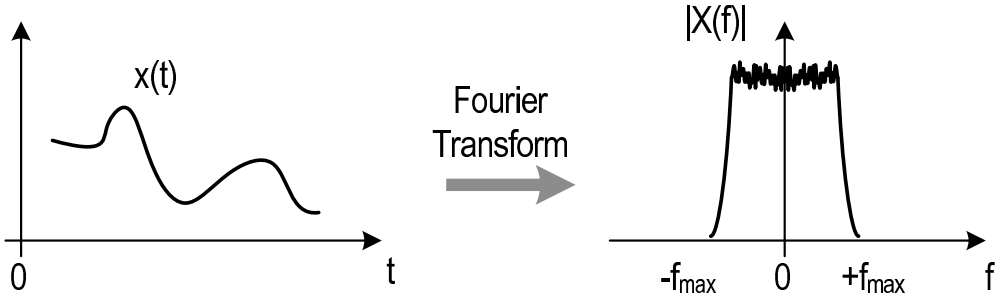

FIGURE 1.3: *A time-domain signal $x(t)$ and his Fourier Transform $X(f)$ in the frequency domain.*

means taking the product of $x(t)$ with a periodic train of impulse functions $x_\delta(t)$, defined as

$$x_\delta(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT_s), \tag{1.2}$$

where $T_s = 1/f_s$ is the sampling period and $\delta(t)$ is the Dirac delta function [3]. In Fig. 1.4 is reported the sampled version of $x(t)$, denoted as $x_s(t)$. It can be expressed as

$$x_s(t) = x(t)x_\delta(t) = \sum_{n=-\infty}^{+\infty} x(t)\delta(t - nT_s) = \sum_{n=-\infty}^{+\infty} x(nT_s)\delta(t - nT_s). \tag{1.3}$$

The signal spectrum of $x_s(t)$ can be obtained from Eq. 1.3. In fact, using convolution [3], the Fourier transform of the sampled signal $X_s(f)$ can be rewritten as the convolution of X_f and the Fourier transform of $x_\delta(t)$ ($X_\delta(f)$):

$$X_s(f) = X(f) * X_\delta(f) = X(f) * \left[\frac{1}{T}\sum_{n=-\infty}^{+\infty} \delta(f - nf_s)\right] = \frac{1}{T}\sum_{n=-\infty}^{+\infty} X(f - nf_s), \tag{1.4}$$

using the frequency domain form of the impulse train:

$$X_\delta(f) = \frac{1}{T_s}\sum_{n=-\infty}^{+\infty} \delta(f - nf_s). \tag{1.5}$$

The spectrum $X_s(f)$ of $x_s(t)$ is exactly the same as X_f of the original signal $x(t)$, to within a constant factor $(1/T_s)$. Moreover, the spectrum repeats itself in frequency every f_s, as depicted in Fig. 1.4.

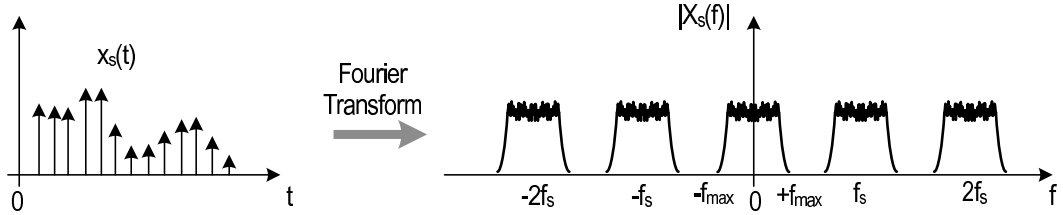

FIGURE 1.4: *Signal $x(t)$ sampled in the time-domain and his spectrum.*

A real DAC is not able to provide ideal impulses at his output. In fact, his output can be seen as an impulse followed by a sample and hold that keeps the value of the impulse for a period of T_s. The mathematical representation is the convolution of the sampled impulse train $x(t)x_\delta(t)$ with a unity amplitude rectangular pulse

$p(t)$ of width T_s:

$$x_s(t) = p(t) * [x(t)x_\delta(t)] = p(t) * \left[x(t) \sum_{n=-\infty}^{+\infty} \delta(t - nT_s) \right]. \tag{1.6}$$

This results in the function represented in Fig. 1.5. His Fourier transform is the product of the Fourier transform $P(f)$ of the rectangular pulse and the spectrum of the impulse sampled sequence:

$$X_s(f) = P(f)\frac{1}{T_s} \sum_{n=-\infty}^{+\infty} X(f - nf_s), \tag{1.7}$$

where $P(f)$ is the cardinal sinus $P(f) = T_s sinc(fT_s)$. As we can see in Fig. 1.5, the signal replicas at multiples of the sampling frequencies are now filtered through a sinc function.

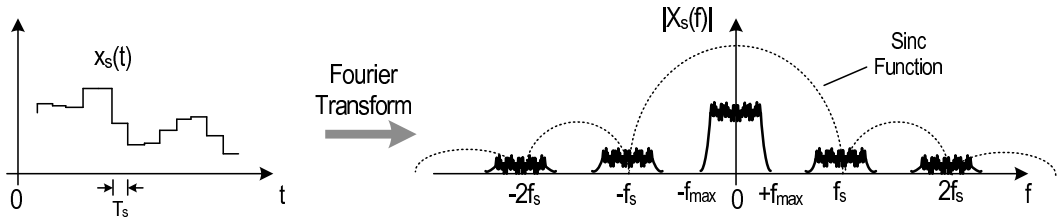

FIGURE 1.5: *Output signal of a real DAC and his spectrum*

However, this filtering is usually not sufficient, since the replicas could fall, when transmitted, in other bandwidth where other standards are or where the receiver (integrated on the same chip) is working. Of course, increasing the DAC sampling rate f_s would push the replicas at higher frequency, but at power consumption costs.

Hence, the usual strategy in transmitter chains is to insert a filtering block (usually with high-order) that eliminate the DAC replicas and it is traditionally place right after the converter.

1.2.3 Out-of-band noise

While in receivers the in-band noise is an issue, in transmitters is the noise out-of-band. We already mentioned that the high-frequency noise leakage of the transmitter passes through the duplexer into the RX-band and can degrade the performances of the receiver. Of course, since there are many operating bands with different TX-RX frequency offsets, the worse situations will be where the offset is small and when the bandwidth of the signal is large (the bandwidth of the noise will be large too, since it depends on the signal processed).

The traditional strategy was to put a SAW filter before the Power Amplifier (PA) to eliminate this leakage, but nowadays the trend is to eliminate these SAW blocks to save costs. Hence, the transmitter must be very low-noise and this could be achieved by changing the structure and optimizing the filtering in the TX chain. For example, a filter is already implemented to attenuate the DAC replicas, but it eliminates also the out-of-band-noise coming from the DAC, since it contributes with thermal noise and with quantization noise. The filter could be useful also to eliminate the high-frequency noise coming not only from the DAC but also from the entire baseband chain. Typically, beside the filtering block already introduced for the DAC replicas and noise, another filtering block is added expecially for out-of-band noise of the other blocks.

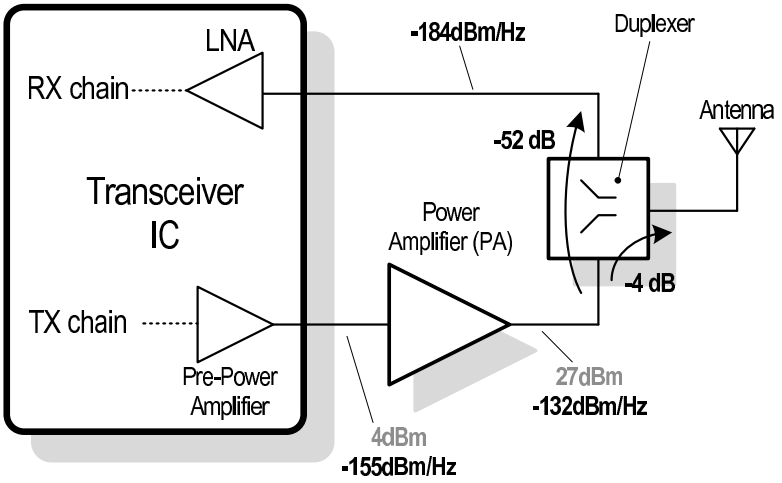

FIGURE 1.6: *Numerical example of out-of-band noise requirement calculations for a transmitter.*

An example of the calculation of the requirement for the out-of band noise is given in Fig. 1.6. The noise floor of a receiver, supposing matched input impedance, is given by

$$10Log\left(\frac{kTR_a}{50\Omega \cdot 1mW}\right) = -174dBm/Hz, \tag{1.8}$$

where k is the Boltzmann constant, T the room temperature in Kelvin and R_a the antenna resistance ($= 50\Omega$). Supposing that the transmitter leakage must not contribute too much to this noise, his level will be $10dB$ lower, i.e. $-184dBm/Hz$. Supposing, moreover, that the duplexer has an attenuation from TX to RX of $-52dB$ and that the Power Amplifier gain is $+23dB$, we get that the required out-of-band noise for the transmitter is $-155dBm/Hz$ when the pre-power amplifier in the IC is emitting $4dBm$. The measurement of this parameter is made with respect to the carrier of the transmitted signal, hence as a signal-to-noise ratio (SNR): the requirement for the transmitter is a SNR of $-159dBc/Hz$.

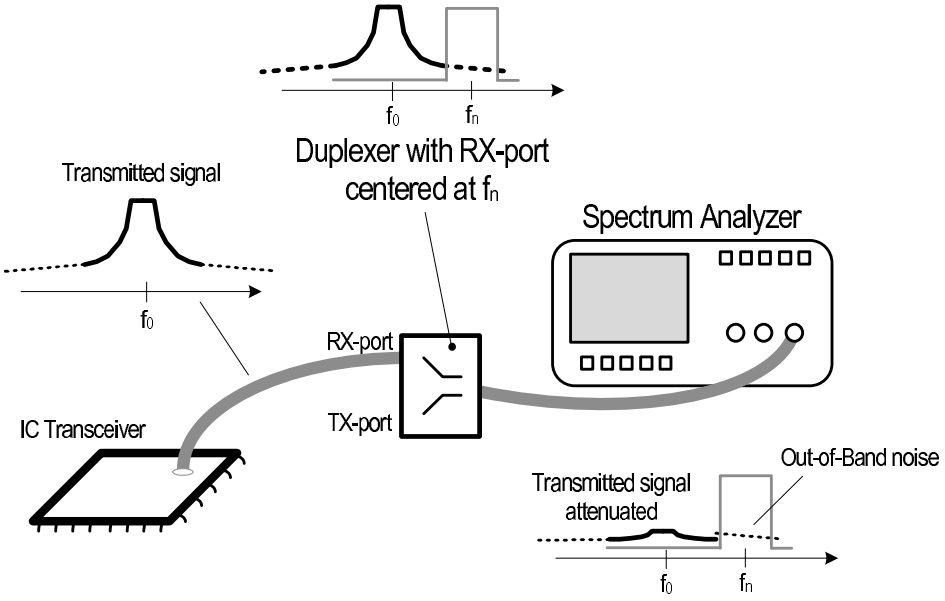

FIGURE 1.7: *Out-of-band noise meaurements testbench.*

When measuring the noise performances of an integrated transmitter, the usual procedure is the following: the RF output is connected to a spectrum analyzer through the duplexer RX-port accorded to the signal carrier. Hence, the stop-band of the duplexer attenuates the transmitted signal, while the noise in the RX-band will pass unchanged (except for the insertion loss) and it can be measured without saturating the spectrum analyzer with the huge transmitted signal.

The procedure is described in Fig. 1.7. The noise is calculated as an integral in the RX-bandwidth and an equivalent noise density is extracted (in dBm/Hz).

Then, moving the IC output probe in the TX-port of the duplexer, it is possible to measure the transmitted power and hence the Signal-to-Noise Ratio (in dBc/Hz).

The 3GPP usually provides specific situations for the noise measurements. For what concerns 3G, the measure is done using the usual signal, occupying a $3.84MHz$ RF bandwidth. For the 4G, where the signals have a bandwidth more large, the signal used for the test is made of partial Resource Blocks (RBs) instead of the full signal: the number of the used RBs depends on the TX-RX offset. The RBs are positioned on the side of the measured noise. An example of partial signal is reported in the spectrum analyzer screenshots of Fig. 1.8, on top: specifically, it's the signal used for noise measurements for LTE20 in Band2 (centered at $1.88GHz$). As we can see, the signal is made of 50 RBs placed on the right side of the carrier

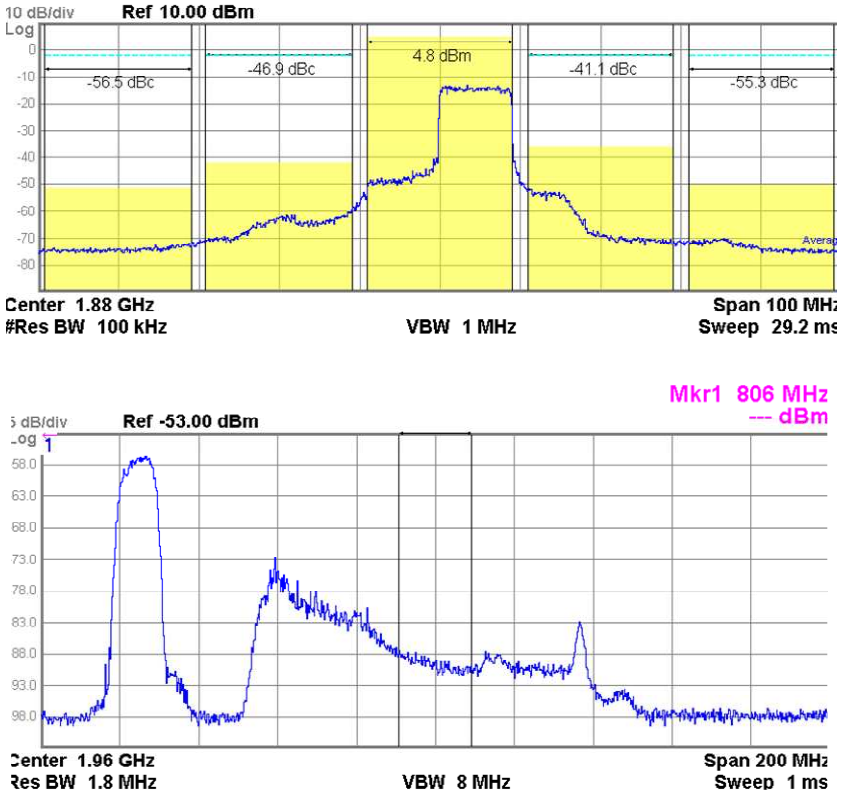

FIGURE 1.8: *LTE20 signal spectrum (from a spectrum analyzer) used for out-of-band noise measurements and, below, transmitted signal spectrum through the RX-port of a duplexer.*

and the noise will be measured at $+80MHz$ offset, i.e. at $1.96GHz$, near the RBs. In the second screenshot of Fig. 1.8, instead, the measured noise on the spectrum analyzer screen is reported: the high power burst, centered at $1.88GHz$, is the transmitted signal attenuated by the duplexer. A bandwidth of $18MHz$ around $1.96GHz$ is taken and an equivalent noise density extracted. Once the power

transmitted is known, it is possible to calculate the SNR in dBc/Hz. Notice the shape of the noise: it is following a first-order filtering roll-off, since the noise in that transmitter was filtered in the baseband with and RC filter. Moreover, it should be noticed that, in this kind of measurements, it is usually very difficult to dicriminate between noise and non-linearities: in fact, when large signals are transmitted, also non-linearities (i.e. $ACLR$, see the following section) contribute to noise. In Fig. 1.8 also some digital spurious tones are also evident, but this is an issue related to the digital baseband and signal routing.

Finally, the major contributors to the out-of-band noise are divided into baseband contributors and pre-power amplifier contributors. Since, as we'll see, the last stage of the on-chip transmitter is a programmable stage to control and increase the output power, when the transmitted power is toward the maximum possible value, the major contribution is coming from the programmable stage driver, since his output signal and noise are amplified. On the contrary, when the output power is scaled down, also the pre-power amplifier is scaled down and his noise contribution starts to be significant and, at very low power, it dominates the total SNR.

1.2.4 Non-linearities considerations: $ACLR$

The Adjacent Channel Leakage Ratio (ACLR or ACPR, Adjacent Channel Power Ratio) is basically the measure of the linearity of the transmitter [4, 5]. Unwanted emissions from mobile transmitters are usually tightly restricted so as not to interfere with other radio systems. Among emission specifications, the most important ones are the emission levels in the adjacent and the alternate channels and thery are strictly controlled in wireless mobile systems. The adjacent/alternate channel emission power specification is generally defined as the ratio of the power integrated over an assigned bandwidth in the adjacent/alternate channel to the total desired transmission power. The expression is

$$ACLR = \frac{\int_{f_0-\Delta BW/2}^{f_0+\Delta BW/2} PSD(f)df}{\int_{f_0-3\Delta BW/2}^{f_0-\Delta BW/2} PSD(f)df}, \tag{1.9}$$

where $PSD(f)$ is the Power Spectrum Density of the transmitted signal, while the other variables are reported in Fig. 1.9. A similar expression is given for the alternate ACLR.

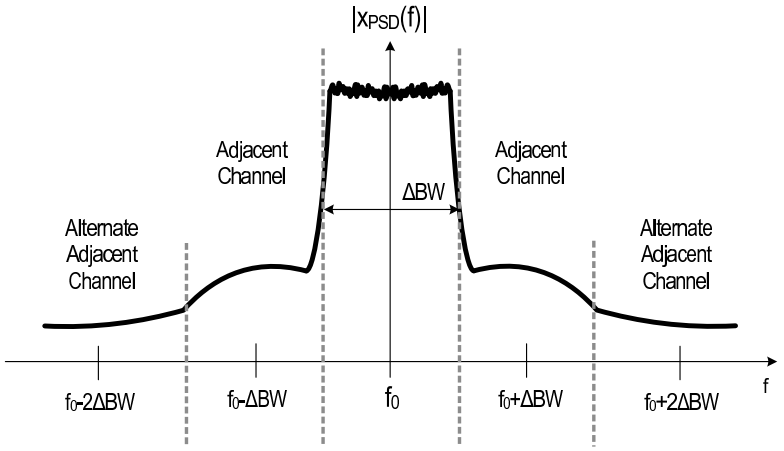

FIGURE 1.9: *Definitions of adjacent and alternate adjacent channels in a transmitted signal spectrum.*

The adjacent/alternate channel powers mainly result from spectral regrowth and non-linearity coming from the Pre-Power Amplifier in the IC transmitter and the Power Amplifier itself. In Cadence simulations, it is usually complicated to simulate a real modulated signal, hence a multitone signal is used. It is possible to emulate both the PAR and also the RMS of the real modulated signal with a multitone test and then evaluate the $IIP3$ of the circuit. The behaviour with the real modulated signal can be extracted with an expression that connects the IIP3 to the ACLR [6]. A simplified ACLR can be simulated with this multitone test, calculating the ratio between the signal tones and his out-of-band intermodulations (a kind of $\Delta IM3$ simulation, as seen in Fig. 1.10 for a baseband signal).

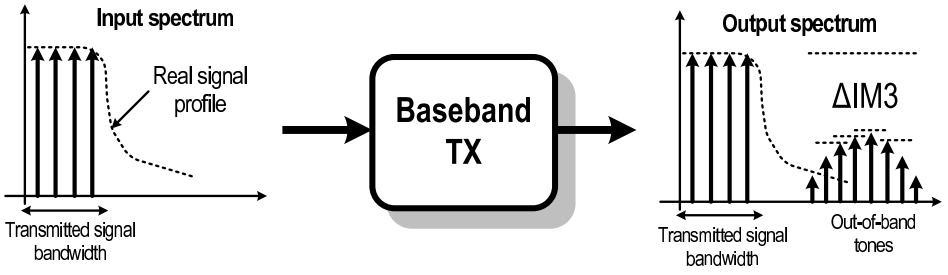

FIGURE 1.10: *Qualitative linearity definition through a 4-tones simulation.*

For what concerns LTE, there are some distinctions in the ACLR parameters: since the standard has to cohabitate with himself, but also with 3G, 2G and other standards like GPS etc..., distinctions between $ACLR_{E-UTRA}$ and $ACLR_{UTRA}$ are made. Without going too much in details, the definitions are reported in Fig. 1.11 for an LTE20 signal with 100 RBs. As we can see, the UTRA ACLR are more

related to the cohexistance of LTE with narrow bandwidths, like the 3G, while the E-UTRA is for larger bandwidths.

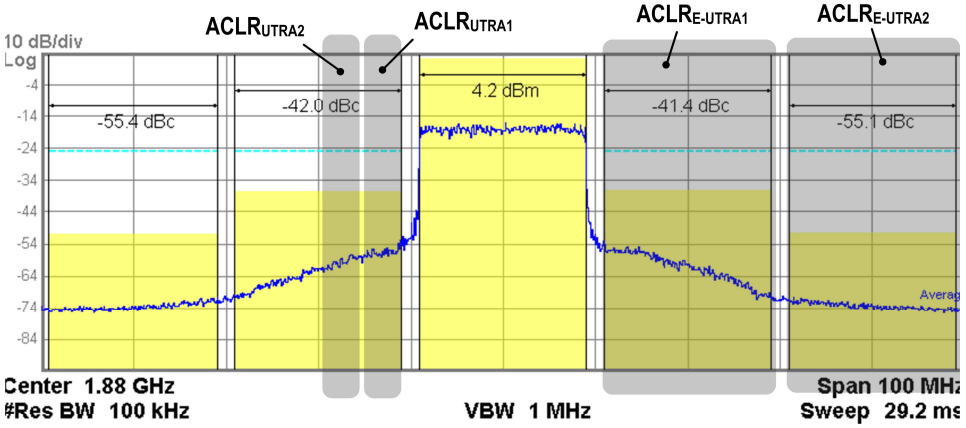

FIGURE 1.11: *$ACLR_{UTRA}$ and $ACLR_{E-UTRA}$ definitions on the transmitted signal spectrum.*

1.2.5 Error Vector Magnitude

Another parameter of transmitted signals is the modulation accuracy, that will ensure an optimum conversion when the signal will be received. The modulation accuracy is represented by the Error Vector Magnitude (EVM) [4], that is the difference between the actual symbol location and the theoretical symbol location on the modulation vector constellation diagram. As an example, in the CDMA downlink, offset QPSK (OQPSK) modulation [5, 4, 7] is used for the PN spreading code because of power and spectrum efficiency consideration. THe bandpass signal with OQPSK modulation can be expressed with an in-phase and a quadrature signal as:

$$s(t) = a_I(t)cos(\omega_c t) - a_Q(t)sin(\omega_c t) \tag{1.10}$$

where $a_Q(t)$ and $a_I(t)$ are the amplitudes of the in-phase and the quadrature signals, respectively,

$$a_I(t) = \sqrt{2}A \sum_{k=-\infty}^{+\infty} I_k g(t-kT_c), \qquad a_Q(t) = \sqrt{2}A \sum_{k=-\infty}^{+\infty} Q_k g(t-kT_c-T_c/2). \tag{1.11}$$

In these equations, A is the modulation signal amplitude, I_k and Q_k are the I and Q PN sequences with value 1 or -1 that are mapped from the I and Q spread data PN sequences 0 and 1, respectively. T_c is the PN chips duration and $g(t)$ is the

time domain response of the pulse shaping filter [4], that is a rectangular pulse before the pulse shaping, $g(t) = g_r(t)$ written as

$$g_r(t) = \begin{cases} 1 & 0 \leq t < T_c \\ 0 & \text{elsewhere} \end{cases} \tag{1.12}$$

Introducing a discrete time variable with a time step $T_c/2$ (half chip duration) instead of the continuous time variable and using Eq. 1.10, the baseband modulation I/Q signal calculated at $t = k_1 T_c/2$ from Eq. 1.11 and Eq. 1.12 we obtain the following:

$$a_I(k_1) = Acos[\phi(k_1)], \qquad a_Q(k_1) = Asin[\phi(k_1)], \tag{1.13}$$

where k_1 denotes the time instant $k_1 T_c/2$ and the modulation angle $\phi(k_1)$ is determined the the PN mapping [4]. The modulation can also be expressed in a vector form:

$$\overline{a}(k_1) = \overline{a_I}(k_1) - j\overline{a_Q}(k_1) = Aexp^{\phi(k_1)} \tag{1.14}$$

and this permits to have an intuitive geometrical interpretation with the signal constellation [7], depicted Fig. 1.12.

The modulation is generally distorted by phase noise of the Local Oscillator (LO) when it upconverts the RF carrier. Furthermore, it will be degraded when the signal passes through a narrow-bandwidth filter due to the magnitude ripple and the group delay of the filter. Thus, the distorted modulation $\overline{a'}(k_1)$ can be expressed as

$$\overline{a'}(k_1) = \overline{a}(k_1) + \overline{e}(k_1), \tag{1.15}$$

where $\overline{e}(k)$ represents the residual error vector. The constellation diagram of the distorted modulation vector is depicted in Fig. 1.12.

The modulation accuracy is represented by the Error Vector Magnitude (EVM) and it is defined as the mean square error between the samples of the actual and the ideal signals, normalized by the average power of the ideal signal. The EVM can be represented as

$$EVM = \left[\frac{E\{|\overline{a}'(k_1) - \overline{a}(k_1)|^2\}}{E\{|\overline{a}(k_1)|^2\}}\right]^{1/2} = \left[\frac{E\{|\overline{e}(k_1)|^2\}}{E\{|\overline{a}(k_1)|^2\}}\right]^{1/2}, \tag{1.16}$$

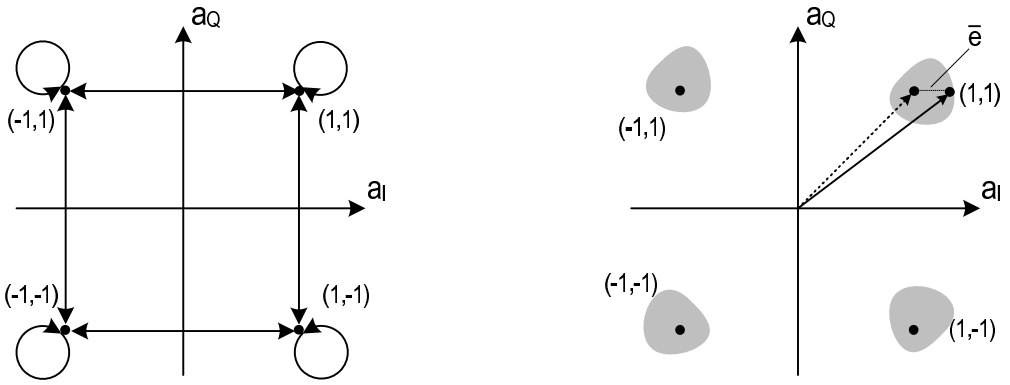

FIGURE 1.12: *Signal constellation of a QPSK modulation: ideal (left) and distorted with EVM (right)*

where $E\{\cdot\}$ represents the expectation of ensemble averages and the values are usually expressed in %. The maximum tolerable EVM is usually around 10% at the antenna, after the external Power Amplifier.

1.3 State-of-the-Art Transmitters

Now that we have discussed about the major problems and parameters of a transmitter, we can deduct the three "natural" elements that are necessary in an analog baseband chain. First, the DAC: the interface with the digital baseband is fundamental. Second, a filtering block: this one will eliminate the out-of-band noise and the DAC replicas. His position must be right before the upconversion to eliminate the most of the out-of-band emission before going to RF. Third, a Variable Gain Amplifier (VGA): actually, this last block is not a mandatory block, but it is necessary from an engineering standpoint. It will be necessary to reconfigure the output power of the transmitter to meet the various requirements. His function can be reparted in many other blocks: usually, there can be some programmability in the digital baseband, in the DAC itself, in the RF section with the pre-power amplifier but also another explicit block in the baseband.

In the next sections we will see how these functions are implemented in some example of transmitters coming from the state-of-the-art.

1.3.1 Cassia [8]

In this work from ESSCIRC 2008, a multi-band CMOS transmitter for cellular applications (in particular, 2G and 3G) is presented. The transmitter covers a wide range of frequency bands and it is designed to minimize power consumption in order to increase hand-set talk time. The external baseband I/Q differential current signals are injected into the baseband filter. Common mode input voltage and input impedance are set by an input buffer: it is crucial to keep a low common-mode voltage as well as low impedance to allow low voltage operations. After the filter, the signal is mirrored to the up-converters with a variable mirror factor G_{bbvga}, filtered, passed through a RF amplifier and transferred to a driver amplifier with a balun.

The purpose of the baseband filtering is to eliminate the DAC replicas and his sampling noise and attenuate out-of-band noise in the receiver bandwidth. The filter bandwidth is reprogrammable from $1MHz$ to $5.6MHz$ and a simplified schematic is shown in Fig. 1.13. The transconductors g_{m1}, g_{m2} and the capacitor C_2 form an

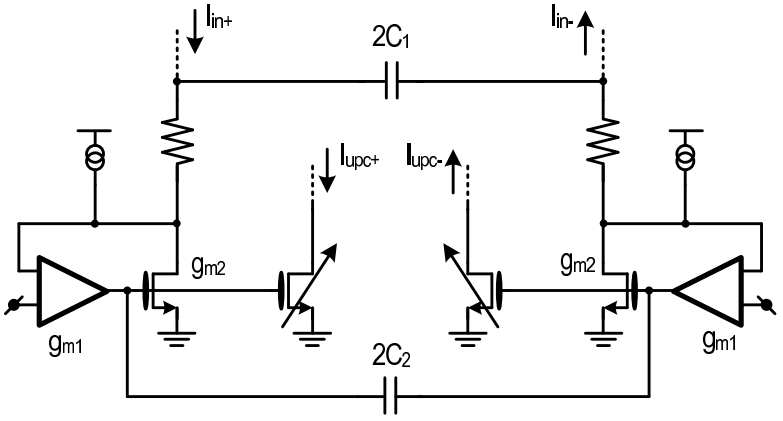

FIGURE 1.13: *Baseband filtering in current-mode proposed by [8].*

active inductor providing an overall second order low-pass transfer function:

$$I_{upc}(s) = I_{in}G_{bbvga}\frac{1}{(\frac{s}{\omega_0})^2 + (\frac{s}{\omega_0 Q}) + 1}, \tag{1.17}$$

where I_{in} is the input current and G_{bbvga} is the current mirror factor. The resonant frequency ω_0 and the Q factor can be expressed as:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}, \qquad Q = \frac{1}{R}\sqrt{\frac{C_2}{C_1 g_{m1}g_{m2}}}. \tag{1.18}$$

With this filter, the transmitter meets the requirements for the elimination of the external SAW filter.

The upconverter is made of a traditional active Gilbert cell. The in-phase baseband signal is upconverted with the in-phase LO signal and the quadrature baseband signal is upconverted with the quadrature RF LO signal. The mixer outputs are summed and the resulting differential signal is passed through a variable attenuator at RF.

The transmitter (excluding the frequency synthesizer) operates from a $2.1V$ supply and the total TX power consumption (including the synthesizer) is around $120mW$ for an ouput power of $5dBm$ and $90mW$ for $-8dBm$. Besides low WCDMA power consumption, output noise performance allows SAW-filter removal across several frequency bands. The measured sensitivity in SAW-less mode is still below $-110dBm$.

The transmitter from [8] shows a complete current-mode approach in the baseband: the input signal is a current and the analog processing (filtering, upconversion and amplification) is operated in the current domain. The filter parameters, anyway, are related to MOS transconductance (g_m) values. Since, to improve the signal-to-noise ratio (SNR), the signal swing is usually maximized (as we'll discuss later), the g_m varies substantially with the signal level. Time-variance of g_m makes the filter signal-dependent causing distortion and degrading the EVM. In fact, the EVM performances for 3G are around 5%. The instantaneous g_m variance can be substantially higher in the 4G standard, where the Peak-to-Average Ratio (PAR) is $3dB$ higher than the 3G.

1.3.2 Giannini [9, 10]

This work from ISSCC 2011 is a multi-standard transmitter LTE-oriented. His approach is the dual of the previous one, since in this one a voltage-mode approach is used: instead of an active Gilbert mixer, where the current signal is switched, a voltage passive-mixer is introduced (as proposed originally from [11]), and instead of a baseband filter that provides a filtered current, a more traditional Tow-Thomas biquad (see Ch. 2) with a voltage output is employed.

Fig. 1.14 shows the block diagram of the presented transmitter: a 3^{rd}-order transimpedance low-pass filter (TILPF) (made up of a biquad plus a RC pole) removes

the DAC replicas and out-of-band noise. The TILPF is followed by a passive mixer which upconverts the baseband voltage on the pre-power-amplifier's (PPA) input capacitor.

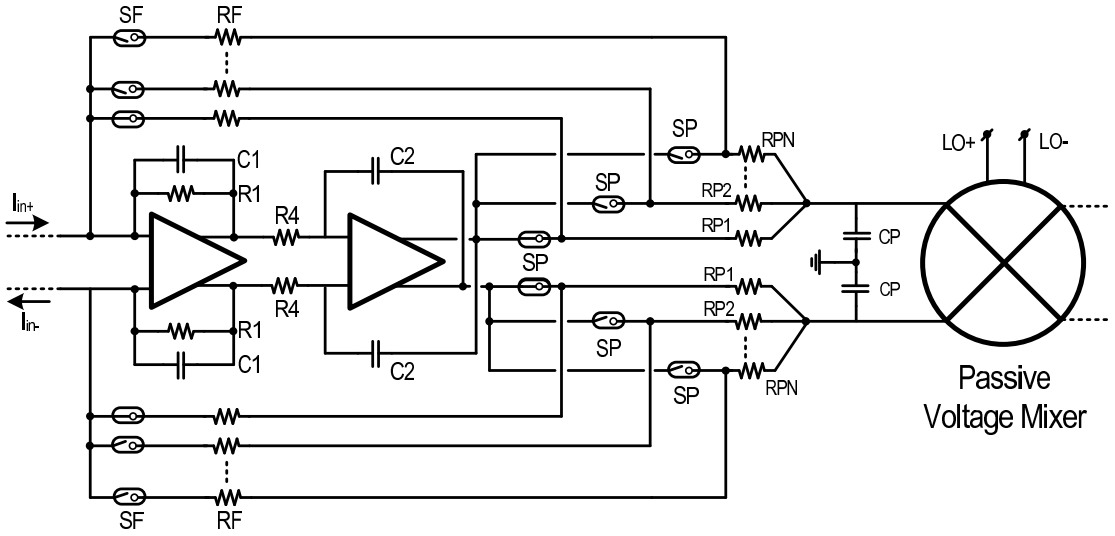

FIGURE 1.14: *Baseband filtering in voltage-mode with a passive voltage mixer, proposed by [9].*

The TILPF design is based on a flexible Tow-Thomas topology that offers independent programming of transimpedance gain, bandwidth and Q factor, whereas a quadrature voltage sampling mixer performs the upconversion using a low-noise 25%-duty-cycle LO driver. Filtering and mixing stages are designed to limit the impact on the transmitter Carrier-to-Noise Ratio (CNR) while keeping the power consumption minimal over the required RF range. At baseband, to achieve out-of-band noise lower than $-180dBm/Hz$ with limited power consumption, a passive LPF is added after the TILPF. From a system perspective, good CNR and high output power over different bands can be achieved with a tuneable passive pole.

To avoid linearity degradation, the switches of the RP array are closed inside a multi-feedback loop generated from the previous filtering stage, as shown in Fig. 1.14. When an SP switch is ON to activate a certain resistor RPx, a corresponding feedback loop is selected through the switch SF and feedback resistor RF. The nonlinear resistance of the active SP switch is thus divided by the open loop gain of the TILPF making his contribution to the distortion negligible. Overall the passive pole bandwidth can be moved from $7MHz$ up to $50MHz$. In order to efficiently drive RP values as low as 40Ω, a Class-AB op-amp topology is implemented that can trade power consumption for linearity.

The transmitter consumes 13 to $44mA$ from the $1.1V$ supply (TILPF + LO generation) depending on the selected bandwidth and LO frequency, whereas the PPA consumes less than $43mA$ from the $2.5V$ (PPA), proportionally to the required output power and linearity.

Notice that the PPA's input capacitor can be a serious issue due to the switched capacitor effect that force the capacitor of the passive filter RC to be very large. This means a large area occupied and a high power consumption, since this capacitor has to be driven in order to prevent slew-rate. Moreover, the fact that I and Q are summed on a voltage node lead to crosstalking of the two paths if the LO are not perfectly disoverlapped. In fact, the effect of this is the presence of a "bending" in the spectrum of the transmitted signal, as it can be seen in the snapshots in the original paper [9].

Finally, the proposed measurements of out-of-band are taken as Carrier-to-Noise Ratio, i.e. the SNR when the TX is transmitting an in-band single tone. With this method, the effect of non-linearities and the noise bandwidth spreading is not actuated, hence the numbers can be very low, since they are related only to the noise floor of the transmitter.

1.3.3 Oliaei [12]

The previous discussed work on LTE has mainly focused on the stringent RX-band noise and ACLR requirements for SAW-less transmitter design without discussing the Counter-InterModulation (CIM) performances. OFDM modulation in LTE20 creates up to 100 Resource Blocks (RB) (as discussed in the introduction) each containing 12 subcarriers with $15kHz$ spacing, spread over the channel bandwidth. For an RB with frequency offset f_s from the LO, transmitter non-linearity causes CIM products at $-3f_s$, $+5f_s$, $-7f_s$, ... from the LO. These spurious signals directly, or through remixing due to PA non-linearity, may fall on other bands. The worst case is when one or just a few RBs are transmitted at the edge of the channel. CIM terms are first generated by mixers. A pre-power amplifier (PPA) placed after the mixers will cause these terms to be regenerated due to high-level harmonic sidebands.

This example from ISSCC 2012 is a multimode multiband PPA-less transmitter which meets the counter-intermodulation and RX-band noise requirements for

SAW-less operation for 2G, 3G and 4G. The transmitter analog section is repre-

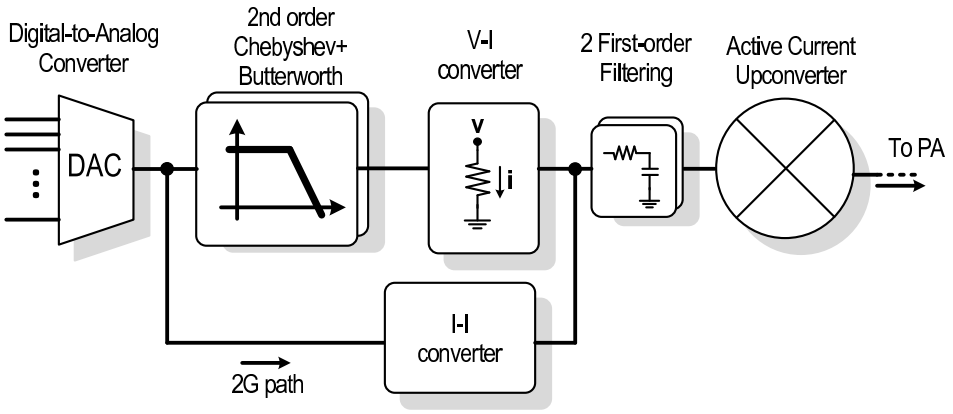

FIGURE 1.15: *Analog transmitter section diagram block proposed by [12]*

sented in Fig. 1.15. The digitally modulated TX signal is converted into analog using a 12-bit current-mode DAC and subsequently transformed into voltage by the baseband filter (BBF) for 3G and 4G signals. The DAC rate is selectable between $62.4MHz$ and $249.6MHz$. The BBF is a cascade of two 2^{nd}-order Butterworth and Chebychev filters to achieve enough quantization noise attenuation and DAC image rejection while maintaining a small group-delay variation and magnitude flatness over the signal bandwidth. The BBF output is converted into current using a voltage-to-current converter (V-I) which also incorporates two cascaded passive RC filters to reject the noise generated by the BBF. The DAC output is directed to a current-to-current converter (I-I) for 2G signals. The V-I (3G/4G) path is designed for high linearity while the I-I (2G) path is optimized for noise performance.

The RF section of the transmitter consists of four separate paths corresponding to four band groups. Only one RF path is activated at any time. The V-I and I-I outputs are routed to current-mode IQ mixers for frequency upconversion. Current-mode mixing has been selected mainly to reduce the CIM effect and avoid the need for digital pre-distortion. The upconverted signal is attenuated using a passive Variable Gain Amplifier (VGA) and eventually delivered to a tuned balun to drive the external PA.

The transmitter draws a maximum current of $52mA$ and $32.8mA$ from, respectively, $2.7V$ (upconverter) and $1.55V$ (baseband) supplies to generate $4dBm$ linear output power in LTE20. Notice that a $2.7V$ has been chosen to achieve a large output swing since the entire output section is working in Class A. The transmitter

shows a total power consumption of $186mW$ and $199mW$ when emitting $4dBm$ in LTE10 and LTE20, respectively, dominated by the RF section. The out-of-band noise is instead $-155dBc/Hz$ at $30MHz$ offset for LTE10 and $-157dBc/Hz$ at $120MHz$ offset for LTE20.

This transmitter is an example of a mixed-mode working. The previous works were entirely voltage-mode or current-mode: this one instead keeps the voltage-mode in the baseband and a current-mode for the upconversion, needing hence a V-I converter.

1.4 Conclusions

In the first part of this Chapter an introductory description of the new standard LTE has been given, together with the new problems that arise with it. In particular, the challenges are related to the transmitter's analog section of the integrated transceiver, that must interface the signal from the digital baseband with the antenna. These challenges gathers the issue of out-of-band emission, constituted of DAC replicas, noise and non-linearity, but also issues for the in-band signal, defined by the EVM. Finally, a survey on the State-of-the-Art for transmitters is given in the last part of the Chapter, taken from recent conferences and journals.

Chapter 2

An LTE Transmitter using a Class A/B Power Mixer

Moving toward the antenna side of the transmitter, the power consumption becomes more and more higher and it is critical to improve the efficiency of the last stages, without compromising the noise performances. In this Chapter, a fully reconfigurable multi-standard transmitter is presented that introduces a high-efficiency active mixer. The transmitter is operated in voltage-mode for the baseband (DAC plus two Biquad cells), while a power mixer is adopted for the upconversion. The two domain are interfaced with a V-I converter that implements also a variable gain. Moreover, the V-I converter drives the mixer in Class A/B through a particular architecture of the output stage. The realized chip and the measurements will be presented in the last part of the Chapter.

2.1 Voltage-mode Baseband

2.1.1 General Block Diagram

As seen in the examples from the State-of-the-Art presented in Ch. 1, there can be two approach in the design of a transmitter (but, of course, also in electronics in general), each one with pros and cons: a voltage-mode and a current-mode.

In the transmitter here presented [17], a voltage-mode has been adopted for the baseband, while a power mixer (and so a current-mode approach) is used for the upconversion of the baseband signal to RF. The block diagram of the entire analog baseband chain is shown in Fig. 2.1 and it is quite similar to the one presented in Fig. 1.15 from [12]. The stage that connects the two modes of operation is a V-I converter and it also acts as an active mixer driver, since the converted current will be mirrored into the switching pair (as described further). Notice that a filter (a real pole) is placed between these two blocks to eliminate out-of-band noise coming from the V-I converter and the high-order filtering block.

Moving upstream, the voltage-mode section is made of a 10-bit current-steering segmented DAC that steers the current signal on a resistor and his voltage drop is fed at the input of a high-order filter. Observe that in Figure 2.1 a very general block diagram is reported: indeed, although the described DAC is intrinsically a current DAC, the fact that the signal is transformed immediately into a voltage to fed the following filter makes it actually a voltage DAC, and so it is represented in the block diagram.

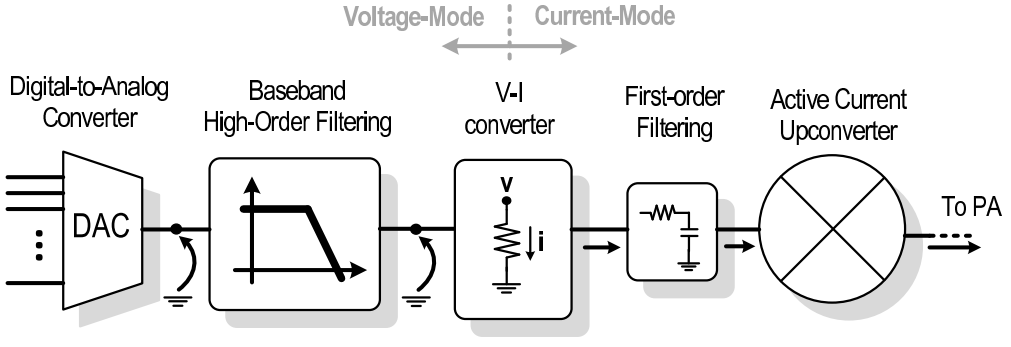

FIGURE 2.1: *Block schematic of the Multistandard Transmitter*

One of the major problem in transmitters for mobile communications, as already pointed out in Ch. 1, is the out-of-band emission: this is constituted by DAC replicas, noise and non-linearities. In the next sections we'll see how this transmitter deals with all these issues.

2.1.2 High-Order Filtering Block: the Tow-Thomas Biquad

Only in the LTE case, we have seen that there are many possible signal bandwidths (from $1.4MHz$ to $20MHz$) and the other previous standards have bandwidths still different. It is not possible to have on the same chip a transmitter chain for each one: the area cost will explode, considering the fact that besides mobile communication standards other communication standards must be implemented in the same transceiver (WLAN, Bluetooth, GPS etc...). Hence, a multi-standard transmitter must be reconfigurable and adaptive to optimize his performances for each standard. Having the aforementioned different signal bandwidths, the filtering function (performed by the filter block before the V-I converter, but also by the real pole before the mixer in Fig. 2.1) must change his cut-off frequency to adapt to the processed bandwidth.

As already pointed out, the main role of the high-order filter is to eliminate the DAC replicas and noise, meanwhile the passive filter is necessary to eliminate the out-of-band noise of the remaining blocks before the upconversion. Two general observations can be made. First, the more sharper the filtering is, the more effective his function is, but the filter order is in trade-off with power consumption and area. Second, we'd like to put the cut-off frequency the closest possible to the signal bandwidth or even inside this bandwidth to increase his filtering effect on the out-of-band side. In this case two problem arises:

- the in-band spectrum of the signal is filtered and it should be pre-compensated in the digital baseband, before driving the DAC;
- the same goes for the phase of the signal: if the cut-off frequency is close to the edge of the bandwidth, the phase delay of the spectrum near the filter cut-off will be different from the spectrum in the low frequency and this could lead to EVM problems.

Of course, if it is possible to pre-process the signal (amplitude and phase) in the digital baseband, there wouldn't be any problem. Otherwise, the filter cut-off frequency must be larger than the signal bandwidth.

The minimum filtering order in this transmitter is decided to be a Butterworth 3^{rd} order and so the high-order filter must be a biquadratic cell, while the single real pole is already placed before the mixer. Among the voltage biquads architectures, the Tow-Thomas biquad is, from an engineering standpoint, one of the best solutions since it permits to configure gain, Q and ω_0 orthogonally. His topology is reported in Fig. 2.2.

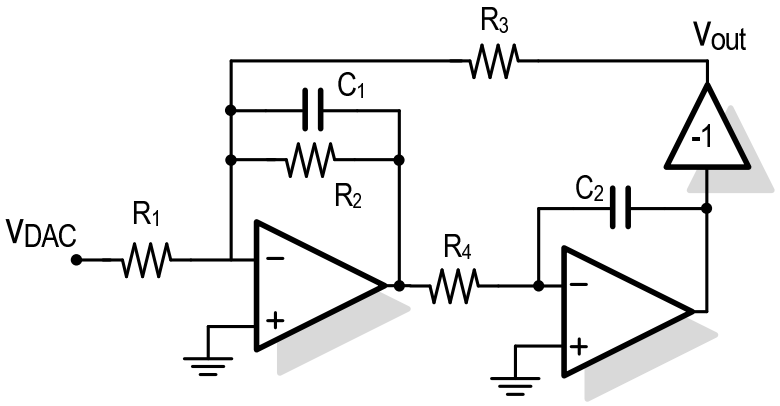

FIGURE 2.2: *Tow-Thomas Biquad schematic.*

The input voltage v_{DAC} is transformed into a current through R_1 thanks to the virtual ground created by the global feedback at the negative terminal of the first Op-Amp. It is then processed with the second integrator and the resistor R_3. The last sign inversion can be easily implemented in a fully differential configuration by crossing the differential output nets.

The transfer function from v_{DAC} to v_{out} is

$$\frac{v_{out}}{v_{DAC}} = \frac{G\omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2} \tag{2.1}$$

where

$$\omega_0 = \frac{1}{\sqrt{R_3 R_4 C_1 C_2}}, \quad Q = \frac{R_2\sqrt{C_1}}{\sqrt{R_4 R_3 C_2}}, \quad G = \frac{R_3}{R_1}. \tag{2.2}$$

A typical strategy is to put $R_4 = R_3 = R$ and $C_1 = C_2 = C$, after which Eq.s 2.2 simplifies to

$$\omega_0 = \frac{1}{RC}, \quad Q = \frac{R_2}{R}, \quad G = \frac{R}{R_1}. \tag{2.3}$$

As seen from Eq. 2.3, the three variables can be modified by changing just one element: ω_0 with C, Q with R_2 and G with R_1. In the proposed solution, the capacitors are fixed and the resistor values are changed to adapt the cut-off frequency to the 2G, 3G and 4G. The Q of the biquad is changeable with R_2, making easily possible to change also the type of the low-pass filter (Butterworth, Chebyshev...).

2.1.3 Operational Amplifier (OA) vs. Operational Transconductance Amplifier (OTA)

Besides DAC replicas, another contributor to out-of-band injection is given by noise. The biquad itself, described before, will filter the DAC replicas and DAC noise, whereas his own noise and the one coming from the following V-I converter will be filtered by the real pole inserted downstream. To ensure that a first-order will be sufficient to eliminate the most part of the out-of-band noise, the noise sources must be minimized and the Signal-to-Noise Ratio (SNR) must be maximized. The first one is directly related to the area occupied and to the power consumption [13]. The second one is achieved by maximizing the signal swing inside the circuit. In fact, in general, noise coming from many blocks of a circuit is loosely independent from the amplitude level of the processed signal (unless non-linearities, high swings or saturations occurr): whereas the noise is almost constant, to improve the SNR the signal level must then be increased as much as possible toward the rail-to-rail, limited by the power supplies.

The output stage of a traditional Operational Amplifier (OA), like the ones used for the Tow-Thomas in Fig. 2.2, is usually a source-follower with a low output impedance and it is unable to maximize the output voltage swing. In fact, as shown in Fig. 2.3, when the output voltage has to go over $V_g - V_{th}$ (where V_{th} is the threshold of the output MOS), the transistor starts to turn off, leading to distortion in the signal. The low boundary in instead given by the V_{ov} of the current souce. On the contrary, an Operational Tranconductance Amplifier (OTA) output stage (Fig. 2.3, on the right) is able to reach almost a rail-to-rail swing (limited by the overdrive of the PMOS and the NMOS).

On the other hand, there are some other issues. Since the ouput stage is now a gain stage and not a buffer stage, when impedances lower than the output stage

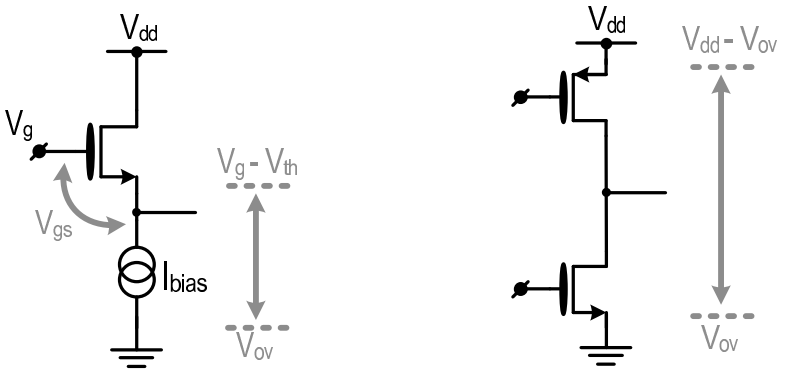

FIGURE 2.3: *On the left, a source follower used as output stage of an OA; on the right, an inverter as output stage of an OTA.*

impedance are used in the feedback network [1], the potential gain of the entire OTA is wasted. If, instead, higher impedances are used, a dominant pole could arise in the output stage, leading to issues in stability. However, in general, the gain loss is not a problem compared to the output signal swing and hence the use of an OTA is preferred. Lastly, even if it could be unusual to think of stages with high output impedance used in voltage-mode applications, we have to remember that they will be used in feedback, taking advantage of the effect of lowering the output impedances, provided that the gain loop is sufficient.

The Op Amp blocks reported in Fig. 2.2 are then actually implemented with OTAs, with the purpose of maximize the signal swings to improve the SNR.

2.1.4 Multipath OTA architecture

Large signal swings obtained with rail-to-rail operation make linearity another issue: the virtual grounds of the filter must be very good and hence the gain loop of the structure must be very high in the bandwidth of interest.

A traditional approach for the OTA is a dominant pole solution. Since the in-band gain must be high, the gain-product bandwidth must be positioned much more beyond the signal bandwidth of interest, as shown in Fig. 2.4. The maximum bandwidth of the desired baseband signal is $10MHz$ (LTE20), so we have to get a gain-bandwidth product around $1GHz$ to get a minimum open-loop gain of $40dB$ at $10MHz$. The requirement of $1GHz$ gain-bandwidth product is not easy to achieve, taking into account stability issues due to corners, parasitic poles etc...

[1] That's why OTA are usually suggested for architecture with capacitors in the feedback network [14].

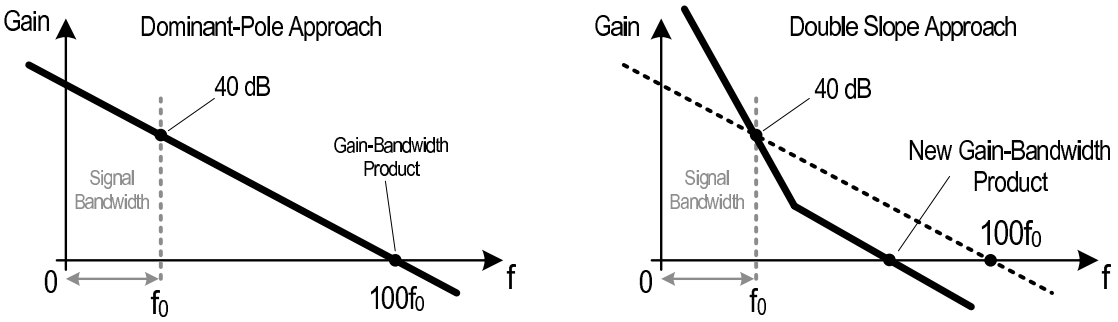

FIGURE 2.4: *Open-loop transfer function of an OTA with dominant pole approach (left) and with double-slope approach (right).*

A more practical solution is a multipath OTA. The structure is based on the sum of two different paths, a low frequency path and a high frequency path that acts when the low frequency path gain is lower than his gain. Fig. 2.4, on the right, shows the transfer function. Two low frequency poles allow an initial slope of $-40dB/dec$ instead of the ordinary $-20dB/dec$, so the gain drops quickily after those two dominant poles. When the low frequency gain path is lower than the gain of the high frequency path, this path becomes dominant and the global transfer function shows a zero that increase the phase. The $0dB$-cross is with $-20dB/dec$: for the Bode cryterion [15, 16], the system will be stable if the OTA is placed in a buffer configuration. Moreover, the gain-bandwidth product will be less than the one of a dominant pole topology, allowing more robustness against parasitic poles, temperatures and process corners.

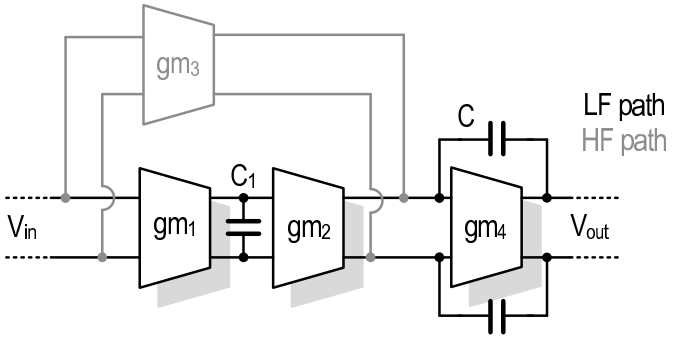

FIGURE 2.5: *Block diagram of a multipath OTA.*

Fig. 2.5 shows how to implement this transfer function. Two gm stages (gm_1 and gm_2) constitute the low-frequency path while the single stage gm_3 is the high-frequency path. gm_4, with the Miller capacitor C, is instead in common with the two paths. When the high-frequency path dominate the other, we can see that the first pole is "skipped". The low-frequency path $H_{LF}(s)$ and the high-frequency

$H_{HF}(s)$ paths are defined as:

$$H_{LF}(s) = \left(\frac{gm_1R_1}{1+sC_1R_1}\right)\left(\frac{gm_2R}{1+sRC(1+gm_4R_4)}\right)(gm_4R_4), \tag{2.4}$$

$$H_{HF}(s) = \left(\frac{gm_3R}{1+sRC(1+gm_4R_4)}\right)(gm_4R_4), \tag{2.5}$$

where R_1 is the output impedance of the first stage, R is the equivalent output impedance after the second stage and R_4 the one of the last stage. The total transfer function is given by $H(s) = H_{LF}(s) + H_{HF}(s)$. Making $1 + gm_4R_4 \approx gm_4R_4$ in the Miller multiplication, we get

$$H(s) = gm_4R_4\left(\frac{gm_1R_1}{1+sC_1R_1}\right)\left(\frac{gm_2R}{1+sRC(1+gm_4R_4)} + \frac{gm_3R}{1+sRC(1+gm_4R_4)}\right) \tag{2.6}$$

$$\approx gm_4R_4\frac{(gm_1gm_2R_1R + gm_3R)}{(1+sC_1R_1)(1+sRCgm_4R_4)}\left(1 + s\frac{gm_3C_1R_1}{gm_1R_1gm_2 + gm_3}\right).$$

If we suppose that $gm_1R_1gm_2 >> gm_3$, then we can easily see that the transfer function has two poles and one zero:

$$p_1 = -\frac{1}{C_1R_1}, \qquad p_2 = -\frac{1}{RCgm_4R_4}, \qquad z = -\frac{gm_1gm_2}{gm_3C_1}.$$

2.1.5 5^{th} Order Filtering

Since a transmitter must cohabit with many wireless standards (2G, 3G, 4G with their different variants in the global frequency plans but also GPS, WLANs etc...), it can happen that the DAC replicas are not sufficiently suppressed by the 3^{rd} order filtering: a signal received by the front-end of the same device with a bandwidth close to the desired transmitted signal bandwidth, where a not sufficiently filtered DAC replica lies, can be degraded. The same goes if another device nearby is using that bandwidth to transmit or receive.

In these cases, a higher order filter is mandatory: adding another Tow-Thomas biquad (that can be turned off whenever not necessary) before the one already placed, it is possible to achieve a 5^{th} order filtering, taking into account the real pole RC shown in Fig. 2.1. Furthermore, Q, ω_0 and gain programmability are easily implemented changing just one passive element, as discussed before.

2.2 Voltage-to-Current (V-I) Converter and Active Upconverter

2.2.1 Conceptual Schematic

The output signal of the biquad (or of the two biquads) is a voltage: to feed the active mixer a conversion from voltage to current (V-I) is necessary. The conceptual single-ended schematic of the V-I converter with the active mixer is shown in Fig. 2.6.

The OTA creates a virtual ground on the positive input terminal v_+ and, through the resistor R_{gm}, the voltage signal v_{in} coming from the Biquad(s) is linearly transformed into the current $i_{in} = v_{in}/R_{gm}$. Furthermore, R_{gm} is a variable resistor, so it acts as a Variable Gain Amplifier (VGA): the smaller the resistor is, the larger the current signal amplification. The output transistor g_{mo} (that represents the output stage of the OTA), through the feedback, is the input branch of a variable current mirror (with an RC filter inside) and the amplified current is then fed to the active mixer. The second branch of the mirror is made up of N programmable stages in parallel that deliver current to a resonant RLC load after the mixer (not shown in Fig. 2.6).

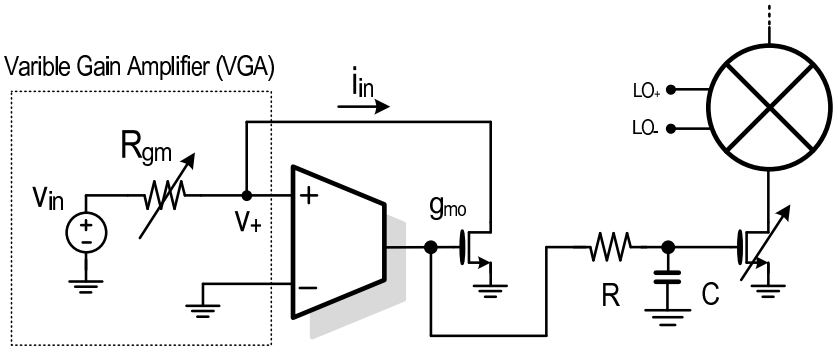

FIGURE 2.6: *Simplified schematic of the V-I converter driving the active mixer.*

2.2.2 Class A vs. Class A/B Operation

As in the case of the Biquad, the power consumption of the V-I stage will determine the noise injected in the out-of-band. This has to be low given that it will be

filtered only by the RC filter inside the current mirror. Moreover, his current consumption will be copied by the transconductor under the active mixer and, since it's a scaled-up copy, it will decide the consumption of the most power-hungry stage of the analog chain.

The final goal of the trasmitter is to deliver a fixed power to the balun after the mixer and there is a current/voltage swing trade-off to get the same power. Increasing voltage swing (by increasing the balun equivalent resistor) at the ouput can lead to stress in the technology and non-linearity. On the other hand, increasing the current means of course power consumption (and so low efficiency), but it can be demonstrated that, if the upconverter is working in Class A, the Signal-to-Noise Ratio of the upconverter will be higher.

In fact, the SNR of each mixer transconductor (schematically represented in Fig. 2.7) is given by

$$SNR_{gm} = \frac{i^2_{RMS}}{i_{noise}}, \tag{2.7}$$

where i_{RMS} is the RMS value of the current signal and the ratio between his peak value and the RMS is defined as

$$PAR = i^2_{peak}/i^2_{RMS}. \tag{2.8}$$

Instead, $i_{noise} = 4kTg_m$, excluding for simplicity the γ factor [18], is the noise current of the MOS (shown on M_n in Fig. 2.7). In particular, g_m is defined by the biasing of the transistor, since $g_m = 2I_{bias}/V_{ov}$.

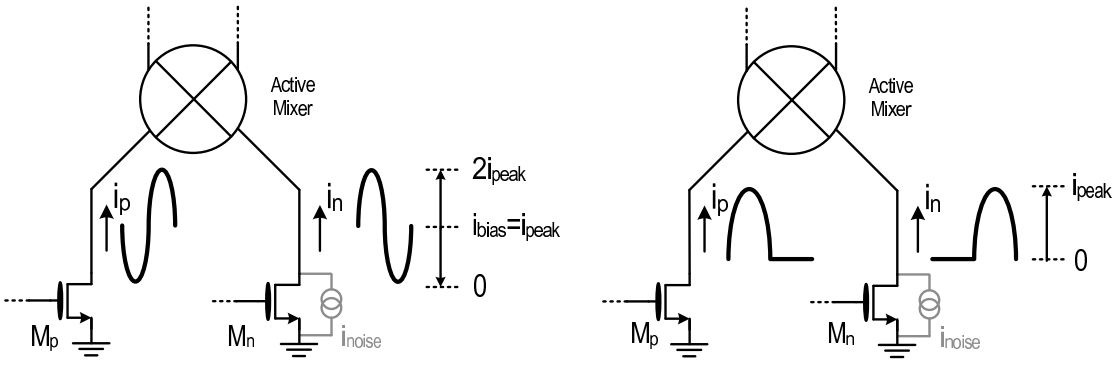

FIGURE 2.7: *Mixer transconductor working in Class A (left) and Class B (right).*

Usually, the mixer transconductors are operated in Class A (Fig. 2.7, on the left): the minimum bias current that they can have is given by the i_{peak} since they must

be able to process both positive and negative half waves. From Eq. 2.7, we can get

$$SNR_{gm} = \frac{i_{RMS}^2}{4kTg_m} = \frac{V_{ov} \cdot i_{peak}^2}{8kT \cdot PAR \cdot I_{bias}}$$

and since we noticed that $I_{bias} = i_{peak}$, we have

$$SNR_{gm} = \frac{I_{bias} V_{ov}}{8kT \cdot PAR}. \tag{2.9}$$

From this equation we can see that increasing I_{bias} maintaining V_{ov} constant permits to increase the SNR. This solution to decrease noise is however opposed to the idea of saving power.

If instead we step back to Eq. 2.7 we can see easily that a better improvement can be made if we introduce a Class B working of the transistors. Indeed, in this situation the transistor has to process only half of the signal (Fig. 2.7) and hence I_{bias} is not constrained by the i_{peak} signal: this makes $i_{noise} = 4kTg_m$ very low and the SNR higher, when the signal will be reconstructed. Ideally, I_{bias} could go to zero, but then non-linearity problems arise, so a bias is always given to the transistors, making the working from Class B to Class A/B. Anyway, this biasing will always be much less than the Class A case, especially for signals with high PAR.

2.2.3 Class A/B OTA output stage

The output stage of the OTA of the V-I converter, depicted as a single MOS in Fig. 2.6, will drive the transconductors of the mixer in Class A/B. A traditional approach for create a driver in Class A/B is shown in Fig. 2.8, where the differential simplified schematic of the V-I converter and the mixer transconductor are reported. The output stage is basically an inverter with a dc offset between the PMOS and NMOS gates that set the DC difference of the two bias. The voltage signal coming on the NMOS gate is hence DC-translated on the PMOS transistor, making the inverter working in a push-pull fashion.

With this configuration we can see that the input signals $i_{in+} (= i_{in-})$ is divided into the currents in the output transistors M_{p+}, M_{n+} (and M_{p-}, M_{n-}). Unfortunately, the mirrored current taken differentially to reconstruct the original signal,

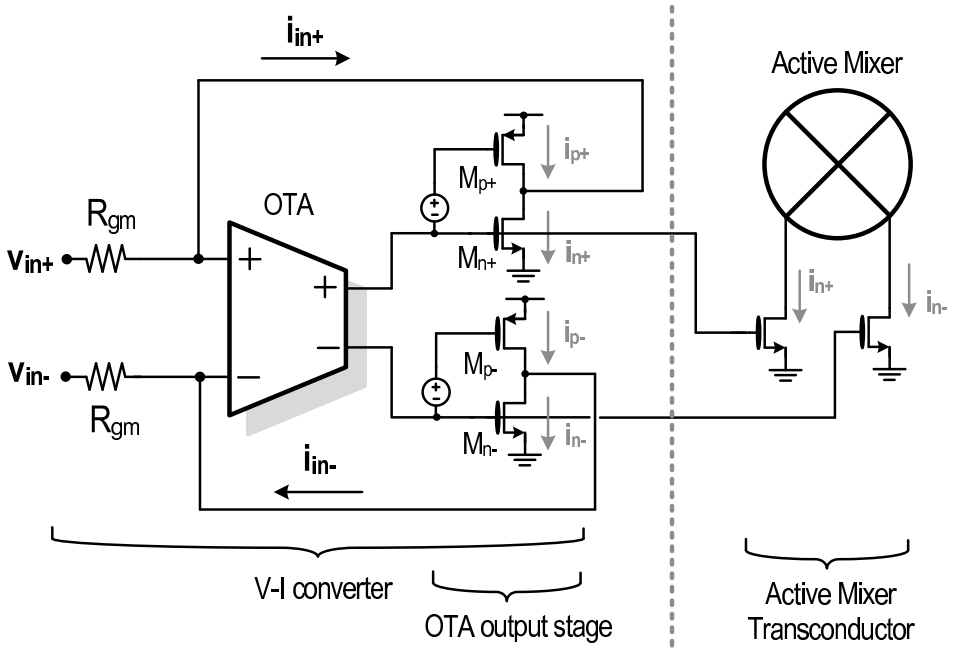

FIGURE 2.8: *V-I converter OTA output stage in Class A/B (the RC filtering has been omitted) driving the active mixer.*

supposing that the mirror factor is unitary, is then

$$i_{mixer} = i_{n+} - i_{n-},$$

that is not equal to the input current, that is

$$i_{in+} = i_{n+} - i_{p+}.$$

As it is shown in Fig. 2.8, the information of the signal must be instead related only to the NMOS transistors, since the transcondutors that drive the active mixer are NMOS.

The solution implemented to drive the NMOS-only transconductor is shown in Fig. 2.9. The gate voltages of M_{n1+} and M_{n1-} will be connected to the mixer transconductors (after being filtered with a RC filter, not shown in the picture for simplicity). For instance, if we follow the current signal i_{in+}, we notice that it is divided between M_{p1+} and M_{n1+}, like before. However, through a crossed current mirror, the current i_{p+} in M_{p1+} is now equal to the signal current flowing in M_{n1-}, that is coming from i_{in-}. The opposite is for the current in M_{p-}, making the output current (that will be mirrored toward the mixer) $i_{in+}(= i_{in-})$

$$i_{in+} = i_{n+} - i_{p+} = i_{n+} - i_{n-} = i_{p-} - i_{n-} = i_{in-}, \tag{2.10}$$

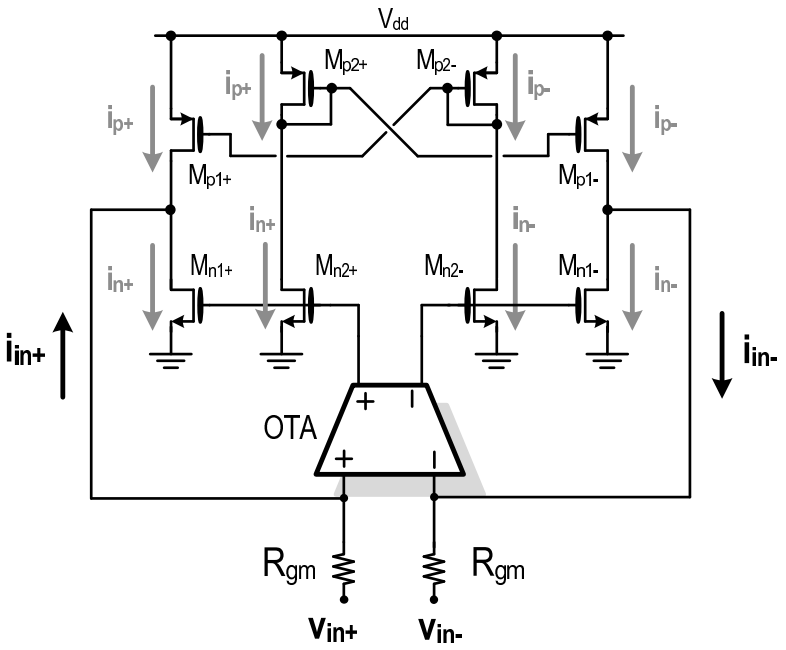

FIGURE 2.9: *Proposed Class A/B output stage of the V-I converter OTA.*

being $i_{p-} = i_{n+}$ and $i_{p+} = i_{n-}$, following Kirchhoff in the central nets.

With this architecture, the signal flowing into the active mixer is equal to the input signal of the V-I converter and (ideally) no non-linearities are introduced. A more detailed schematic showing the flow of the currents with two opposite large signal is reported in Fig. 2.10. The details of the OTA and of the common-mode feedback (CMFB) circuits, necessary to set the output voltage and the bias currents, will be shown in the next chapter.

2.2.4 RC Filter inside the Current Mirror

As we mentioned before, inside the current mirror an RC filter is inserted. His role is to filter the out-of-band noise coming from the Tow-Thomas Biquad and also the noise coming from the V-I converter. The main issue here is that the RC filter is intrinsically a voltage-driven cell. So, the driving impedance must be low (i.e. a voltage source) or well controlled, so that the cut-off frequency is well defined including also the driving impedance together with the explicit R. In Fig. 2.11 a simplified single-ended schematic of the V-I converter is shown and we can see that the driving impedance is dependent on the feedback loop.

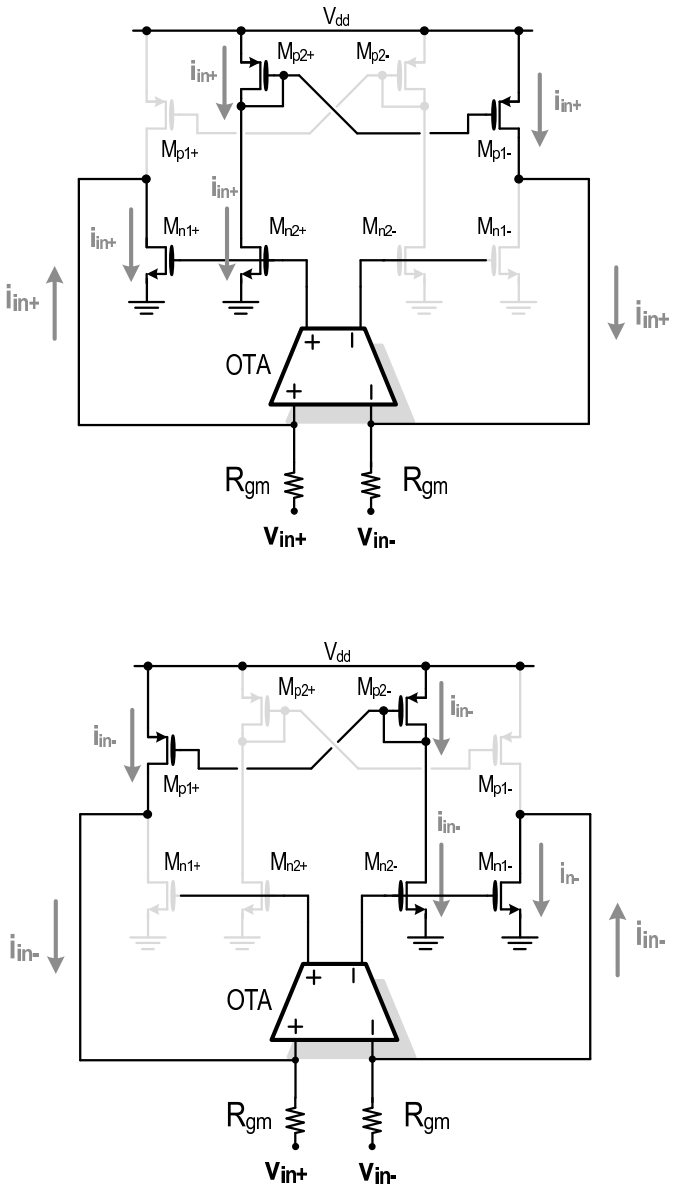

FIGURE 2.10: *Current signal flowing in the unbalanced Class A/B output stage.*

Since the structure already implements an high loop gain to create a good virtual ground at the input, we can exploit it also to get a very low driving impedance for the RC filter and drop the idea of making it well controlled.

Looking at Fig. 2.11 and supposing that the OTA is simply a Norton equivalent with a G_m and a parallel resistor r_o, we can see that the ouput impedance Z_{out} is

$$Z_{out} = \frac{r_o}{1 + g_{mo} G_m R_{gm} r_o} = \frac{r_o}{1 + |G_{loop}|}. \tag{2.11}$$

If the G_{loop} is sufficiently high, the driving impedance Z_{out} can be really low and the RC filter will have a cut-off frequency well defined with $1/CR$.

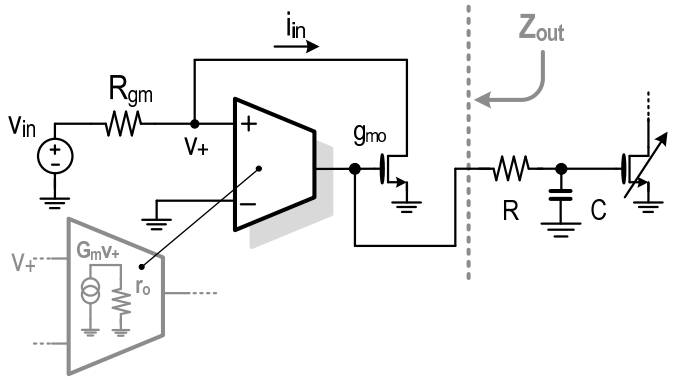

FIGURE 2.11: *RC filter inserted in the output current mirror of the V-I converter.*

Another problem is the trade-off between non-linearity and out-of-band filtering. In Fig. 2.12, the V-I converter can simply be represented as a transistor M_n (that represent the output stage of the OTA) with an amplifier A in feedback (that represents the OTA) and his gate is connected to a matched transistor M_{n2} with the drain placed to AC ground. The drain of the first transistor is a virtual ground so there is no effect related to channel modulation and the same goes for the ouput transistor M_{n2}. Injecting a single tone current i_{signal} in M_n, the voltage v_{gate} (following the classical equation for the MOS [19]) is given by

$$v_{gate} = \sqrt{\frac{2i_{signal}}{K}} + V_{th},$$

where K is $\mu_n C_{ox} W/L$ and V_{th} the threshold voltage of M_n. As we can see, v_{gate} is a non-linear function of the input current i_{signal} and his spectrum contains multiple tones of the input one (Fig. 2.12). Anyway, when this non-linear voltage is applied to the non-linear characteristic of another matched transistor, the output current will return linear: the MOS needs the extra tones to reconstruct the single-tone current at the output.

Hence we can see the problem when a RC filter is inserted in the current mirror (Fig. 2.12): the attenuated tones are not sufficient for the MOS to reconstruct the linear input current, and so the output current contains non-linearity. In this sense we talked about trade-off between non-linearity and out-of-band filtering: the more close the RC cut-off frequency is to the signal bandwidth, the more noise is filtered but also the more non-linearities are introduced at the output. The

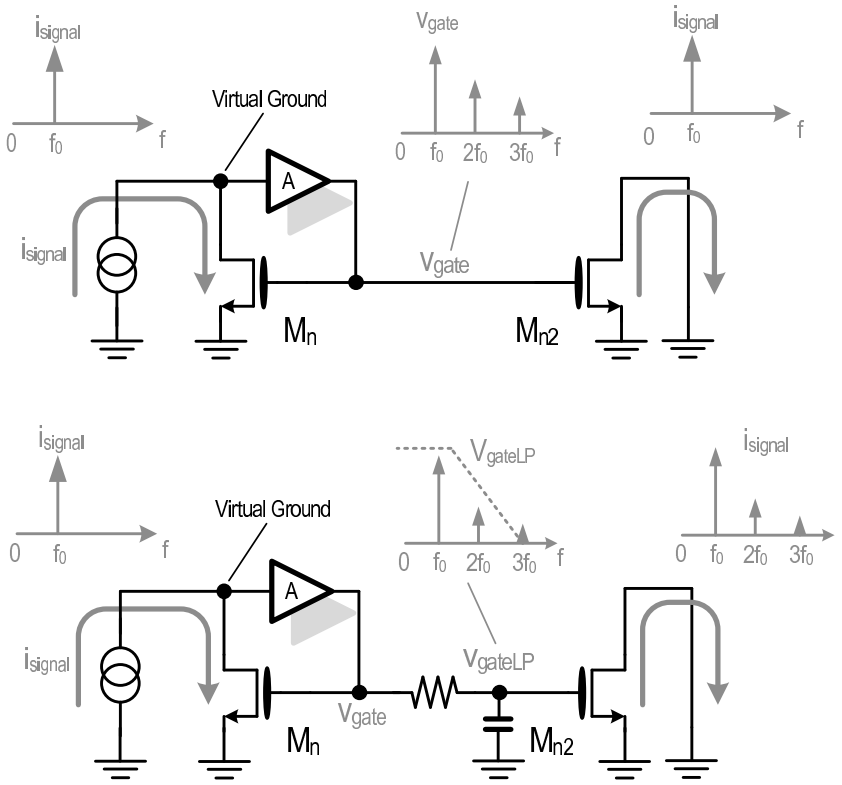

FIGURE 2.12: *Effect of the RC filter on output current linearity.*

position of the RC cut-off frequency must then be chosen taking into account all these effects.

2.2.5 Active Mixer

In addition to improve the current efficiency, another goal is improve the voltage efficiency, i.e. maximize the output voltage swing and this has to be done in the upconverter part. The radiofrequency section of the transmitter is shown in Fig. 2.13.

A controllable array of mixer transconductors permits to change the current mirror factor as depicted in Fig. 2.6 and hence select the ouput power delivered to the RF. For each gain step a single active mixer is used and when the maximum gain is achieved all the mixer are working in parallel. There is also the possibility to use fractional mirror factor, in order to go below the unity mirror factor and hence decrease the power delivered to the balun. Notice that this is the reason why the dominant contributors to the out-of-band noise are coming from the section before the mixer transconductors: a scaled-up mirror multiplies these contributors

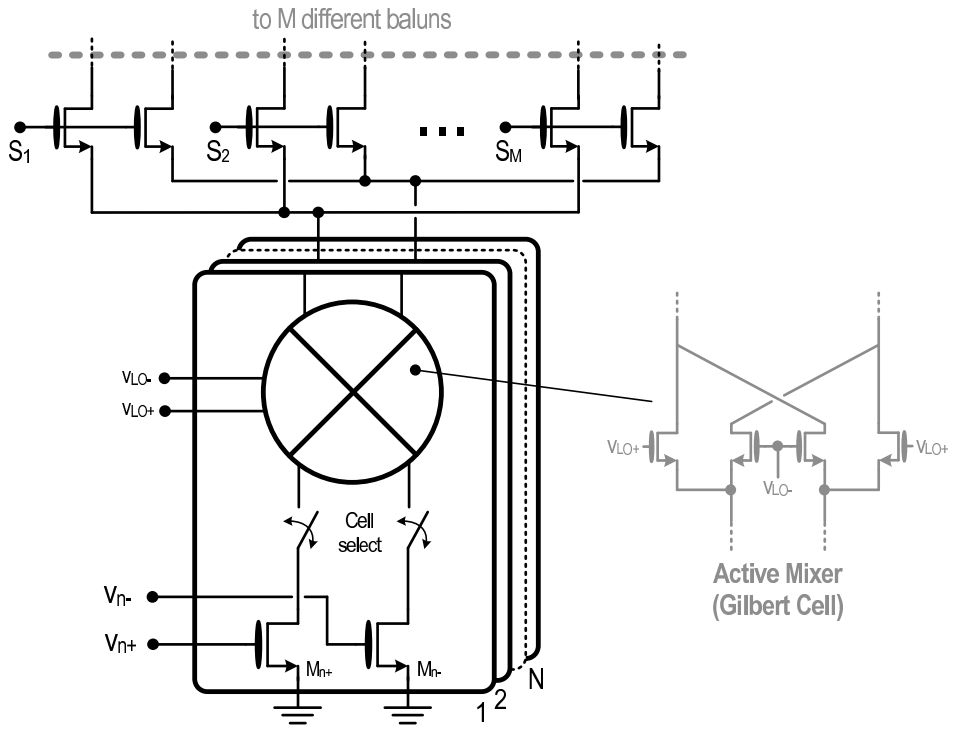

FIGURE 2.13: *Transmitter upconverter section: N active mixers in parallel.*

for the mirror factor squared, while the mixer transconductors contribution grows linearly with the number of stages activated. After the active mixers, an array of switches is placed to select different baluns, each one of them covering different transmission bands.

The mixer switches are traditionally kept in saturation to isolate the RF side from the baseband side. In this case, since the additional balun selectors have to be stacked and we want to keep the maximum voltage swing, the mixer switches are operated in the triode region to save voltage drop. It's instead important that the balun selectors are operated in saturation region, so that they can isolate the RF side from the rest.

2.3 Prototype and Measurements

The transmitter has been implemented inside a full reconfigurable transceiver, manufactured in $55nm$ CMOS technology. In Fig. 2.14 the microphotograph of the entire transceiver is reported together with the detailed layout of the transmitter. The whole analog section (baseband and upconverter) has a single $1.8V$ power

supply and the active area occupied is $1.3mm^2$, divided almost equally between the RF section and the baseband.

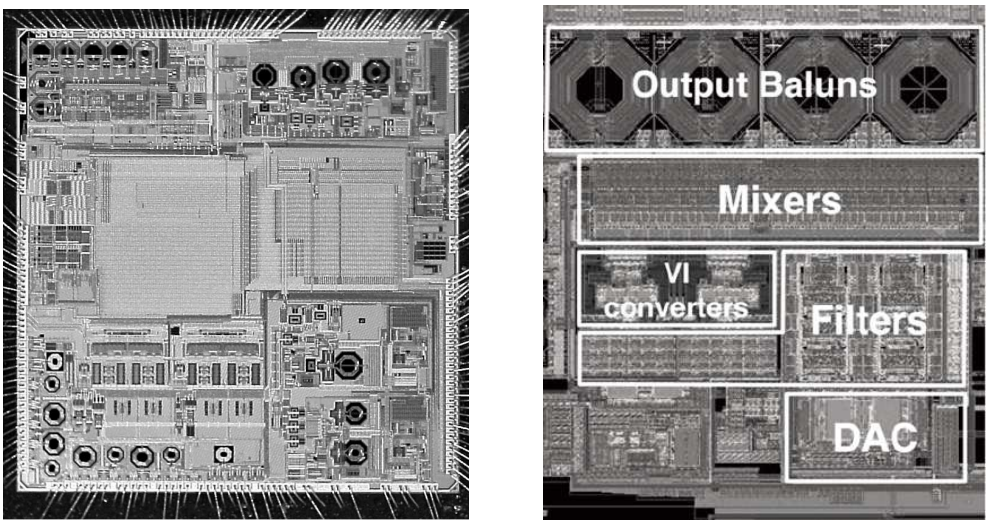

FIGURE 2.14: *Realized chip microphotograph (left) and detailed layout of the transmitter (right).*

The current consumption of the trasmitter (DAC excluded) is reported in Fig. 2.15.

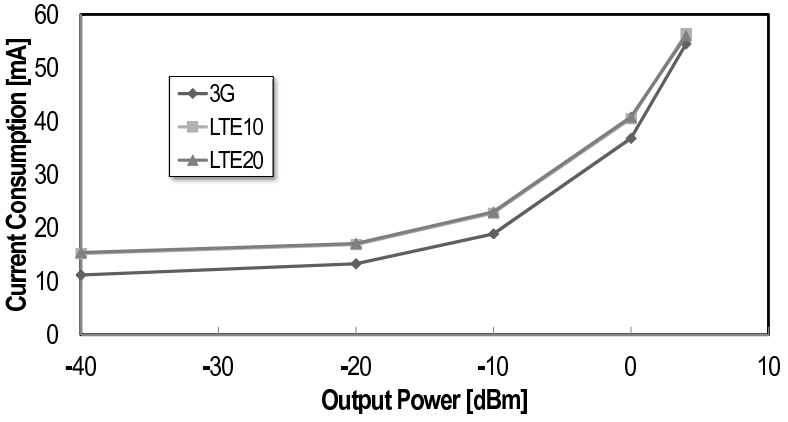

FIGURE 2.15: *Transmitter current consumption from* $1.8V$.

In the configuration for high output power, the dominant contribution is given from the upconverter: if it was operated in Class A the total current consumption would have been much higher. Notice, moreover, that going from 3G to 4G the current consumption is almost constant: this is due to the Class A/B working. In fact, making the upconverter in Class A/B, his current bias is independent from the standard and his current consumption depends only on the RMS value of the

signal, that is almost equal in the two standard cases (the difference is in the PAR).

When lowering the output power (below $-20dBm$), the most power-consuming section becomes the baseband, while the upconverter is just a small fraction. The upconverter becomes instead the dominant contributor in the out-of-band noise while, before, the baseband was the dominant part: also in this configuration, the Class A/B working contribute positively since it decreases the noise of the mixer transconductors.

In Fig. 2.16, various linearity parameters ($ACLR$ described in Ch. 1) are plotted versus the output power for the LTE10 standard, Band2. The E-UTRA

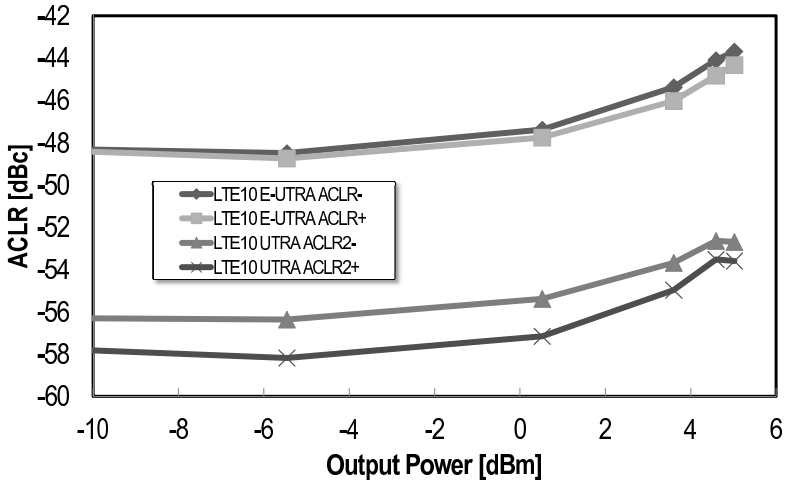

FIGURE 2.16: *Transmitter linearity parameters vs. output power transmitted.*

ACLR1 stays below $-44dBc$ up to $4dBm$ meanwhile the UTRA ACLR2 stays below $-53dBc$. After that, since the output power is increased by changing the number of stages in the upconverter, compression of the upconverter occurs: the ouput voltage signal at the balun starts to compress the balun selector and hence the active mixer. There is also a degradation at low power due instead to difficulty in measurements since the signal is very small and also the non-linearities are too small for detection. Of course, the linearity requirements given from 3GPP at this low power are much more relaxed.

Finally, the out-of-band noise (measured in the receiver bandwidth for different working bands at $0dBm$ output power) versus frequency offset from the RF carrier is reported in Fig. 2.17. In particular, the $31MHz$ offset corresponds to Band12, 13, 14, 17, meanwhile the $45MHz$ is for Band5, and the $80MHz$ for Band2. The

transmitted signal for this type of measurements depends on the 3GPP requirements, as discussed in Ch. 1. The worst case is when the frequency offset is the

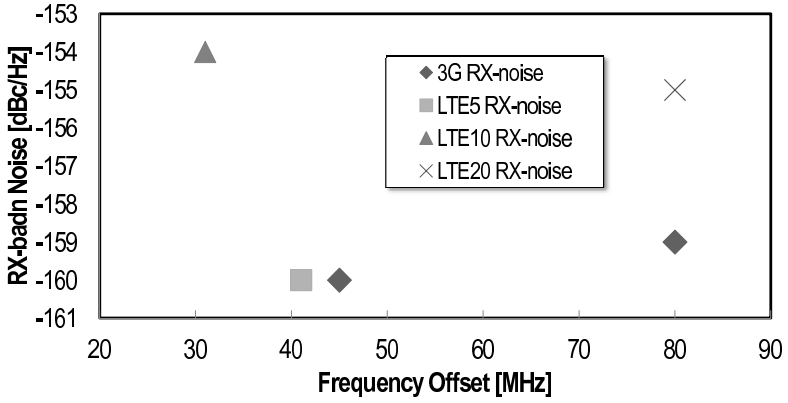

FIGURE 2.17: *Out-of-band noise performances vs. frequency offset from the RF carrier.*

smallest. Actually, also the bandwidth of the signal has a certain impact: the more large is the bandwidth, the more noise can be injected out-of-band. Moreover, also non-linearity has a certain impact on the noise measurements since it is very difficult to discern between noise and non-linearities contributions in the out-of-band noise.

A comparison table with a state-of-the-art transmitter from ISSCC2012 (described in Ch. 1, [12]) is reported in Tab. 2.1.

The maximum output power is higher than the reference: hence, for example, a less expensive Power Amplifier could be chosen since the on-chip transmitter already transmits up to $6dBm$. Good linearity is also shown from this transmitter, compared to the Class A from ISSCC2012. At $0dBm$, the RX-band noise of the presented transmitter for 3G and LTE (5, 10 and 20) varies from -154 to $-160dBc$ depending on the offset frequency. The worst value of $-154dBc$ for LTE10 and an offset frequency of $31MHz$ is due to the baseband, and in particular from the Tow-Thomas Biquad.

A huge difference is seen in the power consumptions: more than a factor 2 is shown at $4dBm$. This is due to the introduction of the Class A/B working in the upconverter, the most power-hungry section (at maximum power), compared to a classic approach in Class A. When decreasing the output power, the baseband consumption affects more significantly the total current drawing, and hence the advantage decrease to about 40% around $-10dBm$. Furthermore, as already pointed out, the power consumption going from 3G to 4G (that means increasing

		ISSCC2012			This Work		
Parameter	Unit	3G	LTE10	LTE20	3G	LTE10	LTE20
Max. Output Power	dBm	4.1	3.7	4	7	6	
ACLR1 @4dBm	dBc	-43.7	-	-	-47	-	-
ACLR2 @4dBm	dBc	NA	-	-	-66	-	-
$ACLR_{E-UTRA}$ @4dBm	dBc	-	-40.3	-40.3	-	-44	-41
$ACLR_{UTRA2}$ @4dBm	dBc	-	NA	-46	-	-53	-47
EVM LB@0dBm	%	NA	NA	NA	1.4	1.4	1
EVM HB@0dBm	%	1.54	0.66	1.05	2.1	1.8	1.4
RX-band noise	dBc/Hz	-156 @45M	-155 @30M	-157 @80M	-160 @45M	-154 @30M	-155 @80M
Consumption @4dBm	mW	150	186	199	98	101	101
Consumption @-10dBm	mW	45	56	70	32.5	39.5	39.5
Supply Voltage	V		1.55/2.7			1.8	
Area	mm^2		5.06			1.3	
Technology	-		90CMOS			55CMOS	

TABLE 2.1: *Comparison with transmitter from ISSCC2012 [12].*

the PAR from $6dB$ to $9dB$) remains almost equal, while in the reference case it increases by about one third.

Finally, one power supply for the baseband and the upconverter compared to two different ones decreases the costs even more, not to mention the fact that the active area is almost one fourth.

2.4 Conclusions

A mixed-mode (voltage and current) baseband for a multistandard transmitter has been described in this Chapter. The requirements on noise, linearity and power consumption, not to mention the engineering standpoint have been explained for the Biquad filtering block and the V-I converter, focusing in particular on a high-level design of the OTAs. The function of the V-I converter has been introduced, together with the particular output stage of the OTA, necessary to introduce a Class A/B approach in the most power-hungry block of the transmitter, i.e. the active mixer. Finally, the description of the realized prototype closes the Chapter, accompained by the measurements results and the comparison with the State-of-the-Art.

Chapter 3

A Low Out-of-Band Noise LTE Transmitter with Current-Mode Approach

A mixed-mode transmitter implements a building block that doesn't belong to the fundamental blocks of a trasmitter: the V-I converter. With the aim of implementing the benefits of a voltage-mode transmitter also in the current-mode domain, in this Chapter the idea of a fully reconfigurable transmitter with a current-mode approach is presented: the whole transmitter is operated in current from the baseband to the RF upconversion and the main filtering function is implemented just before the active mixer, as in the voltage-mode case. Moreover, Class A/B working is introduced in various blocks to save power. The prototype has been realized modifying the transmitter presented in the previous Ch. 2 and the changes will be described in the second part of the Chapter. Measurements of the prototype will also be given at the end of the Chapter.

3.1 Full Current-Mode Approach

3.1.1 Introduction

There were two main limits in the transmitter showed in the previous Ch. 2:

- the voltage Biquad is used to filter the DAC replicas only.
- a V-I converter is necessary, but, strictly speaking, it's a block that doesn't belong to the fundamental blocks of a transmitter.

The limited use of the active filter is a direct consequence of the presence of the V-I converter: since the last block of a voltage-mode baseband connected with a current-mode upconverter must be a linear V-I converter, there is no space for another active biquad at the end of the chain. Instead, a single RC pole is inserted, but it is not sufficient to suppress the most part of the out-of-band noise. In some other state-of-the-art transmitter [12], two passives poles are inserted after the V-I converter. The filtering of the entire baseband noise is for sure more effective for large frequency offsets, but not close to the signal bandwidth. To make it effective also in the close-in offsets there must be some pre-compensation in phase and amplitude of the signal in the digital baseband.

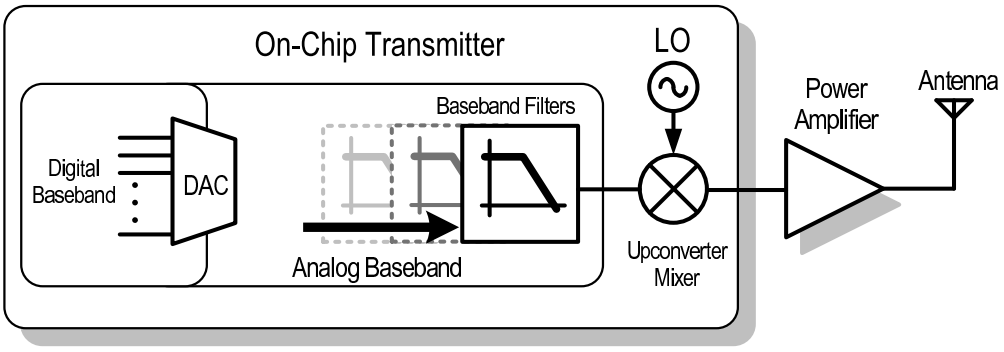

FIGURE 3.1: *Moving the filtering block at the end of the baseband can improve noise and power consumption.*

On the other hand, the possibilities of the voltage-mode transmitters are different, as seen in Ch. 1. In fact, the usual strategy is to put the whole filtering (high-order and low order) at the end of the entire baseband, just before the passive mixer [9, 11]. With this architecture, the whole filtering of noise, non-linearities and DAC replicas is done at the end of the chain, just before the upconverter.

This last one, usually, doesn't contribute to out-of-band injections (at least at maximum output power). Of course, other problems arises from the use of passive mixers (I and Q cross-talk, switched capacitor effect etc...), as already pointed out in Ch. 1.

We want then to apply the same idea also in transmitters with active upconverter: moving the filtering toward the end of the baseband (Fig. 3.1), as already done in voltage-mode transmitters.

3.1.2 Current-Mode Transmitter

The natural approach is then use an entire current-mode chain, instead of the mixed voltage/current-mode presented in Ch. 2. The block diagram of the proposed current-mode transmitter baseband is shown in Fig. 3.2. A current-steering DAC inject his current in a Variable Gain Amplifier (VGA) that will present an input virtual ground to limit the voltage swing at the DAC output that can degrade his linearity. The output current of the VGA will be the input signal of a current-driven filtering cell that will also drive the active mixer for the upconversion.

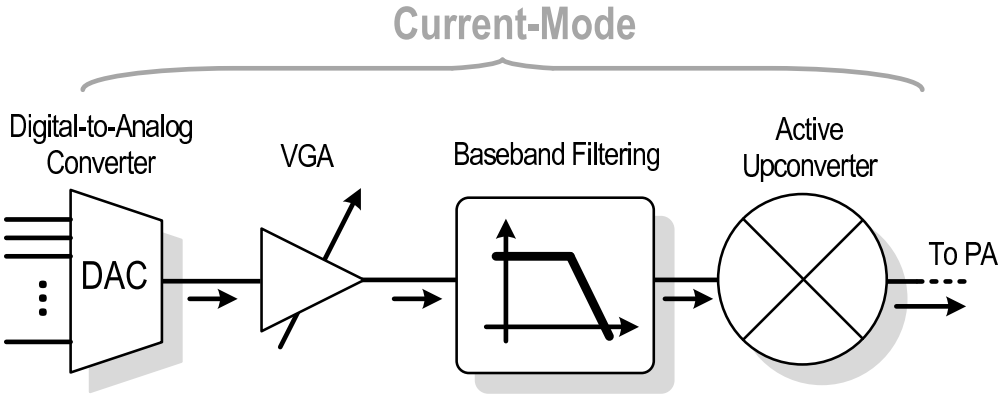

FIGURE 3.2: *Block diagram of a full current-mode transmitter.*

It is interesting to note that the flow of the blocks in the transmission chain is the opposite of those of a receiver chain in current-mode operation [20]. In the RX, after the antenna, an LNA provides the first amplification, while a mixer downconverts the signal to baseband. There, an active filter (Rauch Biquad) eliminates the interferers before amplifying the signal in the resistive feedback network, that acts as a VGA. After, the voltage output will be converted with an ADC.

In the transmitter chain, while the LNA becomes a Pre-Power Amplifier+Power Amplifier (see Fig. 3.2), the preceding blocks have the same functions as the in the receiving situation, but in a reverse order from a signal-flow point of view.

3.2 Current-Mode Transmitter: Building Blocks

3.2.1 Modifications to a Mixed-Mode Baseband

The starting point to discuss the path toward a full current-mode TX is the mixed-mode architecture described in Ch. 2 (Fig. 3.3): after a voltage DAC, a filter (a Biquad cell) eliminates the DAC replicas and his output is transformed into a current through a virtual ground and a variable resistor, that acts as a Variable Gain Amplifier. The current is then mirrored toward the active mixer and, at the same time, filtered with an RC pole.

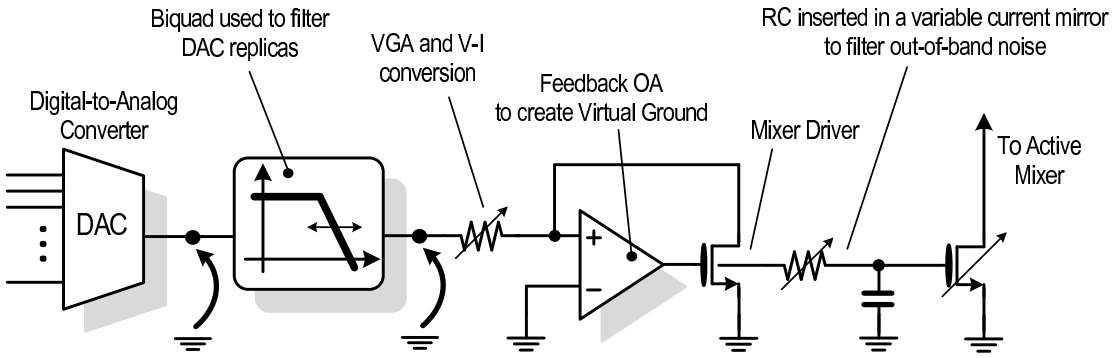

FIGURE 3.3: *Simplified schematic of a traditional mixed-mode transmitter baseband.*

To follow the idea proposed in Fig. 3.2 by changing the traditional scheme of Fig. 3.3, we have to:

- change the voltage DAC into a current DAC;
- eliminate the voltage Biquad;
- eliminate the variable resistor and introduce instead a block that implements the VGA;
- the V-I converter must be transformed into a filter and, in particular, a Biquad filter (since the old one has been eliminated).

The modifications are reported in Fig. 3.4. The VGA must have a low input

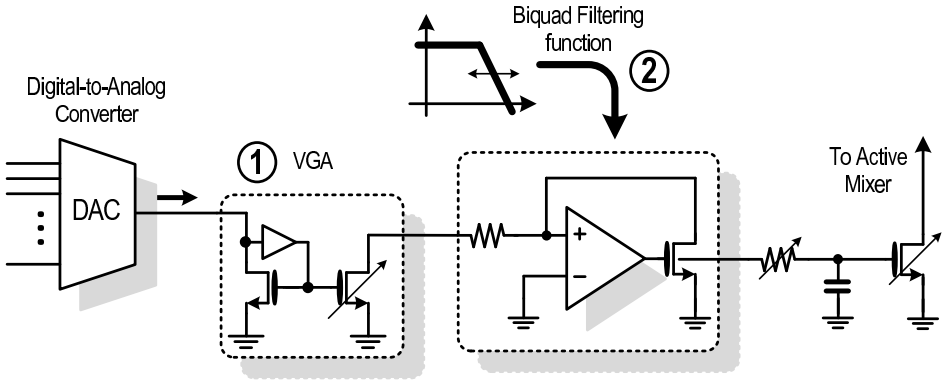

FIGURE 3.4: *Evolution from the mixed-mode to the current-mode transmitter.*

impedance and it must amplify the DAC output current, keeping a high output impedance to drive the following stage. A natural choice is then a feedback current mirror with a variable mirror factor. In fact, the same structure is used in the V-I converter, aside from the resistor.

For the Biquad current-driven cell, instead of the V-I converter, we'll have to introduce a passive network to perform a second-order filtering.

3.2.2 Variable Gain Amplifier

The main idea is to transform a regular current mirror into a low input impedance current mirror. A traditional current mirror has an input impedance of $1/g_m$, where g_m is the transconductance of the input transistor. Of course, it is possible to decrease this impedance by increasing the current biasing of the MOS, but this requires high power consumption: e.g., if we want an input impedance of 5Ω, following the classic equation $g_m = 2I_{bias}/V_{ov}$ and supposing an overdrive of $100mV$, we'll have to consume at least $10mA$ that is for sure preposterous in this kind of applications.

Feedback is the key to achieve virtual grounds. In the current mirror case, the introduction of feedback is shown in Fig. 3.5, in a single-ended version. The input branch of the current mirror is made of an NMOS and a PMOS, and a terminal of an OTA is connected to the drains while the other is connected to an AC-ground (a common-mode reference). The feedback creates a virtual short-circuit between the input node and the reference, leading to a low input impedance. Notice that

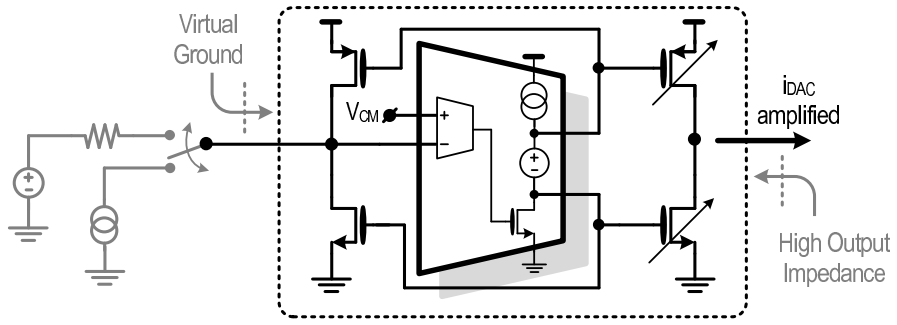

FIGURE 3.5: *Simplified schematic of the implemented VGA.*

this virtual ground, used to absorb a signal from a current generator, can be used also as a V-I converter, simply adding a resistor in series to a voltage generator (Fig. 3.5). The output stage of the OTA is a common-source stage, with a floating battery that drives the gates of the input and output branch of the current mirror. With this method, the two branches are driven in Class A/B.

3.2.3 Huijsing's Floating Battery [21] for a Class A/B VGA

A more detailed single-ended scheme of the OTA output stage proposed for the VGA is shown in Fig. 3.6. We'll check the behaviour of the output stage supposing that the first OTA stage in Fig. 3.5 has two outputs that exit in-phase. We'll be able to discuss it also in the case of a single output as a simpler case. The detailed schematic of the entire OTA will be given in the following sections.

The outputs of the OTA drive with the same phase the gates of M_{ps} and M_{ns}, that are connected through the Huijsing's floating battery [21]. Their drains drive then the gate of the (variable) output stage of the global VGA (the one of Fig. 3.5).

Two advantages come from the use of the floating battery. First, the output current is settled if all the transistors of the floating battery and their current are matched to the biasing network. In fact, if we neglect channel modulation, supposing that the current in the floating battery is $2I_b$ (decided by M_{ns} and M_{ps} that act as current sources) and the transistors M_{nb} and M_n are matched, then $V_{xb} = V_x$ and the current in M_x is equal to I_b, if it is matched to M_{xb}. The same goes for the current in M_y. With this method, the current in the output branch is well defined without the necessity of an additional common-mode feedback.

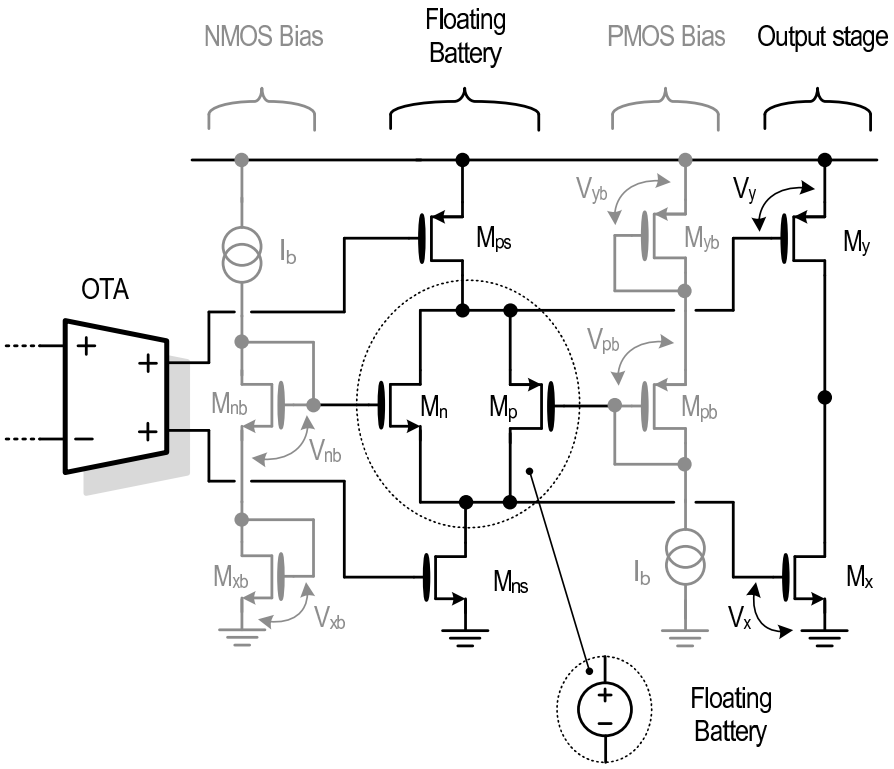

FIGURE 3.6: *Implementation of the floating battery in the OTA output stage.*

Second, the output branch works in a Class A/B fashion. This fact is easier to see with the simpler equivalent circuit in Fig. 3.7. Since the outputs of the OTA are in phase, it means that when a small negative signal is applied at the input of the OTA, M_{ns} will try to decrease his current and M_{ps} will try to increase his current. Of course, if we suppose that the output resistor r_o of M_{ps} and M_{ns} in Fig. 3.6 is infinite, they will not change their current, looking at the Kirchhoff law in the branch. In fact, their fixed current is represented in Fig. 3.7 by the two ideal current generators I_{dc}, while the signal-dependent part is represented by the two transistors. When the two in-phase signal v_{signal} are applied, M_{ps} and M_{ns} will make the V_{gs} of the transistors of the floating battery changing the partition of the current I_{dc}, ideally divided equally. The drain voltage change will drive the output stage and will increase and decrease the currents of M_x and M_y, respectively.

There will be the same behaviour also if the signal is coming only from the N-side of the battery. When the gate of transistor M_{ns} is decreased, the MOS will increase his drain voltage to maintain the same current flowing in the branch. The NMOS of the floating battery will then change his current and the PMOS will balance the change, as in the previous case.

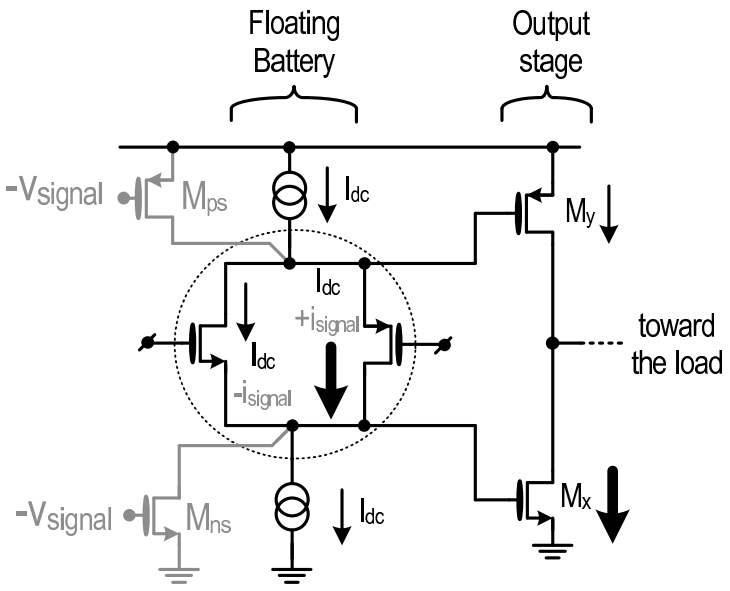

FIGURE 3.7: *Behaviour of the output stage with unbalanced signals.*

We can also see that the network acts actually as a short circuit for small signals (i.e. a battery). An essential schematic to measure the input impedance is shown in Fig. 3.8. A voltage probe v_x is inserted and an r_o is placed on the otherside to modelize the output impedance of M_{ps} of Fig. 3.7. If we use Kirchhoff law on the top node, we can get that

$$\frac{v_x}{i_x} = \frac{g_{mp} r_o + 1}{g_{mn}} \tag{3.1}$$

and, supposing that $g_{mp} r_o >> 1$ and that $g_{mp} \approx g_{mn}$, we get

$$\frac{v_x}{i_x} \approx r_o. \tag{3.2}$$

The input impedance is then the impedance that it's seen beyond the battery: the positive feedback of the network permits to eliminate the floating battery and it is seen as a short circuit for small signal analysis.

3.2.4 Current-Driven Biquadratic Cell

The next step is to insert the biquad filtering function inside the traditional V-I converter. Since the cell is now current-driven (with the VGA), the linear conversion is not needed and the resistor and expecially the feedback will not be used anymore to make a linear V-I conversion. Instead, the feedback will be used to create a virtual-short and the resistor will be part of a passive network aimed to

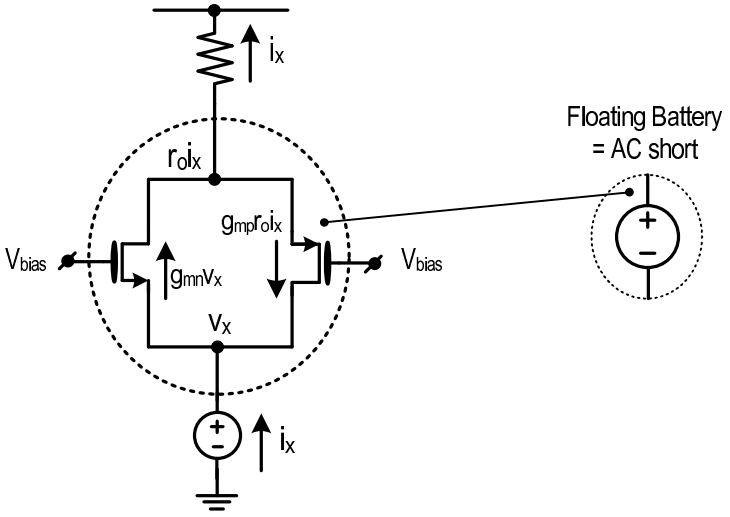

FIGURE 3.8: *Input impedance of the floating battery.*

create a second-order active filtering on the current signal. The idea is reported in Fig. 3.9.

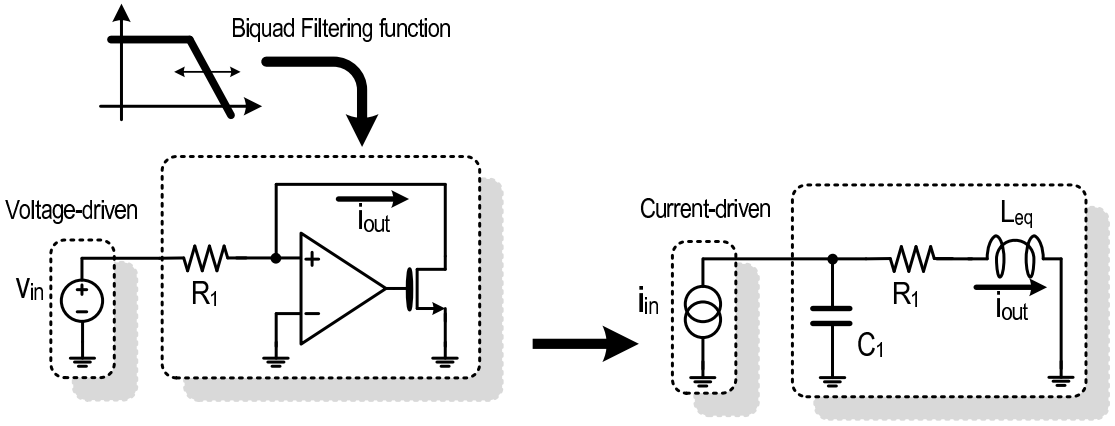

FIGURE 3.9: *Conceptual idea of transforming the V-I converter into a current-driven biquad filter.*

The voltage-driven cell must now become a current-driven cell and implement an active filtering. The simpliest structure that implements this filtering is an RLC network as shown in Fig. 3.9, with a grounded capacitor C_1 and the series of resistor R_1 and inductor L_{eq}. The transfer function $H(s)$ is given by

$$H(s) = \frac{i_{out}}{i_{in}} = \frac{1/L_{eq}C_q}{s^2 + s\frac{R_1}{L_{eq}} + \frac{1}{L_{eq}C_1}}. \tag{3.3}$$

Keeping the same R_1, the voltage-driven V-I converter can be transformed into an equivalent current-driven RLC network with two step. First, inserting a grounded

capacitor C_1. Second, creating, instead of a virtual ground, an inductive behaviour in series with the resistor R_1.

Usually, the inductive behaviour is authomatically created in virtual grounds when the G_{loop} of the feedback system is decreasing, and hence the low impedance seen at low frequency increases. But this is an unwanted result, dependent on the lack of G_{loop} at high frequencies. Instead, we want to implement by purpouse this behaviour, indipendentely from the G_{loop} of the system. The way to do so is shown in Fig. 3.10.

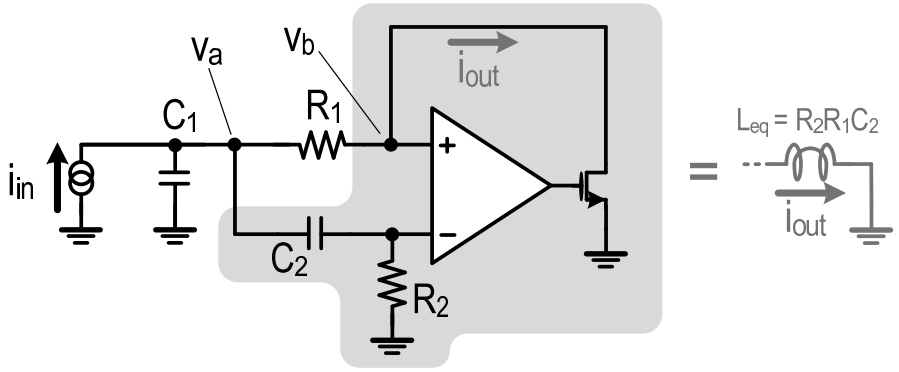

FIGURE 3.10: *Single-ended version of the current-driven biquad.*

First of all, we want to check the input admittance Y_{in} of the structure, that will be given by $Y_{in} = i_{in}/v_a$. From Kirchhoff at the input node, assuming an ideal Op Amp, we have

$$i_{in} = v_a sC_1 + \frac{v_a - v_b}{R_1} + (v_a - v_b)sC_2, \tag{3.4}$$

since the two input terminals of the Op Amp are short-circuited. We also have

$$v_b = v_a \frac{R_2}{R_2 + \frac{1}{sC_2}} = \frac{R_2 sC_2}{R_2 sC_2 + 1} \tag{3.5}$$

as a result of a voltage partition. Substituing Eq. 3.5 inside Eq. 3.4, we get

$$i_{in} = v_a sC_1 + \frac{v_a}{R_1} - v_a \frac{R_2 sC_2}{(R_2 sC_2 + 1)R_1} + v_a sC_2 - v_a \frac{R_2 sC_2}{R_2 sC_2 + 1},$$

that can be simplified and the Y_{in} can be extracted as:

$$Y_{in} = \frac{i_{in}}{v_a} = \frac{s^2 C_1 C_2 R_1 R_2 + s(C_1 R_1 + C_2 R_1) + 1}{(sR_2 C_2 + 1)R_1}. \tag{3.6}$$

The numerator of Eq. 3.6 shows a couple of poles, while the denominator is a high-pass function. If we look at Fig. 3.9, we can see that, at frequencies below the resonant frequency, the input impedance is given by $R_1 + sL_{eq}$. The same goes in this new structure: at low frequency, below the frequency of the complex conjugate poles given by $1/C_1C_2R_1R_2$, the input impedance is given by $R_1 + sC_2R_1R_2$. We deduct that the architecture implements the wanted inductive behaviour and the L_{eq} is equal to $R_2R_1C_2$.

To get the transfer function i_{out}/i_{in}, it is now sufficient to use Eq. 3.5 in the definition:

$$\frac{i_{out}}{i_{in}} = \frac{(v_a - v_b)/R_1}{i_{in}} = \frac{v_a - v_a\frac{sR_2C_2}{sR_2C_2+1}}{R_1 i_{in}} = \\ = \frac{v_a}{i_{in}}\left(\frac{1 - \frac{sC_2R_2}{sC_2R_2+1}}{R_1}\right) = \frac{1}{Y_{in}}\left(\frac{1 - \frac{sC_2R_2}{sC_2R_2+1}}{R_1}\right) \tag{3.7}$$

and, finally, insert the expression for the Y_{in} found in Eq. 3.6 to get

$$\frac{i_{out}}{i_{in}} = \frac{1}{s^2C_1C_2R_1R_2 + sR_1(C_1+C_2) + 1} = \frac{1}{\frac{s^2}{\omega_0^2} + \frac{s}{Q\omega_0} + 1}. \tag{3.8}$$

The implemented transfer function is then a low-pass with ω_0 and Q defined as

$$\omega_0 = \frac{1}{C_1C_2R_1R_2}, \qquad Q = \frac{\sqrt{C_1C_2R_2}}{(C_1+C_2)\sqrt{R_1}}, \tag{3.9}$$

so the cut-off frequency and the Q are entirely dependent on the passive network introduced. Notice that, if we suppose $C_1 >> C_2$, we can simplify the Q to

$$Q \approx \sqrt{\frac{C_2R_2}{C_1R_1}}, \qquad \text{(if } C_1 >> C_2\text{)} \tag{3.10}$$

the ratio of the two time constants, and this result will be useful when considering the cut-off frequency reconfigurability of the biquad introduced.

3.3 Prototype and Measurements

3.3.1 3^{rd} and 5^{th} order filtering configurations

The idea of a full current-mode transmitter has been implemented modifying the transmitter presented in the previous Ch. 2. We didn't want to change the original

current-steering DAC nor eliminate the additional voltage Biquad for the 5^{th} order filtering, so we had to adapt the introduced VGA to the architecture. See Fig. 3.11 for the details on the block diagram.

Since in the previous version the DAC had an output resistor to make it working as a voltage DAC, another resistor R_{IN} has been added in front of the virtual ground of the VGA. If the added resistor is $>> R_{DAC}$, then the DAC behaviour and performances are still the same as before. More precisely, in the case of 3^{rd} order filtering configuration, his output current undergoes a resistive partition. In the 5^{th} order filtering configuration case, the additional Biquad works in voltage-mode, so the DAC is working essentially as in the original design. After that, a V-I conversion takes place on the virtual ground of the VGA and the current-mode approach returns. Let's first discuss the system in the 3^{rd} order configuration.

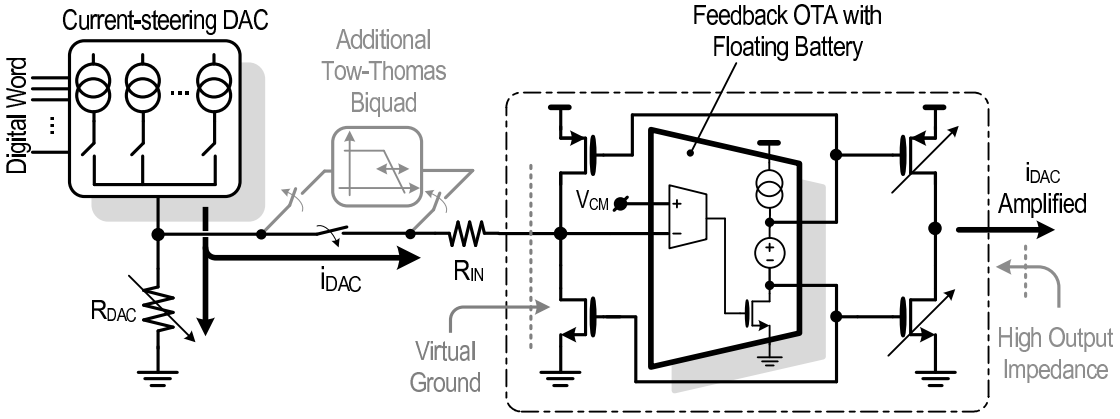

FIGURE 3.11: 3^{rd} *and* 5^{th} *order filtering configuration of the DAC+Additional Biquad+VGA section.*

3.3.2 VGA for 3^{rd} order filtering configuration

The main goal is to change the architecture without changing the performances of the surrounding blocks: the DAC must behave like before. Hence, as already discussed, the inserted R_{IN} must be $>> R_{DAC}$ to not degrade the DAC performances. The ideal situation would be instead putting the virtual ground of the VGA directly at the ouput of the DAC: two advantages will income. First, the output current will flow entirely in the VGA without any loss in a resistive partition. Second, the DAC will not see any voltage swing at his output and this will improve his linearity.

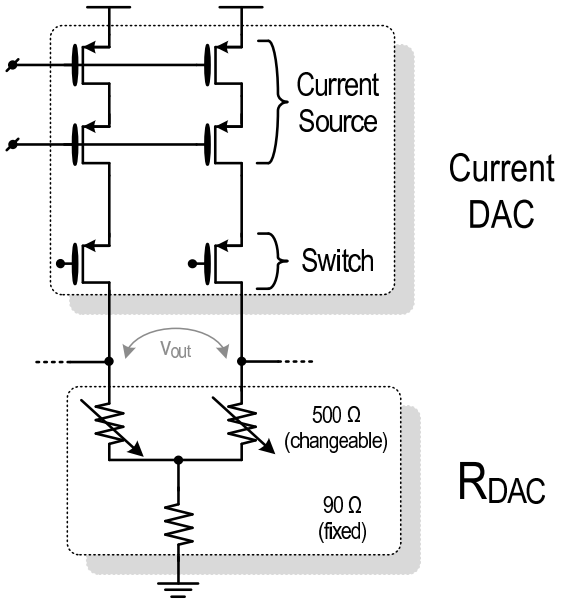

FIGURE 3.12: *Conceptual schematic of the DAC.*

The downside of this approach is that, in this design, the DC working point of the virtual ground and the DAC output are largely different. The DAC must stack three PMOS (two for the current source and one for the switching, see Fig. 3.12) in saturation and hence the output DC voltage must be near ground to work properly, taking into account also the voltage swing in presence of signal. The VGA virtual ground must instead be at $V_{dd}/2$ for the Class A/B working simmetry. Hence the necessity of a R_{IN} to provide the DC difference. In particular, when the DAC is producing zero signal at v_{out}, two currents of $500\mu A$ flow in R_{DAC} (depicted in Fig. 3.12: notice that the resistor of 500Ω is variable to provide attenuation in the output voltage signal). The DC output voltage will then be $(1mA \cdot 90\Omega) + (500\mu A \cdot 500\Omega) = 0.34V$, if we suppose that the input impedance of the next stage is infinite. Actually, it is not: in the 3^{rd} order case an R_{IN} of $2.75k\Omega$ has been decided (his value is in trade-off with the mirror factor of the VGA, that means power consumption). Since the virtual ground of the VGA in Fig. 3.11 is placed at $V_{dd}/2 = 900mV$, there will be a voltage partition between R_{IN} and R_{DAC} that will add DC bias to those $0.34V$. Obviously, if the $900mV$ is maintained, a current coming from the VGA toward the R_{DAC} will be required and the only element that will be able to provide is the PMOS transistor in the input branch (see Fig. 3.11): this will perturb the equilibrium of the Class A/B input mirror. Furthermore, this additional DC current will be mirrored to the scaled-up output branch, translating into power consumption and DC-offset for the next blocks. Later we'll show how to deal with this problem.

The detailed schematic of the differential OTA inserted in the current mirror is shown in Fig. 3.13. The current generator i_{in} represents the current coming from the resistive partition of the output current of the DAC, while the R_{in} are the differential input resistors from Fig. 3.11. The input virtual ground is achieved with a loop including a two-stage OTA and a third stage given by the input branch of the current mirror plus the resistors R_{IN}. Notice that in this case we didn't use a multipath OTA as the one described in Ch. 2. The fact is that, since a strong filtering will be inserted downstream, it is possible to relax the performances of this OTA. Non-linearity and noise added out-of-band will be eliminated with the following high-order filter, so we can save some current consumption.

The first stage is a differential couple with a differential resistive load. The structure permits to set the DC operating point of the active load without the necessity of a common-mode feedback, since, from a common-mode point of view, the load is made up of two MOS diode-connected (M_{n1} and M_{n2}). From a differential point of view, instead, the load is made up of the two resistors R, since the gate of M_{n1} and M_{n2} is a virtual ground.

The second stage is an NMOS common-source using the floating battery described before. The current is set by the current generator I_{b2}, while the transistors M_{cm} are a part of a common-mode feedback (not shown in Fig. 3.13) forcing the common-mode voltage of v_{in+} and v_{in-} to the reference $900mV$ ($= V_{dd}/2$). The floating battery outputs drive then the PN couple of the input branch and also the output branch, making the whole block absorbing and injecting the current signal in Class A/B.

The system without the capacitors C would have 2 dominant poles (the outputs of the first and second stage) and a non-dominant pole (the output of the third stage). With a traditional Miller compensation, the pole-splitting would move far apart the two dominant poles, resulting in a pole in $1/(gm_{ns}r_oRC)$ (indicating r_o as the load resistance of the second stage) and another one in gm_{ns}/C_{par}, where C_{par} is the parasitic capacitor in parallel with M_{ns}, diode-connected by C at high frequency. Moreover, a potential left-plane zero could help the phase margin. However, the second pole could give issues in the stability margins since the parasitic capacitors of the variable current mirror can be relatively large. To eliminate the problem, it is necessary to increase the current consumption in M_{ns} to increase his gm_{ns} and push the pole at higher frequency.

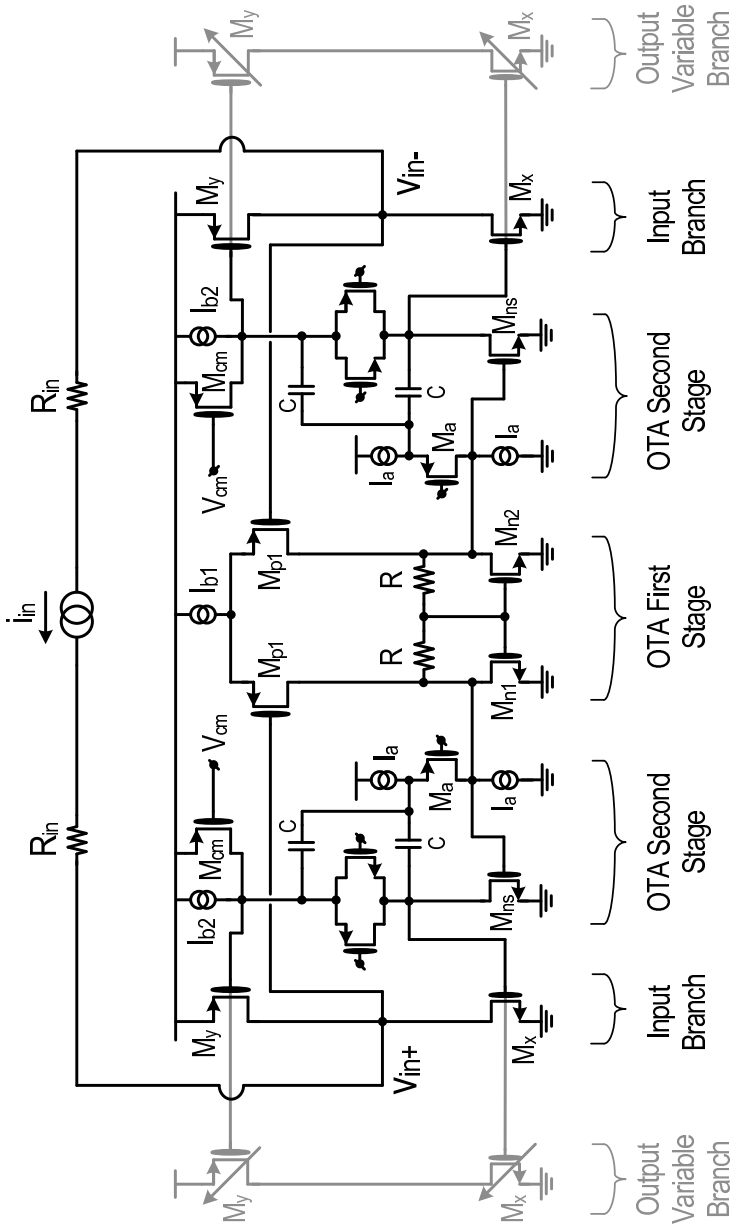

FIGURE 3.13: *Detailed implementation of the VGA OTA.*

A more practical solution is the Ahuja compensation [22]. His principle is represented in Fig. 3.14, taken from the circuit in Fig. 3.13, and compared with a traditional Miller compensation. The current generator i_{signal} with R represents M_{p1} with the load of the first stage. In each case, the dominant pole is given by $1/(gm_{ns}r_oRC)$, if r_o is the output impedance of M_{ns}. The non-dominant pole is instead improved by the high frequency loop-gain gm_aR in the Ahuja case, compared to the traditional Miller case. In fact, calculating the output impedance at high frequency in the first situation, we get $1/gm_{ns}(gm_aR)$ while in the second case only the $1/gm_{ns}$ of the diode-connected transistor. Moreover, a left-plane zero

gm_a/C (changeable with gm_a) is introduced in the first case, while a right-plane zero gm_{ns}/C (changeable into a left-plane one with an additional resistor) in the second case.

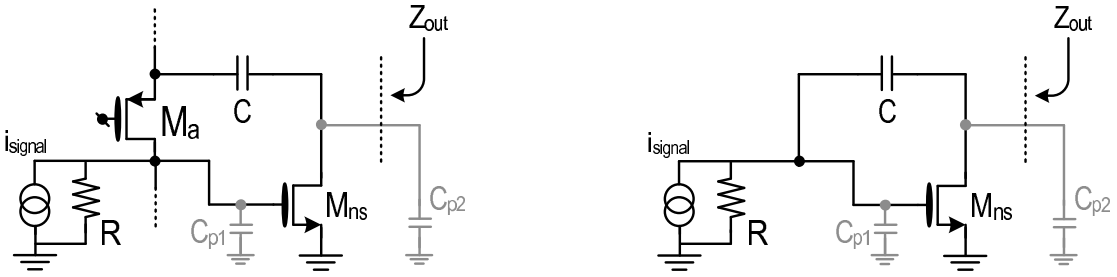

FIGURE 3.14: *Comparison between Miller and Ahuja compensations.*

In Fig. 3.13 we also saw that there are two compensation capacitors for each side. This is due to the Class A/B working. Indeed, looking at Fig. 3.15, if we suppose to eliminate one capacitor and we also suppose to drive the amplifier in deep Class A/B, we will see that the output NMOS will be almost off. In this situation, the capacitor C will be connected to the source of the NMOS of the battery that is carring the whole bias current since the PMOS of the battery is off. Supposing that the output resistance of the current generator I_b is finite, the Miller gain will drop and stability issues can arise. With two capacitors, instead, this problem is resolved since at least one capacitor is always on a high impedance node, providing compensation.

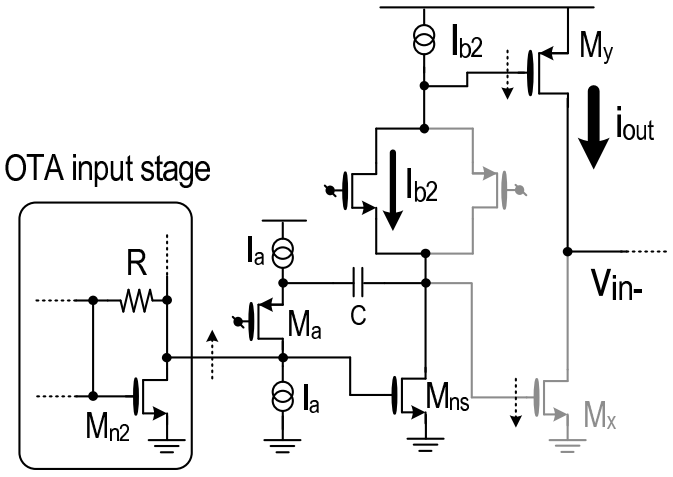

FIGURE 3.15: *Class A/B working of the output stage.*

The current consumptions for this stage are mainly decided by noise, stability and linearity.

- A high input g_m is necessary in the first stage to provide low noise performances and hence the current I_{b1} has been decided to be $90\mu A$;
- The second stage sets the position of the parasitic poles, defining the stability margin of the gain loop: thanks to the help of the Ahuja compensation, a current of $160\mu A$, divided between I_{b2} and the common-mode feedback transistor M_{cm}, is decided for this branch;
- Finally, the Class A/B quiescent current in the mirror branch sets the linearity of the output signal and the current consumption: a quiescent current of $5\mu A$ is forced through the floating battery feedback in the input current mirror branch, meanwhile at the output branch this value is amplified with a factor programmable from 32 to unity.

At the beginning of this section we also talked about the problem of connecting the DAC output with the virtual ground of the OTA (that have different DC voltages) through a resistor. Using superposition and so turning off the DAC currents, we can see that there will be a voltage partition of the virtual ground on the two resistors R_{IN} and R_{DAC} and so a current must be drawn. The voltage common-mode feedback of the OTA will react on the transistors M_{cm} to increase the current in the input PMOS M_y and decreasing the one in M_x so as to provide the current $900mV/(R_{DAC} + R_{IN})$ on the series resistors and keep the common-mode voltage to $900mV$. This will, however, change the DC conditions of the current mirror, limiting his performances.

This current injected in the resistive network is dependent on the value of the resistors (notice again that the R_{DAC} is variable to provide attenuation to the signal) but also will change following temperature and spread of the resistors. If a fixed current generator was used to provide this current, any mismatch would act on the feedback current mirror changing once again his DC working point and presenting a DC offset current for the following stages (that is amplified in the output mirror branch, leading to a furthermore harmful higher current consumption). We need then a feedback to adjust everything automatically and follow all these variations. The implemented feedback is reported in Fig. 3.16.

A copy of the input branch of the mirror is connected to a resistor R_{ref} biased with I_{ref}. When the PMOS will try to draw more current than the equilibrium situation, the DC voltage on the resistor will rise and, compared to the reference

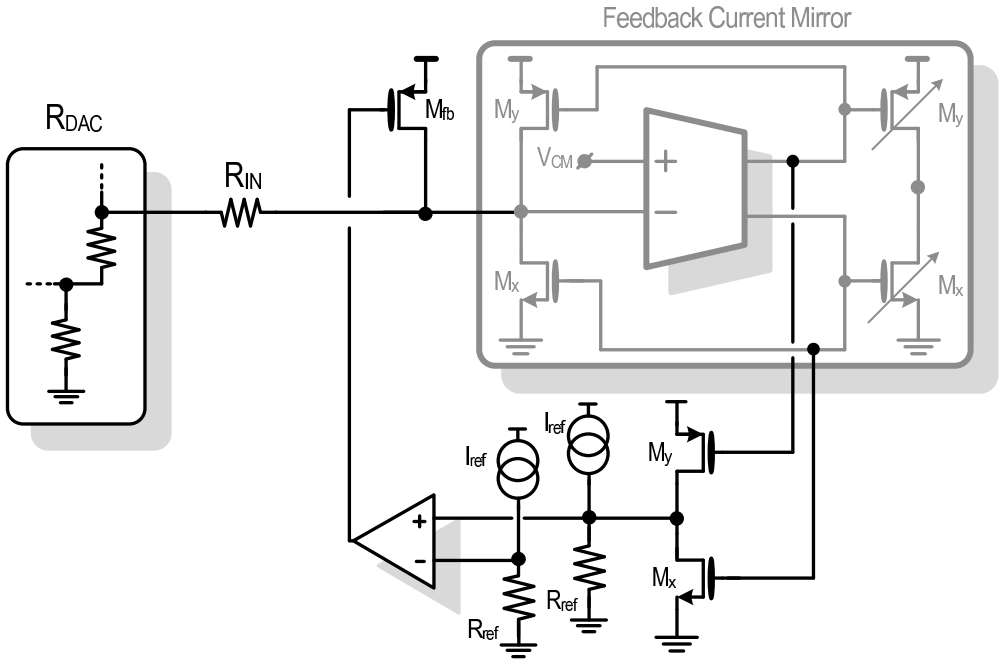

FIGURE 3.16: *Input feedback assuring the current for the DC voltage offset.*

with an Op Amp, it will drive the PMOS M_{fb}. With this feedback, M_{fb} will provide the necessary current for the voltage partition on R_{IN} and R_{DAC}, without disturbing the DC operating point of the whole mirror. Since the stability of this loop is particularly critical because the loop interacts with other common-mode loops and since it is only used for DC offsets, his bandwidth is quite narrow to ensure stability.

3.3.3 VGA for 5^{th} order filtering configuration

When the additional Biquad is added in front of the VGA, the virtual ground and the resistor R_{IN} will be now used as a V-I converter, since the output signal of the Tow-Thomas Biquad is a voltage. In the before discussed case, R_{IN} was chosen $>> R_{DAC}$ to not disturb the behaviour of the DAC. In this new configuration, this is not necessary since the Biquad interfaces the DAC and we can scale down the resistor to increase the transconductance gain of the V-I converter: the limit will be his noise. We decided then to halve the resistor R_{IN}. Moreover, the additional Biquad inherited from the design seen in Ch. 2 already implements a voltage gain of 2 from the input to the output. So, summarizing, the DAC output voltage is amplified by a factor of 2. Furthermore, the following R_{IN} is now halved, so the

incoming signal current in the VGA is four times the value in the 3^{rd} order filtering configuration.

Consequentely, a system of switches has been implented to increase the W/L of the input branch of the mirror while keeping constant the variable array of the output branch: the current for each input branch is now $20\mu A$. Since the g_m of the input branch has increased, another set of switches decreases the current I_{b1} (see Fig. 3.13) of the OTA differential couple from $90\mu A$ to $70\mu A$ to maintain approximately the same gain-bandwidth product of the loop gain of the system.

Finally, the DC ouput of the Biquad and the DC of the virtual ground are now equal, so the feedback to provide the DC current is turned off.

3.3.4 Current-driven Biquad's Multipath OTA

All the considerations done in Ch. 2 about the use of OTAs instead of OAs are still valid. The same goes, at this level, also for the importance of the multipath structure: in fact, only an RC filtering will follow, so linearity and noise performances must be very demanding.

The current-driven biquad presented previously has an Op Amp using both the input terminals (Fig. 3.10). First of all, the Op Amp will be in the practical implementation an OTA. Second, in the differential implementation there is the need for a four inputs and two outputs OTA. Finally, the Class A/B output stage presented in the previous Ch. 2 will be reused also in this design.

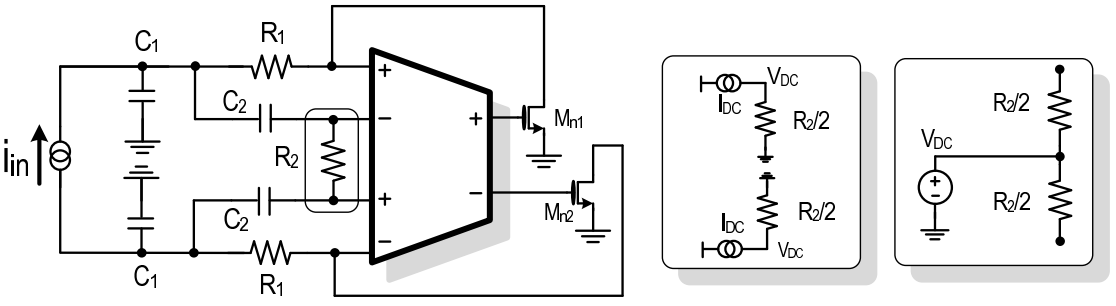

FIGURE 3.17: *DC biasing of the current-driven biquad.*

The final differential implementation is represented in Fig. 3.17. The transistors M_{n1} and M_{n2} represent the Class A/B output stage. The resistor R_2 is in reality

divided in two resistors to give the DC reference for the OTA. Two methods can be implemented:

- the two resistors $R_2/2$ are grounded and a current generator injects a I_{DC} to get $V_{DC} = I_{DC} \cdot R_2$. The DC current generator must change if the resistor is changed (see later) and his noise must be lower than the resistor, i.e. his g_m must be $<< 2/R_2$, so the overdrive of the transistor of the current sources must be high.
- a voltage reference placed in the middle of two $R_2/2$. Since the capacitor C_2 will block the DC current, the voltage reference will be copied on the other terminals of the OTA through the common-mode feedback described later. The voltage reference must be very good, i.e. his output resistance must be lower than R_2 up to the cut-off frequency of the filter;

In this prototype we chose the second possibility.

The internal structure of the OTA is the already introduced multipath architecture (Fig. 2.5) represented more detailed in Fig. 3.18. Two things must be noticed. First, the main path and the feedforward path require a 4-terminals input. Second, an additional selectable current consumption is highlighted in the second stage: this is required when the OTA drives the *RC* filter inside the ouput current mirror with large bandwidth signals (e.g. LTE20). In this situation, the risk of slew-rate on the capacitor can arise, so the current biasing is increased. Attention must be paid to the polarity of the various g_m stage to get the global feedback to be negative.

The g_m blocks are realized as differential couples with active loads. In Fig. 3.19 the schematic of the first stage (two gm_1 in parallel) of the main path is represented. Since the outputs are connected on the same load C_1, a common-mode feedback (CMFB) sense the output voltages and reacts to keep it at $V_{cm} = 900mV$ [23], acting on the bias current I_{b1}.

3.3.5 OTA Common-Mode Feedbacks (CMFBs)

For what concerns the output stage (constitued by the stage gm_2 and the Class A/B gm_3, already described in Ch. 2), two type of common-mode feedbacks

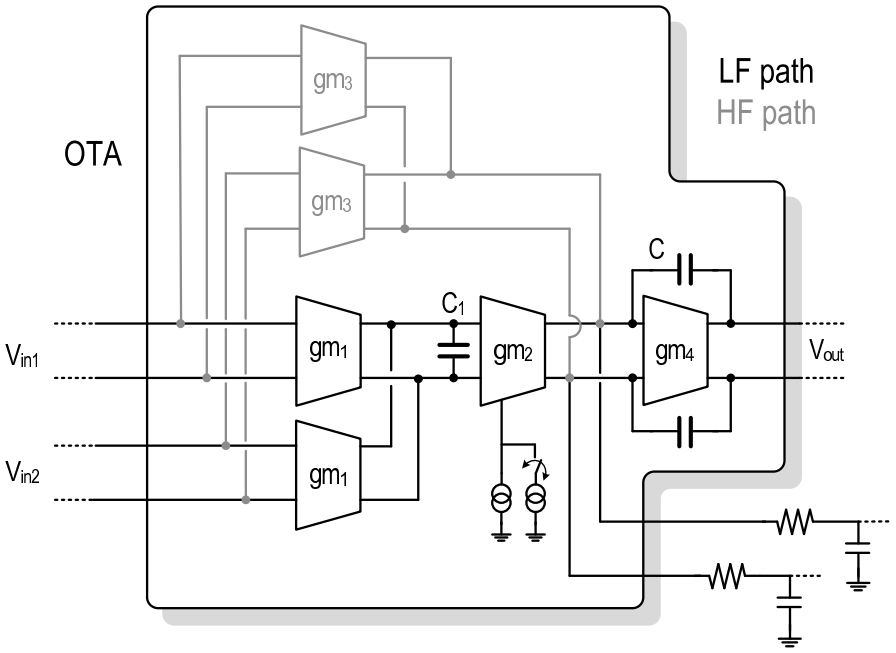

FIGURE 3.18: *Block diagram of the multipath OTA.*

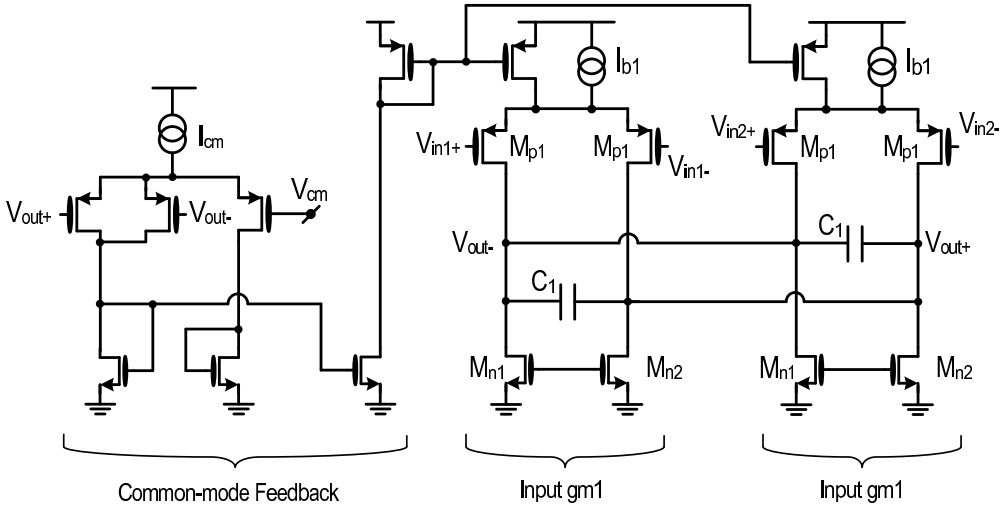

FIGURE 3.19: *Schematic of the input gm_1 of the OTA.*

(CMFBs) are necessary. First, a feedback that controls the quiescent bias current of the output PN stage. Second, a feedback that controls the output voltage of the same stage, setting it to $900mV$. In Fig. 3.20 and Fig. 3.21 the two CMFBs are represented. The transistors $M_{pin+}, M_{pin-}, M_{nin+}, M_{nin-}$ represents a simplified schematic of gm_2 with his load, while the presence of the feedforward gm_3 (that has the same structure of gm_2) is omitted for simplicity.

The current CMFB senses the common-mode voltage at the output of the stage gm_2 with a passive network and it compares it with a diode-connected transistor

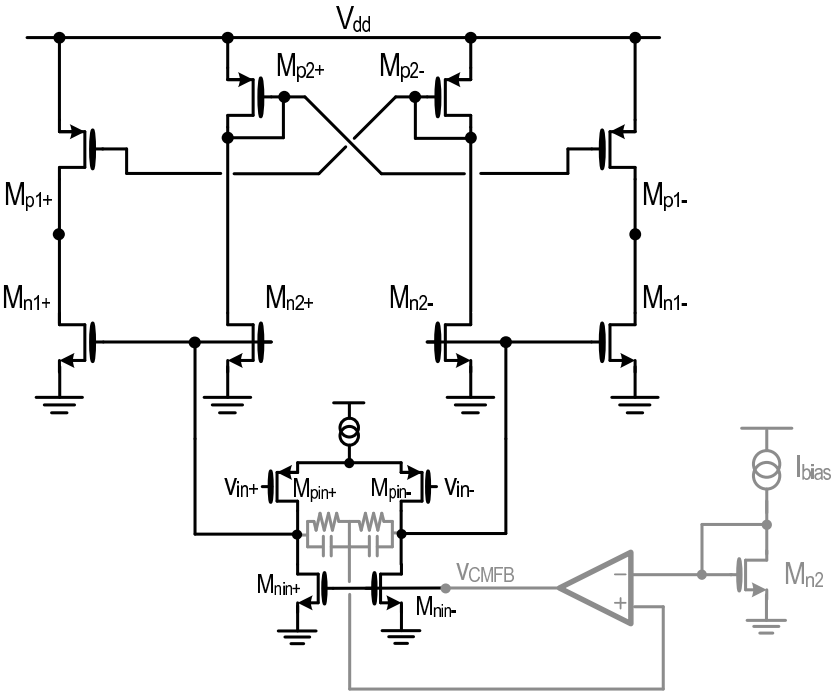

FIGURE 3.20: *Current common-mode feedback of the OTA output stage.*

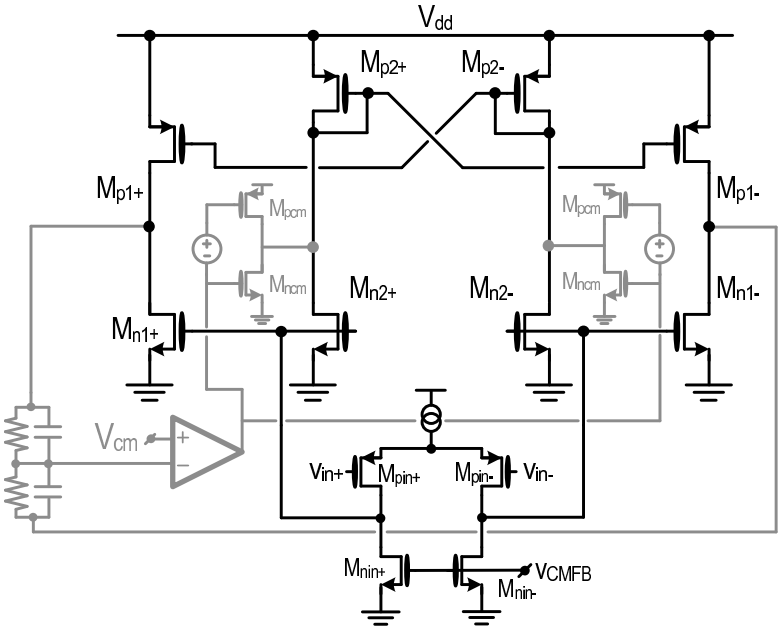

FIGURE 3.21: *Voltage common-mode feedback of the OTA output stage.*

matched with M_{n2} biased with a current I_{bias}. If the two voltages are different, the Op Amp reacts and change the bias current in the OTA output stage until the equilibrium is reached and his bias is equal to the reference. The voltage CMFB senses instead the common-mode output voltage of the Class A/B stage. When it is different from the reference V_{cm}, the transistors M_{pcm} and M_{ncm} working in

Class A/B thanks to a floating battery (described before), injects or draws the exact amount of common-mode current until the equilibrium is reached.

3.3.6 Power Consumptions

A few considerations about the tight bond between noise and power consumption must now be done. While in a receiver the in-band injected noise is the most harmful, in a transmitter is the one injected out of the signal bandwidth. For what concerns the noise of an OTA used in a receiver, for sure his noise is fundamentally given from the input differential couple, so the input stage must draw much more current than the rest of the architecture. Two benefits are given from this: the differential couple's g_m is higher and then the input referred noise lower and all the noise of the successive stages reported at the input are divided by a higher gain, lowering furthermore their contribution.

In an OTA used for transmitters the considerations on the power consumptions depends instead on his bandwidth. In fact, when a multipath architecture is used, the bandwidth of the input stage is narrower than the one of the following ones. So, at high frequency (i.e. out-of-band) their noise become more important when referred to the input of the OTA, since the gain upstream is decreased. The bandwidth of this OTA is around $120MHz$ (variable with the RC filter time-constant and the passive network in front of it), so the effect of every stage on the noise is sensible and especially the last stages. That's one of the reason why the most power consumption is moved toward the second stage and the feedforward stage (that decides the stability of the OTA), besides the fact that the second stage must drive a large capacitor.

In fact, the first stages gm_1 draw $56\mu A$ each. The second and the feedforward stages, instead, draw $400\mu A$ and $600\mu A$, respectively. Moreover, an additional power consumption is provided when processing large bandwidth signal, taking the consumption up to $1mA$ and $1mA$, respectively. The output stage has a reconfigurable bias current based on the reference given from the current CMFB: this is important especially for the consumption of the scaled-up Class A/B upconverter, that is the most power-hungry stage of the on-chip transmitter. The reconfigurable quiescent current of the stage permits a trade-off between nonlinearity/noise and current consumption and it can be programmed from $200\mu A$ (for each one of the four branches of Fig. 3.20 and Fig. 3.21) up to $450\mu A$.

3.3.7 Reconfigurability

To adapt the transmitter to the various standards, the passive elements of the new Biquad and of the RC pole have been made reconfigurable, following the cut-off frequencies of the original voltage Tow-Thomas cell. Using Eq. 3.10, the current-driven Biquad can change his ω_0 keeping the same Q (and in particular $Q = 1$ to perform a 3^{rd} order Butterworth) by changing or modifying the R values or the C values. The following associations have been made:

- for LTE20 and LTE15, the Biquad's and RC's ω_0 are $18MHz$;
- for LTE10, the Biquad's and RC's ω_0 are $9MHz$;
- for the standard with narrower bandwidth, the Biquad will be at $6.3MHz$ and the RC at $4.5MHz$.

While the first change from $18MHz$ to $9MHz$ was possible by doubling the capacitors of the Biquad and changing the R of the real pole, it was not possible to double the Biquad's resistor R_1 in the second step to halve the cut-off frequency. In fact, the last configuration gathers standard with $6dB$ and $9dB$ of PAR, so the voltage swing on R_1, that is maximized for $6dB$ PAR standards, would have saturated the VGA output for standards with $9dB$ PAR. Anyway, simulations have proved that no problems occurred in EVM, even if the filtering function was not exactly a Butterworth one. The same occurs when the additional Tow-Thomas Biquad is activated for the 5^{th} order configuration.

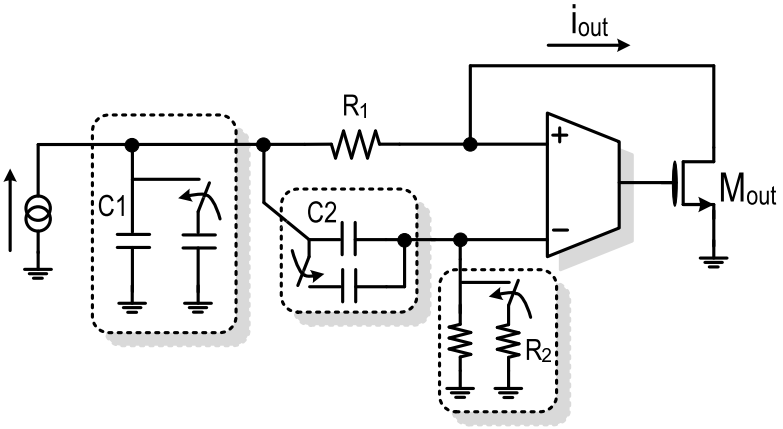

FIGURE 3.22: *Passives reconfiguration of the current-driven biquad.*

The reconfigurable Biquad's schematic is shown in Fig. 3.22. The capacitor C_1 has been made partially grounded because when a Class A/B working is implemented there is the risk that the contributions coming from CMFBs into the differential path arise and, since usually their power consumption is much less than the differential ones, their noise is higher: a grounded capacitor can anyway eliminate both differential and single-ended, with area costs. The values of the single-ended passives for the highest cut-off frequency are $R_1 = 175\Omega$ (that is the lowest value that was used in the V-I converter of Ch. 2), $R_2 = 3.6k\Omega, C_1 = 50pF, C_2 = 2.5pF$. The RC pole is instead changed by keeping the capacitor equal to $18pF$, while the resistor is 500Ω for the $18MHz$, $1k\Omega$ for the $9MHz$ and so forth.

3.3.8 Measurements

The transmitter has been implemented into a full reconfigurable transceiver, manufactured in $55nm$ CMOS technology. In Fig. 3.23 is reported the microphotograph of the entire transceiver and, on the right, the zoomed area of the transmitter. The whole analog section (baseband and upconverter) has a single $1.8V$ power supply and the active area occupied is $1.5mm^2$, divided almost equally between the RF section and baseband. Half of the baseband area is dominated by the capacitors of the filters.

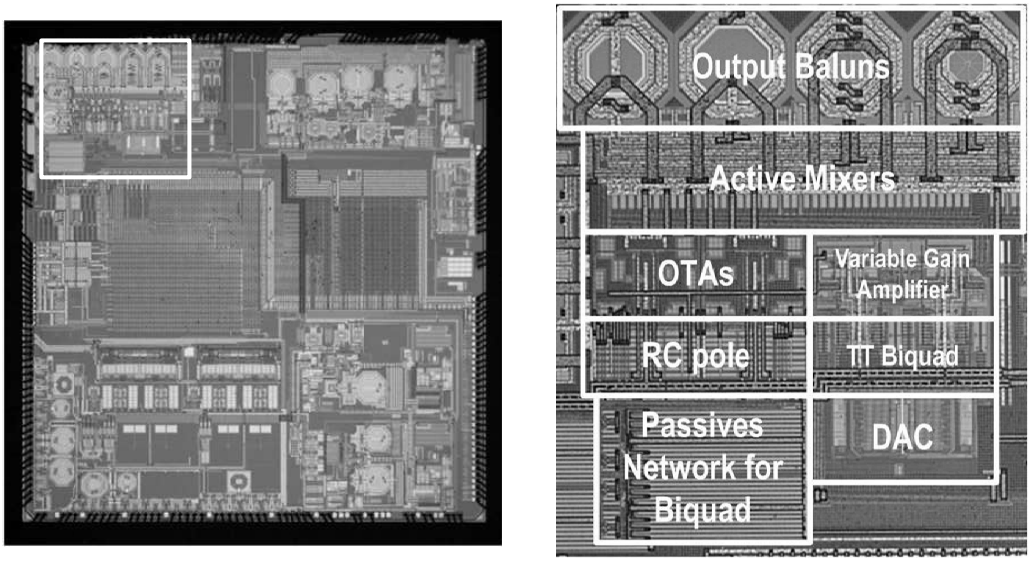

FIGURE 3.23: *Complete transceiver chip microphotograph (left) and transmitter details (right).*

The current consumption of the baseband (DAC excluded) and the upconverter when transmitting in Band2 for LTE20, LTE10 and 3G is reported in Fig. 3.24. Also in this design, the advantages provided by the Class A/B working of the up-

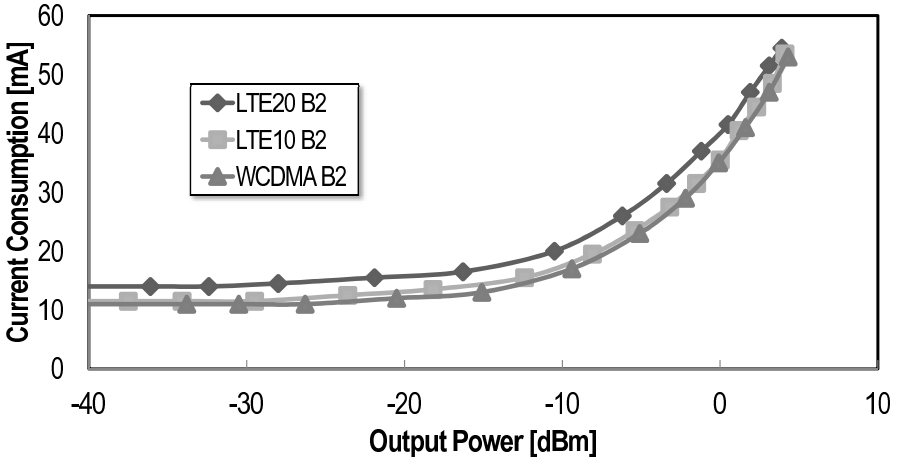

FIGURE 3.24: *Transmitter current consumption from* $1.8V$ *vs. the output power transmitted.*

converter are well seen changing the standard and seeing that the current consumption stays almost equal. When lowering the output power, the power-consuming section becomes the baseband, while the upconverter is just a small fraction. At low power (below $-10dBm$) is always less than $20mA$. Moreover, the possibility of scaling down the current mirror of the VGA to decrease the output power permits to decrease also the current consumption at very low output power. In Fig. 3.24 the current consumption is actually not decreasing really much because the additional implemented fractional mirror factor of the upconverter (discussed in Ch. 2) was not used during the measurements: the output power was scaled down with some attenuator at the balun level. The current consumption given from the upconverter is then still quite high even at low power outputs, but of course it can be lowered by using the fractional mirror factor instead of the RF attenuator, that is used at very low output power. The difference between 3G or LTE10 and LTE20 is due to a larger OTA current in gm_2, required to drive the last RC passive filter when his pole is tuned (as seen in Fig. 3.18).

In Fig. 3.25 the $ACLR$ parameters vs. output power for LTE20, LTE10 and 3G are reported for Band2 for the left-side of the RF signal, which has a worse behavior than the right-side. $ACLR_{E-UTRA1}$ and $ACLR1$ stay below $-42dBc$ and $-45dBc$ (for 4G and 3G) up to $4dBm$. At low power the linearity is limited by the baseband, while at higher power by signal compression in the up-converter.

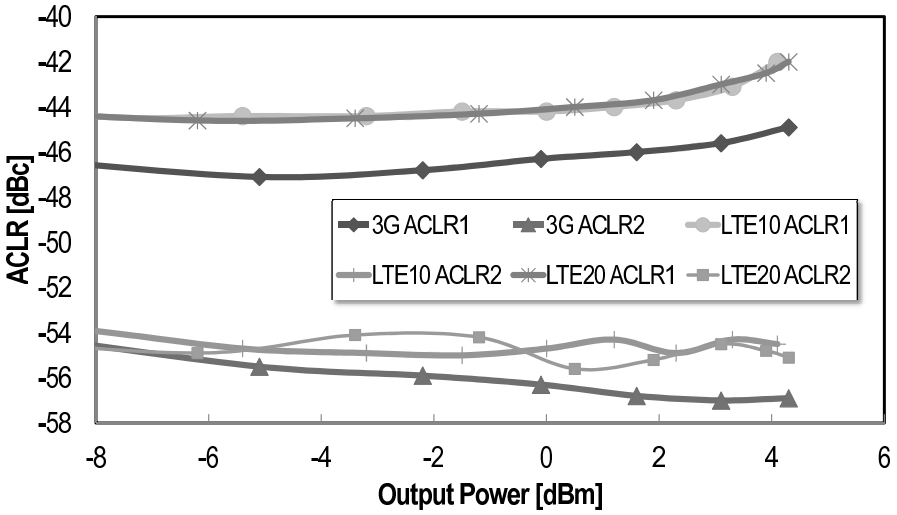

FIGURE 3.25: *Transmitter linearity parameters vs. power transmitted.*

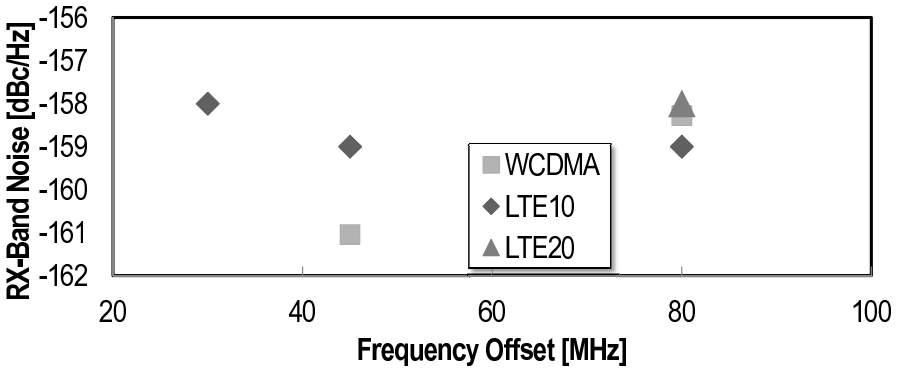

FIGURE 3.26: *Out-of-band noise performances vs. TX-RX frequency offset.*

RX-band noise measurements for the bands with the most critical TX-RX offsets are reported in Fig. 3.26, at $0dBm$ output power. The measures for 4G standard have been made with transmitted signals composed of partial Resource Block (RB), as specified by 3GPP and described in Ch. 1, while in the 3G case the full signal was used. The TX output was fed to the antenna port of a duplexer tuned to the target band and measurements were done on the RX port (with the TX port terminated on 50Ω), de-embedding the duplexer and cable attenuations. In this way, the transmitted signal was sufficiently suppressed by the stop-band of the duplexer to make it possible to measure the RX-band noise without saturating the spectrum analyzer. The worst case is the LTE10 Band17, with a TX-RX offset of $30MHz$, where the transmitter shows $-158dBc/Hz$.

Finally, a comparison with the state-of-the-art is given in Tab. 3.1 and Tab. 3.2: the first one use an entire voltage-mode (as described in Ch. 1) while in the second

table the comparison is done with two mixed-mode transmitter, the first one being decribed in Ch. 2.

		ISSCC2011 [9]			This Work		
Parameter	Unit	3G	LTE10	LTE20	3G	LTE10	LTE20
Band	-	5	12	2	5	17	2
Output Power (OP)	dBm	2.45	0.4	2.6	2.8	0.2	3.1
$ACLR_{E-UTRA1}$ @OP	dBc	-41.4	-41	-38.4	-43.4	-44	-43
$ACLR_{UTRA2}$ @OP	dBc	-63	-67	-59	-54.9	-57.4	-54.5
Consumption @OP	mW	111.2	101.2	126.4	97	90	93
RX-band noise @OP	dBc/Hz	-160.5^a @45M	-159^a @30M	-162.5^a @80M	-159^b @45M	-158^b @30M	-158^c @80M
Supply Voltage	V		1.1/2.5			1.8	
Area	mm^2		0.98			1.06^d	
Technology	nm		90			55	

(a) Carrier-to-Noise ratio; (b) measured with 20 RB; (c) measured with 50 RB; (d) without DAC, TT Biquad and 2 baluns

TABLE 3.1: *Comparison with a voltage-mode transmitter from ISSCC2011 [9]*

Tab. 3.1 compares for similar output powers and TX-RX offsets. This solution shows better $ACLR_{E-UTRA1}$ and less power consumption and, featuring only one (at $1.8V$) supply as opposed to two (at $1.1V$ and $2.5V$), is less costly. RX-band noise is generally a bit larger for our implementation. However, in [9] the noise testing condition used ($1MHz$ baseband tone [10]) is not 3GPP compliant and can give significantly better results. Chip area is less than 10% larger in this last implementation, but using an older technology.

Tab. 3.2 instead compares with two recent current-mode transmitters. Compared to the one described in the previous chapter, this solution shows an improvement of $4dB$ in LTE10 and $3dB$ in LTE20 in the RX-band noise and requires, respectively, about $3mA$ and $2mA$ less current thanks to the new BB that scales down current consumption with the current mirror. In LTE10, the corresponding improvement, although very small at 4dBm, is already about 16% at $-10dBm$ and exceeds 25% at very low output power. The two baseband current consumptions are shown in Fig. 3.27. On the other hand, area is increased by about 15%. Compared to [12] , we have better RX-band noise and ACLR, worse EVM with a drastic power consumption (especially at high output power) and area reduction. Finally, also in this case the use of a single supply as opposed to two reduces costs.

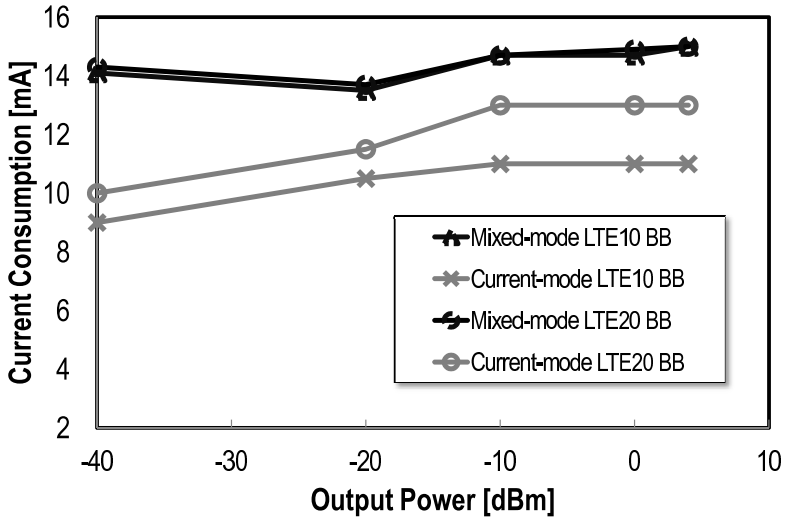

FIGURE 3.27: *Comparison of the baseband current consumptions.*

		[12]	[17]	This Work	[12]	[17]	This Work
Parameter	Unit	LTE10			LTE20		
Max Output Power	dBm	3.7	6	6	4	6	6
Output Power (OP)	dBm	3.7	4	4	4	4	4
$ACLR_{EUTRA1}$ @OP	dBc	-40.3	-44	-42	-40.3	-40.9	-42.5
$ACLR_{EUTRA2}$ @OP	dBc	NA	-55	-54.5	NA	-55	-54.8
Consumption @OP	mW	186	101	96	199	101	98
Consumption @-10dBm	mW	56	39.5	34	70	39.5	36
RX Noise@0dBm	dBc/Hz	-155 @30M	-154 @30M	-158 @30M	-157 @120M	-155 @80M	-158 @80M
Supply Voltage	V	1.55/2.7	1.8	1.8	1.55/2.7	1.8	1.8
Area	mm^2	5.06	1.3	1.5	5.06	1.3	1.5
Technology	nm		90			55	

TABLE 3.2: *Comparison with a current-mode transmitters from ISSCC2012 [12] and Ch. 2.*

3.4 Conclusions

In the effort to overcome the limits of a mixed-mode transmitter compared to a voltage-mode one, a current-approach has been introduced in this Chapter. The main limits were the introduction of a V-I converter that is not a fundamental block of a transmitter and his presence limits the filtering order when we use a power mixer. By changing the operating mode into the current domain, the signal processing doesn't need a V-I converter and hence the block can be reused to perform an high-order filter just before the upconversion. A detailed description of

the introduced blocks VGA and current-driven filter has been carried out, focusing also on the detailed implementation of the main OTAs. The realized prototype and the measurements closes the Chapter.

Chapter 4

Evolution of a Multi-Standard Transmitter

The challenge of minimizing power consumption and out-of-band emission forces the architecture of a transmitter baseband to be reduced to the main fundamental building blocks. In this Chapter, we introduce a basic architecture that reduces the contributors to noise and power consumption to the minimal, relying on the benefits that more advanced and scaled-down CMOS technologies will bring to the Digital-to-Analog Converter. The first part of the Chapter is dedicated to a proposed design for a baseband transmitter in $28nm$ *and some simulations are presented, highlighting the improvements in noise, linearity and power consumption. In the second part, a transmitter proposed for a* $55nm$ *technology is described, focusing in particular on the critical blocks of the chain. Finally, some preliminary considerations about the structure and the possible issues for a real implementation are given.*

4.1 Toward the Out-of-Band noise fundamental limit

4.1.1 Transmitter's fundamental blocks

As we already mentioned in Ch. 1, the fundamental and "natural" blocks necessary to implement a baseband transmitter are reported in Fig. 4.1: a Digital-to-Analog converter (to interface the digital baseband), a filtering block (to eliminate out-of-band noise and DAC replicas) and a programmable gain, that can be implemented into an additional block or inside the already implemented blocks.

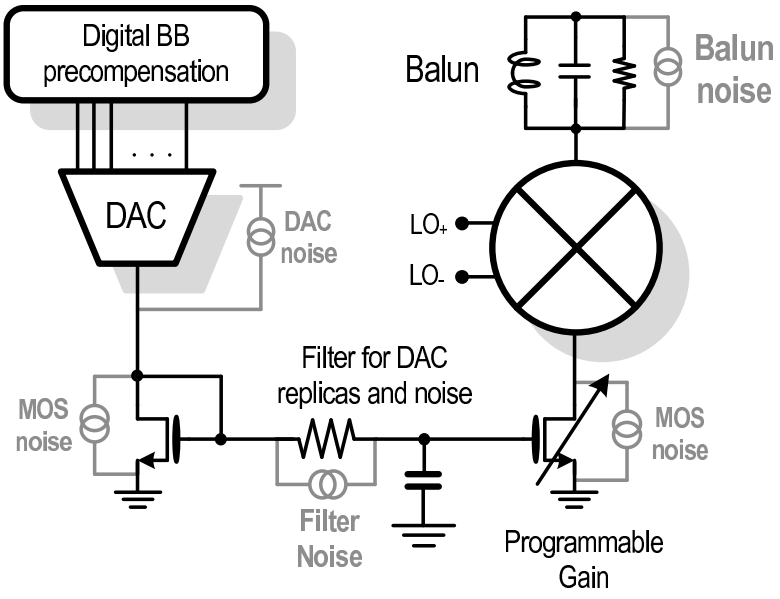

FIGURE 4.1: *Fundamental building blocks of a transmitter.*

The filtering block is only a first order pole: it is assumed that the DAC will exploit the advantage of the future CMOS technology downscaling, increasing the oversampling rate and hence pushing DAC replicas at high frequency. Also the quantization noise will be lowered, so the RC filter will eliminate only the thermal noise coming from the transistor and the DAC itself. Notice that, since the RC pole will be very close to the signal bandwidth to maximize the noise filtering, a digital precompensation of the droop must be implemented in the digital baseband. Furthermore, moving toward the RF side, three more fundamental blocks are necessary: an active mixer to upconvert the signal, a resonant load (a balun) to terminate the mixer and to interface it with the following external Power Amplifier

and a driving block for the mixer (i.e., the transcondutor of the traditional case of a Gilbert cell).

We can say that the noise coming from the balun is the lower intrinsic bound of the out-of-band noise, since it is impossible to eliminate it. Everything's else is extra noise. We can also see that is very difficult to create an architecture that eliminates the noise coming from the mixer and the mixer driver, while the upstream blocks can be filtered through the use of a filter, that will anyway be inevitably noisy.

In the following sections we'll describe the evolution of a multi-standard transmitter with the aim of lowering the out-of-band noise contributors toward the fundamental ones.

4.1.2 Structure of the Baseband Transmitter

A main limit of the transmitters described in the previous Chapters was the linearity of the current mirror with the RC pole inserted. As discussed in Ch. 2, the position of the cut-off frequency is limited by linearity issues: if the pole is too close to the bandwidth signal, the output current of the current mirror will be distorted. On the other hand, more out-of-band noise will be filtered.

Furthermore, power consumption is always an issue in transmitters: the idea of an entire Class A/B transmitter can be an improvement in this sense. In Ch. 3, the Class A/B working was extended from the mixer driver to the VGA and in the idea proposed in this Chapter it will be extended also to the DAC.

In Fig. 4.2 the basic idea of this new prototype is reported. A Class B DAC injects his current into two resistors R_{in} (in Fig. 4.2 only the right-side is reported for simplicity). The stacked MOS M_{in} can't absorb any current since his current is decided by the current generator I_{bias}, hence the current goes entirely in the resistor R_{in}, creating a voltage drop $v_{in}(t) = (i_{in}(t) + I_{bias}) \cdot R_{in}$, that is signal dependent. Since the V_{gs} of the diode-connected M_{in} is fixed, the gate voltage will move exactly like his source to maintain the same current I_{bias} and hence the gate voltage will be $v_{gate}(t) = V_{gs} + (i_{in}(t) + I_{bias}) \cdot R_{in}$. This is a linear voltage, hence it is possible to filter it with an RC filter (variable, taking already into account the reprogrammability of the transmitter) with a cut-off even inside the signal bandwidth without introducing non-linearity (but introducing a droop in

the signal that must be precompensated in the digital baseband, before the DAC). We can see that the trade-off between out-of-band filtering and linearity of the previous transmitters has now been broken.

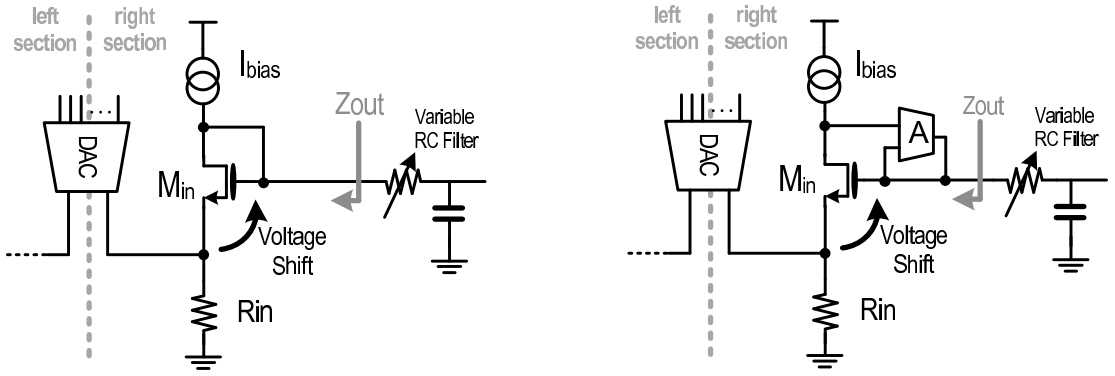

FIGURE 4.2: *Voltage shifter: without (left) and with (right) the OTA in feedback.*

The approach on the left of Fig. 4.2 is anyway not possible. The current necessary to drive the capacitor of the pole will inevitably come from the I_{bias} generator, and the system will not work any longer as a voltage shifter. Moreover, the driving impedance of the RC pole will be high ($1/gm_{in}$) but also signal-dependent. Finally, slew-rate can arise depending on I_{bias} and on the value of the capacitor.

A better approach is shown in Fig. 4.2, on the right. An OTA with a voltage gain of A is inserted to lower the driving impedance: the output impedance is now $r_{OTA}/(1+gm_{in}r_oA)$, where r_{OTA} is the output impedance of the OTA and $gm_{in}r_o$ is the intrinsic gain of M_{in}. Now the linear filtering is possible since the current for the capacitor is given by the OTA block, wihout introducing non-linearities.

The next step is to recreate the current signal and drive an active mixer: the idea is proposed in Fig. 4.3. The RC filter is the same of Fig. 4.2. His output voltage is fed to a scaled-up copy (with a factor of $N/2$: the reason of the $1/2$ factor will be clear later) of the input voltage shifter. The drain and gate of the transistor M_{out} are virtually shorted with an OTA that drives the gate of M_{csc}. The feedback forces the two terminals to be equal and hence the same situation of Fig. 4.2 is recreated here. In fact, since the bias current is $N/2$ the one at the input and the resistor is $R_{in}/N = R_{out}$, the feedback will make the transistor M_{csc} to provide for the missing DC current $NI_{bias}/2$ to perfectly copy the input voltage shifter. When a voltage signal v_{in} drives M_{out}, the voltage swing will be transferred on his drain and on the resistor $R_{out} = R_{in}/N$, while the current signal $v_{in}/R_{out} = Nv_{in}/R_{in}$ will be absorbed by the output MOS M_{csc} and taken to the

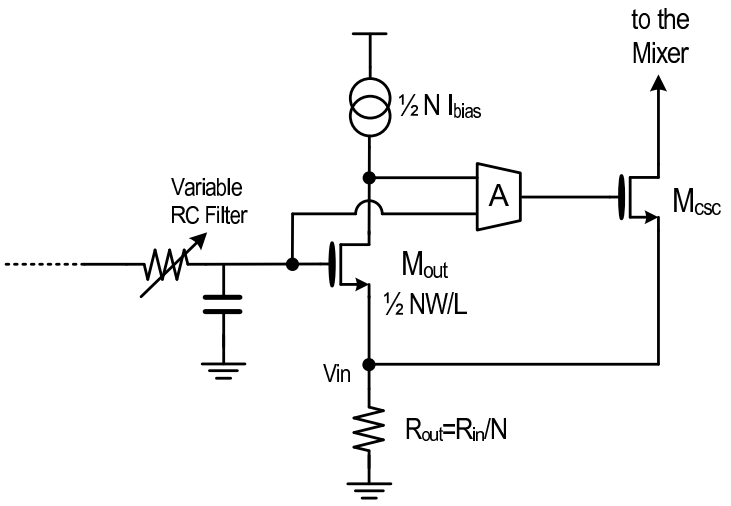

FIGURE 4.3: *Output stage driving the active mixer.*

mixer for the upconversion. The bias current NI_{bias} in Fig. 4.3 is simply equally divided between M_{out} and M_{csc}, but changing the geometrical factors it is possible to redistribute the total current in the two branches.

Finally, the mixer section is represented in Fig. 4.4. The two Class A/B current signals are coming from the two baseband loops through the transistors M_{csc}. Inside the mixer symbol, 4 switches forced to work in triode upconvert the current signal. At the output, two saturated balun selector protect the mixer from the output swing, while the Q-path is connected at the balun.

4.1.3 Considerations on the Architecture

The proposed transmitter is very essential: the DAC injects directly into the input branch of a current mirror that provides the signal to the active mixer. Inside this mirror, a filter for DAC replicas and noise is inserted, aiming to the fact that the DAC will have an high frequency clock and so his replicas will be far away from the signal and a single pole will be sufficient to eliminate them. The same goes for the out-of-band noise: since the TX is very essential, few noise sources are there. The limit for linearity is instead given by the gain and bandwidth of the two proposed loops. Power consumption and area are defined by the noise performances. Finally, since the filtering is now linear (as opposed to the versions of Ch. 3 and Ch. 2), the filter cut-off frequency can be moved very close to the signal bandwidth, provided that in the digital side a precompensation of phase and amplitude is inserted.

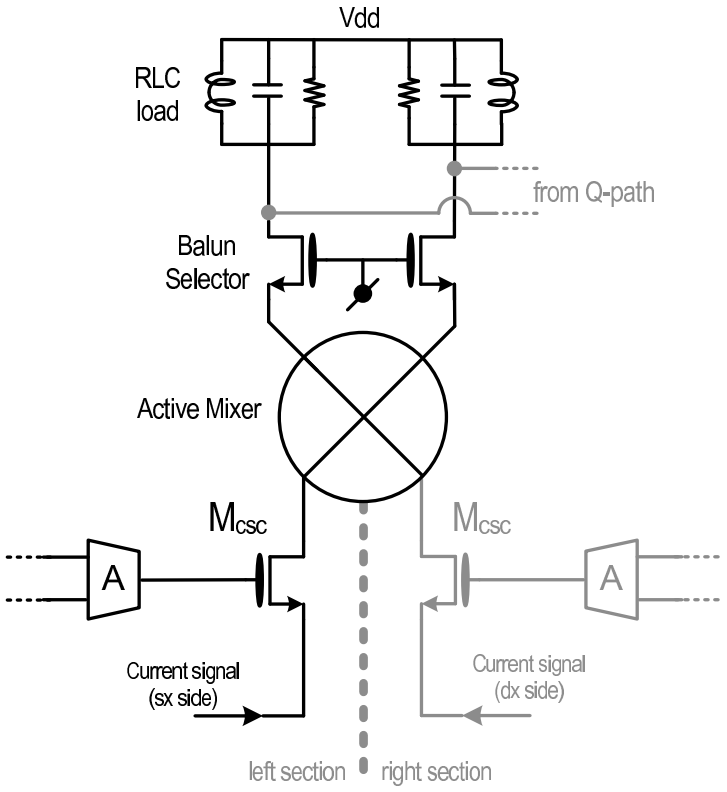

FIGURE 4.4: *RF section of the transmitter.*

Notice that the elements that will contribute to the out-of-band noise are the "fundamental" ones, as we discussed at the beginning of this Chapter: the DAC, the voltage shifters (that work as current mirrors), the RC filter and the balun. In fact, the two OTAs contributions are attenuated by the intrinsic gains of the input and output transistor. In the case of Fig. 4.2, if we suppose an input-referred noise voltage generator placed on the drain of the transistor, his noise must be transferred to the resistor to be processed toward the output. From the drain to the source the intrinsic gain of M_{in} attenuates the noise of the OTA. The same goes for the noise of the second OTA of Fig. 4.3.

M_{csc} is instead inside the loop and the feedback will make his noise recycle. In fact, if a current noise coming from M_{csc} is absorbed by the resistor R_{out}, his voltage drop will increase and the MOS M_{out} will react on the drain to maintain his DC current equal to $NI_{bias}/2$. The OTA will hence react on M_{csc} and make it reabsorb this noise current.

4.2 Simulations of the proposed structure

4.2.1 Reconfigurability and frequency behaviour

A simulation of the proposed transmitter chain was performed to confirm these ideas. Instead of the DAC, a precompensated (to eliminate the droop of the RC filter at the output) 4-tone full scale current signal (to get the PAR of $9dB$) in Class B drives the input voltage shifter. The tones are placed at the limit of the LTE20 bandwidth for a worst-case situation. The output signal is taken as the differential voltage on the balun, that has a differential resistance of 45Ω centered at the $1GHz$ carrier. The LO generator is simplified with an ideal clock generator that drives two real inverters. The resistor of the input voltage shifter is 300Ω while his bias current is $300\mu A$ (with the peak of the signal equal to $2mA$). This current basically sets the noise of the transistor of the voltage shifter. The RC pole has a cut-off of $12MHz$, very close to the LTE20 bandwidth signal, and a grounded capacitor of $20pF$, that sets the noise of the pole resistor. The active mixer is driven with two inverters and a voltage swing of $1.2V$, from $600mV$ to $1.8V$.

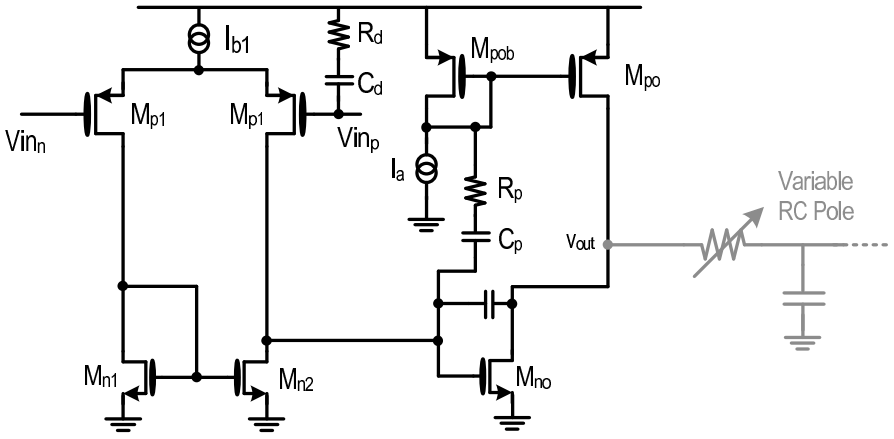

FIGURE 4.5: *Structure of the first OTA.*

The first OTA is a two-stage Miller amplifier (Fig. 4.5). The input is a differential couple with active load and a differential-to-single-ended conversion, while the output is a common-source stage: since the signal is a pure Class B, no fully differential OTA are necessary. The output stage has a bootstrapped Class A/B working. After a certain frequency, depending on the cut-off frequency of R_pC_p, the gate of M_{no} drives also the gate of M_{po}: the output stage hence works as a

Class A/B stage to save power but also to drive the large capacitor of the external RC pole.

An additional dominant pole (besides the one at M_{n2} drain and the output one that anyway is a pole-zero doublet) is added on the terminal Vin_p (that is connected to the M_{in} drain in Fig. 4.2) to perform a double slope OTA, like the ones discussed in the previous chapter, but without the use of additional stages. Notice that this pole must be placed after the bandwidth signal, otherwise the I_{bias} current in Fig. 4.2 undergoes a partition between R_d and the output resistance of the transistor M_{in}, creating disortion. Beyond $1/R_dC_d$, the added pole becomes a resistor, introducing hence a zero in the transfer function. The external variable RC pole, instead, is a capacitor at low frequency, but after the filter cut-off of $12MHz$ is a low resistor, so it can be ignored for stability considerations. Finally, the current consumption of the input stage sets the noise and the one in the output stage sets the linearity by defining the bandwidth of the output loop.

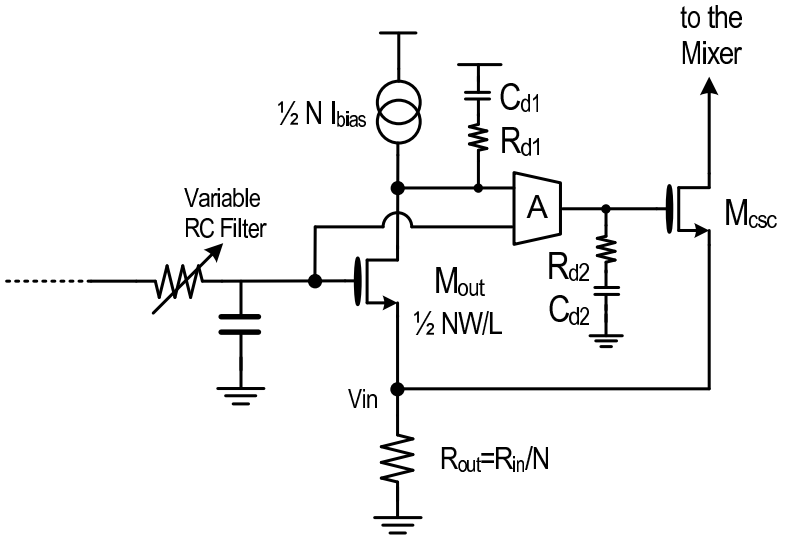

FIGURE 4.6: *Block diagram of the output OTA.*

The second OTA is instead simply a differential couple with a differential-to-single-ended conversion in the active load. The goal was to create again a double slope plus a zero in the transfer function, so two pole-zero doublets are added in high-impedance nodes, as it can be seen in Fig. 4.6. The issue is that this loop is dependent on the mirror factor N that complicates the design. Notice, however, that the DC gain of the loop, neglecting for now the poles, is practically indipendent from this factor. If we cut the loop at the gate of M_{csc}, we can see that this MOS acts as a source follower with a gain almost equal to 1 if we suppose

$gm_{csc}R_{out} >> 1$, that is independent from N. Even if $gm_{csc}R_{out}$ is not $>> 1$, the product is independent from N since the transconductance increases linearly with N and R_{out} decreases inversely proportional to N. The product will instead change in function of time (but keeping the same N) since the signal swing will change the current flowing in M_{csc}, i.e. his gm_{csc}. Then, from the M_{out} source to his drain, there is approximately the intrinsic gain of the transistor, $gm_{out}r_o$. When increasing N we increase also the dimensions of the MOS (i.e. his overdrive V_{ov} doesn't change when increasing the bias current) and therefore the intrinsic gain is constant, since

$$gm_{out}r_o \approx \frac{2N \cdot I_{bias}}{V_{ov}} \cdot \frac{1}{\lambda N \cdot I_{bias}}, \tag{4.1}$$

where λ is the channel-lenght modulation factor. Finally, the OTA gain is indipendent of N and the loop is closed.

For what concerns the frequency behaviour, the first doublet $C_{d1}R_{d1}$ is placed in a node with an impedance that depends on the mirror factor. In fact, when the mirror is scaled-up with the factor N, the impedance seen at the drain ($[1 + gm_{out}r_o]R_{out} + r_o$, with $R_{out} = R_{in}/N$) decreases and to keep the pole in the same position the capacitor C_{d1} must change in the opposite way. Hence, the unit value of C_{d1} is decided when $N = 1$ and then scaled-up. The resistor R_{d1} must change consequentely to keep the introduced zero at the same frequency. Finally, the pole-zero doublet $C_{d2}R_2$ is limited by the parasitic capacitance of M_{csc} when N is maximum, hence C_{d2} must be larger than that parasitic. For what concerns the bandwidth of the loop, it is also set by the DC current in the mixer branch: anyway, the bandwidth will be variable with the signal swing and attention must be paid to the stability of the loop. The DC current consumptions of the chain

Block	DC Current [A]
Input Voltage Shifter	$2 \cdot 300\mu$
First OTA	$\approx 2 \cdot 300\mu$
Output Voltage Shifter	$2 \cdot 20 \cdot 150\mu$
Active Mixer Branch	$2 \cdot 20 \cdot 150\mu$
Output OTA	$\approx 2 \cdot 300\mu$
Total	$1.8m(\text{BB}) + 12m(\text{RF})$

TABLE 4.1: *DC biasing of the transmitter.*

(I-path only) is reported in Tab. 4.1. The factor N is 20, giving an output power

of $\approx 3dBm$ on 45Ω. For what concerns linearity, the baseband shows a linearity (taken as an equivalent ACLR with the 4-tones signal, as described in Ch. 1) of $\approx 60dB$, while the mixer limit this value to $50dB$.

4.2.2 Out-of-band Noise Performances

The most interesting results are given from the noise contributors simulation, taken differentially at the balun at a frequency offset of $30MHz$ from the carrier at $1GHz$, reported in Tab. 4.2 and visualized in Fig. 4.7. As already pointed out, also the major contributors to out-of-band noise are the fundamental blocks: the input and output voltage shifter and, expecially, the RC pole, while the two OTA contributions are attenuated through the intrinsic gain of the transistors M_{in} and M_{out}. The fact that the RC pole is one of the principal contributors means that the further limit is given by the area of the device [13]. The SNR reached is $-160.5dBc/Hz$ at a frequency offset from the $1GHz$-carrier of $30MHz$, a very low value.

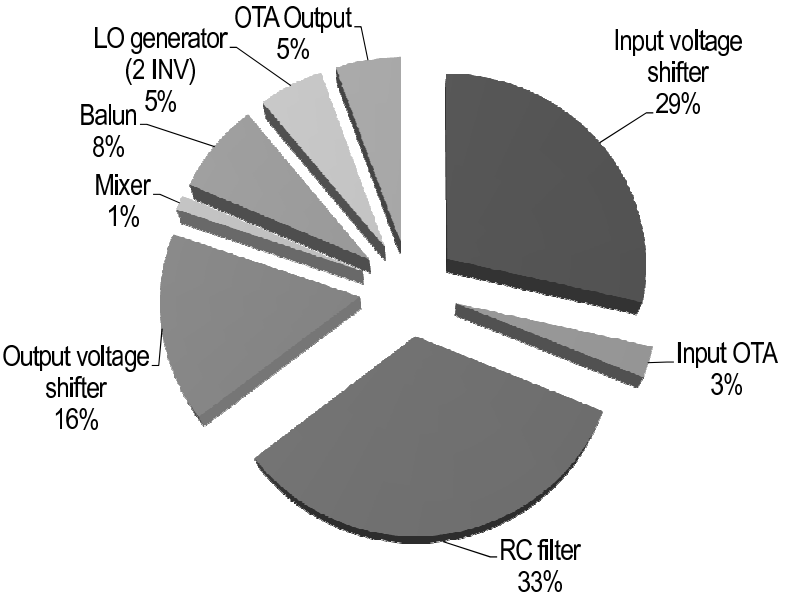

FIGURE 4.7: *Contributors percentage of the out-of-band noise.*

This structure can be really useful for those technologies (like $28nm$ and below) where it will be possible to increase the DAC clock (toward $1GHz$), so that his replicas and noise won't be a problem for the out-of-band emission because the high oversampling rate and the single-pole filter will be sufficient to make them negligible.

Contributor	Noise $[V^2/Hz]$	Noise %
R_{in}	$1.205 \cdot 10^{-18}$	14.89
M_{in}	$1.06 \cdot 10^{-18}$	13.13
First OTA	$2.06 \cdot 10^{-19}$	2.55
RC Filter	$2.63 \cdot 10^{-18}$	32.51
R_{out}	$4.41 \cdot 10^{-19}$	5.44
M_{out}	$8.17 \cdot 10^{-19}$	10.08
Second OTA	$4.29 \cdot 10^{-19}$	5.31
Active Mixer	$9.85 \cdot 10^{-20}$	1.2
RLC Load	$6.08 \cdot 10^{-19}$	7.5
LO generator	$4.26 \cdot 10^{-19}$	5.28
Total	$7.93 \cdot 10^{-18}$	97.9

TABLE 4.2: *Detailed contributors percentage and absolute values of the out-of-band noise.*

For this prototype, the idea is to use a $55nm$ and the DAC clock would be around $300MHz$. The strategy is then to change the architecture to achieve at least a 2^{nd} order passive filtering, but also using an N-type current-steering DAC, that will absorb current instead of injecting it. Notice that also in the just described system a 2^{nd} order filtering was possible: in fact, placing a capacitor in parallel to R_{in}, it was easily possible to achieve this filtering order, since the two passive poles would have been isolated. However, since the R_{in} is quite small and since the input Class B signal requires a grounded capacitor, the area would be prohibitive.

4.3 Transmitter Baseband with a 2^{nd} order passive filtering

To decouple the voltage shifter resistor from the cut-off frequency of an additional pole, we have to change the structure: the new architecture is shown in Fig. 4.8. Instead of the input voltage shifter, a single pole is introduced using a damped integrator with R_p and C_p. While before the DAC was injecting current in the resistor R_{in}, now the DAC is drawing current from the virtual ground. Moreover, the new OTA is driving the additional variable RC pole, already present. The following structure is the same as before. The DAC is still working in Class B and hence a fully differential OTA is not necessary, but only a single ended version is implemented. Furthermore, no common-mode feedbacks are used, that are

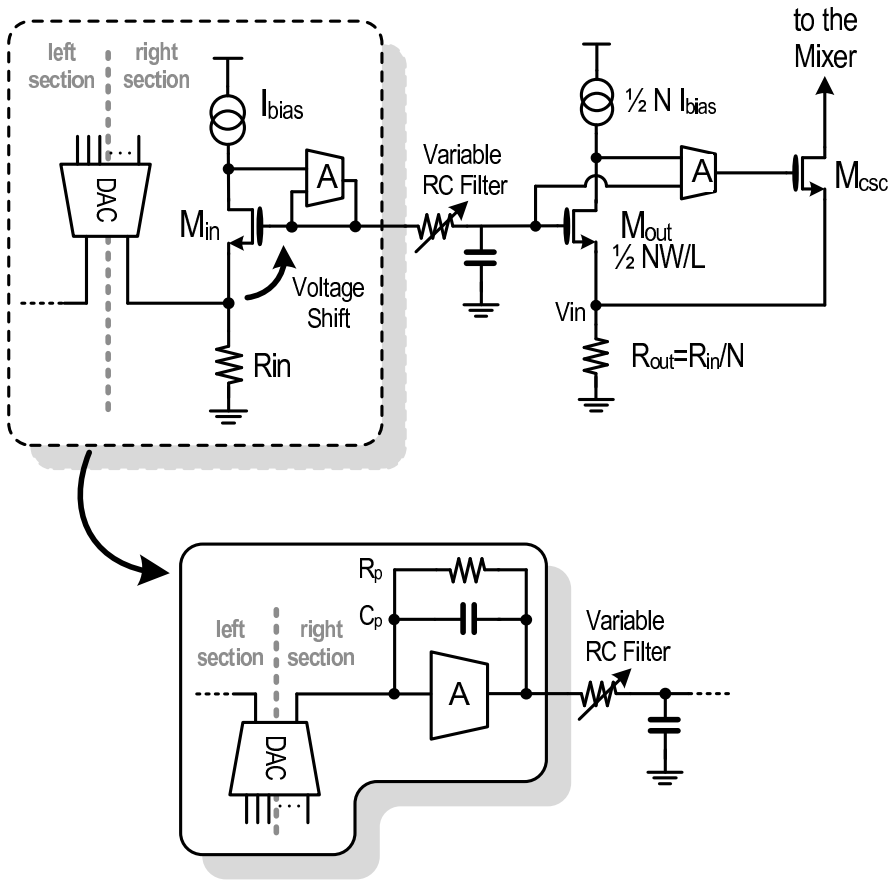

FIGURE 4.8: *Transformation from a first to a second filtering order.*

usually problematic in Class A/B or Class B systems since they introduce noise in the differential path.

4.3.1 Considerations on the Architecture

The DC working point is defined only by the input stage of the OTA: no DC current is drawn from the DAC, so the DC voltage is the same at the input and at the output of the OTA. In particular, this DC voltage must be the one that makes the following loop under the mixer working as before. This could be achieved if the input stage of the OTA is a scaled copy of the following voltage shifter, as reported in Fig. 4.9. With this approach, the DC voltage of the OTA output will make the V_{gs} of M_{out} the one necessary to force the voltage drop on R_{out} equal to $I_{bias} \cdot R_{in}$, adjusted by the loop.

However, there is another consideration to state: in the preceding proposed base-band, the noise of the first OTA was not an issue since it was attenuated by the

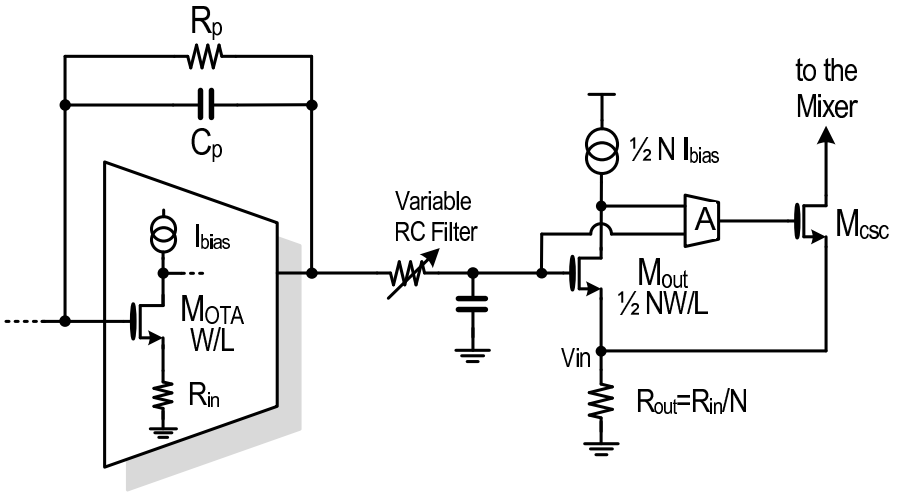

FIGURE 4.9: *Matching of the output stage with the input stage of the OTA.*

intrinsic gain of the input transistor M_{in}. In this case, instead, his noise goes directly at the output and it must be minimized. We can say that the noise of the original voltage shifter (coming from R_{in} and M_{in}) has been now substituted by the noise of R_p and the single-ended OTA. With this in mind and the fact that the dominant noise contributor (in band [24], at least) of an OTA is the input stage, we can see that the potential g_m of M_{OTA} is heavily degenerated with the resistor R_{in}. In fact, the equivalent Gm_{in} of this input stage is given by

$$Gm_{in} = \frac{R_{in}/g_m}{1/g_m + R_{in}}. \tag{4.2}$$

If we suppose a current I_{bias} of $300\mu A$ and an overdrive of $100mV$, we get $g_m \approx 2I_{bias}/V_{ov} \approx 6mS$, that is lowered to $\approx 2mS$ with the resistive degeneration of R_{in}. To exploit successfully I_{bias}, we introduce the complementary input stage proposed in [25] and depicted in Fig. 4.10 (the variable RC pole is omitted for simplicity). To match the voltage drops of the following stage, composed of a V_{gs} and a drop on a resistor, we introduce two current generators, I_{b1} and I_{b2}. The transistor Mn_{OTA} will have the same W/L and I_{bias} (possibly scaled) of M_{out} and the added current generators will provide the other voltage drop. Their noise will be attenuated by the RC filtering (I_{b1}) and by the OTA gain (I_{b2}).

4.3.2 Single-ended OTA for the damped integrator

The required architecture is a multipath OTA with a low-frequency path and a high-frequency path: the benefits of this structure are already been described in

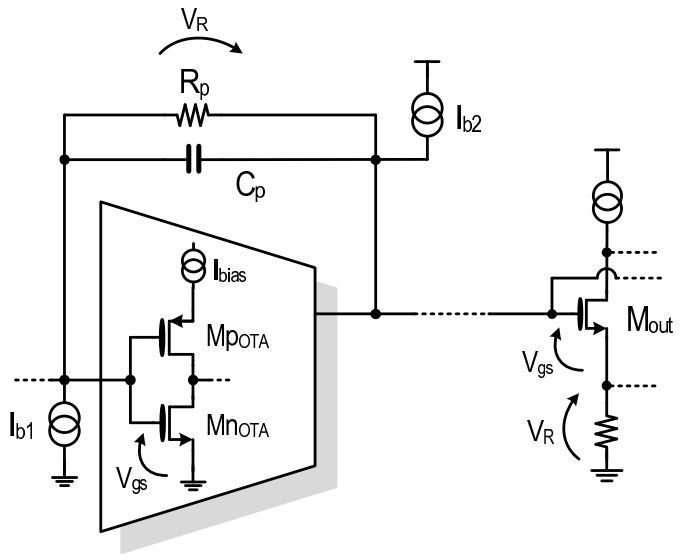

FIGURE 4.10: *Matching of the output stage with the input structure.*

Ch. 2. In Fig. 4.11 the detailed circuit diagram is depicted.

The input stage gm_1 drives the first dominant pole and the second stage gm_2. His output current, together with the output current of the feedforward stage gm_3 that skips the dominant pole at high frequency, is injected in the floating battery [21] that drives in Class A/B the output stage, composed of M_{pout} and M_{nout}. The two stages gm_2 and gm_3 share the same Miller compensation (R_m and C_m) around the output stage.

The input stages of gm_1, gm_2 and gm_3 are complementary transconductor stages: above a certain frequency, decided by the $1/gm_{pin}$ and the capacitors C_{in}, the current generators I_{in} are shorted and the equivalent input G_ms are doubled. Their output currents flow into low impedances, created with M_{nref} and M_{pref}, that are then mirrored through M_{nm} and M_{pm}. The DC currents are defined with a scaled-down replica of M_{nref} and M_{pref}.

Notice that the use of feedback allows to adjust the DC bias points: e.g. let's take a look at the input stage gm_1. If we suppose that the current I_{in1} is not flowing in M_{nin1} but directly into M_{pref1} because -we can say- his input impedance is lower than the r_o of M_{nin1}, the current of the two current mirrors will be unbalanced. Hence, M_{nm1c} will draw more current than M_{pm1c} and the drain voltage will be close to ground (i.e. decremented). Now suppose to put an ideal inverting stage after this first stage (since the first gm stage is non-inverting) and then close the loop with a resistor. The output voltage, that is now inverted and hence a positive

incremented voltage, will force the input transistor M_{pin1} to draw more current, until the equilibrium of the current mirrors is reached. The same reasoning can be extended to the entire OTA.

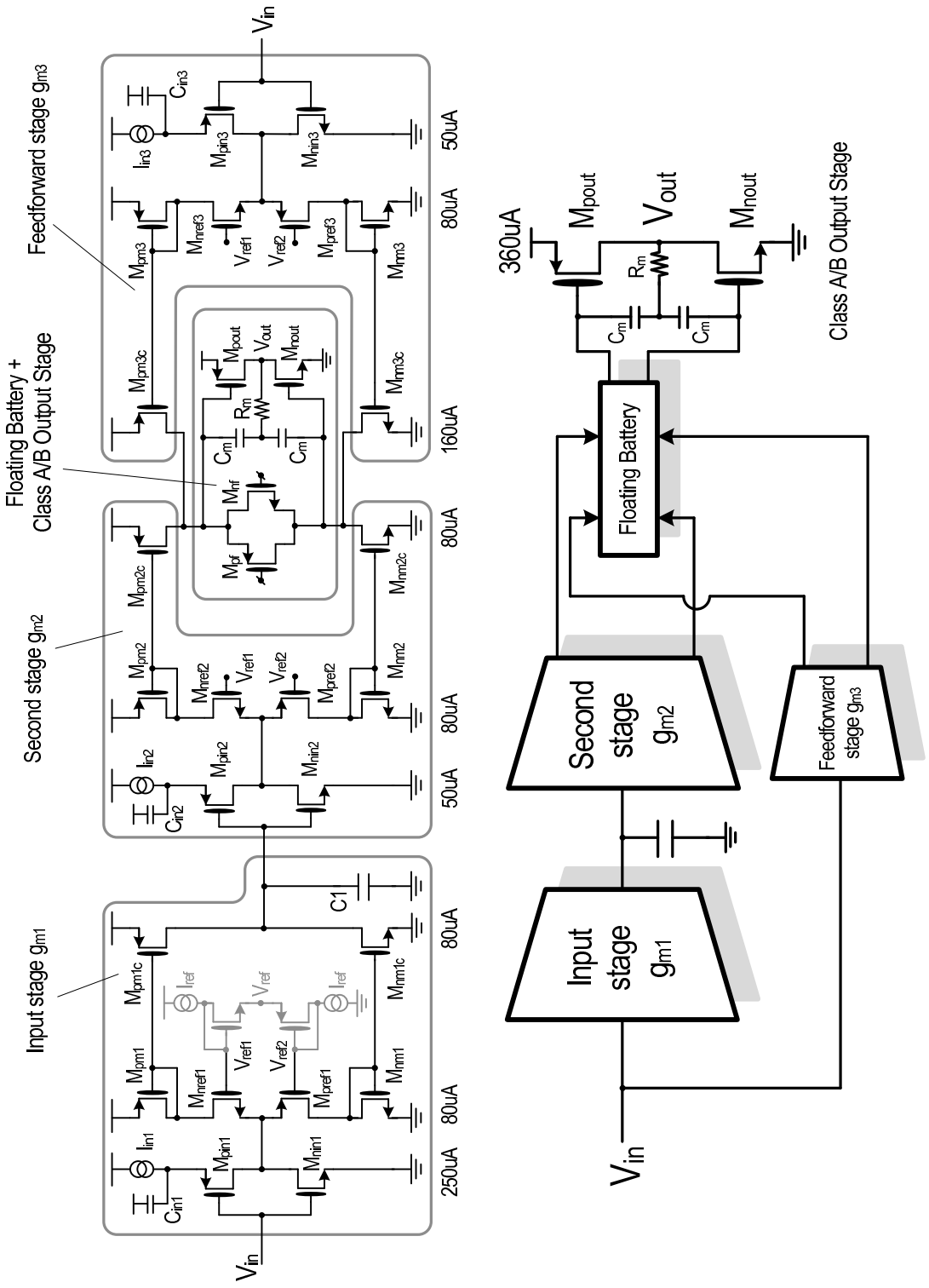

FIGURE 4.11: *Detailed schematic of the proposed input OTA.*

The second stage and the feedforward stage inject their output currents into the floating battery. For a simple design, $gm_1/C_1 = gm_2/C_m$, while the feedforward stage has a double gain-bandwidth product, doubling his current mirror (compared to the second stage) to get $2gm_3/C_m$. The current consumptions are reported in Fig. 4.11: $250\mu A$ at the input transconductors are necessary for noise performances, while the consumption in the current mirrors is necessary for stability, since their many parasitic poles impact phase and gain margins, but it increase the noise coming from the active loads. The other solution to overcome parasitic poles with low currents would have been making small transistors, but this increases mismatch and flicker noise.

With these numbers, we got a phase margin > 60 degrees and a gain margin $> 10dB$ at $530MHz$ and $1.9GHz$, respectively, taking already into account the presence of the RC filter placed at $12MHz$ with a $25pF$ capacitor.

4.3.3 Simulation results

The same simulations of the preceding design have been performed on this new design: basically, we were interested in linearity and out-of-band noise. A Class B 4-tones signal ($7 - 8 - 9 - 10MHz$) current is injected inside the virtual grounds of the two single-ended OTAs: the values are a worst-case situation since we want to simulate a LTE20 signal. The signal is processed with ideal analog filters to precompensate the droop from the two RC poles: the peak value of the injected current would be (without the precompensation) $500\mu A$. The signal is then converted into a voltage swing on the feedback resistor of $1.2k\Omega$ and furthermore filtered with a second real pole with a capacitor of $25pF$: the cut-off frequencies of the two filters, placed at $12MHz$, are very close to the bandwidth signal edge of the real signal ($9MHz$). The voltage signal is afterwards processed with the output loop that drives the active mixer.

More attention has been paid on the stability of this loop, on his noise and on linearity issues. In this second design, the mixer branch DC current consumption at maximum gain has been modified from $3mA$ to $2mA$. In fact, as already pointed out, this current defines the bandwidth of the second loop for low signal swings, meanwhile the noise coming from the elements on this path is less impacting: the current has been then decreased. The large current signal swing (from $2mA$ up to $40mA$) into the cascode transistor M_{csc} modifies the loop bandwidth of

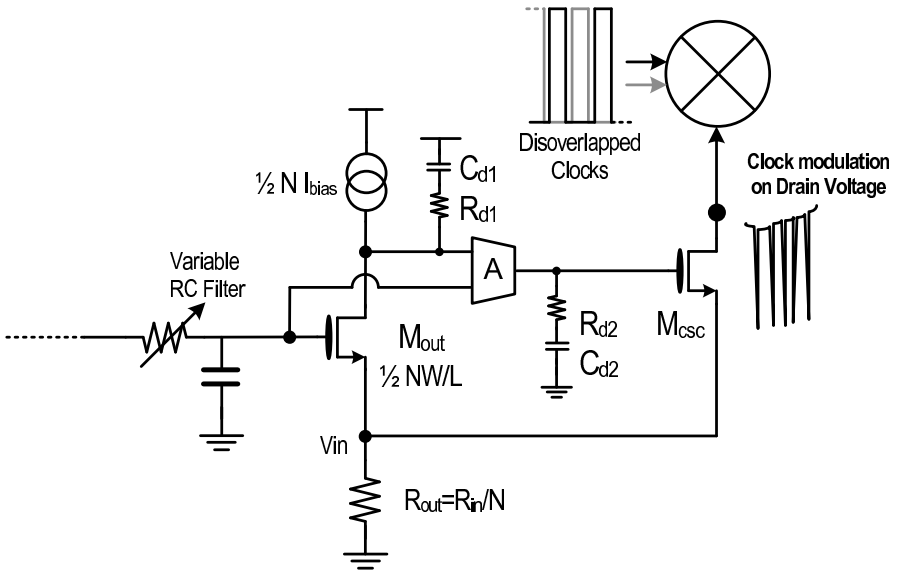

FIGURE 4.12: *Clock modulation of the output transistor drain.*

the second OTA and impact his robustness. Moreover, current consumption is increased for linearity and noise issues: the simple differential stage with active load has been modified into a complementary input stage with the same bias current of the previous design, whereas the load branches have their own current. This leads to a current consumption of $800uA$. Through *stb* and *pstb* simulations from *spectre*, carried out at low and high currents, sufficient stability margins have been implemented: at maximum gain N, phase margin varies from 74 degrees (at $300MHz$) to 64 degrees (at $800MHz$) whereas gain margin is always $> 20dB$.

Another potential problem is given from the variability of the LO clock driving the mixer. In fact, observing Fig. 4.12, when the mixer is driven with disoverlapped clocks, the current injected from the baseband will see for a short time a high impedance in the mixer input, leading to large voltage swings at the M_{csc} drain. These glitches occur at $2f_{LO}$, being f_{LO} the frequency of the local oscillator. The risk is that M_{csc} enters in the triode region every $1/2f_{LO}$ seconds, making the RF section interfere with the low-frequency baseband signal, leading to intermodulations and distortion (i.e. $ACLR$ degradation).

Many solutions could have been implemented. First, the second OTA with a very large bandwidth (up to $2f_{LO}$) could have been designed: hence, the feedback would have reacted to the presence of high-frequency signals inside the loop, counteracting them. However, loop gain bandwidth so large can lead to poor stability and high power consumption. Second, a very narrow gain loop bandwidth can make

the feedback system totally insensitive to high-frequency signals. However, narrow bandwidth means high noise.

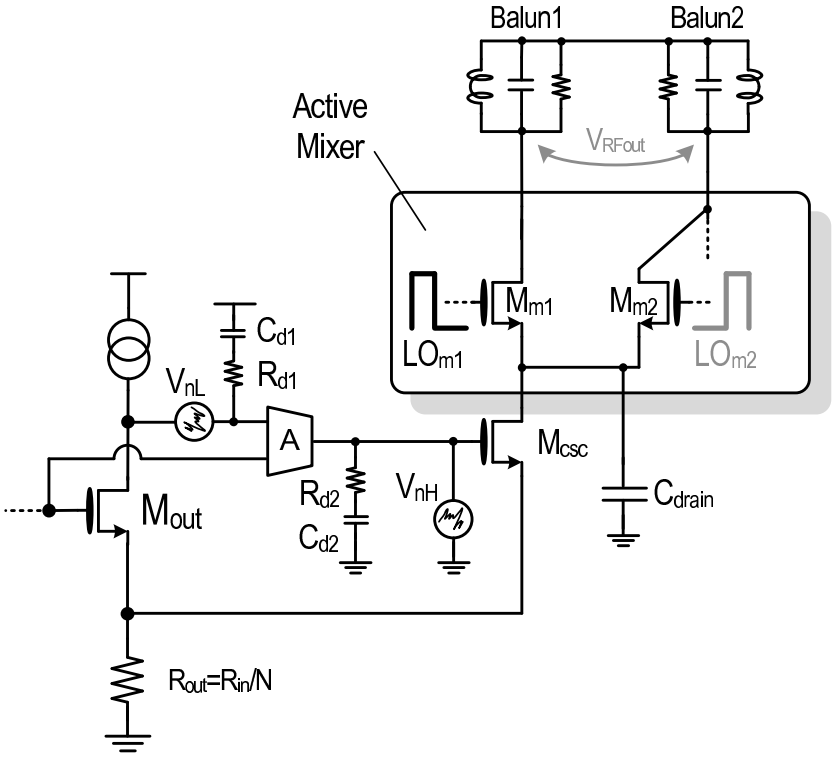

FIGURE 4.13: *Output noise from upconversion and from leakage.*

An easier way to eliminate this high-frequency modulation is to put a capacitor C_{drain} at the M_{csc} drain: this capacitor will be a low impedance for the clock modulation and it will attenuate it. Moreover, this capacitor give also another advantage, filtering the high-frequency noise coming from the output OTA and that is not upconverted. This is explained in Fig. 4.13. The low frequency noise of the OTA can be represented as an equivalent input noise generator V_{nL}, since the gain of the OTA is still high. In this case we can see that this noise can be translated on the resistor R_{out} divided by the transistor intrinsic gain and then transformed into current by the resistor and injected toward the mixer. There, the noise is upconverted to the RF: if we think to the noise current flowing toward $balun_1$, for example, we can see that it is multiplied by a square wave between 0 and 1, at the f_{LO} frequency.

The high-frequency noise of the OTA can be instead represented as an equivalent output voltage generator placed at the M_{csc} gate V_{nH}, since the OTA gain has dropped below unity and an equivalent generator reported at the input is less

straightforward than before. The noise is mainly dominated by the active load of the single stage OTA and by the second doublet, that at high frequency is equivalent to the resistor R_{d1}. M_{csc} acts as a common-source stage, degenerated by R_{out} in parallel with $1/gm_{out}$ [1], and injects the noise current into the mixer. As seen before the noise signal is multiplied by a square wave between 0 and 1: the noise power will be then translated with the harmonics of the square wave and, in particular, the DC harmonic will let it flow toward the output balun. However, thanks to the capacitor C_{drain} added for linearity purposes, this high-frequency noise is filtered, whereas the baseband signal is not disturbed by C_{drain}, being a high impedance at low frequency. In Fig. 4.14 we can see the difference of the drain and source voltage swings on M_{csc} with and without the use of C_{drain}. The voltage swings are the same but the modulations at $2f_{LO}$ are attenuated in the version with the capacitor.

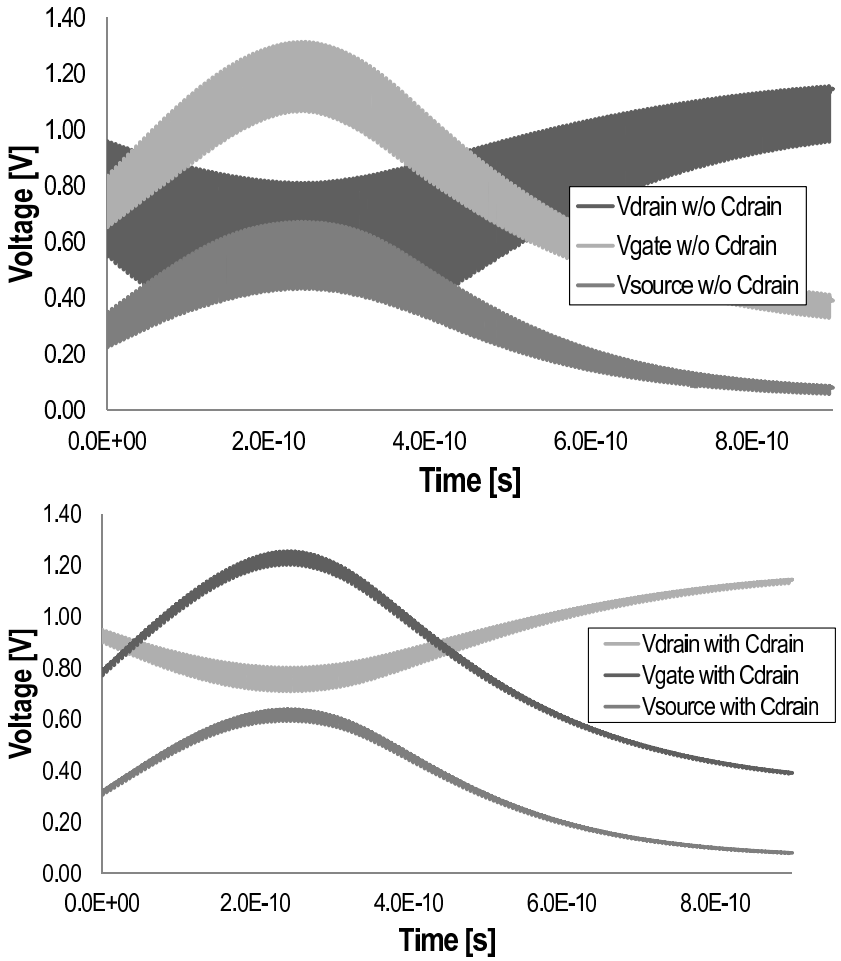

FIGURE 4.14: *Filtering effect of the drain capacitor.*

[1] At high-frequency the doublet $C_{d1}R_{d1}$ has become the low impedance R_{d1} and hence the output impedance of the voltage shifter is lowered from high to $1/gm_{out}$.

Another problem is highlighted in the Fig. 4.14: the output MOS M_{csc} has a small v_{ds} when the signal reaches the peak value. This phenomenon is even worse when the DC voltage gate at the balun selector is lowered (from $1.8V$) to give more space to the swing on the balun: the transistor enters in the linear region deteriorating the $ACLR$.

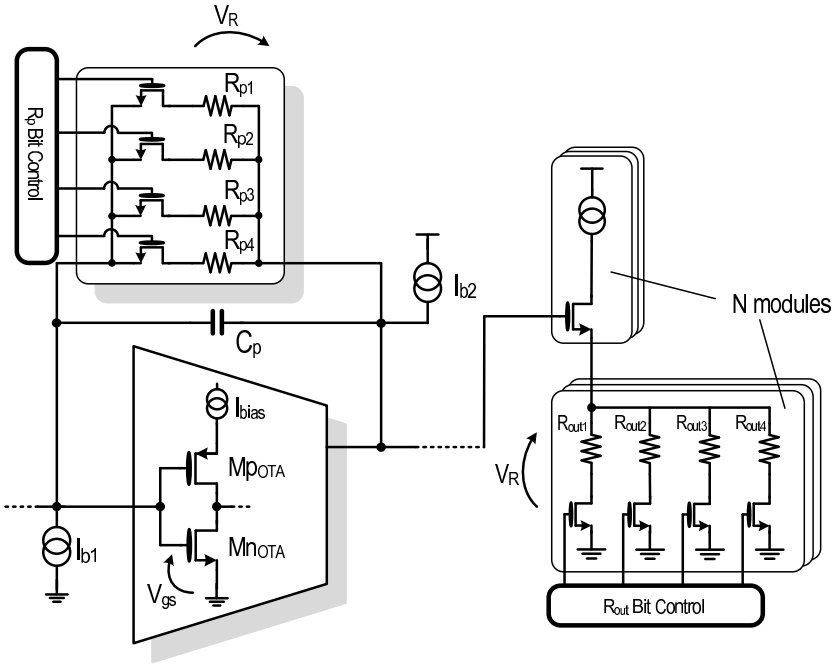

FIGURE 4.15: *Resistor reconfigurability in the transmitter baseband.*

There are several methods to prevent this risk. If we modify and optimize the dimensions of the mixer and the balun selector we can decrease the voltage drop and swings on the stacked devices. For example, the balun selector are High Voltage devices, hence with a minimum L of $200nm$, that limits the maximum achievable transconductance: if it was possible to use Low Voltage devices this could help a little bit. Also the dimensions of the mixer could be increased, but this means a larger capacitance to drive for the LO clock. Another solution, that however introduces a trade-off between noise and linearity, is making the output resistor R_{out} (and hence also R_p from Fig. 4.10) smaller to decrease the voltage swing. In fact, decreasing R_p lowers the voltage swing, that is however converted in current through a lower resistor R_{out}, keeping the same output swing. Anyhow, this degrades the signal-to-noise ratio performances since the signal swing along the system is lowered. In the following simulations, a unity fixed resistor of 250Ω has been decided.

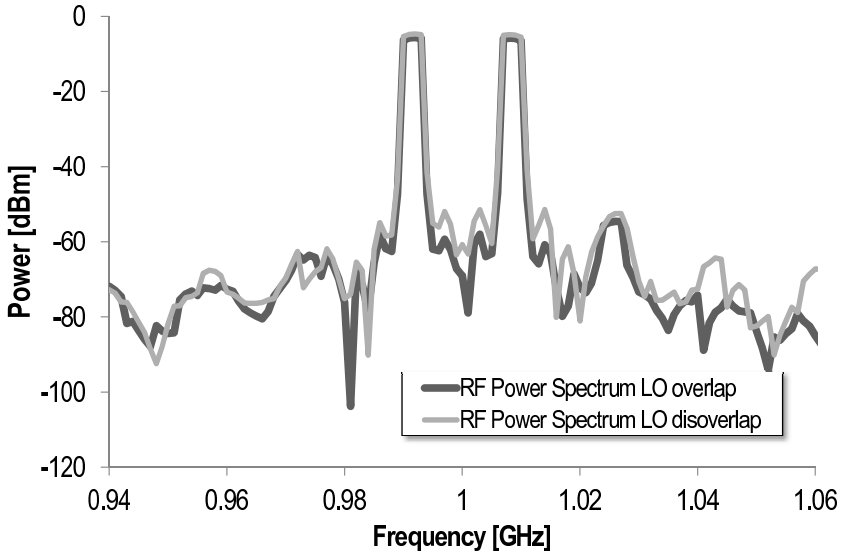

FIGURE 4.16: *RF power spectrum with and without LO disoverlap.*

A more engineering approach would be to insert some programmability in R_{out} together with R_p, maintaining the same structure to preserve matching on the voltage drops. In this way, it will be possible to trade-off linearity with out-of-band noise whenever necessary.

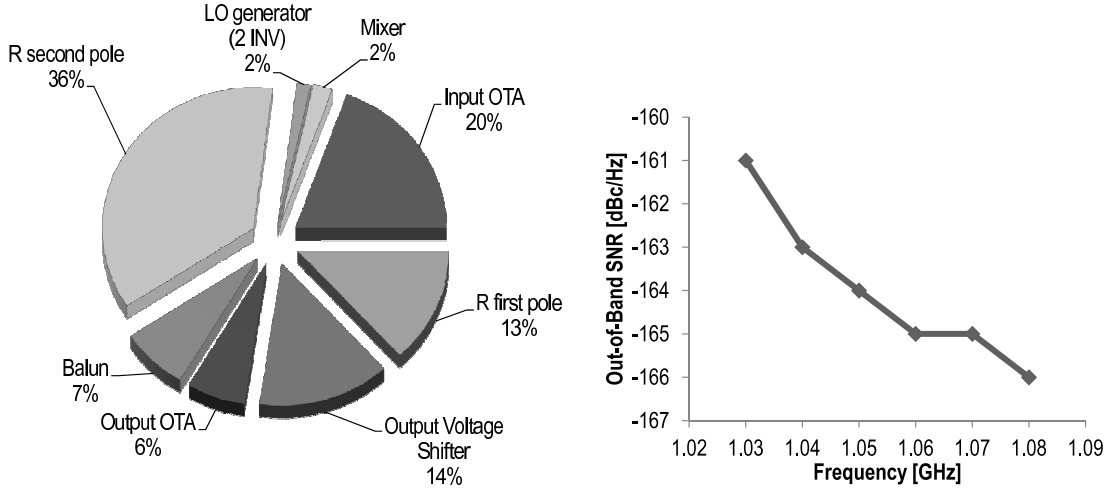

FIGURE 4.17: *RF out-of-band noise contributors and behaviour vs. frequency offset from the carrier.*

In Fig. 4.16 the linearity at the balun is reported with LO clocks overlap and disoverlap, using the capacitor C_{drain}: as we can see the results are quite similar. Before the mixer the linearity is again around $60dB$ meanwhile the mixer limits the value to $\approx 50dB$ in each case.

For what concerns the out-of-band noise, in Fig. 4.17 the contributors percentage at $30MHz$ from the carrier at the balun are reported. The noise is dominated by the input OTA, the filters and the mixer driver, as in the original design. In the same Fig. 4.17 is instead reported the out-of-band SNR versus frequency offset from the carrier: the SNR in dBc/Hz is always below $-161dBc/Hz$ for the most critical Band of LTE, showing very good performances.

4.4 Conclusions

The main idea proposed in this Chapter is to limit the transmitter architecture to the fundamental blocks (i.e. the DAC, a filter, a mixer driver, a mixer and the balun) and exploit the technological advance in the digital domain to perform analog filtering helped with digital compensations: in this way, the power consumption and the out-of-band emission will be very low. In the first part, a proposed design for CMOS $28nm$ is described, together with some simulation results, while in the second part another design for $55nm$ technology is presented.

Conclusions

Toward the effort of limiting power consumption and cost of modern transceivers, keeping anyway high performances, this Thesis describe different types of architecture that are moving in that direction.

The mixed-mode transmitter described in Chapter 2 shows very good performances for what concerns the power consumption, introducing a Class A/B approach in the most power-hungry section of the analog section, i.e. the power mixer.

The Class A/B idea has been implemented also in the transmitter presented in Chapter 3, together with the advantage that the voltage-mode transmitters implement (i.e. placing the whole baseband filtering at the end of the chain, just before the upconversion) but used here into a full current-mode structure. This permits to eliminate, with one building block, all the contributors to the out-of-band emission.

Finally, the idea of Class A/B working is extended to the entire baseband, from the DAC to the upconversion, and the main building blocks of the transmitter are minimized toward the fundamental ones. In Chapter 4, two proposed solutions that implements, respectively, a 1^{st} and a 2^{nd} filtering order are described with simulation results, showing very good performances and high possibility of reconfigurability.

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