Università degli Studi di Pavia

Facoltà di Ingegneria

Dipartimento di Ingegneria Industriale e dell' Informazione

VERY HIGH DYNAMIC RANGE CMOS INTERFACE CIRCUIT FOR GAS SENSOR MATRIX READ-OUT

Tutor:
Chiar.mo Prof. Piero Malcovati

Co-Tutor:
Dott. Ing. Marco Grassi

Coordinatore del Corso di Dottorato:
Chiar.mo Prof. Franco Maloberti

Tesi di Dottorato
di Fabrizio Conso

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Contents

INTRODUCTION

The research activity reported in this thesis has taken place during the period November 2009 - October 2012 at the Sensors and Microsystems laboratory (SMS), University of Pavia. This activity has been carried out in the framework of the Italian Government PRIN project IT-20085AJSEB, entitled "Interface and control circuits for high-selectivity gas sensors operated with temperature pattern". Three research groups have been involved in the realization of this project under the coordination of the Department of Innovation Engineering of University of Lecce, which directed the activity. The Research Center IMM-CNR of Lecce is developing the microsensor, the Department of Electronics of University of Rome Tor Vergata studied the algorithms for gas concentrations extraction and the University of Pavia realized the integrated interface circuit for the sensor. The presented manuscript is mainly about the integrated interface circuit, that consists of a temperature control circuit and a wide dynamic range read-out circuit. These circuits are compatible with the blocks designed by the project partners and in particular they match at the input with IMM-CNR sensor specifications and at the output with University of Rome data analysis algorithms. The manuscript is organized as follows:

1. Chapter 1 is an overview about the aim of the research activity. Gas sensors applications, technological trends and working principles are presented and the motivations that push in developing semiconductor gas sensor are explained. State of the art fabrication techniques and

materials used are then reported. At the end the actual sensor exploited in the project for the chemical measurements is presented, showing its main specifications.

2. In Chapter 2 the developed integrated circuit (IC) is presented. It consists of a low cost resistance-to-time converter with 2 floating inputs, capable of reading a resistence which is not referred to ground. Problems with nowadays interface circuits already developed are analyzed and a valid solution is proposed, which enhances state of art circuits in terms of dynamic range, power efficiency and area consumption (thus cost). Design details will be added in each section and simulation results will be provided at the end of the chapter.

3. In Chapter 3 is the design of an Low-DropOut (LDO) circuit. It has been designed to handle the biasing of the interface circuit, but can be treated as a separate circuit. In fact the specifications for its design have been picked up so that the resulting chip will be considered as much "general porpouse" as possible. The bangap circuit features a 2^{nd} order temperature compensation and its compensated output voltage is buffered by an amplifier to provide a low resistance voltage reference. Particular care is put in the power consumption of the device too. Again, design details will be added in each section and simulation results will be provided at the end of the chapter.

4. Chapter 4 contains two main sections which report the experimental results of each one of the two integrated circuits developed. The instrumental setup used to measure the various performances is described and the measured results are compared with state of art devices that are already existing.

A brief conclusion recalls the outline of the manuscript and the advantage of the proposed solution on the basis of electrical measurements results.

Chapter 1

GAS SENSING MICROSYSTEMS

In this chapter the state of art gas-sensor microsystems are introduced and charaterized in terms of overall technical specifications, basic building block functions and fields of application. Substantial weight is thus given to the fact that the global performance may actually be obtained by careful development of every single sub-circuit, thus requiring cooperation between differently experienced scientists and designers. An overwiev on gas-sensors along with the aim of this activity is then presented, with a brief overview of the sensor exploited in this project and of the whole system.

1.1 Trend in Gas Sensing Microsystems

Gas sensors are widely used for several applications, ranging from environmental and air-quality monitoring to automotive and industrial control. Recently, especially in view of legislative initiatives aimed to the reduction of pollution and of human exposure to dangerous gasses, hand-held systems for gas sensing are becoming quite important, thus pushing in the direction of improving the performance (especially in terms of dynamic range for exploiting novel gas recognition algorithms), minimizing size, power consumption

and cost of such systems [5] [3] [27] [8].

Actually, a gas-sensing microsystem consists of three main parts that are subject to continuous development from researchers: an array of gas sensors, an electronic read-out circuit and a pattern recognition data processor, while the improvements in the overall gas-sensing microsystem are, as mentioned, obtained by improving the single parts and/or their coordination.

Micromembrane resistive gas sensors [7] [15] have been developed in the last decade and proved to be the most promising sensing devices for portable applications, since their thermal time constant is small enough to reach the operating temperature by means of a low-power integrated heater, and to operate the device at different temperatures in time and in space [13] [6]. Furthermore, exploiting portability, wireless protocols like Bluetooth or Zigbee may be used for sensors intercommunication.

On the other hand, the research is also concentrated on developing read-out electronic circuits in integrated (IC) form, which are mandatory for realizing portable gas sensing systems. Their compactness is extremely interesting since it is possible include in the same IC both the conditioning of the signal coming from the sensor and the signal digitalization. In this way the read-out electronic circuit can be directly connected to the block implementing the pattern recognition digital processing algorithms for the final detection of the target gasses. These digital blocks [29] [10] are the objective also of important research activity. For instance, recently developed dynamic pattern recognition techniques extract important information also from the derivative of the sensor response [28]. Therefore, they require an electronic interface circuit sufficiently fast to preserve the transient data, i.e. that provides at least some accurate samples of the resistance value of every element of the array per second. These digital blocks can be realized on the same chip of the sensor read-out circuitry or in a different device, such as a microcontroller or a FPGA, for guaranteeing a better versatility.

1.2 State of Art and Applications in Gas-Sensing Solutions

In the last years, the research activity on gas monitoring systems and in particular on the so called "electronic noses" received a strong push because of the huge number of applications of these devices in several fields, ranging from environmental monitoring to domotic and industrial process control. A very important field of application of this activity involves the attention to the ambient, which is growing more and more in view of its effects in the life of human beings. Indeed, the atmospheric pollution leads to an alteration of the natural equilibria, which not only produces damages to the health of humans, animals and vegetables, but has also significant effects on the climate. This pollution, due to gaseous compounds and particles, derives mainly from domestic heating systems, thermoelectric power plants, waste burning, road traffic and industries. Carbon monoxide (CO), nitrogen oxides (NOX), ozone (O_3), as well as sulphur oxides (SOX), for example, represent the most significant part of the polluting agents of the atmosphere and, in addition, they are among the most dangerous for the human health. The resulting and necessary actions aimed to the protection of the ambient require on one hand a careful monitoring of the air quality, both for outdoor and indoor environment, and on the other hand the introduction of rules and laws always more stringent, which regulate and limit the emission of pollutant compounds. Both these activities require an intensive research and development in order to improve the gas monitoring and emitting systems, which should be supported by governments in terms of legislative provisions and of course research stimulation. This is confirmed by the introduction of the "ambient care"[1] among the key actions starting from the "European Community 6th Framework Program"and in particular among the key action of the "Information Society"work program.

The activity reported in this work falls into this scenario and, in particular, is focused on the air quality monitoring, which, as already mentioned, is one of the most important tasks to prevent pollution. The effectiveness of this monitoring task has to be guaranteed with continuity, especially in the urban areas, trying to detect the eventual presence of pollutants. High priority is therefore given to the possibility of performing a reliable monitoring by means of user friendly portable instrumentation.

The present methods for gas monitoring are still essentially based on spectroscopic techniques, such as chromatography and mass spectroscopy, ultraviolet absorption, chemi-luminescence and atomic absorption, which, besides being very expensive, are also very bulky and require highly qualified personnel both for the initial calibration and for normal operation. A drawback of these systems, indeed, is that, for achieving acceptable performance, they require a heavy initial calibration phase as well as periodic adjustments. Nowadays air-monitoring network, hence, consists of expensive and sophisticated fixed control stations, where measurements of different specific pollutants are carried out continuously. Actually, the air quality control is only one aspect of the environmental pollution analysis, which more generally includes the analysis of a complex system as the atmospheric ambient.

Besides the air-monitoring network, other measurement techniques, not necessarily continuous, as passive samplers, vegetable bio-indicators and remote-monitoring can be used. These techniques allow the information provided by the air-monitoring network to be supplemented from the point of view of both environmental chemistry and physics.

Also very important for studying the atmospheric pollution is the combination of the measurements with the forecast models, which can be used to interpret the experimental data. It is indeed essential to understand that the evaluation of air quality requires a combined system of measurements and theoretical models. This integrated approach should provide an effective

support to the management of governments interventions and reclamation tasks. To this end it would be interesting to operate with small, reliable, low-cost, reproducible and versatile gas monitoring systems. As of today, such a device does not exist but in experimental stage, and hence the reported project activity aims to deal with the most critical issues related to its design. Furthermore, the high density of fixed monitoring stations, required to ensure a suitable air quality control as well as the high purchase and maintenance costs for the analytical instrumentation of these monitoring stations are a real problem in the management of the air-monitoring network. In the context of this approach based on the combination and complementarity among different techniques, the semiconducting gas sensors could play a fundamental role in terms of innovative potential, reduced costs and possible applications. The intensive scientific research aimed to the development of reliable semiconducting gas sensors is due to their numerous advantages.

Besides the reduced size and the low production cost, the semiconducting gas sensors show high sensitivity in the detection of a wide range of chemical compounds in very low concentrations in air, like parts per million (ppm). Moreover, these gas sensors are really easy to operate. However, in spite of the above mentioned advantages, a common feature of almost all the gas sensors is the low selectivity, i.e. the sensitivity to different gasses at the same time. To overcome this problem and use these devices in actual applications, it is necessary to combine the output of several different sensors in sensor arrays to achieve with pattern recognition techniques the selectivity that the single stand-alone sensor cannot provide. Therefore, the implementation of an ambient monitoring system requires a complex array of sensing elements, an electronic interface for signal conditioning and a complex phase of digital signal processing of the obtained data. All of these components need to be developed with the goal of achieving a versatile system.

Some solutions for the considered problem have been proposed in liter-

ature, but they are almost all characterized by large dimensions and they are all tailored for a particular target [27] [8]. Few exceptions exist [19] [18] but still they lack the flexibility needed by novel gas sensors. Therefore, the available solutions cannot guarantee optimal performance when the characteristics of the sensor change as typically happens for example because of ageing, temperature variation or hysteresis effect. In this context, a key element for implementing a robust instrument is a smart signal processing system, capable of adapting its performance to the instantaneous characteristics of the sensor to which it is connected, thus making the system not only insensitive to the effects of ageing, temperature drift or hysteresis, but also versatile, that means capable of working with different sensors, feature which is mandatory for simultaneous multiple gasses detection. For achieving these results an intensive research activity both at the architecture level and at the building block level has been required.

1.3 Semiconductor Gas-Sensors

Solid state gas sensors, based on a variety of principles and materials, are the best candidates for the development of commercial gas sensors for a wide range of applications. This comes from their numerous advantages, like small size, high sensitivity in detecting very low concentrations (at level of ppm) of a wide range of gaseous chemical compounds, possibility of on-line operation and, due to possible large scale production, low cost. On the other hand solid-state chemical sensors have already been widely used, but they also suffer from limited measurement accuracy and problems of long-term stability. However, recent advances in nanotechnology, i.e. in the cluster of technologies related to the synthesis of materials with new properties by means of the controlled manipulation of their microstructure on a nanometer scale, produce novel classes of nanostructured materials with enhanced gas sensing properties providing in such a way the opportunity to dramatically

increase the performance of these solid-state gas sensors.

Furthermore, a particular characteristic of solid state gas sensors is the reversible interaction of the gas with the surface of a solid-state material. Semiconductor Gas Sensors (SGS), known also as chemoresistive gas sensors, are typically based on metal oxides, like SnO_2, TiO_2, In_2O_3, WO_3 and NiO. The interactions between the gas and the semiconductor surface on which is based the gas sensing mechanism of SGS occur at the grain boundaries of the polycrystalline oxide film. They generally include reduction or oxidation processes of the semiconductor, adsorption of the chemical species directly on the semiconductor or adsorption by reaction with surface states associated with previously adsorbed ambient oxygen. The response may be also determined by the transfer of delocalized conduction band electrons to localized surface states and vice versa, by catalytic effects and in general by complex surface chemical reactions between the different adsorbed chemical species. The effect of these surface phenomena is a commonly reversible and leads to a significant change in electrical resistance, i.e. a resistance increase or decrease under exposure to oxidizing or reducing gases, respectively, referring as example to an n-type semiconductor oxide. Thus, the resistance variation can be easily observed and used to detect chemical species in the ambient.

An important type of semiconductors gas sensors is based only on changes in surface conductivity at lower temperatures ($< 600°C$) and at quasi-constant oxygen partial pressure. In this condition the sensor detects small concentrations of reactive gases in air by a displacement from the constant oxygen pressure equilibrium state, induced by gas interfering effects at the surface of the sensor. The working temperature, for these devices, varies depending on the specific target gas in the ambient and on the selected sensor material in conjunction with its properties in every different case. As this working temperature ranges usually from 200 to 400°C, it is necessary to implement

a heating element inside the sensor device which of course needs a control circuitry [23].

A simple SGS (see Figure 1.1) is thus basically composed of a substrate in alumina or silicon on which the sensing layer is deposited, the electrodes used to measure the resistance variation of the sensing film and the heater, commonly a Platinum integrated resistor of some hundreds Ohms, which may also accomplish the function of thermometer, actually knowing the Pt thermal resistive coefficient. This heater is obviously employed to reach the optimum sensing temperature for gas detection. More details about gas sensors operating principles, manufactury, application examples and analytes recognition techniques can be found in [16].

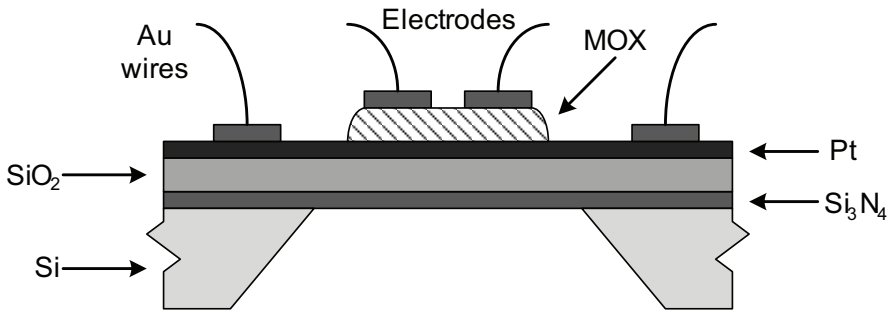

Figure 1.1: SGS example.

The working principle of the semiconducting gas-sensors is based on reversible surface interaction processes between the reactive gas molecules and a polycrystalline metal oxide film, that actually is a combination of adsorption and charge transfer processes. These occurrences, thermally activated, cause a change of the electrical resistance of the sensitive element. These gas sensors are realized with very advanced specific technologies; the sensing layer can be deposited as thin film on suitable small-sized, like 2mm x 2mm alumina or silicon substrates. Recently, specific substrates for sensors based on micromachined silicon have been developed [7], which allow a reduction of power consumption, the miniaturization of the device and the integration in a

single package of the sensors and the interface electronics (sensing integrated device).

Each sensor is typically equipped with electrical contacts and a platinum resistive heater, which may also be realized with a standard photolithographic process. The main disadvantages of these sensors are the long-term instability and the influence of water vapour. Moreover, the selectivity and the accuracy of the measurement performed by the semiconducting gas sensor are limited. However, specific functional strategies allow us to improve the selectivity and make the sensors acceptable for applications in domestic, semi-industrial and environmental applications. In fact, the selectivity can be modulated by a suitable choice of sensing film, catalysts and dopants, geometry, nature of the electrodes and filters. Different configurations of electrical contacts can be used to study the response of the sensors to variations in the gas composition in the ambient. For a given contact geometry the electrical characterization of the sensor can be carried out in different operation modes, like in DC, applying a constant voltage or a constant current, or by AC response evaluation.

The scientific research in the field of gas sensors follows two complementary directions: the implementation of high selectivity sensors and the development of new types of applications based on arrays of non-selective sensors.

Finally, a new type of sensor, which this work deals with, exploits the use of different non-selective sensors arranged in a matrix form, thus requiring an innovative front-end and signal processing circuitry to operate correctly. The sensors matrix object of this work is composed by (see figure1.2):

- 25 interconnected sensors arranged in 5x5 matrix accessible at the beginning and end of each row and column.
- 5 series connected heaters in each row.

- 5 series connected thermometers in each row.

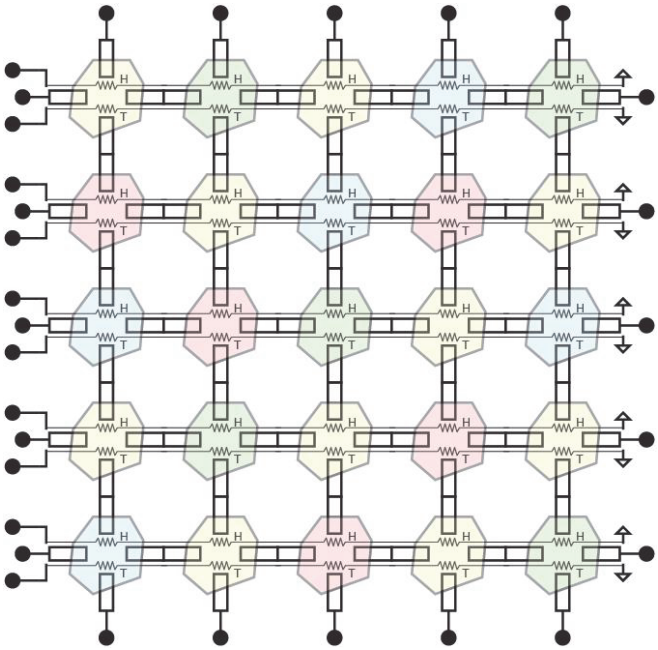

Figure 1.2: 5x5 S_nO_2 sensors matrix

Differently from sensor arrays, in which each sensor can be measured separately and referred to ground potential, each couple of the 20 terminals of the matrix has to be measured floating and is the result of many series-parallel connected sensors.

1.4 Electronic Interface

In view of the large spread of the electrical characteristics of gas sensors, it is evident that the interface and signal processing circuitry becomes very important in order to achieve a robust system. Although some IC approach in gas monitoring systems has already been developed, in many others the most significant design effort has always been devoted to the development of the sensors, while "off the shelf "discrete components mounted on printed circuits boards have always been used, even in the most recent implementations, for

the interface circuit and mostly also for signal processing electronics. The resulting circuits have to be trimmed every time to match the characteristics of the sensor, have large power consumption and dimensions, thus being unsuitable for portable applications. The implementation of the interface circuits in integrated form could overcome this problems, leading to a highly innovative gas monitoring system.

The gas sensors which have been used in this project are semiconductor devices, which from the electrical point of view, as will be justified in Chapter 2, behave as resistors, whose resistance changes with the gas concentration. The resistance value in the absence of gas, the so-called baseline, can vary in the same sensor during time as much as two-to-three orders of magnitude, while among nominally equal sensors this variation can become three-to-four orders of magnitude. Obviously, this introduces big challenges in the design of an interface circuit capable of working over the whole resulting resistance range, without requiring any calibration phase performed by the operator, as in the case of the systems reported in literature. In the interface circuits implemented with discrete components this problem can be solved by replacing or trimming some components depending on the characteristics of the sensor.

An interface circuit which achieves this goal whith enough dynamic range is described in [24] but, unfortunately cannot handle the readout of a sensors matrix such as the one mentioned above. The designed circuit is an improvement of that work to suit it for the novel sensor. It also enhances it's dynamic range, power efficiency and area consumption.

Concerning the control of sensors parameters, considerable attention has been paid to temperature control and actuation. Temperature is a key parameter for semiconducting gas sensors mostly because the interactions between analytes and sensitive materials are always governed by processes characterized by defined activation energies and hence they are extremely sensitive to

temperature. For this reason, the temperature control sub-system can play an important role in determining the sensors characteristics such as sensitivity and selectivity, which are of great importance for sensor arrays. From this point of view, many documents, appeared recently in literature, pointed out how in metal-oxide semiconductor resistive sensors, such as Tin-Oxide (S_nO_2) it is possible to virtually increase the number of sensors of an array by changing from time to time the sensor temperature and the catalytic metal [22]. Thus, the temperature is not only a parameter to be controlled in order to ensure a stable behavior of the sensor, but also a parameter to be actuated in order to modify the sensor performance thus increasing the information provided by the sensor array. For instance, the application of well defined temperature profiles, like ramps or thermal cycles, recently allowed spectral techniques exploiting both Fourier and wavelet transforms. This new approach for studying the sensor signal opens new perspectives on the kind of information which can be extracted from chemical sensors.

1.5 Signal Processing

Data analysis of sensor array is presently a well consolidated field, where a collection of algorithms, derived from chemometric techniques, like principal component analysis or partial least squares and neural networks, like self-organising maps or radial-basis functions, allow us to extract qualitative and quantitative information from sensor arrays [11] [21]. These data analysis techniques are generally based on the assumption that from each sensor a numerical figure, representing the sensor response to a single gas or to a complex mixture of gasses, can be extracted. On the other hand, the extraction of this information from the temporal evolution of sensor signal, named feature extraction, is very interesting from the research point of view. In this area, although empirical approaches exist, a robust and complete formulation of the problem has not been developed yet. Another important issue in the field

of data analysis is the possibility to discriminate in the sensor signal those components which are not immediately correlated with the sample under test and hence that could introduce uncorrelated noise. Correction techniques, based on geometric approaches such as the analysis of principal components and the analysis of independent components have been recently proposed as methods to optimize the sensor response. More details on data analysis and in particular on different pattern recognition techniques are reported in [16].

1.6 Objective of reported microsystem design activity

The reported gas-sensing microsystem design activity [2] concerns the development of a miniaturized and, hence, portable ambient gas monitoring circuit, with large dynamic range and able to properly operate the read-out of a sensors matrix in spite of the technological variations in the fabrication of the included gas sensors and of the use of various types of gas sensors. This system will be composed by a certain number of semiconductor sensing devices, arranged in a matrix, by an A/D multiplexed integrated circuit including a dedicated conditioning network for the read-out of the data coming from the sensors and by a system of digital processing of the acquired data. In addition an electronic circuit will also have to supply the five series connected microheaters that will allow the matrix rows to operate at the optimal temperature.

As mentioned, gas monitoring systems are widely used in several applications: in the agricultural and food-field, in the emergency control (for the toxic gas survey), in the control of combustion and in the quality control of the air. The target device will be used mostly for ambient analysis and/or for the generation of chemical images of the ambient: this will be done for ambient used by humans and for hostile environment. Several kinds

of gas sensors and different complete systems have been already developed and largely distributed over the global market, but they are characterized by large dimensions, large power consumption and, in particular, high cost. In fact they are inspired to traditional measurement laboratory instruments technology, which may grant high accuracy and wide-range paying in terms of higher supply voltage, difficult portability and periodic factory calibration need. Finally in these cases the synergy in the sensor-front-end is not always present and this does not allow the optimization of the performances in terms of system resolution for several gasses. Often this last limitation is due to the wide variability of the sensor electrical characteristics, due to effects of ageing and to the various kinds of gasses to be detected. It is thus interesting, from the point of view of the scientific validity and of the industrial interest, the development of a low power miniaturized system, in which the front-end is self-adapting with respect to the output impedance of the sensor to which it is connected (which is variable as a function of the kind and the entity of the adsorption process) and to the preamplifier input impedance. In this way it is possible to obtain the minimal theoretical noise and, as a consequence, the maximum obtainable resolution for any variation of the sensor electrical characteristics and for any change of the sensor. Moreover the resolution and the functionality of the system will be optimized by using appropriate pattern recognition algorithms which process the acquired digital data. The reported system design faces the following aspects among the most critical ones in the development and realization of a complete portable gas sensing system:

- realization of a family of miniaturized semiconductor gas sensors manufactured with sol-gel technique on micromachined substrate having large stability, high linearity, large sensitivity, low noise and, as a consequence, high resolution;

- development of a smart integrated mixed-signal A/D front-end circuit with a large dynamic range, able to reconfigure the read-out section depending on the characteristics of the sensor to which it is connected;
- design of an integrated microheater, able to regulate the sensor temperature;
- development of novel algorithms of pattern recognition for the processing of the acquired data from the front-end.

The research activity has been assigned to three groups, which operated in parallel but in strong coordination, as described in the following. A first group the sensors matrix. This matrix will be composed by different semicondutcor gas sensors to provide high sensitivity to molecules like CO, CH_4, NO_X, and O_3, which are critical in ambient monitoring applications. The activity performed by the second group, on which is mainly focused the manuscript, has been the design of the electronic front-end circuit, which processes the signals coming from the gas sensors. In fact, these devices may be characterized electrically as an impedance whose value depends on the type and the concentration of a given gas. Such block has been realized using a 0.35m CMOS technology, in order to have satisfactory and long life constant performance, at low cost and with reduced dimensions. Such interface circuit may be used with sensors having different electrical characteristics. This is possible since a fundamental peculiarity of this block is the high dynamic range of the resistance values which can be correctly measured. Another task of this second team has been to develop another integrated circuit which controls the heater, providing the necessary power to maintain the sensor at constant temperature, thus granting more stable electrical sensor characteristics. A third team has been assigned to the development of novel pattern recognition algorithms aimed to process the digital data supplied by the A/D interface circuit. To achieve this objective, those algorithms able

to provide both qualitative and quantitative evaluation of analysed samples have been considered. The study of the data analysis has been approached in two distinct phases: the first concerns the definition of those features to be associated to the sensor response and the second the application and the optimization of the data analysis algorithms. The feature extraction, beside the trivial steady-state response, takes into consideration also the time behaviors of the sensor signals.

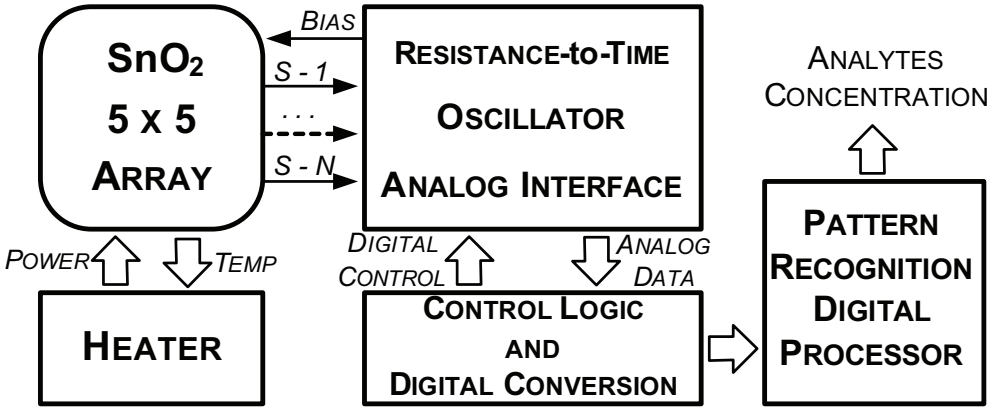

Figure 1.3: Block diagram of the system.

The peculiarity of realizing a miniaturized system can then give the advantage of connecting the developed system as underlined, with a wireless transmission system (Bluetooth, for instance) in order to create a distributed and remotely controllable net of gas sensors of several kinds, each one with optimized performance.

1.7 System Overview

In Figure 1.3 is shown an overview of the whole system described in the previous section. The sensor matrix is composed by 5x5 different sensors directly connected to the analog parts of the interface circuit: the gas sensing circuit which takes care of connecting the two matrix terminals under measurement to the front-end, and the temperature control loops which set the

temperature of each matrix row independently. The gas sensing circuit is also composed by a digital part which performs the conversion of the measured resistance value into the digital domain. The digital data is suitable for the pattern recognition digital processor to be handled to obtain the analytes concentration.

Chapter 2

SENSORS MATRIX INTERFACE CIRCUIT

This chapter is particularly focused on the design of a low-cost, uncalibrated, wide-range resistive gas sensor front-end circuit. The circuit is based on resistance-to-time conversion and the state of the art of this measurement method has been improved first by enhancing its linearity and power efficiency, and then allowing for a complete sensors matrix read-out modifying the sensor biasing. Simulation results in 0.35μm CMOS technology show that the circuit achieves, without calibration, a linearity error in resistance measurement of about 0.8% over 6 decades of resistance variation range.

2.1 Designed IC Overview

The aim of the designed circuit is to operate the conversion of a whole 5x5 gas sensor matrix (380 possible measures, since current flow direction is also important) with a linearity error lower than 1% over an equivalent resistance variation range of 6 decades. In particular, the equivalent resistance measured between each couple of the matrix terminals (hereafter referred as "the sensor") can vary in the extimated range of 1 kΩ - 1 GΩ. This extimated sensor resistance is made of the combination of three independent variables:

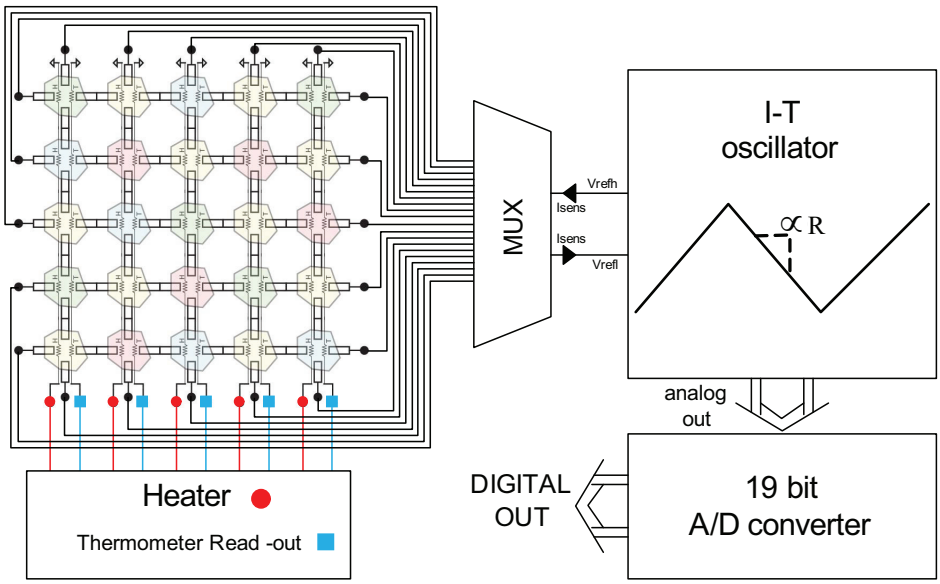

Figure 2.1: Block diagram of the read-out chip connected to the sensors matrix

the baseline resistance R_{BL} which is the typical resistance value, a deviation from this value due to technological process spread and ageing ΔR_{BL} (in the order of one-two decades) and a variation due to the gas concentration ΔR_{GAS} (also in the order of one-two decades). This last contribution is the one of interest and can be extracted by means of a pattern recognition digital processor.

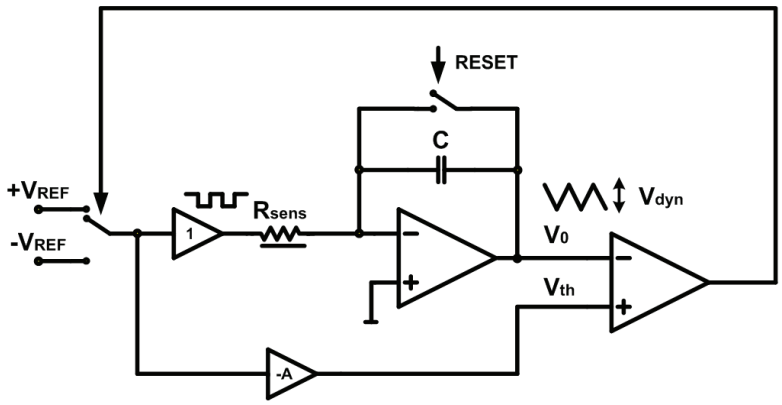

Figure 2.2: traditional resistance-to-time conversion

The proposed circuit (block diagram in Figure 2.1) is composed of an anolog-digital mixed circuit. As already stated, the analog part performs a resistance-to-time conversion [17] [14] [26] which has proved to be the most promising method to achieve a very high dynamic range required by gas sensing applications. This conversion is achieved in a very simple way by the circuit shown in Figure 2.2.

Such circuit however suffers of the major drawback that the sensor itself is included in the feedback loop thus greatly reducing the maximum theoric dynamic range achievable (these sensors are widely non-linear with the biasing voltage, specially also due to their parasitic capacitance biased at a dynamic voltage value). This problem is solved with the circuit showed in Figure 2.3 [16] in which the sensor is biased with a constant voltage and the current produced (V_{ref}/R_{sens}) is sourced/sinked to/from the virtual ground of an integrator. The result is a triangular waveform, which is squared by a flip-flop, with a period equal to:

$$T = \frac{2 \cdot C \cdot (V_H - V_L)}{V_{ref}} \cdot R_{sens} \tag{2.1}$$

Even this circuit, however, is not suited for the proposed system being

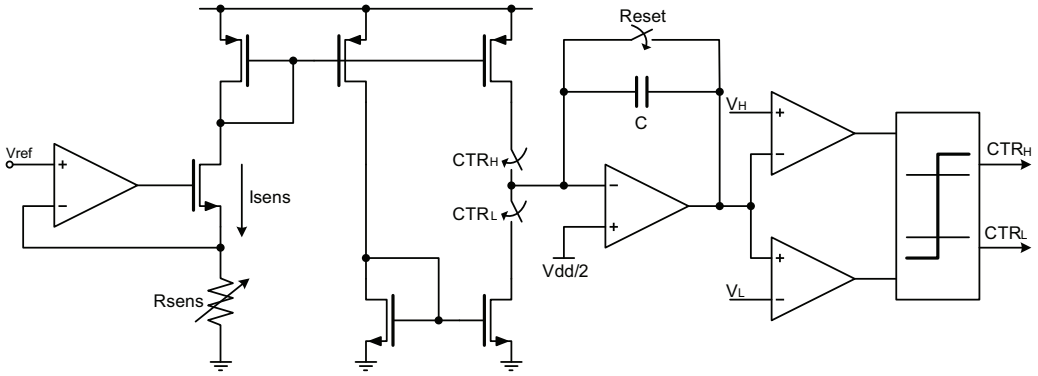

Figure 2.3: enhanced resistance-to-time conversion

capable of reading resistances only referred to ground.

The subsequent digital part of the circuit, on the other hand, performs a

fully digital anolg-to-digital conversion and affects the behavior of the whole chip as will be seen in Section 2.2.3.

To operate the sensors at the correct temperature another mixed signal circuit has been implemented in the same chip, which performs the temperature control loop. In particular, the temperature of each row is set independently so this circuit contains in fact five different temperature control loops (see Section 2.3).

2.2 Sensors Resistance Read-Out Circuit

The analog part of the designed read-out circuit is showed in Figure 2.4. It is composed mainly by a biasing branch, a mirroring branch, an integrator and a couple of comparators. The description of each block along with the

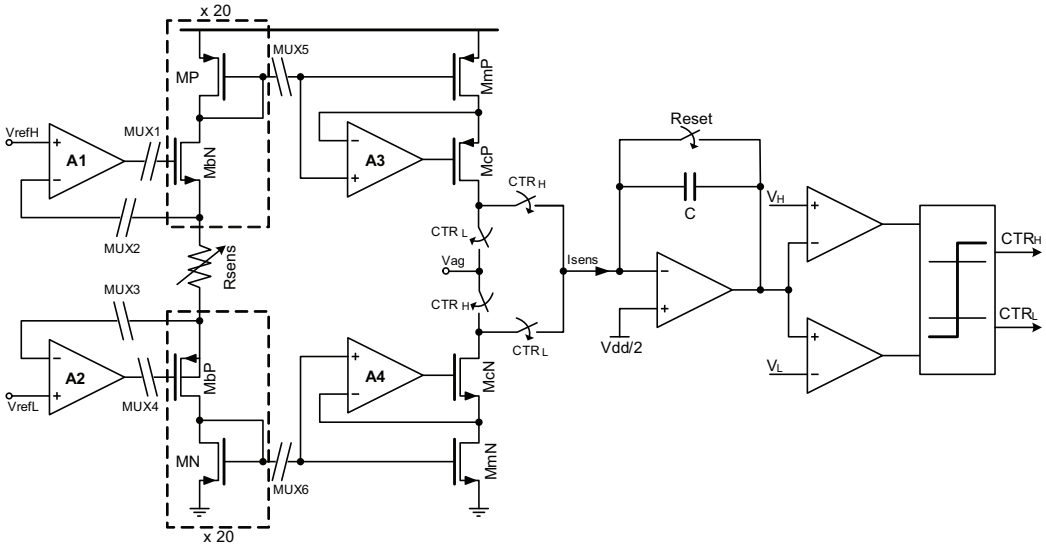

Figure 2.4: resistance read-out circuit

design details is found in the following sections.

2.2.1 Biasing of the Sensor

The biasing stage has been designed to perform a floating measure of the resistance seen between each couple of the sensors matrix terminals. Since any mux switch in series with the sensor would greatly decrease the overall dynamic range (big switches would have bigger leakage current compared to a GΩ sensor while small switches would have an on resistance comparable to a kΩ sensor) the biasing branch has been modified as shown in Figure 2.5 where each of the 20 matrix terminals are connected to 1 of 20 identical biasing branches. This way all the multiplexers that select the two terminals

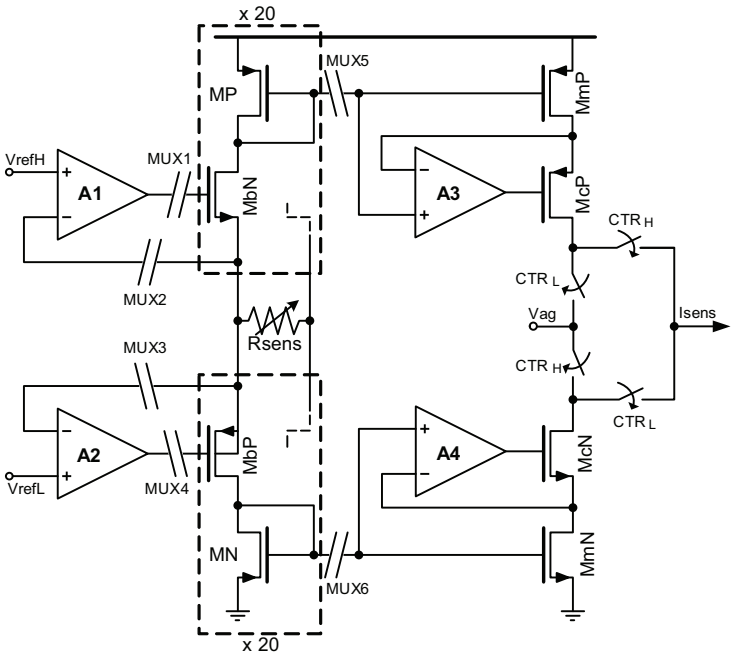

Figure 2.5: sensor biasing stage

under measurement can be moved outside the signal path on high impedence nodes, thus avoiding all the multiplexers non-linearities. The design of the bias branches has taken particular care because of the high number of stacked transistors. The transistors dimensioning for this particular CMOS 0.35μm technology is shown in Table 2.1.

BIAS BRANCH DIMENSIONING		
Transistor	L(μm)	W (μm)
M_P, M_{mP}	0.5	150
M_N, M_{mN}	0.5	50
M_{bN}, M_{bP}	0.35	1000
M_{cP}	0.8	80
M_{cN}	0.8	20

Table 2.1: transistors dimensioning for the biasing branch.

Amplifiers A1 and A2 bring bias voltages to the two terminals of the matrix under measurement with high impedence and are connected to the correct upper and lower halves of the bias branch through multiplexers 1-4.

The two bias voltages $V_{refH} = 1.65\,V$ and $V_{refL} = 1.15\,V$ are not symmetrical to $V_{DD}/2$ due to the greater threshold voltage of the transistor MbN whose bulk cannot be connected to its own source in the employed technology (there is no triple well option), otherwise there would not have been enough room for transistor MP to operate correctly. In Figure 2.6 is reported the

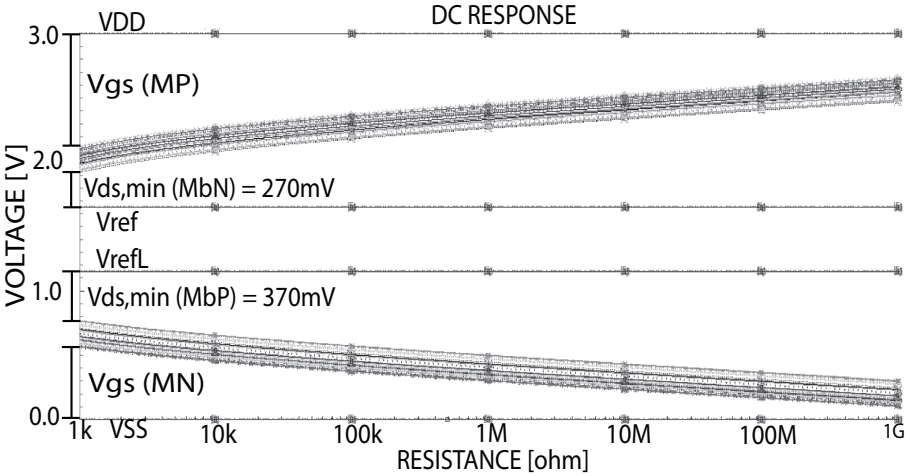

Figure 2.6: Montecarlo simulation for the bias branch

montecarlo simulation of the bias branch at the minimum extimated operating temperature of -10 °C (highest thresholds) and minimum power supply

voltage of 3 V. Under these conditions the two current conveyor transistors MbN and MbP have a minimum drain-to-source voltage V_{DS} voltage sufficient to keep them in the saturation region even with the minimum sensor resistance (maximum V_{GS} for current mirrors MP and MN). Likewise transistors MbN and MbP have been designed with an high aspect ratio $\frac{W}{L}$ to mantain their gate-to-source voltage V_{GS} low, at the maximum current and lower temperature, so that the output stage of amplifiers A1 and A2 does not saturate (Figure 2.7).

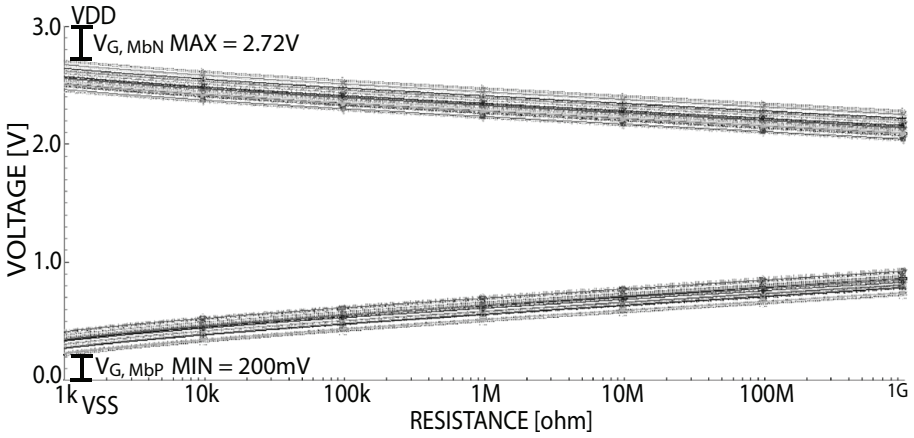

Figure 2.7: Montecarlo simulation for the bias branch

The resulting current in the bias branch $\frac{V_H - V_L}{R_{sens}}$ is then mirrored by transistors MmP and MmN to obtain two identical currents of opposite polarities in the upper and lower halves of the mirror branch. These currents are injected/absorbed to the following stage by means of the two opposite phases CTR_L and CTR_H.

Amplifiers A3 and A4 are used to keep the V_{DS} of the mirroring transistors equal to the diode reference one. This helps to greatly increase the output resistance of the current mirrors, as required by a very high dynamic range specification, without suffering of the high voltage drops of other current mirrors tipologies (cascode or high compliance for example). In Table 2.2 is a summary of the current consumption of the various block in this

input stage.

BIAS BRANCH CURRENT CONSUMPTION	
Block	Consumption (μA)
Amplifiers A1-A2	7
Amplifiers A3-A4	7
Bias branch	0.0005 - 500
Mirror branch	0.0005 - 500

Table 2.2: input stage current consumption details.

2.2.2 Resistance Proportional Oscillator Period

The current produced biasing the sensor with a costant voltage drop is sourced/sinked to/from the virtual ground of an oscillator by means of a couple of current mirrors. If, with the given initial condion, the current is being sourced into the virtual ground (see Figure 2.8) a ramp is produced at the output of the amplifier, until saturation occurs if nothing else intervenes. To bind the voltage swing at the output of the amplifier to an acceptable

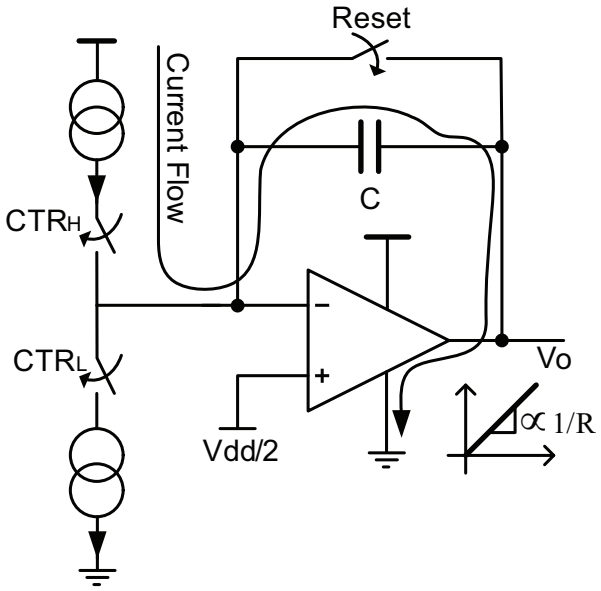

Figure 2.8: current flow for a current inkected into the virtual ground.

range, two high speed comparators are used as shown in Figure 2.4. As soon as the ramp crosses one of the two binding voltages V_H and V_L the control phase CTR changes and the slope of the ramp is inverted. As a result a triangular waveform is obtained at the output of the integrator with an amplitude $\Delta V = V_H - V_L = 1\,V$ and a period proportional to the sensor resistance, given by:

$$T = \frac{2 \cdot C \cdot (\Delta V)}{V_{refH} - V_{refL}} \cdot R_{sens} \tag{2.2}$$

The triangular wave is then squared by a latch to be used by the following digital blocks and to operate correctly the current inverting switches. The latch has also the function of forcing the comparators to switch alternately. This principle is also called: *half-infinite hysteresys* [12] [4].

With an integrating capacitor of 100 pF a square wave with a frequency in the range [2.5 Hz - 2.5 MHz], depending on the sensor resistance, is obtained. This value has been chosen as a good compromise between conversion speed and power consumption in the amplifier and comparators.

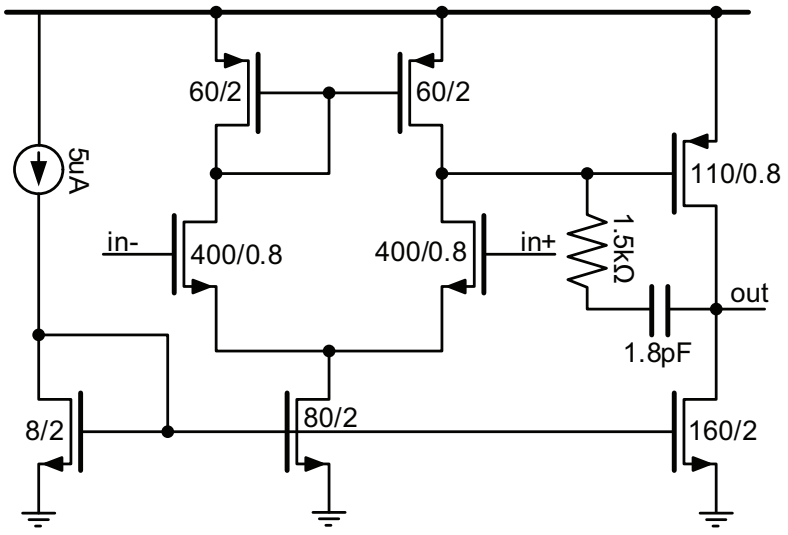

Figure 2.9: two stages amplifier schematic.

The architecture used for the integrator amplifier is a two stage with a class A output stage (Figure 2.9). The transistor dimensioning is reported

in the figure. This amplifier achieves a gain-badwith of 120 MHz and a DC gain of 85 dB while consuming 150 μA. This consumption may seem strange considering that the class A output stage should be biased with a current greater than the maximum sensor current I_{sens}. This will be explained in Section 2.2.4.

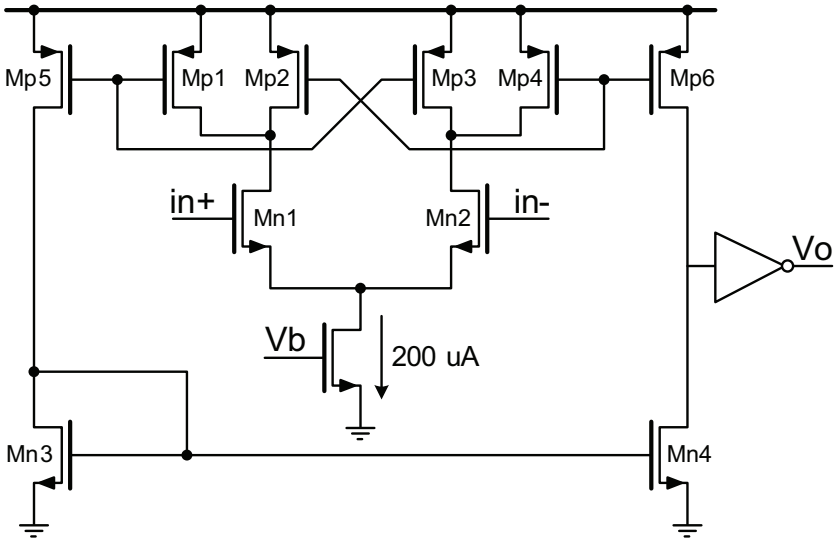

Figure 2.10: two stages amplifier schematic.

The two comparators are two high speed continuous time comparators, whose topology is inspired to the ones employed in nuclear application devices [12] [4], followed by a latch that regenerates the comparators outputs. This Set-Reset (SR) latch has also the function of forcing the comparators to switch alternately (half-infinite hysteresys principle as mentioned above). Complete comparators switching time is, for triangular integrator output signal frequency above 100 kHz, only 2 ns, including latch regeneration. For lower integrator output signal frequencies, the switching time is longer, accordingly with more relaxed timing requirements. The comparator embeds a positive feedback loop made up of Mp1, Mp2, Mp3 and Mp4, as shown in Figure 2.10, in order to rise unbalancing speed, while the output signal is extracted by means of suitable current mirrors and squared by a digital inverter.

By dimensioning MP1-MP4 is also possible to set up single comparator finite hysteresis threshold voltage, which has been fixed to $V_{th} \simeq 100\,mV$ in this design. Each comparator has also been dimensioned to exhibit asymmetrical speed response respect to input signal. This means that the circuit response has been optimized for being much faster when the negative input crosses the positive input level, respect than vice-versa, according to half infinite hysteresis advantage. In fact, considering this principle, the complementary switching condition (actually the one in which the comparator has already been unbalanced and must be released) will have no effect on the oscillator system, being the regenerating SR latch listening to the other comparator output at that time. This asymmetry may be obtained, as operated, by designing MN4 with a pull-down capability larger that the pull-up factor of MP6, leading to an unbalancing-to-release time ratio of about a decade. Each comparator is characterized by an average current consumption of $300\,\mu A$.

The linearity of the whole interface, at simulation level, has been tested with the polyfit Matlab function. The result is showed in Figure 2.11. If the added non-linearity of the measure speed-up functionality (see Section 2.2.4) is considered, the result is a linearity error of about 0.8% as stated in the chapter introduction.

2.2.3 Frequency Measurement Logic Circuit

The frequency measurement logic developed (see Appendix A.1 for the Verilog © code) is the first of the implemented digital blocks to be described. The block diagram of the main digital circuitry is shown in Figure 2.12.

The frequency measurement is made up by a couple of counters (fine counter in the figure): the clock of the first one is generated by the oscillator discriminator circuit and thus has a period proportional to the value of the R_{sens} under measurement, while the cadence of the second counter is driven by an external reference clock whose frequency is set at the midrange of the

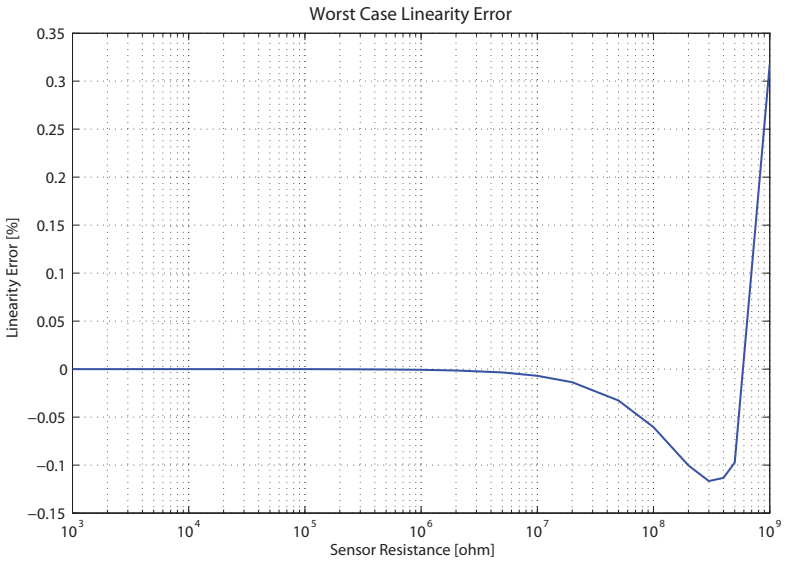

Figure 2.11: interface linearity tested with Matlab.

given oscillator frequency interval (2.5 Hz - 2.5 MHz):

$$f_{ext} = \sqrt{f_{min} \cdot f_{max}} = 2.5\,kHz \tag{2.3}$$

Therefore, the measured resistance value is given by:

$$R_{meas} = \alpha \cdot R_{mid} \cdot \frac{N_{ref}}{N_{osc}} + \beta \tag{2.4}$$

where N_{ref} and N_{osc} indicate the reference and the oscillator frequency dependent counter values at the end of the conversion respectively, R_{mid} the logarithmical center of the scale, while α and β represent instead the front-end circuit gain and offset contribution terms. These coefficients may be left uncompensated in gas sensing because they do not affect linearity in gas concentration extraction. The measurement ends when the slower of the two counters reaches a given value N* which is sufficient to achieve the desired accuracy, i.e. N*=256 for a minimum guaranteed 8-bit equivalent precision. This 8-bit precision is required to keep the linearity error well under 1%, so that the quantization error can be neglected.

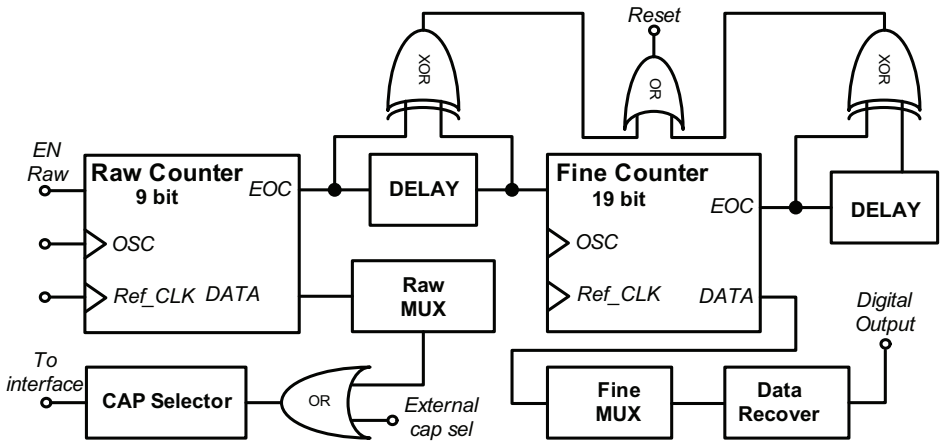

Figure 2.12: frequency measurement and interface control logic circuitry.

If the applied R_{sens} value is lower than midrange, the slower of the two counters reaching N* is going to be the reference one and the measurement time is constant. By contrast, the slower counter is going to be the one controlled by the oscillator if the measured R_{sens} is greater than midrange, leading to a measurement time proportional to the resistance value itself. As a consequence, the measurement time required for the acquisition of a single sample for one of the 380 total possible measures ranges from 102.4 seconds for $R_{sens} = 1\,G\Omega$ to 102.4 milliseconds for $R_{sens} < 1\,M\Omega$ as shown in Figure 2.13. Such an high measurement time is not acceptable for practical applications, considering also the high number of measures required for a total matrix conversion. This problem is partially solved in the following Section 2.2.4.

If a measurement of resistance values in the range of at least ± 3 decades centered around R_{mid} is needed, over a single read-out scale, the minimum number of bits needed for each of the two counter registers is given by:

$$N_{BIT} > \log_2 N^* \cdot \frac{R_{max}}{R_{min}} = \log_2(256) \cdot 10^3 > 18 \tag{2.5}$$

Therefore, the output digital word will be composed by 19 bits, which represent the value reached by the faster of the two counters during the mea-

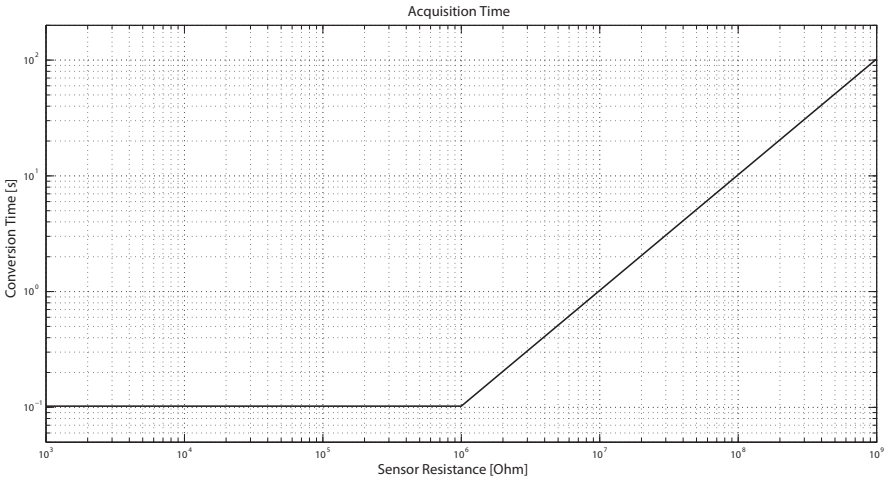

Figure 2.13: acquisition time as a function of the sensor resistance.

surement and by an additional bit which indicates if the converted resistance value is either higher or lower than R_{mid}. This task is performed by the finemux of Figure 2.12, that decides which of the two counters is the correct output word and sets the additional bit accordingly. Figure 2.14 represent the ideal output code as a function of R_{sens}. Since it is not an univocal function, the necessity of the additional bit is explained, so that the correct information ca be reconstructed by the data-recover block of Figure 2.12.

2.2.4 Improved Conversion Speed Logic Circuit

Another logic circuit has been designed to generate the signals for the control of the interface behavior. These mainly consist in the reset and power-down signals and a functionality to increase the conversion speed to solve the problem mentioned above.

The simplest way to increse the acquisition time of the interface is to decrease the capacitance in the integrator loop. If 1 pF is chosen instead of 100 pF, the conversion time is decreased by a factor 100 too. This cannot, however, be done roughly because of the increase in the bandwidth of the sensor signal by a factor 100 too, requiring a lot more power consumption

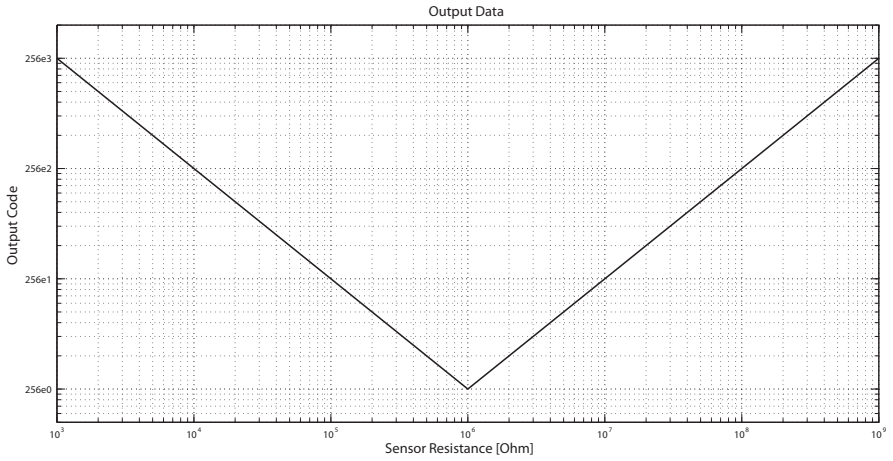

Figure 2.14: output code as a function of the sensor resistance.

in the integrator and comparators and dynamic power consumption in the latch.

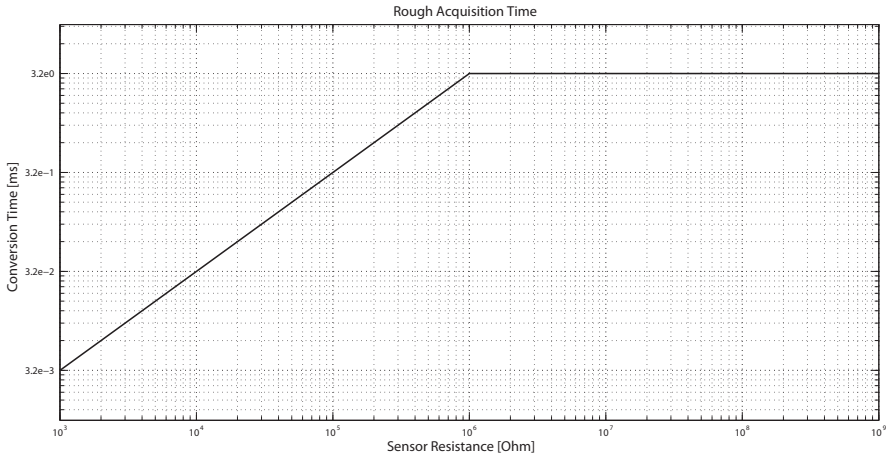

Figure 2.15: rough conversion time as a function of the sensor resistance.

To solve this problem another couple of counters can be used. These counters perform, when enabled, a rough conversion before the fine 19-bit one, to sense the sensor resistance range. In particular, they are two 3-bit registers and work as follows:

- if the rough conversion is enabled (externally) the rough counters start

to count as soon as the acknowledge signal raises;

- the first one to saturate (111, or 7 count) raises a flag and a mux decides which one was the first to saturate;
- if the external clock counter saturates first (i.e. when the sensor resistance is greater than 1 MΩ) a x100 signal is passed to the interface to lower the integrator capacitance;
- the conversion time for high sensor resistances can thus be lowered by a factor 100 at a small expence of increasing all the conversion times by a maximum of 7-8 cycles of the external clock (3.2 ms) as shown in Figure 2.15.

This solution, however, brings along the problem highlighted by Figure 2.16. When the biasing stage feeds (or drains) the maximum current to the integrator the amplifier output is easily saturated. Even if the structure of Figure 2.16 is used with a single switch on the lower current branch (current is inversely proportional to the capacitance value), a huge nonlinearity is introduced. To avoid this problem a different solution has been adopted, which is showed in Figure 2.17. The current mirrored from the bias branch is controlled by the x100 signal. If the signal is low only a x0.1 mirror factor will be used, in the other case a x10 mirroring factor will be used. To bring back the signal to the 2.5 kHz center bandwidth the integrator capacitance has been lowered to 10 pF. This solution has four other advantages:

1. the area occupied by the x10 current mirror is lower than the area necessary for 90 pF poly capacitor.
2. transistors matching is better than capacitors one.
3. the maximum current consumption has been greatly reduced both in the bias branch and in the class A output stage of the amplifier (see Table 2.3).

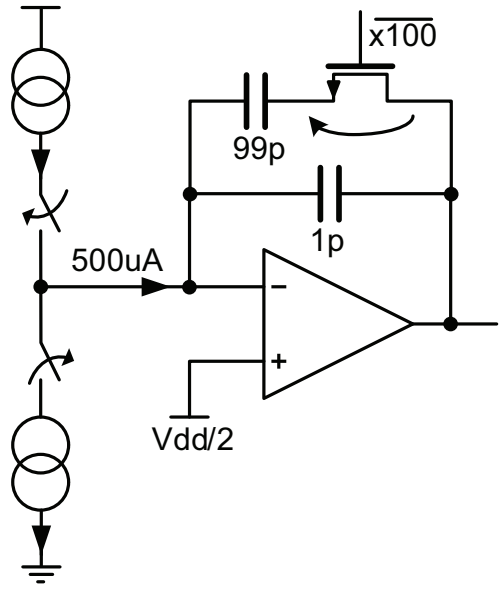

Figure 2.16: particular of the capacitance switch problem.

4. a thinner variation range in the current mirrored from the bias branch brings itself to a better linearity (less parasitics sensibility).

INTERFACE CURRENT CONSUMPTION	
Block	Consumption (μA)
Amplifiers A1-A4	7
Bias branch	0.0005 - 500
Mirror branch	0.005 - 50
Integrator amplifier	150
Comparators	300

Table 2.3: interface current consumption details.

2.2.5 Measure Multiplexer and External Comunication Logic Circuits

An explaination of the external measure acquisition process is mandatory before starting to describe the measure multiplexer logic circuit. The external world interacts with the chip through registers. These mainly consist of:

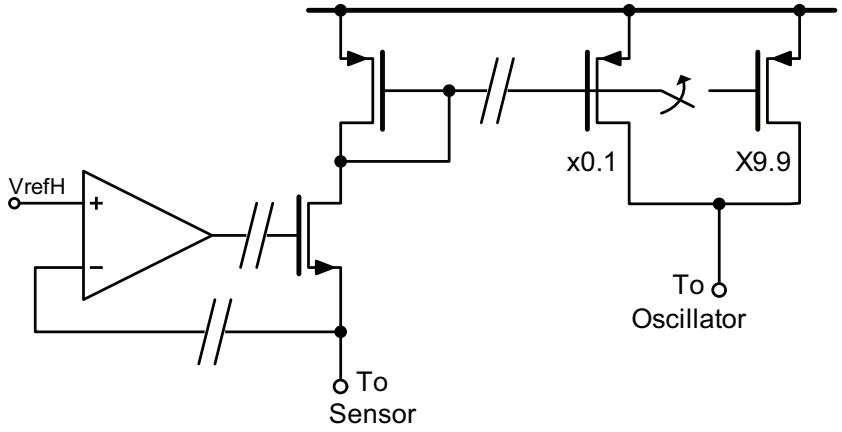

Figure 2.17: implemented speed-up technique.

- a 20-bit output register.
- a 1-bit of acknowledge.
- a 9-bit measure selection register.

The 20-bit output register is read by the external application to acquire the measurement result, the 1-bit acknowledge is written by the external application to make known that the acquisition of the output register has ended and a new measure can start and the 9-bit measure selection register is written by the external application to pass down the next measure that will be performed.

To simplify the reading/writing procedures with the external world an I^2C slave circuit has been implemented on chip. It consists in a series of 8-bit registers, divided into a reading and a writing section. The reading section registers contain all the informations gathered by the interface which are available for the external application to be read while the writing section registers contain all the external control signals and can be written by the external application.

In more detail, the interface input is sensible to the rising edge of the acknowledge signal and the whole procedure works as follows (see also Figure

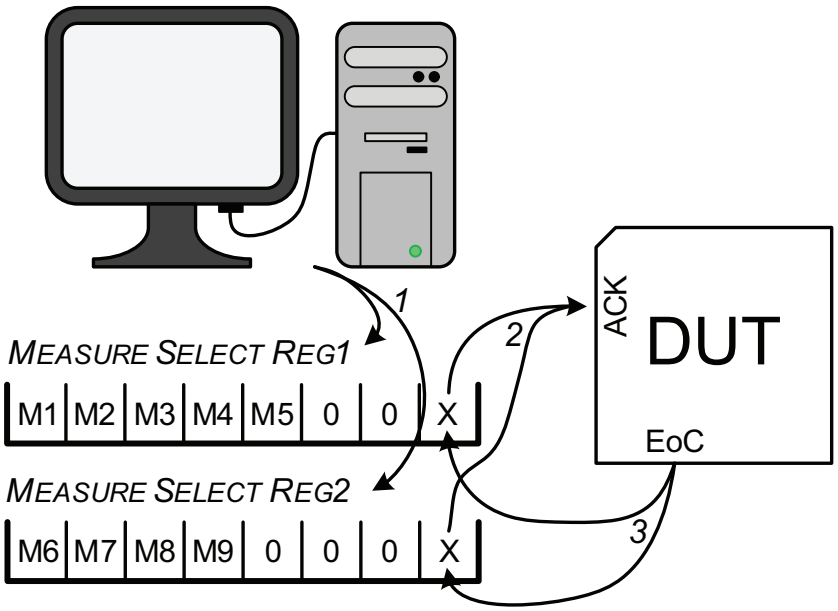

Figure 2.18: schematic of the measurement and data gathering process.

2.18):

1. first the external application writes the measure selection register and sets the last bit (a 10th one) to the digital 1. This last bit is passed as acknowledge signal to the interface;

2. the interface senses the positive edge of the acknoledge signal, retards it by one clock period of the 2.5 kHz reference clock to prevent any retard in the signals path to disrupt the correct functionality;

3. the end of conversion (EoC) signal, which is raised at the end of the conversion process, is used to reset to 0 the same 10th one bit in the measure selection register;

4. the I^2C master checks for this falling edge on the 10th bit and starts the procedure to acquire the output register from the slave circuit. And so on.

For practical reasons related to the I^{2}C slave synthetization, every register has been been split into 8-bit registers. The case of the measure selection register is reported in Figure 2.18, because it is important for the measure mechanism understanding. In this case the last bit of each register (marked with X) is considered as acknowledge signal: to start the measure the I^{2}C master writes them both to 1 and the interface considers the digital AND function of the two bits while the at the end of the acquisition process the EoC signal resets both bits to 0.

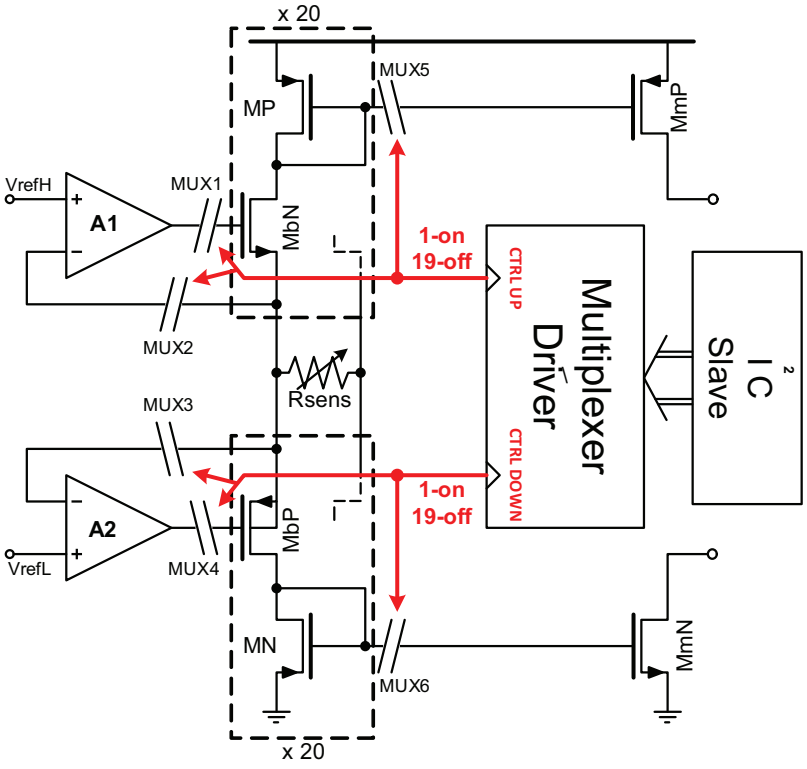

Figure 2.19: multiplexer driver circuit.

The measure multiplexer logic implemented (see Appendix A.1 for the Verilog © code) reads the 9 measure selection bits in the I^{2}C slave and generates the command signals for all the multiplexers in the biasing branch to enable the correct upper and lower halves of the bias branches and put the other 19 upper and lower halves in a power down mode. This way the inter-

face is connected with the two matrix terminals under measurement without the inteference given by all the other terminals which are connected to very high impedence paths so that their contribution is negligible. The procedure is summarized in the Figure 2.19. The measure multiplexer logic circuit has also been designed to avoid enabling both the upper and lower halves connected to the same terminal of the matrix or a short circuit between the virtual short circuits of the bias branch amplifiers would occur.

Finally, a simulation for a sequence of acquisitions is presented in Figure 2.20. It can be seen that a small rough conversion is operated before the fine one. The upper waveform refers to the reset signal generated by the frequency measurement logic circuit. This is done to leave the proper time to the interface to set-up correctly after each conversion cycle. In the figure two consecutive acquisition are showed, the first one converting a sensor resistance of 100 kΩ and the second one converting a sensor resistance of 1 GΩ. The things to note are:

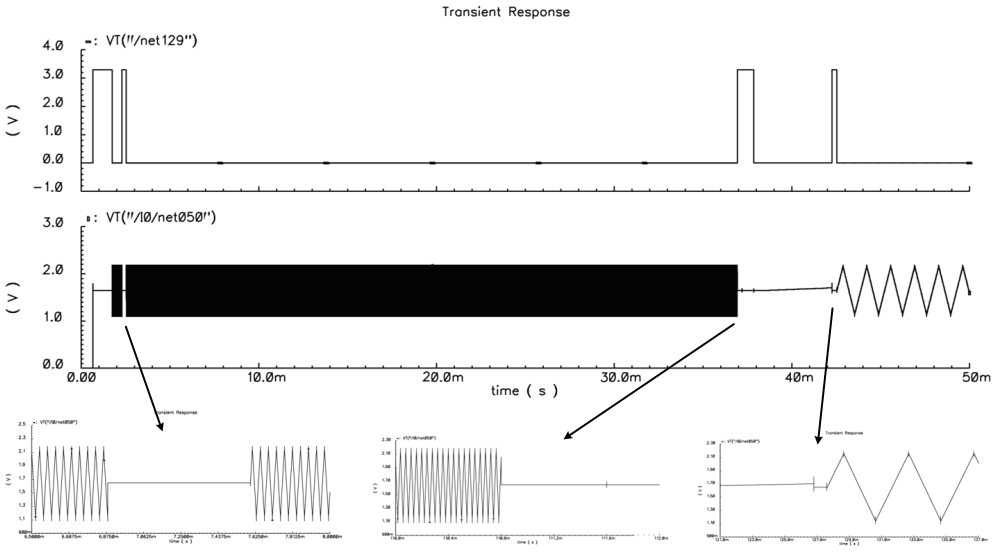

Figure 2.20: simulation for sequence of acquisitions.

- the first rough conversion time is much smaller than the second one

according to what said in Section 2.2.4 and showed in Figure 2.15;

- at the end of the first rough conversion the frequency of the resistance dependant oscillator is unchanged, being the sensor resistance lower than the midrange (1 MΩ), as also said in Section 2.15;
- at the end of the second rough conversion the oscillator frequency is increased by a factor 100, being 1 GΩ greater than the midrange;
- the two wider reset pulses at the beginning of a new conversion leave time to the interface to set-up before the actual acknowledge is raised. The two smaller reset pulses at the end of the rough conversion phases are enough for the mirroring factor change to occur.

2.3 Temperature Control Circuit

The temperature control circuit is in fact five identical temperature control circuits, based on the one described in [23], each controlling the temperature of a line of the sensors matrix independently. These circuits consists in five separate analog circuits and a digital circuit which has been designed to have some blocks in common for all the loops to minimize the area occupation and dynamic power consumption. The single line temperature control will be described, emphasizing the parts in common for all the five circuits.

The control implemented is shown in Figure 2.21. It consists in a mixed signal analog/digital circuit. The temperature is set/measured by means of the heater/thermometer platinum resistance embedded in each sensor. A conditioning network converts the thermometer resistance (or better the five series connected thermometers in each row) first into a voltage and then in a digital number which is compared in the digital domain with the setpoint turning on/off a nMOS to feed power to the heater resistances.

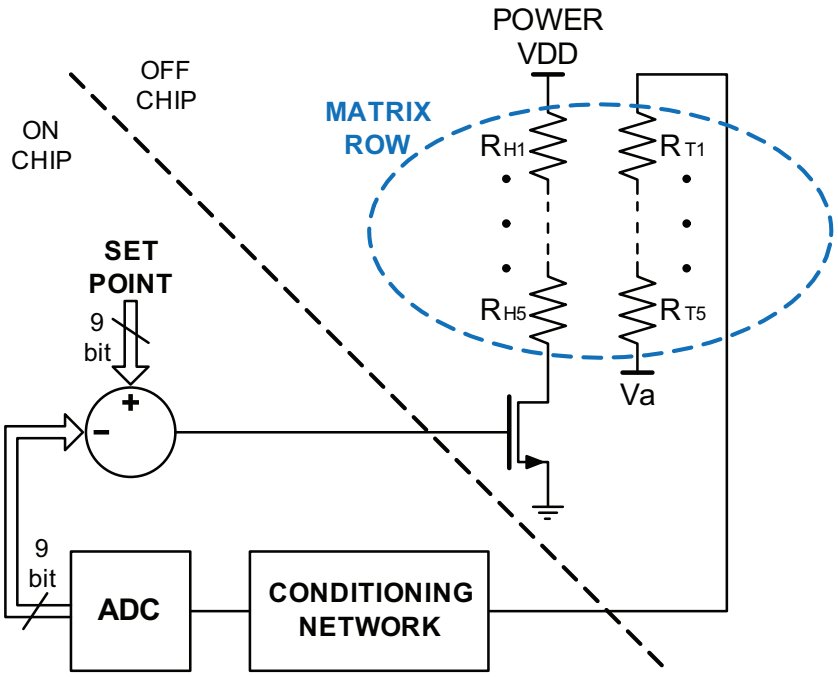

Figure 2.21: block diagram of the temperature control loop.

2.3.1 Conditioning Network

The conditioning network designed is the continuous time circuit shown in Figure 2.22. Since the new sensor is still uder development, only the expected thermometer resistance is known and can even vary with the fabrication process. Thus the biasing stage has been designed to have high flexibility so that the signal could be tuned to the input range of the amplifier. In particular:

$$V_+(T) = V_A + I_{DAC} \cdot 5 \cdot R_T(T) \tag{2.6}$$

$$R_T(T) = R_{T0} \cdot (1 + \alpha(T - T0)) \tag{2.7}$$

Any offset and gain deviation from the expected thermometer signal variation range can be canceled adjusting V_A and I_{DAC}. The DAC has been realized by using four cascoded current mirrors that provide 1.6 mA, 0.8 mA, 0.4mA and 0.2 mA, respectively (see [23], pp. 83-86 for the design details).

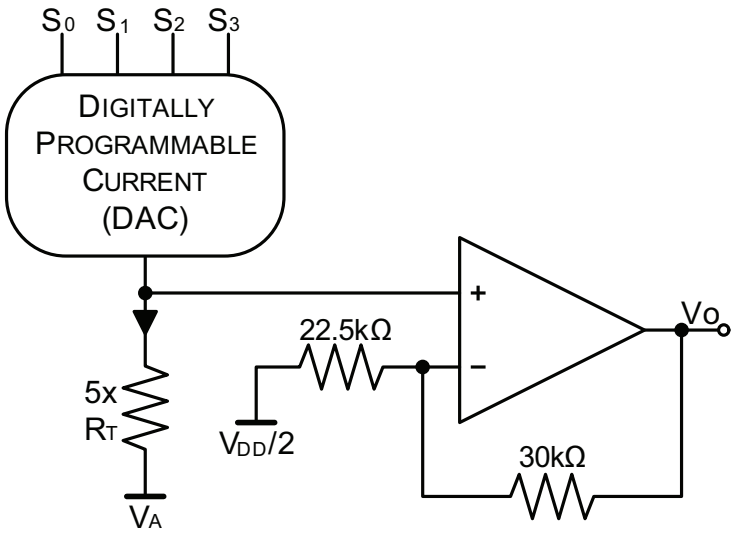

Figure 2.22: block diagram of the temperature control loop.

The expected design parameters for the thermometer are $R_{T0} = 75\,\Omega$ and $\alpha = 0.00216\,C^{-1}$. Thus the extremes of the total thermometer resistance variation range in a matrix row are $5 \cdot R_T = 375\,\Omega$ ($T = 25\,°C$) and $5 \cdot R_T = 750\,\Omega$ ($T = 500\,°C$) . If a DAC current of $800\,\mu A$ and a V_A of $1.2\,V$ are chosen the resulting signal will be centered around $V_{DD}/2$ with an amplitude of 150 mV. The additional gain in the amplifier feedback (A=2.3) brings this signal to the proper voltage levels required by the ADC input dynamic. Moreover it is possible to exploit the current DAC in order to adapt to the input range of the ADC the most common temperature ranges (250-400 °C for example) or to more limited temperature ranges to increase the conversion accuracy.

The implemented amplifier is, again, a two-stage architecture with Miller compensation (Figure 2.23). The current flowing through the second stage ensures a good driving capability and hence it is not necessary to implement a source follower output stage. In fact, the output impedance thanks also to the feedback is low enough. The gain of this amplifier is around 60 dB, the gain bandwidth product is 280 MHz with 1 pF capacitive load, the phase margin

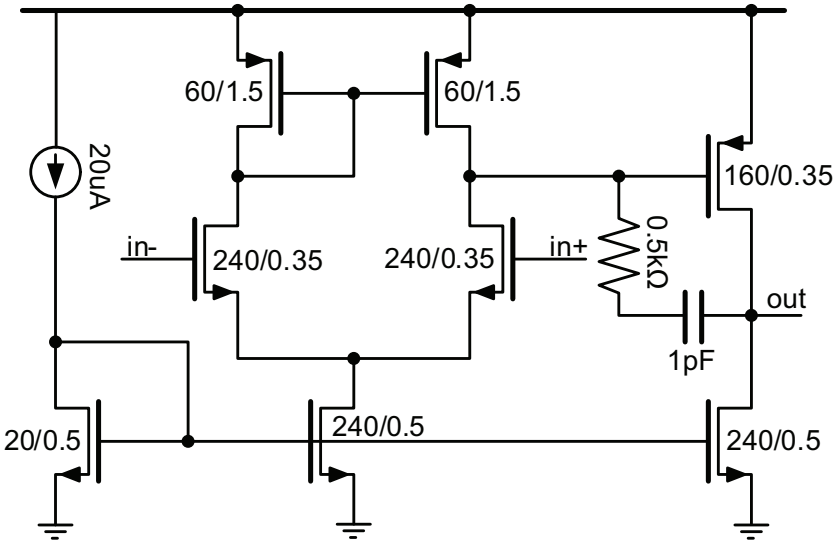

Figure 2.23: amplifier used in the conditioning network.

is 70 ° and the power dissipated is about 3 mW. Such a large bandwidth and driving capability are required to handle the kickback of the input stage of the ADC. In fact, during every clock cycle, the input capacitance of the ADC (2 pF) must be charged with complete settling in 100 ns.

2.3.2 ADC

As will be described in the next section, the temperature control loop chosen is the on/off topology. Because of this choice a key parameter of the ADC is the conversion time. Approximating the trend of the temperature over time with a first order exponential equation, it is possible to obtain the maximum allowed conversion time in order to keep the temperature ringing lower than 1.5 °C. How much the instantaneous temperature deviates from the desired value depends on the time interval between two successive updates of the output of the ADC. In Figure 2.24, the points when the A/D converter updates the output are underlined by vertical chopped lines. It is possible to note that, for example, when the temperature crosses the upper limit of the selected temperature, the system keeps furnishing heat till the successive

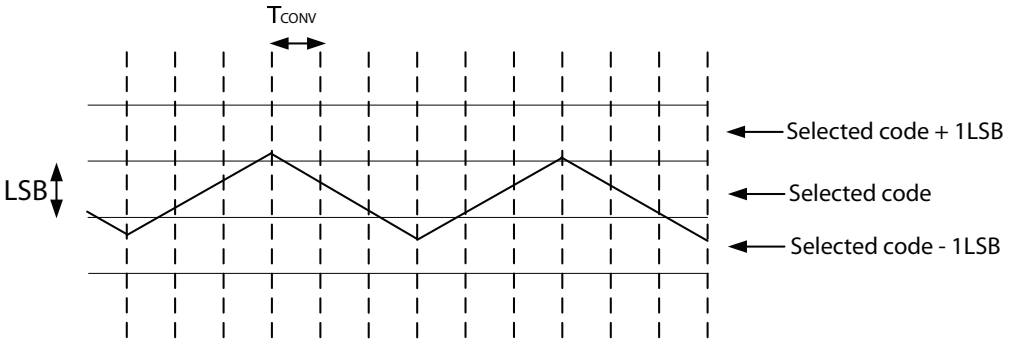

Figure 2.24: temperature ringing for an ADC with a finite conversion rate.

update of the ADC output, increasing the amount of the temperature ringing.

If a typical configuration in which the LSB corresponds to 1 °C is considered, the unavoidable minimum ringing is therefore 1 °C and since the system needs to show an overall ringing smaller than 1.5 °C, the conversion time T_{CONV} is forced by design to be as small as necessary to limit the temperature to move less than 0.5 °C between two ADC output updates (see again [23], pp75-76 for more details).

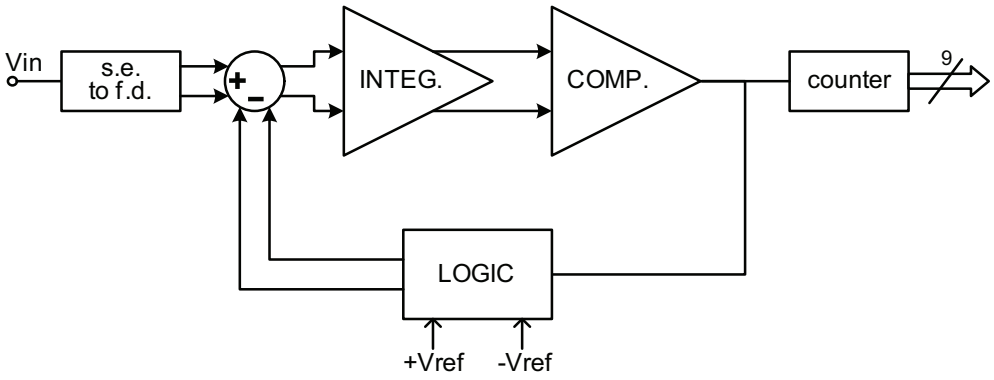

Figure 2.25: block diagram of the employed sigma-delta ADC.

The ADC structure is showed in Figure 2.25. It is a first order sigma-delta modulator, in which the digital decimator filter is an accumulator that counts the number of times in which the output of the comparator has been positive during the entire conversion cycle. The main limitation of this solution is

that, in order to respect the output throughput specification, $\Delta_{CONV} \simeq 3\,\mu$s to keep the temperature ringing below 1.5 °C and considering a 9-bit resolution, the circuit would have to work with a clock frequency around 100 MHz to perform a complete conversion (512 clock cycles per conversion). A circuit that work at such high frequency dissipates a larger amount of dynamic power and also serious switching noise interference problems may arise in the chip between the high frequency temperature control circuit and the low frequency sensor read-out circuit. A solution to overcome these problems, paying in terms of area occupancy, is to develop a more complex decimation digital filter (Section 2.4) at the output of the comparator, to relax the specifications for the rest of the circuit.

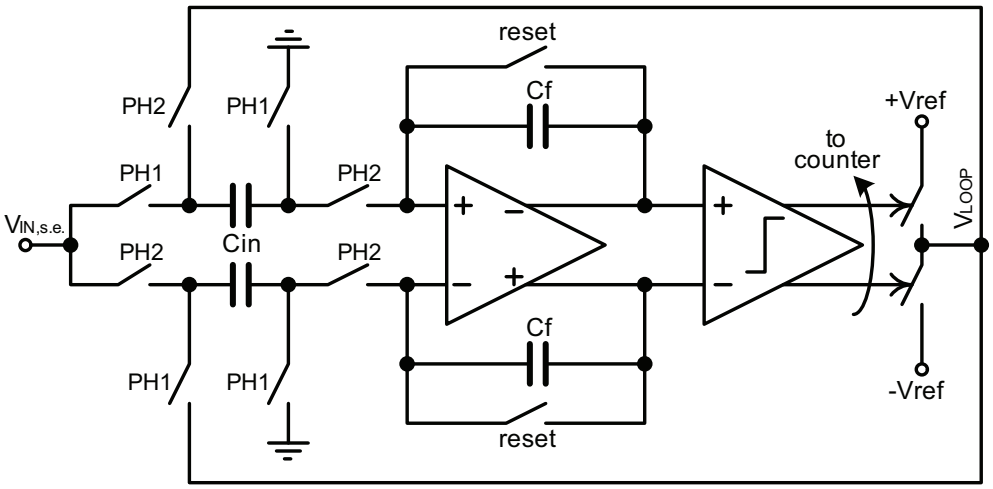

Figure 2.26: ADC analog core.

The analog core of the A/D converter (see [9], Chapter 4 for more details) is reported in Figure 2.26. It is a switched capacitor structure that is mainly composed by a fully-differential resettable integrator followed by a comparator. The input sampling network of the integrator has also the function of converting the single-ended (s.e.) signal into fully differential (f.d.). Being the amplifier fully differential a common mode feedback circuit is needed, also implemented with a switched-capacitor circuit, but is not reported in

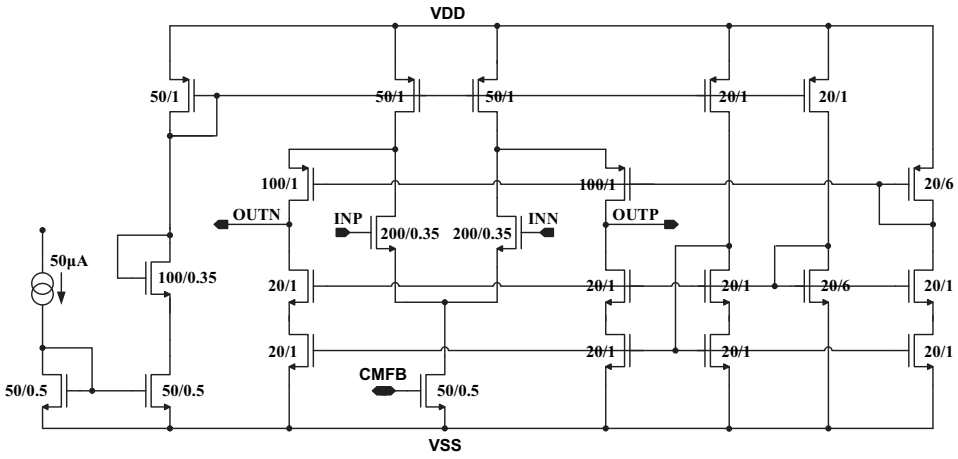

Figure 2.27: ADC folded cascode operational amplifier.

the figure for simplicity.

The amplifier embedded in the integrator is based on a folded cascode topology, as shown in Figure 2.27. It achieves a full scale linearity performance in switched capacitor signal processing of 79 dB when driven by 1 MHz clock. It exhibits a DC-gain of 79 dB and a unity-gain bandwidth of 85 MHz, while consuming 500 μW including bias branches. Particular care in operational amplifier design has been taken for the generation of the bias voltages of the folded cascode active loads in order to improve the dynamic swing performance of the amplifier which is, in simulation, 3.5 V peak-peak differential, with 3.3 V supply. The phase margin is 60 ° when the capacitive load is 1 pF.

Figure 2.28 shows the schematic of the latched comparator used in the ADC, which nominally consumes 40 μA. Different timing are used in the two paths of the integrator input circuit, to implement the s.e. to f.d. conversion. Furthermore, during PH2 the comparator samples the signal from the integrator, while it updates its output on the rising edge of PH1, actually selecting the reference value (V_{LOOP}), which will be subtracted from the input signal in the successive cycle. After 512 clock periods the value stored in

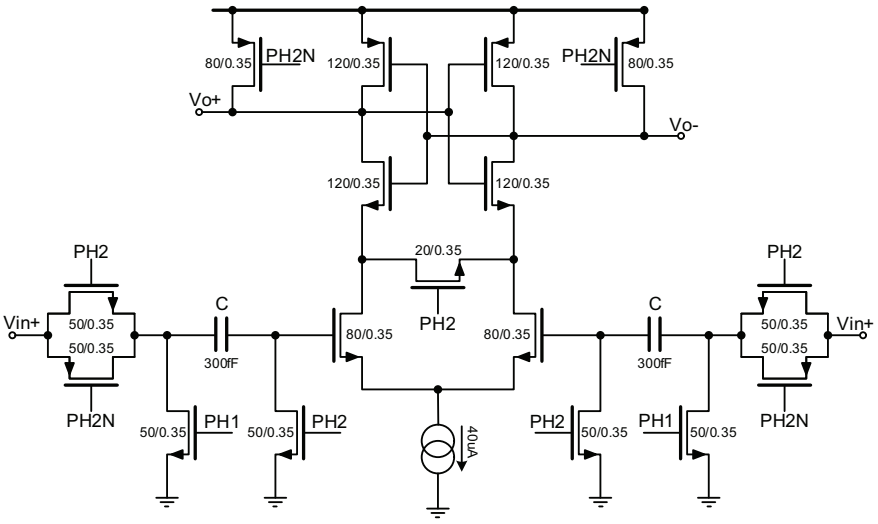

Figure 2.28: ADC comparator.

the 9-bit register, incremented of one unit every time the output of the comparator has been high, gives the digital converted value of the single ended input $V_{in,s.e.}$

2.4 Digital Decimation Filter and Control Circuit

As said in the previous section, to relax the specifications for the rest of the circuit a more complex decimation digital filter has been designed. The circuit (see Figure 2.29) is composed by three different subcircuits: a time base, a buch of flip-flops and a multiplexer. This solution presents 32 9-bit counters for each temperature control loop that process the output of the comparator. Every counter starts to count 16 clock cycles after the previous one and, as a consequence, the output of adjacent counters will exhibit a timing offset of 16 clock cycles. The time base circuit (see Appendix A.1 for the Verilog code) takes care of driving the 32 counters releasing their reset one after the other every 16 clock periods and also selects the last updated counter for the output multiplexer. This circuit is in common for all the five

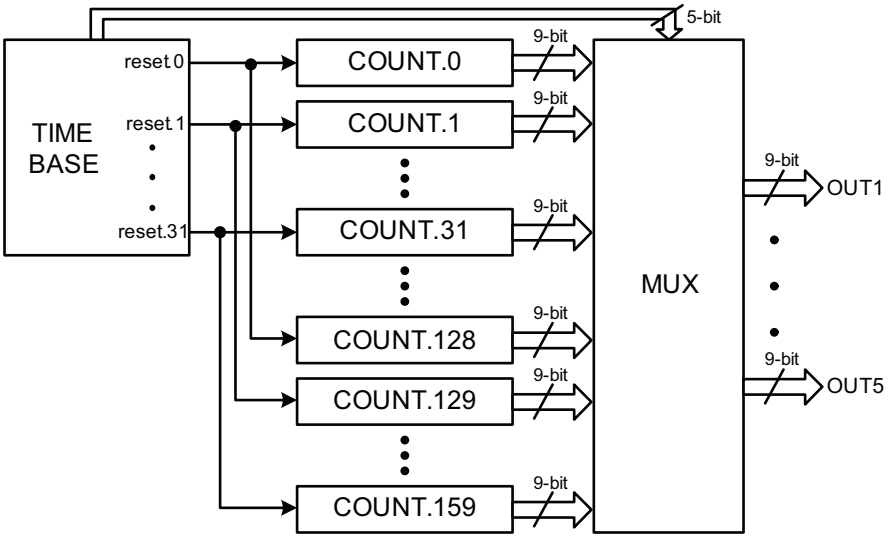

Figure 2.29: block diagram of the decimation filter.

heater circuits. The five sets of 32 registers and the multiplexer have also been joint in the same verilog file to be optimized by the digital synthesis program.

2.4.1 Closing the Loop

Since the row heater resistance, which is the series of 5 elemental heaters, is quite high and approximately five times greater than the one described in [23], the same solution where an embedded p-MOS transistor is used to feed power to the ground connected heater does not apply to this design. In fact the maximum power delivered to the heater V_{DD}^2/R_H would be five times lesser and as a consequence the maximum reachable working temperature greatly lower.

The dual solution in which an n-MOS is used to feed power to the heater connected to an high voltage pad (15-20 V), besides generating a lot of noise, would require the use of an high voltage technology too at the expense of the low voltage analog blocks.

To solve the promlem the five power transistors were moved outside the

chip and five discrete n-MOS transistors are putted on the testing boad, as shown in Figure 2.21. This way even if the thermal constants differ from the expected ones, the maximum reachable temperature can be increased by simply augment the on-board high voltage source. An inverter chain has also been designed to drive the external transistors gate capacitance (Cf $\simeq$ 10-15 pF) without introducing noticeable delay. Since the output stage of the logic control circuit is an elementary inverter (INV.0) with a gate capacitance $C_i = 3\,\text{fF}$, the optimal number of stages in the inverters chain to minimize the signal propagation delay is:

$$N = ln\left(\frac{C_f}{C_i}\right) \simeq 8 \tag{2.8}$$

Since the resulting simulated delay is resulted far lower than the minimum tolerable one, as a good compromise between area occupation and time delay a 4 stages chain has been designed with an inter-stage dimensions ratio of:

$$R = \left(\frac{C_f}{C_i}\right)^{\frac{1}{N}} \simeq 8.4 \tag{2.9}$$

An even number of stages (counting also INV.0) was chosen considering that the output of the control stage is at high level when the set-point temperature is higher than the actual temperature, i.e. when the the switch needs to be turned off.

The overall temperature control loop working princile is the same as described in [16] and [23]. The major efforts in this design have concerned the optimization of the digital block, whose area consumption has been greatly reduced while performing the same functionalities, the adjustment of the conditioning network and heater drivers electrical parameters, adapted to match the new sensor specifications, and the layout optimization of the analog blocks.

Finally, in Figure 2.30 is the simulation example of the sensor temperature regulation. In this case a low temperature (55.5 °C) has been considered

because of the very long simulation time necessary to achieve higher temperatures. To perform the simulation a substitute of the sensor has been written in Verilog-A language so that the analog loop could be closed.

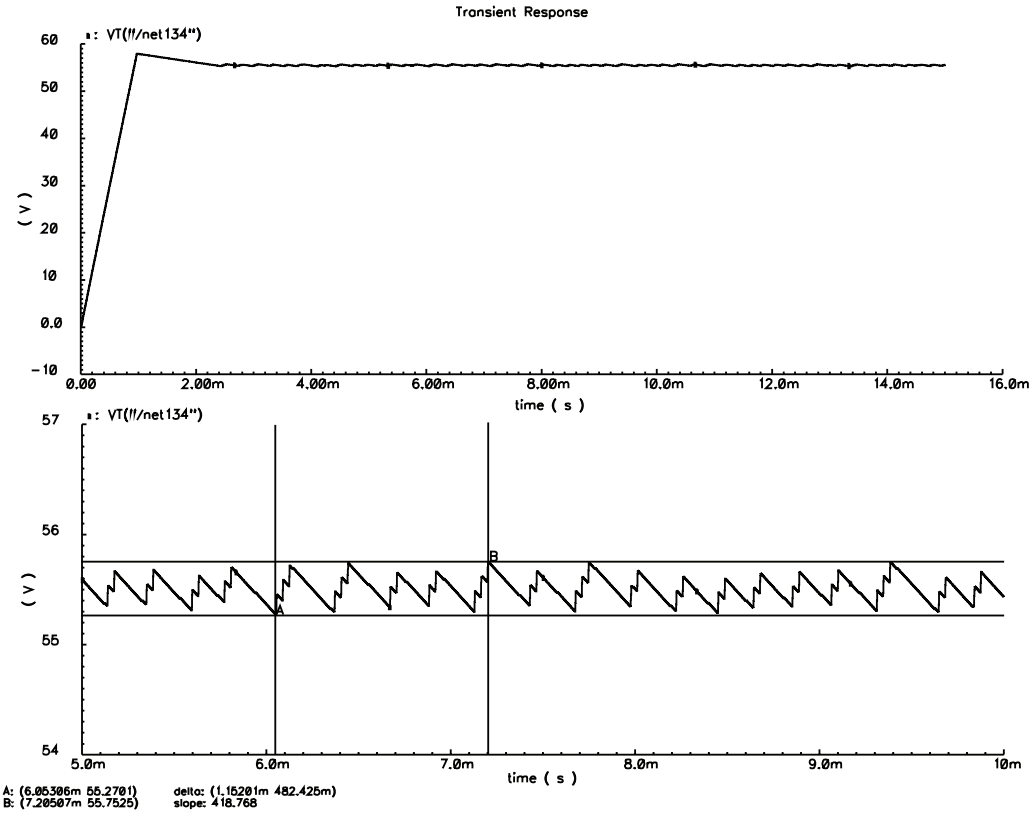

Figure 2.30: block diagram of the decimation filter.

2.5 Layout

In this section the layout of the most important blocks is presented along with the layout of the whole chip. As usual the primary rule followed in the drawing of the analog blocks has been to interdigitize and draw common centroids structures as much as possible for the matching devices, as well as a good use of common sense. A good symmetry helps also to equalize path delays and to improve some performances like the CMRR of an amplifier for

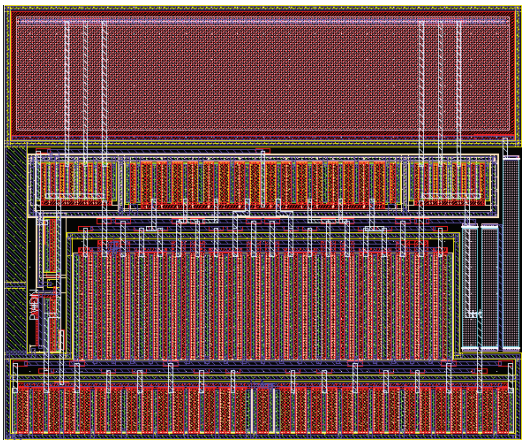

Figure 2.31: layout of the two-stages operational amplifier.

example.

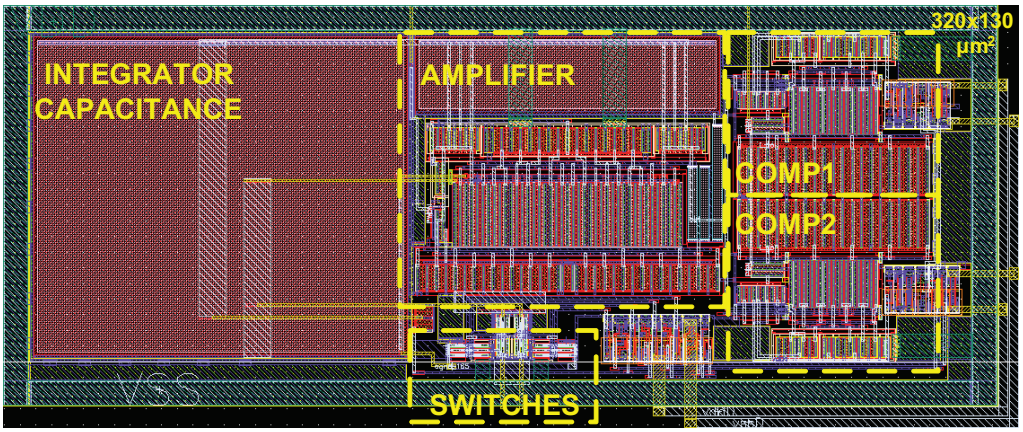

Figure 2.32: layout of the resistance dependant oscillator (AC part).

The fist layout depicted is showed in Figure 2.31 which represents the layout of the amplifier used in the resistance dependant oscillator. Figure 2.32 instead shows the whole AC part of the resistance transducer, i.e. the oscillator with the bias and mirror branches excluded, with the various blocks highlighted.

In Figure 2.33 the layout of a single bias branch is showed. Twenty of these layouts are placed side-by-side to obtain the bias branches complete layout. Even though there can be a great distance between different branches

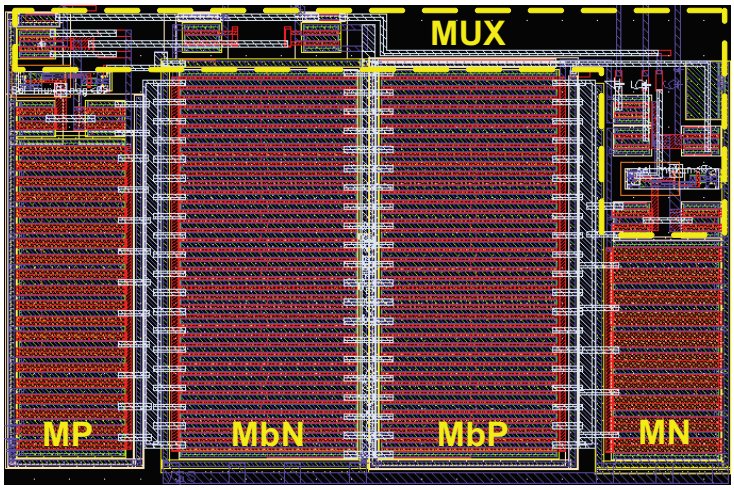

Figure 2.33: layout of a single bias branch.

the matching between the measure of different couples of the matrix terminals is not important, what matters is only the linearity of every single measurement channel. This also simplify the routing between each single branch and the corrisponding matrix termial through the dedicated pad a lot, as shown in Figure 2.34.

Figure 2.35 shows the layout of the analog blocks of a single temperature control loop, in which the ADC, the current generator and the pre-amplifier of the conditioning network are highlighted. Since during one measurement the input code of the DAC remains constant, the accuracy of the ratios between current mirrors is not very important thus layout and interconnections easyness has been preferred over interdigitation. All the five temperature loops are shown togheter in Figure 2.36. This part of the chip contains also all the 5 MHz digital circuits, i.e. the time base, registers and multiplexer of the temperature control and the I^2C slave.

Finally, in Figure 2.37 is the layout of the whole chip, containing all the blocks already described.

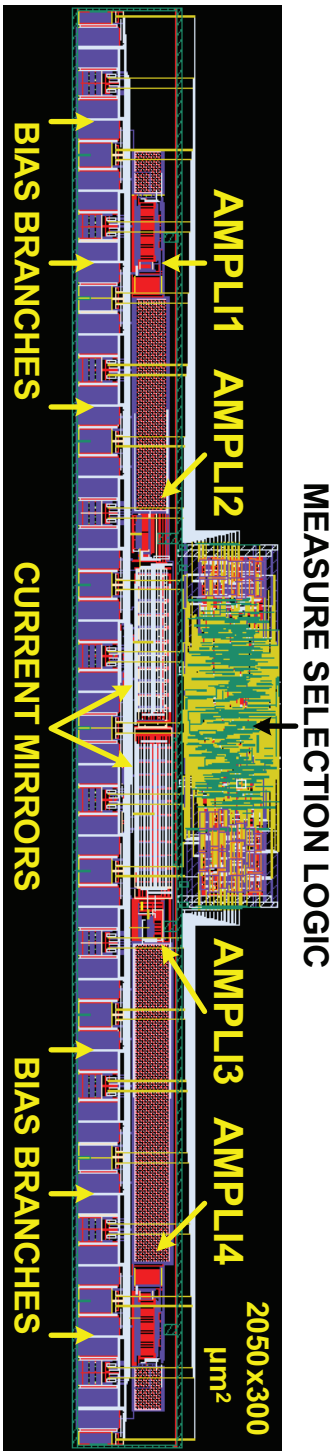

Figure 2.34: layout of the resistance dependant oscillator (DC part).

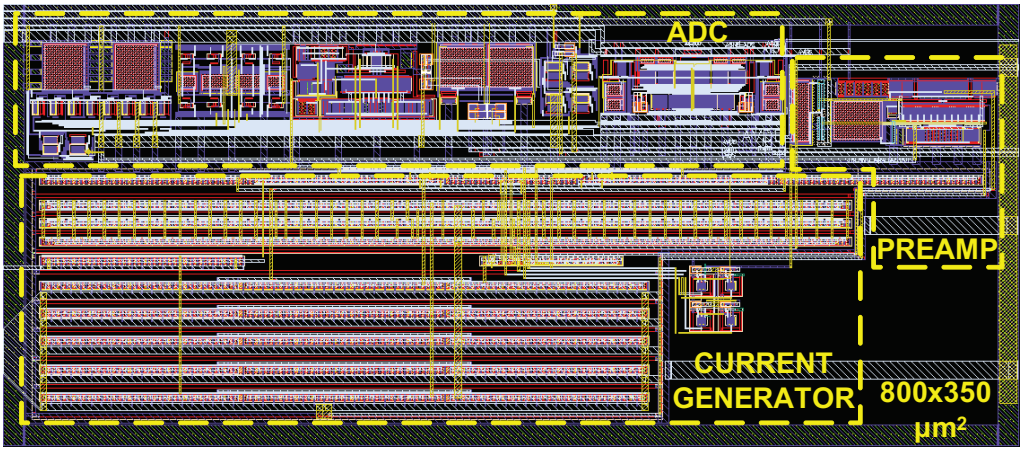

Figure 2.35: layout of a single temperature control loop (analog part).

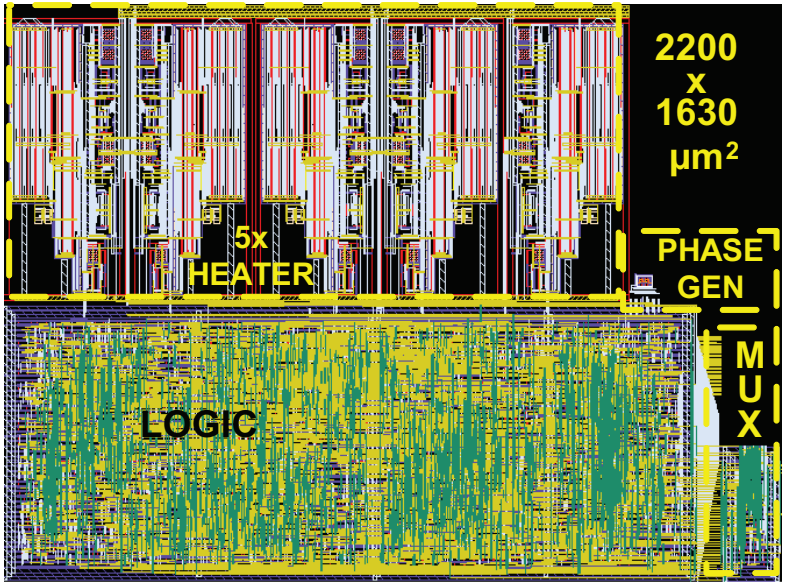

Figure 2.36: layout of the 5 whole temperature control loops.

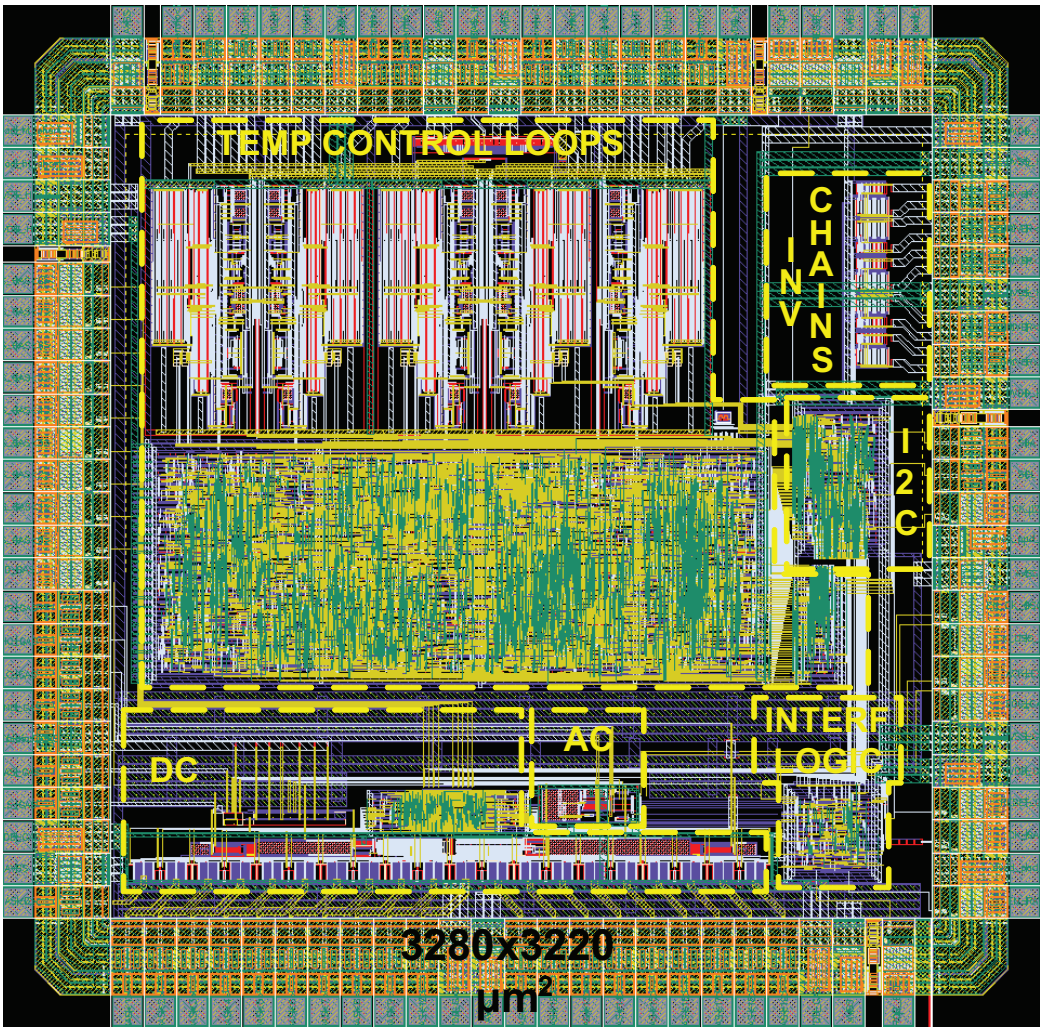

Figure 2.37: layout of the chip.

Chapter 3

HIGH PRECISION VOLTAGE REFERENCE

Voltage reference circuits are very common and used in a wide number of applications. The testing of the gas sensor interface requires intense use of such devices but with very different characteristics. The aim of this chapter is to present the design of an high precision micro-power voltage reference which can be considered competitive with commercial devices and with electrical characteristics as more general porpouse as possible. The resulting device should be stable, able to sink/-source current to/from a load, suppress the power source and thermal fluctuations, provide different voltage levels as output and with very low power consumption.

3.1 IC Overview

The circuit is composed by two major blocks, as shown in Figure 3.1: a bandgap and an amplifier. The bandgap block generates a voltage which is (almost) independant from the external power source and temperature variations. In particular, the reference voltage is generated by a current based cell and it features a second order temperature compensation. Because of the high output resistance of a bandgap cell, which typically is higher the lower is the power consumption, a buffer amplifier is needed too when the aim is to

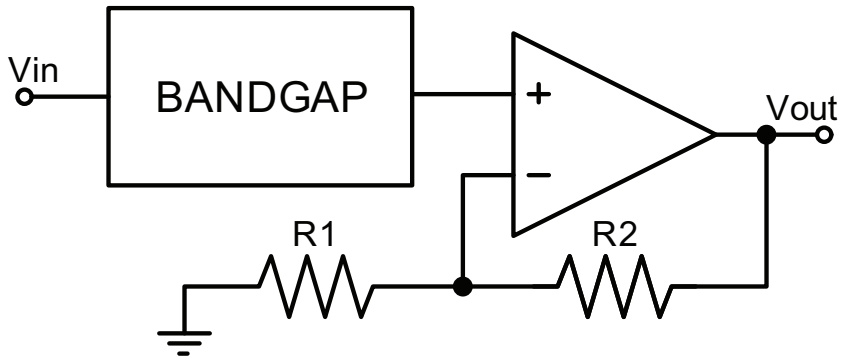

Figure 3.1: Block diagram of an LDO voltage regulator.

source/sink current to/from a load. To keep the overall current consumption in the μA range a class AB output stage has been designed for the amplifier. As shown in Figure 3.1 the bandgap voltage is not simply buffered by the amplifier but a gain factor has been introduced. This way the bandgap can be designed to exibit an output voltagge of 1 V and the various versions of the chip with different regulated outputs are obtined by simply changing the amplifier feedback gain.

Between the reference voltage generator and the error amplifier a low pass filter has been designed. This filter can be enabled if the noise performace of the device results to be worse than the expected one.

The most important parameter for the LDO study is the definition of the output load (see Figure 3.2). The load is usually divided in a capacitive part and a resistive one. The capacitive part defines the frequency of the pole related to the output node, while the resistive one defines both the gain of the output stage of the amplifier and the current flowing through the load. While the capacitance value C_L can be set to an high enough value to make the output pole dominant or to a low enough value to make an internal pole dominant by specification, not knowing the exact nature of the load makes it impossible to predict R_L accurately, yet its impact on stability and circuit requirements can be very demanding from the designing point

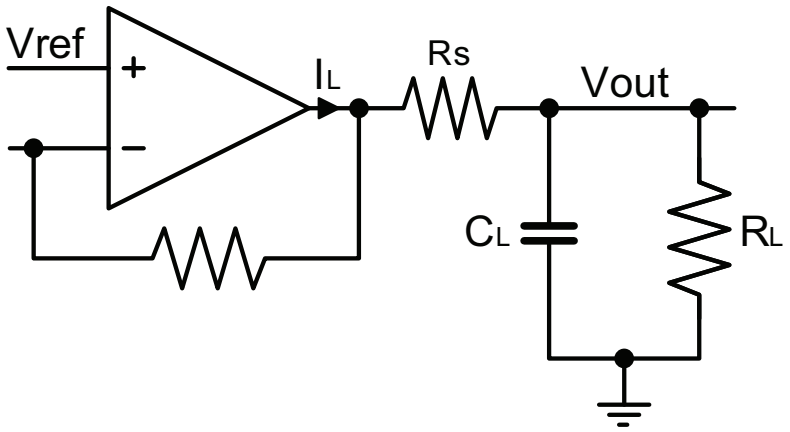

Figure 3.2: simplified LDO output load.

of view. In the case of internally compensated LDOs, for instance, whose output pole is parasitic to the system, a purely resistive load places the output pole at optimistically higher frequencies. Subjecting this LDO to a higher impedance load pulls the output pole to lower frequencies, compromising the stability of the system. Similarly, assuming the load is purely active, that is, only a current sink, may be unrealistically optimistic in the case of externally compensated LDOs, where the dominant low-frequency pole is at the output and a high-impedance load optimistically places this pole at lower frequencies. A lower impedance load pushes the output pole to higher frequencies, closer to the parasitic poles of the system, where stability may be compromised.

The role of R_S is also vary important, causing voltage drop and power losses on the load, while affecting the stability of the sistem too. This is usually considered in the low resistance range (R_S <1 Ω) meaning as well the use of good on-board capacitors.

3.2 Bandgap Reference Circuit

The most important performance parameters of a voltage reference circuit are represented by temperature behavior, power supply rejection ratio, transient response and, for the latest designs, by low-power low-voltage operation [30]. Depending on the load requirements, the output of the circuit can be regulated or unregulated. In order to reduce the sensitivity of the reference voltage with respect to the supply voltage variations, modified cascode structures can be implemented, a trade-off between line regulation and low-voltage operation being necessary in this case. Another important trade-off has to be made between a large bandwidth of the voltage reference, which improves the transient behavior of the circuit, and noise rejection.

3.2.1 Temperature Compensation

The output voltage of a bandgap circuit is usually composed by two contributions: one is the voltage across a directly biased diode (base–emitter voltage) and the other is a term proportional to the absolute temperature (PTAT). The negative temperature coefficient of the former term compensates for the positive temperature coefficient of the latter. If $V_T = \frac{kT}{q}$ is used to obtain a PTAT voltage, the bandgap output voltage is given by:

$$V_{BG} = V_{BE} + n \cdot \frac{kT}{q} \tag{3.1}$$

It is well known that using an n value of 22 the first order temperature compensation is achieved and the output voltage obtained is approximately 1.2 V. This voltage, however may be unpractical for low voltage applications.

To solve this problem, a fraction of the traditional bandgap voltage can be obtained by scaling both terms of equation 3.1 using currents proportional to V_{BE} and V_T. These currents are suitably added and transformed into a voltage by means of a resistor. The temperature dependence of the resistors used by obtain these currents is compensasted by fabricating them with the

same kind of material. Figure 3.3 shows the schematic of a circuit able to implement the described operation [25]. Two diode connected bipolar tran-

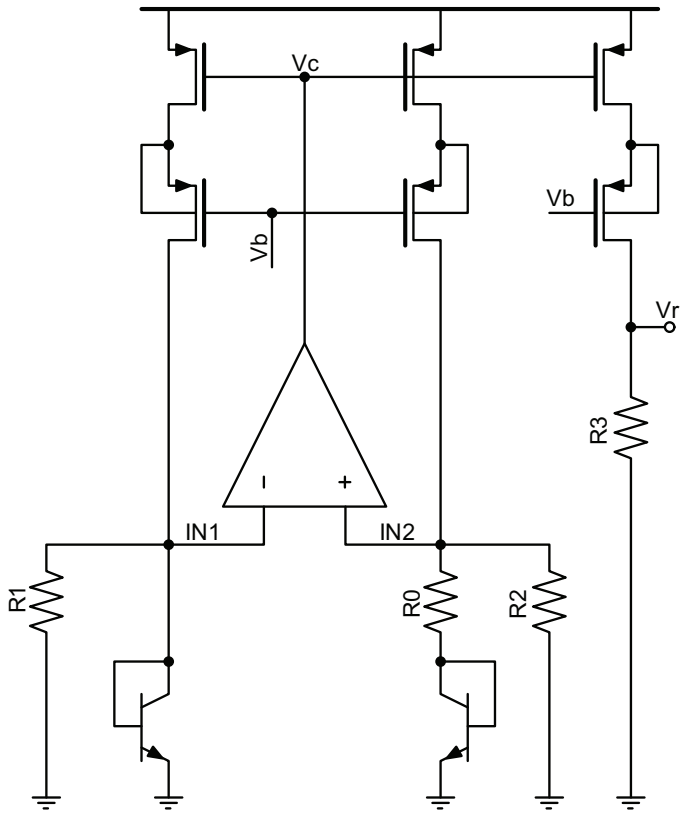

Figure 3.3: current bandgap structure.

sistors with different emitter area, whose ratio is N, sink the same current, leading ΔV_{BE} to be equal to $V_T \ln N$. The current in R0 is therefore PTAT. Since the operational amplifier forces the two voltages V_{IN1} and V_{IN2} to be equal, the current in the nominally equal resistors R1 and R2 will be proportional to V_{BE}. As a result, the current in M1, M2 and M3 is the same (if their dimensions are equal) and is given by:

$$I_1 = \frac{V_T \cdot \ln N}{R_0} + \frac{V_{BE}}{R_1} \tag{3.2}$$

The output voltage is simply given by $I_1 \cdot R_3$ and the first order compensation

is achieved by chosing a value for N and $\frac{R_1}{R_0}$ which satisfies:

$$\frac{R_1}{R_0} \cdot \ln N = 22 \tag{3.3}$$

If N = 8 to minimize both the area consumption and the spread of the bipolar transistors and a minimum value for R_1 is chosen to minimize the power consumption, the value of R_0 is readily obtained. In particular $R_1 = 600\,k\Omega$ and $R_2 \simeq 6.4\,M\Omega$ has been chosen.

Moreover, since transistors M1, M2 and M3 maintain almost the same drain–source voltage V_{DS}, independently of the actual supply voltage, the power supply rejection ratio of the circuit is only determined by the operational amplifier.

Since the base-emitter voltage V_{BE} of a bipolar transistor does not change linearly with the temperature, the simple temperature compensation described is not sufficient if the required precision is at the level of ppm/°C. A more accurate equation to the describe the temperature dependency of the V_{BE} voltage [30] is:

$$V_{BE}(T) = V_{g0} - \frac{T}{T_r} \cdot [V_{g0} - V_{BE}(t_r)] - (\eta - \chi) \cdot V_T \cdot \frac{T}{T_r} \tag{3.4}$$

where η depends on the bipolar structure and usually has an approximate value between 3.6 and 4, V_{g0} is the extrapolated diode voltage at 0 °K, T_r is the reference temperature and χ equals 1 if the current in the BJT is PTAT and goes to 0 when the current is temperature independent. Various approaches to compensate for the nonlinear term have been proposed in [20], [31]. In this design the basic idea has been to correct the nonlinear term by a proper combination of the voltage across a junction with a temperature-independent current ($\chi = 0$) and the voltage across a junction biased with a PTAT current ($\chi = 1$). Referring to the circuit of Figure 3.3 it can be noted that the current in the bipolar transistors (Q1 and Q2) is PTAT while the current in the p-MOS transistors is at first-order temperature independent.

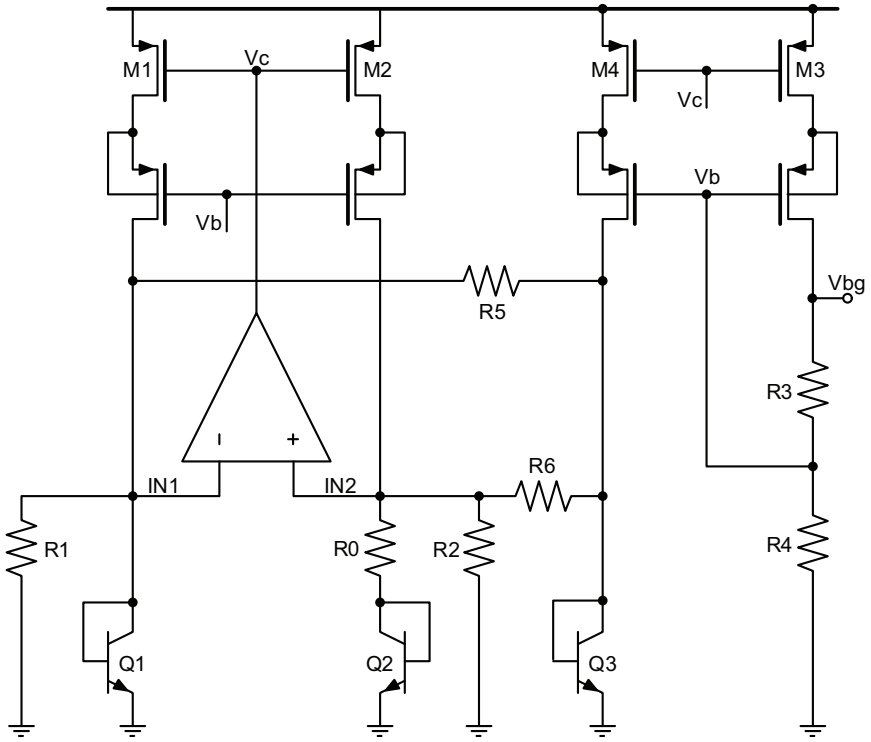

Figure 3.4: current bandgap structure.

Therefore, if the current of the p-MOS transistor is mirrored into a diode connected bipolar transistor (Q3), as shown in Figure 3.4, across Q3 a V_{BE} with a χ close to zero is produced.

Using equation 3.4, the V_{BE} of bipolar transistors Q3, Q1 and Q2 can be expressed as:

$$V_{BE,Q3}(T) = V_{g0} - \frac{T}{T_r} \cdot [V_{g0} - V_{BE}(t_r)] - \eta \cdot V_T \cdot \frac{T}{T_r} \tag{3.5}$$

$$V_{BE,Q1,2}(T) = V_{g0} - \frac{T}{T_r} \cdot [V_{g0} - V_{BE}(t_r)] - (\eta - 1) \cdot V_T \cdot \frac{T}{T_r} \tag{3.6}$$

The difference between $V_{BE,Q3}$, $V_{BE,Q1}$ and $V_{BE,Q2}$ leads to a voltage proportional to the non linear term given by:

$$V_{NL} \simeq V_{BE,Q3}(T) - V_{BE,Q1,2}(T) = V_T \cdot \ln \frac{T}{T_r} \tag{3.7}$$

Curvature compensation has thus been achieved subtracting from both I_{M2} and I_{M1} a current proportional to V_{NL}. This can be obtained by introducing

resistors R5 and R6 (nominally equal), which drain from M1 and M2 the required currents, thus leading to:

$$V_{BG} = \frac{R_3}{R_1}\Big(\frac{R_1 \cdot \ln(N)}{R_0} \cdot V_T + V_{BE} + \frac{R_1}{R_{4,5}} \cdot V_{LN}\Big) \tag{3.8}$$

The value of R5 and R6 which leads to the proper curvature correction can be derived by comparing 3.6 and 3.8:

$$R_{4,5} = \frac{R_1}{\eta - 1} \tag{3.9}$$

and parametric simulations has been used to come to the proper value to optimize the thermal coefficient. In the simulation section is reported the temperature coefficient simulation showing second order temperature compensation. According to what said in the introduction the temperature range has been chosen to match the largest commercial range. The thermal coefficient may be calculated as (Figure 3.15):

$$TC = \frac{V_{O,Max}(T) - V_{O,Min}(T)}{V_{BG} \cdot (T_{Max} - T_{Min})} \simeq 2\,\frac{ppm}{^\circ C} \tag{3.10}$$

at simulation level. This very low result can be made repetitive despite process and mismatch variations with the use of a trimming strategy as will be described in Section 3.4.

3.2.2 Bandgap Amplifier

The bandgap circuit needs an operational amplifier whose input common-mode voltage is approximately 0.65V (the V_{BE} value). Since its output has to drive p-MOS current sources the output common mode should be at the voltage V_{DD} - $V_{th,P}$. Moreover it has been proved that a DC gain of 60 dB, without bandwith constraints, would be enough for the bandgap to operate correctly.

In Figure 3.5 is the schematic of the bandgap amplifier. Two grounded bipolar transistors has been used to operate as input differential pair instead

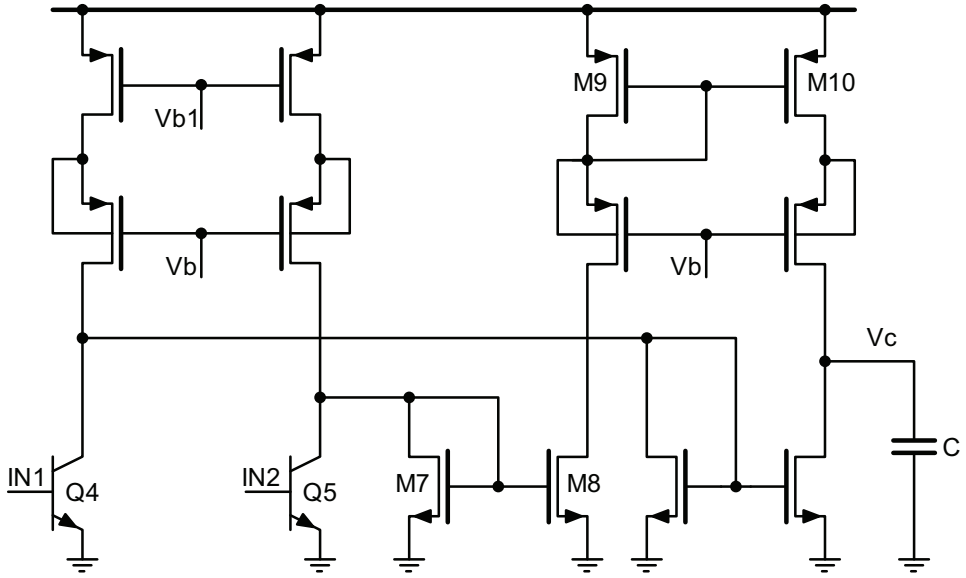

Figure 3.5: bandgap two-stage amplifier.

of the classical circuit with the tail current generator, sparing the 0.15 V needed at least to keep in the saturation region the current generator. In fact a current control is not needed being the current in the input stage already a replica of the bandgap current. The signal current generated by the input differential pair Q4–Q5 is folded and collected by two diode connected MOS transistors (M7 and M8). The second stage is a push–pull circuit. Since the quiescent value of the output voltage is one $V_{GS,p}$ below V_{DD}, the V_{DS} voltages of M9 and M10 match, and the systematic offset of the second stage is practically zero as well. For the same reason an excellent power supply rejection ratio and common-mode rejection ratio are obtained.

The bias current in the operational amplifier matches the current flowing in the bandgap, which in turn is designed low. However, since the bias current of the circuit has a PTAT feature, power consumption will increase proportionally to the absolute temperature. Finally, the stability of the whole bandgap circuit under any operating conditions is assured by the compensating capacitance C.

3.2.3 Start-Up Circuit

The designed bandgap reference needs a more effective startup circuit than those usually adopted, consisting of simple pull-up or pull-down capacitor. In fact a significant amount of current has to flow in the resistors R1 and R2 in order to turn on diodes Q1 and Q2.

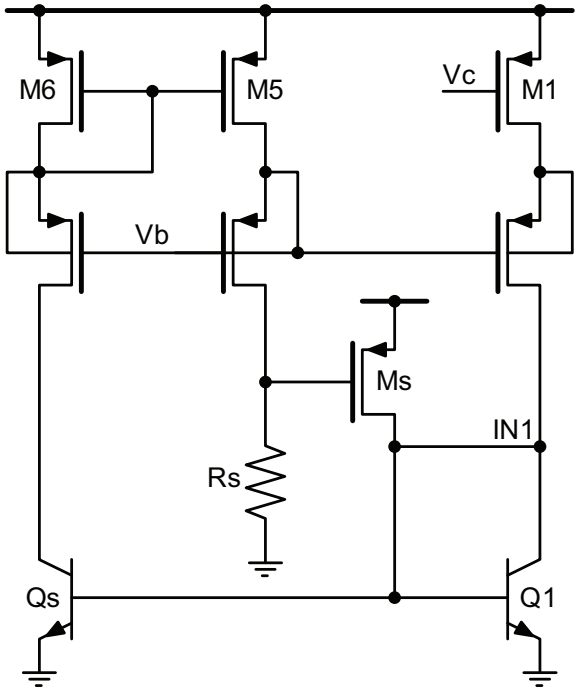

Figure 3.6: start-up circuit inplemented.

In Figure 3.6 is shown a start-up circuit which continually provides the additional current to the diode connected transistor Q1 until the circuit reaches the proper operating point. In particular, if the current in IN1 is zero, the current in M3 is zero as well, and the p-channel current source M5 is off. The gate of Ms is pulled down to ground, thus injecting a significant current into Q1 and R1. At the end of the startup phase, when the circuit reaches the normal operating conditions, the current in M5 and the value of Rs used bring the gate of Ms close to V_{DD}, thus turning off the startup circuit. A very large resistance value for Rs has been used to reduce the leakage current

in Ms.

3.3 Error Amplifier

In the design of the error amplifier the main specifications has been considered in order to mantain the general porpouse operation characteristic. In particular, the major efforts have been focused on:

- driving a wide range of output capacitive loads;
- ability to source and sink currents in the mA range;
- supporting a wide range of input voltages;
- keeping the current consumption as low as possible.

The schematic of the implemented amplifier is reported in Figure 3.7. It

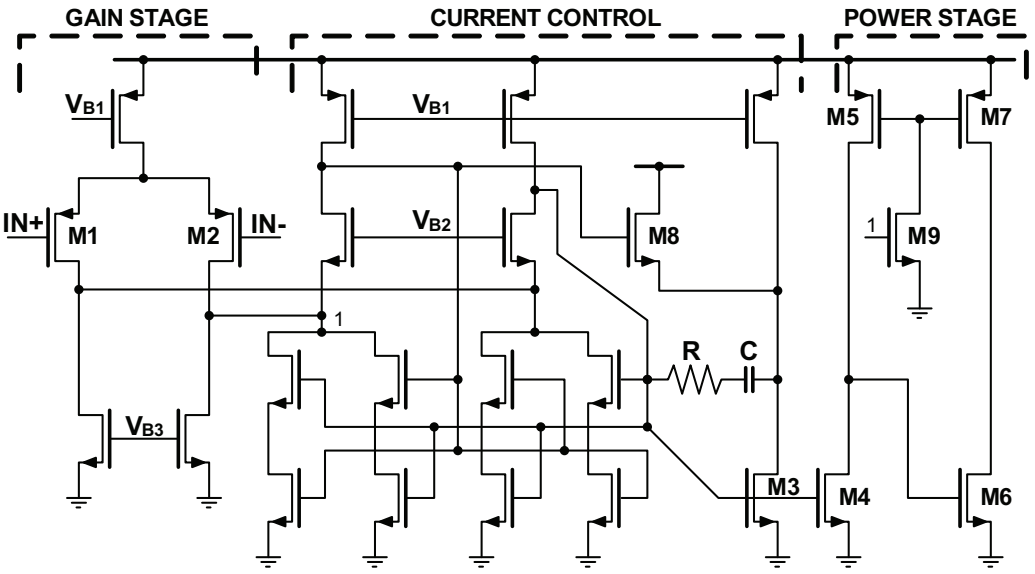

Figure 3.7: class AB error amplifier.

consists in a two stages amplifier with push-pull output stage.

As required by low power functionality, a class AB output stage has been chosen for it represents a good trade-off between power consumption

and distortion. This way the output transistors can be biased with a small quiescent current compared to the maximum output current while reducing crossover distortion in comparison with a class B output stage. To obtain the control for the class AB output stage a non-linear circuit is necessary and can be implemented by a translinear circuit. Referring to Figure 3.8, if all transistors have the same dimensions, when I_N is much larger than I_B,

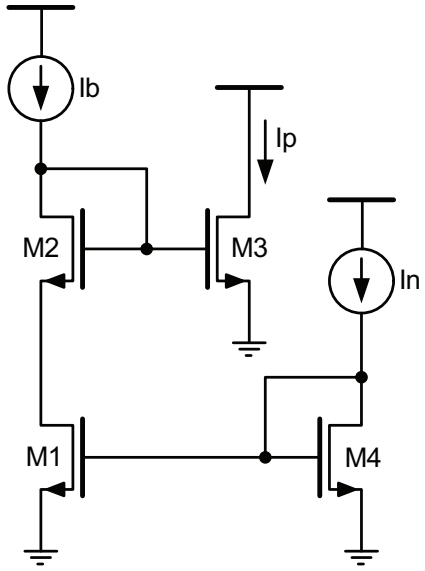

Figure 3.8: minimum current selector circuit.

transistor M1 operates in the linear region. Consequently, $V_{GS,M2} = V_{GS,M3}$ and $I_P = I_B$. When I_P is much larger than I_B, the voltage $V_{D,M1}$ increases forcing M1 to operate in saturation and $I_N = I_B$. Finally, for $I_N = I_P$ $V_{GS,M3}$ = $V_{GS,M4}$ so M1 and M2 behave as the series association of two transistors. Therefore, $I_N = I_P = 2 \cdot I_B$. This circuit, called *minimum current selector*, is asymmetric. To convert it into a symmetrical circuit, transistors M1 and M2 are divided into $M1_A$, $M1_B$, $M2_A$, and $M2_B$, as shown in Figure 3.9.

The LDO regulator must work with a maximum supply voltage of 5.5V. For this reason many internal nodes in the circuit reach high voltages. In particular, there are some V_{GS} and V_{DS} voltages greater than 2.5V. This

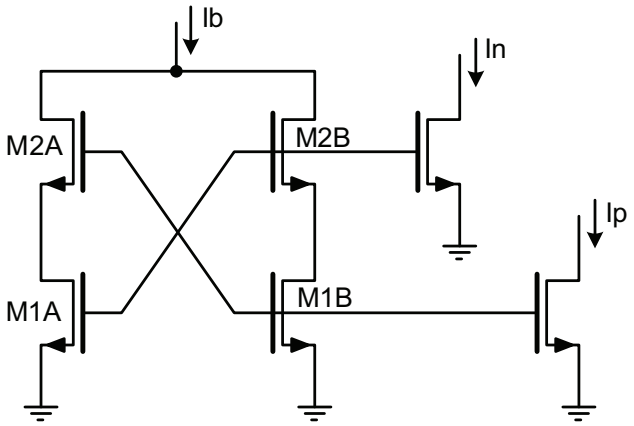

Figure 3.9: symmetrical minimum current selector circuit.

makes it necessary the use of MOS transistors with greater thickness of gate oxide and consequently with greater threshold voltages. Consequently, the biasing of the circuit is made more problematic when the voltage supply is 1.8V and the load current is high. Therefore, to ensure that the LDO works correctly also in these conditions, it is necessary to enlarge the width W of the channel of the power transistors to reduce their gate voltage. There is consequent enlargement of the gate capacitance that further complicates the stability study.

3.4 Trimming

The trimming of this device has been an important and time-consuming activity. The trimming strategy is made up of three diffent trimmings:

- a trimming which defines the device version;
- a trimming to settles the thermal coefficient;
- a trimming to settle the output voltage.

The first trimming defines the device version i.e. defines the output voltage range by changing the error amplifier feedback resistances as shown in Figure

3.10. This kind of trimming is achieved through a technique called *metal*

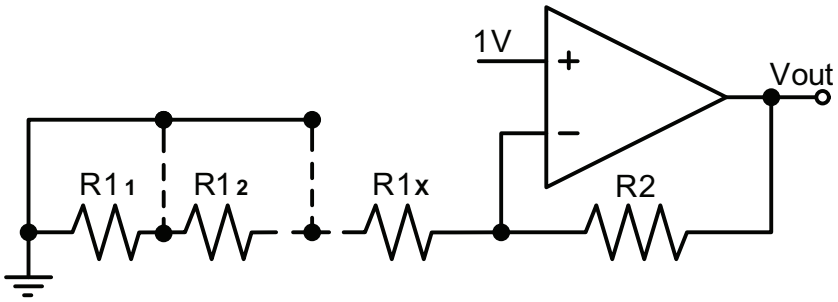

Figure 3.10: device version selection.

option in which the various versions of the device (mainly 1.25 V, 1.8 V, 2.5 V, 3.3 V) are obtained with the change of a single fabrication mask, and in particular by changing metal1 mask. This means that all the contacts which connect the various resistance slices to ground potential are already predisposed in the general layout which is in common and the same for all versions except for a metal1 segment.

The second trimming is related to the resistance R0 of the bandgap circuit (see Figure 3.11) and aims to the calibration of the thermal coefficient. Since the thermal coefficient, as shown in equation 3.3 is given by the $\frac{R1}{R0}$ ratio, a fine trimming of the R0 resistance leads to an optimized thermal coefficient. The R0 resistance is thus composed by a fixed term (R3) and a variable one ($R3_X$) which is composed by the series connection of six unity resistances, each with a fuse in parallel. Each of the six fuses, also called *laser fuse*, is usually closed and can be shot with a laser beam to be made open. The operation is, of course non reversible.

The last trimming is performed on the resistance R3 of the bandgap circuit to finely adjust the output of the bandgap to 1 V. This trimming is performed in a very similar way as the one already described for the R0 resistance. There is again a fixed resistance R0 and a variable one $R0_X$ which is composed by 7 series connected unity resistances with a laser fuse

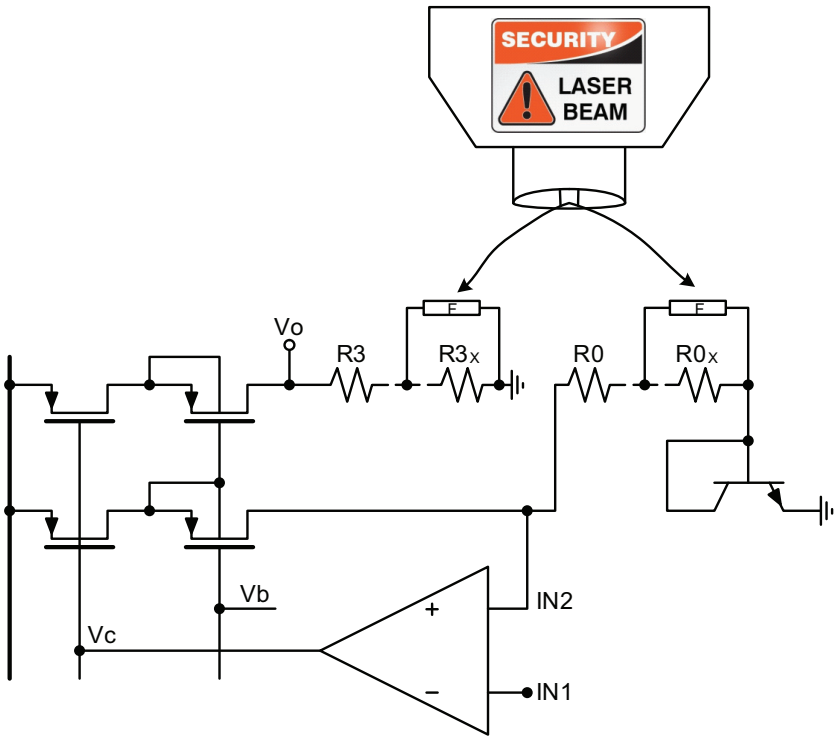

Figure 3.11: bandgap trimming.

in parallel. This trimming, as will be explained in the next section, must be performed after the thermal coefficient one.

3.4.1 Trimming Strategy

Before stating the effectiveness of the trimming strategy a correlation must be found between a probe of the untrimmed output and the the resistance to be trimmed. While for the R3 resistance the process is straightforward being the output voltage of the LDO directly dependant on that resistace value, for R0 the situation is more complicated and the trimming cannot be performed with a single measure of the output voltage. The correlation function between the output and the R0 value has been tested with cadence simulations and, to achieve a correlation high enough to be of interest, two measures of the output voltage must be performed with the circuit working

at two different temperatures whose difference is at least 40 °C

After this correlation has been found an Ocean script has been developed to achieve the trimming words for both R0 and R3. This script runs a montecarlo simulation for both process and mismatch variations fixing at each step the montecarlo index while performing the following operations:

1. a DC temperature sweep is launched;
2. ΔV = V_0(25°C)-V_0(65°C) is acquired and, through preliminary coefficients, the corresponding R0 trimming word (W0) is calculated;
3. starting from the initial W0 value a while cycle is performed to refine its value, incrementing or decrementing W0 by one each step towards the reduction of the thermal coefficient. If no value for W0 is found, which brings the thermal coefficient into the specification range within 8 steps, the montecarlo iteration is marked as *out of spec*;
4. if the R0 trimming succeeds the R3 trimming cycle starts in a very similar way except that because of the greater variation range of W3 the while cycle has been split into a rough cycle where W3 is incremented/decremented by 5 and a fine cycle where W3 is incremented/decremented by 1. Again, if no value for W3 is found, which gives the output voltage sufficient precision the montecarlo iteration is marked as *out of spec*;
5. finally, the script returns the values of W0 and W3 found, the corresponding ΔV and $V_{0,PT0}$ (output voltage obtained after the R0 trimming) and the number of out of spec iterations. As said the iteration is set out of spec if the thermal coefficient is greater than 8 $\frac{ppm}{°C}$ or the output voltage precision is lower than 1 ‰ of the steady-state value.

The correct coefficients, which give no out of spec iterations, have been obtained through multiple learning Ocean script runs, being refined after

```
%RUN |deltaV    |ppm_pre  |W0   |ppm_PT |V0_PT0      |W3 |V0_PT3      |ppm     |prec_permil
1    -0.005953   113.53     36     4.99     1.174287     76  1.250398     5.45     0.32
2    -0.003236   59.09      17     5.23     1.212580     36  1.249647     6.74     0.28
3    -0.006139   119.70     37     5.11     1.181866     67  1.249905     5.39     0.08
4    -0.004383   82.57      25     4.71     1.190584     58  1.250124     2.81     0.10
5    -0.003691   69.89      20     6.45     1.204479     44  1.250170     6.70     0.14
6    -0.005590   102.13     32     6.39     1.217109     32  1.250269     6.67     0.22
7    -0.003722   69.05      21     6.13     1.194511     54  1.249670     6.41     0.26
8    -0.002779   50.48      15     4.88     1.229877     19  1.249756     4.95     0.19
9    -0.004642   87.29      26     5.62     1.204294     44  1.249850     5.81     0.12
10   -0.004521   85.85      26     6.91     1.197559     52  1.250338     6.15     0.27

out of spec= 0
```

Figure 3.12: Ocean script output file example.

each run with Matlab polyfit function. In particular a 5^{th} order polynomial equation has been chosen to obtain both W0 and W3 as a good compromise between equation complexity and results. The goodness of the equation found has been tested over 800 montecarlo iteration in which the searching cycles for W0 and W3 have been disabled and no iteration has resulted out of spec. In Figure 3.12 is an example of the Ocean script result for 10 montecarlo iterations. Following this example, the Matlab script executes the 5^{th} order polyfit function between columns 4 and 2 to refine the W0 value and between columns 7 and 6 to refine the W3 value.

3.5 Noise Filter

To reduce the bandgap noise, which arises from the use of large resistors, a low pass filter has been implemented. This filter can be turned on or off according to noise measurements. Because of the very small bandwidth needed to perform an effective filtering, the use of an off transistor has been mandatory to achieve a low frequency pole. This transistor is turned off as soon as the circuit reaches a steady-state condition. In particular a p-channel transistor has been used, as showed in Figure 3.13, for it can be implemented in a separate n-well biased with the bandgap voltage so that there is no leakage current to corrupt the bandgap output voltage. The only

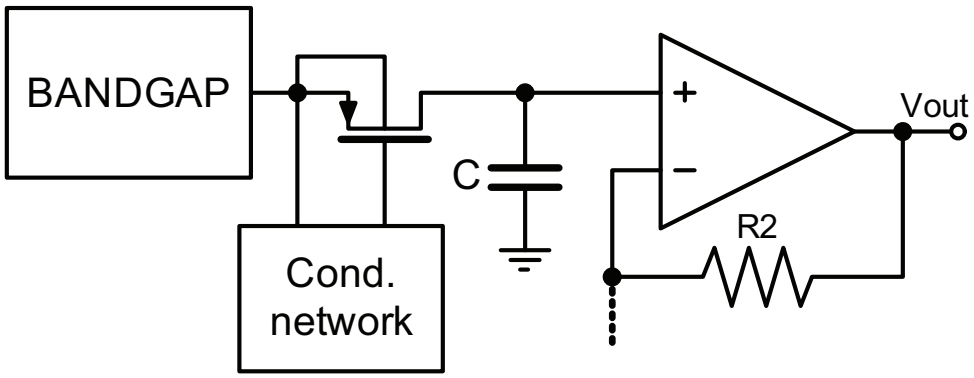

Figure 3.13: noise filtering solution.

problem in this circuit is that, due to the drain leakage current, the output of the filter tends to drift toward ground potential with a very high time constant. As a solution a low frequency oscillator has been implemented to generate a reset pulse which "resets"the filter turning the transistor on for 400 μs over a period of about 10 seconds.

3.6 Layout

The layout of the chip is showed in Figure 3.14. To reduce the mismatch the bandgap resistors have been separated from the transistors part and arranged in a common centroid structure where necessary. For the same reason the 8:1 bandgap bipolar transistors have been arranged in a 3x3 matrix with the 1 in the middle. Moreover the bandgap resistors have been oriented to result in parallel with the isotherm lines arising from the power stage of the amplifier.

The laser fuse section has been surrounded with a special layer to avoid thick oxide passivation which would prevent laser trimming capability.

The total area occupation for this chip is 500 μm x 700 μm

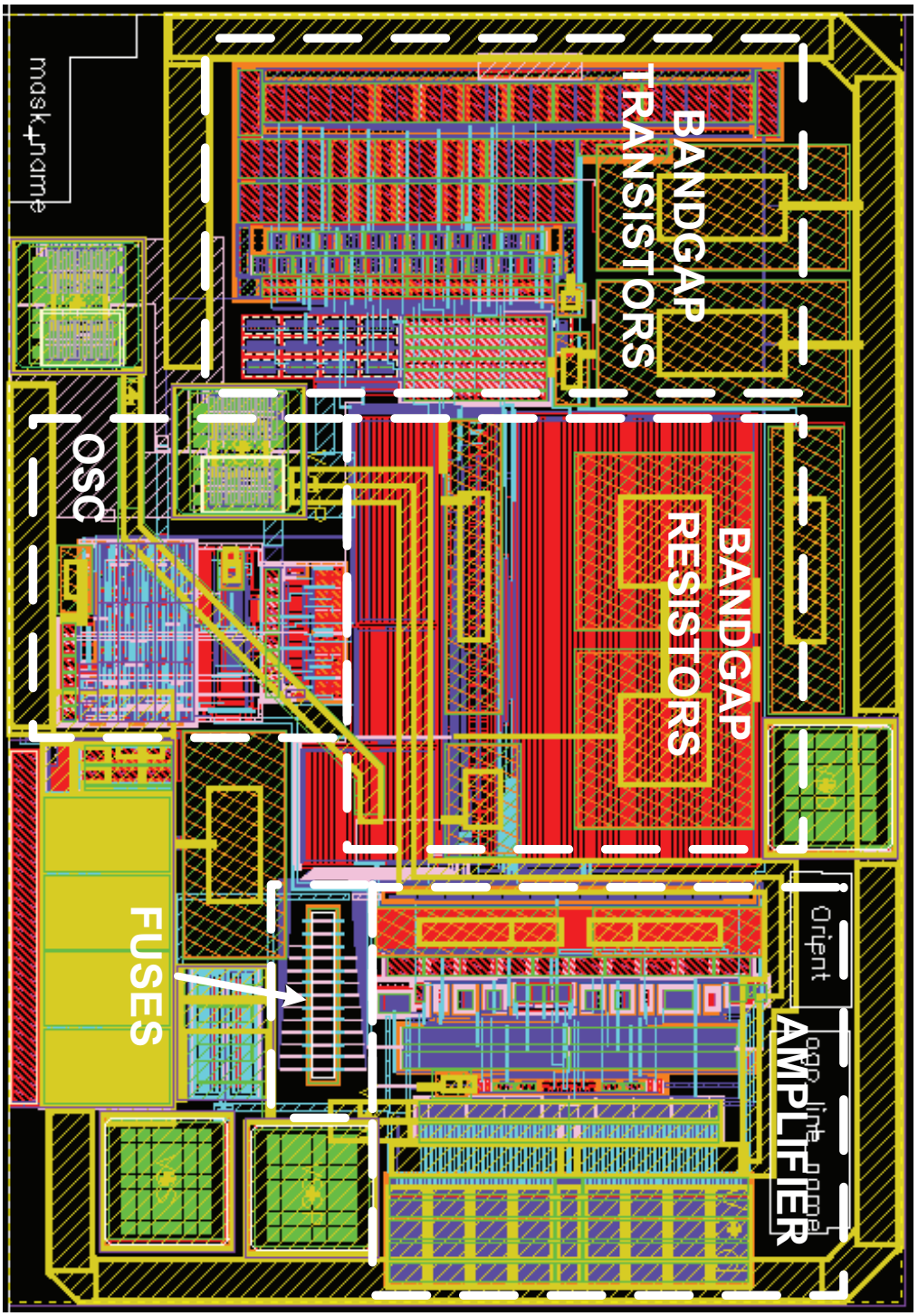

Figure 3.14: LDO layout.

3.7 Simulations

A summary of the most important simulations related to the LDO design is reported in this section. All the reported simulations refers to 1.25 V device version. The first parameter which has to be verified is the circuit thermal coefficient. Figure 3.15 shows the temperature behavior of the LDO. It can

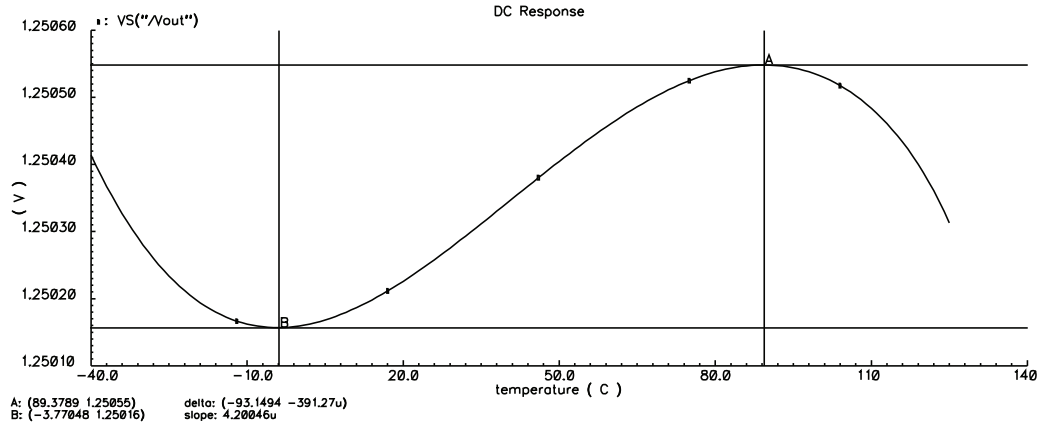

Figure 3.15: temperature coefficient simulation.

be seen that the second order compensation has been achieved because the variation with temperature has a third order trend. Recalling equation 3.10 a thermal coefficient lower than 2 $\frac{ppm}{°C}$ over a temperature range of 165 °C has been obtained with typical models.

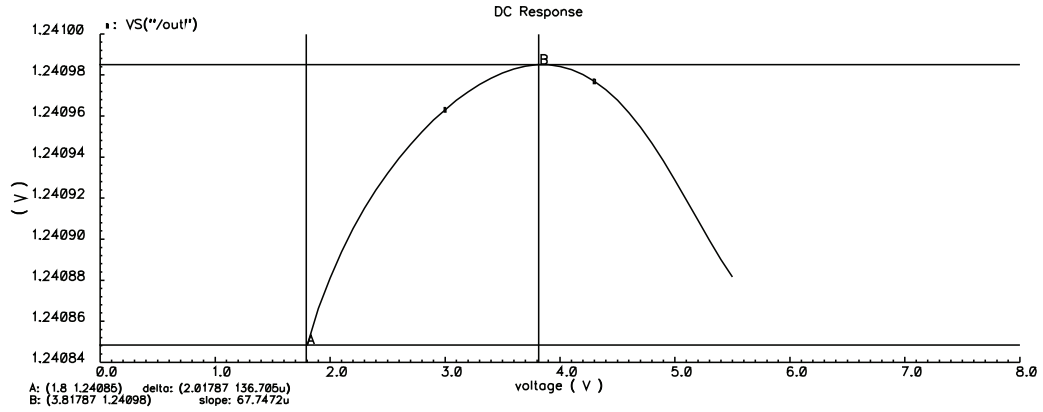

Figure 3.16: line regulation simulation @ 1mA load current.

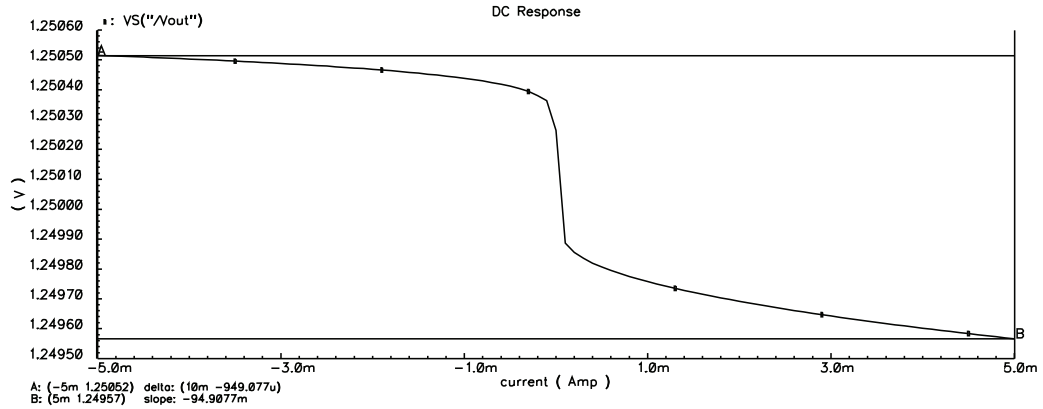

Figure 3.17: load regulation simulation @ 5V supply.

The other two important parameters to define the static behavior of the circuit are the line regulation (Figure 3.16) and load regulation (Figure 3.17), obtained through a DC sweep varying the bandgap input voltage and the output load current respectively. Both these results are usually expressed in ppm by the following equations:

$$\text{Linereg} = \frac{\Delta V_0}{V_0 \cdot \Delta V_{IN}} \cdot 10^6 = 30 \ \frac{ppm}{V} \ \text{ typical} \tag{3.11}$$

$$\text{Loadreg} = \frac{\Delta V_0}{V_0 \cdot \Delta I_L} \cdot 10^6 = 76 \ \frac{ppm}{mA} \ \text{ typical} \tag{3.12}$$

Turning to the dynamic behavior of the regulator, the most important

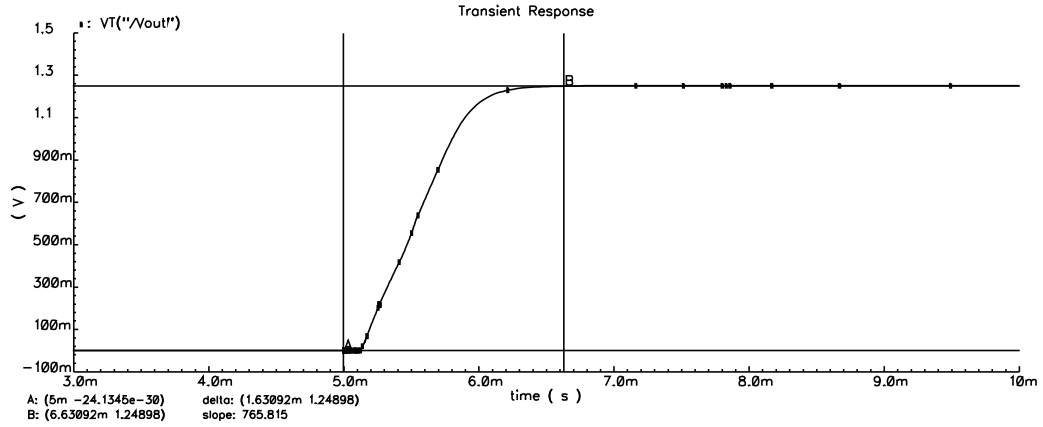

Figure 3.18: turn-on simulation @ 5V supply, 0mA and 1μF load.

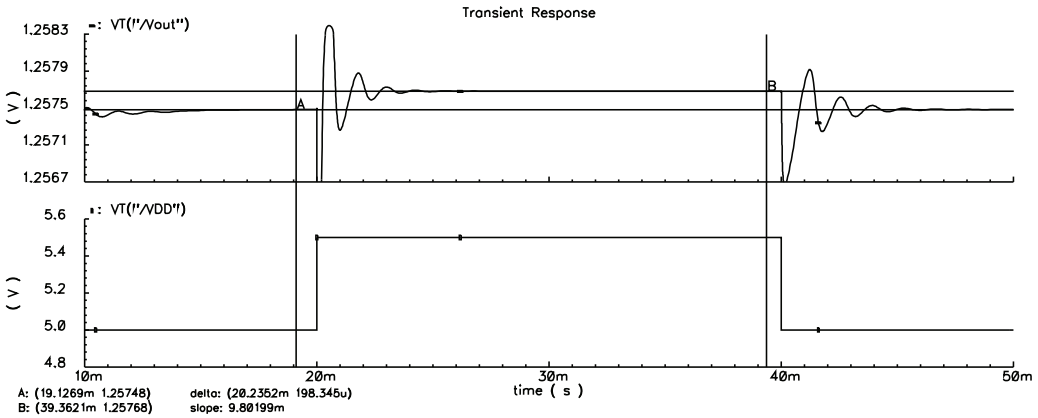

Figure 3.19: line transient simulation @ 1mA, 1μF load.

aspects to be considered are: turn-on time, transient line regulation and transient load regulation. Turn-on time simulation is relized "turning on"the device biasing voltage from ground to V_{DD} potential. Figure 3.18 shows a typical turn-on time of about 1.2 ms for $V_{DD} = 5\,V$, $I_L = 0\,mA$ and $C_L = 1\,\mu F$. The rising time of the supply voltage step used is 0.1 μs. transient line and load simulations are obtained superimposing a square wave to the supply voltage and output current respectively. In Figure 3.19 is shown the line

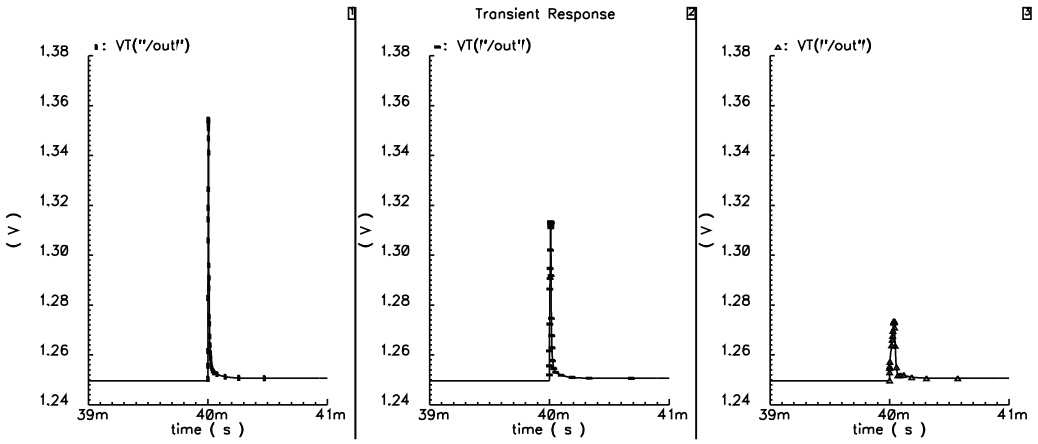

Figure 3.20: load transient simulation @ 5V supply, 0.1μF - 1μF - 10μF loads.

transint simulation. The supply woltage is switched between 5 V and 5.5 V

with 0.1 μs rising and falling edges. It can be seen that the peaks arising from the power supply dynamic switching are about 100 mV on both rising and falling eges. Figure 3.20 shows the load transient simulation instead where the load current is switched from -5 mA to +5 mA. In particular the simulation is reported for three different load capacitance values: 0.1 μF, 1 μF, 10 μF respectively. It can be seen that the peak height decreases almost linearly with the load capacitance value.

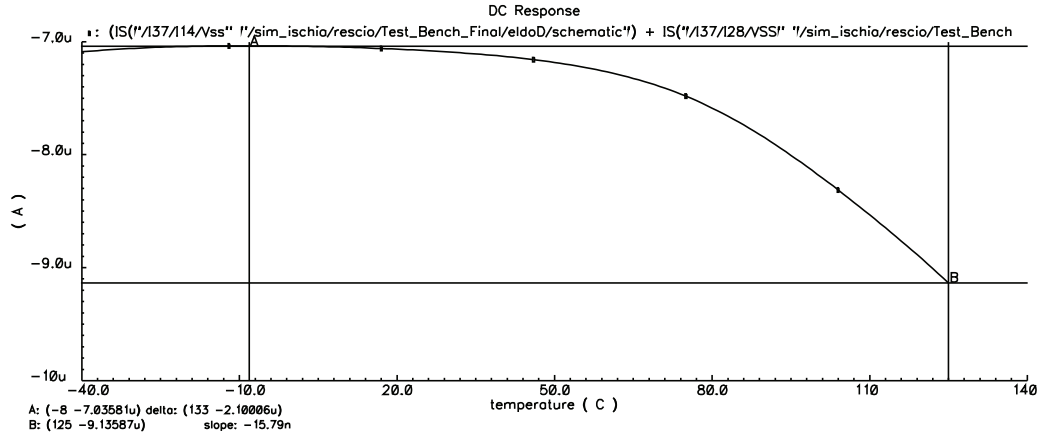

Figure 3.21: current consumption simulation as a function of the device temperature.

In Figure 3.21 is reported the current consumption simulation of the device as a function of the working temperature. The maximum current consumption is reached at the maximum temperature, being the lowest resistance and highest carrier mobility case. Being the current in the power stage driver circuit a scaled replica of the load current, if a current is sourced to the load this term becomes dominant in the current consumption of the device. This is shown in Figure 3.22 where it can be seen that the current consumption increases linearly with the load current. The same thing happens if the device is sinking a current from the load.

Finally, the stability of the circuit has been verified in all the possible situations and in particular, for each of the device versions for any combination

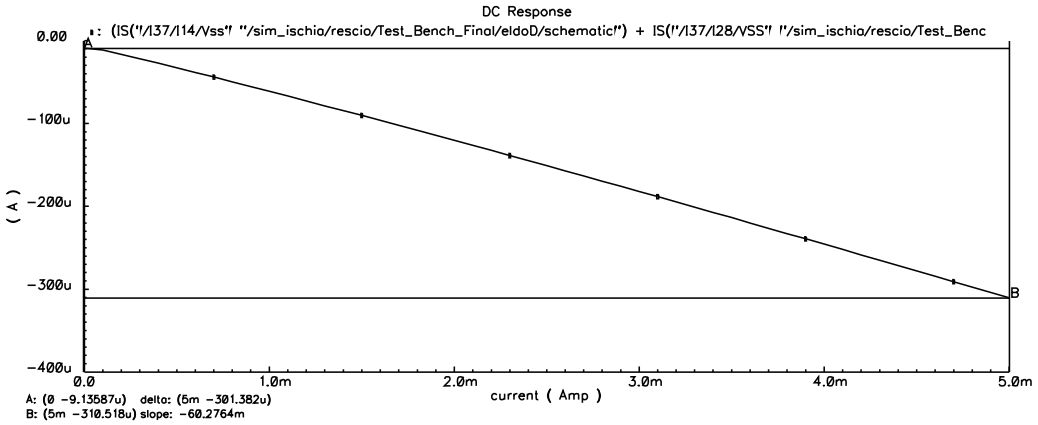

Figure 3.22: current consumption simulation as a function of the load current.

of supply voltage, load current and load capacitance. Despite being shown for the 1.25 V device version and and with a single combination of the veriables mentioned above, all the simulations have been repeated for all device versions and all possible supply voltage, load current and load capacitance combinations too.

Chapter 4

ELECTRICAL MEASUREMENTS

In this chapter is reported a summary of the measured characteristics of both the integrated circuits described. The first to be described is the LDO one, whose electrical characteristics has been widely tested and measured. Then an overlook on the gas sensor interface preliminary measurement results is given on the last part of the chapter. The instrumentation setup used is described for both devices and some making of pictures are added for completeness.

4.1 Voltage Reference Electrical Measurements

A summary of all the electric measurements made on the LDO chip is reported in this section. These measurements include both static and dynamic characterisctics of the regulator, which are compared with the simulation results.

4.1.1 Experimental Setup

In Figure 4.1 are shown two of the boards used in the LDO testing. The one on the left is a multichip board used to perform intensive static and dynamic measures while the one on the right is a single chip mini-board used to test

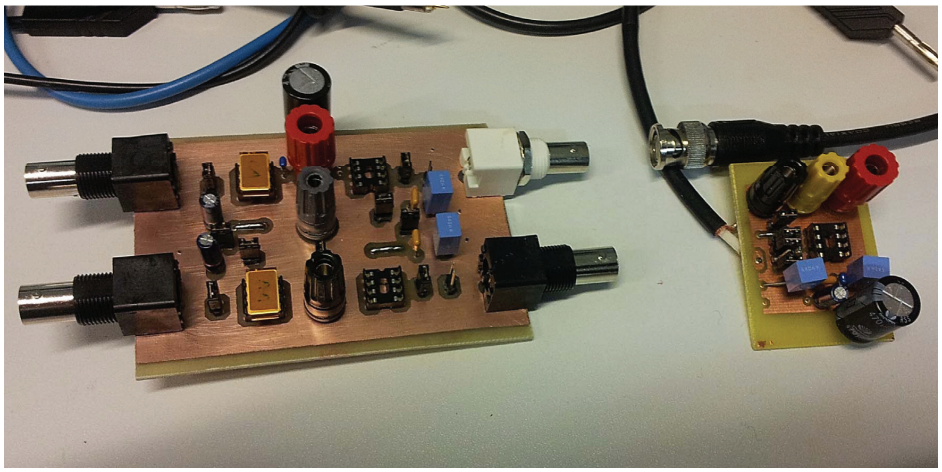

Figure 4.1: Boards used in the LDO measures.

the temperature behavior of the device and can be put inside an oven.

The instrumentation employed in the measure process is composed by:

- Agilent E3631A voltage source
- Kethley 2000 6-digits digital multimeter
- HP3245A universal source
- μ-frequency spectrum analyzer
- WaveRunner204Xi digital oscilloscope
- ThermoStream climate chamber

4.1.2 Temperature Coefficient Measure

In the practical implementation the trimming is performed in a very similar way as the Ocean script does. In particular the steps that has been performed to trim the device are:

1. the output is measured with the precision multimeter at room temperature (25°C);

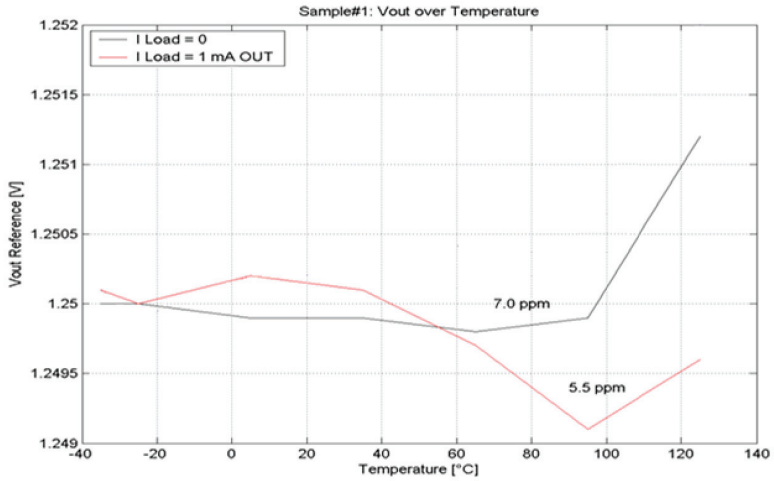

Figure 4.2: Tempco measure.

2. the DUT temperature is raised to 65°C by means of an oven and the output is measured again;

3. the trimming word for R0 (W0) is evaluated using the trimming coefficients reported in Section 3.4.1;

4. the R0 laser fuses are shot. Since the laser fuses switches can only be opened, the ones to be shot are the ones related to a 0 in the trimming word. In particular, since they can be opened only once, the output of the device is measured after each shot to verify that the expected voltage shift has occurred. Proceeding step-by-step avoids to mess up in this process;

5. the output is measured after the trimming of R0 at any working temperature (the device is by all means temperature independant now);

6. the trimming word for R3 (W3) is evaluated;

7. the R3 laser fuses are shot, using the same precautions as for the R0 trimming;

8. the device is now trimmed in both thermal coefficient and output voltage.

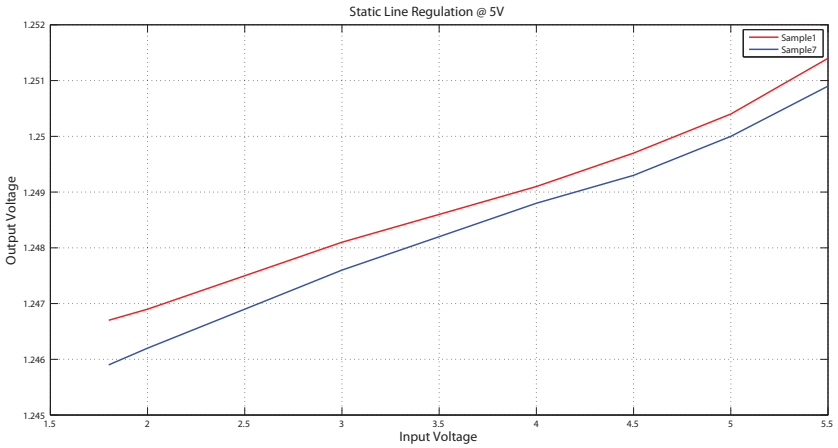

Figure 4.3: static line regulation measure.

The result of a thermal coefficient measure is shown in Figure 4.2 for a trimmed 1.25 V device. This measure has been peerformed with the aid of a ThermoStream climate chamber (thanks to STMicroelectronics for the support), leaving approximately 10 minutes settling time between each temperature step. Moreover, upward and downward temperature sweeps led to the same result.

4.1.3 Line Regulation Measure

The line regulation features, both static and dynamic, have been tested at room temperature with various load configurations. For the static measures (example in Figure 4.3) the input voltage has been changed gradually by tuning the power supply output voltage, while in the dynamic ones (example in Figure 4.4) a square wave with 0.5 V amplitude and 0.1 μs rising and falling edges has been superimposed to the LDO input voltage. Figure 4.3 and 4.4 refers to the 1.25 V device with the typical 1 mA, 1 μF load. No significant changes occur with different load configurations except a reduction

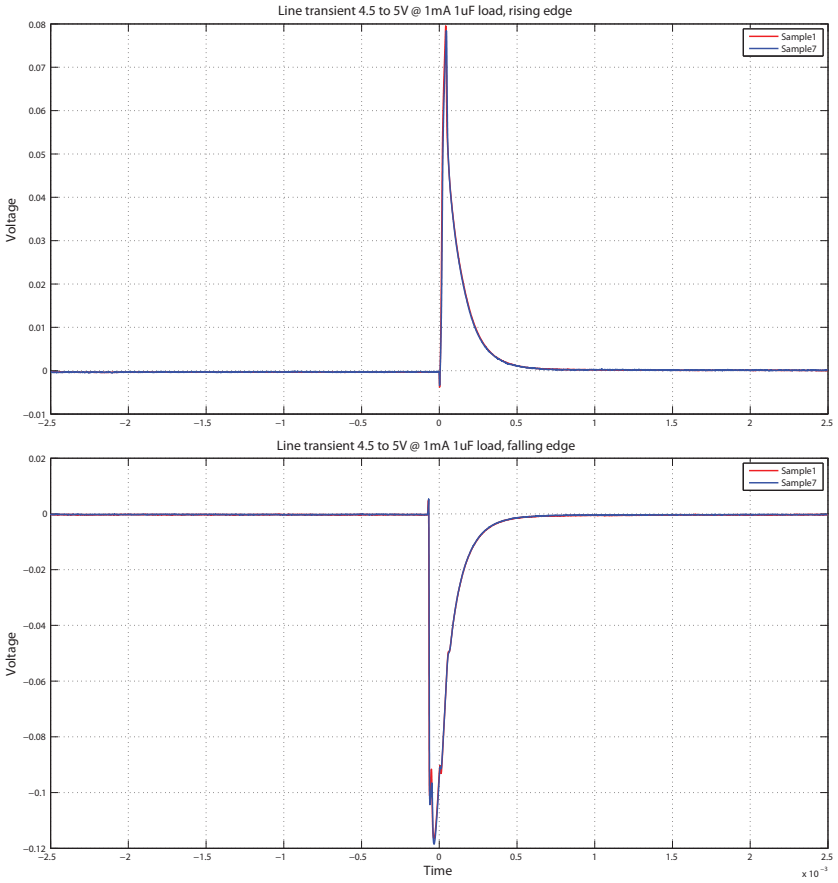

Figure 4.4: dynamic line regulation measure.

in the transient peak heights, which of course decrease linearly with the load capacitance. The results obtained have been very variable, almost certainly due to a not optimal matching between the bandgap amplifier transistors, and ranging from 100 to 1000 $\frac{ppm}{V}$.

4.1.4 Load Regulation Measure

The load regulation features, both static and dynamic, have been tested at room temperature with various supply and load capacitance configurations.

For the static measures (example in Figure 4.5) the load current has been changed gradually by means of a universal source able to source and sink

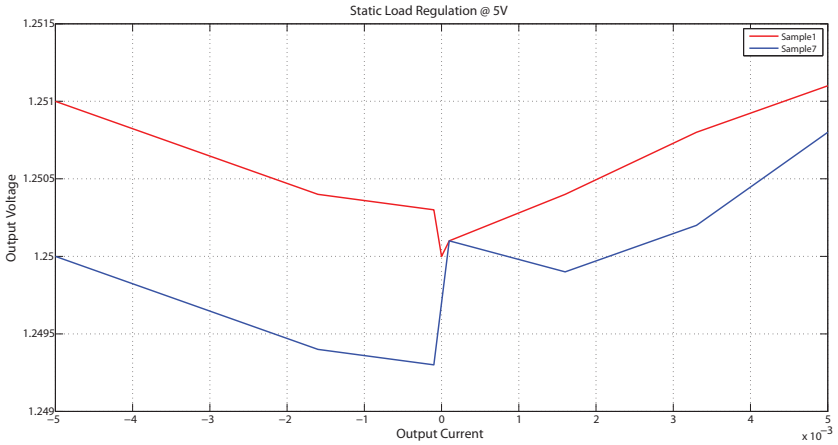

Figure 4.5: static load regulation measure.

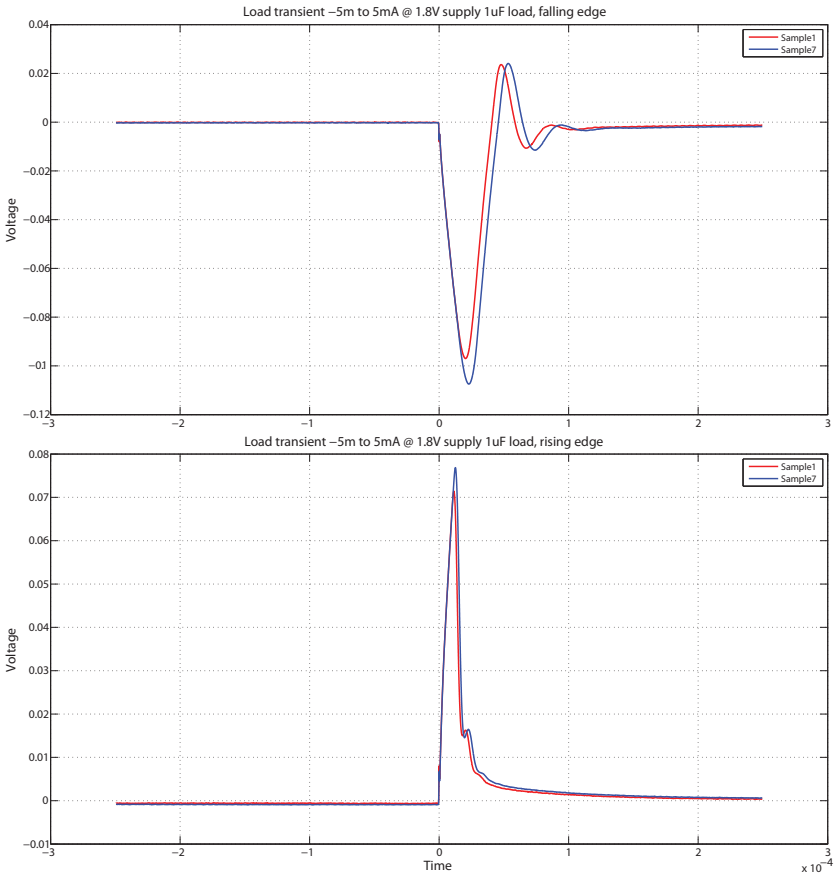

Figure 4.6: dynamic load regulation measure.

currents with high impedence, while in the dynamic ones (example in Figure 4.6) the output of the device has been connected to a 1 kΩ resistor in series with a square wave generator. To generate, at the output of the device, a current square wave of ±5mA, the voltage square wave should have 10 V amplitude and 1.25 V mean value for the 1.25 V device version. No significant changes occur with different supply and load capacitance configurations except a reduction in the transient peak heights, which of course decrease linearly with the load capacitance. The results obtained have always been repetitive and in the range 50-100 $\frac{ppm}{mA}$

4.1.5 Other Measures

First of all the devices stability has been tested in all combination of the input voltage (1.8-5.5 V), load capacitance (0.1-10 μF) and load current (± 5 mA) without denoting any stability issue.

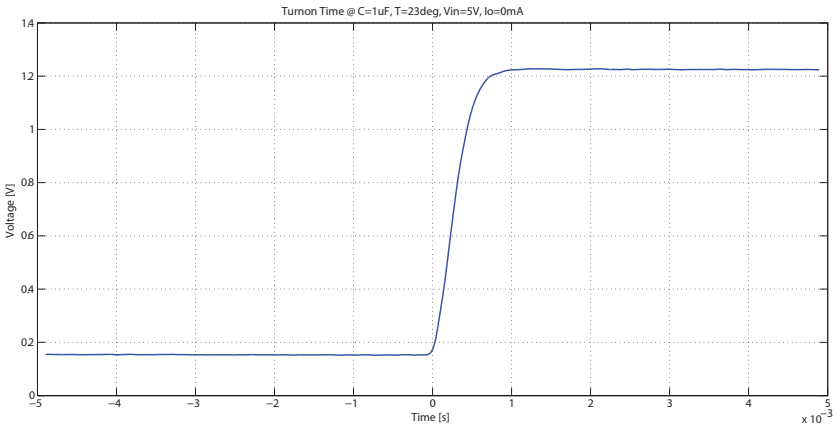

Figure 4.7: turn-on time measure.

A parameter which has been repetitive in all measurements is the turn-on time (example in Figure 4.7 for the 1.25 V device), whose value is approximately $1\frac{ms}{V}$ for a load capacitance of 1 μF

Another very repetitive measured parameter has been the device current consumption (example in Figure 4.8 for the 1.25 V device) whose value, at

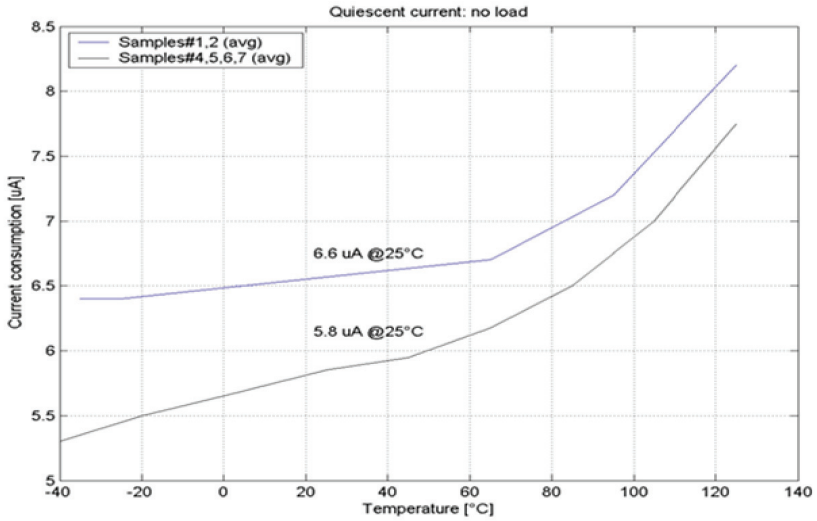

Figure 4.8: current consumption measure.

room temperature and no load current, has always been below 7 μA.

Finally, the LDO RMS noise has been tested with a μ-frequency spectrum analyzer and resulted in the 10 μV range when integrated between 0.1 Hz and 10 Hz.

4.2 Interface Circuit Electrical Measurements

A summary of all the electric measurements made on the sensor interface is reported in this section. Although the sensor still hasto be produced, the interface linearity has been tested with prcision metal resistances. Heating system measures, depending on the heater-thermometer relationship to close the analog loop could not been performed. The photograph of the chip is shown in Figure 4.9

4.2.1 Linearity Measurements

The result for the linearity measurements of the sensor interface is shown in Figure 4.10. For the linearity extimation, 1% precision metal resistances has

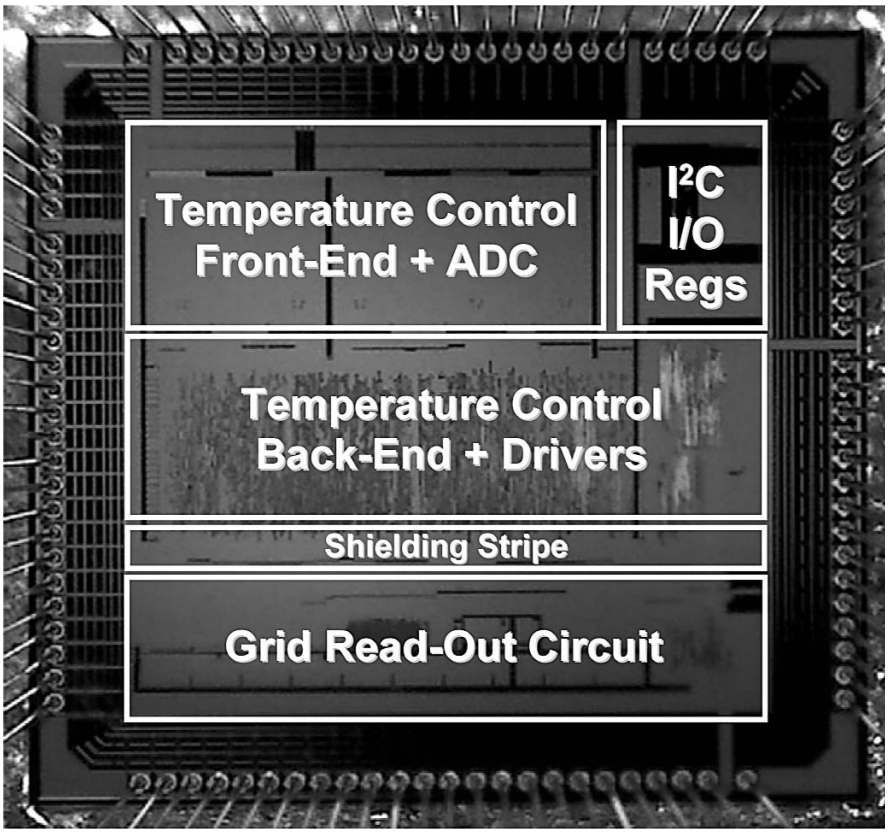

Figure 4.9: micrograph of the chip.

been used. since this 1% precision is not satisfying for the required linearity, every resistance has been measured by means of a precision multimeter. Even with process an error is introduced in the resistance value definition for resistances greater than 100 kΩ, due to a change of scale in the instrument, which is in the order of 0.1%-0.2% and uncorreletad between any resistance value in the linearity curve. The Matlab polyfit function used to extract the linearity curve seems to suffer a bit from this source of error. For this reason a more accurate measurement process is currently being implemented which will give better results. The linearity result for the first decades in which the test resistance value could be measured whith absolute precision is shown in Figure 4.11.

Finally, the current consumption observed is (almost) equal to the simu-

lated one.

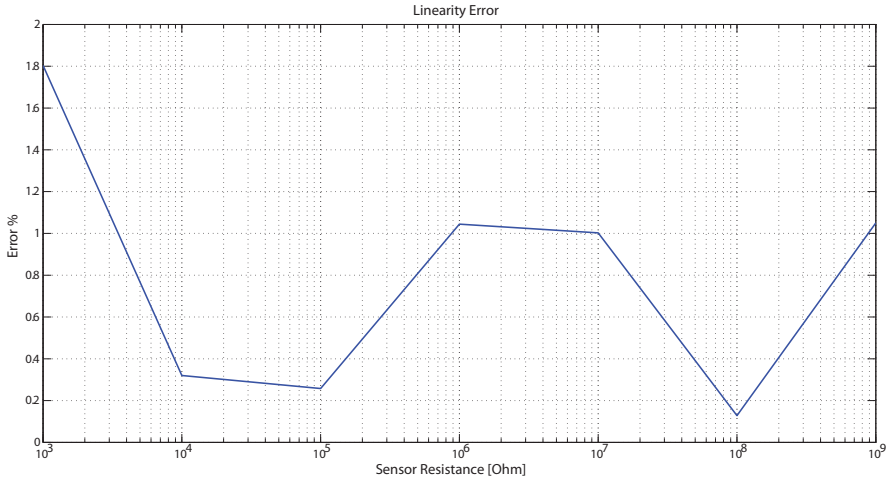

Figure 4.10: interface linearity.

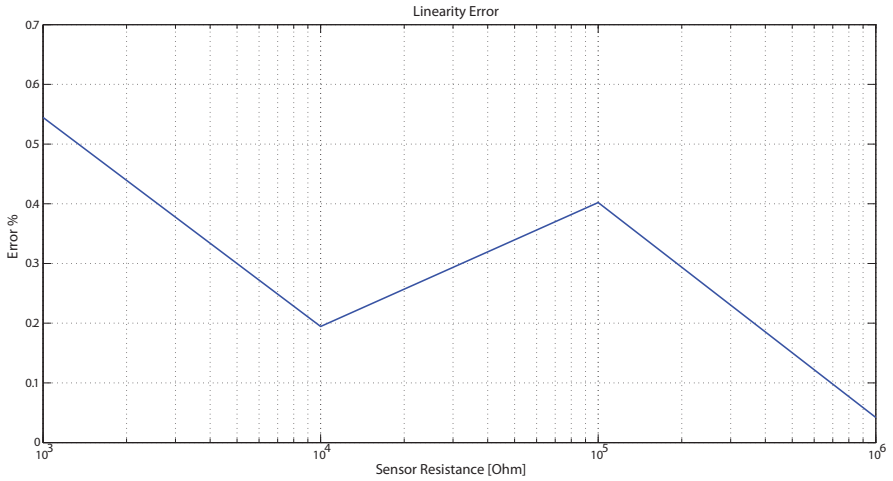

Figure 4.11: interface linearity for the first decades.

Appendix A

AUXILIARY CODE

A.1 Verilog Code Listings

In this section the Verilog code blocks referred throughout the whole thesis are reported for quick reference.

Rough Counter

```
module COUNTER_3bit (CK, ENABLE_COUNT, REACHED, RESET);
    output REACHED;
    input CK;
    input RESET;
    input ENABLE_COUNT;
    reg [2:0] CNT;
    reg REACHED;

always @(posedge CK or posedge RESET) begin
    if (RESET) begin
        CNT[2:0]=0;
        REACHED=0;
    end
    else if (ENABLE_COUNT) begin
        CNT=CNT+1;
        if (CNT[2:0]==7)
            REACHED1=1;
    end
end
endmodule
```

Rough Multiplexer

```
module MUX_3bit (UPDATE_N, RESET, x100, REACH_OSC, REACH_REF);
    output x100;
    input UPDATE_N;
    input RESET;
    input REACH_OSC;
    input REACH_REF;
    reg x100;

always @(negedge UPDATE_N or posedge RESET) begin
    if (RESET) begin
        x100=0;
    end
    else begin
        if(REACH_REF==1) begin
            if (REACH_OSC==1)
                x100=0;
            else
                x100=1;
        end
        else
            x100=0;
    end
end
endmodule
```

Fine Counter

```
module COUNTER_18bit (CK, ENABLE_COUNT, REACHED, RESET, OUT);
    output [18:0] OUT;
    output REACHED;
    input CK;
    input RESET;
    input ENABLE_COUNT;
    reg [18:0] OUT;
    reg REACHED;

always @(posedge CK or posedge RESET) begin
    if (RESET)
    begin
        OUT[18:0]=0;
        REACHED=0;
    end
```

```
    else if (ENABLE_COUNT) begin
        OUT=OUT+1;
        if (OUT[18:0]==256)
            REACHED=1;
    end
end
endmodule
```

Fine Multiplexer

```
module MUX_18bit (UPDATE_N, REF_DATA, OSC_DATA, RESET, DATA_OUT, WHICH);
    output [18:0] DATA_OUT;
    output WHICH;
    input [18:0] REF_DATA;
    input [18:0] OSC_DATA;
    input UPDATE_N;
    input RESET;
    reg [18:0] DATA_OUT;
    reg WHICH;

always @(negedge UPDATE_N or posedge RESET) begin
    if (RESET) begin
        DATA_OUT[18:0]=0;
        WHICH=0;
    end
    else begin
        if (REF_DATA[18:0]>OSC_DATA[18:0]) begin
            DATA_OUT[18:0]=REF_DATA[18:0];
            WHICH=1;
        end
        else begin
         DATA_OUT[18:0]=OSC_DATA[18:0];
         WHICH=0;
        end
    end
end
endmodule
```

Measure Multiplexer

```
module Measure_Logic (AKNOWLEDGE, ENABLE, INPUT_WORD, OUTPUT_CTRL, RES_DIG);
    output RES_DIG;
    output [39:0] OUTPUT_CTRL;
```

```
    input [8:0] INPUT_WORD;
    input ENABLE;
    input AKNOWLEDGE;
    reg [39:0] OUTPUT_CTRL;
    reg RES_DIG;

always @(posedge AKNOWLEDGE) begin
    if (ENABLE==0)
        RES_DIG=1;
    else begin
        RES_DIG=0;
        case (INPUT_WORD)
            1:   OUTPUT_CTRL=40'b0000000000000000000100000000000000000010;
            2:   OUTPUT_CTRL=40'b0000000000000000000100000000000000000100;
            3:   OUTPUT_CTRL=40'b0000000000000000000100000000000000001000;
            4:   OUTPUT_CTRL=40'b0000000000000000000100000000000000010000;
            5:   OUTPUT_CTRL=40'b0000000000000000000100000000000000100000;
            6:   OUTPUT_CTRL=40'b0000000000000000000100000000000001000000;
            7:   OUTPUT_CTRL=40'b0000000000000000000100000000000010000000;
            8:   OUTPUT_CTRL=40'b0000000000000000000100000000000100000000;
            9:   OUTPUT_CTRL=40'b0000000000000000000100000000001000000000;
            10:  OUTPUT_CTRL=40'b0000000000000000000100000000010000000000;
            11:  OUTPUT_CTRL=40'b0000000000000000000100000000100000000000;
            12:  OUTPUT_CTRL=40'b0000000000000000000100000001000000000000;
            13:  OUTPUT_CTRL=40'b0000000000000000000100000010000000000000;
            14:  OUTPUT_CTRL=40'b0000000000000000000100000100000000000000;
            15:  OUTPUT_CTRL=40'b0000000000000000000100001000000000000000;
            16:  OUTPUT_CTRL=40'b0000000000000000000100010000000000000000;
            17:  OUTPUT_CTRL=40'b0000000000000000000100100000000000000000;
            18:  OUTPUT_CTRL=40'b0000000000000000000101000000000000000000;
            19:  OUTPUT_CTRL=40'b0000000000000000000110000000000000000000;
            .
            .
            .
            362: OUTPUT_CTRL=40'b1000000000000000000000000000000000000001;
            363: OUTPUT_CTRL=40'b1000000000000000000000000000000000000010;
            364: OUTPUT_CTRL=40'b1000000000000000000000000000000000000100;
            365: OUTPUT_CTRL=40'b1000000000000000000000000000000000001000;
            366: OUTPUT_CTRL=40'b1000000000000000000000000000000000010000;
            367: OUTPUT_CTRL=40'b1000000000000000000000000000000000100000;
            368: OUTPUT_CTRL=40'b1000000000000000000000000000000001000000;
            369: OUTPUT_CTRL=40'b1000000000000000000000000000000010000000;
            370: OUTPUT_CTRL=40'b1000000000000000000000000000000100000000;
```

```
            371: OUTPUT_CTRL=40'b1000000000000000000000000001000000000;
            372: OUTPUT_CTRL=40'b1000000000000000000000000010000000000;
            373: OUTPUT_CTRL=40'b1000000000000000000000000100000000000;
            374: OUTPUT_CTRL=40'b1000000000000000000000001000000000000;
            375: OUTPUT_CTRL=40'b1000000000000000000000010000000000000;
            376: OUTPUT_CTRL=40'b1000000000000000000000100000000000000;
            377: OUTPUT_CTRL=40'b1000000000000000000001000000000000000;
            378: OUTPUT_CTRL=40'b1000000000000000000010000000000000000;
            379: OUTPUT_CTRL=40'b1000000000000000000100000000000000000;
            380: OUTPUT_CTRL=40'b1000000000000000001000000000000000000;
        default: OUTPUT_CTRL=40'b0000000000000000000000000000000000000;
        endcase
    end
end
endmodule
```

Heater Time Base

```
module Time_base2 (CK, out, reset, res_reg, res_integ, en_fb);
    input CK;
    input reset;
    output [0:8] out;
    output [0:31] res_reg;
    output res_integ;
    output en_fb;
    reg [0:31] res_reg;
    reg [0:8] out;
    reg res_integ;
    reg en_fb;

always @(posedge CK or posedge reset) begin
    if (reset) begin
        out=0;
        res_reg=32'b11111111111111111111111111111111;
        res_integ=1;
    end
    else begin
        if (out==0) begin
            res_integ=0;
            res_reg[0]=0;
        end
        if (out==15)
            res_reg[1]=0;
```

```
        .
        .
        .
        else if (out==495)
            res_reg[31]=0;

        out=out+1;
    end
end

always @(posedge reset or negedge CK) begin
    if (reset)
        en_fb=0;
    else if (out==2)
        en_fb=1;
end
endmodule
```

Heater Decimation Filter

```
module Logica_Heater (inc_input, dig_out, EOC, reset, timebase, res_reg, CK);
    input CK;
    input reset;
    input inc_input;
    input [0:31] res_reg;
    input [0:8] timebase;
    output [8:0] dig_out;
    output EOC;
    reg [0:8] reg0;
    .
    .
    .
    reg [0:8] reg31;
    reg EOC;
    reg [8:0] dig_out;

always @(posedge CK or posedge reset) begin
    if (reset) begin
        EOC=0;
        dig_out=0;
        reg0=0;
        .
        .
```

```
        .
        reg31=0;
    end
    else begin
        if (timebase==0)
            reg31=0;
        else if (timebase==15)
            dig_out=reg0;

        else if (timebase==16)
            reg0=0;

        else if (timebase==31)
            dig_out=reg1;
        .
        .
        .
        else if (timebase==496)
            reg30=0;
        else if (timebase==511) begin
            dig_out=reg31;
            EOC=1;
        end

        if (res_reg[0]==0) begin
            if (inc_input)
                reg0=reg0+1;
            else
                reg0=reg0;
        end
        else
            reg0=0;
        .
        .
        .
        if (res_reg[31]==0) begin
            if (inc_input)
                reg31=reg31+1;
            else
                reg31=reg31;
        end
        else
            reg31=0;
```

```
    end
end
endmodule
```

A.2 Matlab Code Listings

In this section the Matlab scripts referred throughout the whole thesis are reported for quick reference.

Interface Linearity Calculation

```
format long;
load /home/conso/tm.txt
x=A(:,1); %resistances values
y=A(:,2); %oscillator period
yn=y./x
pol=polyfit(x,y,1);
m=pol(1);
q=pol(2);
ris_poly=(m*x+q);
err=(y-ris_poly);
err_rel=max(abs(100*err))
poln=polyfit(x,yn,1);
mn=poln(1);
qn=poln(2);
ris_polyn=(mn*x+qn).*x./y;
errn=y-ris_polyn;
err_reln=max(abs(100*errn))
err_rel_plot=errn*100;

figure(1)
semilogx(x,err_rel_plot,'LineWidth',1.5)
grid on
title('Linearity Error','fontsize',14)
xlabel('Sensor Resistance [Ohm]','fontsize',14);
ylabel('Error %','fontsize',14);

figure(2)
plot(x,y,'b',x,ris_poly,'r','LineWidth',1.5)
title('Linearity Error','fontsize',14)
xlabel('Sensor Resistance [Ohm]','fontsize',14);
```

```
ylabel('Oscillator Frequency [Hz],'fontsize',14);
```

Heater ripple calculation

```
load /home/conso/gas.txt
l=length(gas);
t=(1:1:l)*10^-5;
maxpeak=max(gas(500:l));
minpeak=min(gas(500:l));
deltaT=maxpeak-minpeak;
disp('temperature ripple =')
disp(deltaT)
maxvector=maxpeak+zeros(l,1);
minvector=minpeak+zeros(l,1);
disp('average temperature =')
disp(mean(gas(500:l)))

figure(1)
plot(t,gas,'r',t,maxvector,'b',t,minvector,'b','LineWidth',1.5)
grid on
title('Temperature Simulation','fontsize',14)
xlabel('Time [s]','fontsize',14);
ylabel('Temperature [°C]','fontsize',14);
```

LDO Trimming Coefficients Refining

```
format long
load /home/conso/ocean_result.txt
r0 = ocean_result(:,4);
dv = ocean_result(:,2);
r3 = ocean_result(:,7);
pt = ocean_result(:,6);

fit1 = polyfit(dv,r0,5);
fit2 = polyfit(pt,r3,5);

m0 = fit1(1);
m01 = fit1(2);
m02 = fit1(3);
m03 = fit1(4);
m04 = fit1(5);
q0 = fit1(6);
```

```
m3 = fit2(1);
m31 = fit2(2);
m32 = fit2(3);
m33 = fit2(4);
m34 = fit2(5);
q3 = fit2(6);

r0new=m0*(dv(1)^5)+m01*(dv(1)^4)+m02*(dv(1)^3)+m03*(dv(1)^2)+m04*dv(1)+q0
r3new=m3*(pt(1)^5)+m31*(pt(1)^4)+m32*(pt(1)^3)+m33*(pt(1)^2)+m34*pt(1)+q3
```

A.3 Ocean Script

In this section the Ocean script used to automatically run through the trimming simulations is reported.

Ttrimming Simulation Script

```
load(".cdsinit_ocean")
ocnWaveformTool( 'awd )
simulator( 'eldoD )
design("/sim_panarea/conso/Sim/LDO_trimming_bench/eldoD/schematic/netlist/netlist")
resultsDir("/sim_panarea/conso/Sim/LDO_trimming_bench/eldoD/schematic" )
analysis('dc ?dcFileName "../netlist/LDO_trimming_bench.iic"  ?sweep "Temperature"
        ?from "125"    ?to "-40"  ?by "-10"  )
desVar(      "dec_r3" 0)
desVar(      "dec_r0" 0)
desVar(      "VDD" 5    )
desVar(      "CAP" 1u    )
envOption('includeEldo  "models")
option(    'TEMPDC  "27.0"
    'geaIntegrationMethod  "GEAR"
    'OPTYP  "2"
    'NOBOUND_PHASE  t
    'CAPTAB  t
    'ITOL  "1e-6"
    'geaDefaultEPS  "1.0e-8"
    'TUNING  "VHIGH")
save( 'alli )
temp( 27.0 )
file_out = outfile("./trimming.txt" "w")
fprintf(file_out "%Run\tdvout\t\tppm0\tr_0\tppm\tvout_25pr\tr_3\tvout_25ps\tppm_fin\
    tout_err_mill\tspec\n")

nspec=0
oneshot=0
```

```
qoneshot=0

for(current_cont 1 400
    file_port = outfile("/sim_panarea/conso/Sim/LDO_trimming_bench/eldoD/schematic/
        netlist/stat_commands" "w")
    fprintf(file_port ".mc 400 all irun=%d\n" current_cont)
    close(file_port)

    run()

    dvout=ymax((value(VS("/out") 25) - value(VS("/out") 65)))
    ppm0 = ymax(((ymax(VS("/out")) - ymin(VS("/out"))) / 1.25 / 165) * 1000000)
    r_0=round((4.866344651965128e11 * dvout * dvout * dvout * dvout * dvout) +
    (0.205099673619486e11 * dvout * dvout * dvout * dvout) +
    (0.002784568013197e11 * dvout * dvout * dvout) +
    (0.000016499405541e11 * dvout * dvout) - (0.000000026079362e11 * dvout) -
    0.000000000000217e11)

    if((r_0<=0) then r_0=0)
    desVar("dec_r0" r_0)

    run()

    ppm = ymax(((ymax(VS("/out")) - ymin(VS("/out"))) / 1.25 / 165) * 1000000
    i=1
    j=0
    while((((ppm >7) || (ppm<-7)) && (i<6) && ((r_0>0) || (r_0<=63)))
        if((j==0) then
            r_0=r_0+1
            desVar("dec_r0" r_0)
            run()
            ppm_1 = (ymax(VS("/out")) - ymin(VS("/out"))) / 1.25 / 165 * 1000000
            i=i+1
            if((ppm_1<ppm) then    j=0
            else j=1)
            ppm = (ymax(VS("/out")) - ymin(VS("/out"))) / 1.25 / 165 * 1000000
        else
            r_0=r_0-1
            desVar("dec_r0" r_0)
            run()
            ppm_1 = (ymax(VS("/out")) - ymin(VS("/out"))) / 1.25 / 165 * 1000000
            i=i+1
            if((ppm_1<ppm) then    j=1
            else j=0)
        )
        ppm = (ymax(VS("/out")) - ymin(VS("/out"))) / 1.25 / 165 * 1000000
    )

    vout_25pr = ymax(value(VS("/out") 25))
```

```
r_3=round(0 - (0.091586124959589e8 * vout_25pr * vout_25pr * vout_25pr *
vout_25pr * vout_25pr) + (0.547169846487039e8 * vout_25pr * vout_25pr *
vout_25pr * vout_25pr) - (1.307317499983437e8 * vout_25pr * vout_25pr *
vout_25pr) + (1.561414766894295e8 * vout_25pr * vout_25pr) -
(0.932267168199967e8 * vout_25pr) + 0.222612657825488e8)

if((r_3<=0) then r_3=0)
desVar("dec_r3" r_3)

run()

ppm_fin = (ymax(VS("/out")) - ymin(VS("/out"))) / 1.25 / 165 * 1000000
vout_25ps = ymax(value(VS("/out") 25))
i=1
if((vout_25ps>1.25) then
    while(((vout_25ps>1.26) && (i<3) && ((r_3>0) || (r_3<=255)))
        r_3=r_3-5
        desVar("dec_r3" r_3)
        run()
        i=i+1
        ppm_fin = (ymax(VS("/out")) - ymin(VS("/out")) / 1.25 / 165) * 1000000
        vout_25ps = ymax(value(VS("/out") 25))
    )
else
    while(((vout_25ps<1.24) && (i<6) && ((r_3>0) || (r_3<=255)))
        r_3=r_3+5
        desVar("dec_r3" r_3)
        run()
        i=i+1
        ppm_fin = (ymax(VS("/out")) - ymin(VS("/out")) / 1.25 / 165) * 1000000
        vout_25ps = ymax(value(VS("/out") 25))
    )
)

i=1
while((((vout_25ps >1.2506) || (vout_25ps<1.2494)) && (i<8) && ((r_3>0) ||
    (r_3<=255)))
    if((vout_25ps>1.250625) then r_3=r_3-1)
    if((vout_25ps<1.249375) then r_3=r_3+1)
    desVar("dec_r3" r_3)
    run()
    i=i+1
    ppm_fin = (ymax(VS("/out")) - ymin(VS("/out"))) / 1.25 / 165 * 1000000
    vout_25ps = ymax(value(VS("/out") 25))
)

if(((vout_25ps >1.25125) || (vout_25ps<1.24875) || (ppm_fin >10) ||
    (ppm_fin<-10)) then
    spec="*"
```

```
        nspec=nspec+1
    else spec="")
    out_error_mill = abs(((vout_25ps - 1.25)/1.25)*1000)
    fprintf(file_out "%d\t%f\t%4.2f\t%d\t%4.2f\t%f\t%d\t%f\t%4.2f\t%4.2f\t\t%s\n"
        current_cont dvout ppm0 r_0 ppm vout_25pr r_3 vout_25ps ppm_fin
        out_error_mill spec)
    drain(file_out)
    desVar("dec_r0" 0)
    desVar("dec_r3" 0)
)
fprintf(file_out "Out of spec = %d\n" nspec)
close(file_out)
```

Conclusions

In this work the full design and characterization of two different circuits for gas-sensor interfacing have been reported. The research activity has been carried out since 2009 in the Italian Government PRIN project IT-20085AJSEB, named "Interface and control circuits for high-selectivity gas sensors operated with temperature pattern". Both circuits described have been entirely developed at the Sensor and MicroSystem laboratory of the University of Pavia. After introducing the reader to gas-sensing architectures, with particular care in the description of modern micromachined based Tin Oxide sensors with embedded heater and thermometer in the first chapter, the interface solution has been iuntroduced. This interface is able to discriminate resistance values with a precision bettere than 1% over 6 decades without needing any calibration, thus being cost efficient. Since a minimum throughput of 2.5 Hz is not acceptable a speed enhancing feature has also been implemented. The second developed circuit is a general porpouse LDO which is able to perform the biasing of the interface but that can also be considered as a stand alone cirtcuit with a competitive performace.

Chemical measurements by means of the sensor interface are currently in progress.

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