UNIVERSITÀ DEGLI STUDI DI PAVIA

DIPARTIMENTO DI INGEGNERIA INDUSTRIALE E DELL'INFORMAZIONE

DOTTORATO DI RICERCA IN MICROELETTRONICA
XXIX CICLO

HIGH DENSITY ANALOG CIRCUITS FOR SEMICONDUCTOR PIXEL DETECTORS

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Anno Accademico 2015/2016

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High Density Analog Circuits for Semiconductor Pixel Detectors

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Abstract

An upgrade of the physics experiments, also called "phase 2 upgrade", is in progress at the LHC (Large Hadron Collider), the particle collider installed at CERN in Geneva, and will become operational in 2022-2023. The experiment upgrade will follow the upgrade of the accelerator itself, which will change its name to HL-LHC (High Luminosity LHC). CERN (Centre Européen pour la Recherche Nucléaire) is leading an international collaboration, called RD53, whose aim is to design a new generation of hybrid pixel readout chips to enable the ATLAS and CMS phase 2 upgrade. The submission of the first demonstrator chip, called RD53A, is foreseen for April 2017. The chip will be designed, using a 65 nm CMOS technology for the first time in the high energy physics (HEP) community, to be compliant with extremely high particle rates and radiation levels. In particular, the readout circuit under development will need to withstand extremely high total ionizing doses, in the order of 1 Grad in 10 years of operation in the experiment. With respect to the pixel detectors currently employed in the LHC experiments, the new chip will feature a significantly finer granularity, with a pixel pitch of 50 μm in both X and Y directions.

A number of functional blocks or IP (Intellectual Property) blocks, are required for a complete ASIC system. The IP blocks have to be designed and optimized taking into account the very harsh radiation environment and the resulting effects on individual transistors and more complex circuits. In this work, the development of two IP blocks is presented and discussed. In particular, a rad-hard bandgap voltage reference and a differential IO link have been designed and characterized. They will be included in the RD53A demonstrator chip, in particular, in the monitoring and IO sections.

The rad-hard bandgap reference has been designed in two different versions: the first one has been designed using the same architecture (i.e. a bandgap reference based on a current mode approach) for three circuits. Each circuit exploits a different active device (i.e. bipolar, diode or MOS in sub-threshold region) to generate a temperature dependent voltage reference. The purpose of this first version was to understand which solution is the best in term of radiation hardness. The power supply is 1.2 V and the

layout has the same area, 260 μm x 120 μm, for the three different circuits. In this first prototype, the best choice in terms of temperature insensitivity is provided by the circuit using the bipolar transistor as the voltage reference device. Indeed the temperature coefficient is 76 ppm/K with an output voltage of 700 mV at room temperature. In terms of radiation hardness, instead, the best solution is the one based on the MOSFET transistor in weak inversion region. Indeed, the maximum voltage shift after irradiation with a total dose of 225 Mrad (SiO_2) is less than 8 mV, to be compared to the 40 mV shift which was detected in the case both of the circuit based on bipolar transistors and of the one based on diodes. A second version of the bandgap has then been submitted and characterized, based on MOS transistors in weak inversion. In this second prototype, new features have been incorporated. In particular, the biasing current has been increased by a factor of about 4, in order to mitigate the TID effect. Also a trimmable resistor has been included in order to minimize mismatch and process variation induced effects. The output voltage at room temperature is close to 400 mV and the temperature coefficient in a range between -40 °C and -110 °C is 18 ppm/K (after trimming). The second prototype has also been irradiated with 10 keV X-rays at CERN, with a total ionizing dose close to 500 Mrad. The maximum shift of the output voltage is 16%.

The second IP developed in this work is a differential IO link again use in to severe radiation environment. Differential signaling is an almost mandatory choice to remove or minimize the effects of common mode disturbances in the harsh environment of the HL-LHC experiments. The transmitter and receiver, both biased at 1.2 V, comply with the SLVS JDEC specification: output common mode of the driver is 200 mV and the output differential mode is $\pm$200 mV on a 100 Ω termination resistance. The transmitter has been characterized with a microstrip transmission line on a test PCB with a length close to 5.5 cm. The maximum data rate is 1.2 Gbps with a jitter of 9.8 ps. After exposure to a total ionizing dose of 550 Mrad, the differential IO link did not show any significant performance degradation.

INTRODUCTION

The research activity carried out in this work is relevant to the design and characterization of high density analog circuits for semiconductor pixel detectors. This activity has been developed in the framework of the CERN RD53 collaboration, whose aim is the design of the next generation of hybrid pixel readout chips for the ATLAS and CMS phase 2 pixel upgrades. The ultimate goal of this three year project is the development of an innovative chip for pixel detectors, using a 65nm CMOS technology for the first time in the High Energy Physics (HEP) community. The detectors are to be used in experiments with extremely high particle rates and radiation levels at the future high luminosity colliders, in particular at the so called high luminosity LHC (Large Hadron Collider), an upgraded version of the present LHC accelerator. In this thesis, the design, simulation, characterization and also irradiation results of two Intellectual Property (IP) blocks are described: a rad hard bandgap voltage reference and an SLVS link composed of a driver and a receiver.

The first chapter begins with a brief introduction of the requirements for the upgrade (phase 2) of HL-LHC. Then it describes the general requirements for the final chip demonstrator of the RD53 collaboration, called RD53A, in which the IPs described in this thesis will be integrated.

The second chapter is devoted to the design of a rad-hard bandgap voltage reference. Two different versions have been developed: the first one has been designed using the same architecture (i.e. a bandgap reference based on a current mode approach) for three circuits. Each circuit exploits a different active device (i.e. bipolar transistors, diode or MOS in sub-threshold region) generating the voltage reference as a function of the temperature. The purpose of this first version was to understand which solution is the best in terms of radiation hardness. The second version, based only on MOS in sub-threshold region, is an improved version of the one designed in the first run. This new version includes the possibility to trim a component in order

to mitigate the variations introduced by process, mismatch and radiation effects.

Chapter three discusses the design and characterization of an SLVS driver and receiver system, with a maximum data-rate up to 1.2 Gbit/s. These devices, which comply with the JEDEC specifications, will be used in the RD53 demonstrator chip.

CHAPTER 1

ASIC REQUIREMENTS FOR THE CMS PIXEL DETECTOR AT THE HL-LHC

Contents

This chapter is dedicated to a general overview of the CMS experiment at the LHC (Large Hadron Collider), describing the proposed timeline and upgrades for the pixel detectors. The second part is dedicated to the activity carried out by the RD53 collaboration, which aims to the design of the next generation of ASIC pixel detectors for HL-LHC.

1.1 The CMS experiment at the LHC

The Compact Muon Solenoid (CMS), shown in figure 1.1, is one of the two general purpose detectors for particle physics experiments installed at the LHC.

1.1.1 Large Hadron Collider

The Large Hadron Collider is the largest particle collider in the world, installed at CERN, where CMS is one of the four main experiments. The

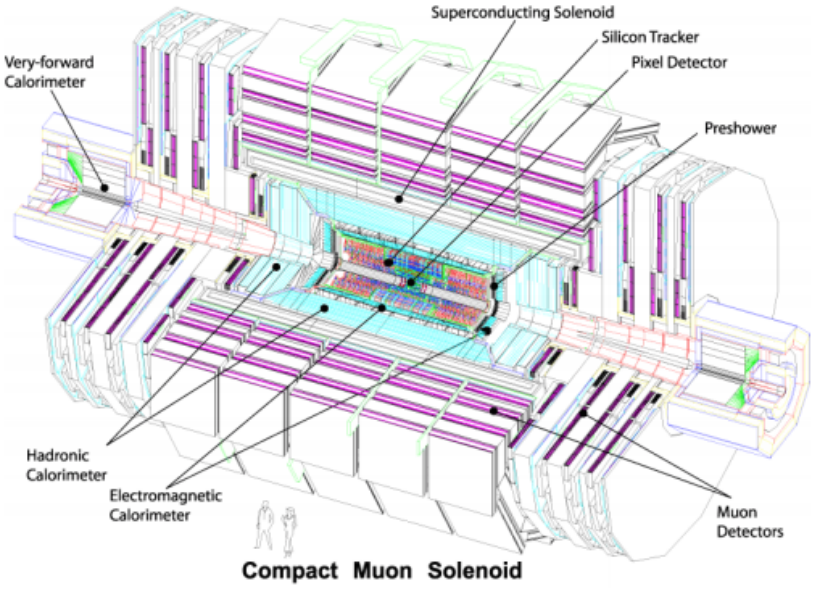


Figure 1.1: the CMS detector.

collider has been designed in order to work with a nominal centre-of-mass energy of 4 TeV and a nominal luminosity of 10^{34} cm^{2}s^{-1} at 40 MHz bunch crossing rate.

In 2013-2014, the LHC suffered the first planned Long Shut-down, called LS1. The aim of this operation was to improve the machine performance. After the first shut-down, beam energies between 7 TeV and 14 TeV were achieved. A second shut-down (LS2) is foreseen in the 2018-2019 period. In that occasion, the LHC luminosity will be be raised to twice the nominal luminosity. This performance improvement, called *phase 1 upgrade*, will also require an upgrade of the detectors, because the present version of the detector could not be operated in the environment of the upgraded accelerator. A new version of the pixel detectors will be introduced in 2018-2019.

As displayed in figure 1.2, which shows the LHC upgrade timeline, LHC will suffer another long shut-down period, called LS3, from 2023 to 2025, during which the High Luminosity (HL)-LHC will be installed. Its name comes from the huge luminosity of the collider: the beam energy will be around 14 TeV and the luminosity will be increased by a factor of 5 to 7 with respect to the nominal luminosity. During LS3, the CMS experiment (and also the ATLAS experiment) will be upgraded (*phase-2 upgrade*), to

comply with the increased environment hostility. In the ALICE and LHCb experiments, major detector upgrades are instead foreseen during LS2.

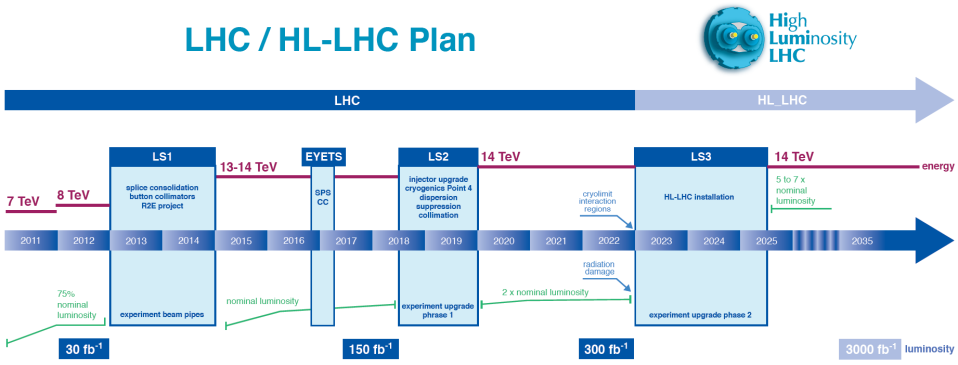


Figure 1.2: LHC timeline.

1.1.2 Overview of the CMS Experiment

The goal of the CMS experiment is to investigate a wide range of physics phenomena, including the search for the Higgs boson, extra dimensions, and particles that could make up dark matter. The CMS detector has approximately the shape of a cylinder 21.6 m high and with a base diameter of 16.6 m. The total weight of the detector is about 14000 tonnes. It is located in an underground cavern at Cessy in France, just across the border from Geneva. In July 2012, along with ATLAS, CMS discovered the Higgs boson.

CMS consists of four detectors, which exploit the different properties of particles to catch and measure the energy and momentum. The CMS detector is required to provide a high performance system to detect and measure muons, a high resolution method to detect and measure electrons and photons (an electromagnetic calorimeter), a high quality central tracking system to give accurate momentum measurements, and a "hermetic" hadron calorimeter, designed to entirely surround the collision region and prevent particles from escaping.

The CMS detector is built around a huge solenoid magnet, in order to take advantage of the properties of the charged particles: the higher a charged particle momentum, the less its path is curved in the magnetic field. Thus, once its path has been tracked, its momentum can be calculated. A strong magnet is therefore needed to enable accurate measurements even of the very high momentum particles, such as muons. The solenoid takes the form of a cylindrical coil of a superconducting cable that generates a magnetic field of 4 T.

As anticipated, the CMS detectors are composed by four different layers, as shown in figure 1.3. From the innermost layer, the detectors are: the silicon tracker, the electromagnetic calorimeter (ECAL), the hadron calorimeter (HCAL) and the external muon chamber, which is separated form the previous detector by the superconducting solenoid.

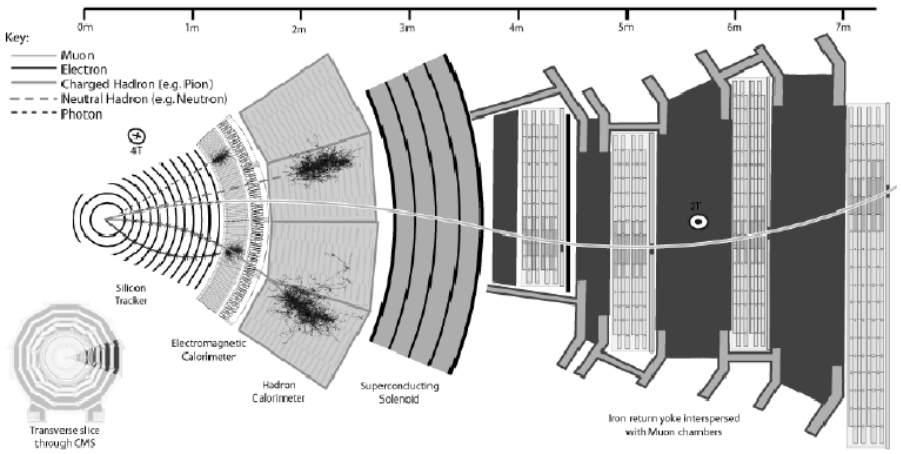


Figure 1.3: transverse section of the CMS detector and signatures for different particles crossing the volume.

The tracker can reconstruct the paths of high-energy muons, electrons and hadrons and it is composed by 13 layers in the central region and 14 layers in the endcaps. The innermost three layers (up to 11 cm radius from the interaction point) consist of 100×150 μm pixels. The next four layers (up to 55 cm radius) consist of 10 cm × 180 μm silicon strips, followed by the remaining six layers of 25 cm × 180 μm strips, out to a radius of 1.1 m. With a total active silicon area of 200 m^2, the CMS tracker is the largest full-silicon tracking system, with 1440 pixel-modules and 14148 strip modules, corresponding to 66 million pixels and 9.3 milion silicon strips.

The tracking system is followed by the electromagnetic calorimeter (ECAL), which achieves accurate measurements of electron and photon position and energy. The third detector is the hadronic calorimeter (HCAL), which is used for measurement of energy and direction of particle jets and the reconstruction of missing transverse energy contributions[1]. The last detector is the one dedicated to muon detection and is the farthest from the beam interaction point, because muons can penetrate several meters of iron without interaction.

1.1.3 Current status of the CMS pixel detectors

The silicon pixel tracking system in CMS is located very close to the interaction point, implying a very high track density and particle fluence which require radiation hard sensors and electronics. In particular, the innermost layer, which is at about 4 cm from the interaction region, is subjected to a charged particle flux of the order of 100 MHz/cm^2.

Each pixel sensor cell is bump-bonded to a full-custom ASIC, designed in a 0.25 μm CMOS technology using special layout techniques which ensure the required radiation hardness. Therefore, the lifetime of the tracker is limited by the damage in the silicon sensor. The innermost layer of the silicon pixel tracker has been designed in order to survive at least 2 years at the nominal LHC luminosity, while 10 years of lifetime is expected for the third layer.

The pixel sensor for the innermost layer in the silicon tracker is composed by 52 columns x 80 rows (4160 cells). Each pixel has an area of 100 μm x 150 μm. The signal generated when a charged particle passes through the sensor, is processed and read out by a full-custom ASIC bump-bonded to the sensor. The ASIC chip, called PSI46V2, is shown in figure 1.4[2], [3].

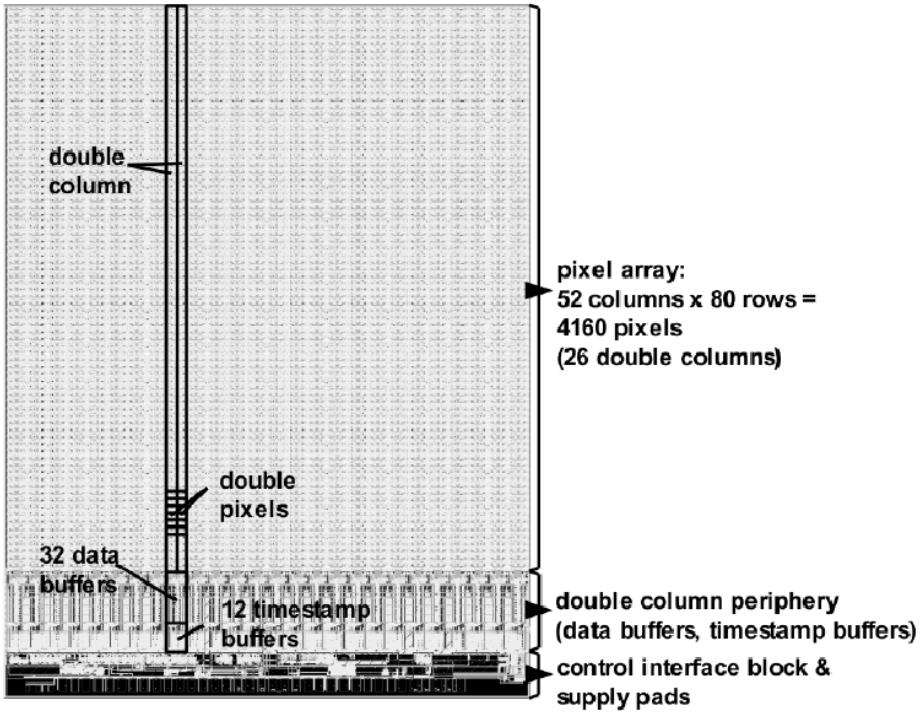


Figure 1.4: layout of the PSI46V2 chip employed in the CMS silicon tracker.

The PSI46V2 has an area of 7.8 mm x 9.8 mm, where 7.8 mm x 8 mm are taken by the core pixel matrix and 7.8 mm x 1.8 mm are used for the chip periphery. The core pixel matrix is composed by 52 columns x 80 rows of pixel. Each pixel cell is bump-bonded to a sensor. In the chip, two adjacent columns are assembled in order to share services, such as power distribution, bias and data-buses. Each pixel cell has to provide some storage and buffering capabilities for the signals coming from the sensors. On the other hand, only when a trigger signal is sent to the the detectors, the chip itself has to read the pixel matrix and send the data off-chip. In particular, the PSI46V2 uses a full analog readout. Indeed, charge information is retrieved by only a sample-and-hold circuit, placed in each pixel cell. This piece of information is transferred to the analog buffer in the chip periphery. Thus, the readout is performed in analog form, using a 40 MHz serial analog link.

Figure 1.5 shows the block diagram of the pixel cell of the PSI46V2 chip. The charged particle, which passes though the sensor, generates a signal. Such signal is sent to the analog front-end system by means of the bump-bonding interconnection. The front-end system is composed by a charge sensitive amplifier (CSA) and a shaper. The output of the shaper is connected to a continuos-time voltage comparator. The comparator threshold is adjustable with an 4-bit DAC.

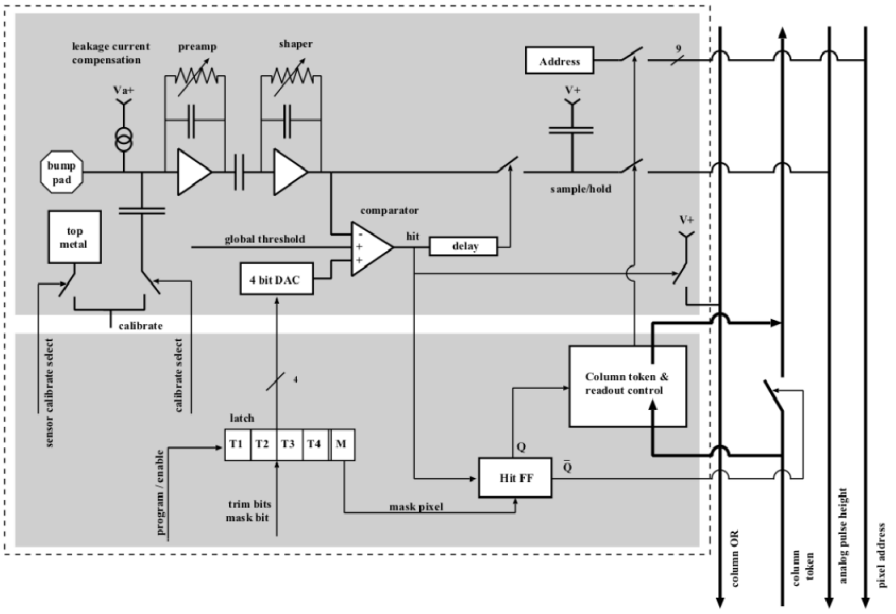


Figure 1.5: block diagram of the pixel cell of the PSI46V2 chip employed in the CMS innermost silicon pixel layer.

The power supplies are 1.5 V for the analog section and 2.5 V for the digital section. The overall power consumption is 120 mW, with 29 μW for pixel cell. The overall chip configuration uses an I^2C serial programming interface at 40 MHz. Table 1.1 summarizes the main specifications of the PSI46V2 chip.

Table 1.1: main specifications of the PSI46V2 chip.

Parameters	Values
pixel size	100 μm x 150 μm
chip size	7.9 mm x 9.8 mm
technology	CMOS 0.25 μm
number of pixel	52 columns x 80 rows
readout	full-analog
readout speed	40 MHz
nominal charge threshold	3 ke$^-$
supply voltage	1.5 V (A), 2.5 V (D)
power consumption	$\approx 30\mu$W/pixel

1.1.4 The phase 1 upgrade of the CMS pixel detector

The phase 1 pixel upgrade for CMS is planned to meet the requirements at the expected peak luminosity of 2 times the nominal luminosity. Furthermore, the innermost barrel layer has to be replaced, due to radiation damage in the sensor module.

In particular the main goals of the upgrade are:

- optimization of the layout for four barrel pixel detectors in the inner tracker;
- reduction of the material budget;
- improvement in the efficiency and minimization of radiation induced degradation;
- minimization of data loss in the new pixel readout chip (ROC).

During the upgrade, a new external layer will be introduced, as shown in figure 1.6. Also a new, smaller diameter beam pipe, needed to accommodate the innermost pixel layer, will replace the older one in order to have the detectors as close as possible to the beam. The new barrel layer will increase the number of pixel modules from 768 to 1184 and the number of pixels from 48 to 79 million. Quadruplicating the tracks seeds will greatly reduce the fake rate.

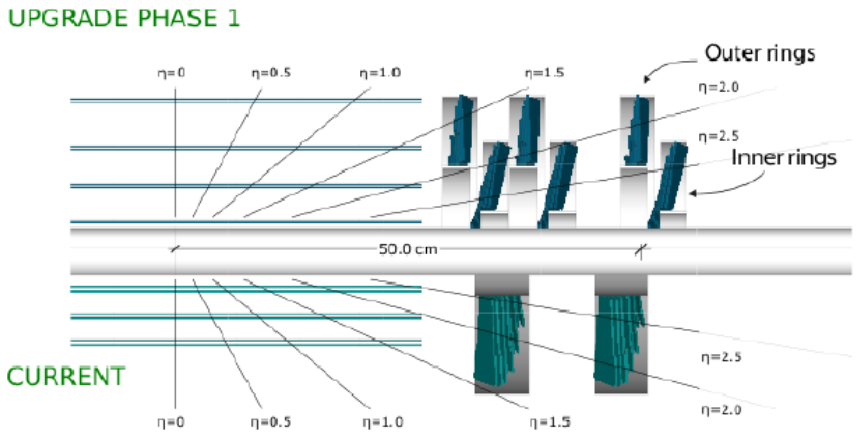


Figure 1.6: comparison between the current 3 layers (bottom) and the *Phase 1 upgrde* 4 layers for the CMS silicon tracker.

The amount of material around the interaction region can exacerbate the multiple scattering issue and degrade the detector accuracy in momentum measurement. In order to solve this problem, in the phase 1 upgrade a different cooling system will be adopted and the electronic boards and connections will be located out of the interaction volume.

Another improvement concerns the pixel readout chip (ROC). Indeed, the new design of the ROC will use a 160 Mbit/s LVDS data link instead of the 40 Mbit/s analog link currently being used. There will be 24 time stamp buffer cells, twice the current number. The data buffer size will increase from 32 to 80, and an additional buffer will be added to the readout chip level. Indeed, the current detectors have a relatively large amount of data loss, due to an insufficient readout speed[5].

In order to efficiently operate at increased data rate, an improved version of the present pixel detector ASIC, called PSI46V2 has been designed. The new chip, called PSI46DIG, has been designed in 0.25 μm CMOS technology. Such improvements, including digital readout blocks, have been incorporated, in order to guarantee the high tracking performance required by the *phase 1*.

The block diagram of the new PSI46DIG chip is shown in figure 1.7. The core architecture is mostly unaltered. Indeed, some improvements have been included in the new analog front-end: in particular the charge threshold has been reduced from 3.5 ke$^-$ to 1.5 ke$^-$. However, most of the new features are in the chip periphery. An 8 bit SAR ADC has been included in order to perform on-chip charge digitization. Also, an LVDS link operated at

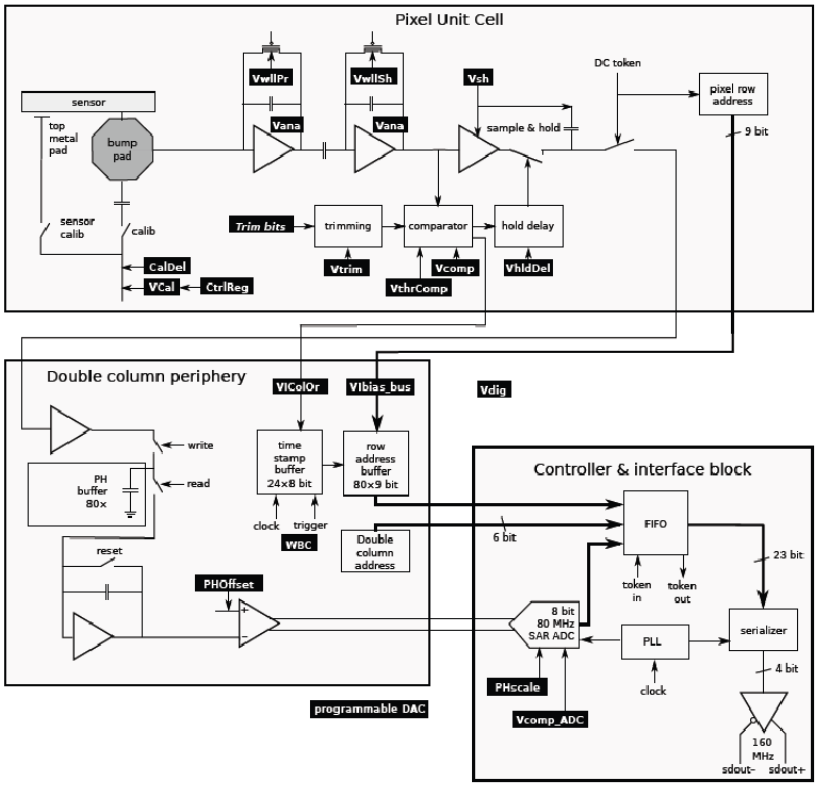


Figure 1.7: block diagram of the PSI46DIG ASIC chip.

160 Mbit/s has been included for the digital readout. The PSI46DIG can be considered the second generation of the hybrid pixel detector for the CMS silicon tracker. Table 1.2 shows a comparison between PSI46V2 and PSI46DIG readout chip specifications[5].

Table 1.2: comparison between PSI46V2 and PSI46DIG readout chip specifications.

Parameter	PSI46V2	PSI46DIG
chip size	7.9 mm x 9.8 mm	7.9 mm x 10.2mm
pixel size	100 μm x 150 μm	100 μm x 150 μm
technology	CMOS 0.25 μm	CMOS 0.25 μm
charge readout	analog	digital 8bit
redout speed	40 MHz	160 Mbit/s (LVDS)
double-column readout speed	20 MHz	20 MHz or 40 MHz
PLL for clock moltiplication	no	yes
threshold	3.5 ke$^-$	1.5 ke$^-$

1.1.5 The phase 2 upgrade of the CMS pixel detectors

As already mentioned, during the third long shutdown (LS3) of LHC (2023-2025), the collider will be upgraded to the High Luminosity LHC stage with a luminosity up to 5-7 times the nominal luminosity and an energy of 14 TeV. At this luminosity, the foreseen particle hit rate will rise to about 500 MHz/cm^2 (almost 10 times the present hit rate) and the foreseen total ionizing dose (TID) will be close to 1 Grad in 10 years of lifetime, while the particle fluence is expected to be about $2 \cdot 10^{16}$ (1MeV)n.eq/cm^2. Such a harsh radiation environment requires the installation of a new generation of hybrid pixel detectors in the CMS innermost layer of the silicon tracker, able to withstand these radiation doses. Moreover, the pixel detectors for the CMS phase 2 upgrade (as this new experiment stage is called), will have to cope with the very high data rate and guarantee an increased track resolution.

The pixel size is a critical aspect and the chosen one represents a trade-off between physics performance requirements, sensor technology, scale of integration of the front-end chip process and interconnection technology. At the moment, in the technical proposal, the pixel size of the sensor for the inner tracker is 50 μm x 50 μm or 25 μm x 100 μm in order to guarantee the required resolution. In each pixel cell for the pixel detector ASIC, an analog front-end chain is integrated in order to perform the signal amplification and hit discrimination with a minimum detectable charge close to 1 ke$^-$. Another challenge for the third generation of the pixel detectors, besides resolution, is the hit rates per unit area, that is close to 2 GHz/cm^2. To summarize the main goals of the new pixel detector ASIC are:

- higher radiation hardness for the innermost layer, indeed the working period in very harsh radiation environment is supposed to be $\sim$10 years with up to $\sim$1 Grad total dose;

- increased granularity, with pixels 50 μm x 50 μm in area and a pixel matrix of 1024 rows x 256 columns;
- improved rate capability of the ROCs, with a bandwidth increased from 40 Mbit/s (1^{st} generation) to 3 Gbit/s (3^{rd} generation);
- lower power consumption, with a power budget around 0.4 $\frac{\mathrm{W}}{\mathrm{cm}^2}$and an estimated front-end chip area of 4 cm^2.

General ASIC specifications for the 3^{rd} generation of hybrid pixel detectors are shown in table 1.3, while table 1.4 shows the evaluation of the requirements evolution for the pixel detectors.

Table 1.3: specification for the 3^{rd} generation of hybrid pixel detectors for the innermost layer of the CMS silicon tracker.

Parameters	Specifications
number of barrel layers	4
charged particle flux	500 MHz/cm^2
total radiation damage	1 Grad in 10 years
pixel size	50 μm x 50 μm or 25 μm x 100 μm
chip size	$\sim$ 4 cm^2
hit-rate	1-2 GHz/cm^2
hit-time resolution	$<$ 25 ns
signal threshold	$1 - 1.8$ ke^-
charge resolution	4-8 bits
power budget	$<$ 0.4 W/cm^2
hit memory per chip	16 Mbit

65 nm CMOS technology has been chosen as the technology for the design of the new pixel detector for the phase 2 upgrade. The choice of the 65 nm CMOS technology is mainly dictated by the good radiation tolerance of the process, also validated through experimental measurements. This technology will bring some further advantages. As compared to the 250 nm technology used for the previous generations of front-end chips, it can offer larger speed and low power consumption. It is true that the 65 nm CMOS technology is used for the first time in HEP experiments. Nevertheless, it is a mature technology, used in many commercial applications and it guarantees long-term availability. The latter characteristic is very important, because will have to be available for the time the phase 2 upgrade becomes operational (2022-23) and for several year after that.

Figure 1.8 shows the block diagram of the hierarchical organization of the front-end chip for the innermost layer of the CMS silicon tracker. A small signal must be detected and amplified in each pixel by a low noise

Table 1.4: evolution of the main requirements of the pixel detectors ASIC for the innermost layer of the CMS silicon tracker.

Parameter or FEATURE	CMS 1^{st} generation LHC Phase 0	CMS 2^{nd} generation LHC Phase 1	CMS 3^{rd} generation LHC Phase 2
pixel size	100 μm x 150 μm	100 μm x 150 μm	50 μm x 50 μm
technology	CMOS 250 nm	CMOS 250 nm	CMOS 65 nm
power supply	1.5 V(A), 2.5 V (D)	1.5 V(A), 2.5 V (D)	1.2 V(A), 1.0 V(D)
Max Particle Flux	$\sim$ 50 MHz/cm^2	$\sim$ 200 MHz/cm^2	$\sim$ 500 MHz/cm^2
Max Pixel Flux	0.2 GHz/cm^2	$\sim$ 0.6 GHz/cm^2	$\sim$ 2 GHz/cm^2
Rad. Hardness	0.15 Grad	0.35 Grad	1 Grad
Signal Threshold	2500-3000e$^-$	1500-2000e$^-$	$\sim$ 1000 e$^-$
ASIC side	$\sim$ 1 cm^2	$\sim$ 4 cm^2	$\sim$ 4 cm^2
Hit memory per chip	$\sim$ 0.1 Mb	1 Mb	$\sim$ 16 Mb
Chip output bandwidth	$\sim$ 40 Mb/s	$\sim$ 320 Mb/s	$\sim$ 3 Gb/s
Power Budget	$\sim$ 0.3 W/cm^2	$\sim$ 0.3 W/cm^2	$<$ 0.4 W/cm^2

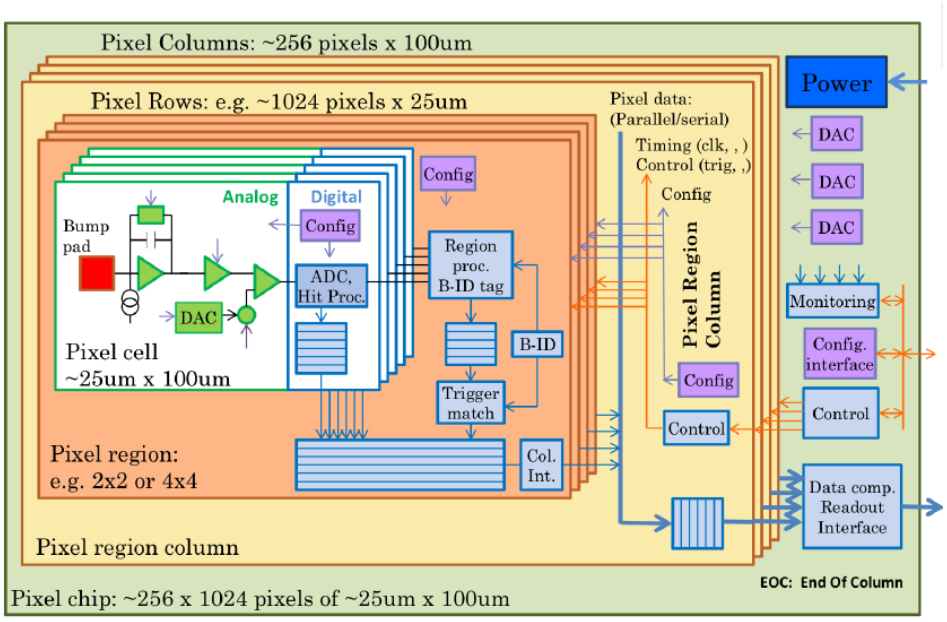


Figure 1.8: block diagram of the 3^{rd} generation of front-end chip for the innermost layer of the CMS silicon tracker.

charge sensitive amplifier and, eventually, digitized for further processing. The large number of pixels (100k – 1M) implies that the analog circuit design has to address some critical aspects for physical layout area and for very low power consumption. To overcome these limitations, a design approach based on subdividing the chip array in regions of 4x4 pixel cells will be explored in order to share digital resources.

The chip will include also a number of so called IP (intellectual property) blocks, typically located in the chip periphery. The IP blocks will have to be designed and optimized for the specific pixel application, in such a way to deal with the expected levels of radiation. A non-exhaustive list of these IP blocks follows:

- current and voltage references, they must provide a stable reference independent of variations in supply voltage, temperature, fabrication process parameters and radiation;
- compact low speed (static) Digital to Analog Converters (DAC) are required for generating adjustable analog biases;
- analog to digital converters (ADC) are required for monitoring some parameters (e.g. temperature, supply voltage, etc);
- temperature measurement circuits;
- adjustable (and self-calibrating) timing generators are required to align the sampling point of the pixel detector to the bunch collisions and be capable of making timing sweeps of calibration pulses across the sampling clock period;
- phase locked loops (PLL) are required for clock recovery from encoded input and for high speed serial readout;
- high speed, low power output drivers will be required to drive the local data link to the location of the final high speed serializer and driver for the optical link;
- command decoder and clock recovery to process incoming serial input;
- SEU hard static memory cells; they do not have to be logic library elements, but can be designed as an analog block in order to achieve the maximum possible tolerance for storage of configuration values;
- voltage regulators and DC-DC converters;
- programmable processors, for example a DSP (digital signal processor) or AM (associative memory block), these could be used for many things, not necessarily for processing hit data, for example self testing or of the chip functions could be implemented;
- analog test and calibration circuits, for example to obtain a chip-by-chip calibration of the charge injection absolute scale.

In this thesis, the design and characterization of two IP blocks will be discussed. In particular, the description of a rad-hard bandgap voltage reference will be described in chapter 2 and the description of a differential IO link system, in particular an SLVS transmitter and an SLVS receiver, will be described in chapter 3. In the following section, a general overview of the first demonstrator for the CMS pixel front-end chip is provided. The aim of this chip is to demonstrate the feasibility of the third generation of pixel front-end ASICs using for the first time the 65 nm CMOS technology in the High Energy Physics community despite the very harsh radiation environment, the very high resolution requirements and the necessity to comply with very large particle rates.

1.2 The RD53A demonstrator chip

RD53 is an international collaboration, whose final goal is the design of the next generation of pixel readout chips to enable the ATLAS and CMS Phase 2 pixel upgrades. The collaboration started in 2013 and includes research groups from: Bonn, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, UC Santa Cruz, INFN Bari, INFN Pavia, Fermilab, INFN Padova, INFN Perugia, INFN Pisa, PSI, RAL, Torino, CERN and RAL. The duration of the project is estimated in three years (2013-2016) and will lead to a final chip demonstrator, called RD53A.

The requirements for pixel detector ASIC for CMS and ATLAS, while not identical, are quite similar. So, RD53 will design a first demonstrator CHIP (RD53A) with common requirements and features for the two experiments[7], [8]. However, a cross-experiment collaboration does not imply that ATLAS and CMS will adopt the same ASIC for their phase 2 upgrades.

The engineering run of RD53A is foreseen for April 2017. The aim is to demonstrate, in a 65 nm CMOS technology, stable low threshold operation and compatibility with high hit and trigger rate, as required for HL-LHC upgrades of ATLAS and CMS, in a large format IC. RD53A is not intended to be a final production IC for use in the experiments. It will contain design variations for testing purposes, making the pixel matrix non-uniform.

The RD53A IC will have an area of 20x11.8 mm^2 and will consist of a matrix will composed by 400 rows and 192 columns. Each pixel will have an area of 50x50 μm^2[9]. The main features of the chip are summarized in the following list:

- tolerance to TIDs larger than 500 Mrad;
- high hit rate: 2 GHz/cm^2;
- dead time loss: $< 1\%$;

- trigger rate: 1 MHz;
- low threshold: 1000 e^-;
- serial powering

1.2.1 RD53A chip design and assembly

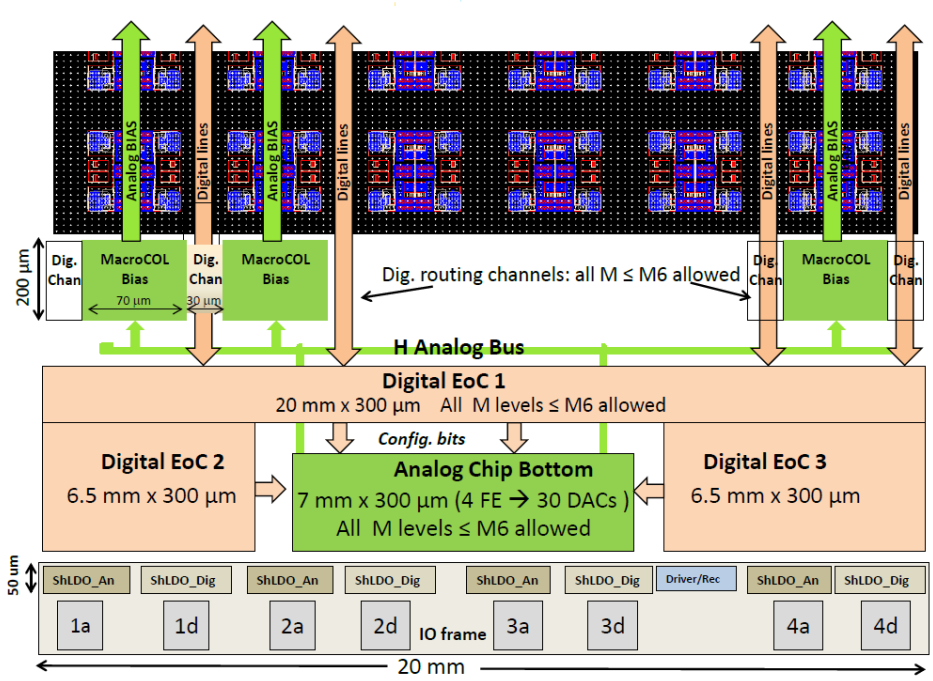


Figure 1.9: preliminary floorplan of the RD53A chip

The preliminary floorplan of the RD53A chip is shown in the figure 1.9. The top side shows the pixel matrix, in which each pixel is an analog island surrounded by a digital sea. Such design methodology is a new approach used in the HEP community, which enables the use of place and route automatic tools for VLSI chips. An analog island including the analog sections of four pixels is shown in figure 1.10.

Each pixel region is composed by a 4x4 analog pixel cell to share the digital function (i.e. buffering and time-stamp generation). For each two columns of pixels, there is a column base block (MacroCOL Bias) at the end of the column. Such block provides the biasing and voltage reference and the calibration levels for the pixels in the column. The current references are generated in the analog chip bottom (ACB) block through a voltage bandgap reference. The current reference is used by a current DAC, providing the

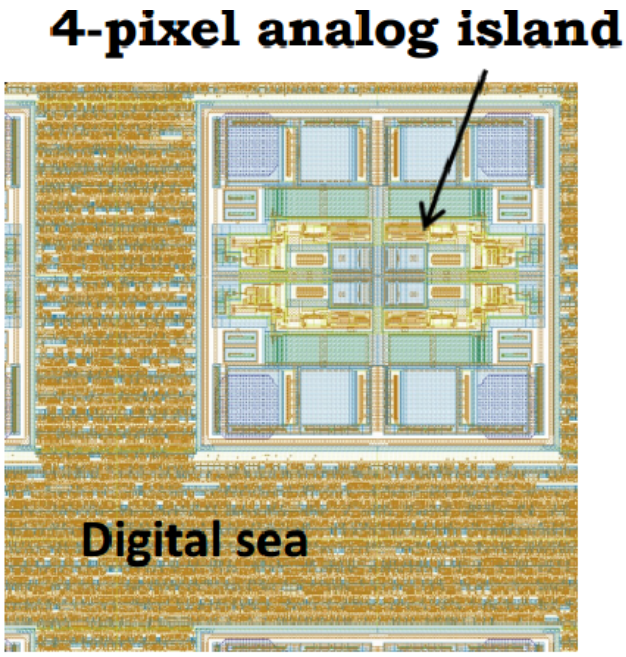


Figure 1.10: example of the new design approch. Four custom analog pixels are surrounded by a digital sea, where the digital standard cells are automatically placed and routed by synthesis tool.

biasing reference to the Macro COL Bias. The purpose of the DAC is to compensate for mismatch variations among pixel columns.

The digital EoC (End of Column) manages the readout of the pixel matrix and sends the data off-chip by means of an SLVS transmitter. There will be also an SLVS receiver for ASIC programming (i.e. threshold level, calibration level, current reference, etc...). The transmitter and receiver will be presented and discussed in chapter 3.

At the bottom of the floorplan, the I/O frame is shown. This frame includes the shunt-LDO (Low Drop-Out) and the wire bond pads. Shunt-LDOs are used to address the inefficiency issue due to power distribution in such large systems, as the CMS detectors. Phase 2 upgrade will consists of millions of channels grouped in modules. The modules are powered by cables with a length up to 100 m, introducing significant power losses. A serial powering approach has been proposed to overcome this problem. In a serial powering configuration, modules are placed in series and powered by a constant current source. Shunt regulators are used at module level to generate the supply voltage of the current supply and the LDO is used to regulate the output voltage[10]. In the RD53A chip, 5 shunt-LDOs are

foreseen in order to power four front-end topologies and the analog chip bottom (ACB) block.

The pixel matrix includes four topologies of analog front-end, each with a bump bond pad at the channel input for interconnection with the sensor. The analog channel has to comply with the following requirements: a typical input of 10 ke$^-$, a minimum detectable charge of 0.1 MIP (minimum ionizing particle), i.e. 1000 e$^-$, and an input dynamic range as large as 30 ke$^-$ (3 MIPs) and a hit time response shorter than 25 ns. The main requirements for the analog front-end are summarized in the table 1.5.

The pixel matrix will include four different analog front-end, designed by four different institutes: the Lawrence Berkeley National Laboratory (LBNL), the Fermi National Accelerator Laboratory (FNAL), the Universities of Bergamo and Pavia and INFN Pavia and, finally, INFN Torino. The schematic diagram of each analog front-end are shown in figure 1.11, 1.12 , 1.13 and 1.14. More details about the realization and measurement results of the analog front-ends can be found in the literature [12], [13], [14].

Table 1.5: specification for the RD53A analog front-end.

Parameters	Specifications
Input polarity	Negative
Pixel capacitance	$<$ 100 fF
Pixel leakage current	$<$ 10 nA
Minimum detectable charge	1 ke$^-$
Threshold	600 e$^-$
Equivalent Noise Charge	$<$ 130 e$^-$
hit time response	$<$ 25 ns

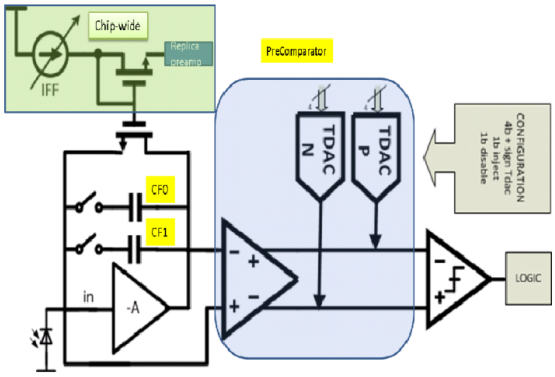


Figure 1.11: schematic of the analog pixel front-end designed at LBNL.

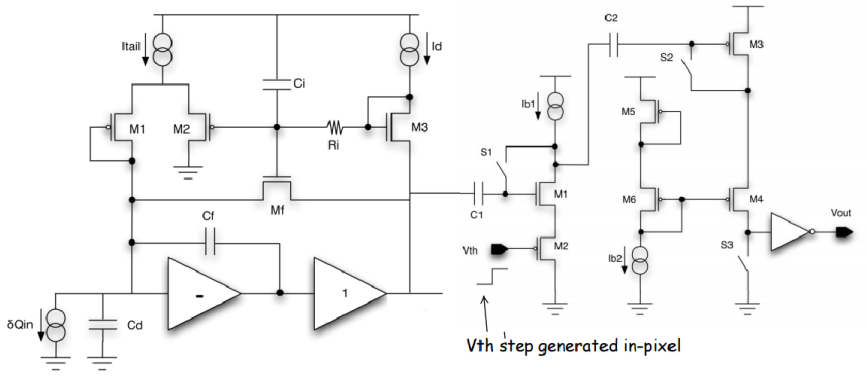


Figure 1.12: schematic of the analog pixel front-end designed at FNAL.

The analog chip bottom (ACB) block, a multi-purpose block, is located in the periphery of the chip[1]. The task performed by the ACB are described by the block diagram in figure 1.15. The first task of the block is to provide different current references to 40 current DACs in the macro COL Bias block. A 4 μA current reference can be regulated with a DAC in order to compensate for the process variations. The second task of the ACB is to monitor different signals coming from the RD53A chip (i.e. 4 μA current reference, temperature sensor, radiation sensor, VCO, etc...). Such signals are digitized by a 12 bit ADC and fed to the DSP. The ACB also includes the clock data recovery, the serializer and power on reset blocks. All these circuits have been thoroughly tested, also from the standpoint of radiation tolerance before the integration in the RD53A chip.

The IP blocks, that will be presented and discussed in this thesis will be integrated in R53A chip. In particular, the bandgap voltage reference will be included in the ACB block, as a voltage reference for the monitoring ADC and as reference for the current DAC. The SLVS I/O link will be inserted in the digital I/O section.

[1]The author has been in charge of the integration activity for this block during the last period of PhD.

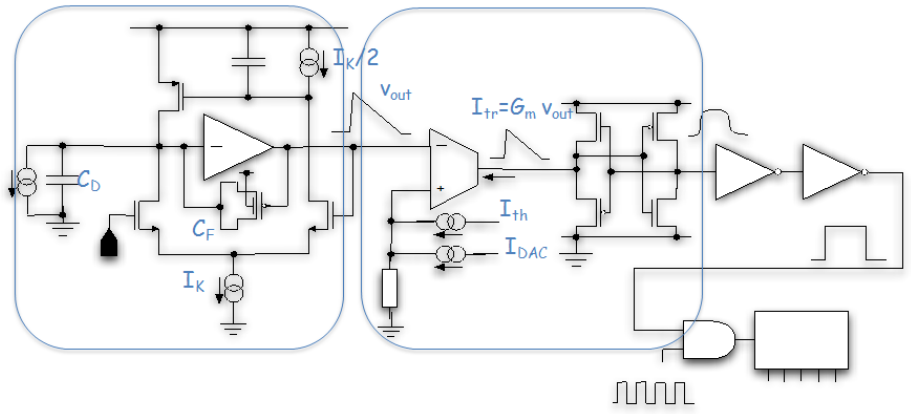


Figure 1.13: schematic of the analog pixel front-end designed at Universities of Bergamo and Pavia and INFN Pavia.

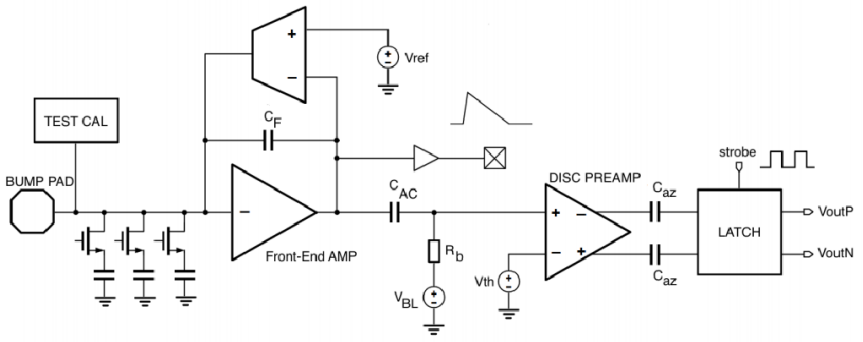


Figure 1.14: schematic of the analog pixel front-end designed at INFN Torino.

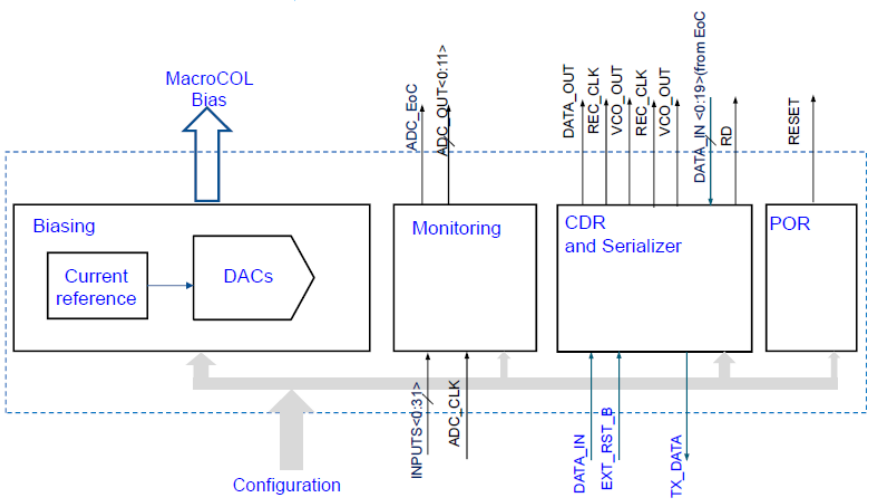


Figure 1.15: analog chip bottom block diagram.

CHAPTER 2

RAD-HARD BANDGAP VOLTAGE REFERENCE

Contents

The bandgap voltage reference (BGR) is a circuit which provides an accurate voltage (or current) insensitive to process, supply voltage and temperature variations. For applications to the phase 2 upgrade of the pixel detector in the CMS experiment, tolerance to very large total ionizing doses is a mandatory feature of the circuit. For this reason, the first part of this chapter has been dedicated to a general overview about the radiation

effects on CMOS transistors and radiation hardening techniques for electronic circuits. The main part, instead, has been dedicated to the design and characterization of the radiation-hard bandgap voltage reference.

2.1 Radiation effects on CMOS transistors and integrated circuits

This section describes the physical mechanisms underlying radiation damage in MOS structures. The focus is on the effects of ionizing radiation in silicon dioxide and at the oxide-semiconductor interface.The variation of electrical parameters (i.e. threshold voltage, transconductance and leakage current) due to ionizing radiation is also described. The last part of this section is dedicated to radiation hardness techniques for electronics circuits.

2.1.1 Radiation-matter interaction

The interaction between ionizing radiation and matter depends on the kinetic energy, the mass and the type of incident particle. Particles can be subdivided in two main groups: charged and neutral particles.

Charged Particles

Charged particles interact with the electrons or the nucleus of the target atoms through Coulomb forces. The charged particles of interest are *protons*, *heavy ions* and *electrons* and their interactions are described in the following for the different kinds of particles.

- Protons and Heavy Ions:
  - Coulomb interaction, which is responsible for ionizing and atomic excitation;
  - collision with nuclei, which is responsible for excitation or atom displacement in the lattice;
  - nuclear reaction, which occurs for energies higher than 10 MeV.
- Electrons, which can be generated by an external source (primary electrons) or can be produced by the target material itself after interaction with other particles (secondary electrons).
  - Coulomb interaction, which is responsible for ionizing and atomic excitation;
  - scattering with nuclei, which can cause the atom displacement in the target lattice, in case the incident electron energy is high enough.

Neutral Particles

Neutral particles, such as neutrons and photons, differ from charged particles because they are not affected by the Colombian forces. Neutrons can be classified as a function of their energy level: *slow* for energies lower than 1 eV, *intermediate* for energies in a range between 1 eV and 100 eV and *fast* for energies greater than 100 eV. When interacting with the nuclei of the target material, such particles can generate different effects:

- nuclear reaction: neutrons are absorbed in the nuclei, which then emit other particles (i.e. protons, α particles and/or γ photons);
- elastic collision: neutrons collide with some nucleus and then continue their path; if neutrons acquire enough energy, they can generate displacement and ionization.
- inelastic collision: it is similar to the elastic collision, but the excited nucleus decays and emits gamma rays.

Photon interaction can occur in three different ways:

- photoelectric effect: the target atom is ionized by incident photon, which is completely absorbed; in addition an electron is emitted;
- Compton effect: the incoming energy is divided between the generated free electron and an emitted photon;
- pair production: the energy of the photon is converted into an electron-positron pair; this effect takes place for energies greater than 1.022 MeV.

Effects from particle interaction with matter can be subdivided into two groups: ionization and nuclear displacement. Neutrons, which are neutral and massive particles, give origin to nuclear displacement, while photons, electrons and charged particles are responsible for ionization effects. Ionization produces electron-hole pairs in semiconductors. The created pair number is proportional to the energy deposited in the semiconductor. Highly energized particles (protons, electrons, neutrons and heavy ions) can damage semiconductor materials by displacing atoms as the particle moves through the material. In silicon, Frenkel defects[1] (interstitial silicon and vacancy pairs) are formed when incident particles collide with silicon nuclei or when primary recoil atoms collide with other atoms in the lattice [15].

[1] A Frenkel defect is a defect type in crystalline solids wherein an atom is displaced from its lattice position to an interstitial site, creating a vacancy at the original site and an interstitial defect at the new location within the same element without any changes in chemical properties.

2.1.2 Radiation effects on MOS transistors

MOS transistors are more sensitive to ionization than displacement damage. Figure 2.1 shows a schematic energy band diagram for a MOS structure, where positive bias is applied to the gate, so that electrons flow toward the gate and holes move to the silicon substrate. Four major physical processes, which contribute to the radiation response of a MOS device, are also indicated. The most sensitive part of a MOS system to radiation is the oxide insulator[16].

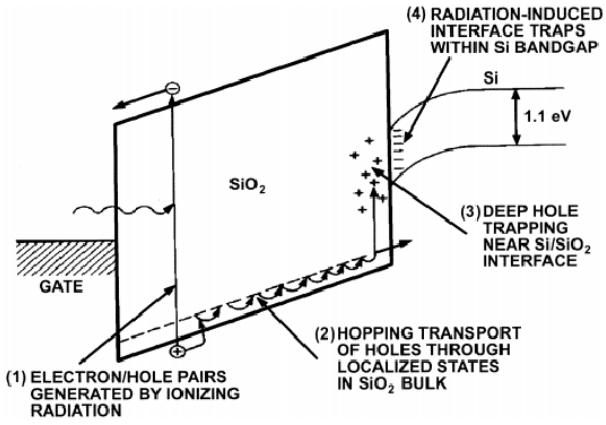


Figure 2.1: schematic energy band diagram for MOS structure, indicating major physical processes underlying radiation response.

Electron-holes pairs are generated, when an ionizing particle passes though a MOS structure. In the substrate, which is a low resistivity material, the pairs are recombined immediately after being created. In silicon dioxide, the mobility of the carriers can be 5-20 orders less than in the substrate. Indeed, a fraction of electron-hole pairs recombines immediately, while the remaining pairs are separated in the oxide by the applied field. For example, when a positive voltage is applied at the gate, the electrons are attracted by the gate electrode in a few picoseconds, whereas the holes are moved to the silicon-dioxide interface. Near the interface and in the oxide, the holes may be trapped and can generate a fixed potential in the oxide itself. The purpose of this paragraph is to discuss MOS parameter degradation due to charge trapped in the oxide and to radiation-induced interface traps.

Threshold voltage shift

The variation ΔV_T of the threshold voltage in a MOSFET is an effect of the exposure to ionizing radiation. The effect is different in P-channel and N-channel devices. Since the charge trapped in the oxide is always positive,

the threshold voltage, for NMOS devices, undergoes a reduction for low TID (Total Ionizing Dose) due to the positive charge trapped in the oxide, before increasing back again for high values of the TID, due to negative charge trapped at the interface. In the case of PMOS devices, the threshold voltage tends to decrease steadily with increasing dose. A textbook example of such variations is shown in figure 2.2 [17].

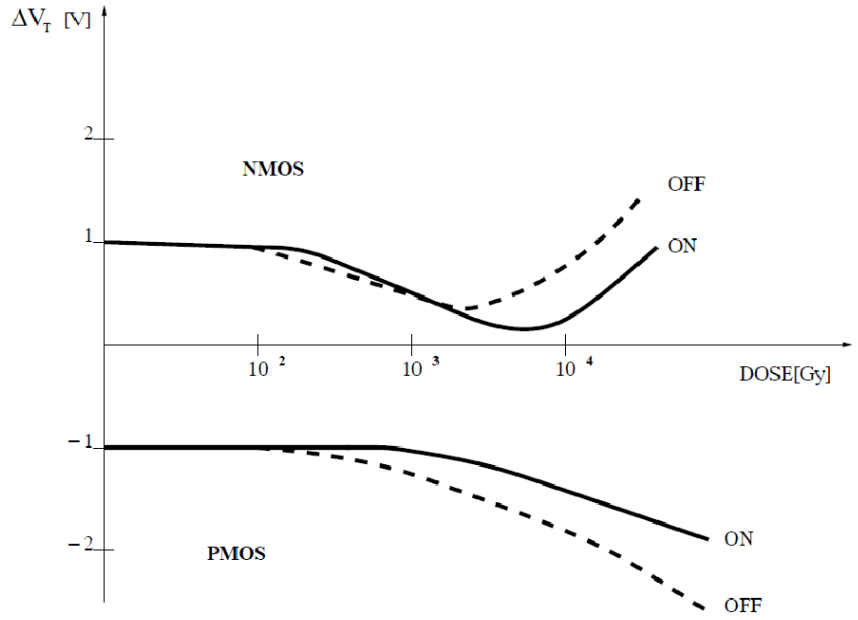


Figure 2.2: variation of the threshold voltage as a function of the Total Ionizing Dose (TID) for PMOS and NMOS devices.

The effect on the threshold voltage due to positive charge trapped in the silicon dioxide can be explained by the MOSFET working principle. Indeed, in the case of an NMOS device, the minority carriers in the substrate (electroncs) are attracted by positive charge build-up in the gate oxide: this helps in the creation of an inversion channel beneath the device gate and is equivalent to a reduction in the device threshold voltage. In the case of PMOS devices, instead, the trapped positive charge opposes the formation of the P-type channel.

On the other hand, due to radiation-induced traps at the interface between substrate silicon and silicon dioxide, both in NMOS and in PMOS devices the threshold voltage tends to increase. Since the interface state creation is a slow phenomenon, the threshold voltage in NMOS devices tends to decrease at the beginning and starts increasing only at higher dose. In scaled technologies, threshold voltage shift due to gate oxide, is negligible, if

compared with the interface state effect. For this reason, threshold voltage of the NMOS device tends to increase already at small doses[17].

Leakage current

In deep sub-micron CMOS technologies, transistors are surrounded by the shallow trench isolation (STI) oxide, which does not scale down as the gate oxide with the technology node. As a consequence, radiation-induced charge trapping in the STI oxide (see figure 2.3) still leads to macroscopic effects such as source-drain or inter-diffusion leakage currents, ultimately limiting the radiation tolerance of conventional CMOS circuits. The STI oxide is thicker than the gate oxide, so the positive charge trapped in the STI can create a parasitic path between source and drain of NMOS transistors. This parasitic transistor is a composition of different devices connected in parallel mode, as shown in figure 2.4. Moreover, a 1/f noise increase is observed in irradiated NMOS devices at low drain current density as in figure 2.5 [19],[18]. In PMOS devices, no inversion can take place close to the STI, because the substrate is of the N-type, so no parasitic device is created.

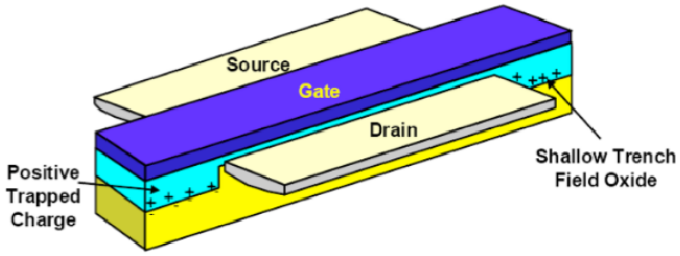


Figure 2.3: conceptual drawing (not to scale) showing how positive charge build-up in STI oxides can lead to lateral leakage currents in NMOS devices.

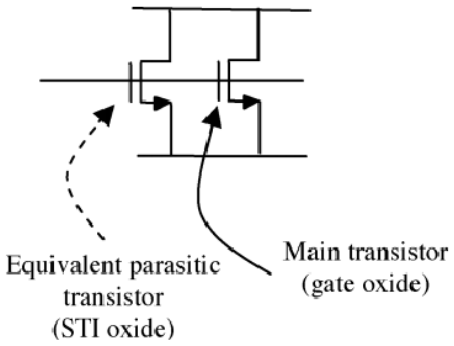


Figure 2.4: circuit model for an NMOS exposed to ionizing radiation with the parasitic devices due to charge trapped in the STI.

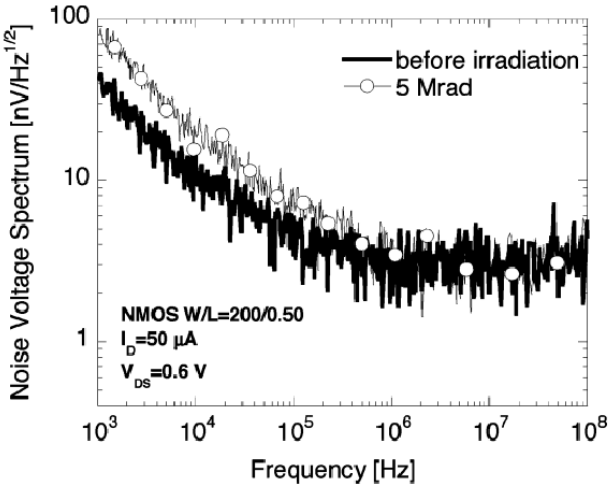


Figure 2.5: Noise voltage spectra before irradiation and after exposure to a 5 Mrad total dose of X-rays for an NMOS with W/L=200/0.5 in the 65 nm process, at 50 μA drain current.

Mobility and transconductance degradation

Ionizing radiation can also produce mobility degradation. This phenomenon is essentially related to the increment of the interface traps between silicon (Si) and silicon dioxide (SiO_2). This effect degrades the mobility, since the conducting channel in a MOS device is close to the silicon-oxide interface.

The mobility degradation is expressed by the following formula:

$$\mu = \frac{\mu_0}{1 + \alpha \cdot (\Delta N_{it})} \tag{2.1}$$

where μ_0 is the mobility before irradiation, ΔN_{it} is the increase in interface trap density and α is a technology parameter. The mobility degradation may also lead to an increase of the thermal noise of the channel, due to the degradation of the transconductance.

2.1.3 Layout techniques for the design of radiation-tolerant circuits

Radiation effects may be mitigated by means of different techniques. In particular, the TID effects can be seen as an "analog" issue, because it can modify the parameters of the MOS. The parasitic transistor created in the STI thick oxide, due to the trapped charge, is the main contributor to the TID effects. A possible solution to mitigate this effect, is to enclose the drain or source diffusion within the gate oxide. This layout technique is called ELT (Enclosed Layout Transistor), shown in figure 2.6.

The ELT eliminates the parasitic path between drain and source. In the case of multi-finger devices, the ELT can be laid out using an interdigitated structure with an extension of the poly-sylicon layer, as shown in figure 2.7 (The poly-sylicon layer is in blue). In figure 2.8, data for two devices biased at low current density are compared. The TID effects on the noise voltage spectrum of an enclosed transistor, if any, are small as compared to the radiation-induced increase in the 1/f term that is measured in a standard layout multifinger device with the same gate width and length [20].

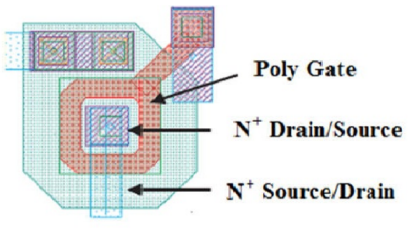


Figure 2.6: layout of an enclosed transistor (ELT) for rad-hard design.

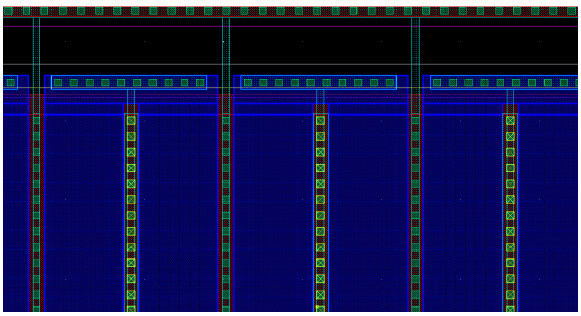


Figure 2.7: example of an enclosed layout for a multifinger device.

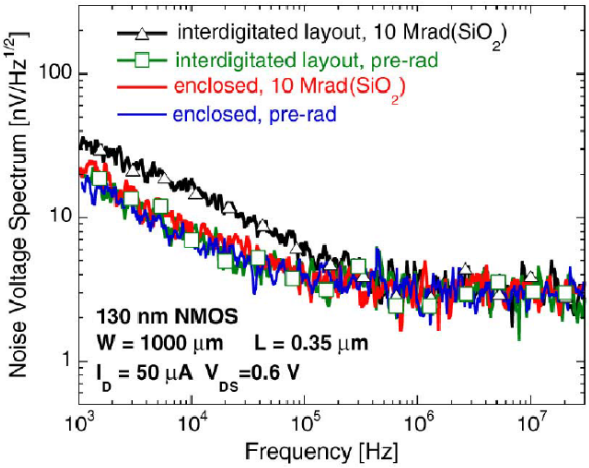


Figure 2.8: Noise voltage spectra before irradiation and after exposure to a 10 Mrad total dose for NMOSFETs with enclosed layout and with interdigitated layout, at 50 μA.

2.2 Rad Hard Bandgap Voltage Reference

Bandgap voltage references provide an output voltage reference with a low sensitivity to the temperature, voltage supply and process variations. They are fundamental building blocks in mixed-mode circuits, such as DRAM, ADC or flash memories. Conventional BGR circuits provide an output voltage (V_{REF}) which is in the range of 1.2-1.25 V [21]. Such circuits can hardly be implemented in the modern deep sub-micron CMOS technologies, where the supply voltage is in the same range or smaller. Several architectures have been proposed to overcome the problem of the supply voltage in conventional BGRs. One of them is called current mode architecture, since it generates a temperature-independent current, which is then mirrored to an output resistor to generate a sub-1V output voltage [22]. Typically realized by parasitic vertical pnp BJTs in CMOS technology[23], [24]. Bandgaps have always been based on parasitic bipolar transistors in CMOS technologies, but recently, many of them have been designed with MOSFETs biased in sub-threshold region, where MOS and BJTs exhibit similar temperature behaviour[25]. Another architecture for the sub-1V bandgap is called voltage-mode reference[26]. This solution uses the reverse bandgap voltage principle (RBVP). Instead of adding V_{BE} voltage to a factor of the thermal voltage kV_T, this circuit adds a V_T voltage to an attenuated base-to-emitter voltage V_{BE}[27]. Another solution has been explored in standard CMOS technology, without exploiting the traditional BGR principle. This solution is based on the sub-threshold operation of the MOSFETs[28],[29] and [30]. The bandgap voltage reference called ZTC (Zero-Temperature-Coefficient), which exploit the ZTC point of an MOSFET in the weak inversion region, can be also included in the non-conventional architecture [31].

In the framework of the High Energy Physics community, the radiation hardness is one of the most important criteria in the design of the bandgap reference circuits. Several works exploit the current-mode architecture using MOSFET in Dynamic Threshold configuration (DTMOS) [32] or using parasitic diode in CMOS process [33]. Other solution of rad hard bandgap reference without exploiting the traditional BGR principle can be found in [34]. This work focuses on the design of rad hard bandgap voltage reference based on current mode approach, in order to overcome the low voltage supply issue. This solution is based on the sum of two currents, respectively directly (PTAT) and inversely proportional (IPTAT) to the absolute temperature, to obtain the V_{REF} output voltage. Different solutions have been considered and implemented in a 65 nm CMOS technology. The BGRs developed can work with a 1.2 V supply voltage. The proposed circuit has been designed for biasing an ASIC system in HL-LHC applications. So the harsh radiation environment in which the bandgap is operated poses additional design requirements in terms of radiation tolerance. The 65 nm CMOS technology chosen for this prototype has been tested by exposing single devices to ion-

izing doses of several hundreds of Mrad with promising results, but some components of the BGR, namely bipolar devices, may be affected also by bulk damage effects. For this reason, in order to understand their behaviour after irradiation, three different BGR versions with the same architecture (i.e., current mode approach) have been designed and fabricated in a first prototype chip. The first version, which provides the best performance in terms of temperature insensitivity, is based on parasitic PNP bipolar transistors. The second, based on pn diodes, is the best solution in terms of area, while the third one, based on enclosed-layout MOSFETs biased in weak inversion region, is the most promising in terms of radiation tolerance.

A second prototype of the BGR has also been designed. In this second version of the BGR, a trimming resistor with 5 control bits has been included to minimize mismatch effects. The bias current has also been increased in order to mitigate the TID effects.

2.2.1 Guidelines and specifications

General guidelines and some specifications have been provided by the RD53 community in order to design the IP blocks for the *Phase 2*. In particular, the general guidelines regards the minimum size for the MOS devices (length of the channel $\geq$ 120 nm) in order to guarantee some radiation hardness constrains [19].

The most important specification for all IP blocks and also for the bandgap reference circuits is the radiation tolerance. Indeed, all IP blocks have to withstand a TID up to 500 Mrad. In this case, the maximum variation, before and after irradiation, for the bandgap, that will be used to generate the 4 μA in RD53A, has to be less than 20 mV. The design of the BGR for the RD53 has to also comply some general specification, shown in table 2.1. For this kind of application, the variation of the output voltage between two specific temperature: room temperature and $-20°C$, which is the temperature of the LHC experiment, has to be less 10 mV.

Table 2.1: design specifications of the BGR.

Parameter	**Value**
Area	$\leq$ 250 μm x 250 μm
Power Dissipation	$\leq$ 250 μW
ΔV_{out}[2]	$\leq$ 10 mV
Radiation tolerance	500 Mrad
Power Supply	1.2 V $\pm$ 10%
Line Regulation	$\leq$ 10 %/V
Metal Routing	M1 - M4

[2]Maximum ariation between room temperature and -20 °C

2.3 Design and simulation results

This section describes the working principle of the bandgap reference. This working principle is the same for all circuits, even if the developed prototypes use three different active devices.

2.3.1 Working principle of bandgap voltage reference

The voltage across the base-emitter junction of a bipolar device or, more generally, the forward voltage of a pn-junction diode has a negative temperature coefficient (V_{BE}), called Inversely Proportional to Absolute Temperature (IPTAT) or also Complementary to Absolute Temperature (CTAT).

For a bipolar device, collector current can be expressed as:

$$I_C = I_S \exp(V_{BE}/V_T) \tag{2.2}$$

where $V_T = k_B T/q$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, q is the electron charge and I_S is the saturation current. The saturation current I_S can be expressed by the following equation:

$$I_S = bT^{(4+m)} \exp\left(\frac{-E_g}{k_B T}\right) \tag{2.3}$$

where b is a proportionally factor, m is a carrier mobility temperature coefficient ($m \approx -3/2$) and E_g is the bandgap energy in silicon. The temperature coefficient of the base-emitter voltage can be calculated by working out the derivative of the V_{BE} with respect to T. So, the base-emitter voltage can be expressed as $V_{BE} = V_T \ln(I_C/I_S)$. In order to simplify the analysis, the current I_C is held constant. Thus,

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T} \tag{2.4}$$

Deriving (2.3) with respect to T and substituting in (2.4) we get:

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \tag{2.5}$$

where the temperature dependence can be expressed as

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - E_g/q}{T} - (4+m)k_B/q \tag{2.6}$$

The CTAT temperature coefficient of the base-emitter voltage at a given temperature is shown in (2.6). With $V_{BE} \approx 750$ mV and $T = 300$ K, the Temperature Coefficient (TC) is $\frac{\partial V_{BE}}{\partial T} \approx -1.5$ mV/K.

The temperature coefficient of V_{BE}, shown in (2.6), depends on the temperature itself, determining an error in the reference generation but, in the

first order approximation, the temperature coefficient can be considered constant. Consequently, the base emitter voltage can be expressed as [36], [35]:

$$V_{BE}(T) = V_{BE0} - \beta T \tag{2.7}$$

where $\beta = \frac{\partial V_{BE}}{\partial T}$ is close to -2.2 mV/K.

A positive temperature coefficient can be obtained by means of two bipolar transistors, that have a different current density or a different base-emitter area, as shown in figure 2.9. In this case, the difference between the two V_{BE} voltages is positive.

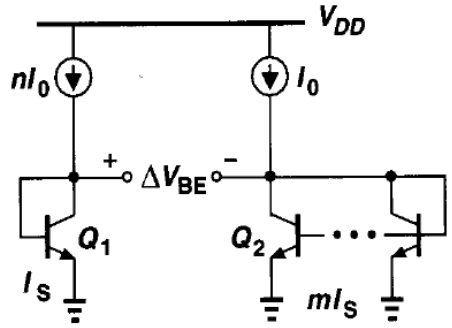


Figure 2.9: generation of positive TC.

Consider, for example, figure 2.9. If the two transistors are biased with the same current ($n = 1$), then the difference of the two base-emitter voltages can be expressed as:

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \tag{2.8}$$

$$= V_T \ln \frac{I_O}{I_{S1}} - V_T \ln \frac{I_O}{mI_{S2}} \tag{2.9}$$

$$= V_T \ln(m). \tag{2.10}$$

Thus, ΔV_{BE} is the thermal voltage multiplied by a factor $\ln(m)$. The derivative of ΔV_{BE} with respect to the temperature will be positive, as shown in(2.11)

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k_B}{q} \ln(m). \tag{2.11}$$

A bandgap reference circuit, whose block diagram is shown in figure 2.10, should be designed in such a way that the overall temperature coefficient is zero. Such TC can be obtained by the sum of positive TC and negative TC. As shown in figure 2.10, the thermal voltage is multiplied by a factor K, so that the output voltage V_{REF} can be expressed as:[36].

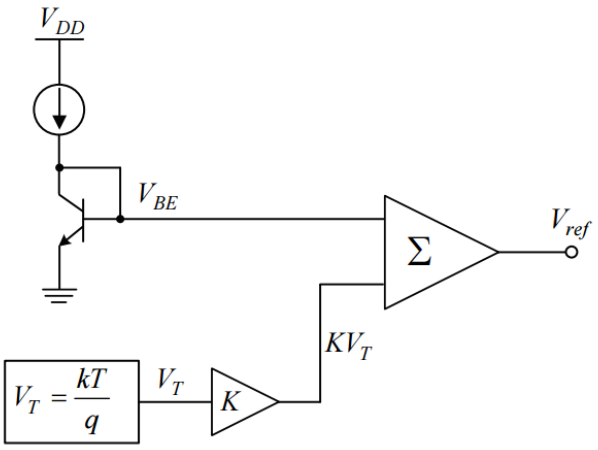


Figure 2.10: block diagram of the bandgap voltage reference.

$$V_{REF} = V_{BE} + KV_T \tag{2.12}$$

The output voltage reference is, therefore obtained as the sum of a PTAT voltage and a CTAT voltage.

The design of the Bandgap in current mode (CM) approach is useful to overcome the issue of the low power supply voltage in deep sub-micron CMOS technologies. The schematic of the bandgap voltage reference (BGR) is shown in figure 2.11. The current I_3 in the output branch is equal to I_2 by means of the current mirror. So, the current I_2 is obtained by the sum of two contributions: I_{2a} and I_{2b}. The first term is inversely proportional to the absolute temperature, while the second one increases with temperature. It is possible to obtain $dI_3/dT \approx 0$ by properly choosing N, R1, R2, where N is the emitter ratio of Q2 and Q1.

V_A and V_B are kept equal by the op-amp. The current flowing through resistor R_1, called I_{1a}, is equal to $\frac{V_A}{R_1}$, where the voltage V_A is the emitter-base voltage in the BGR version with bipolar transistors, or the anode to cathode voltage in the BGR with diodes (not shown here). The emitter-base voltage is a CTAT voltage ($V_{EB}(T)$) and can be expressed in a simplified form as [35]:

$$V_{EB}(T) = V_{EB0} - \beta T \tag{2.13}$$

consequently the current I_{1a} is CTAT, as shown by the following equation:.

$$I_{1a} = \frac{V_{EB}(T)}{R_1} = \frac{V_{EB0} - \beta T}{R_1} \tag{2.14}$$

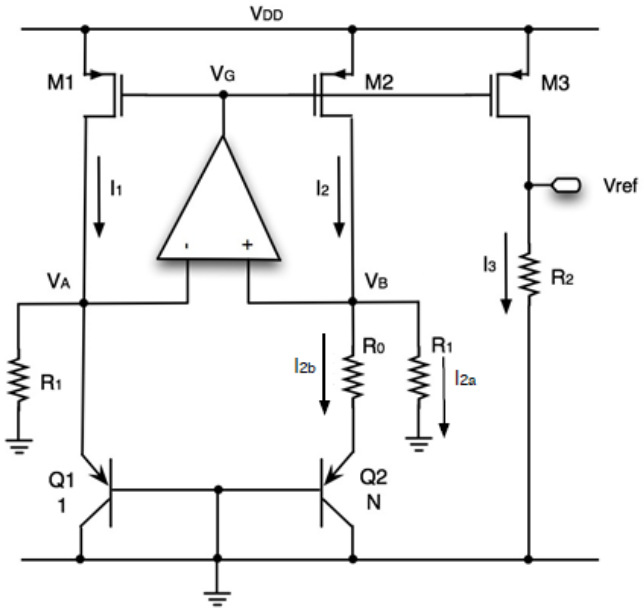


Figure 2.11: schematic of the current mode bandgap voltage reference based on bipolar devices.

The current I_2 in the node V_B is the sum of I_{2a} and I_{2b}, where I_{2a} is also a CTAT current, because the node V_B is equal to V_A. I_{2b} is instead a PTAT current, as shown by the following equation:

$$I_{2b} = \frac{k}{q} T \ln(N) \frac{1}{R_0}. \tag{2.15}$$

So, the current I_2 can be expressed as

$$\begin{aligned} I_2 =& I_{2a} + I_{2b} = \frac{V_{EB}(T)}{R_1} + \frac{k}{q} T \ln(N) \frac{1}{R_0} \\ =& \frac{V_{EB0} - \beta T}{R_1} + \frac{k}{q} T \ln(N) \frac{1}{R_0} \end{aligned} \tag{2.16}$$

N, R_0 and R_1 can be chosen in such a way to minimize the sensitivity of the current I_2 to temperature variations, i.e., in such a way to minimize the derivative of I_2 with respect to temperature:

$$\begin{aligned}
&\frac{dI_2}{dT} \approx 0 \\
&\frac{d}{dT}\left(\frac{V_{EB0} - \beta T}{R_1} + \frac{k}{q} T \ln(N) \frac{1}{R_0}\right) \approx 0 \\
&\frac{-\beta}{R_1} + \frac{k}{q} \ln(N) \frac{1}{R_0} \approx 0
\end{aligned} \tag{2.17}$$

From (2.17), I_2 sensitivity to temperature is minimized when

$$\frac{R_0}{R_1} = \frac{\frac{k}{q} \ln(N)}{\beta} \tag{2.18}$$

The current I_2 is mirrored in the output branch by M_3 transistor, as shown in figure 2.11. Thus, the output voltage can be expressed as

$$V_{REF} = \left[\frac{V_{EB}(T)}{R_1} + \frac{kT}{qR_0} \ln(N)\right] R_2 \tag{2.19}$$

2.3.2 Current mode bandgap reference based on MOS biased in weak inversion region

The evolution of the CMOS technology with a reduction of the gate-oxide thickness, combined with special layout techniques (i.e., enclosed layout), has led to design circuits with high inherent tolerance to ionizing radiation. This is in particular due to the reduction of the gate-oxide thickness to about 2 nm or below [20]. Indeed, CMOS technology has better performance, in terms of radiation hardness, than parasistic transistors and parasistic diodes, as provided by the foundry in the same process. Such devices are sensitive to TID effects related to ionizing radiation and, furthermore, they are affected by bulk damage due to neutrons, highly energetic electrons and ions. For this reason, the use of CMOS devices in sub-threshold region or of Dynamic Threshold NMOS (DTNMOS) as active elements has already been proposed for applications in harsh radiation environment [32].

Gate-to-source voltage as a function of the temperature

A MOS that is biased in weak inversion region (or sub-threshold) and in saturation condition ($V_{DS} > 3V_T$) has a similar characteristic as that of bipolar transistor, in which the drain current varies exponentially with the gate-to-source voltage. The drain current can be expressed by the following equation:

$$I_D(V_{GS}, T) = \mu(T) C_{OX} \frac{W}{L} V_T^2 \exp \frac{[V_{GS} - V_{Th}(T)]}{nV_T} \tag{2.20}$$

where n is the slope factor and μ is the mobility. The MOS parameters, such as threshold voltage and carrier mobility, are strongly affected by temperature. In particular, the threshold voltage as a function of the temperature can be expressed by a linear equation: $V_{Th}(T) = V_{Th}(T_0) - k_4(T - T_0)$, while the carrier mobility can be expressed by the following equation:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{2.21}$$

where k_4 and m are technology parameters, with $1 \leq m \leq 2$ [37]. Substituting (2.21) in (2.20), the gate-to-source voltage can be expressed as [49]:

$$V_{GS} = V_{Th} + nV_T \ln\left[\frac{I_{DS}L}{n\mu(T_0)(T/T_0)^{-m}C_{OX}WV_T^2}\right] \tag{2.22}$$

Assuming that the current is constant and m=2, then the gate-to-source voltage can be differentiated with respect to temperature, resulting in following equation [37]:

$$\frac{\partial V_{GS}}{\partial T} = \frac{\partial V_{Th}}{\partial T} + \frac{nk_B}{q}\ln\left[\frac{I_{DS}LT_0^2}{n\mu(T_0)C_{OX}WV_T^2}\right] \tag{2.23}$$

The argument of the logarithm is less than 1, thus the second term is negative. Moreover, the temperature coefficient of the threshold voltage is also negative, as shown before. The gate-to-source voltage has, therefore, a negative temperature coefficient (TC).

Current mode bandgap based on MOS in sub-threshold region

The current mode bandgap voltage reference based on MOS in sub-threshold region has the same architecture described in section 2.3.1. The schematic is shown in figure 2.12. In this case, the active elements are two MOS transistors in weak inversion region.

The output voltage of this BGR, after a similar analysis as for the previous versions, can be expressed by the following equation [38]:

$$V_{REF} = \left[\frac{V_{GS}(T)}{R_1} + \frac{kT}{qR_0}\ln N\right]R_2 \tag{2.24}$$

where V_{GS} is the gate-to-source voltage of the active element (i.e., MOS in weak inversion) and N is the multiplicity factor.

2.3.3 Design of the operational amplifier

The operational amplifier senses V_A and V_B, driving the gate voltage of M_1 and M_2 transistors such that V_A and V_B settle to an approximately equal voltage. Equation (2.24) is valid in an ideal scenario, when resistors are

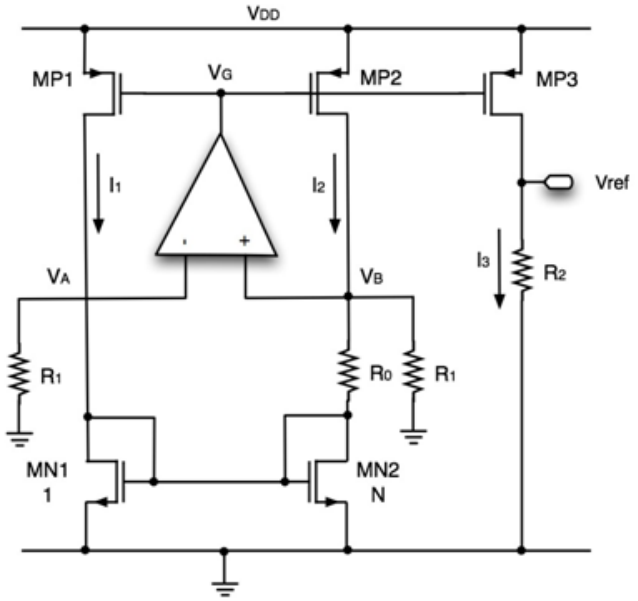


Figure 2.12: schematic of the current mode bandgap voltage reference based on MOSFETs in sub-threshold region.

perfectly matched and the operational amplifier has infinite gain and zero offset voltage. In particular, when the offset voltage (V_{OS}) is present, such voltage is amplified, introducing an error in the I_2 current, as shown in the following equation:

$$I_2 = \frac{V_A}{R_1} + \frac{kT}{qR_1}\ln(N) - V_{OS}\left(\frac{1}{R_2} + \frac{1}{R_1}\right) \tag{2.25}$$

The main contribution to the offset voltage in a operational amplifier is due to threshold voltage mismatch between the transistors of the input differential pair. The operational amplifier has been designed with large devices so as to minimize the input offset, which depends on mismatch $\sigma_{V_{Th}}$ [39], [40].

$$\sigma_{V_{Th}} = \frac{A_{VT}}{\sqrt{WL}} \tag{2.26}$$

The common-mode input voltage is $V_A \approx 0.65$ V of the operational amplifier for the BGR with bipolar transistors and diodes, while $V_A \approx 0.3$ V for the BGR based on MOSFET in weak inversion region.

The architecture for the opamp is a two stage Miller OTA, as shown in figure 2.13. The input differential pair is p-type in order to ensure that the transistor (M_5) providing the tail current to the stage remains in the

saturation region. Indeed, the input common mode voltage tends to decrease when the temperature raises.

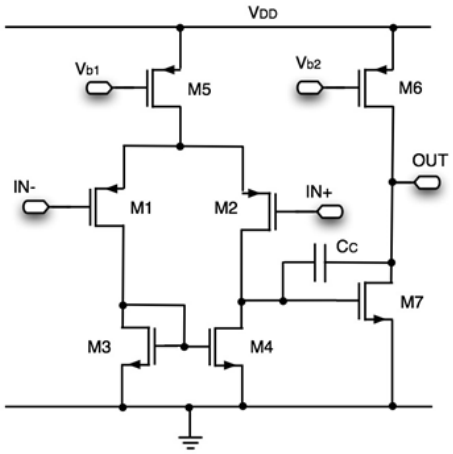


Figure 2.13: schematic of the proposed operational amplifier.

The operational amplifier is designed in order to hit a DC gain A_0 greater than 60 dB and a phase margin greater than 60 deg. In order to minimize the power dissipation of the bandgap, the operational amplifier has been biased with a DC current close to about 1 μA. Moreover, an operational amplifer with PMOS transistors as differential input pair guarantees better performance, if compared with the NMOS input version, especially in terms of flicker noise (the bandgap reference circuit works at low frequency)[41],[39]. In figure 2.14, the open loop frequency response of the operational amplifier is shown, while in table 2.2, the main parameters of the operational amplifier as a function of the temperature are listed.

Table 2.2: main parameters as a function of the temperature.

Temperature [deg C]	DC gain [dB]	GBW [kHz]	ϕ_M [deg]
-50	69.8	62	61
0	68.4	144	66
27	67.6	176	67
50	66.9	200	68
100	64.9	243	70
150	61.5	269	72

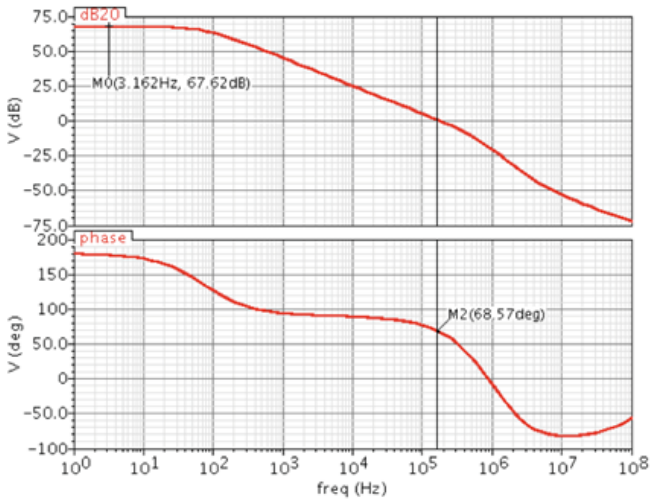


Figure 2.14: open-loop frequency response of the operational amplifier at room temperature.

2.3.4 Startup circuit

The bandgap reference circuit exhibits two possible operating points: the typical working condition and an operating point where no current flows in the bandgap ($V_A = V_B = 0$ V). A startup circuit is therefore needed to ensure that, after power up, the BGR finds itself in the nominal operating condition. In figure 2.15, the bandgap reference with the startup circuit is shown[42].

During power on, a current starts charging C_1. The same current is mirrored from M_{11} to M_{10}. In this way, the current in M_{10} charges the gate of M_{13}, turning M_{13} on. M_{13} pulls down the gate of the PMOS current mirror (VG), injecting current into $Q1$ and $Q2$ transistors. After startup, M_{14} is turned on, then M_{13} is switched off. When C_1 is charged at one threshold below the power supply voltage, M_{10} and M_{11} are cutoff and the power consumption of the startup circuit is zero. M_{12} discharges C_1 when the supply is switched off.

2.3.5 Bandgap voltage reference

The main parameter used to evaluate the performance of the bandgap reference is the temperature coefficient TC, which can be calculated as

$$TC = 10^6 \frac{\Delta V_{REF}}{\Delta T \cdot V_{REF_{MIN}}} \text{ [ppm/K]} \tag{2.27}$$

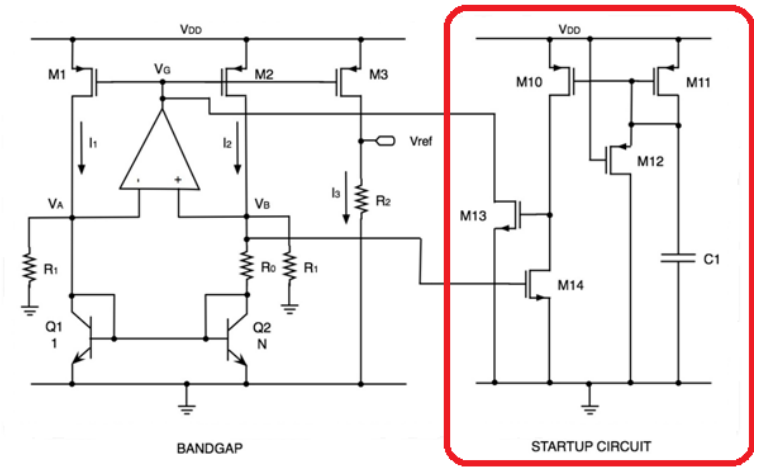


Figure 2.15: schematic of the proposed startup circuit.

Another important parameter is the line regulation defined as the capability to maintain a constant output voltage level, despite variations in the power supply. It can be defined as

$$LR = \frac{\Delta V_{REF}}{V_{REF}} \cdot \frac{1}{\Delta V_{DD}} \cdot 100 \ [\%/\text{V}] \tag{2.28}$$

Finally, the power supply rejection (PSR) is defined as the capability of the circuit to reject noise coming from the supply line. The PSR is defined as:

$$PSR = 20 \cdot \log\left(\frac{v_{REF}}{v_{DD}}\right) \tag{2.29}$$

where v_{DD} is a superimposed noise and/or signal in the power supply line, while v_{REF} si the small signal at the output node of the BGR[43].

Simulation results for the bandgap reference circuit based on bipolar transistors

The bandgap reference based on bipolar devices (the schematic is shown in figure 2.11) has been simulated in a temperature range between -50 °C and 150 °C. The nominal output voltage at room temperature (300 K) is 707.5 mV. The simulated temperature coefficient of $TC = 5.2$ ppm/K was obtained. The BGR output voltage as a function of the temperature is shown in figure 2.16.

The simulated line regulation is $LR \approx 0.4$ %/V. The single bipolar transistor (Q_1) is biased with a current of 7 μA, instead the bipolar transistor Q_2 is composed by 24 single devices. Each bipolar transistor is biased with the same current as Q_1. The total dissipation of the overall circuit is close

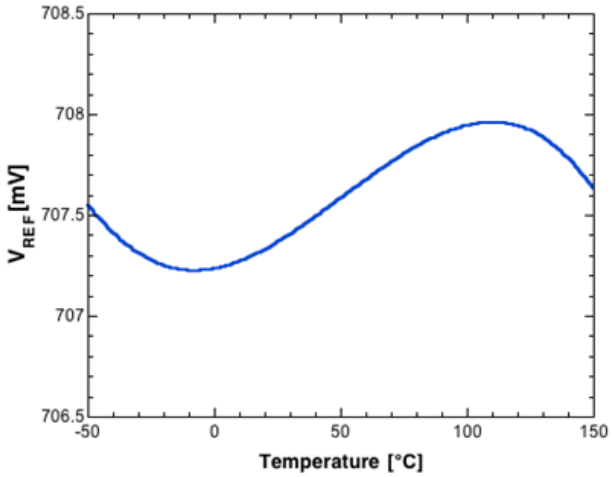


Figure 2.16: voltage at the output of the BGR based on bipolar devices simulated in nominal condition.

to 105 μW. Also, the simulated power supply rejection is close to -28.55 dB at 1 kHz. The PSR as a function of the frequency is shown in figure 2.17.

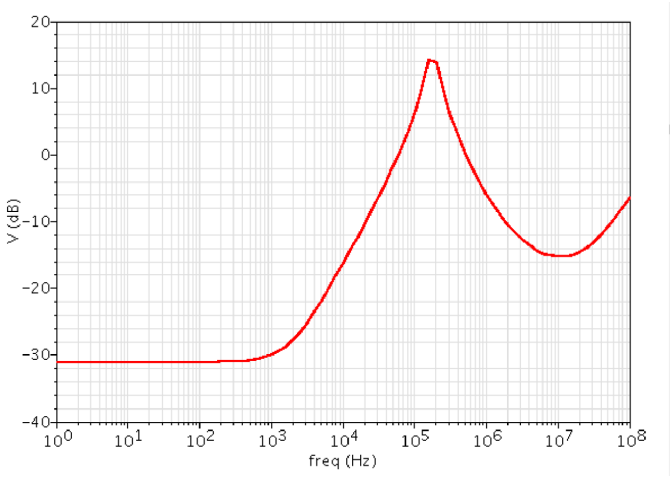
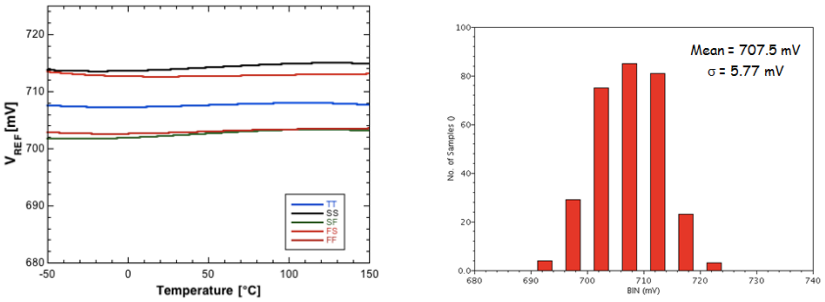


Figure 2.17: simulated PSR for the bandgap reference circuit based on bipolar devices.

In order to fully characterize the reference circuit performance, the BGR schematic has been also simulated with process and mismatch variations. These simulations are used to asses the robustness of the circuit against manufacturing process variations. Figure 2.18a shows the output voltage



(a) (b)

Figure 2.18: (a) four corners simulations and (b) Monte Carlo simulation for the bandgap reference circuit based on bipolar devices.

Table 2.3: output voltage and temperature coefficient of the bandgap based on bipolar transistors from four corner simulations.

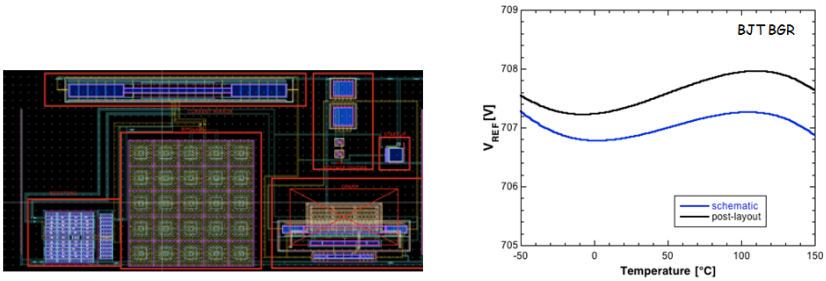
Corners	Output Voltage Reference [mV]	TC [ppm/K]
FF	702.8	6.9
FS	712.6	5.9
SF	702.2	11.8
SS	713.9	10.2
TT	707.5	5.2

in the four process corners (SS, SF, FS, FF), while in figure 2.18b, the results from the Monte Carlo simulations (including process and mismatch variations) for the output voltage at room temperature are shown. The average of the output voltage is $\mu_{V_{Out}} = 707.5$ mV with a standard deviation $\sigma_{V_{Out}} = 5.8$ mV, so that the maximum deviation, defined as($\pm 3\sigma/\mu$,is ± 2.5 %). In table 2.3, the TC and the output voltage for the four-corners simulations are shown.

The layout has an area close to 260 μm x 120 μm. In figure 2.19a, the proposed layout for this bandgap version is shown, while figure 2.19b shows the comparison between pre and post layout simulations.

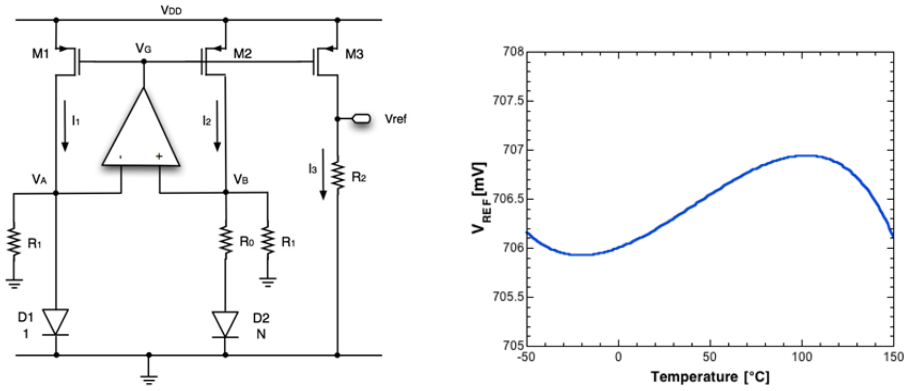
Simulation results for the bandgap reference circuit based on diodes

The schematic of the bandgap based on diode is shown figure 2.20a. The diode is obtained with junction composed by P^+ and NW (n-well). This solution has an output voltage of $V_{REF} = 706.3$ mV at room temperature and a temperature coefficient: $TC = 7.2$ ppm/K in a temperature range from -50 °C to 150 °C. The output voltage (V_{REF}) as a function of the temperature is shown in figure 2.20b. Table 2.4 shows the simulation results in nominal conditions.



(a) (b)

Figure 2.19: (a) proposed layout and (b) comparison between pre and post layout simulations of the bandgap reference with bipolars transistors.



(a) (b)

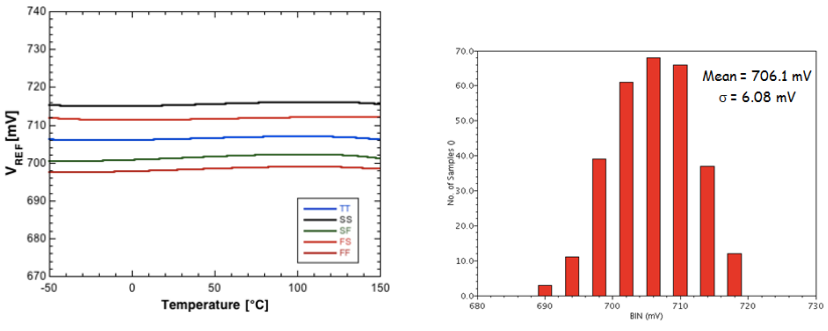
Figure 2.20: (a) schematic and (b) output voltage as a function of the temperature in nominal conditions for the bandgap reference circuit based on diode devices.

The simulation results for the output voltage in the four process corners (SS, SF, FS, FF) is shown in figure 2.21a, while the histogram resulting from the Monte Carlo simulation (including process and mismatch variations) for the output voltage at room temperature is shown in figure 2.21b. The average value of the output voltage is $\mu_{V_{REF}} = 706.1$ mV. The standard deviation is $\sigma_{V_{REF}} = 6.1$ mV, thus the maximum deviation, calculated as $\pm 3\sigma/\mu$ is ± 2.6 %. The TC and the output voltage for the four corner simulations are shown in table 2.5.

The proposed layout for this bandgap version is shown in the figure 2.22a, while the comparison between pre and post layout simulations is shown in figure 2.22b. The layout has an area close to 240 μm x 110 μm.

Table 2.4: simulations results in nominal conditions for the bandgap based on diode devices.

Parameters	Values
Line Regulation (LR)	0.6 %/V
Total Power Dissipation	103 μW
Power Supply Rejection	-33 dB at 1 kHz



(a) (b)

Figure 2.21: (a) output voltage as a function of the temperature as obtained from four corners simulations and (b) Monte Carlo simulation results for the bandgap based on diodes.

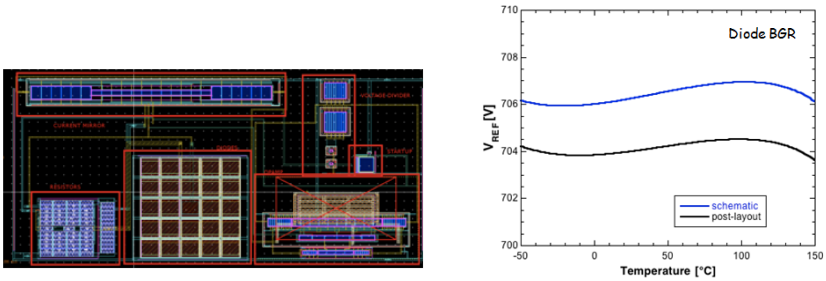
Table 2.5: simulations results from four corner simulations for the bandgap based on diode devices.

Corners	Output Voltage Reference [mV]	TC [ppm/K]
FF	698.1	10.3
FS	711.4	5.8
SF	701.2	12.7
SS	715.2	8.12
TT	706.3	5.2

Simulation results for the bandgap based on MOSFET

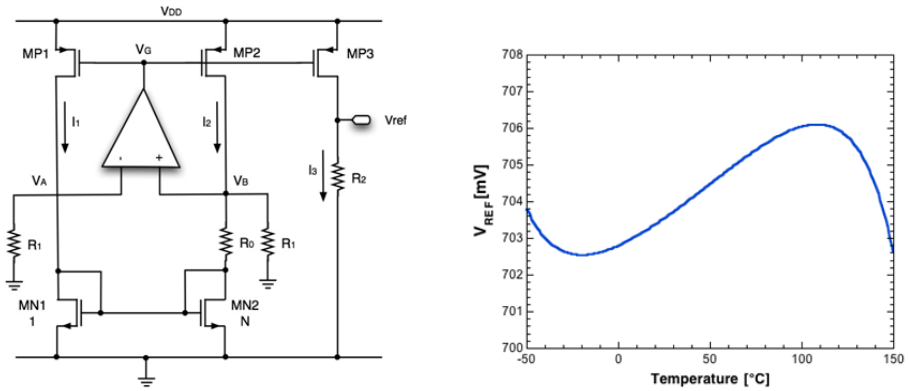
This third solution of bandgap voltage reference, based on enclosed-layout MOSFETs biased in weak inversion region, is the most promising in terms of radiation tolerance and also a better solution in terms of power dissipation, thanks to the sub-threshold voltage operating point of the devices.

This kind of bandgap reference circuit has a simulated output voltage $V_{REF} = 703.6$ mV and a temperature coefficient $TC = 25$ ppm/K. The schematic of the proposed BGR is shown in the figure 2.23a. The total power dissipation is close to 47 μW. In figure 2.23b, the output voltage as



(a) (b)

Figure 2.22: (a) layout and (b) comparison between pre and post layout simulations for the bandgap with diodes.



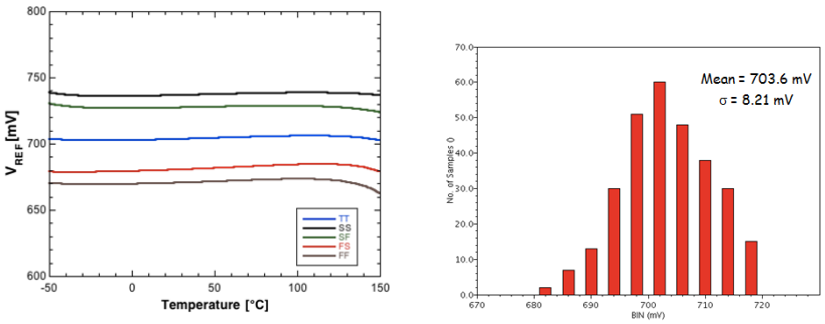
(a) (b)

Figure 2.23: (a) schematic of the bandgap based on MOS in sub-threshold region and (b) output voltage as a function of the temperature in nominal conditions.

a function of the temperature is shown, while the simulated line regulation is $LR = 2$ %/V.

The output voltage from four corner simulations is shown in figure 2.24a, while the figure 2.24b shows the histogram of the Monte Carlo simulations for the output voltage at room temperature. The average value of the output voltage is $V_{REF} = 703.6$ mV and the standard deviation is $\sigma_{V_{REF}} = 8.2$ mV, with a maximum deviation of ± 3.5 %. Table 2.6 summarizes the TC and output voltage for the four corners simulations.

The layout has an area close to 240 μm x 110 μm. Figure 2.25a shows the proposed layout, whereas the comparison between pre and post layout simulations is shown in 2.25b.

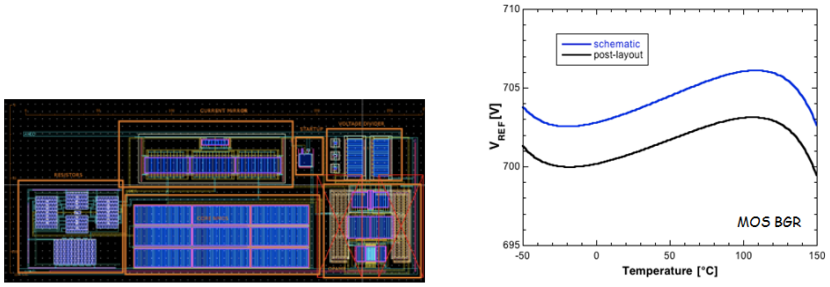


(a) (b)

Figure 2.24: (a) output voltage for four corners simulations and (b) Monte Carlo simulations for the bandgap output voltage at room temperature.

Table 2.6: four corners simulation results for the bandgap based on MOS in weak inversion region.

Corners	Output Voltage Reference [mV]	TC [ppm/K]
FF	670.6	81.6
FS	680.5	43.7
SF	727.4	6.7
SS	736.8	18.43
TT	703.6	25.32



(a) (b)

Figure 2.25: (a) layout and (b) comparison between pre and post layout simulations for the bandgap based on MOS devices

2.3.6 Design of the second version of the bandgap voltage reference

A second version of the bandgap voltage reference circuits based on NMOS with enclosed layout and biased in sub-threshold region has been designed with some improvements. The performance of the circuit, in terms of output

voltage, is degraded by process and mismatch fluctuations in the resistor values. In order to mitigate this effect, the resistor R_0 has been replaced with a programmable resistor[44]. The trimming resistor has been designed to correct up to ± 20 % variations in the value of R_0. A 5 bit signal is used to control the state of the switches and to trim the value of the resistor [24].

In the new BGR version, the DC biasing current of the bandgap is also increased in order to mitigate the TID effects. The biasing current has been increased by a factor of 5. The rms integrated noise from 0.01 Hz to 100 MHz is about 410 μV and the power consumption is 180 μW. The maximum output deviation is ± 4.2 % due to mismatch and process fluctuations. This result is obtained when the programmable resistor is configured in order to minimize the temperature coefficient. Figure 2.26 shows the simulated output voltage of the bandgap reference as a function of the temperature for the 32 possible combinations of the trimming resistor.

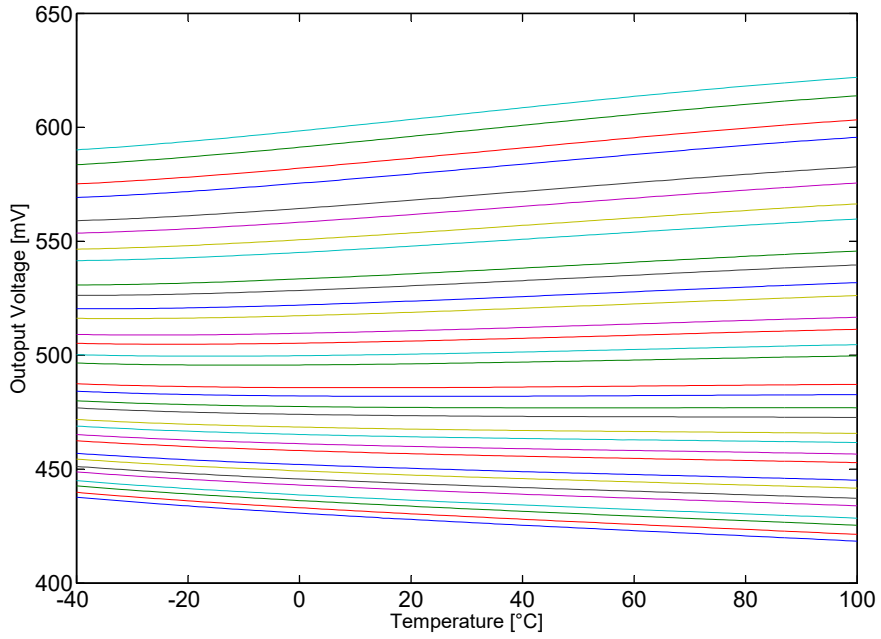


Figure 2.26: output voltage vs. temperature for the 32 possible values of R_0.

2.4 Characterization and irradiation results

The bandgap circuits have been characterized in a climatic chamber in order to evaluate the stage behaviour as a function of the temperature [45]. Then, the circuits have been exposed to ionizing radiation in order to evaluate the radiation tolerance. In this section, the relevant results will be presented and discussed.

2.4.1 Characterization and irradiation results of the first prototype of bandgap voltage reference

The measurements as a function of the temperature have been carried out by means of a climatic chamber at INFN - Milano, while the irradiation tests were performed at Laboratori Nazionali di Legnaro (Italy) with an X-ray machine at a dose rate of about 1 krad(SiO_2)/s. During irradiation, the bandgap circuits were biased as in the real application.

Pre-irradiation results

In the case of the bandgap based on bipolar devices, measurement results show a variation as low as ±3.4 mV over a temperature range of 170 °C (−30 °C to 140 °C). Figure 2.27 shows the output voltage as a function of the temperature. The output voltage at room temperature is 698.7 mV with a temperature coefficient: $TC = 57$ ppm/K.

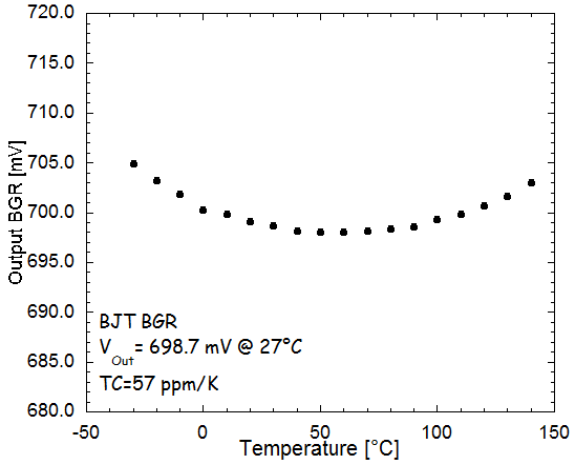
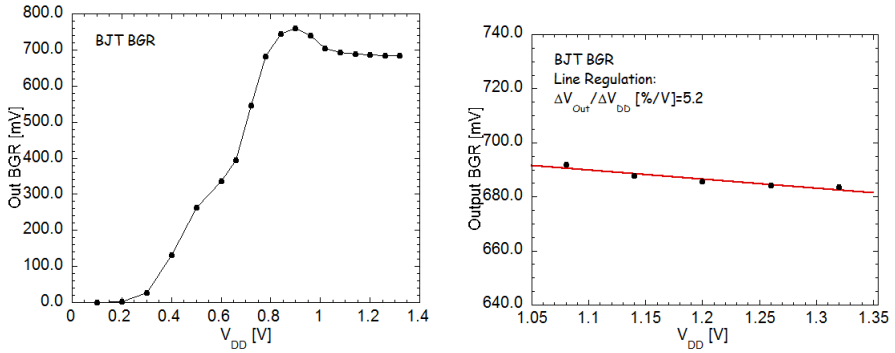


Figure 2.27: measurement of the output voltage vs. temperature for the bandgap based on bipolar transistors.

Figure 2.28a shows the output voltage as a function of the power supply.

The minimum power supply[3], defined as $V_{REF} + V_{SD3_{sat}}$ is close to 0.9 V, where $V_{SD3_{sat}}$ is the saturation voltage of the pMOS in the output branch [46], [47]. The line regulation (Fig. 2.28b) is 5.2 %/V at room temperature. The output voltage, for 26 samples on the same wafer, is 691.5 mV±14.7 mV (3σ).



(a) (b)

Figure 2.28: (a) output voltage of the bandgap vs power supply and (b) line regulation for the bandgap based on bipolar devices.

Table 2.7 shows the measured main parameters (before irradiation) for the bandgap reference circuit based on diode devices. Figure 2.29 shows the output voltage as a functions of the temperature.

Table 2.7: main parameters (before irradiation) for the bandgap reference circuit based on diode devices.

Parameters	**Values**
Temperature range	−30 °C to 140 °C
Output voltage at room temp.	695.1 mV
Variation	±4.5 mV
Temperature Coefficient (TC)	76 ppm/K.

Figure 2.30a shows the output voltage as a function of the power supply. The minimum power supply is close to 0.9 V and the line regulation (Fig. 2.30b) is 1.1 %/V at room temperature. The output voltage, for 26 samples on the same wafer, is 697.9 mV ± 26.7 mV (3σ).

The last circuit is the bandgap reference based on MOS in sub-threshold region. The variation of the output voltage is ±12.1 mV over a temperature range of 170 °C (−40 °C to 130 °C). Figure 2.31 shows the output voltage as a function of the temperature. The output voltage at room temperature

[3]The minimum power supply is the intersection point between the two straight lines interpolating the points included in the ranges 0.2 V - 0.7 V and 1.0 V - 1.4 V

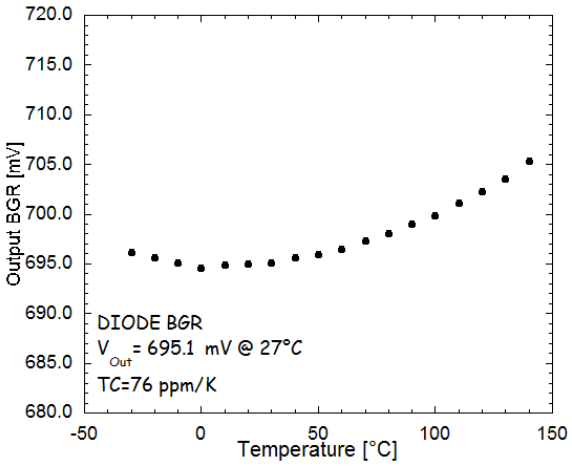
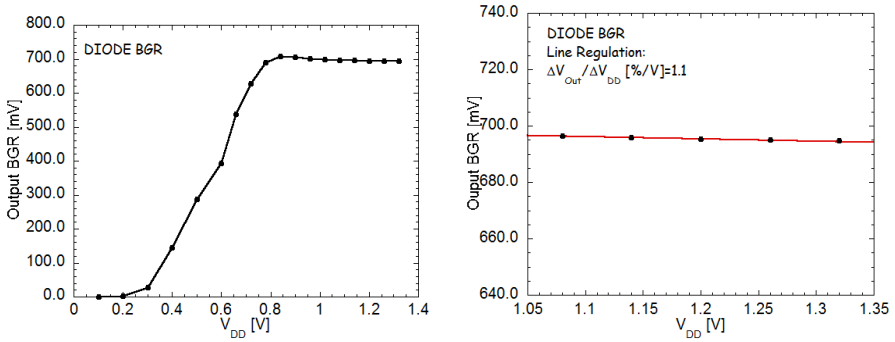


Figure 2.29: output voltage vs. temperature for the bandgap based on diode.



(a) (b)

Figure 2.30: (a) output voltage as a function of the power supply and (b) line regulation of the bandgap based on diode devices.

is 665.1 mV with a temperature coefficient $TC = 201$ ppm/K. The output voltage as a function of the power supply is shown in figure 2.32a. The minimum power supply is close to 0.9 V. The line regulation (Fig. 2.32b) is 3.6 %/V at room temperature. The output voltage, for 26 samples on the same wafer, is 662.9 mV $\pm$ 30.75 mV (3σ).

The main parameters of the bandgap reference circuits (i.e., based on bipolar transistors, diodes and MOS devices) are summarized in table 2.8.

Both the temperature coefficient (TC) and the line regulation (LR) measured experimentally are much worse than the simulated values. This difference could be ascribed to a poor modelization of the transistor behaviour with respect to temperature. Moreover, in this version, the variation of the

process parameters cannot be compensated by a trimming of the bandgap parameters.

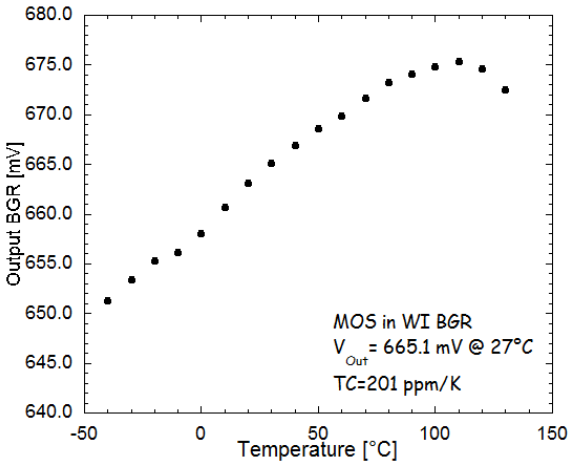
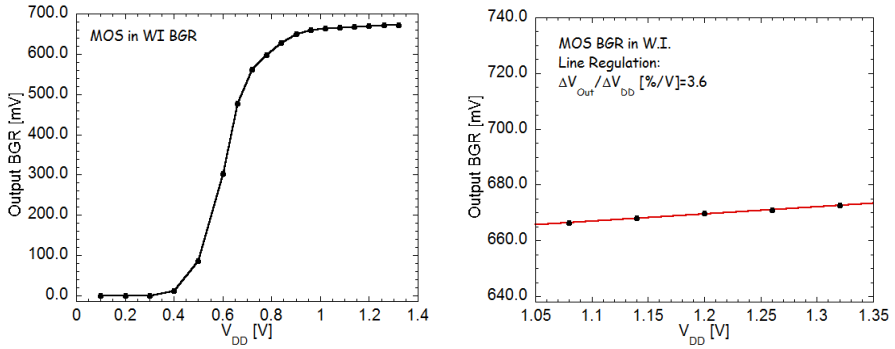


Figure 2.31: output voltage vs. temperature for the bandgap based on MOS devices in weak inversion.



(a) (b)

Figure 2.32: (a) output voltage vs power supply and (b) line regulation for the bandgap based on MOS transistors.

Table 2.8: main parameters (before irradiation) for the bandgap reference circuits.

	Parameter	value
Bipolar	Temperature range	−30 °C to 140 °C
	Output voltage at room temp.	698.7 mV
	Variation	±3.4 mV
	Temperature Coefficient (TC)	57 ppm/K
	Minimum power supply	0.9 V
	Line Regulation	5.2 %/V
	$\mu \pm 3\sigma$ (26 samples)	691.5 mV ± 14.7 mV
Diode	Temperature range	−30 °C to 140 °C
	Output voltage at room temp.	695.1 mV
	Variation	±4.5 mV
	Temperature Coefficient (TC)	76 ppm/K
	Minimum power supply	0.8 V
	Line Regulation	1.1 %/V
	$\mu \pm 3\sigma$ (26 samples)	697.9 mV ± 26.7 mV
MOS	Temperature range	−30 °C to 140 °C
	Output voltage at room temp.	665.1 mV
	Variation	±12.1 mV
	Temperature Coefficient (TC)	201 ppm/K
	Minimum power supply	0.8 V
	Line Regulation	3.6 %/V
	$\mu \pm 3\sigma$ (26 samples)	662.9 mV ± 30.8 mV

Irradiation Results

Irradiation tests have been carried out taking into account the severe requirements set for phase 2 upgrades of the LHC experiments. The devices were irradiated at Laboratori Nazionali di Legnaro (Italy), with 10 keV X-rays up to an integrated dose of 225 Mrad(SiO_2). Figure 2.33 shows the output variation as a function of the dose. A significant variation can be detected for the diode and bipolar based bandgap references. This result is due to an increase of the leakage current in the diode and in the bipolar devices. Such effect is due to the irradiation induced holes get trapped in the body of the field oxide near the SiO_2 – Si interface [33]. In fact, a shallow trench isolation (STI) field oxide layer is usually placed surrounding the p^+ diffusion region, which is the emitter of the pnp transistor. The charge trapped results in an increase of the base leakage current which degrades the current gain of the bipolar transistor. A limited recovery can be observed after the annealing process (after 7 days at room temperature). The bandgap reference based on MOS in sub-theashold region has good perfor-

mance in terms of radiation hardness. A modest variation, about 1.1 %, is observed in bandgap circuits based on N-MOSFETs [48]. The maximum voltage shift is less than 10 mV with a TID up to 225 Mrad. On the other hand, this solution suffers from mismatch problems and process variation and is worse than the other two versions in terms of temperature coefficient. These problems have been addressed through the design of the bandgap reference circuit with trimming resistor, already discussed in section 2.3.6.

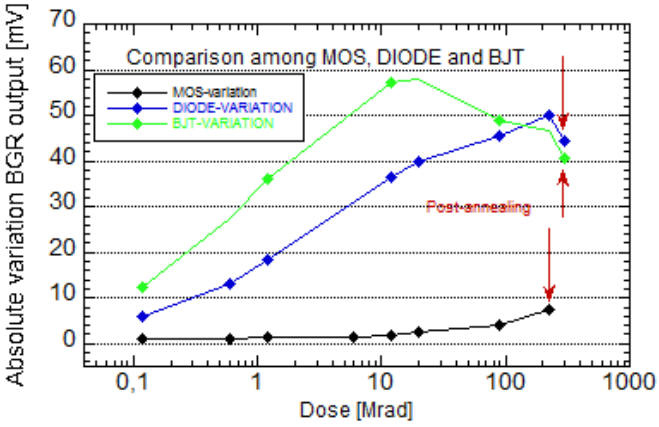


Figure 2.33: output voltage vs. TID for the three kinds of BGRs irradiated at room temperature and biased as in the real application.

2.4.2 Characterization and irradiation results for the second prototype of bandgap voltage reference

Test setup

In order to carry out automated and systematic measurements, a test system has been purposely developed. The hardware of the test system consists of two printed circuit boards (PCBs):

- **Main Board**: the *Main Board* hosts the bias circuits, supply voltage, slow control signals and configuration bits for the chip. The output of each bandgap is connected to the instrumentation by means of a 50 pin flat cable.

- **ASIC carrier**: the *ASIC carrier* hosts the prototype chip, which is directly bonded on the PCB. The ASIC carrier is plugged into the main board by means of 4 arrays of pins and placed at the edges of the board.

Figure 2.34 shows the layout of the PCB test boards. The ASIC carrier is shown at the top of the figure, whereas the main board is shown at the bottom.

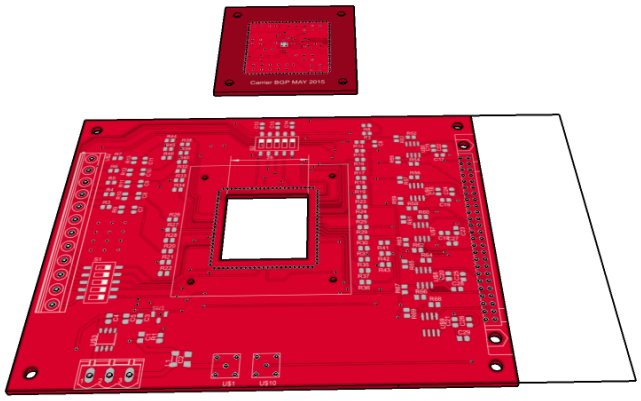


Figure 2.34: layout of the PCB test board.

As shown in figure 2.35, the test system is composed by the following blocks:

- A computer, that by running Matlab scripts, is able to control the instrumentation through a GPIB protocol and to collect data coming from the bandgap.
- A power supply that provides the 1.2V to the chip.
- A switching matrix (Tektronix K7001) that connects each bandgap output to the multimeter system.
- A multimeter (Tektronix K2000) is used to perform the measurements of the BGR output voltage. The data are sent to the PC, via GPIB, and are saved in a file.
- A DAQ board (NI USB-6008), which is connected to the PC by USB, that controls the bits of the programmable resistor in the bandgap.

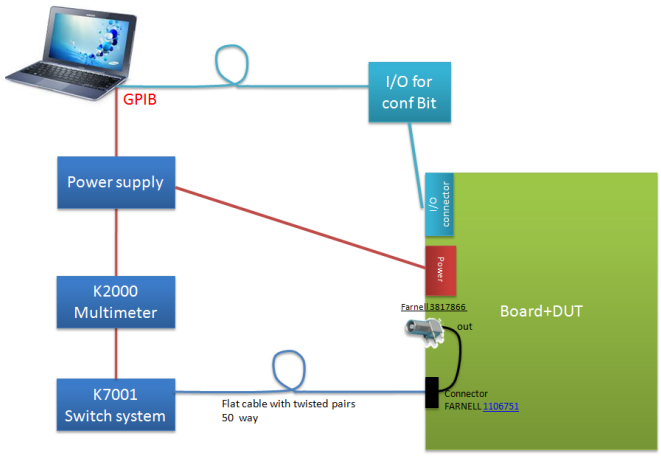


Figure 2.35: block diagram of the automated test system.

Pre-irradiation results

The second prototype of the BGR has been characterized using the climatic chamber facility at INFN-Milano. The measurements have been performed with the test setup shown in the previous section. Figure 2.36 shows the output voltage in one of the three tested chips as a function of the temperature for different configurations of the programmable resistor. The output voltage at room temperature in the best configuration (the one minimizing the TC) is $V_{OUT} = 395.1$ mV with a temperature coefficient of $TC = 18$ ppm/K in a temperature range from -40 °C to 110 °C. Figure 2.37 shows the TC as

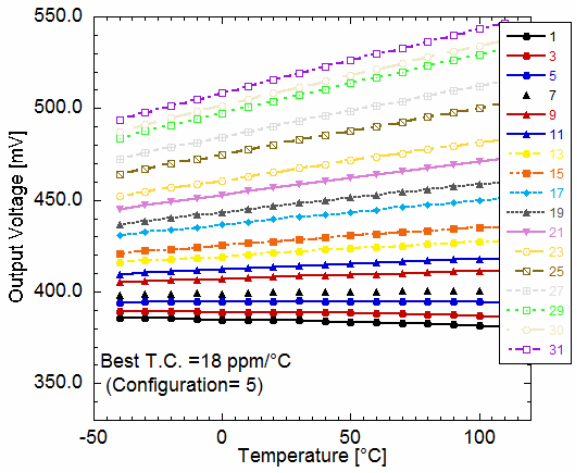


Figure 2.36: bandgap output voltage vs. temperature for different configurations of the trimming resistor.

a function of the trimmable resistor settings. The minimum TC is obtained for a configuration word equal to 5. During the characterization phase in the climatic chamber, three chips have been characterized. There is a limited process dispersion among the chips in the same wafer.

Figure 2.38 shows the output voltage as a function of the temperature (in the range $-40°C \div -110°C$) in the three chips tested in the climatic chamber. The maximum output variation is close to 2.3 mV and is detected in chip number 2. A voltage voltage drop of about 2 mV at 0 °C is apparent in two devices. The reason of this behaviour is at the moment unknown since it is not present in simulation and only three circuits have been characterized. More chips should be measured but it is worth noting that the measure of each of them in a climatic chamber requires about eight hours and the voltage drop is well below the maximum voltage variation allowed by the requirements of RD53. Table 2.9 summarizes the main parameters of the three chips. Figure 2.39a shows the output voltage as a function of the power supply for different resistor settings. Figure 2.39b shows the output voltage for the configuration minimizing the TC. In this case the line regulation is $LR = 4.2$ %/V.

Characterization results after irradiation

The second version of the bandgap has been irradiated at four different facilities, in order to assess the radiation hardness. One sample has been irradiated with the 10 keV X-ray CERN facility up to a total ionizing dose of 500 Mrad with a dose rate of 9.5 Mrad/h. The final dose is larger than the maximum dose of 500 Mrad expected for the IP in the foreseen application.

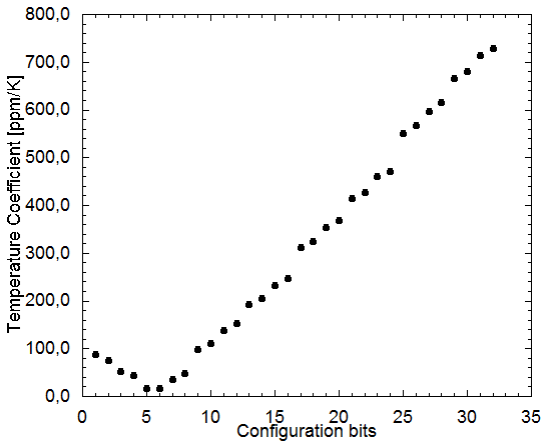


Figure 2.37: temperature coefficient vs. configuration bits.

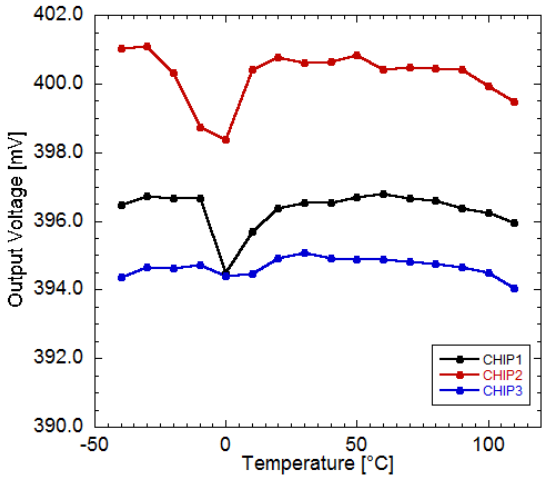
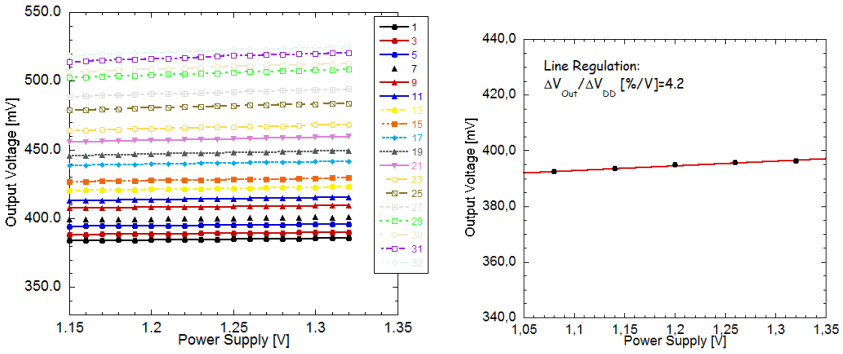


Figure 2.38: bandgap output voltage as a function of the temperature for three different chips.

Table 2.9: output voltage and temperature coefficient for the three chips tested in the climatic chamber.

Chip Number	Output Voltage Reference [mV]	TC [ppm/K]	Configuration Bits
1	396.5	39	6
2	400.6	46	6
3	395.1	18	5



(a) (b)

Figure 2.39: (a) output voltage vs. power supply and (b) line regulation for the second version of the bandgap based on MOS in sub-threshold region.

The chip, during the irradiation, was biased as in the real application. The output voltage as a function of the TID is shown in figure 2.40. Table 2.10 shows the variation of the output voltage for different TIDs. The maximum variation is close to 15% of the output voltage at room temperature. The output voltage has been monitored throughout the irradiation.

Table 2.10: variation of the bandgap output voltage in a chip exposed to 10 keV X-rays.

V_{REF} pre-rad	395.6 mV	
ΔV_{REF} at 200 Mrad	7 mV	< 2 %
ΔV_{REF} at 400 Mrad	3 mV	< 16 %
X-ray machine off	3 mV	< 1 %

The second facility is the CN accelerator at Laboratori Nazionali di Legnaro (LNL, Padova, Italy) where other two chips have been irradiated. The facility may produce 3 MeV protons, which can induce both displacement damage in the bulk and ionization effects. The chips have been irradiated at room temperature and biased as in the real applications. The samples have absorbed a total fluence of $5 \cdot 10^{15}$ (1MeV)n.eq/cm^2 and a TID of 500 Mrad. One of the two chips was damaged during irradiation and could not be tested after the irradiation procedure. The radiation induced variation of the output voltage as a function of the configuration bits for the second sample is shown in figure 2.41. The maximum shift of the output voltage for the best configuration bits, which minimizes the temperature coefficient, is 6.2 mV. Other samples were also irradiated with 10 MeV protons at the TANDEM accelerator, also in Legnaro. In this case, three different chips have been irradiated at different fluences and TIDs. The first one has been irradiated at a fluence of $2.1 \cdot 10^{15}$ n.eq/cm^2 and at a TID of 300 Mrad, the second one at $4.5 \cdot 10^{15}$ n.eq/cm^2 and 650 Mrad and the last one at

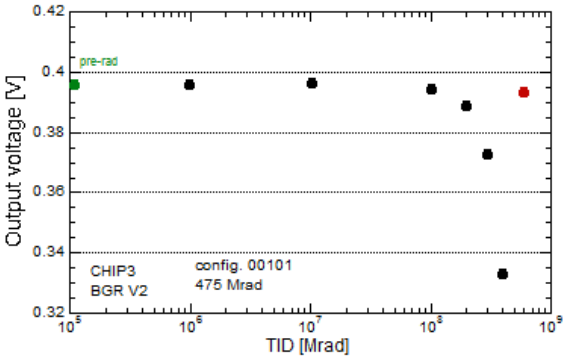


Figure 2.40: output voltage as a function of the dose in the sample irradiated with 10 keV X-rays.

$5.5 \cdot 10^{15}$ n.eq/cm^2 and 800 Mrad respectively. The three chips were unbiased during the exposure. As shown in figure 2.42, the maximum shift between pre and post irradiation conditions is less than 25 mV in the best configuration. Table 2.11 summarizes the variation of the bandgap output voltage irradiated at the TANDEM accelerator.

Table 2.11: variation of the bandgap output voltage with 10 MeV protons at the TANDEM accelerator (Legnaro).

TID and Fluence	ΔV_{REF}
300 Mrad and $2.1 \cdot 10^{15}$ n.eq/cm^2	5 mV
650 Mrad and $4.5 \cdot 10^{15}$ n.eq/cm^2	11 mV
800 Mrad and $5.5 \cdot 10^{15}$ n.eq/cm^2	21 mV

The last facility used to irradiate the second version of the bandgap voltage reference is the neutron irradiation facility in Ljubljana. Two samples were irradiated at room temperature and unbiased. The final fluence was $2 \cdot 10^{15}$ n.eq/cm^2. The output variation for the first chip is 2.5 mV, while the variation in the second chip is 1.9 mV. Figure 2.43a and 2.43b show the output voltage as a function of the configuration bits, before and after irradiation, for the two devices under test. In conclusion, the variation of the output voltage due to the exposure to radiation is within specifications, demonstrating the possibility to use the designed IP block in the pixel front-end chip for the HL-LHC experiments.

The main performance are summarized in Table 2.12 together with a comparison of rad-hard bandgaps in 130 nm and belonging at the same process published in literature.

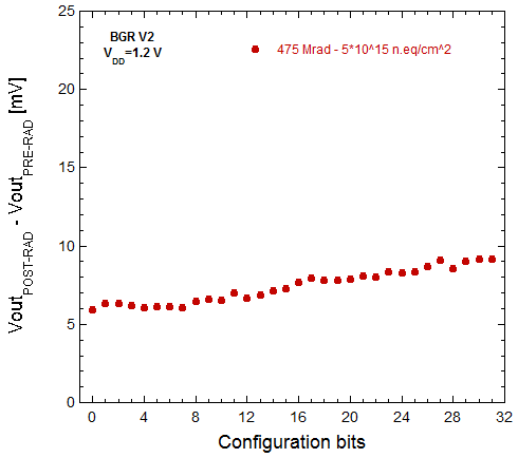


Figure 2.41: variation of bandgap output voltage after irradiation with 3 MeV protons at the CN accelerator in Legnaro.

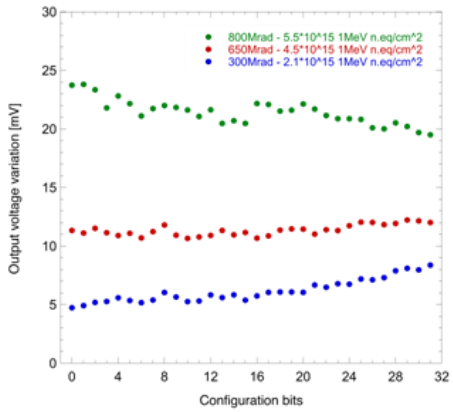
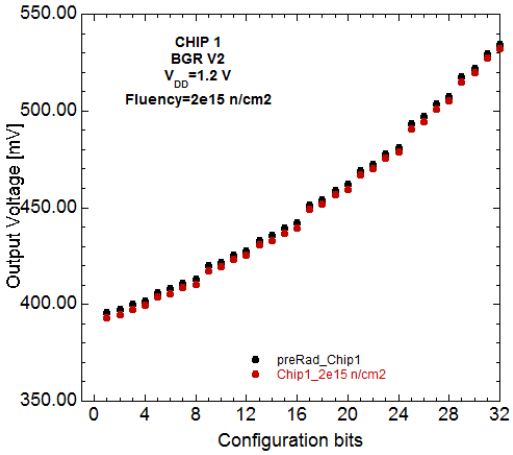
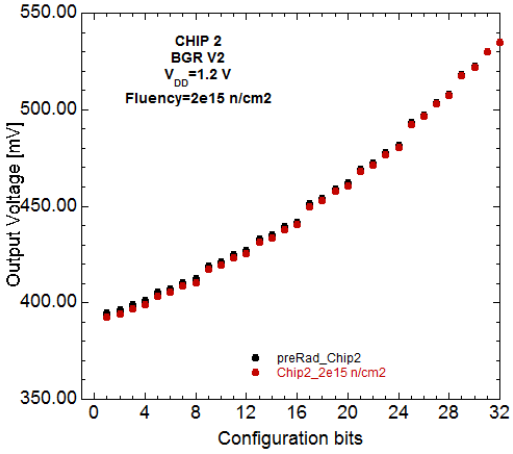


Figure 2.42: bandgap output voltage variation as a function of the configuration bits for different fluences and TIDs, from the 10 MeV proton source at the TANDEM accelerator in Legnaro.



(a)



(b)

Figure 2.43: output voltage as a function of the configuration bits for two chips irradiated with a fluence of $2 \cdot 10^{15}$ n.eq/cm^2 at the neutron source in Ljubljana.

Table 2.12: performance comparison with similar bandgap reference circuits.

Parameter	**This work** 2^{nd} proto	**This work** 1^{st} proto			**Cao [33]**	**Gromov [32]**	**Boufouss [34]**	**Abdelfattah [25]**
Technology (nm)	65 CMOS	65 CMOS			130 CMOS	130 CMOS	130 CMOS SOI	65 CMOS
Supply Voltage [V]	1.08 ÷ 1.32	1.08 ÷ 1.32			0.85 ÷ 1.5	0.85 ÷ 1.4	1.5	0.4 ÷ 0.6
Ref. Voltage @ 25°C [mV]		BJT	Diode	MOS				
	395	690	706	675	600	405	1500	275
Temperature Range [°C]	−40 ÷ 110	−30 ÷ 120			−40 ÷ 125	0 ÷ 80	−40 ÷ 200	−50 ÷ 80
TC [ppm/K]		BJT	Diode	MOS			133 (-40 to 90 °C)	
	18 (best case)	57	70	230	15	31	470 (-40 to 200 °C)	176
Trimming	yes	no			yes	no	no	no
Power [μW]		BJT	Diode	MOS				
	180	103	102	46	42 ÷ 75	-	50	62
ΔV_{out} (due to radiation)	6.5 % @ 800 Mrad	1.1% (best case)@225 Mrad			±3 % @ 450 Mrad	0.8 % @ 40 Mrad	5% @ 1.5 Mrad	-
Area [mm^2]		BJT	Diode	MOS				
	0.0264	0.0312	0.0262	0.0264	0.056	0.064	0.09	0.01

CHAPTER 3

LOW-POWER, LOW VOLTAGE, DIFFERENTIAL I/O LINK

Contents

This chapter presents the design of a low-power, differential I/O link in a 65 nm CMOS technology for high energy physics experiments. In particular, the driver and receiver comply with the scalable low voltage signaling

(SLVS) JEDEC electrical specification. The first part of the chapter has been dedicated to an overview of the differential transmission techniques and the relevant issues. The second part has been devoted to describing the design and the characterization of the SLVS transmitter and receiver.

3.1 Introduction

Low-Voltage Differential Signaling (LVDS) is a well-known and widely used technique in chip-to-chip interconnection. The differential I/O link provides a low-power, high-speed I/O interface for point-to-point transmission. Although differential transmission doubles the number of the lines required to transmit information, it improves the robustness of the link against common mode noise, and achieves low-power consumption together with low radiated electromagnetic interferences (EMI). An LVDS system enables the transmission of digital signals at very high data rates from 320 Mbit/s up to 10 Gbit/s. An LVDS transmitter can be modelled with a current generator with switching polarity. A 100 Ω differential load resistor at the receiver converts the current into a voltage signal with common-mode and differential-mode voltage that falls within the LVDS standard specifications. Figure 3.1 shows a point-to-point LVDS link. Since the proposed link will be used in a harsh radiation environment, the design is based on thin gate oxide transistors and a voltage supply of 1.2 V. This value is not compatible with the nominal common-mode voltage of the LVDS standard, which is 1.25 V. Moreover, due to the very low power dissipation constraint, the 350 mV differential swing has been reduced. Indeed, the physical layer chosen for these IP blocks is the JEDEC SLVS one [50].

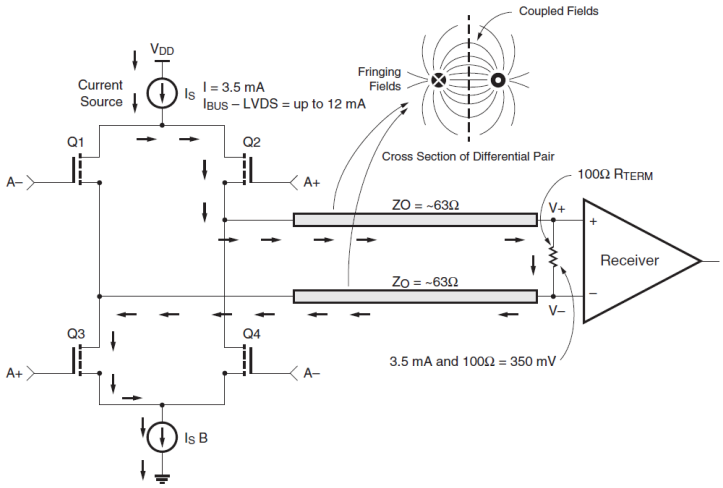
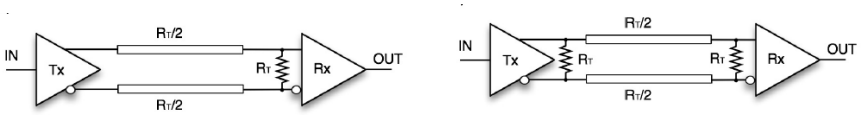


Figure 3.1: point-to-point LVDS link.



(a) differential signalling interface with termination resistance at the receiver end.

(b) differential signalling interface with termination resistance at the receiver and at transmitter end.

Figure 3.2: differential solution for high-speed data link.

3.2 SLVS system and specifications

The design of an SLVS transmitter and receiver was carried out in the framerwork of the RD53 collaboration [7]. The transmitter will be used in the pixel detector ASIC for the readout of the pixel matrix and to send the data off-chip. Instead, the SLVS receiver will be used for ASIC programming (i.e., to set the threshold level, the calibration signal level, the reference currents and voltages, etc...). The SLVS link uses differential data transmission. The transmitter works as a switched polarity current generator, like in the LVDS transmitter model described above. A differential resistive load provides the means for converting the current to a voltage, besides optimum impedance line matching. This is shown in figure 3.2a. For operation in the gigabits-per-second range, package parasitics or non correctly matched terminations may cause reflections from the load to the driver and back. To avoid this, an additional termination can be connected at the source end (figure 3.2b), at the cost of doubling the static power consumption needed to obtain the same output differential mode voltage. Since this design aims at minimizing the power consumption, the use of a termination resistor at the transmitter end was avoided[51].

Scalable Low Voltage Signaling (SLVS) is the differential interface adopted for the physical layer of the serial (data and clock) signals in the front-end chips for the CMS pixel detectors. The JEDEC protocol prescribes a differential current-steering circuit with voltage swing of ± 200 mV on a 100 Ω termination resistance. So, the typical output current is 2 mA with a common mode output voltage of 200 mV. The differential voltage is 400 mV as shown in figure 3.3.

The receiver detects the differential signal and converts it into a single ended CMOS signal. Noise picked up along the PCB interconnection is seen as common-mode by the receiver and rejected (figure 3.4). The reduction of the common mode voltage, with respect to the LVDS standard, makes it possible to use of a supply voltage as low as 0.8 V for the transmitter. A few commercial parts which comply with this standard are available, mainly from National Semiconductors, and their target application is in short (< 30 cm) communication links over PCB traces and flat cables for

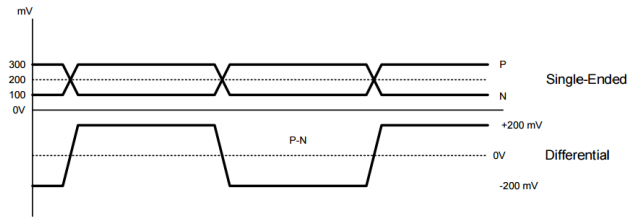


Figure 3.3: single ended and differential SLVS waveforms

mobile/portable devices.

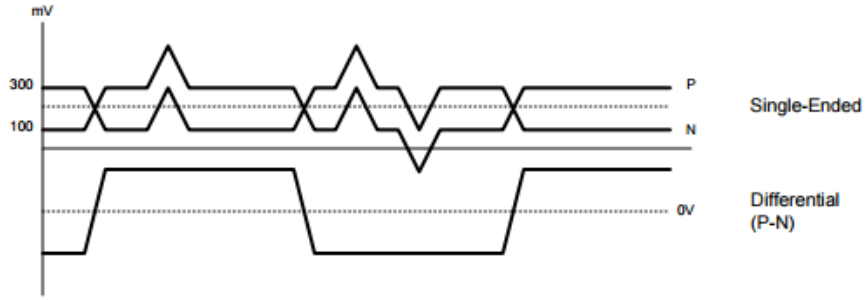


Figure 3.4: common-mode noise rejection.

The transmitter DC specifications are shown in table 3.1, whereas the receiver DC specifications are shown in table 3.2.

3.3 Performance qualification

A typical chip-to-chip architecture is composed by a transmitter, a physical channel and a receiver. The transmitter is the chip that sends data into the channel. The channel is the medium, such as a PCB trace, on which electrical signals travel. The receiver is the chip that recovers the original data from the received signal. In high speed signaling, the capability to recover the data from the transmitter and the receiver depends on different factors. The most important factors are losses in transmission lines, impedance mismatch and noise.

The PCB interconnections, typically, have a limited bandwidth due to skin effect. This phenomenon is responsible for a low-pass filter behaviour of the interconnection. In the time-domain, frequency-dependent attenuation of the channel manifests itself as intersymbol interference (ISI). ISI causes attenuation of the transmitted signal and spreads the energy of the transmitted signal into adjacent bits causing interference.

Table 3.1: transmitter SLVS JEDEC DC specifications.

Parameter	Description	Min	Nom	Max	Units
V_{CMTX}	output common mode voltage	150	200	250	mV
$\Delta V_{CMTX(0,1)}$	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV
$\|V_{OD}\|$	Output differential voltage	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0			10	mV
Z_{OS}	single ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	single ended output impedance mismatch			10	%

Table 3.2: receiver SLVS JEDEC DC specifications.

Parameter	Description	Min	Nom	Max	Units
$V_{CMRX(DC)}$	input common mode voltage	70		330	mV
V_{IDTH}	Differential input high threshold			70	mV
V_{IDTL}	Differential input low threshold	-70			mV
Z_{ID}	Differential input impedance	80	100	125	Ω

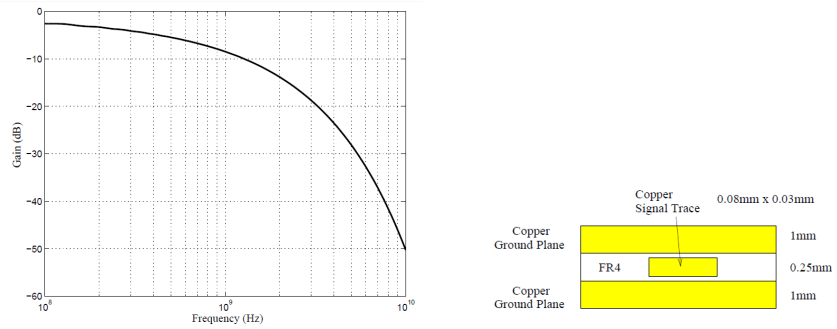
The transmission medium may have some discontinuity, which may cause signal reflections. Reflections, similarly to ISI, interfere with the received signal and lead to detection errors.

A physical stochastic process, called noise, is always associated with the transmission of a signal. Basically, noise is an undesirable signal added to the ideal signal. The deviation of a noisy signal from the ideal case can be examined in terms of timing deviation, also called jitter, and of amplitude deviation.

3.3.1 Lossy transmission line and intersymbol interference (ISI)

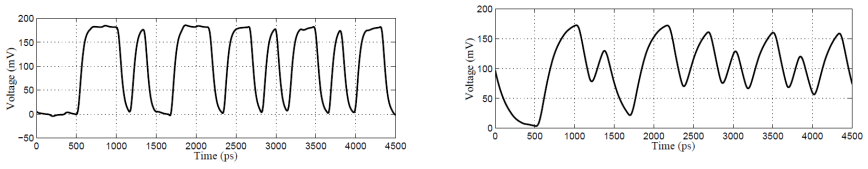
An ideal channel with flat frequency response does not introduce any distortion in the signal. However, any practical PCB channel in chip-to-chip signaling (i.e., microstrip, stripline, etc...) causes a frequency-dependent attenuation of the signals, due to the loss component in the transmission line. Loss in transmission lines is the principal signal-integrity problem for all signals with clocks higher than 1 GHz and for distances longer than 10 cm [54] [52].

The S21 parameter (insertion loss) obtained from the simulation of a simple 50 cm long, nearly 50 Ω transmission stripline is shown in figure 3.5a, while its cross-section is shown in figure 3.5b. The measurement shows



(a) (b)

Figure 3.5: (a) S21 parameter and (b) cross-sectional view of 50 cm (FR4) PCB stripline.



(a) (b)

Figure 3.6: (a) data transmitted at 6 Gbit/s and (b) received signal at 6 Gbit/s affected by ISI due to a lossy channel.

that the channel introduces an attenuation for frequency components below 1 GHz.

In the time domain, the low-pass filter effect of the channel manifests as intersymbol interference (ISI). The effect of ISI can be seen in figure 3.6b. The example signal is transmitted at 6 Gbit/s through a band-limited channel and has an amplitude of 200 mV. The frequency components above the channel cut-off frequency are attenuated, affecting the shape of the pulse that arrives at the receiver. Such phenomena lead to an error during the recovery of the original data. Assuming that, in figure 3.6b, the threshold is set to 100 mV, the received signal in some cases barely crosses the threshold, which increases the error probability in signal detection.[53].

Assuming that the bandwidth provided by the channel depends on the geometry, another important aspect is to understand how much bandwidth is required to transmit a random digital stream. Typically, in LVDS system, the random data transmitted and received is nonreturn-to-zero (NRZ) encoded data. In NRZ data transmission, each binary bit is assigned an equal bit period both for low value and high value. The synchronization of the system is maintained by a clock signal. Figure 3.7 shows a random bit sequence with a clock signal.

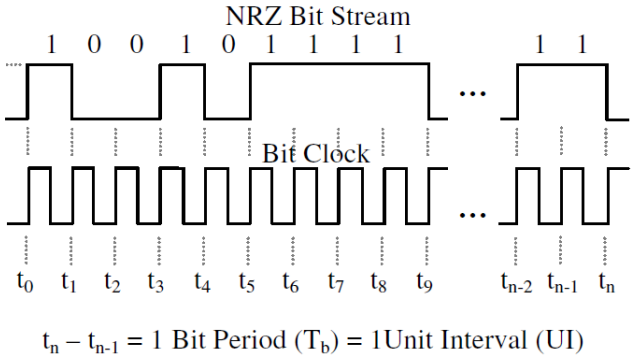


Figure 3.7: example of an NRZ random signal.

NRZ random data can be defined as a sequence of bits in which the probability of a bit to have value one or zero is the same and this probability is completely independent of all the other bits in the sequence (this is a memory-less system). In other words, there are no patterns in the stream. A statistical model can be used to analyze the bandwidth of the signal. The autocorrelation of any function of time can be defined by the following equation:

$$R_{XX}(\tau) = \lim_{t\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} X(t)X(t+\tau)d\tau \tag{3.1}$$

where τ is the time-shift. The autocorrelation function of the NRZ data, shown in figure 3.8, where $\tau = T_b$ is the shift (T_b is the bit period), is expressed in (3.2):

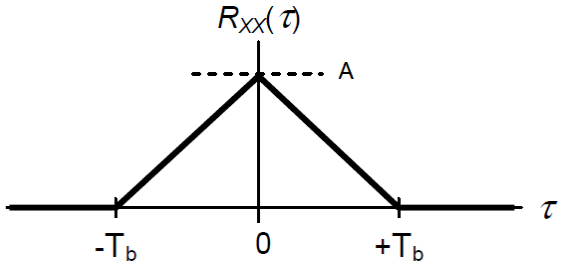


Figure 3.8: autocorrelation of a random NRZ stream.

$$R_{XX}(\tau) = \begin{cases} A^2\left(1 - \frac{|\tau|}{T_b}\right), & \text{if } |\tau| < T_b \\ 0, & \text{otherwise} \end{cases} \tag{3.2}$$

The power spectral density (PSD) of an NRZ signal is: [55]:

$$S_x(f) = A^2 T_b \left[\frac{\sin(\pi f T_b)}{\pi f T_b}\right]^2 \tag{3.3}$$

The plot of a sinc square function is shown in figure 3.9. The PSD shows that most of the power, 94% of the total, is contained in the frequency range between 0 and $0.75/T_b$. Thus, as a general criterion, an NRZ signal is required to have a bandwidth larger than $0.75/T_b$.

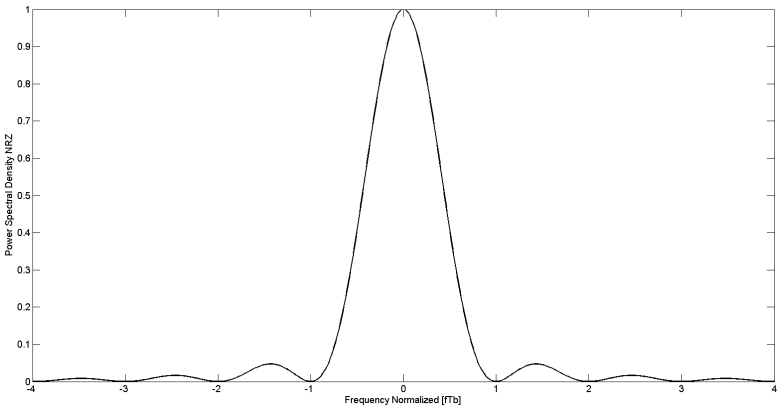


Figure 3.9: power spectral density of a random bit stream.

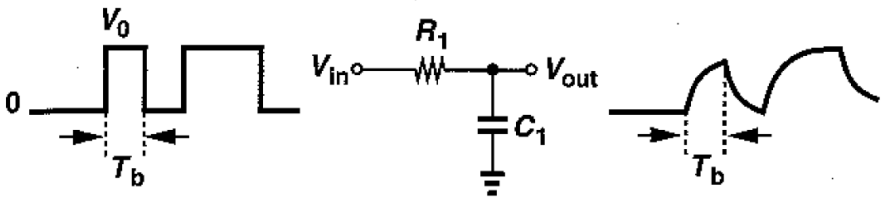


Figure 3.10: response of a single pole system to a random stream.

Another problem potentially leading to ISI is the limited bandwidth of the receiver itself. To understand this phenomenon, the receiver can be

approximated with a single pole system. The worst case occurs when there is a zero-bit (or a one) followed by a single one (or zero) as shown in figure 3.10. The settling process for each bit can be expressed as:

$$V_{OUT}(t) = V_0 \left[1 - e^{(-\frac{t}{\tau})}\right] \tag{3.4}$$

where $\tau = R_1 C_1$. The error between V_{OUT} at $t = T_b$ and the final value is given by

$$V_0 - V_{OUT}(T_b) = V_0 e^{(-\frac{T_b}{\tau})} = V_0 e^{\frac{-2\pi f_{-3dB}}{R_b}} \tag{3.5}$$

where $f_{-3dB} = \frac{1}{2\pi R_1 C_1}$ and $R_b = 1/T_b$ is the data rate (expressed in bit-per-second). Figure 3.11 shows the normalized error as a function of f_{-3dB}/R_b (called the fractional bandwidth). In order to obtain an error probability less than 5%, the receiver bandwidth should be in a range between $0.5R_b$ and $0.7R_b$[56].

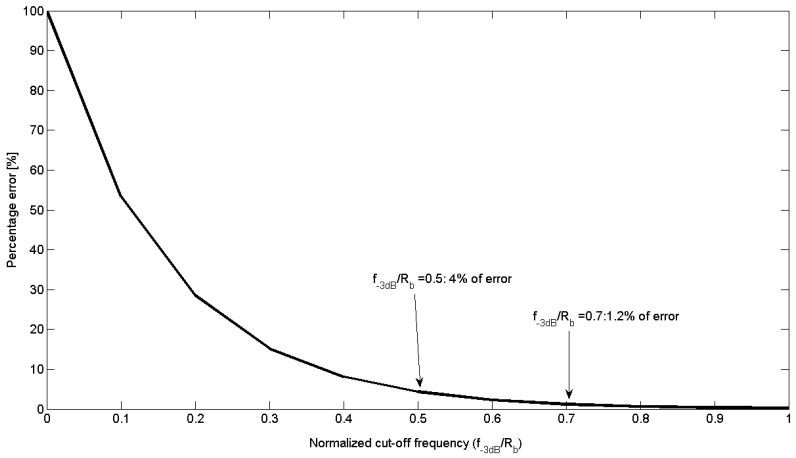


Figure 3.11: error as a function of the fractional bandwidth.

The above analysis provides just a design hint, because the above equations were obtained under the assumption of small signal operation. Since the receiver works with a differential signal amplitude close to hundreds of mV and the input differential pair works in slew rate mode, the main constraint becomes the channel bandwidth [39].

3.3.2 Impendance mismatch and reflection

Channels, such as microstrips, striplines, etc., may have some discontinuity that are responsible for signal reflection. Reflections, similar to ISI, interfere with the received signal and lead to detection errors. Reflections can be of

the resistive type, which occur when the characteristic impedance changes along the channel. The change of impedance can occur at the termination or at the junction between two PCB traces with two different characteristic impedances. Figure 3.12 shows a system with Z_0 characteristic impedance with termination resistors at both transmission and receiver ends. In case the resistance at the driver end is equal to the characteristics impedance and also to the resistance at the receiver end, the channel is completely matched and there is no reflection. But if the resistors at transmitter and/or receiver end are different, then there will be multiple reflections between the driver and the receiver. Figure 3.12 shows also the lattice diagram, which provides a convenient graphical means for keeping track of multiple wave reflections. Starting with the voltage $V_1^+ = V_0 Z_0/(R_S+Z_0)$ of the first wave component, the voltage amplitude of each successive wave is obtained from the amplitude of the previous wave rescaled with the appropriate reflection coefficient. In particular, at the transmitter end, the reflection coefficient is:

$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \tag{3.6}$$

and at the receiver end, the reflection coefficient is

$$\rho_L = \frac{R_L - Z_0}{R_L + Z_0} \tag{3.7}$$

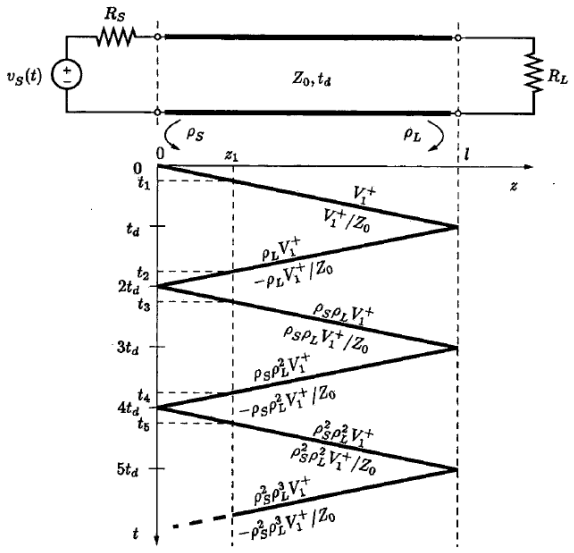


Figure 3.12: lattice diagram for a lossless transmission line with unmatched terminations.

Considering the case where there is an impedance mismatch, both at the transmitter and at the receiver ends, a reflected wave travels along the channel from the receiver to the driver and back again from the transmitter to the receiver causing interference with the received signal.

3.3.3 Noise and timing jitter

A physical stochastic process, called noise, is superimposed to the transmitted and received signal. Noise is an undesired signal, which is added to the ideal signal. A signal in digital communication, whose information is encoded in logical bits, can be represented by a trapezoidal wave with a finite rise and fall time. Noise, which is summed to the ideal signal, induces a degradation of the signal itself, as shown in figure 3.13

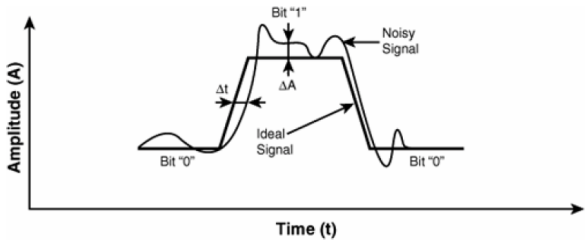


Figure 3.13: ideal digital signal and a noisy version of the same signal.

The deviation of a noisy signal from an ideal signal may be viewed in two ways: as an amplitude deviation and as a timing deviation. The first one (ΔA) is defined as the amplitude noise (or simply noise); the second one (ΔT) is defined as the timing jitter (or simply jitter). The impact of the amplitude noise or the jitter can be understood from the perspective of the receiver. The signal received can be degraded in terms of amplitude due to the noise and in terms of rising and falling edge due to jitter. The receiver has an amplitude threshold in order to recognize if the bit is a logic 1 or a logic 0 and also a timing threshold, which allows to discriminate the bit period. Such a threshold is provided by the clock signal. In the presence of jitter and noise, the rising and falling edges can move along the time axis, while the voltage amplitude can move along the amplitude axis. Consequently, the conditions of the receiver, that allow it to correctly detect a bit, may not be satisfied, resulting in a bit detection error due to a bit 1 being detected as a bit 0 or vice versa.

Jitter

The jitter can be defined as the short term variation of the significant instants (e.g., threshold crossing) of a digital signal from their ideal positions in time (ΔT) [58]. The main cause of the jitter is noise. Other possible causes of jitter can be classified as *system phenomena* or *data-dependent*.

System phenomena are effects on a signal resulting from the fact that the transmitter and the receiver are digital circuits in an analog environment. Examples of these system-related jitter sources include: crosstalk from radiated signals, dispersion effects and impedance mismatch.

Data-dependent phenomena are patterns or other characteristics of the data being transferred that affect the overall jitter of the signal arriving to the receiver. Data-dependent jitter sources are inter-symbol interference (ISI), duty-cycle distortion and pseudorandom bit-sequence periodicity[59]

The jitter can be divided into two main categories: the first one is that of deterministic jitter, which is bounded and is typically expressed in terms of peak-to-peak value. Such a jitter component is influenced by system and data dependent phenomena. The second category is that of random jitter, which is due to noise. Figure 3.14 shows the main components of the total jitter, also listed in the following.

- **Random Jitter (RJ):** is the principal source and is due to noise within system components. It interacts with the slew rate of signals and produces timing errors at the crossing points.
- **Deterministic Jitter (DJ):** jitter with non-Gaussian probability density function. It is always bounded in amplitude and is due to specific causes. Sources are imperfections of devices, crosstalk, EMI, grounding problems.
- **Periodic jitter (PJ):** the periodic jitter has sinusoidal form; the source of interference generally lies in the data pattern, ground bounce or power supply variations.
- **Data dependent jitter (DDJ):** consists of inter symbol interference (ISI) and duty cycle distortion (DCD). Timing errors vary as a function of data pattern. Component and system bandwidth limitations. Higher frequency components have less time to settle than lower frequency ones, due to the bandwidth limited channel.
- **Inter Symbol Interference (ISI):** inter symbol interference is the most common form of DDJ. It is usually caused by bandwidth limitations of transmission lines.
- **Duty Cycle Distortion (DCD):** takes place when certain bit states have different durations. Typically there is a difference between the rise time and the fall time for each bit period.

- **Total jitter(TJ):** the sum of deterministic and random jitter. Total jitter is the peak-to-peak value obtained by $TJ = DJ + nRJ$ where n = number of standard deviations corresponding to the maximum allowable Bit Error Rate (BER)[1].

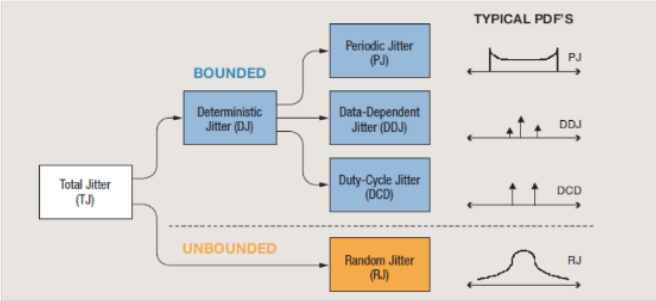


Figure 3.14: main components of the jitter: noise, system-phenomena and data-dependent contributions.

As already mentioned, the ideal signal is corrupted by noise, which can be quantified in terms of timing jitter. The amplitude of noise can be expressed as $\Delta A(t)$, while $A_0(t)$ represents the ideal signal. The total waveform can be expressed as the superposition of the two terms,

$$A(t) = A_0(t) + \Delta A(t) \tag{3.8}$$

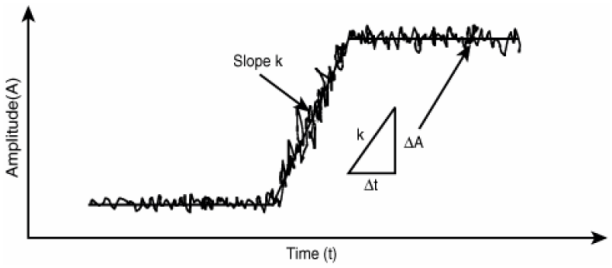


Figure 3.15: amplitude noise to timing jitter conversion through the linear model.

resulting in the waveform of figure 3.15. $\Delta A(t)$ can be expressed by using a linear small signal perturbation model. Since [57].

[1]The BER is the ratio between the number of incorrectly detected bits and the total number of transferred bits.

$$\Delta A(t) \sim \frac{dA_0(t)}{dt}\Delta t \tag{3.9}$$

the timing jitter can be expressed as:

$$\Delta t \sim \frac{\Delta A(t)}{\frac{dA_0(t)}{dt}} = \frac{\Delta A(t)}{k} \tag{3.10}$$

where k is the slope of the waveform. As shown in (3.10), the timing jitter is caused by additive noise. The jitter effect due to noise can be reduced by increasing the slope of the signal.

3.3.4 Eye diagram

The eye diagram is a useful tool to verify the integrity of the signal in the case of a random sequence of binary bits. The eye diagram is generated by folding all bits into a bit period, as shown in figure 3.16.

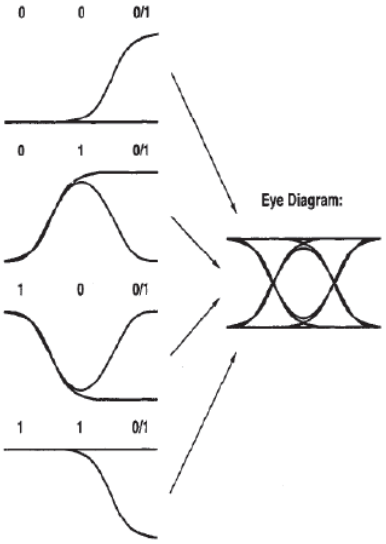


Figure 3.16: generation of the eye diagram.

The most import characteristic of the eye diagram is the possibility to display the overall transmitted signal in a compact representation. The eye aperture is the most important parameter that can be extracted from the eye diagram. The eye aperture describes, in qualitative terms, the integrity of the transmitted signal.

Figure 3.17 shows an example of eye diagram and the parameters of the signal quality that can be extracted from the eye. The width and the height provide information about the aperture of the eye. Others important

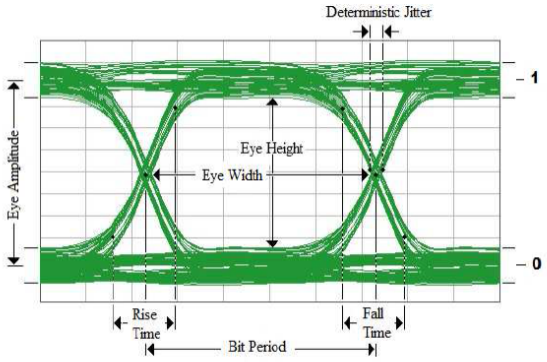


Figure 3.17: example of eye diagram with the relevant eye parameters.

parameters are the fall and the rise time and the deterministic timing jitter, that can be measured at the intersection between the rising and the falling edges of the signal.

3.4 Design and simulation results of the SLVS transmitter

Figure 3.18 shows the schematic adopted for the SLVS transmitter. The transistors M_8, M_9, M_3 and M_4 form the current polarity switch block. The output current is generated by means of the M_{15} transistor, which is programmable by means of the three bits B_0, B_1 and B_2. Each bit enable a switch and the reference current generated is mirrored with a 20:1 ratio from M_{11} to M_{15}. Table 3.3 shows the configuration bits and the relevant output current.

Table 3.3: output current configuration of the SLVS transmitter.

$B2$ $B1$ $B0$	$I_{OUT}/20$ [μA]	I_{OUT} [mA]
0 0 0	External reference	
0 0 1	25	0.5
0 1 1	50	1.0
1 0 0	75	1.5
1 0 1	100	2.0
1 1 1	125	2.5

Resistors R_1 and R_0 sense the common mode output voltage, which is generated at the output of the driver. The common mode voltage is com-

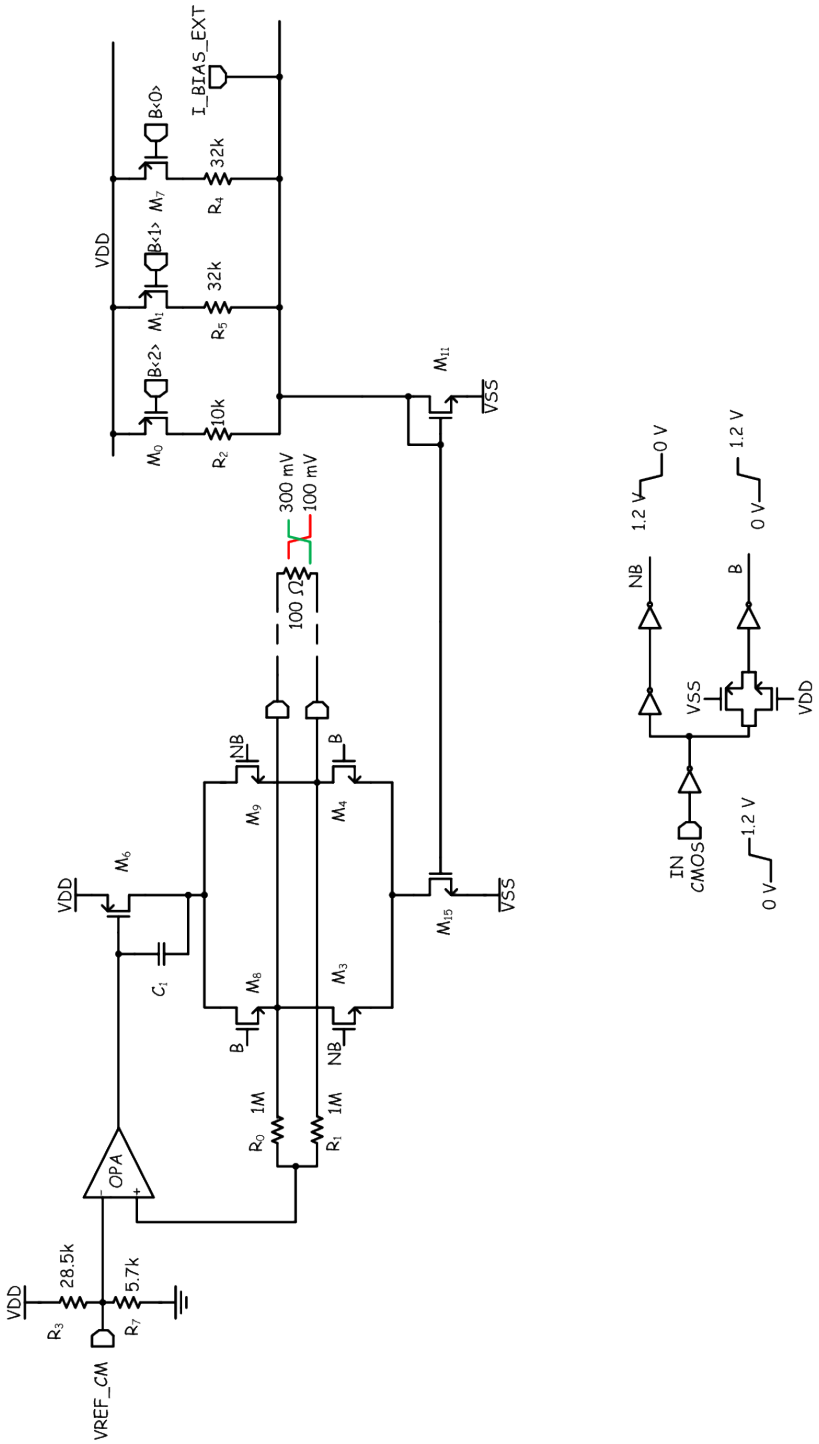


Figure 3.18: schematic of the SLVS transmitter.

pared with the reference common voltage, which is provided by two resistors, R_3 and R_7. $V_{REF_{CM}}$ is also available at the output for control purposes. The two resistors provide a reference of 200 mV, as foreseen by the JEDEC SLVS specification. The operational amplifier and the M_6 transistor compose the common mode feedback loop in order to obtain an output common mode voltage that is stable against PVT variations. The operational amplifier is based on a symmetrical OTA stage, in order to reduce the systematic offset of the operational amplifier itself, and is biased with a low current in order to reduce the overall power consumption. A capacitance has been added between the gate and the drain of the M_6 transistor, using the Miller effect, to achieve a large stability margin over PVT variations.

3.4.1 Operational amplifier and stability of the common mode feedback

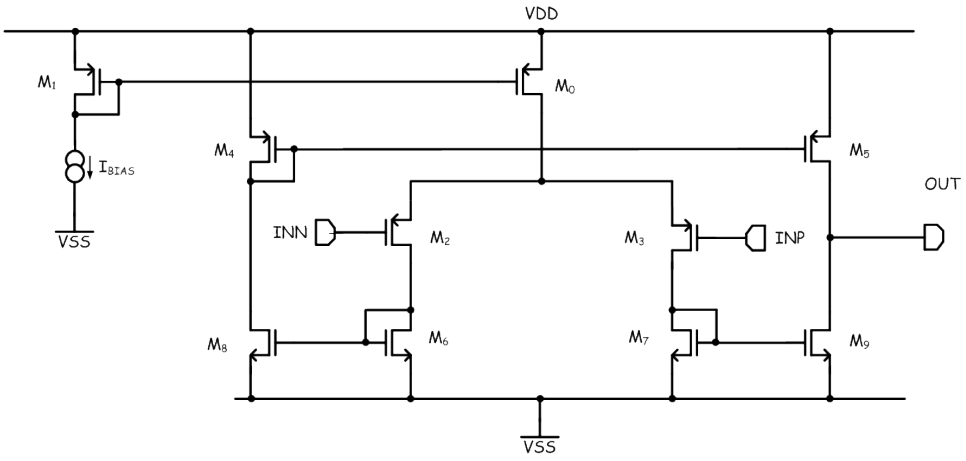


Figure 3.19: schematic of the symmetrical operational amplifier

The architecture of the operational amplifier used for the common mode feedback loop is a symmetrical OTA, in order to reduce the systematic offset. The schematic is shown in figure 3.19. A trade-off between phase margin and gain has to be satisfied. On one hand, the phase margin of the common mode feedback loop has to be grater than 45°, in order to ensure stability. On the other hand, the gain of the loop, obtained by the product of the OpAmp gain (A_0) and the gain $g_{m6}r_{ds,M_{15}}$ has to be sufficiently high in order to reduce the error between the output common mode and the reference itself.

The analysis of the phase margin of the common mode feedback loop is performed when the transmitter is in the linear region. This condition is obtained when the voltages applied at the nodes B and NB are both equal to $V_{DD}/2 = 600$ mV. In this condition, the common mode output voltage

is 195.5 mV with a reference of 200 mV. Figure 3.20 shows the loop gain and the relevant phase margin. The phase margin in nominal condition is close to 72°.

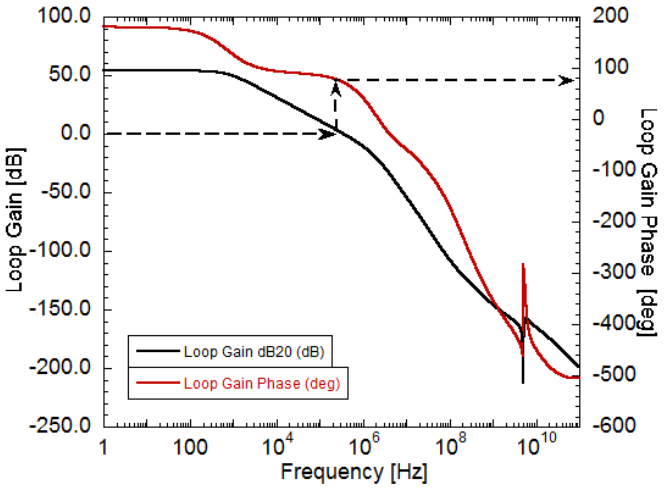


Figure 3.20: Bode diagram of the common mode loop gain.

3.4.2 Phase splitter

As shown in figure 3.18, the signals B and NB are CMOS signals with opposite phases. To obtain these signals, two inverters chains have been implemented in order to perform single ended to differential conversion. Such signals are generated by a phase splitter. This component has a CMOS input signal (0, 1.2V) and produces at the output two CMOS signals with opposite phase. The NMOS of the switched current polarity block has a large size, to reduce the r_{ds} resistance in triode region. But the large size of the transistor implies a large $C_p \approx C_{OX}WL$ capacitance. The phase splitter is composed by a long chain of inverters in order to drive this load. The inverter chain is composed by two stages. The first one includes four inverters connected in parallel, whereas the second stage contains eight inverters. The number of the elements has to be such to obtain a rise and fall time less than 1/10 of the minimum period of the input signal (1/1.2 Gbit/s). Since the two inverter chains typically have not the same number of elements, an always-on CMOS switch was introduced to obtain the same propagation delay of the signals at the inputs of the driver. Figure 3.21 shows the B and NB output waveforms of the phase splitter, in particular, when at the input a Pseudo Random Binary Sequence (PRBS)[2] signal at 1.2 Gbit/s is applied.

[2]A PRBS is a binary sequence that, generated by a deterministic algorithm, exhibits statistical behavior similar to a truly-random sequence

Figure 3.22 shows the degradation of the duty cycle at the output of the phase splitter during a transient simulation. The maximum degradation of the duty cycle is close to 2%.

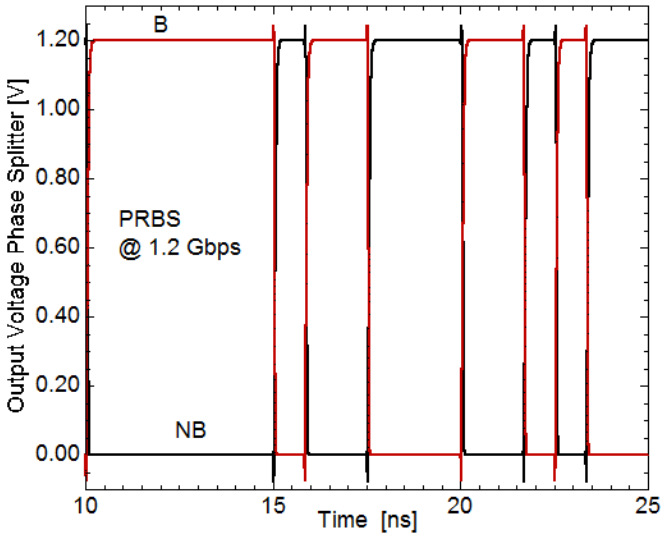


Figure 3.21: outputs of the Phase Splitter block, when at the input a PRBS signal at 1.2 Gbit/s is applied.

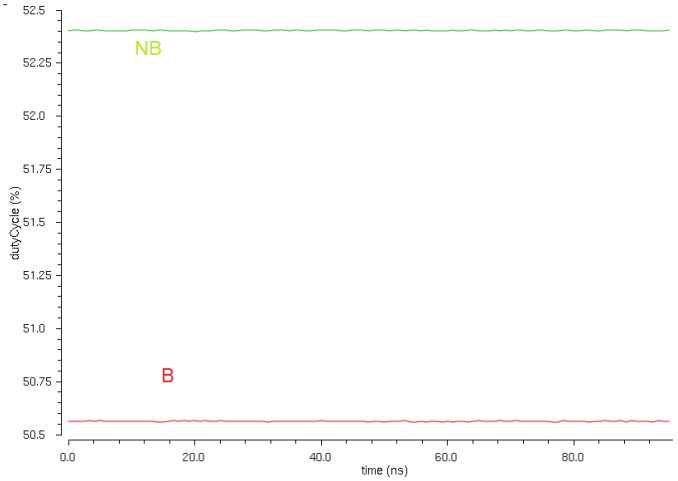


Figure 3.22: duty-cycle distortion during a transient simulation. The input signal is a clock at 1.2 GHz.

Table 3.4: microstrip properties

Base Copper Weight	35 μm
Plating Thickness	35 μm
Conductor Width (W)	0.2 mm
Conductor Spacing (S)	0.3 mm
Dielectric layer thickness (H)	0.16 mm

3.4.3 Test Bench

In order to evaluate the degradation due to reflection, attenuation by parasitic capacitance and so on, the test bench in figure 3.23 has been used to simulate the transmitter circuit.

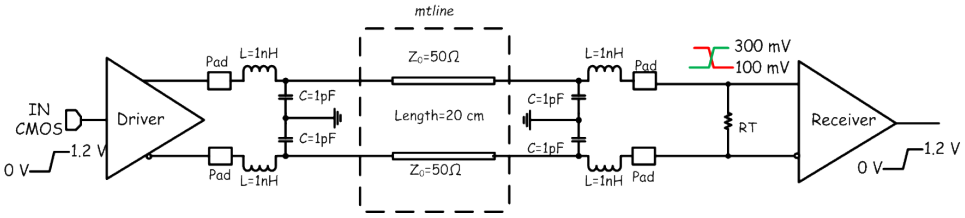


Figure 3.23: test bench for the transmitter.

The pads include ESD protections, while the inductor of 1 nH models the parasitic effect of the wire bonding. Instead, the capacitance of 1 pF accounts for the parasitic capacitance of the PCB pad. The transmission line has also been included in the simulation. The *mtline* used in Cadence Virtuoso has a characteristic impedance of $Z_0 = 50\ \Omega$ and a length of 20 cm. Table 3.4 summarizes the main characteristics of the microstrip model. The cross section of the microstrip is shown in figure 3.24.

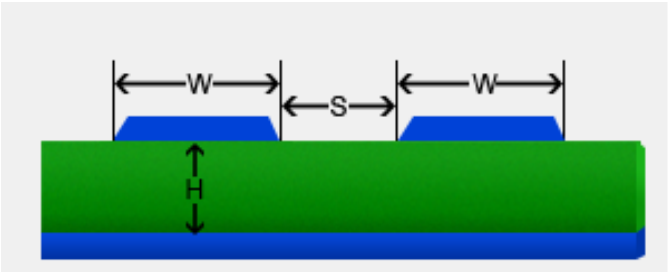
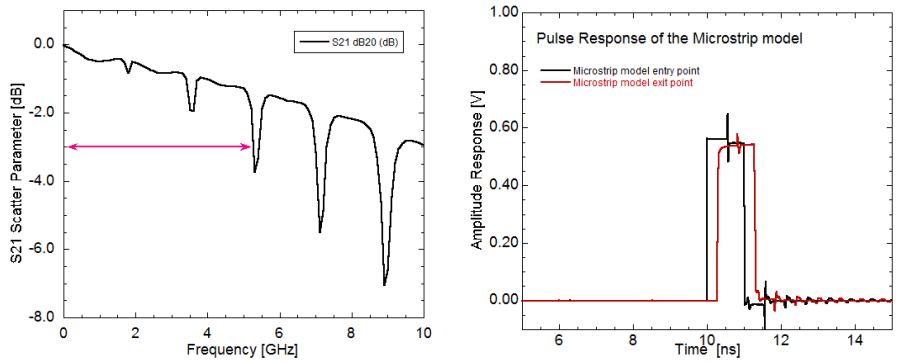


Figure 3.24: cross section of the microstrip.

The dielectric of the PCB is PrePreg 7628 with a relative dielectric constant $\epsilon_r \approx 4.6$. Figure 3.25a shows the insertion loss of the microstrip (S21

scatter parameter). The bandwidth of the microstrip is larger than 1.2 GHz. The propagation delay between the input (black line) and output (red line) of the microstrip, which is 290 ps, is shown in figure 3.25b. In the Cadence environment, the microstrip has been stimulated by a pulse signal. Time domain reflectometry (TDR) simulation shows that the characteristic impedance is matched with the input and the output resistance. Indeed, the input signal (black line) does not manifest any mismatch induced amplitude variation during the transmission, as shown in figure 3.25b. A small attenuation effect of the signal can be seen due to frequency limitations of the modelled microstrip. The transmitter has been simulated with a PRBS at 1.2 Gbit/s and with a clock signal at 1.2 GHz.



(a) (b)

Figure 3.25: (a) S21 insertion loss scatter parameter of the microstrip and (b) impulse response of the microstrip line.

3.4.4 Simulation results

In this section, the results from the simulation of the transmitter will be reported. Two values of temperature have been used during the design and simulation: room temperature (for characterization activity) and −20 °C (operating condition during the experiment at HL-LHC).

The transmitter has been stimulated with two CMOS signals: the first one is a PRBS at 1.2 Gbit/s, the second one is a clock signal at 1.2 GHz. When the input of the driver is stimulated with a PRBS signal, the eye diagram and the relevant parameters are evaluated at the 100Ω termination resistance. Instead, when at the input a clock signal is applied, the duty cycle and the clock jitter degradation are assessed. Figure 3.26 shows the differential output voltage with a bit stream speed of 1.2 Gbit/s. In particular, the top time diagram shows the input PRBS signal, while the bottom one is the differential output (the voltage across the output termination resistance), with a peak-to-peak amplitude close to 400 mV. Instead, the simulated eye

diagram of the differential output is shown in figure 3.27. Some significant parameters can be extracted from the eye diagram, as shown in figure 3.17. The bottom level, also called level-0, is $\mu_0 = -201.5$ mV $\pm$ 11.7 mV($\pm\sigma$); for the top level (level-1) is $\mu_1 = 203.5$ mV $\pm$ 9.5 mV. Figure 3.28 shows the eye diagram levels. The amplitude of the eye diagram is 404 mV, the height is 341 mV, and the signal-to-noise ratio ($S/N_{Eye} = \frac{\mu_1 - \mu_0}{\sigma_{level-0} + \sigma_{level-1}}$) of the eye is 19. The width of the eye is 808 ps and the total jitter pk-to-pk is 7 ps. The rise time and fall time are 48 ps and 47 ps respectively. The total power consumption (static + dynamic) is 3.3 mW and the average of the output common mode voltage is 192.9 mV.

As mentioned before, the temperature in the real application will be -20 °C. Figures 3.29 a and b show the eye diagram of the driver output, when a 1.2 Gbit/s PRBS signal is applied and the differential output voltage with an input clock signal (1.2 GHz) when the system is kept at -20 °C. In Table 3.5, a comparison at different operating temperatures is shown.

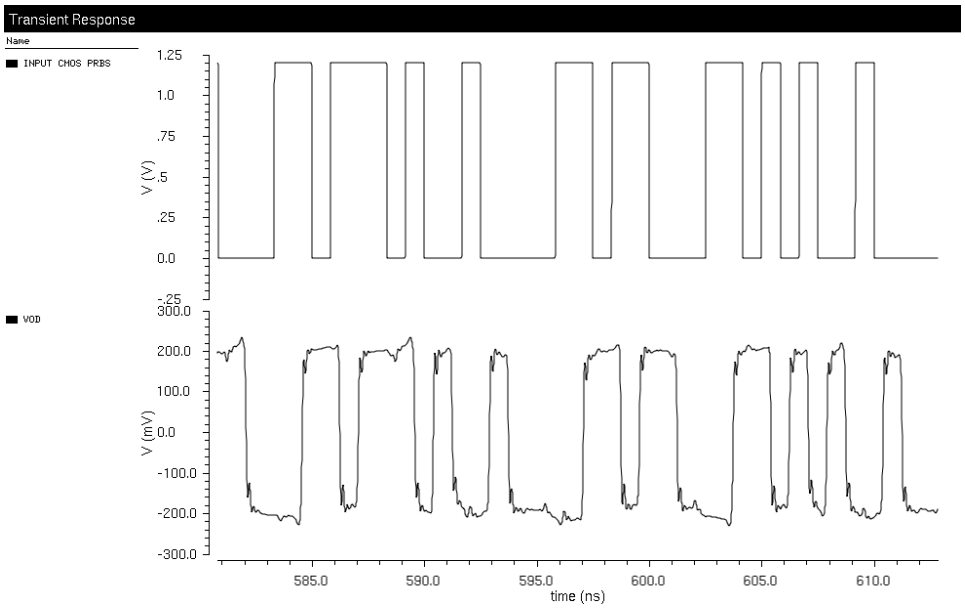


Figure 3.26: differential output of the transmitter. Stimulated with a PRBS at 1.2 Gbit/s.

Figure 3.30 shows the time response when a 1.2 GHz clock signal is applied at the input of the driver. The simulated duty cycle is 50.4% and the absolute clock jitter is 5.8 ps.

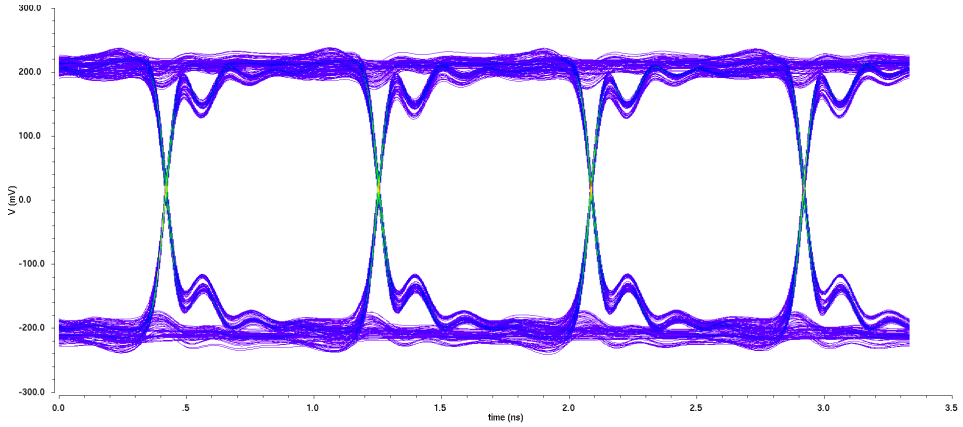


Figure 3.27: simulation of the transmitter eye diagram taken at the input termination resistance of the receiver.

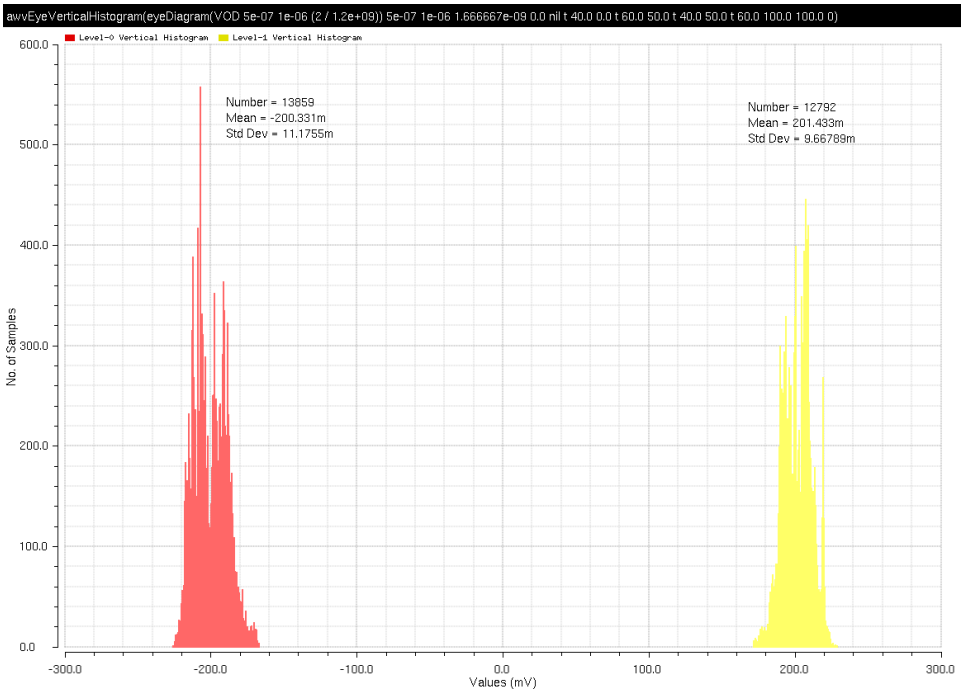
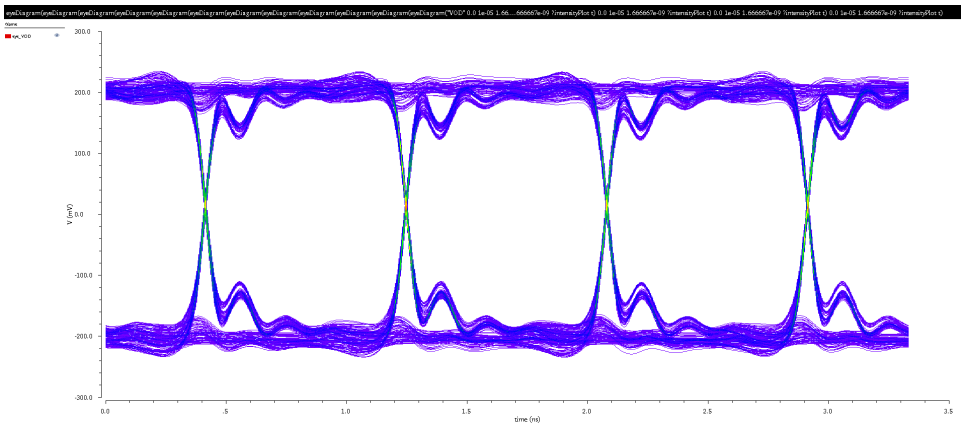


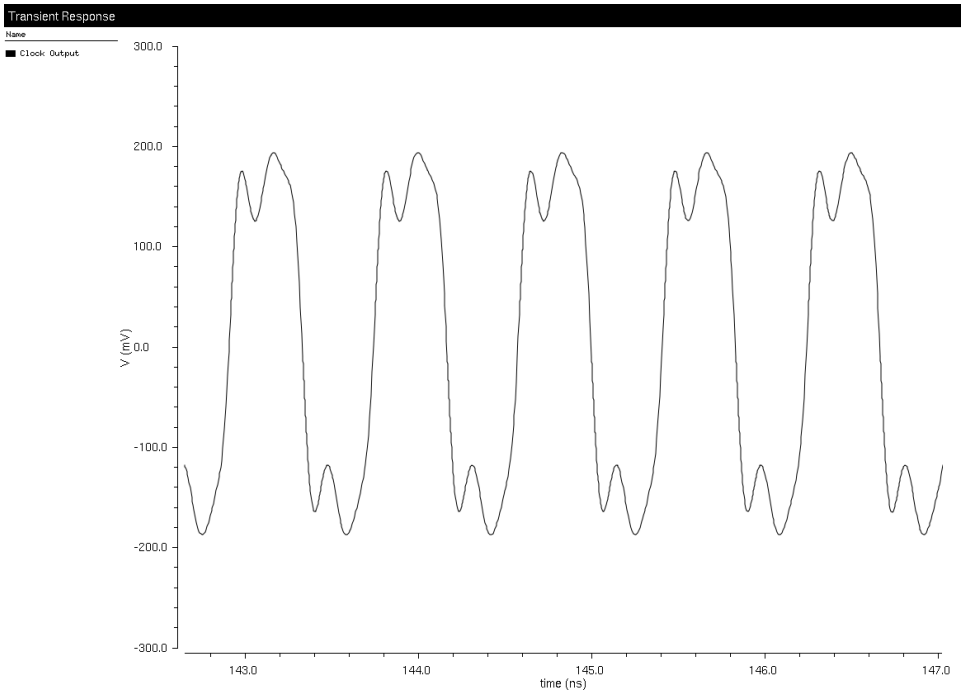
Figure 3.28: histogram of the eye diagram levels

PVT simulations

The transmitter was also simulated in some corners in order to take into account process, temperature and power supply voltage variations. PVT analysis is a worst-case approach in which the robustness of the transmitter is



(a)



(b)

Figure 3.29: (a) eye diagram of the transmitter output at −20 °C and (b) transient response applying a clock input signal at −20 °C.

evaluated against process (SS, SF, FS and FF), temperature (−40 °C,−20 °C, 0 °C, 27 °C, 100 °C) and power supply variations (1.08 V, 1.2 V and 1.32). Of the above corners, only three are discussed: the fast corner (FF, $-40°C$, 1.32 V) and the slow corner (SS, $100°C$, 1.08 V), which are the worst ones, and the typical corner (TT, $27°C$, 1.2 V). Figure 3.31 shows the eye diagram of the differential output for the worst case corners (slow and fast)

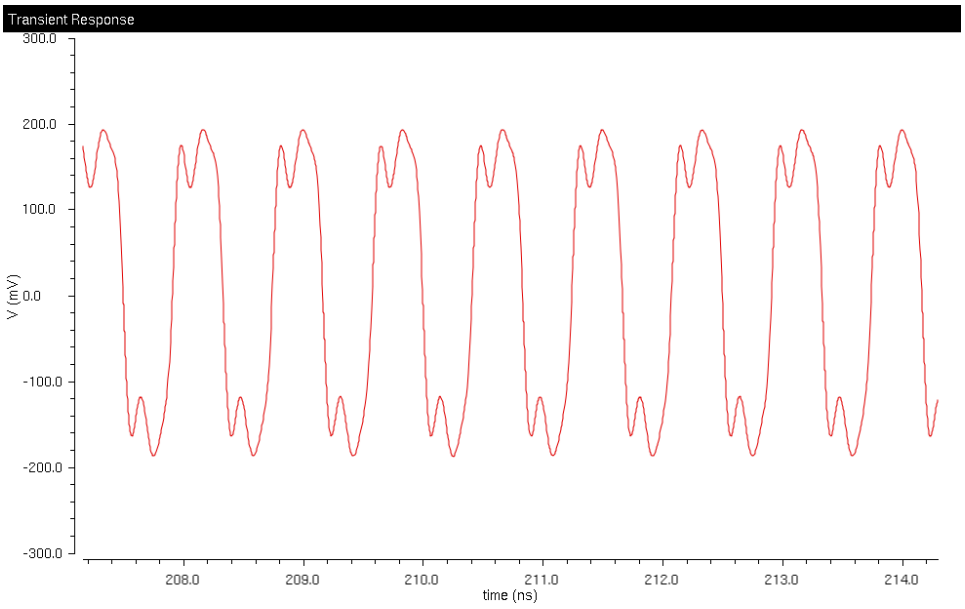


Figure 3.30: differential signal at the driver output. Input signal is a clock at 1.2 GHz at room temperature and nominal condition.

Table 3.5: comparison of the driver performance.

Test	Description	27 °C	−20 °C
PRBS	Level-0	-201.5 mV $\pm$ 11.7 mV	-197.2 mV $\pm$ 11.9 mV
	Level-1	203.5 mV $\pm$ 9.5 mV	199.1 mV $\pm$ 10.6 mV
	Eye Amplitude	404.6 mV	336.6 mV
	Eye Height	341.1 mV	328.9 mV
	Eye Width	808.8 ps	809.9 ps
	S/N	19.13 dB	18.2 dB
	Rise Time	48 ps	50 ps
	Fall Time	47 ps	52 ps
Clock	Duty-Cycle	50.3 %	50.4 %
	rms jitter	5.9 ps	5.6 ps

and the typical corners. There is a degradation in the slow corners (yellow plot), because the rise time and fall time are slower and the amplitude is lowered due to the reduction of the power supply. However, the amplitude of the eye complies with the JEDEC specifications. Figure 3.32 shows the differential output of the transmitter when a clock signal is applied at the input in the worst case corners. Also in this case there is a degradation of the amplitude and of the dynamic performance, still within specifications.

Table 3.6 summarizes the main parameters of the transmitter obtained from simulations in two worst cases and in the nominal case. Figure 3.33 shows the layout of the transmitter. The area of the block is close to 150 μm x 200 μm

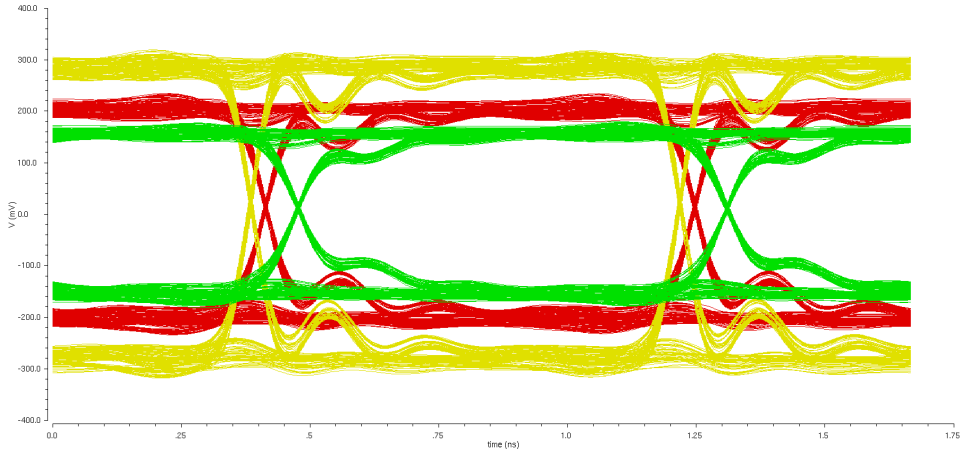


Figure 3.31: eye diagram simulated in three different corners: the green diagram obtained in the slow corner, the red one in the typical corner and the yellow one in the fast corner.

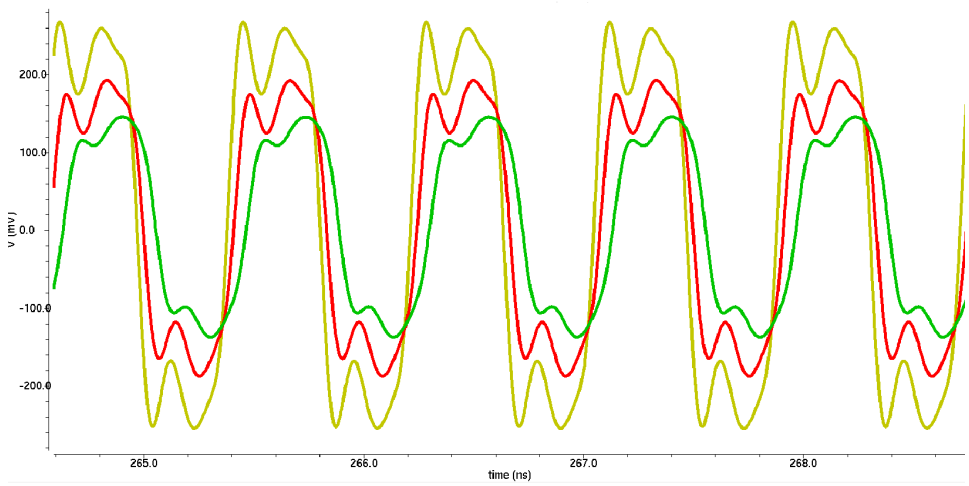


Figure 3.32: differential output of the driver, stimulated by a clock signal obtained from PVT simulations. The green time diagram refers to the slow corner, the red diagram to the typical corner and the yellow one to the fast corner.

Table 3.6: performance of the transmitter in PVT simulations.

Test	Description	Nominal	Fast	Slow
PRBS	Level-0	-201.5 mV $\pm$ 11.7 mV	-278.7 mV $\pm$ 14.8 mV	-133.9 mV $\pm$ 16.3 mV
	Level-1	203.5 mV $\pm$ 9.5 mV	283.3 mV $\pm$ 12.8 mV	137.2 mV $\pm$ 13.9 mV
	Eye Amplitude	404.6 mV	562.0 mV	271.6 mV
	Eye Height	341.1 mV	479 mV	211.4 mV
	Eye Width	808.8 ps	816.4 ps	789.6 ps
	S/N	19.13 dB	22.9 dB	10.6 dB
	Rise Time	48 ps	32 ps	75 ps
	Fall Time	47 ps	35 ps	110 ps
	Average Output Common mode	192.9 mV	215.2 mV	170.9 mV
	Total Power Consumption	3.31 mW	4.6 mW	2.3 mW
Clock	Duty-Cycle	50.3 %	51 %	49 %
	rms jitter	5.9 ps	6.8 ps	11 ps

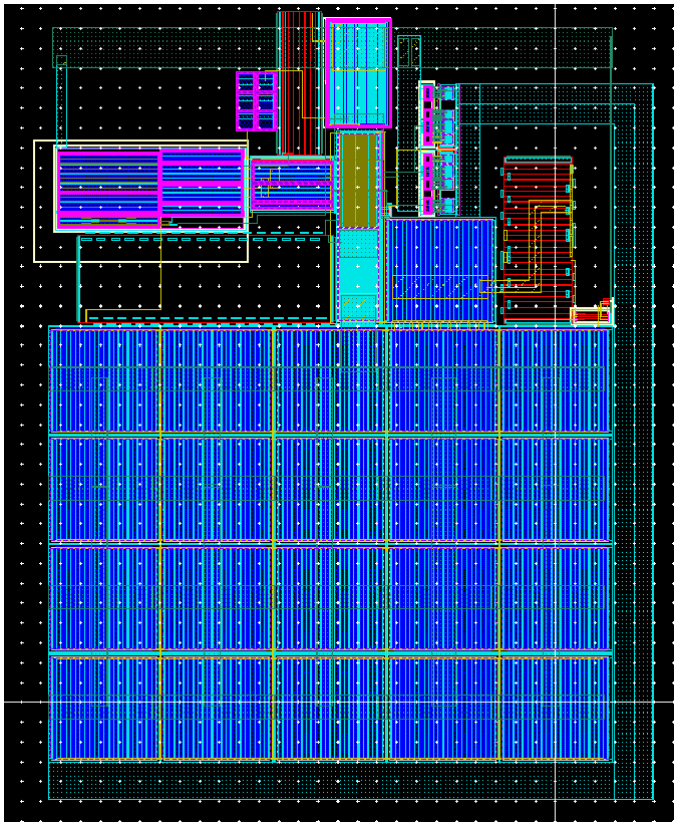


Figure 3.33: layout of the transmitter.

3.5 Design and simulation results of the SLVS receiver

Figure 3.34 shows the schematic of the SLVS receiver. The architecture is based on two differential pairs in cross-coupled configuration and are con-

nected in parallel. One input pair is composed by two NMOS transistors, while the second pair is composed by two PMOS transistors. In this way, a rail-to-rail architecture is implemented in the input stage, which is then capable to detect signals with a common mode ranging from VDD to VSS. Moreover, each differential pair has a cross-coupled load, which creates a positive feedback. Such a feedback loop increases the gain of this block [60]. For each of the two differential input stages, the output is sent to a differential-to-single ended converter. The last stage of the receiver is a chain of two inverters serving the purpose of squaring the output waveform. The output of the receiver is loaded with a capacitance of 100fF. The re-

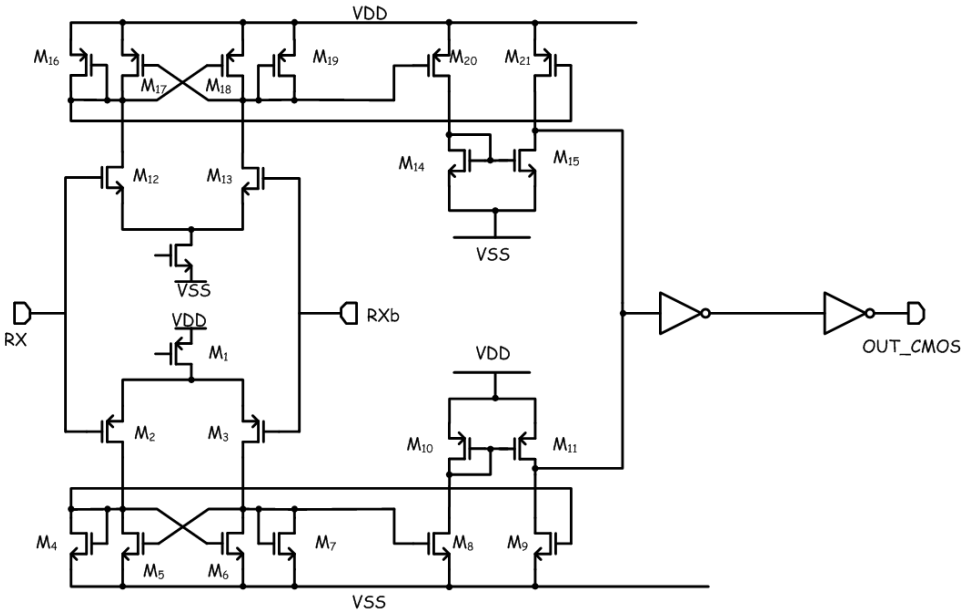


Figure 3.34: schematic of the receiver.

ceiver has been stimulated with a differential PRBS signal at 1.2 Gbit/s. The peak-to-peak value of the input signal goes from 70 mV, which is the minimum differential signal allowed by the JEDEC specification, to 300 mV. The common mode goes from to 0 to 1.2 V. The total power consumption is close to 1.5 mW.

3.5.1 Small-signal analysis

In case a common mode of 200 mV is applied to the input, a reasonable approximation is that only the stage with n-MOS input differential pair is working. Thanks to the positive feedback, the gain of the first stage is very high [61]. In fact, the gain stage can be expressed by:

$$A_0 = \frac{g_{m2}}{g_{m4} - g_{m5}} \tag{3.11}$$

In the receiver design, a trade-off between the gain and the bandwidth has to be found. Indeed, the gain of the receiver need not be very high, because the differential signal applied at the input is close to 70 mV (in the worst case for SLVS specification). Thus, the bandwidth of the receiver can be incremented in order to have a faster response and reduce the ISI. Figure 3.35 shows the bandwidth (cut-off frequency) and the gain of the receiver in small signal conditions for different values of the common mode voltage applied to the input. The required bandwidth is close to 1 GHz. For the

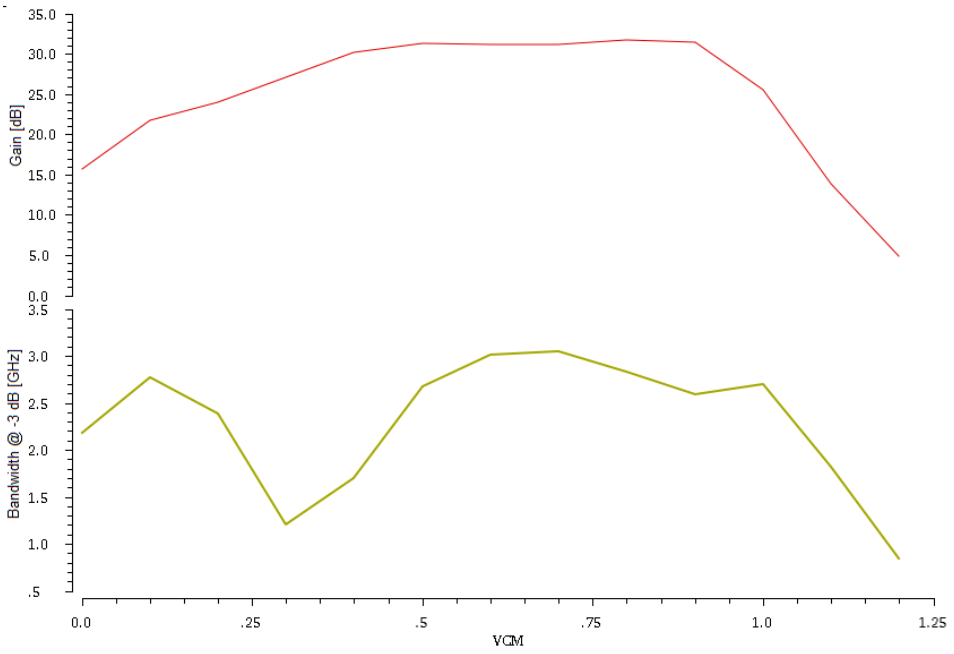


Figure 3.35: bandwidth and gain of the receiver as a function of the common mode voltage of the input signal.

typical operating conditions (V_{CM} = 200 mV), the gain is close to 23 dB and the bandwidth is grater than 2 GHz. Furthermore, the bandwidth is greater than 1 GHz for a common mode voltage from 0 V to 1.15 V, with a local minimum of the bandwidth around 300 mV. However, this worse case complies the minimum bandwidth required. The worst case is when the common mode input is equal to VDD. In this case, the bandwidth is 0.75 GHz and the DC gain is close to 5 dB.

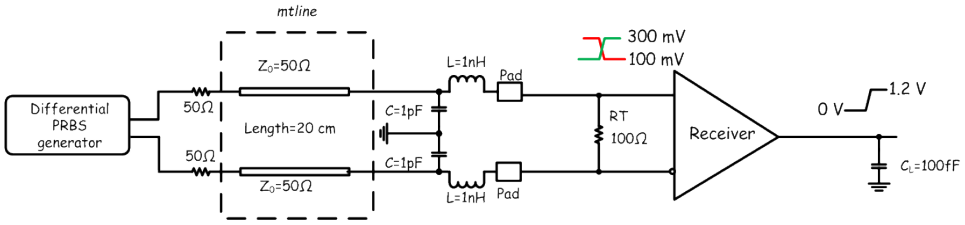


Figure 3.36: test bench used to stimulate the SLVS receiver.

3.5.2 Simulation results

The receiver has been stimulated with the test bench shown in figure 3.36. The differential PRBS generator provides the two voltage levels at the input of the receiver. In particular, the positive voltage is:

$$V_P = V_{CM} + \frac{V_{OD}}{2} \tag{3.12}$$

and the negative voltage is

$$V_N = V_{CM} - \frac{V_{OD}}{2} \tag{3.13}$$

where V_{OD} is the differential input amplitude, while V_{CM} is the input common mode. The differential PRBS generator is composed by two voltage signal sources, which produce two PRBS signals with opposite phase. The two generators are connected to the same microstrip described above. The microstrip output is connected to the bonding inductive model (1 nH) and to a 100 Ω termination resistance. The output of the receiver stage, which consists of two inverters, is connected to a load capacitance of 100 fF. Such a value is the capacitance estimation of the digital part connected to the receiver output.

Figure 3.37 shows the transient response of the receiver when a 1.2 Gbit/s PRBS differential signals is applied at the input for two different temperatures: −20 °C (red line) and 27 °C (yellow line). The differential input signal has a peak-to-peak voltage of 400 mV which is the nominal value for SLVS JEDEC standard. The CMOS output signal at room temperatures goes from 0 to 1.2 V (voltage supply value of the 65 nm CMOS technology). A slight difference can be detected between the waveforms obtained at the two different temperatures.

Figure 3.38 shows the same analysis, this time with the amplitude of the differential input $V_{ID} = \pm 70$ mV. Such a value is the minimum value allowed by the SLVS standard. Also in this case, for the two different temperatures, the receiver is able to detect the input signal.

To verify the capability of the receiver to correctly detect the input signal, the eye diagram at the output of the receiver, shown in figure 3.39,

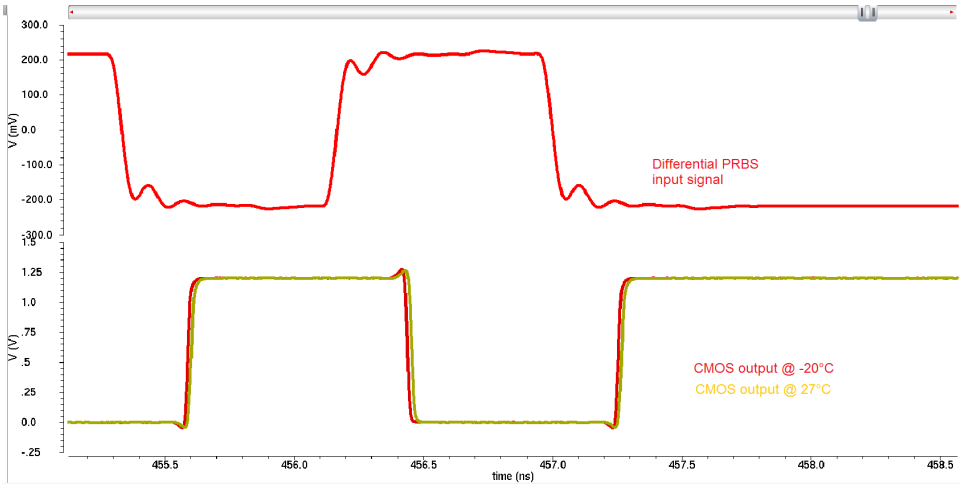


Figure 3.37: top plot is the PRBS differential input of the receiver at 1.2 Gbit/s and peak value $V_{ID} = \pm 200$ mV. The bottom plot is the transient response of the receiver in nominal conditions for two different temperatures, -20 °C (red line) and 27 °C (yellow line).

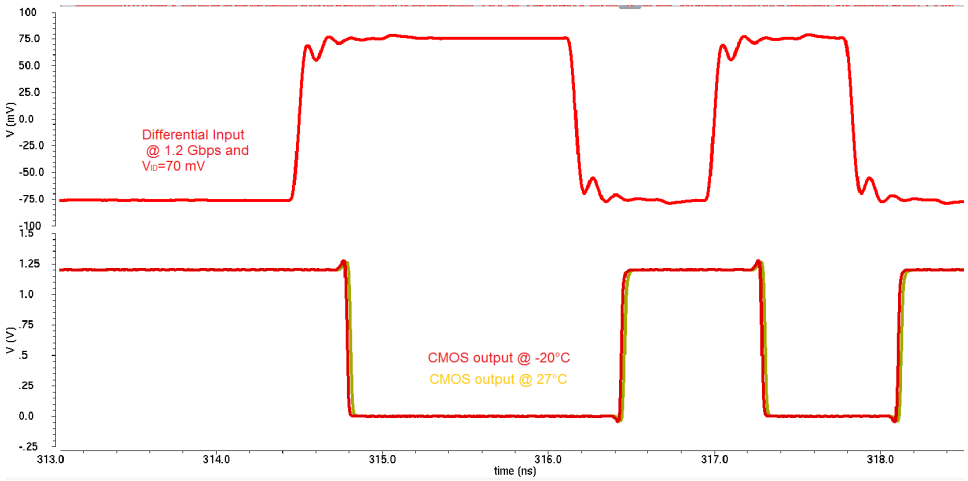


Figure 3.38: output CMOS of the receiver in worst case operating conditions ($V_{ID} = \pm 70$ mV).

can be studied. In this case, the eye diagram is completely open, but the crossing point is slightly larger than 50%. This degradation can result from a duty cycle distortion phenomena. The red waveform in figure 3.39 shows the eye diagram at the temperature of $-20°C$ at the receiver output, which has a peak-to-peak jitter close to 6 ps. The yellow waveform shows, instead, the eye diagram at a temperature of $27°C$. In this case, the peak-to-peak

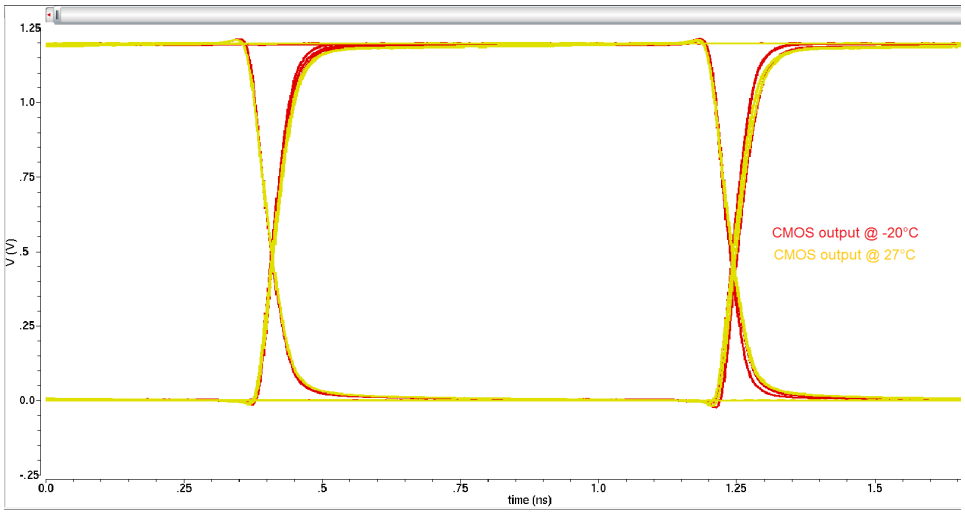


Figure 3.39: eye diagram of the output receiver signal. Stimulated by a PRBS signal 1.2 Gbit/s and differential input signal $V_{ID} = \pm 200$ mV.

jitter is close to 15 ps.

Figure 3.40 shows the output of the receiver when a clock signal at 1.2 GHz at two different temperatures (−20 °C and 27 °C) is applied at the input. Also in this case there is a slight difference between the two responses.

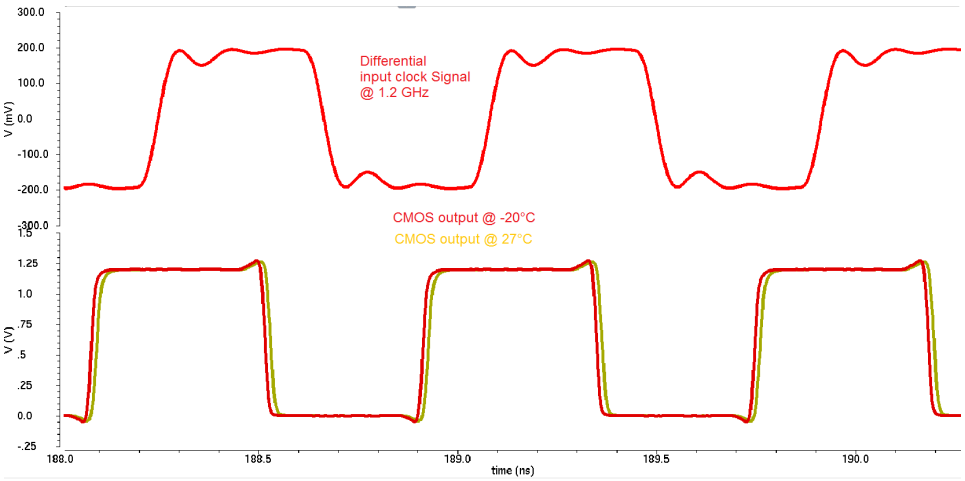


Figure 3.40: transient response of the receiver when a 1.2 GHz clock signal is applied for two operating temperatures: −20 °C (red line) and 27 °C (yellow line).

Table 3.7 illustrates the main parameters of the receiver when a PRBS differential signal at 1.2 Gbit/s is applied at the input.

Table 3.7: comparison of the receiver performance.

Test	Description	Value at 27 °C	−20 °C
PRBS	Rise Time	23 ps	21 ps
	Fall Time	20 ps	18 ps
	Power Consumption	1.5 mW	1.6 mW
	pk-to-pk jitter	15 ps	6 ps
Clock	Duty-Cycle	52.2 %	52.3 %
	Rise Time	24 ps	21 ps
	Fall Time	20 ps	18 ps
	rms abs clock jitter	7.7 ps	8.8 ps

PVT simulations

The SLVS receiver has been simulated in order to evaluate the robustness of the receiver against process, voltage and temperature variations. In particular, in this section the simulation results in the slow (SS, 1.08 V, 100 °C) and in the fast corners (FF, 1.32, −40 °C) are discussed. Figure 3.41 shows the transient response when a differential 1.2 Gbit/s PRBS signal is applied at the input. The slow corner shows a degradation of the crossing point and an increase in the peak-to-peak jitter, due to the strong difference between rise and fall time.

Figure 3.42 shows the eye diagram of the receiver output. In the three cases, the eyes are completely open, which implies a reduction of the bit error rate during the conversion between differential to single ended. Table 3.8 illustrates the main parameters of the receiver in the three different corners.

Figure 3.43 shows the waveform at the output of the receiver for Monte

Table 3.8: comparison of the receiver performance in PVT simulations.

Test	Description	Slow	Nominal	Fast
PRBS	Rise Time	55 ps	24 ps	14 ps
	Fall Time	34 ps	21 ps	13 ps
	Power Consumption	1.1 mW	1.6 mW	2.5 mW
Clock	Duty-Cycle	51.1 %	52.2 %	53.4 %
	Rise Time	55 ps	24 ps	14 ps
	Fall Time	34 ps	21 ps	13 ps
	rms abs clock jitter	16.5 ps	7.7 ps	3.2 ps

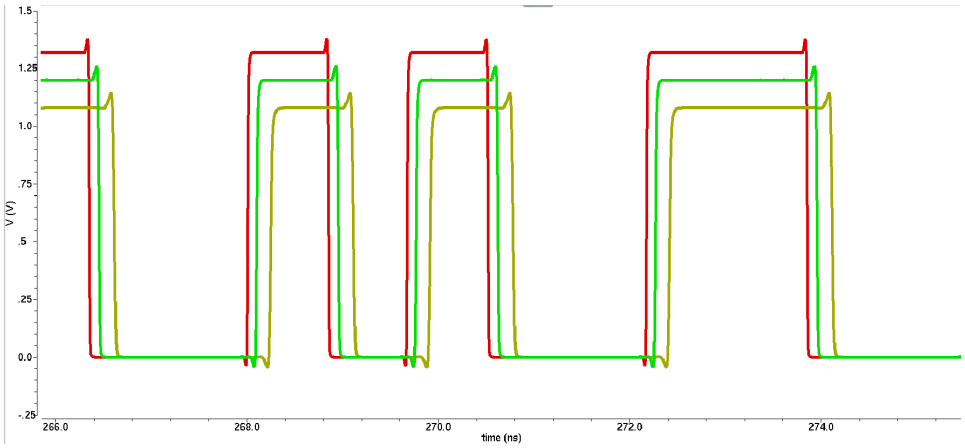


Figure 3.41: CMOS output of the receiver from PVT simulations. Red line refers to the fast corner, green line to the typical corner and yellow line to the slow corner.

Carlo simulations (process+mismatch). The maximum deviation during the transition of the output signal is close to 50 ps.

The layout of the receiver is shown in figure 3.44. The layout has an area of 50 μm x 90 μm. The 100 Ω termination resistance is placed on-chip. In particular, the integrated resistor is made of *rppolywo* and it is located on the left side of the layout. Integrated passive termination resistors are typically realized with unsalicided poly, diffusion, or n-well resistors, but poly resistors are typically used due to linearity and tighter tolerances, but they typically vary $+/-30\%$ over process and temperature [62].

Figure 3.45 shows the complete layout of the chip with the pad-ring for the I/O connections. Two receivers and one driver have been integrated into the chip. Each driver pin has been connected to an analog pad, in order to connect the test signals (i.e., single ended CMOS input and two differential outputs for the driver). Also, the pins of the receiver have been connected to the analog pads. Moreover, the single ended CMOS output of the second receiver is connected to a current mode logic (CML) driver, previously designed and already characterized[63], [64]. This block converts the signal from single ended to CML differential making it possible to measure the signal at the receiver output at high frequency.

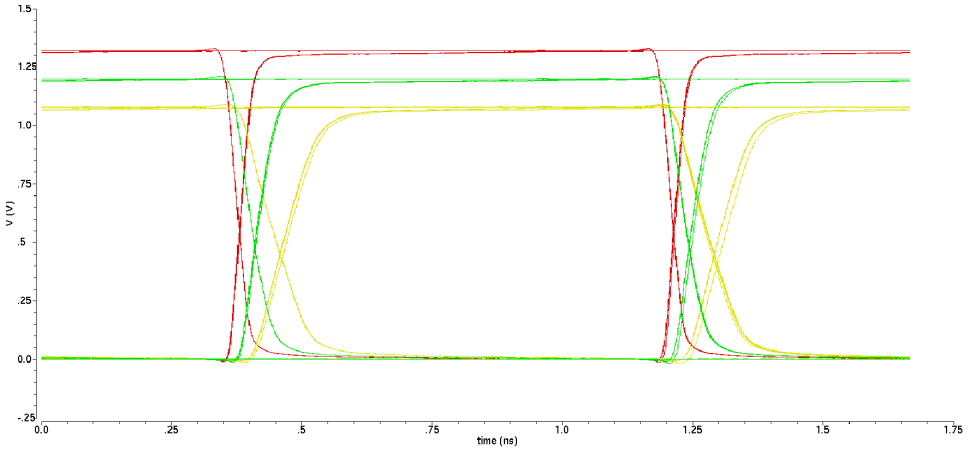


Figure 3.42: Eye diagram of the receiver output from PVT simulations. Red line refers to the fast corner, green line to the typical corner and yellow line to the slow corner.

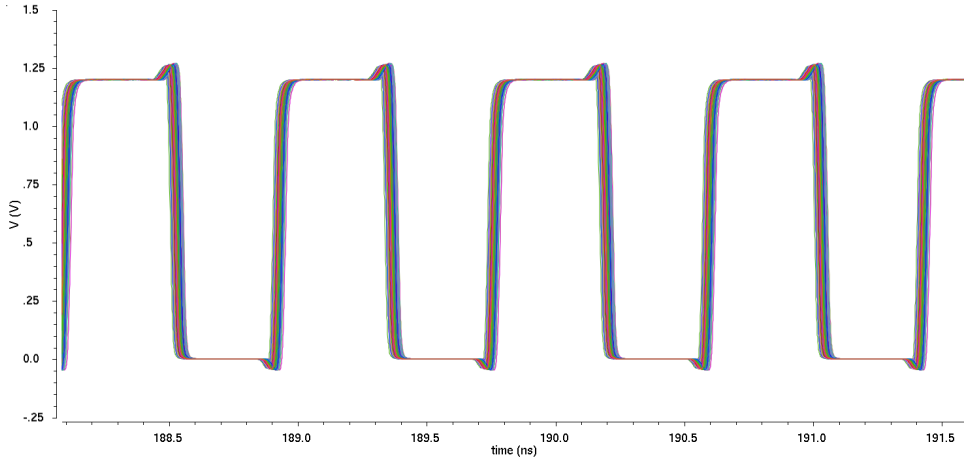


Figure 3.43: Monte Carlo simulation results.

3.6 Characterization and irradiation results

The SLVS driver and receiver designed in 65 nm CMOS technology have been fabricated and characterized. The circuits were also irradiated in order to evaluate their tolerance to TID. In this section, the experimental results will be described and discussed.

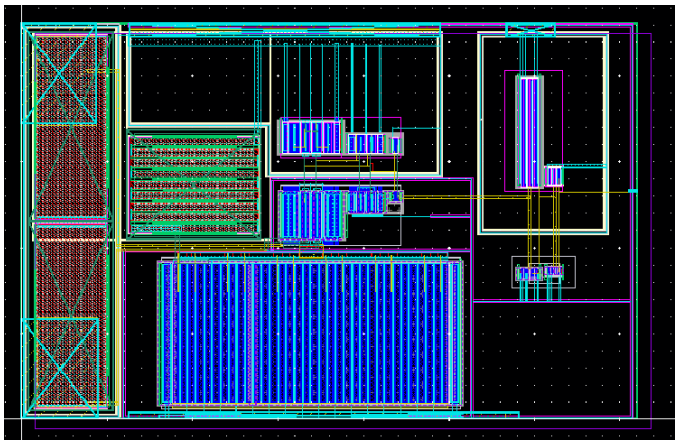


Figure 3.44: layout of the SLVS receiver.

3.6.1 Test setup

In order to carry out systematic measurements, a test system has been purposely developed. The hardware of the test system consists of a PCB: the main board, which hosts two ASICs that will be directly bonded on the PCB. One of the two ASICs, called ASIC1, has the output of the driver connected to the input of the receiver of the second ASIC, called ASIC2. A differential microstrip 5 cm long is used to connect the driver and the receiver. Also the driver of ASIC2 and the receiver of ASIC1 have been characterized. Figure 3.46 shows the structure of the test-bench used to characterize the chip. A signal generator stimulates the input of the driver with a single ended CMOS signal at 1.2 Gbit/s, while it can be used in differential mode in order to stimulate the receiver input. At the same time, using a differential active probe, the eye diagram at the output of the transmitter can be measured by an oscilloscope. Using, instead, a passive probe the single ended CMOS output of the receiver can be measured up to 320 Mbps. Above this frequency, the receiver output has been monitored by measuring the output of the CML driver.

The main board also includes some voltage reference generators and current reference generators. For example, the reference of the driver common mode voltage can be set by means of a voltage reference on the test board.

Figure 3.47a shows the top layer of the main board. Instead, Figure 3.47b shows a blow up of the ASIC area and the differential microstrip, used for the I/O communication with the driver and receiver.

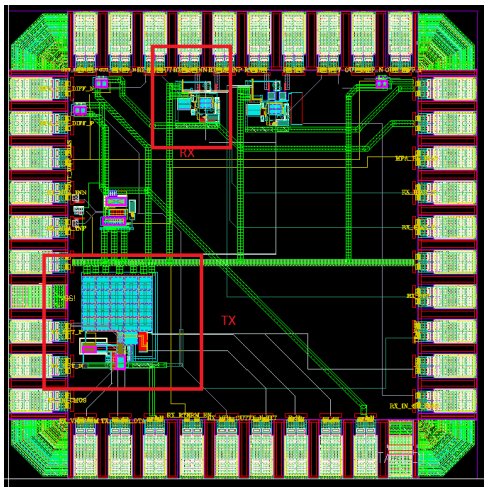


Figure 3.45: layout of the chip with transmitter and receiver (red box) submitted in May 2015.

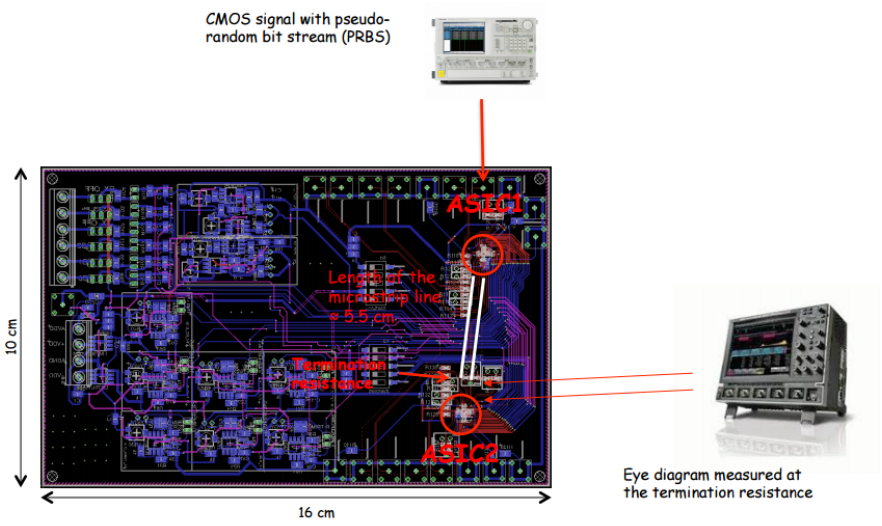
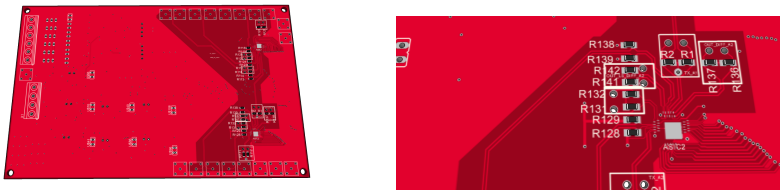


Figure 3.46: block diagram of the test bench setup and PCB test board with two ASICs, which are directly bonded on the PCB.

3.6.2 Experimental results

In this section, the experimental results of the SLVS driver and receiver will be presented and discussed. The first part is dedicated to the characterization before irradiation, while the second part is dedicated to evaluate the



(a) (b)

Figure 3.47: (a) 3D sketch of the PCB test board and (b) zoom of the top layer of the PCB.

performance after irradiation with X-rays.

SLVS Transmitter

The SLVS transmitter has been stimulated with a 1.2V CMOS PRBS signal. A differential active probe has been inserted at the end of the microstrip. Figure 3.48 shows the eye diagram measured at 1.2 Gbit/s. Figure 3.49 shows the differential signal measured at the termination resistance.

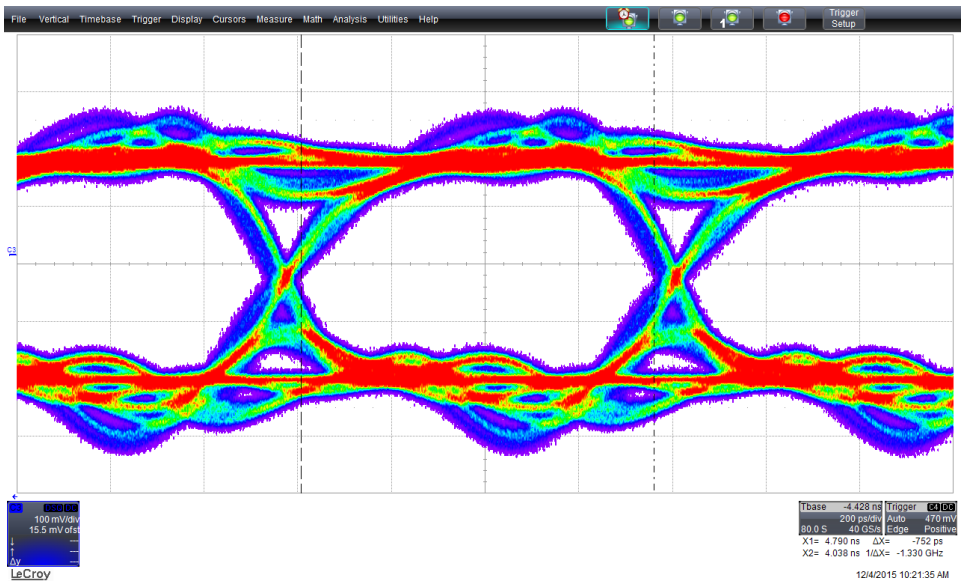


Figure 3.48: eye diagram at 1.2 Gbit/s of the transmitter signal.

The amplitude of the eye is 377.7 mV $\pm$ 3.86 mV, level-1 is 192.5 mV $\pm$ 2.0 mV and level-0 is -216.3 mV$\pm$3.6 mV. The eye height is 365.1 mV. Such values imply a Signal-to-Noise ratio equal to 72, guaranteeing a sufficiently low bit error rate. The eye width, which can be related to the opening, is 752 ps. The ratio between this value and the bit period ($1/1.2{\cdot}10^9 \approx 833$ ps)

Figure 3.49: measurement of the output waveform of the transmitter, with the relevant parameters.

is 0.9. The measured rise time and fall time of the transmitted signal is 309 ps $\pm$ 44 ps and 220 ps $\pm$ 29 ps. The rms jitter measured from the time interval error (TIE)[3] is 9.8 ps. The ratio between the jitter and the bit period is less than 2%.

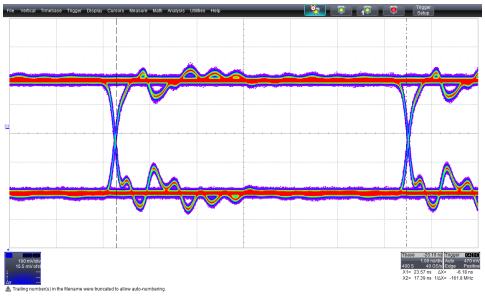
Figure 3.51 shows the output common mode, which is measured in the middle of the termination resistances[4], as a function of the power supply variation. The common mode has a low sensitivity in the range 0.8 V - 1.32 V, the variation of the output common mode being lower than 5 mV.

In table 3.9, the main parameters extracted from the eye diagram at 160 Mbit/s, 320 Mbit/s and 640 Mbit/s are summarized, while figures 3.50a, 3.50b and 3.50c show the relevant eye diagrams.

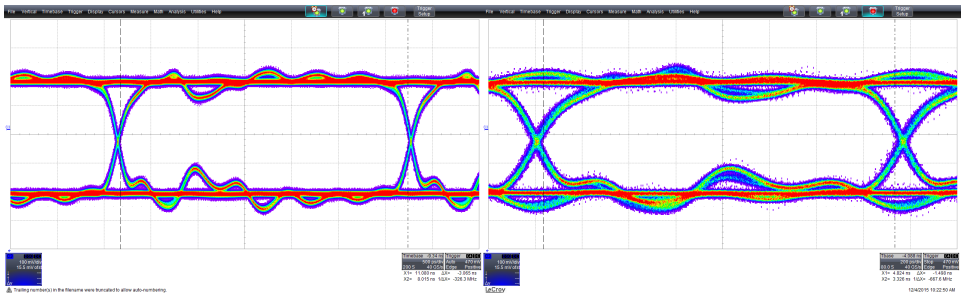
Figure 3.52 shows the clock signal transmitted by the driver. The duty cycle is 52% and the clock jitter measured as TIE is 3.5 ps. In this case, the difference between the jitter measured when at the input is applied a PRBS signal and the clock jitter is due to different noise sources. In the first approximation, the clock jitter (3.5 ps) is caused by the noise of the transmitter, while the jitter measured, when a PRBS signal is injected, is also due to the ISI phenomena. Indeed this jitter increases with the rate. Another jitter component, contributing to the total rms jitter, is the data-dependent jitter.

[3]The TIE is a set of random time interval each one corresponding to the time difference between a real clock or PRBS and a reference ideal signal.

[4]The 100 Ω termination resistance is composed by the series of two 50 Ω resistances



(a)



(b) (c)

Figure 3.50: measurements of the eye diagram of the transmitter at (a) 160 Mbit/s, (b) 320 Mbit/s and (c) 640 Mbit/s.

Table 3.9: eye diagram parameters.

	160 Mbit/s	320 Mbit/s	640 Mbit/s
Amplitude	389.8 mV ± 0.9 mV	389.8 mV ± 1.6 mV	385.6 mV ± 2.3 mV
Level-1	192.9 mV ± 0.5 mV	193.8 mV ± 0.9 mV	192.8 mV ± 1.4 mV
Level-0	−201.1 mV ± 0.7 mV	−195.0 mV ± 0.9 mV	−193.2 mV ± 1.2 mV
S/N	194	155	148
rms jitter @TIE	7.4 ps	6.1 ps	10ps
Rise Time	322 ps ± 16 ps	339 ps ± 15 ps	339 ps ± 24 ps
Fall Time	228 ps ± 11ps	268 ps ± 55 ps	331 ps ± 75 ps

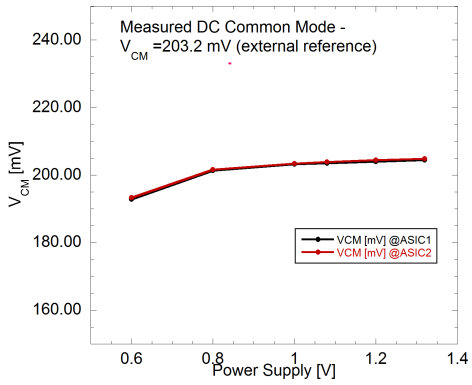


Figure 3.51: measured output common mode voltage (V_{CM}) as a function of the power supply (V_{DD}).

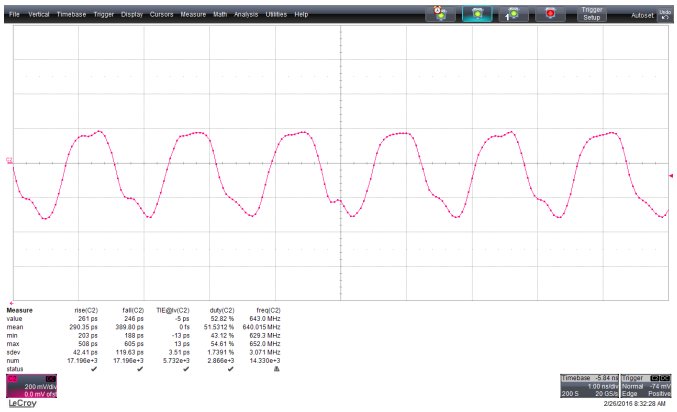


Figure 3.52: measurement of the differential output of the transmitter stimulated by a clock signal at 640 MHz.

SLVS Receiver

The SLVS receiver has been stimulated with a differential voltage PRBS signal at 1.2 Gbit/s and 640 Mbit/s. The 200 mV common mode complies with the JEDEC specifications, while the differential input goes from 100 mV to 200 mV. Measurements have been performed at the output of the CML driver. Figure 3.53 shows the eye diagram of the receiver output in worst case conditions, when the amplitude of the differential input (V_{ID}) is 100 mV. Unfortunately, in this conditions, the eye is partially closed. This closure causes an increment of the bit error rate during bit detection. This eye closure at 1.2 Gbit/s may be related to two independent factors: the first one is the impedance mismatch between the signal generator and the input of the

receiver; the second is a possible under-estimation of the load capacitance at the output of the receiver during the design phase. In the condition considered in figure 3.53, the receiver is not able to drive the load. However, figure 3.54 shows the eye diagram at 640 Mbit/s. In this case the eye is more open than the previous one. The minimum detectable differential signal is 150 mV, as shown in figure 3.55. Figure 3.56 shows the eye diagram in nominal conditions, when 1.2 Gbit/s signal with a differential mode of 200 mV is applied at the input. In this case the eye is open.

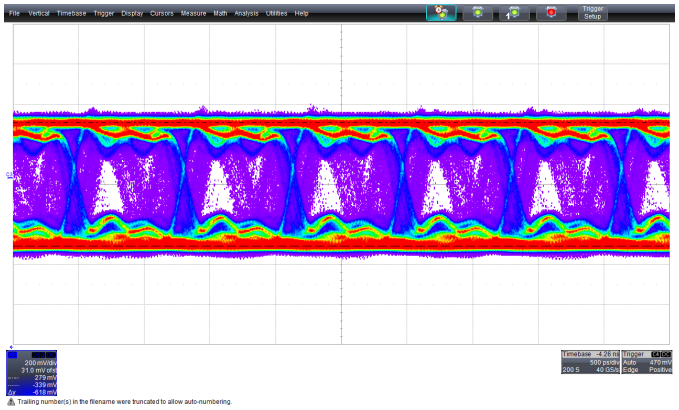


Figure 3.53: eye diagram of the receiver, as a response to a differential PRBS at 1.2 Gbit/s and differential input of $V_{ID} = 100$ mV (worst case condition). The measurement has been performed at the output of the CML driver.

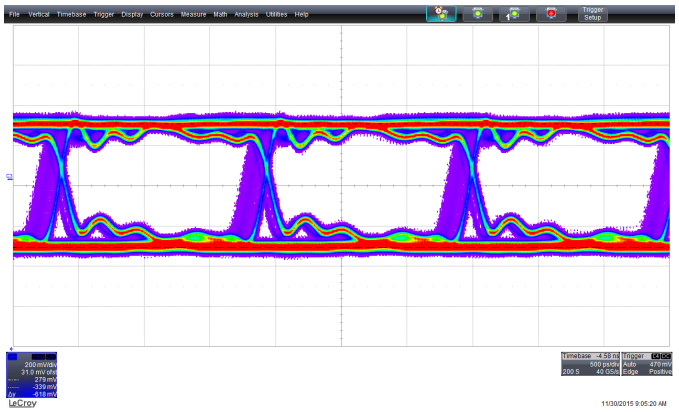


Figure 3.54: eye diagram of the receiver as a response to a differential PRBS at 640 Mbit/s and differential input of $V_{ID} = 100$ mV. The measurement has been performed at the output of the CML driver.

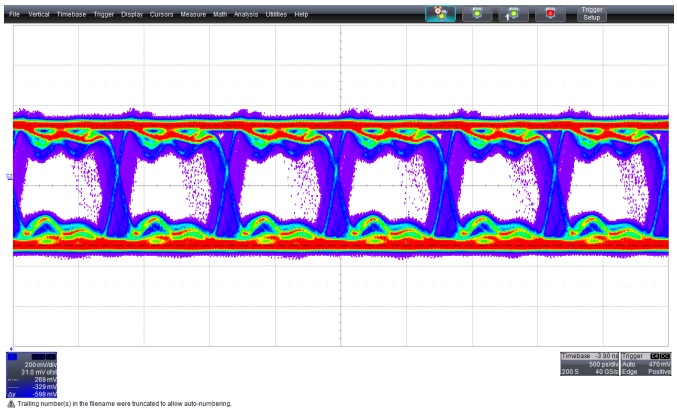


Figure 3.55: eye diagram receiver output, as a response to a PRBS at 1.2 Gbit/s and with $V_{ID} = 150$ mV. This is the minimum detectable signal at 1.2 Gbit/s.

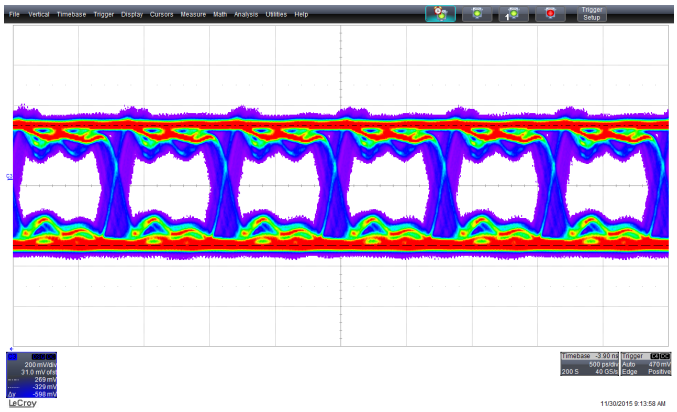
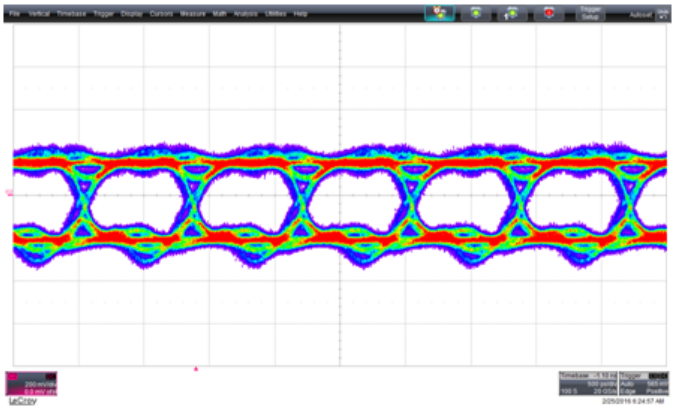


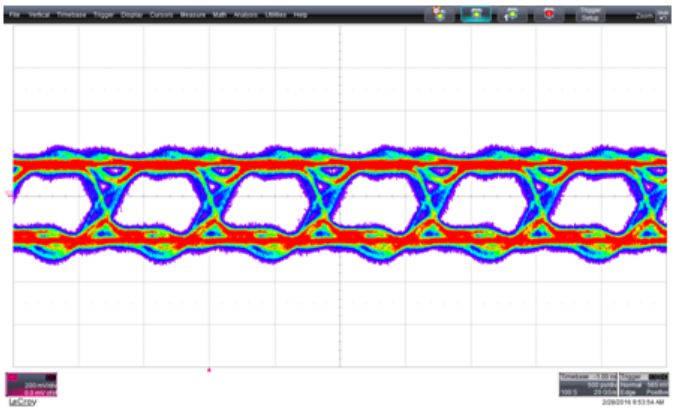
Figure 3.56: measured eye diagram of the receiver in nominal condition at 1.2 Gbit/s.

3.6.3 Irradiation results

A chip with the driver and the receiver was irradiated with X-rays at the CERN facility up to a total ionizing dose of 550 Mrad with a dose rate of 9 Mrad/h. The IP blocks are required to withstand a total dose of 500 Mrad. The eye diagram before irradiation and after irradiation with a TID of 550 Mrad are shown in figures 3.57a and 3.57b. Before irradiation, the eye is completely open and the crossing point is located in the middle of the eye. Figure 3.57b shows instead a partial closure of the eye. Indeed, there is a degradation of the rise time and fall time, but the eye is still open. There is also a degradation of the crossing point. The jitter after the irradi-



(a)

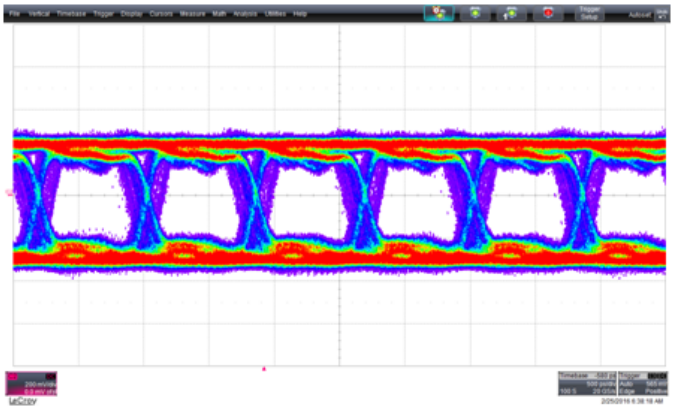


(b)

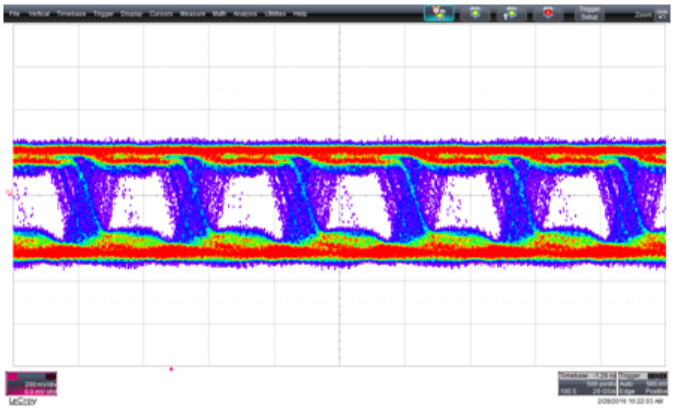
Figure 3.57: eye diagram measurements for the transmitter, stimulated by a 1.2 Gbit/s PRBS signal (a) before irradiation and (b) after irradiation with a TID of 550 Mrad.

ation is degraded from 9 ps to 25 ps, while the degradation of the amplitude is close to 18.7 mV. Indeed, the amplitude is reduced from 377.7 mV to 359 mV. The transmitter still works at the maximum frequency even after irradiation.

Figures 3.58a 3.58b show measurements taken at the receiver output before and after irradiation. After the irradiation, with a TID of 550 Mrad, the eye diagram of the receiver is partially degraded (fig. 3.58b). This can bring to an increase of the bit error rate.



(a)



(b)

Figure 3.58: eye diagram measurements for the receiver, stimulated by a 640 Mbit/s PRBS signal (a) before irradiation and (b) after irradiation with a TID of 550 Mrad.

3.6.4 Jitter components analysis

This section is dedicated to an example on the extraction of the jitter components from the signal at the output of the transmitter. This example is based on the measurements of the jitter as Time Interval Error after irradiation.

As described above, the jitter consists of by the sum of the random jitter (RJ) and of the deterministic jitter (DJ). In other words, the jitter is considered to be composed of normally distributed RJ components and a fixed pair of DJ components. Using the dual Dirac distribution, the dual normal distributions can be obtained using (3.14)

$$PDF(x) = \frac{1}{\sqrt{2\pi}\sigma_L} \exp\left(-\frac{(x-\mu_L)^2}{2\sigma_L^2}\right) + \frac{1}{\sqrt{2\pi}\sigma_R} \exp\left(-\frac{(x-\mu_R)^2}{2\sigma_R^2}\right) \tag{3.14}$$

where the deterministic jitter can be expressed as:

$$DR = \mu_L - \mu_R \tag{3.15}$$

and the random jitter (RJ) can be expressed as the mean of the two standard deviations:

$$RJ_{rms} = \frac{\sigma_R + \sigma_L}{2} \tag{3.16}$$

An histogram of the TIE measurements has been created. Data coming from the oscilloscope have been normalized to $(\frac{x_i-\mu}{\sigma})$. The resulting rms jitter of the TIE is 15.8 ps. The histogram has been interpolated with (3.14). In table 3.10, the parameters extracted from the interpolation are summarized. Figure 3.59 shows the histogram of the TIE measurement.

This analysis enables the possibility to understand and separate the different component of the jitter. In this case, the deterministic jitter is 16.5 ps, while the random jitter is 5.7 ps.

Table 3.10: parameters of the fitted model.

μ_R	5.4 ps
σ_R	3.7 ps
μ_L	-11.1 ps
σ_L	7.7 ps
R^2	0.91
DJ	16.5 ps
RJ_{rms}	5.7 ps

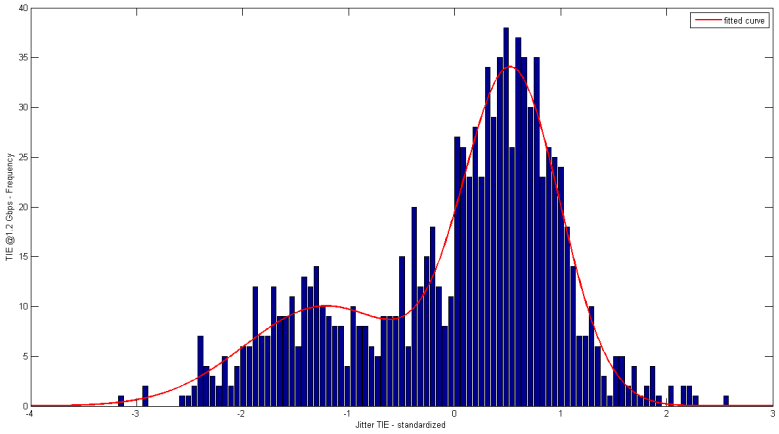


Figure 3.59: histogram of the fitted model.

CONCLUSIONS

In this thesis, the design and characterization of two IP blocks for the RD53A chip demonstrator have been discussed. The activity has been carried out in the framework of the international collaboration RD53, proposed and led by CERN. The main intent of the collaboration is to develop the next generation of hybrid pixel detectors for the upgrade of LHC.

The first IP is a rad-hard bandgap voltage reference, designed in 65 nm CMOS technology with core devices. For these blocks, two versions have been designed. The first one has been designed using the same architecture for three circuits. In each circuit, a different active device (i.e. bipolar transistors, diodes and MOSFETs in sub-threshold region and with enclosed layout) has been used to generate the voltage reference as a function of the temperature. The purpose was to find out the better solution in terms of radiation hardness. The second prototype, based only on MOS in sub-threshold and with enclosed layout, is an improved version of the first one. In particular, in this second version, the biasing current has been increased and a trimming resistor has been included in order to compensate for mismatch and process variations. This solution presents also good performance in terms of temperature insensitivity.

The second IP block designed is a differential I/O link for harsh radiation environments. The IP complies with the SLVS JEDEC specification and was designed using core devices, in order to ensure an adequate radiation hardness. The system was characterized using signals with a data-rate up to 1.2 Gbit/s. The driver can be operated at this data rate both before and after irradiation, while the receiver has good performance at a data-rate up to 640 Mbit/s both before irradiation and after exposure to a TID of 550 Mrad.

Currently, the final demonstrator chip, called RD53A, is being integrated in the framework of the RD53 collaboration and will be submitted in April 2017. The chip includes a pixel matrix of 192 rows x 400 columns, with a

pixel area of 50 μm x 50 μm. A bandgap voltage reference will be included in the monitoring section of the chip, in order to provide the voltage reference for the monitoring ADC. A bandgap voltage reference will also be used to provide bias voltages for the pixels in the matrix. In the IO section, together with the CML transmitter and receiver for data IO, the SLVS transmitter and receiver IP developed in this work will be integrated for slow control commands. The RD53A prototype is the first step towards the design of the final chip for the readout of the innermost pixel layer of the upgraded CMS tracker.

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RINGRAZIAMENTI

In queste ultime righe vorrei ringraziare tutti colori che in questi tre anni mi hanno sopportato con le mie continue insicurezze. Innanzitutto un ringraziamento doveroso è rivolto a Gianluca Traversi, mio tutor e superivisore durante questi tre anni di dottorato. Voglio ringraziarlo per i preziosi consigli e tutta la fiducia che ha riposto in me durante l'attività lavorativa. Inoltre, non posso non ringraziare Lodovico Ratti. Gli sono debitore di una pizza, per tutta l'attività di supervisione della tesi e dei preziosi consigli matematici. Desidero ringraziare inoltre tutte le persone del laboratorio di Microelettronica dell'Università di Bergamo e del laboratorio di Strumentazione elettronica dell'Università di Pavia. Un grazie, in particolare, è rivolto a Massimo Manghisoni, perché senza di lui, questa avventura non sarebbe partita e al Prof. Valerio Re, perché in un momento di sconforto, mi ha convinto a rimanere. Rimangono da ringraziare tutte le persone del laboratorio: Bendetta, Daniele, Elisa, Patrick e Michele per avermi incoraggiato e per avermi ascoltato durante i momenti più difficili. Voglio ringraziare anche Luca, per i momenti condivisi al CERN e a Losanna. Un grazie particolare va alla mia famiglia, in particolare a mio padre e a mia madre, perché hanno sempre creduto in me e alla famiglia della mia fidanzata, i quali mi sono sempre stati vicini e mi hanno incoraggiato. In questi ringraziamenti vanno sicuramente citati i miei amici che riescono sempre a strapparmi delle risate anche quando vedo tutto grigio. In ultimo, penso di dover ringraziare due persone: Luigi Gaioni e Marika Quadri. Il primo perché non è soltanto mio dirimpettaio di scrivania, ma è colui che mi ha insegnato il "mestiere" di designer, per le profonde chiacchierate di statistica o matematica (che a volte non portavano a nulla!), per i profondi consigli, per essere stato correlatore nelle precedenti tesi, diventando una persona fondamentale nella mia vita. Ovviamente, le ultime parole non possono che essere rivolte alla mia fidanzata Marika. Mi è stata vicina ed è colei che più di tutti mi ha sopportato durante le giornate più intense e con la quale sta cominciando

una nuova avventura.

Francesco De Canio