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2G-3G SAW-less Analog Front-End

Supervisor:
Chiar.mo Prof. Rinaldo Castello

Coordinator:
Chiar.mo Prof. Franco Maloberti

Author:
Ivan Fabiano

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Declaration of Authorship

I, Ivan FABIANO, declare that this thesis titled, '2G-3G SAW-less Analog Front-End' and the work presented in it are my own. I confirm that:

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"It can scarcely be denied that the supreme goal of all theory is to make the irreducible basic elements as simple and as few as possible without having to surrender the adequate representation of a single datum of experience."

Albert Einstein

UNIVERSITÀ DEGLI STUDI DI PAVIA

Abstract

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2G-3G SAW-less Analog Front-End

by Ivan Fabiano

This thesis proposes two innovative receivers to handle the 2G and 3G mobile communication standards without the use of external SAW filters. Starting from the standard requirements, a briefly analysis of the overall structure constraints will be presented. A boosted common-gate transformer-based topology in a current-mode architecture is exploit for its high linearity and low noise. A new low-power low-phase-noise divider with 25% intrinsic duty-cycle and a new resonant mixer for harmonic rejection are presented. Each block of the proposed receiver chains is analysed showing the mains peculiarities and weaknesses. Finally the measurements-simulations results of the two test chips fabricated are shown to validate the proposed solutions.

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I certainly have a lot of people to thank but not enough space for all of them. However few people have significantly contributed to my development and this little space is for them.

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To my Family.

Introduction

The mass diffusion of wireless devices, like smart phones, has brought to the coexistence of multiple bands and standards for different applications. The continuous growing of data-speed demand led to an evolution of the standards with more bands to handle and tougher specifications. Nowadays one single smart phone has to manage different applications such as Bluetooth, Wi-Fi and data-voice communications, which can be performed trough different standards. As example data-voice communication today presents three different standards: 2G, 3G and 4G. To handle the coexistence of multiple standards, the complexity, size and cost of the modern wireless terminals is becoming more and more dominated by the very large number of passive components like Surface-Acoustic-Wave (SAW) filters, Duplexer and high Q filters, that are required to separate the applications-standards domains and to discriminate the tiny wanted signal amongst many huge interferers. Another limiting factor is the use of differential inputs in the transceiver to increase immunity to spurious signal that could couple into the signal path. This approach not only increases the pin count but also complicates the board design increasing the overall cost.

Focusing on data-voice communications application, up to 30 bands divided in Time-Division-Duplexing (TDD) and Frequency-Division-Duplexing (FDD) [1, 2] access are present. With the new evolution of 4G more bands are available and thanks to the the carrier aggregation feature, adaptive transceiver are required. Moreover the new releases [3] contemplate the Multiple-Input-Multiple-Output (MIMO) data exchange with up to 8 different antennas, which have to be able to manage all the bands. In this scenario the number of external fixed frequency filters will explode affecting the cost, the complexity and design constrains of the devices. As a matter of fact external filters, like SAW and Duplexer, that are typically used, are bulky and expensive compared to the rest of the device. On top of that a large number of lines, at least one for each filter, have to be route.

Each one of them needs one Input-Output (IO) pad for the connection with the transceiver limiting potentially the integration scaling down and increasing the platform complexity. In this view a SAW/Duplexer-less transceiver is highly desirable and puts a big challenging not only to the industry but also to the research world.

In literature few designs have been developed for TDD access like standards (e.g. GSM) but none of them is commercially attractive due to the poor performances in terms of sensitivity, power consumption or blocker resilience. On the other hand in the FDD access like world (e.g. W-CDMA) only Duplexer-less architecture demonstrators have been developed, just able to show a possible path to follow but nothing more. A complete transceiver able to meet all the requirements for TDD and FDD has not been designed yet.
Being able to operate with a single ended signals, removing both SAW and Duplexer, at least in some bands, while maintaining good performances and satisfying the specifications for both 2G and 3G standards is the main goal of this work.

Chapter 1 will present an overview on the modern implementation of the typical commercial device focusing on the platform design constrains. It will then explain the standard specifications for the SAW-less transceivers with particular regards for 2G-3G standards.

Chapter 2 will present a novel design for a 2G SAW-less receiver explaining the basic implementation and function of all the chain blocks and finally presenting the measurements.

Chapter 3 will focus on a possible implementation of a 3G Duplexer-less architecture based on the structure proposed in Chapter 2 and able to meet the specifications required, presenting simulation results to validate the idea.

Chapter 1

Standards requirements and design challenges

Wireless communications are regulated by standard protocols that define the specifications for the physical device. In order to manage all the standards and meet all the requirements the mobile devices, like smart-phones, need a large number of external filters (e.g. SAW and Duplexer) as explained in Section 1.1. In this Chapter the specifications required for a SAW-less receiver implementation will be addressed focusing on the 2G standard in Section 1.2 and on the 3G standard in Section 1.3.

1.1 Data-Voice Standard Platform Configuration

Nowadays high performance mobile phones manage different standards, 2G-3G-4G, to meet the multiple needs of the users such as: fast data transfer, power saving and territory coverage. Switching from one standard to an other, is possible to meet all the requirements with only mobile handset. The number of frequencies and the coexistence of multiple standards put some challenge/limit to the platform performances and cost. Indeed, high performance wireless receivers invariably use external SAW filters to attenuate out-of-band blockers before they reach the Low-Noise Amplifier (LNA) input in order to relax the receiver requirements. For TDD systems such as GSM (2G), isolation between transmitter (Tx) and receiver (Rx) is provided by the Tx/Rx switch and not by the SAW. On the other hand, in FDD systems like W-CDMA (3G) the external SAW performs both filtering and

duplexing (Figure 1.1).
Both, FDD and TDD, have multiple operation bands [1, 2], from 400MHz up to 2.4GHz, which require almost one filter for each band. For new LTE releases, 10 and higher, up to 8 antennas for MIMO are contemplate [3] to meet the high data rate demand. Each antenna can work on all the frequencies thus requiring a large number of external passive components as depicted in Figure 1.1.
In this scenario the cost and the performances are affected. The external filters are bulky, requiring an extensive routing that could even corrupt the sensitivity or demand a lower NF to compensate the losses associated to long lines. The cost is therefore determined by the filters themselves and the complexity of the board, significantly impacting on the overall Bill-of-Material (BOM).

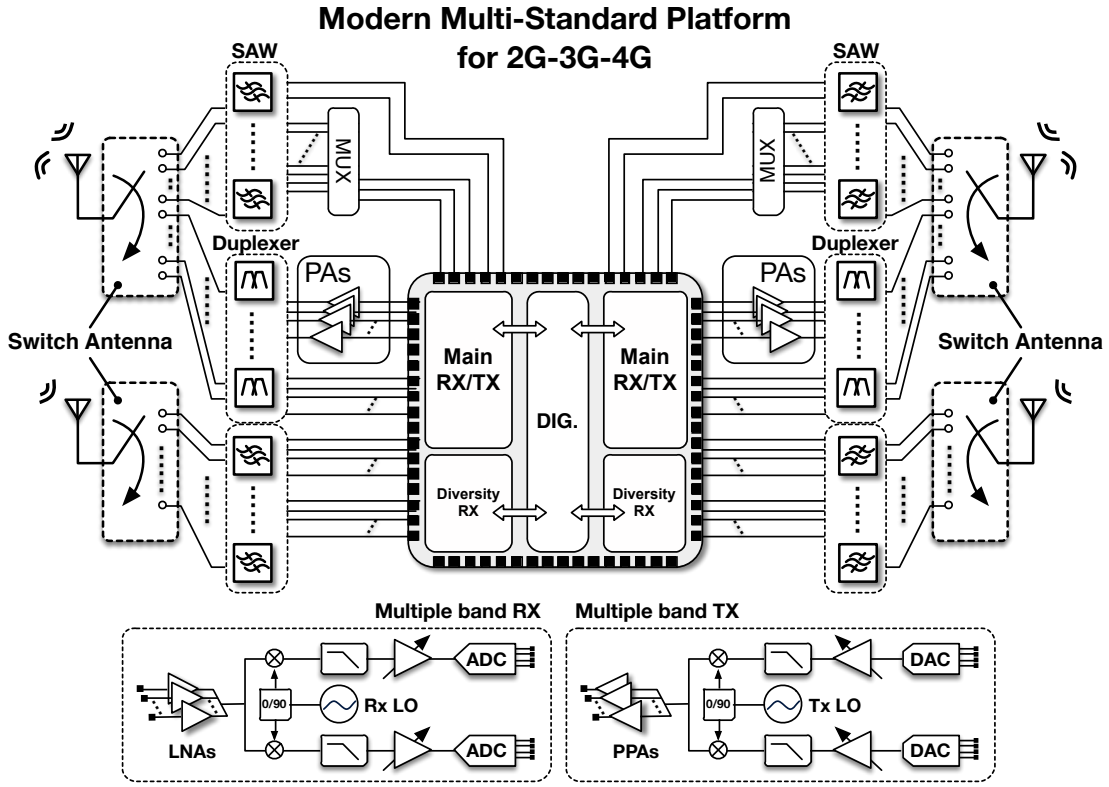


FIGURE 1.1: Antenna-Chip interface.

Another critical aspect is the scalability of the C-MOS process that could be compromised due to the large number of Input-Output (IO) PADs required for the external filter and Rx-Tx connections. The dimensions of the chip could be potentially limited by the IO PADs space occupation and thus not have any benefit from the technology scaling down. This condition is in contrast with the past and current trend of the microelectronics industry to reduce the cost reducing the area

for same functionality with new super-scaled technology. A big effort has been made to produce architecture with the digital part of the transceiver closer to the antenna [4, 5] in order to exploit the benefits of the technology scaling down but the antenna-chip interface still represents the bottleneck of such an approach making very desirable to eliminate any external filter.

1.2 Second-Generation (2G) wireless standard and SAW-less challenges

The standard defines the performances of both Base Station (BS) and User Equipment (UE) across different scenarios. Several parameters are defined but for this thesis purpose only sensitivity, bandwidth and blockers for UE will be taken in account.
The sensitivity defines the minimum detectable input signal power level for a given output Signal-to-Noise-Ratio (SNR) necessary to obtain the required Bit-Error-Rate (BER) and can be expressed by Equation (1.1).

$$S_{dB} = 10 \cdot log(K_B T_0 \cdot B) + NF + SNR_{min} \tag{1.1}$$

Where K_B is the Boltzmann constant, T_0 is the temperature expressed in Kelvin, NF is the noise figure of the system and SNR_{min} is the minimum signal-to-noise ratio required. The minimum SNR is determined by the modulation technique adopted and the BER required. From the data provided by [1] is thus possible to calculate the NF of the overall system by Equation (1.1), which results to be lower then 7dB.
The channel bandwidth and the channel spacing is set to 200kHz. For each band a set of in-band and out-of-band blockers are defined. In Figure 1.2 is reported as example the blocking profile mask of the DCS-1800 band [1]. The in-band blockers are modulated signals with a relative low power level. The out-of-band blockers, instead, are Continuous-Wave (CW) signals with a large amount of power up to 0dBm. The CW blockers test mainly cause compression issues instead of intermodulation. As stated in Section 1.1 external SAW filters are used to attenuate these interferes and to convert the signal from single ended (SE) to differential, thus relaxing the Rx performances.

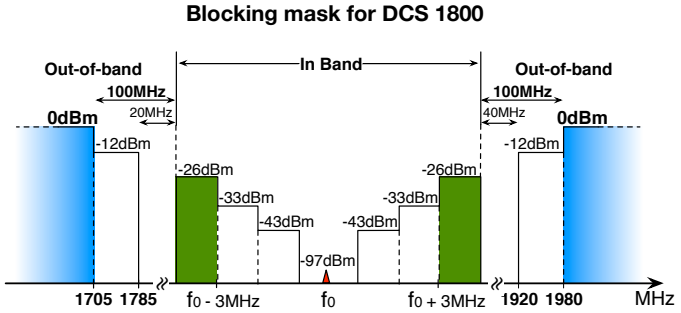


FIGURE 1.2: Example of blocking mask profile for 2G standard.

Without external SAW, it would be very desirable to use a SE input receiver and connect it to the antenna (through the Tx/Rx switch). This lowers cost, reduces complexity/form-factor and improves the sensitivity. Indeed, without fixed frequency RF filters, it is possible to use a single wide-band receiver in place of multiple narrow-band ones. Furthermore, eliminating the attenuation associated with the SAW/bal-un, a SAW-less single ended transceiver can have a NF 2 to 3dB higher than a classical one and still achieve the same sensitivity.
On the other hand, without RF filtering some of the classical problems of wireless receivers are exacerbated i.e. gain compression, intermodulation, reciprocal mixing, harmonic mixing and noise folding.

1.2.1 Gain Compression

The non-linear behaviour of a device can be approximated with a sum of powers series as:

$$y(t) = a_1 \cdot x(t) + a_2 \cdot x^2(t) + a_3 \cdot x^3(t) \tag{1.2}$$

Considering an input signal $x(t) = A \cdot \cos(\omega_0 t)$, Equation (1.2) becomes:

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 + \frac{3a_3 A^3}{4}\right)\cos(\omega_0 t) + \frac{a_2 A^2}{2}\cos(2\omega_0 t) + \frac{a_3 A^3}{4}\cos(3\omega_0 t) \tag{1.3}$$

The gain at the fundamental frequency ω_0 depends on both linear and non-linear coefficients. If the input signal increases, desensitization can occur. However, since no RF filtering is provided, the gain compression can occur even with an out-of-band continuous wave blocker, due to either limited current range (slewing) or limited voltage range (clipping) at RF and/or at Base Band (BB) causing desensitization. Through the same mechanisms two or more out-of-band interferers can generate intermodulation products that fall in band as it will be shown in

Section 1.3.1. A blocker tolerant receiver should, therefore, have the lowest LNA transconductance (to avoid slewing when a class A LNA is used) and the smallest voltage gain throughout the RX chain (to avoid clipping) while maintaining good sensitivity [6, 7]. Furthermore the BB should have the largest possible dynamic range i.e. the ratio between the maximum out-of-band signals that it can handle and the in band noise [4, 5].

1.2.2 Reciprocal Mixing

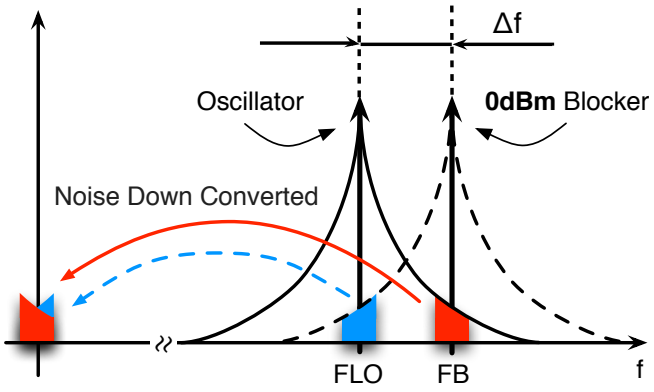


FIGURE 1.3: Reciprocal mixing effect.

Reciprocal mixing is due to the down-conversion of the LO phase noise by the blocker as shown in Figure 1.3. The convolution between blocker and LO down-convert in band either the noise produced by the LO and the noise associated to the blocker. The last one should be filtered during the test since a pure CW tone is required by the standard. It follows that in a SAW-less receiver, to preserve the NF, the LO phase noise must be reduced by the amount of filtering originally provided by the SAW [8]. Small LO phase noise implies large power consumption in the VCO/PLL and in the clock phases generation/distribution blocks, which is not acceptable.

1.2.3 Harmonic Mixing

Finally harmonic mixing/noise folding occurs since down-conversion is done multiplying the RF signal by a square wave. As shown in Figure 1.4 the odd harmonics (for a differential topology) of the LO frequency present in the square wave clock, folds to BB any signal located at these harmonics. 3GPP requires

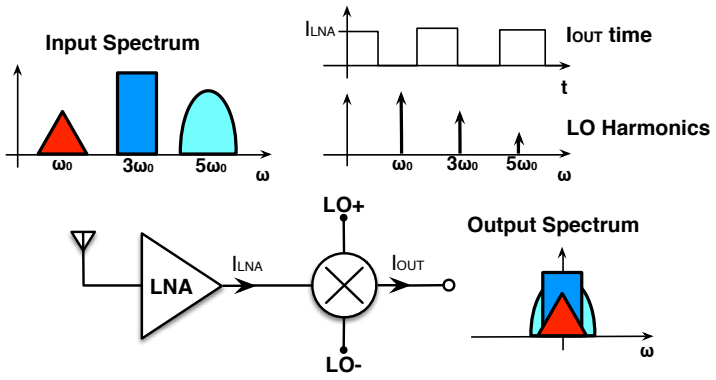


FIGURE 1.4: Harmonic mixing effect.

coexistence with blockers located at all multiple frequency as shown in Figure 1.2 of the channel spacing allowing, however, some exceptions. To limit the number of required exceptions, LO phase noise should be low and harmonic rejection mixing and/or filtering at the LO harmonics should be implemented. On the other hand, noise folding occurs even when no blocker is present and can only be reduced by minimizing the noise energy at the LNA output at the clock harmonics. Chapter 2 will show how, through architecture and circuit innovations, all the above critical problems can be addressed without incurring in large power consumption penalties.

1.3 Third-Generation (3G) wireless standard and Duplexer-less challenges

While 2G is voice-centric, with some data connectivity (SMS and fax), the 3G standard aims to enabling a broadband Internet access with high-speed data transfer capability. For this purpose the channel bandwidth is increased to 2MHz claiming a data-exchange capability up to 2 Mb/s for a stationary user. Since each channel occupies a larger band a W-CDMA is adopted to increase the number of simultaneous users. Tx-Rx separation is made trough FDD enabling a *full-duplex* communication. An external duplexer is used to discriminate between the two close frequencies of Tx and Rx signals and relax the receiver performances. In Figure 1.5 are reported three examples for three bands that represent as many scenarios. Two main aspects are changing: Tx and Rx frequency separation and the most powerful CW blocker frequency position. In Figure 1.5(a) the -15dBm CW interferer can be present up to the Half Duplex (HD) frequency while in

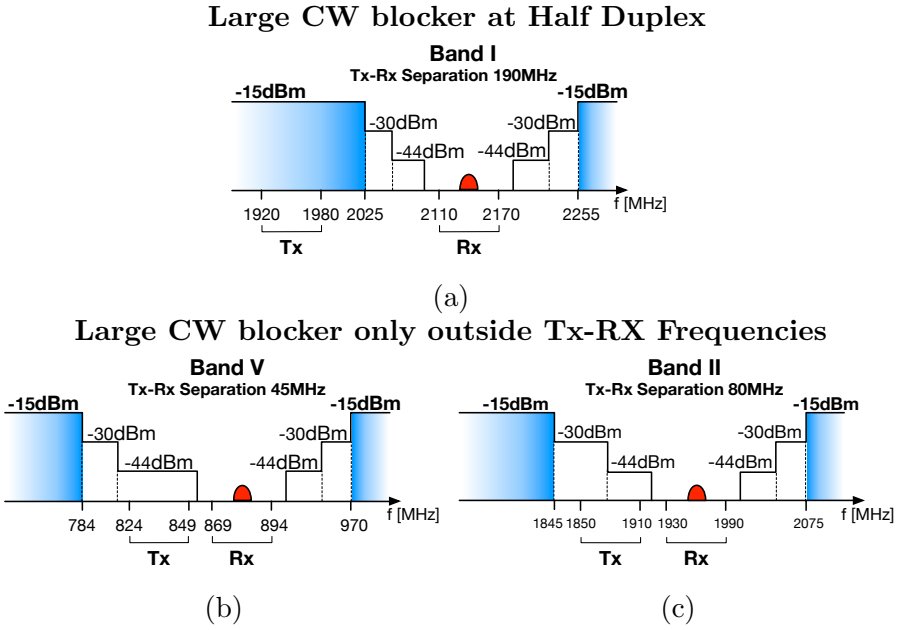


FIGURE 1.5: Bloking profile masks for:(a) band with CW blocker at HD, (b) and (c) bands w/o CW at HD but with different Tx-Rx frequencies separations.

Figure 1.5(b) and 1.5(c) is present only outside the Tx-Rx Frequencies.
The main function of the duplexer is to separate the Tx and Rx signals, thus filtering out the Tx noise and the CW interferes in the Rx band. The most critical case is due to the CW at half duplex because the attenuation provided by the duplexer is decreasing [9] hence making the linearity requirements more demanding.

Typically, due to the finite isolation of the duplexer, the strong Tx signal leaks to the Rx input, causing two issues: NF degradation due to Tx noise falling in the Rx band and Rx desensitization due to the front-end third-order non-linearity caused by the large out-of-band blocker (for example the blocker at half-duplex frequency) mixing with the leakage itself [9].

As explained in Section 1.2 eliminating the external and bulky filter leads to undeniable benefits but enhance the already tough requirements. Additionally to the challenges introduced in Section 1.2, for 3G case also the *linearity* performances and lifetime (due to high voltage of the Tx signal) of the transceiver are exasperated, moreover the SAW filter performs also the duplexing function for Tx-Rx that should be somehow implemented.

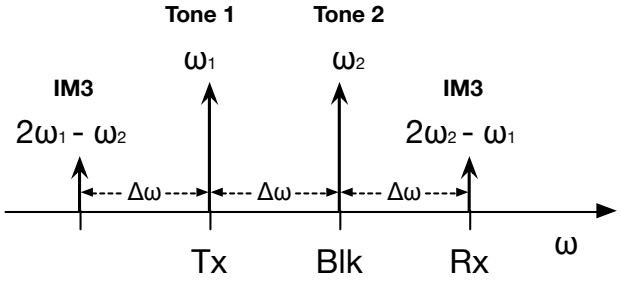


FIGURE 1.6: Third order intermodulation effect.

1.3.1 Non-linearities: Intermodulation and desensitization

Considering again a non-linear device whose transfer function can still be represented by Equation (1.2) and applying two signals with different pulsations ω_1 and ω_2, spurious emission can be seen at the output. The characteristic represented by Equation (1.2) can lead to different non-linearities that can cause: desensitization (explained in Section 1.2.1), cross-modulation and intermodulation. While desensitization is less demanding for 3G mask blocking profile (the CW blocker is -15dBm instead of 0dBm of 2G standard) as well as the cross-modulation effect, intermodulation can originates products that fall in Rx band.
Considering an input signal $x(t) = A_1 \cdot cos(\omega_1 t) + A_2 \cdot cos(\omega_2 t)$ and expanding the Equation (1.2) is possible to isolate few interesting terms (see Appendix A for full calculation):

$$y(t) = a_1 A_1 cos(\omega_1 t) + a_2 A_2 cos(\omega_2 t) + \cdots + \\ + \cdots + \frac{3a_3 A_1 A_2^2}{4} cos(2\omega_2 - \omega 1)t + \frac{3a_3 A_1^2 A_2}{4} cos(2\omega_1 - \omega 2)t + \cdots \quad (1.4)$$

The first two terms represents the tones at the output due to the linear component. The tones at $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$ are the third order products. These components, if $\omega_1 \simeq \omega_2$, are close to the linear ones. In Figure 1.6 is represented a case in which ω_1 is the Tx center pulsation while ω_2 is the CW blocker pulsation and one of the intermodulation products (IM3) falls exactly in the Rx band. In this scenario is possible to calculated the IIP3 necessary to obtain a given sensitivity (assuming that all the NF degradation is due only to non-linearities Appendix A) as follows:

$$IIP_{3,HD} = \frac{P_{Tx} + 2 \cdot P_B + SNR - (Sensitivity + 3dB)}{2} \quad (1.5)$$

TABLE 1.1: IIP3 performances at the Antenna for 3G standard.

Band	Tx Band [MHz]		Rx Band [MHz]		Spacing [MHz]	out-of-band Blocker (-15dBm) [MHz]				Sensitivity [dBm/3.84MHz]	$IIP_{3,HD}$ [dBm]	$IIP_{3,FD}$ [dBm]
	min	max	min	max		min	max	min	max			
1	1920	1980	2110	2170	190	1	2025	2255	12750	-117	46.5	67.5
2	1850	1910	1930	1990	80	1	1845	2075	12750	-115	-	66.5
3	1710	1785	1805	1880	95	1	1720	1965	12750	-114	-	66
4	1710	1755	2110	2155	400	1	2025	2240	12750	-117	46.5	67.5
5	824	849	869	894	45	1	784	979	12750	-115	-	66.5
6	830	840	875	885	45	1	790	970	12750	-117	-	67.5
7	2500	2570	2620	2690	120	1	2570	2775	12750	-115	-	66.5
8	880	915	925	960	45	1	840	1045	12750	-114	-	66
9	1749.9	1784.9	1844.9	1879.9	95	1	1759.9	1964.9	12750	-116	-	67
10	1710	1770	2110	2170	400	1	2025	2255	12750	-117	46.5	67.5
11	1427.9	1447.9	1475.9	1495.9	48	1	1390.9	1580.9	12750	-117	-	67.5
12	699	716	729	746	30	1	644	831	12750	-114	-	66
13	777	787	746	756	31	1	661	841	12750	-114	-	66
14	788	798	758	768	30	1	673	853	12750	-114	-	66
15	Reserved		Reserved		Reserved	Reserved				Reserved	Reserved	Reserved
16												
17												
18												
19	830	845	875	890	45	1	790	975	12750	-117	-	67.5
20	832	862	791	821	41	1	706	906	12750	-114	-	66
21	1447.9	1462.9	1495.9	1510.9	48	1	1410.9	1595.9	12750	-117	-	67.5
22	3410	3490	3510	3590	100	1	3425	3675	12750	-114	-	66
23	Reserved		Reserved		Reserved	Reserved				Reserved	Reserved	Reserved
24												
25	1850	1915	1930	1995	80	1	1845	2080	12750	-113.5	-	65.75
26	814	849	859	894	45	1	774	979	12750	-113.5	-	65.75

Where P_{Tx} is the Tx power, P_B is the blocker power and SNR is the signal-to-noise-ratio necessary for a given BER.
In a SAW-less 3G receiver the complementary situation (Tx at blocker pulsation and vice versa) is even more demanding in terms of linearity requirements since the IIP3 is given by:

$$IIP_{3,FD} = \frac{2 \cdot P_{Tx} + P_B + SNR - (Sensitivity + 3dB)}{2} \tag{1.6}$$

The Equation (1.5) and (1.6) represent the IIP_3 for *half-duplex* (HD) and *full-duplex* (FD) case respectively. Since the Tx is the most powerful signal (24dBm instead of -15dBm of the CW blocker) the linearity requirements is more demanding for the *full-duplex* case. In Table 1.1 are reported the calculated IIP3 for both cases at the antenna (no attenuation for Tx or CW) assuming the full power transmission delivered (+27dBm at Tx port), the nominal sensitivity increased by 3dB and a SNR of -18dBm (21dB of process gain are required) [9].

The required linearity of the active part (e.g. the LNA) depends on the amount

of filtering provided by the duplexer on both Tx signal and CW tone. In a SAW-less design, while the CW blocker passes unaltered, the Tx signal can be balanced (see Chapter 3) providing an equivalent amount of attenuation and a *duplexing* behaviour. Figure 1.7 shows the IIP3 for *half* and *full duplex* considering the equivalent power that hit the active part. In order to meet the achievable per-

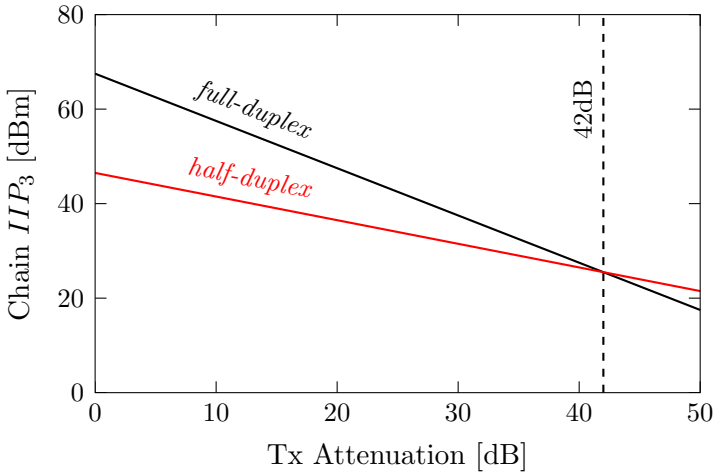


FIGURE 1.7: IIP_3 required by the receiver as a function of the Tx attenuation.

formances of the state-of-the-art integrated front-end (assuming 1.8V supply), at least 40dB of Tx attenuation are required. It follows that the same considerations explained in Section 1.2.1 should be followed for a 3G Duplexer-less design.

1.3.2 Transmitter noise leaking

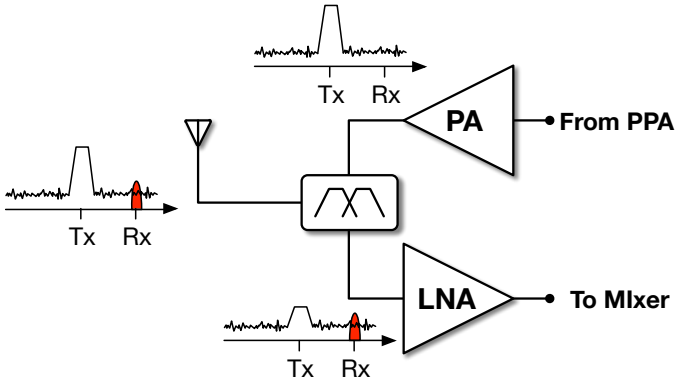


FIGURE 1.8: Tx noise leaking on Rx side.

Another fundamental aspect is the out-of-band noise of the transmitter that leaks back to the receiver. This noise is directly added to the overall noise degrading the NF. While in ordinary front-end it is filtered by duplexer, thus relaxing the noise performance of both Tx and Rx, in SAW-less design should be balanced (see Chapter 3) as well as the Tx signal in order to limit the impact on the overall NF.

1.3.3 Lifetime

The 3G standard specifies a maximum output power level of 24dBm at the antenna. A modulation with a typical peak-to-average ratio of 3.2dB will induce 15V peak-to-peak swing at the antenna. While this voltage can be handled by passive components (e.g. capacitor, inductor and poly-resistor), for the active part can lead to a breakdown of the MOS transistors directly connected to the antenna (e.g. the input LNA MOS transistors) if not properly designed [10]. Isolation should be provided in order to guarantee acceptable voltage level. In Chapter 3 will be shown how the Tx signal can coexist in the same substrate of the receiver with no penalties in terms of lifetime performances.

Chapter 2

SAW-less Analog Front-end

In this Chapter a briefly introduction of the evolution of the 2G SAW-less receivers and the proposed architecture are presented 2.1. A novel architecture is analysed focusing on the main building blocks. First the Low-Noise-Transconductor-Amplifier is introduced showing the trade-off and the limitations 2.2. In Section 2.3 it will then shown an intrinsic 25% duty-cycle divider with improved power performances that drives a new resonant mixer to improve the harmonic rejection. The last stage of the implemented chain (the BB) is presented in Section 2.4, analysing the main design constraints. Finally the prototype and measurements results are presented 2.5.

2.1 SAW-less receiver: State-of-the-art

Over the years there has been an evolution of the architecture of wireless receivers and today the *de-facto* standard is shown in Figure 2.1. It is made up of a transconductance LNA (LNTA) that drives a current mode passive mixer followed by a low input impedance filter or TIA. Such an architecture was studied by Redmann-white [11] and was first implemented at GHz frequency by Sacchi et al. [12]. Later many other have used it [8, 13, 14] to improve linearity and save power. The advantages of this architecture stem primarily from the fact that most of the voltage gain is moved to BB after a certain amount of filtering has occurred. Furthermore the I and Q mixers are almost invariably driven by non-overlapping 25% clock. Such an approach complicates phase generation and

distribution but its better noise for both mixer and BB [15, 16] and larger conversion gain, makes it the solution of choice. More recently the close correspondence between a multi-phase passive mixer and a switched capacitor n-path filter has been pointed out [17] and its potential for implementing high Q band-pass filters analytically demonstrated [18].

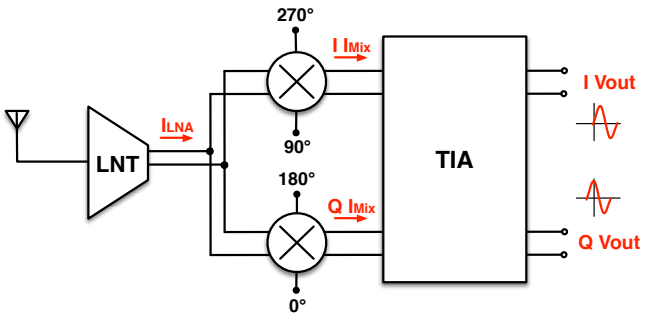


FIGURE 2.1: Current-mode receiver chain.

Leveraging the architecture of Figure 2.1 [12, 19, 20], wireless receivers have gone from narrow to wide-band at the cost, however, of increased noise and/or power consumption [8]. Examples are the so-called mixer first topology [21, 22] that eliminates the LNTA from the RX path or some SAW-less architectures [23, 24].

Recently another step toward the so-called Software Defined Ratio (SDR) has been taken by the Blocker-Tolerant, Noise-Cancelling Receiver [8] that extends noise cancelling to the entire front-end. While the original noise cancelling LNA [19, 25] implements broad-band voltage gain (at the risk of clipping), the new receiver uses two noise cancelling front-ends operated in the current domain. Harmonic mixing is cancelled with an 8 phases harmonic rejection mixer whose outputs are summed in the TIA. The RF front-end achieves excellent antenna sensitivity (1 to 2dB better than traditional receivers with external SAW), which degrades by only about 2dB with a 0dBm blocker. However, even with a SE signal path, it requires about 65mW at 2GHz and 1.2 mm^2 in 40nm CMOS. Furthermore the SE circuit gives only around 50dBm IIP2 and is susceptible to spurious couplings since simple inverters are used as gain stages.

As a further step in this evolution this thesis report a SAW-less SE receiver with excellent linearity and blocker tolerance together with a good mix of sensitivity and bandwidth. Compared with the best of the art [8] it has a narrower band and a larger NF but provided that the correction of the transformer errors yields

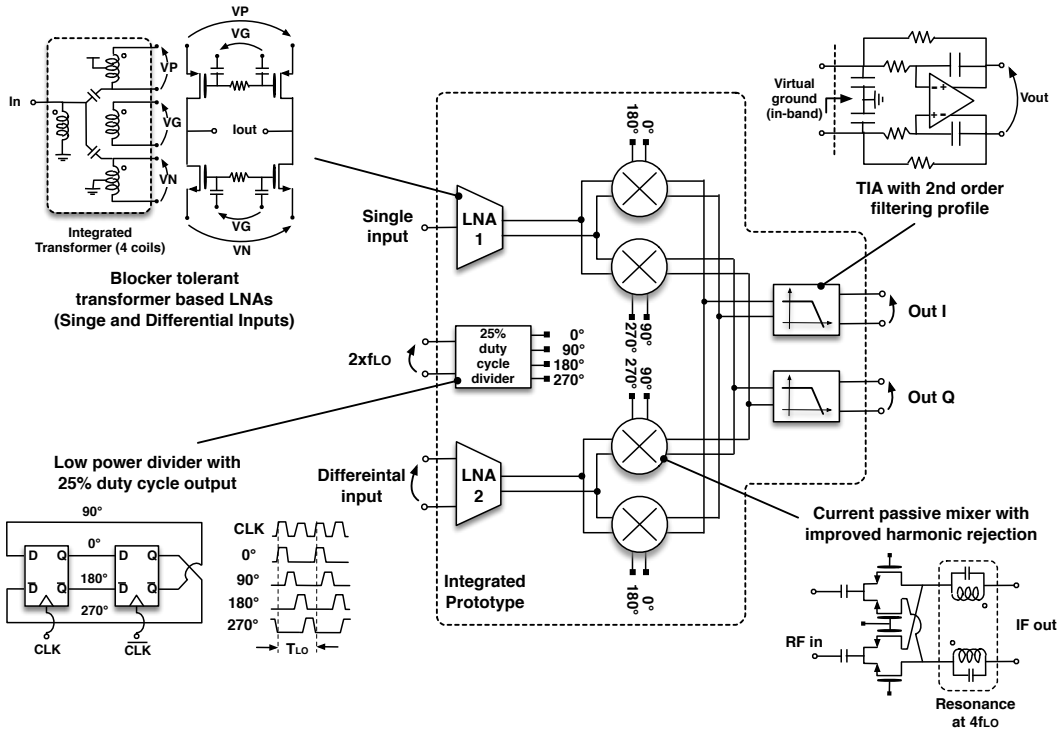


FIGURE 2.2: Proposed receiver chain block diagram.

the expected results has the potential to be used in commercial smart phones. On the other hand, it requires much less power and area while offering much better disturbance immunity thanks to the use of a fully differential (FD) signal path. Good harmonic rejection is obtained without the use of a very large number of LO phases. Furthermore no noise cancellation is used to avoid duplicating the front-end.

The same architecture is used to implement a differential input receiver for FDD applications (like W-CDMA). In this case the main goal is to take advantage of the fully differential signal to simplify the transformer structure and get much better NF (by almost 2dB) although with less harmonic filtering.

The proposed receiver chain is schematically depicted in Figure 2.2 and each block will be separately addressed in the following Sections.

2.2 Low Noise Transconductor

Figure 2.3 presents a simplified SE version of the LNTA. The circuit is built around an input transformer with one primary and two identical secondary coils. The transformer splits the signal feeding it to the two inputs of a class AB p-n

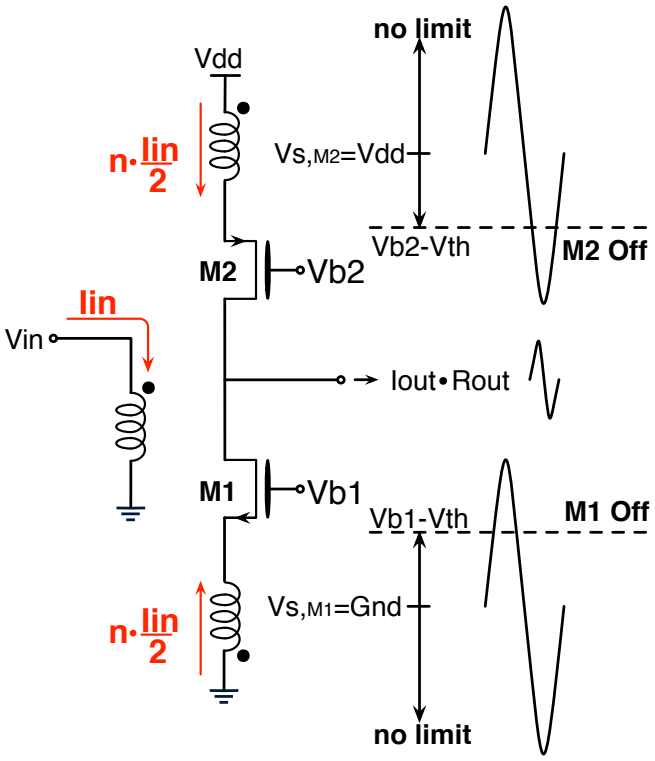


FIGURE 2.3: Single-ended LNTA basic structure.

Common-Gate amplifier. The use of a transformer allows the voltage to swing above the supply and below ground, class AB operation and low noise biasing. Moreover the small turn ratio between secondary and primary (high n for a transformer n:1) reduces voltage swing and gives current gain at the secondary. Reducing the swing at the source of the input transistors improves linearity, while current gain is achieved at no linearity penalty. As shown in Figure 2.3, the current is split almost equally between the two secondary coils that have the same inductance and drive almost the same impedance. While the input ideally cannot compress, the output can if the load impedance is too high. With an equivalent transconductance of 40mS the output compresses at 0dBm if the differential output impedance is grater than 200Ω. However, current-mode operation implies a low impedance load giving a high linearity/compression point.

A common gate topology is used for better linearity but at the cost of a high NF in matching condition [26]. To reduce noise a passive gate boost is used, as shown in Figure 2.4. Applying a replica of the input voltage to the gates of the MOS transistors, the excess noise becomes $1 + n$ times smaller than the noise of

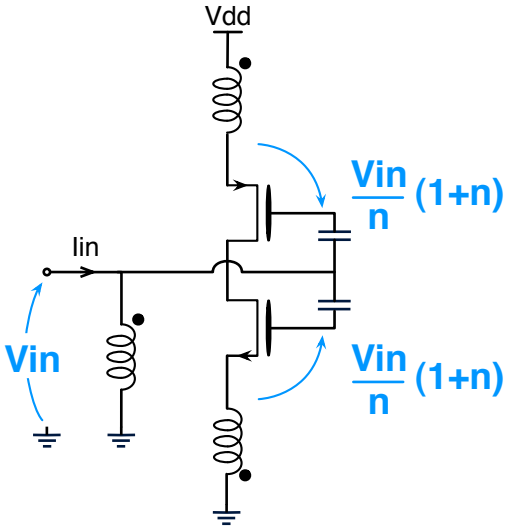


FIGURE 2.4: Single-ended LNTA boosted structure.

the classical common gate amplifier as reported in Equation (2.1).

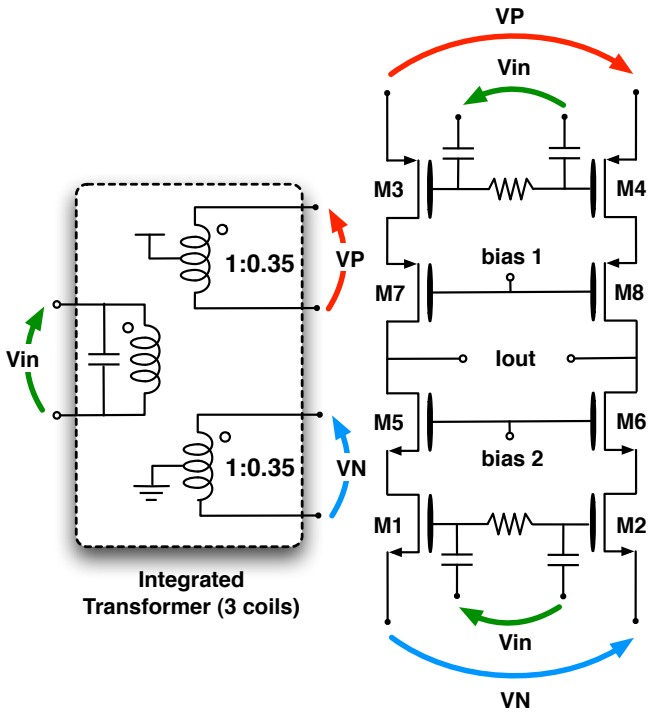
$$NF_{CG} = 1 + \gamma \tag{2.1a}$$

$$NF_{boost} = 1 + \frac{\gamma}{1+n} \tag{2.1b}$$

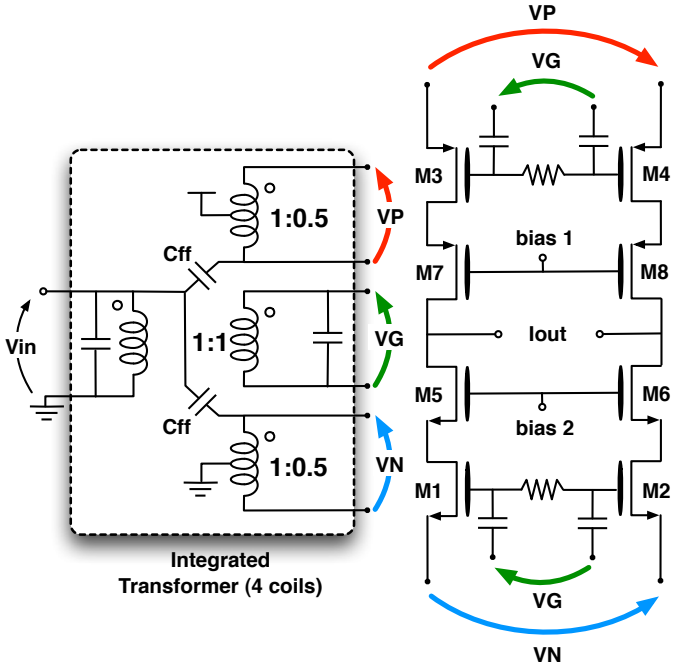
Where NF_{boost} and NF_{CG} are the NF with and without boost, γ is MOS excess noise factor and n is the transformer ratio for a transformer $n:1$. On the other hand, a larger gate-source voltage swing degrades linearity, thus a trade-off between linearity and NF exists. Both implemented circuits (shown in Figure 2.5) use a fully differential signal path to reject common mode noise and a cascode stage to improve output impedance (higher real impedance and lower parasitics) for current-mode operation of the mixer. The FDD LNTA (shown in Figure 2.5(a)) is fully differential, making it compatible with an external differential duplexer. Boosting is done through a couple of capacitors connected to the input pins. The TDD LNTA (shown in Figure 2.5(b)) is SE and can be directly connected to the antenna switch in SAW-less applications. In this case the transformer acts like a bal-un to drive the FD on chip signal path. With a single-ended input it is not possible to use a capacitive boost, so a fourth coil is required [27].

2.2.1 Boosting trade-off

The amount of boosting depends on the transformer ratio n and sets the performance of the LNTA. On the other hand, in matching condition the gm of each



(a)



(b)

FIGURE 2.5: (a) Fully Differential LNTA for FDD applications. (b) Single-ended input LNTA for TDD applications.

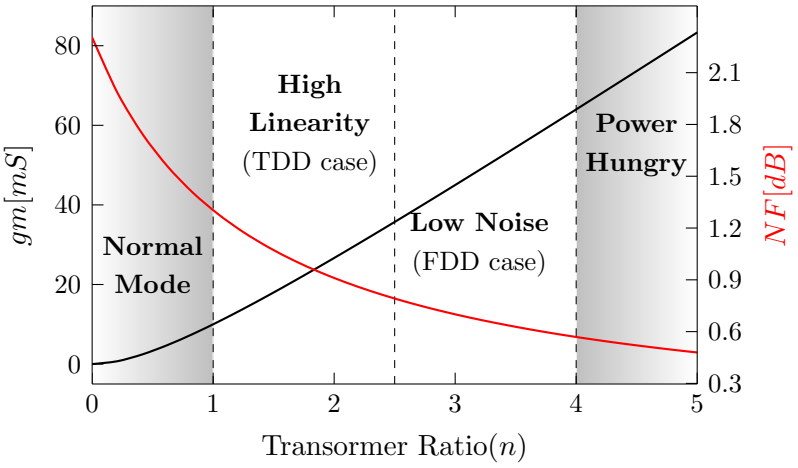


FIGURE 2.6: Input MOS transcoductance and NF versus transformer ratio.

input MOS transistor is constrained to be:

$$gm = \frac{n^2}{Rs(1+n)} \tag{2.2}$$

Where Rs is the source resistance. Figure 2.6 shows the gm required to achieve the matching condition and the corresponding NF versus the transformer ratio. For $n < 1$ the NF is close to that of a classical common-gate, while for $n > 4$ the required gm, and therefore power consumption, is not compatible with the targets of a mobile handset. The range $1 < n < 4$ has been divided into two zones one more suitable for TDD ($n < 2.5$) with higher linearity and one for FDD applications ($n > 2.5$) with lower noise. For the TDD case high linearity/compression has been favored with respect to NF since a SAW-less receiver can have a NF 2-3dB higher but should handle large out-of-band interferers (0dBm). On the other hand for the FDD case, the duplexer introduce losses requiring a lower NF but reducing the linearity requirement.

2.2.2 Transformer design issues

In both the single-ended and the fully-differential LNTA the transformer has a key role, however, being connected to the input pins, its noise is directly added to the noise of the source degrading the NF. To reduce losses, the transformer should have a coupling coefficient as close as possible to one and the highest Q to reduce its intrinsic noise. The achievable performances are strictly correlated to the technology adopted. Nowadays, a low cost RF process (as the one used) has

typically no more than 6 copper layers, of which just one thick, plus a thick aluminum one for bond pads (AP). To maximize the coupling coefficient the primary and the secondary coils should be overlapped [28], however, with only one thick metal layer, this compromises the quality factor of one coil.

In the case of a simple transformer, it is possible to demonstrate that, independently of the current gain n, the two coils contribute equally to the overall noise and thus a stacked design inevitably penalizes one of the two windings. However, in the case of the LNTA proposed (Figure 2.7) it is possible to demonstrate that when the impedances of the windings are much greater than the driving and loading impedances, the noise transfer function associated to the primary coil is:

$$\overline{i_{n,out}^2} = \left|\frac{n}{2Rs}\right|^2 \cdot \overline{V_{n,1}^2} \tag{2.3}$$

while for a single secondary coil is:

$$\overline{i_{n,out}^2} = \left|\frac{n^2}{4Rs(1+n)}\right|^2 \cdot \overline{V_{n,2}^2} \tag{2.4}$$

therefore the noise contribution of the secondary with respect to the primary is:

$$\overline{V_{n,2}^2} = \left|\frac{n}{2(1+n)}\right|^2 \overline{\cdot V_{n,1}^2} \tag{2.5}$$

Where $\overline{i_{n,out}^2}$ is the output current noise, $\overline{V_{n,1,2}^2}$ is the voltage noise associated to the primary or secondary coil, n is the transformer ratio and Rs is the source resistance.
From Equation (2.5) for $n > 1$ (as used in this design) the noise of the secondary is lower than that of the primary for the same Q. Therefore the primary coil should use the thick copper metal while the secondary should use the AP metal due to its minor impact on the overall noise of the transformer.

When an additional coil is needed, as in the case of the LNA topology of Figure 2.5, it is not possible to use a three layers stacking to have both symmetric secondary and maximum quality factor since the bottom metal would give too much series resistance. The two secondary coils are thus realized on the same plane using the AP metal while the boosting coil is implemented with the thick copper layer as the primary coil. In general the transformer use no more than 2 or 3 turns coils to avoid a large number of crosses that would degrade the overall

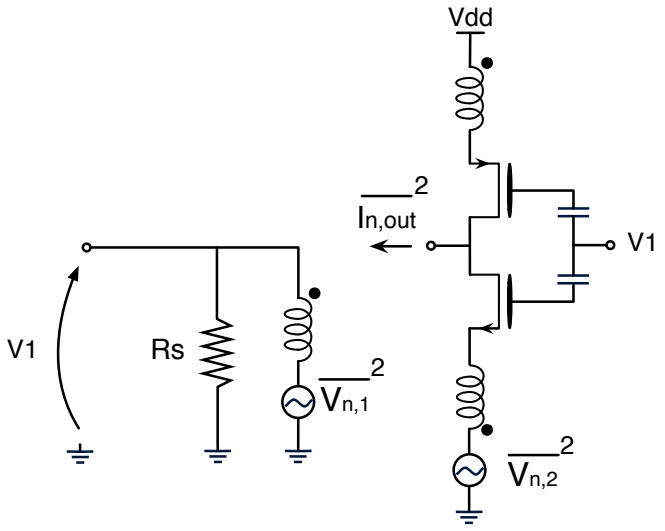


FIGURE 2.7: LNTA simplified scheme for transformer noise analysis.

quality factor.

Considering all the above constraints (NF vs Power Trade-off and technology limits), the transformer nominal ratios for the SAW-less receiver is 2 : 1 (high linearity zone) while for the FDD receiver is 3 : 1 (low noise zone). For the 2 : 1 transformer a primary with two turns is used. This is because the two secondary can be obtained using the exact same shape as the primary changing only the metal layer and the position of the cross. Unfortunately, since in this case the secondary coils need a center tap to provide VDD and ground connections, a symmetrical structure demands two crosses instead of one. To maximize coupling and to minimize the number of crosses the position of the crosses should be the same for both primary and secondary coils. This can be obtained in a simple way rotating the input (primary) by 90 degrees with respect to the outputs (secondary) (Figure 2.8). Notice that, through this layout an exact 2 : 1 ratio is obtained taking advantage of the constructive mutual inductance between the two coils. For the third secondary, a concentric spiral winding is used. Placing one turn of the secondary inside and one outside of the primary winding as shown in Figure 2.8 the desired 1 to 1 ratio is obtained. The light gray lines are the ultra-thick copper used for the primary and the boosting coil while the dark gray lines are the AP used for the two secondary. To maximize the coupling the primary and the two main secondary are perfectly overlapped.

According to [28] a transformer can have a notch in the transfer function due to the coupling capacitor that always exists between primary and secondary coil. This notch occurs at the particular frequency for which the capacitor current and

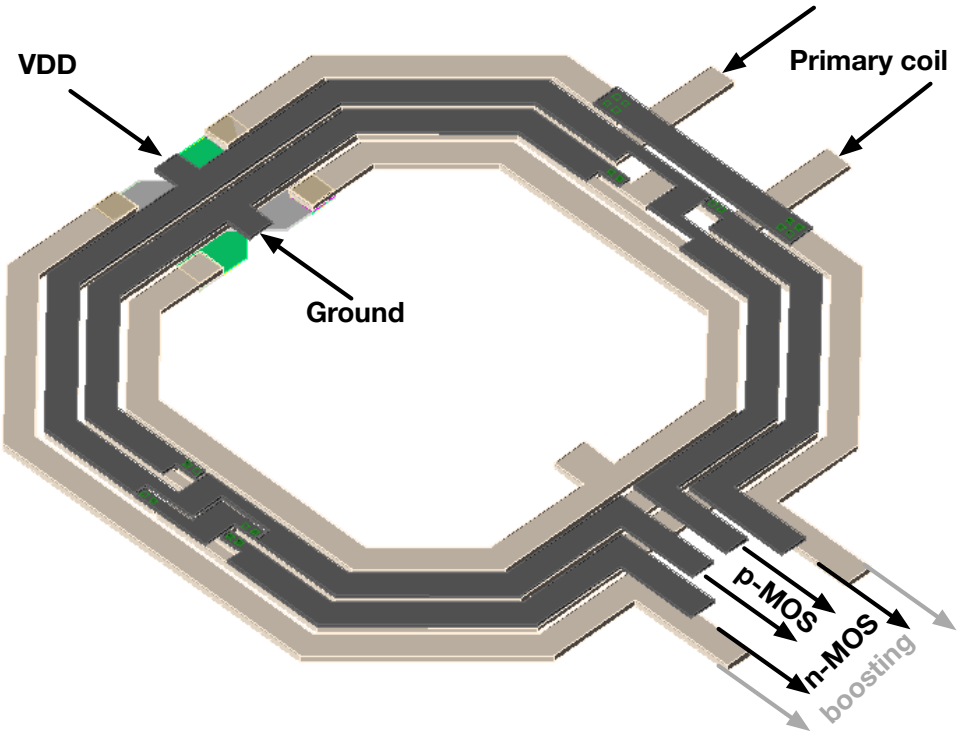


FIGURE 2.8: Layout of three secondaries transformer topology for SE LNTA.

the induced current cancel out being equal in module and opposite in phase. The frequency of the notch can be adjusted adding an explicit capacitance between the primary and the secondary coil as shown in Figure 2.5(b). Tuning the position of the notch such that it corresponds to the frequency of the third harmonic at least 30dB of extra harmonic rejection can be obtained over the entire band of interest.

Using the same criteria outlined above it is possible to realize the two secondary of the 3 : 1 transformer as shown in Figure 2.9. The two couple of dark gray lines (the two secondary) occupy the same space as the three turns light gray lines (the primary) in order again to maximize coupling.

2.3 Resonant Mixer and 25% Duty Cycle clock

The I and Q down-converters are realized by using a current mode passive mixer in series with an LC tank resonating at the 4^{th} harmonic of the local oscillator (LO) (Figure 2.10). The impedance of the LC tank Z_{bb} is reflected at the input of the mixer shifted up and down in frequency by f_{LO} (and scaled in value). This increases the impedance seen looking into the mixer around the 3^{rd} and the 5^{th} harmonic of the LO. Due to such an impedance translation mechanism, the

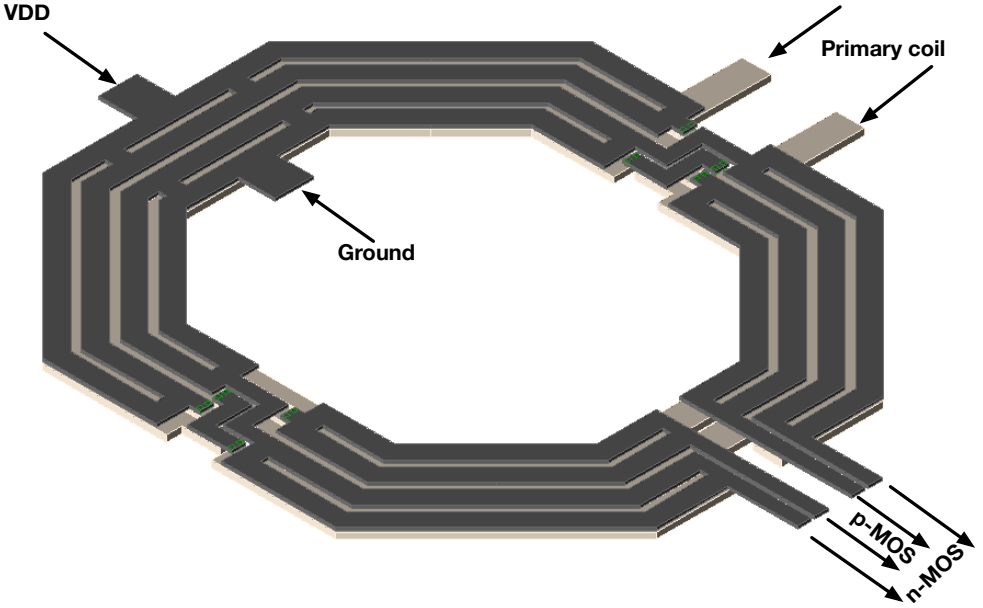


FIGURE 2.9: Layout of two secondaries transformer topology for FD LNTA.

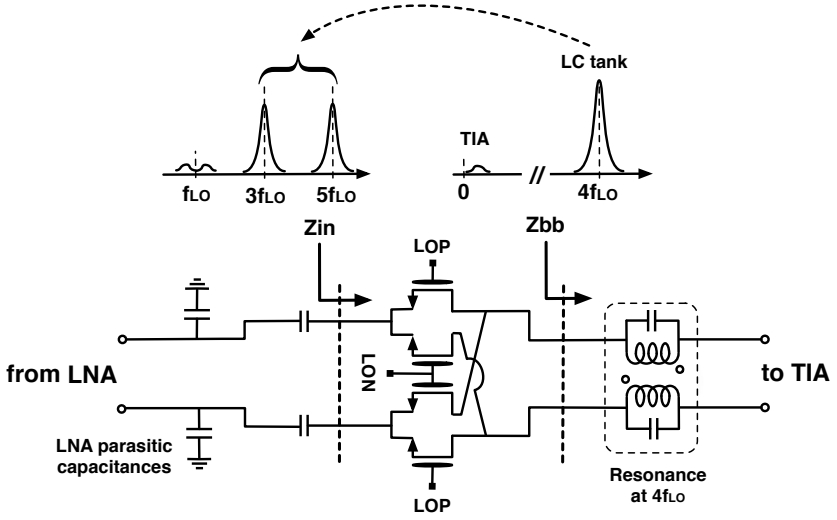


FIGURE 2.10: Resonant Mixer.

current partition between the output impedance of the LNA ($Zout_{LNA}$) and the mixer input impedance reduces the current entering the mixer at the 3^{rd} and the 5^{th} harmonic of the LO without significantly affecting the one at the fundamental frequency. The end result is an improvement in the overall harmonic rejection of the RF front-end.

2.3.1 3^{rd} and 5^{th} harmonic rejection

Assuming a perfectly differential structure (i.e. neglecting even harmonics), the input impedance of the 25% duty-cycle quadrature mixer $Zin(\omega)$ can be approximately found using the theory of Mirzaei et al. [15]:

$$\begin{aligned} Z_{in}(\omega) = R_{SW} + \frac{2}{\pi^2}\left[Z_{LC}(\omega-\omega_{LO}) + Z_{LC}(\omega+\omega_{LO})\right] + \\ + \frac{2}{9\pi^2}\left[Z_{LC}(\omega-3\omega_{LO}) + Z_{LC}(\omega+3\omega_{LO})\right] + \cdots \end{aligned} \tag{2.6}$$

where $Z_{LC}(\omega)$ is the impedance at the mixer output (assumed to be narrow band). Assuming for simplicity that the down-converted signal is sensed by an ideal TIA, Z_{LC} becomes the LC tank resonating at $4\omega_{LO}$. Z_{LC} appears at the input of the mixer scaled by a factor $2/\pi^2$ around the 3^{rd} and the 5^{th} harmonic and by a factor $2/(9\pi^2)$ at ω_{LO} (higher harmonics have been neglected for simplicity). Since the LC tank is reflected also around ω_{LO}, Z_{LC} should satisfy the following condition to minimize current attenuation at ω_{LO}:

$$\left|\frac{\pi^2}{2}Z_{LNA}(3\omega_{LO})\right| \ll |Z_{LC}(4\omega_{LO})| < \left|\frac{9\pi^2}{2}Z_{LNA}(\omega_{LO})\right| \tag{2.7}$$

The right hand side of this inequality assumes $|Z_{LNA}(3\omega_{LO})| > |Z_{LNA}(5\omega LO)|$, as it is usually the case. The trade-off set by Equation (2.7) indicates a limit in the maximum rejection achievable with this technique. Assuming Z_{LNA} is dominated by the capacitance at the output of the LNA (C_{LNA}), equation Equation (2.7) can be rewritten as:

$$\frac{1}{6}\frac{\pi^2}{\omega_{LO}C_{LNA}} \ll |Z_{LC}(4\omega_{LO})| < \frac{9}{2}\frac{\pi^2}{\omega_{LO}C_{LNA}} \tag{2.8}$$

From Equation (2.8) and allowing less than 0.5dB attenuation at the fundamental frequency, the maximum attenuations at the 3^{rd} and the 5^{th} harmonic is 18dB and 23dB respectively giving a potential additional harmonic rejection of 17.5 and 22.5dB respectively.

The harmonic rejection of the resonant mixer is also limited by both the Q and the self-resonance of the integrated inductor in the tank. In this design a rejection just above 10dB was obtained around $3\omega_{LO}$ and 15dB around $5\omega_{LO}$. Considering that the mixer itself intrinsically provides 10dB of rejection at the 3^{rd} harmonic and 15dB at the 5^{th} (for a perfect square wave LO), the total achieved rejection obtained was about 20dB and 30dB respectively. Notice that these harmonics

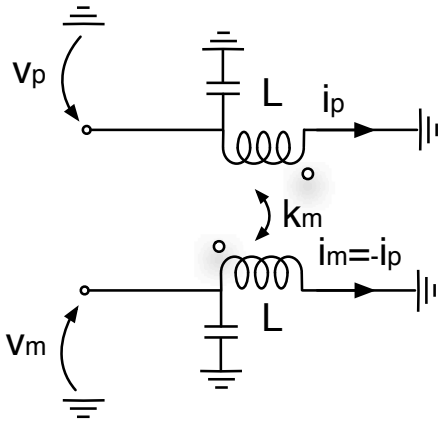


FIGURE 2.11: Transformer based resonant load.

are also filtered by the input transformer (by about 30 dB) before they reach the mixer leading to a total rejection around 50-60dB.
Since the $Zout_{LNA}$ is relatively low at these frequencies due to the the parasitic capacitance (estimated at 250fF), the voltage swing at the 3^{rd} and the 5^{th} is not enough to degrade the linearity performances. Considering for example a 3^{rd} harmonic at 6GHz, $Zout_{LNA}$ is around 100Ω. For a 0dBm blocker with an equivalent transconductance of 40mS and 30dB of filtering provided by the transformer, the voltage swing at the output of the LNA is around 40mV.

2.3.2 Transformer based differential resonant tank

The use of a resonant tank in series with each output of both I and Q mixers requires 4 inductors that, even considering their high resonance frequency, could increase area. Exploiting the differential signal currents provided by the mixer, a transformer based resonant tank was realized which maximizes the quality factor and minimizes the area (Figure 2.11) thanks to the constructive mutual coupling present between the two branches. Referring to Figure 2.11, the inductance of each LC tank is given by:

$$L_{tank} = L(1 + k) \tag{2.9}$$

where L is the inductance of each transform coil and k the coupling between them. With this strategy the area of the coils is significantly reduced and the Q increased since the inductance is effectively doubled. Furthermore such a resonator has a high impedance only for differential signals thereby preventing amplification of the even harmonic that could be present due to mixer mismatches. The tank

was designed to have a 1.5nH of differential inductance and 538fF of capacitance (250fF fixed and 36fF per 8 elements switchable).

2.3.3 25% Duty Cycle Divider

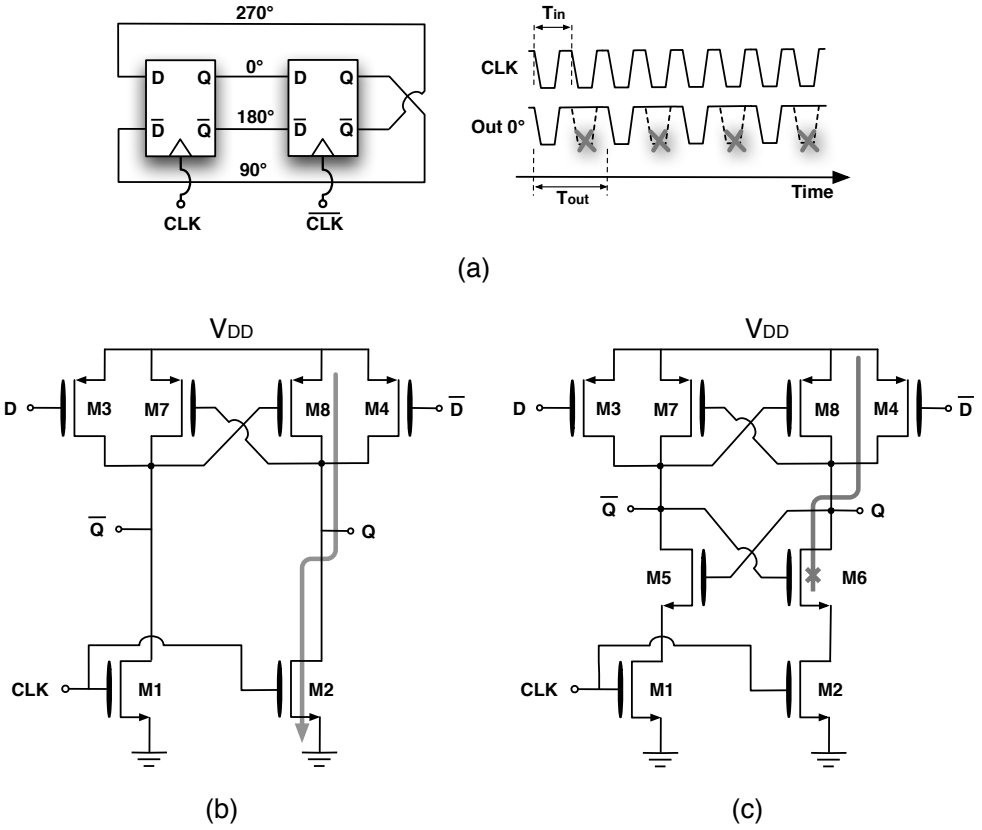


FIGURE 2.12: (a) Divider block diagram and waveform. (b) Old latch structure. (c) Proposed latch structure.

Without any SAW before the LNA, reciprocal mixing can cause a significant NF degradation [29] since any interferer at the mixer input convolving with the phase noise of the local oscillator increases the in-band noise proportionally to the blocker magnitude (see Figure 1.3). Since the receiver must handle blockers up to 0dBm starting from 20MHz offset, the phase noise of the LO should be lower than -172dBc/Hz to minimize the SNR degradation [8]. Because of this, when multiple-phase mixers are used to satisfy the harmonic rejection required from the absence of a SAW, the generation and distribution of the clock could become the most power hungry section of the entire receiver [8].

The use of the LNTA and the resonant mixer just described limits to four the number of phases required to drive I and Q mixers. However, to maximize

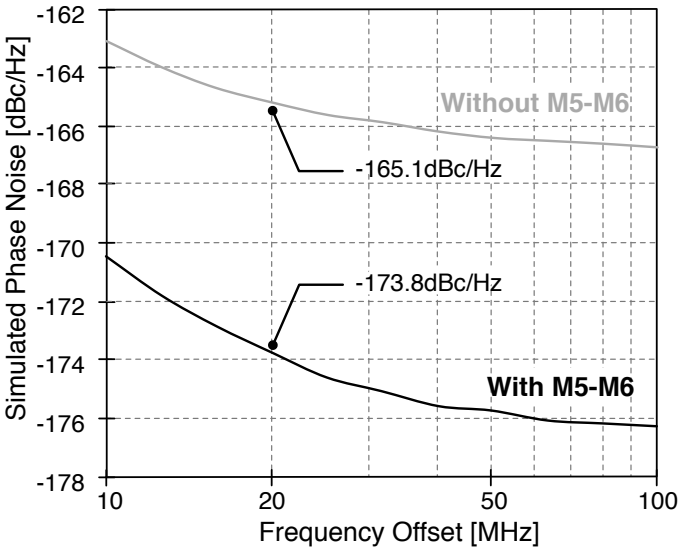


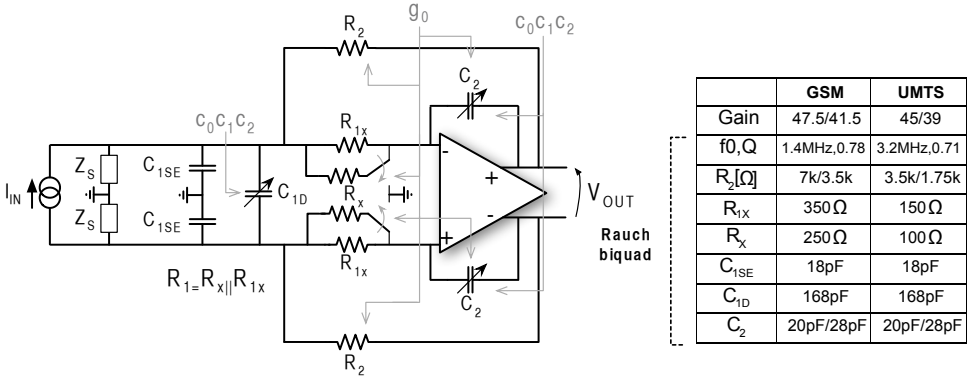
FIGURE 2.13: Simulated PN from extracted layout for old and proposed design.

conversion gain and to reduce I Q interaction a 25% duty-cycle must be used [16]. The four clock phases are generated directly by the divider avoiding the use of a dedicated stage and saving power. The divider is derived from one proposed by Razavi et al. [30] that generates the 25% duty-cycle outputs thanks to a particular latch (Figure 2.12b). When the latch senses the input signal (M1-M2 are OFF) the NMOS pull-down devices are OFF and both output are high (one pulled up by the input and the other maintaining the high state from the previous cycle) [30]. This asymmetry in the latch response gives the 25% duty-cycle output.
In the original design (Figure 2.12b), with M1-M2 ON and either one of the two inputs low a static current flows between the rails during the entire clock phase leading to an excessive power consumption. To solve this problem, the original divider is modified adding M5-M6 in series to M1-M2 to eliminate the direct path between Vdd and ground (Figure 2.12c). Starting from a very clean external clock the divider gives a quadrature clock with -173.8dBc/Hz phase noise at 20MHz burning 6.4mA (simulated from extracted layout) (Figure 2.13).
The presence of M5-M6 introduces an additional degree of freedom in the sizing of M1-M2. In fact in this case, no static current is present and M1-M2 are buffered by the M5-M6 reducing their load to the output. For the same power consumption, a size increment of M1-M2 leaded to a phase-noise reduction of 8.7dB compared to the solution proposed in [30] (Figure 2.13).

2.4 Base Band

The absence of RF selectivity for both the in-band blockers (e.g. from 200kHz to 3MHz offset in GSM, adjacent channels in UMTS) and the out-of-band ones (e.g. 20MHz offset in GSM, TX leakage in UMTS) creates a challenging dynamic range requirement for the BB. Indeed the BB section has to handle these large interferers without increasing the noise floor of the receiver due to both intermodulation terms and extra noise. The frequency profile of the BB input impedance represents another design constraint, since it affects the operation of the current-mode Rx chain. Therefore a BB with low noise, high linearity and low input impedance over a broad band is targeted. Furthermore the BB should accomplish these goals with the smallest possible power budget i.e. consuming less than 30% of the RF section.

Few representative examples are given below. For GSM, a -23dBm (antenna referred) blocker 3MHz away has to be handled with less than 5dB NF. This corresponds to -116dBm input referred noise for the entire chain or -126dBm for the BB (assuming 10% BB noise contribution) i.e. more than 100dB BB dynamic range at 3MHz. Also in the presence of two -40dBm tones at 0.8-1.6MHz an IM3 more than 85dB below the interferer power is required to give an intermodulation term comparable to the level of the BB noise.



	GSM	UMTS
Gain	47.5/41.5	45/39
f0,Q	1.4MHz,0.78	3.2MHz,0.71
R_2[Ω]	7k/3.5k	3.5k/1.75k
R_{1X}	350Ω	150Ω
R_X	250Ω	100Ω
C_{1SE}	18pF	18pF
C_{1D}	168pF	168pF
C_2	20pF/28pF	20pF/28pF

FIGURE 2.14: Rauch biquad based BB.

The detailed BB schematic (I or Q section) is shown in Figure 2.14. A current driven Rauch filter is used to directly interface the RF and BB sections, thus avoiding the need of cascaded I-V and V-I stages and compared with [8] has a second order filter as opposed to a first order. The input signal I_{IN} is the mixer down-converted current (Figure 2.10) while the output is the voltage V_{OUT}. Therefore a trans-impedance stage is obtained with Z_S representing the BB driving

impedance, i.e. the equivalent mixer output impedance [16]. One control bit switches from TDD to FDD mode, acting on the resistors.

The base-band design goals are met exploiting the following features of the current driven Rauch filter. First, the passive current filter (first order) implemented by C_1 that limits the amount of interferer current that reaches the OTA, high pass shapes the major noise contributors, and keeps the high frequency BB input impedance low. Second the low in-band input impedance, provided by the feedback loop built around the high DC gain OTA. Third the possibility of implementing gain reconfigurability as explained in [4] to extend the handling capability of high power blockers (more robustness to fading and input signals PAR). Notice that, although [4] describes a Filtering ADC and not an analog filter, its architecture originated from a Rauch biquad. Furthermore, the approach proposed in [4] to handle both GSM and UMTS scenarios has been followed in the present design.

In the following sub-paragraphs the key elements of the BB are explained in detail, focusing on how they affect the entire chain.

2.4.1 STF, input impedance and Gain selection

As expected the signal transfer function $H(s) = V_{OUT}/I_{IN}$ of the Rauch filter Figure 2.14 is a biquad:

$$H(s) = \frac{G}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{2.10}$$

in which:

$$G = R_2, \quad \omega_0 = \sqrt{\frac{1}{R_1 C_1 R_2 C_2}}, \quad Q = \frac{1}{\omega_0 C_0 \left(R_1 + R_2 + \frac{R_1 R_2}{Z_s}\right)}$$

The feedback resistance R_2 sets the in band transimpedance gain, while the time constants R_1C_1 and R_2C_2 set the selectivity. Gain, cut-off frequency and Q will experience PVT variations, since no automatic calibration has been implemented. However, the possibility to tune the capacitances by 30% has been implemented (using bits $c_0c_1c_2$ in Figure 2.14) which could be used to compensate PVT effects, and/or to allow cut-off reconfigurability. Notice that since Z_S (whose value is not easily predictable [4]) affects only the Q, the transfer function displays good robustness with respect to parasitic effects. Assuming a purely resistive driving

impedance, a Butterworth STF has been chosen to maximize in-band flatness. The simulated STF (for nominal capacitance and high gain mode) for TDD and FDD is depicted in Figure 2.15.a.

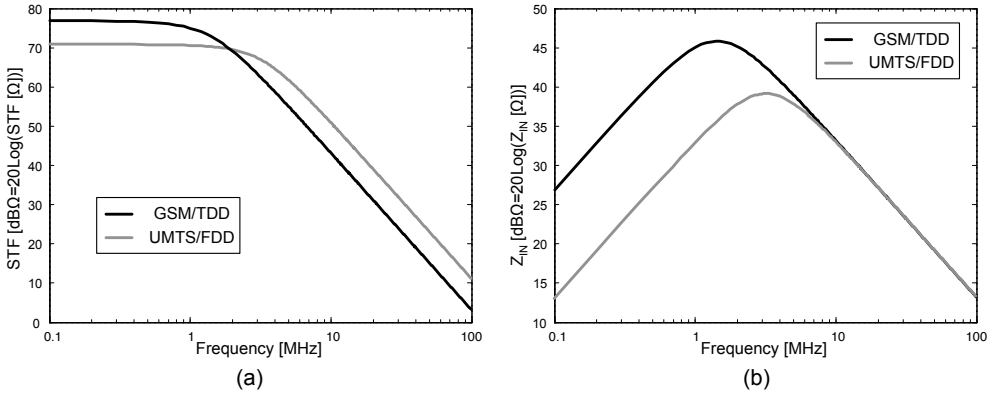


FIGURE 2.15: Base Band (a) Signal-Transfer-Function. (b) Input Impedance

As already mentioned, a low BB input impedance is required to insure current operation. This is because a high BB impedance deteriorates the down-converter linearity, (which limits the receiver linearity) and in an I-Q architecture increases the asymmetry of the signal transfer function between positive and negative frequencies (complex STF) [15]. The Rauch filter input impedance is equivalent to an RLC resonant network where the inductance is synthesized by the gyrator made up of R_2 and the integrator $1/(sC_2R_1)$. In-band the inductance creates a virtual-ground while beyond the cut-off frequency the impedance is set by C_1. At cut-off the inductance and the capacitance resonate, and the impedance reaches its maximum equal to R_1. The simulated input impedance profile for both TDD and FDD is reported in Figure 2.15.b.

The gain control does not affect the BB cut-off frequency and the BB input impedance level [4]. First, the gain is modified reducing R_2 (Figure 2.14). Then, R_x is switched from virtual ground (high-gain) to ground (low-gain), introducing a current partition in the filter forward gain. This reduces the integrator bandwidth limiting the increase of C_2 and keeping the resistance seen at the BB input. Finally, C_2 variation compensates the previous changes to maintain the BB selectivity

2.4.2 Noise and linearity analysis

The dominant noise contributors are the input resistance R_1 and the operational amplifier. They both benefit from the high pass noise shaping mechanism

of current filters explained in [31]. Notice that the noise analysis given in [4] can be applied with very little modifications to the Rauch filter, substituting the continuous time feedback DAC with R_2. The noise of R_2 is not high pass shaped but follows the STF profile, however it can be neglected with a small error. There is a trade-off between in-band noise and selectivity [31], and between in-band noise and input impedance [32]. Widening the filter bandwidth increases the amount of noise filtering but reduces the interferer attenuation. Furthermore, noise can be reduced lowering C_1, and increasing R_1, at the price of a higher input impedance. BB linearity can be improved increasing the OTA open-loop gain at the signal frequency. In fact the higher is the OTA gain, the smaller is the swing at the virtual ground node which reduces the amount of non-linear terms, for a given output swing. This has been accomplished with a feed-forward compensated OTA [32].

2.4.3 Operational Amplifier

The operational amplifier is the core of the BB. It determines its power consumption, decides its non-linearity and contributes in a non-negligible way to its noise.

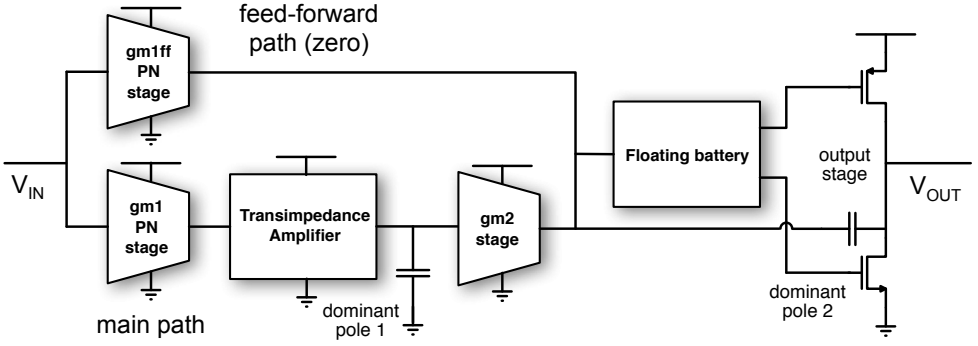


FIGURE 2.16: BB Op-Amp diagram block scheme.

Considering non-linearity, the key goal is to increase the OTA bandwidth. Using a traditional single pole architecture, a very high open loop unity gain frequency f_T would be required to get sufficient gain at the frequency of the blockers (e.g. at 2MHz). On the other hand the use of feed-forward compensation can overcome this limitation [33]. A fast low-gain feed-forward path (Figure 2.16) ensures the stability of the structure by determining the OTA f_T and ensuring -20dB/decade

slope when crossing the 0dB axes. At the same time a lower bandwidth higher order main path, creates a -40dB/decade gain slope below f_T increasing the gain at the frequency of interest.
Considering noise, the input differential pair represents the main OTA noise source. To save power, a complementary p-n MOS architecture with current reuse has been chosen for the first stage. Its main benefit is that it gives the same equivalent gm with half of the current of a simple p-MOS or n-MOS only differential pair. Since the current folding branches of the p-n input stage consumes 25% of the total input stage current, 40% power saving is obtained (15% of the total OTA budget).

The OTA needs to drive a very large capacitive load due to the following reasons. First, the need to satisfy the demanding $1/f$ noise target of a direct conversion GSM receiver (100Hz lower noise integration edge) mandates big input transistors. Combining this with the relatively large feedback capacitance C_2 makes the large C_{GS} of the input transistor to load the output at high frequency. Second, capacitance C_2 (reconfigurable) has about 5% parasitic to ground at both the top and the bottom plate. Finally some margin should be allowed to cover PAD and off-chip parasitic together with the differential probe input capacitance. It follows that a high OTA power consumption would be required to ensure system stability, since the non-dominant pole is directly linked to the output capacitance. For a given OTA target bandwidth and a given capacitive load, to reduce the power consumption of the output stage, the Ahuja compensation technique can been exploited [34]. This gives, about 60% of current saving to push the non-dominant pole at twice the OTA f_T (60 degrees phase margin), compared with a traditional Miller compensation. In addition, the right hand side zero typical of a Miller amplifier is naturally avoided.

The operational amplifier detailed architecture is shown in Fig. 16. The main path is composed by the input complementary p-n stage (gm_1), a transimpedence amplifier based on the topology proposed by P. W. Li et al. [35] but driven in current from the source of the transistors, a second transconductance stage (gm_2), which feeds the output push pull stage (through a floating battery) [36]-[37]. The feed-forward path is made by a simple transconductance stage (gm_{1ff}), which sums its current with the one of the main path in front of the class-AB common source output stage. This latter section embeds the Ahuja compensation loop.
The Rauch loop is designed to have more than 90MHz bandwidth in all working conditions (GSM/UMTS, high/low gain) with >65 degrees phase margin and

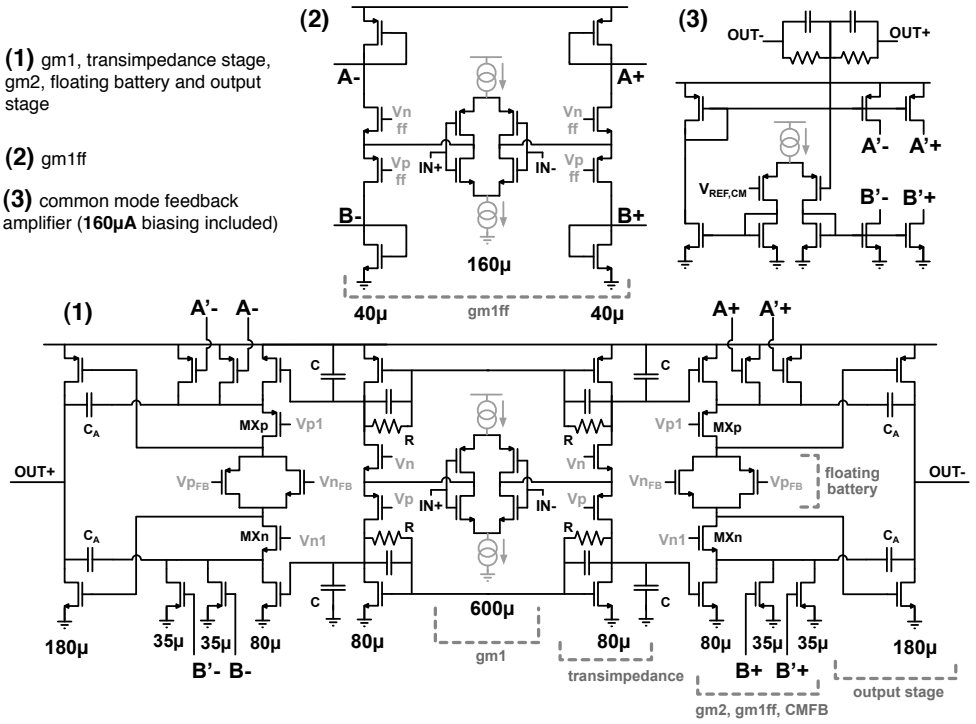


FIGURE 2.17: BB Op-Amp MOS transistors simplified scheme.

>14dB gain margin. The -40/-20dB per decade dual slope approach gives the possibility to achieve 40dB open loop gain at 2MHz (i.e. the edge of the UMTS band) and 75dB at 200kHz (i.e. the edge of the GSM low-IF band). Notice that considering only the operational amplifier gain, these values are significantly higher (62dB and 90dB respectively). The OTA equivalent input referred noise resistance is 50Ω with another 50Ω required to represent the flicker noise contribution (GSM).

2.5 Prototype and Measurements

A chip prototype that includes two receivers was fabricated in 40nm CMOS technology (Figure 2.18). The two RF paths (SE and Differential) share a common BB (I and Q) and a supply voltage of $1.8V$. The mixers are also used as switches to select the receiver path. The SE path implements the GSM standard, while the differential path implements the UMTS standard. As shown in Figure 2.18 the GSM input transformer is bigger than the UMTS one due to the boosting coil. Thanks to its high resonance frequency the resonator at the mixer output requires a small area (less than 5% of the entire receiver). The 25% Duty Cycle divider, under a 1.2V supply voltage, is also shared by two RX chains and is placed in

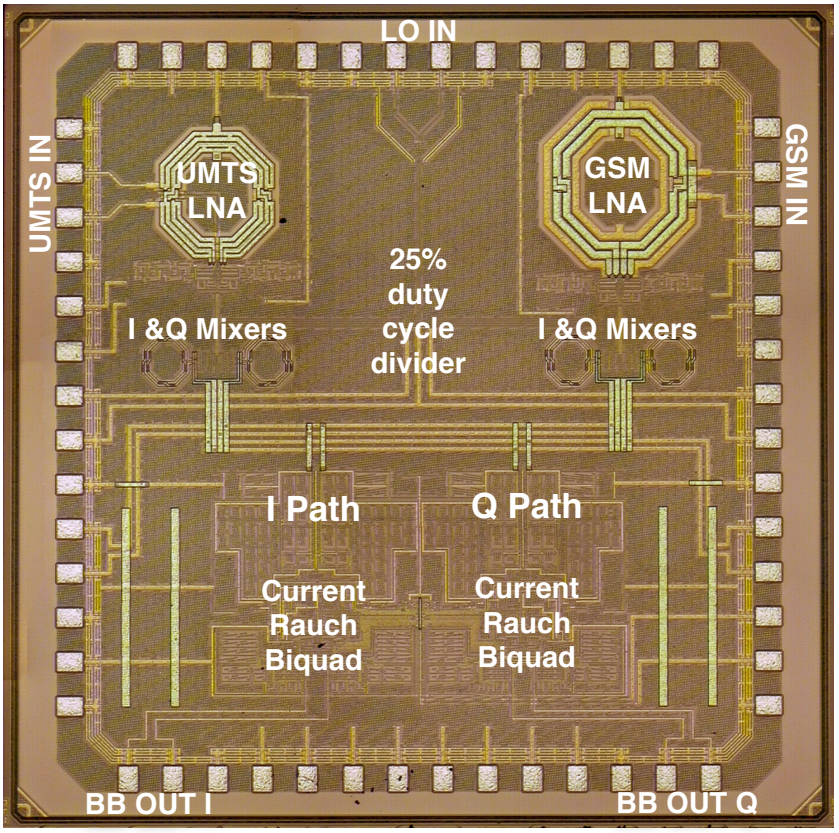


FIGURE 2.18: Chip die photo.

the center of the die to optimize the LO distribution. The BB input capacitance is made of a differential part C_{1D} and a single ended part C_{1SE} (Figure 2.14). This capacitor is not tuned when changing the gain or the bandwidth simplifying the layout and increasing the capacitor density. 95% of the equivalent BB input capacitance is contributed by C_{1D} (equal to 350pF) while the remaining 5% by C_{1SE}. In this way the actual area is only 30% of that required by an entire single-ended solution. Using a M1-M5 MOM implementation the area required by the input capacitance for the I (Q) path is about $500x300\mu m^2$ (50% of the I (Q) BB). The C_2 feedback capacitance value is modified from 20pF to 28pF passing from high-gain to low-gain mode. The resistance R_1 has nominal values of 250Ω and 100Ω (GSM and UMTS, high-gain), while the resistance R_2 has nominal values of 7kΩ and 3.5kΩ (GSM and UMTS, high-gain).

Figure 2.19 shows both measured and simulated gain and NF of the SAW-less receiver versus frequency. The minimum NF is 3.8dB and is located at 2.2GHz instead of the design value of 1.8GHz (GSM standard) due to an error in the transformer design. From 2.1GHz to 2.3GHz the NF stays below 4.5dB. Simulation shows that the mismatch between the resonance frequency of the primary and the

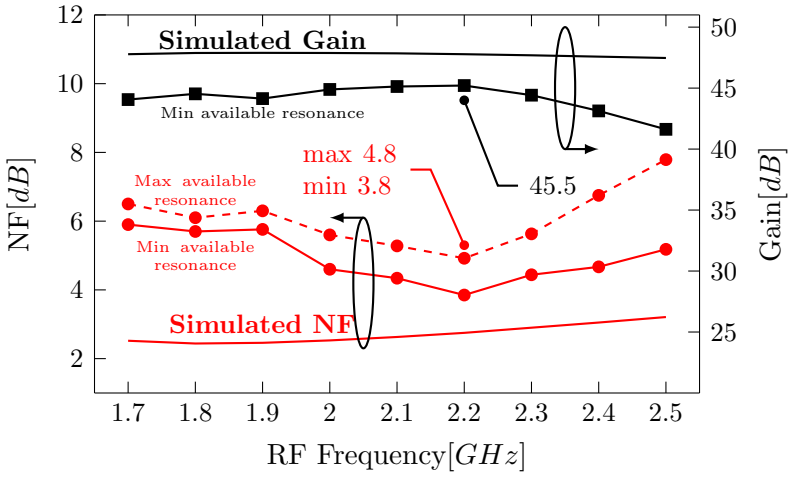


FIGURE 2.19: Gain and NF from measurements and simulations of TDD receiver path.

boosting coil (due to inaccurate EM simulations) causes an extra 1dB of NF and about 1.4dB gain reduction.

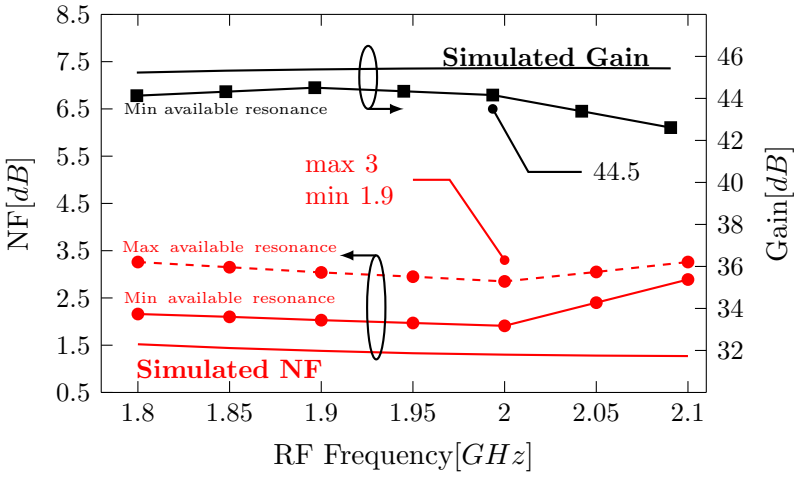


FIGURE 2.20: Gain and NF from measurements and simulations of FDD receiver path.

This conclusion is confirmed by the fact that for the FD receiver, where resonance mismatch cannot exist thanks to the using of capacitive boosting, the measured 1.9dB NF and 44.5dB gain (with the resonant mixer tuned at the minimum possible frequency), are much closer to simulations as shown in Figure 2.20. The minimum NF is 1.9dB and is located at 2GHz, from below 1.8GHz to 2.05GHz the NF stays below 2.5dB. All the NF measurements were performed at 100kHz IF.

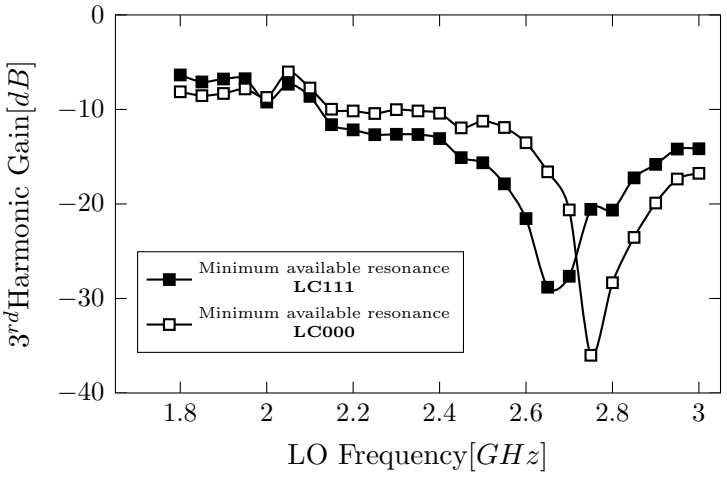


FIGURE 2.21: TDD 3^{rd} Harmonic Gain and resonant mixer tuning.

Figure 2.21 shows the 3^{rd} harmonic gain vs. LO frequency while tuning the resonance frequency of the mixer load at the maximum and at the minimum possible values. Since the mixer load resonance frequency, even at its minimum, is too high due to the inaccurate EM simulations the full potential of the technique cannot be exploited. However, at the wanted frequencies a sizeable improvement in the harmonic rejection is still visible.

Furthermore the same technique reduces LNA noise folding by the mixer improving NF as shown in Figure 2.19. The 1dB improvement is due to the fact that the spectrum of the LNA noise at the mixer output is not white but increases moving away from the RF band. In a similar way the resonant mixer improves the NF for the FDD receiver as shown in Figure 2.20.

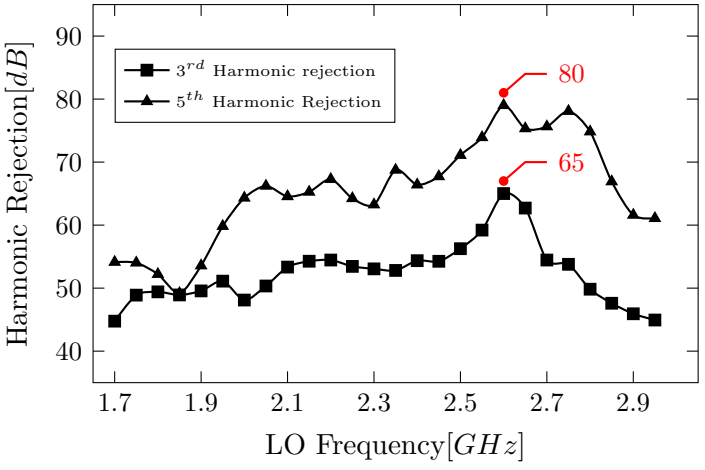


FIGURE 2.22: TDD 3^{rd} and 5^{th} harmonic rejection.

Figure 2.22 shows 3^{rd} and 5^{th} harmonic rejection versus f_{LO}. 54dB and 65dB are measured at 2.2GHz for TDD. The maximum achievable rejection is 65dB and 80dB respectively around 2.7GHz i.e. at the mixer load resonant frequency.

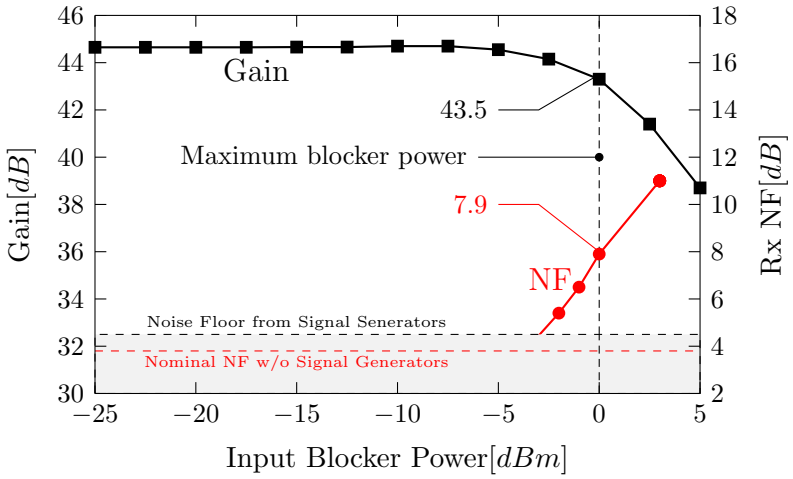
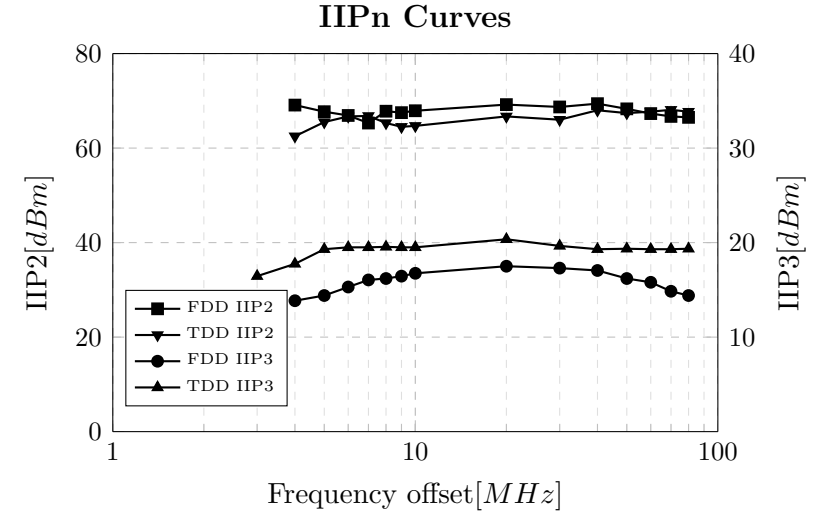


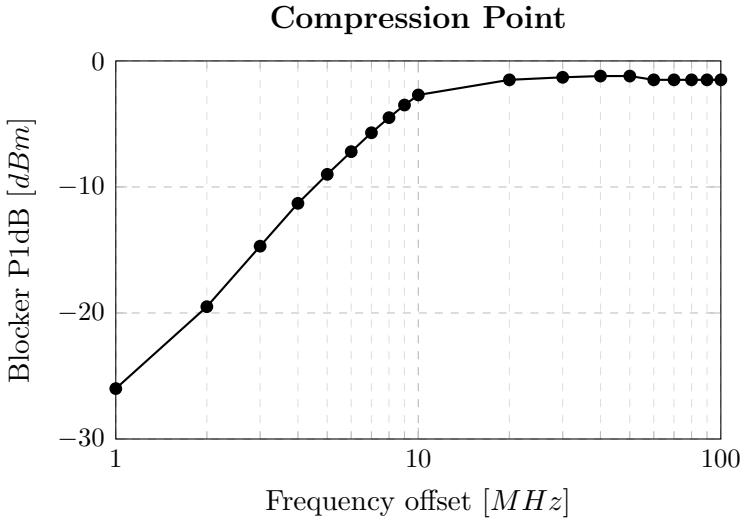
FIGURE 2.23: TDD Gain and NF versus input blocker power.

Figure 2.23 shows NF and gain of the SE receiver as a function of the power level of an input blocker located at 20MHz offset. Below -2dBm the noise floor of the signal generator used to supply the blocker dominates NF. At 0dBm, which is the maximum blocker power defined by the standard, the NF reaches 7.9dB. Notice, however, that also this value is affected by the measurement set-up. In this case the dominant factor is the phase noise of the LO generator at 20MHz offset which folds in band part of the blocker energy through reciprocal mixing. Gain compression at 0dBm is only 1.4dB demonstrating the excellent dynamic range of the entire front thanks to the class A/B LNA (no current slewing) the current mode mixer and the high selectivity Rauch filter (no voltage clipping).

Figure 2.24a shows the un-calibrated out-of-band IIP2 versus the position of the interferers for a typical sample. IIP2 is always above 64dBm for both receivers and for all three measured samples from 3 MHz on. Figure 2.24a also shows the IIP3 versus the position of the interferes. IIP3 is >18dBm and >16dBm for the TDD and FDD receiver respectively for an offset frequency above 3 MHz. Figure 2.24b shows the one dB compression point as a function of the blocker position for the TDD case. P1dB is approaching -1.5dBm above 20MHz. All linearity measurements are taken setting the gain at its maximum and the resonance of the mixer load at the minimum available frequency as it is done for the minimum NF measurements. In both cases the LNA consume 9mA, the BB 4mA and the LO generation/distribution block 6.5mA at 2GHz.



(a)



(b)

FIGURE 2.24: Measured receiver linearity at $f_{LO} = 2GHz$, (a) Measured IIP2 using two-tones test ($f_1 = f_{LO} + \Delta f$, $f_2 = f_{LO} + \Delta f + 500kHz$) and measured IIP3 using two-tones test ($f_1 = f_{LO} + \Delta f$, $f_2 = f_{LO} + 2\Delta f - 500kHz$), (b) Measured blocker P_{1dB} with blocker located at $f = f_{LO} + \Delta f$.

In Table 2.1 is reported the comparison with the other recently published SAW-less/blocker tolerant/noise cancelling receivers. Both multiple frequency and SDR architectures have been taken in account. Despite the NF of the presented works is comparable with the state-of-the-art, the IIP3 is much higher making them more robust to the interferers. The TDD architecture achieves the highest harmonic rejection which is fundamental for SAW-less applications.

Thanks to the class AB current-mode approach high linearity performances are achieved with the lowest power consumption (only $32mW$). Moreover using 4

TABLE 2.1: Comparison with recently published SAW-less, blocker tolerant receivers

	[23] JSSC2011	**[24] ISSCC2011**	**[19] JSSC2011**	**[38] ISSCC2012**	**This Work (TDD)**	**This Work (FDD)**
RF Frequency [MHz]	850-950 1800-1900	850-950 1800-1900	400-6000	80-2700	1800-2400	1800-2100
RF Input	SE	Diff	Diff	SE	SE	Diff
Min in-band NF [dB]	3.1	2.9[1]	3.2[1]	1.9	3.8	1.9[1]
0 dBm Blocker NF [dB]	11.4[2]	7[2]	15[3]	4.1[2]	7.9[3]	-
$3^{rd}/5^{th}$ harmonic rejection [dB]	>40/N.A	44/N.A	–	42/45	54/65	–
IIP3 [dBm]	>-12.4 (IB)	0 (IB)	10 (OB)	13.5 (OB)	>18 (OB)	>16 (OB)
IIP2 [dBm]	>45 (IB)	>44.3 (IB)	70 (OB)	54 (OB)	>64[4](OB)	>66[4](OB)
Active area $[mm^2]$	2.4[5]	1.4	2	1.2	0.84	0.74
Supply Voltage [V]	1.3/1.7	2.8	1.1/2.5	1.3	1.2/1.8	1.2/1.8
Power Cons. [mW]	55 $[mA]$ [5]	58.9 $[mA]$ [6]	38.9[7]	65[7]	32[7]	32[7]
LO divider Current [mA]	N.A.	N.A.	N.A.	26(2GHz)	6.4(2GHz)	6.4(2GHz)
CMOS Technology	65nm	65nm	40nm	40nm	40nm	40nm

[1] An off-chip balun can result in an additional 1.2dB of NF degradation [2] 80MHz Blocker Offset
[3] 20MHz Blocker Offset [4] Measured from 3 samples [5] Including VCO and synthesizer
[6] Including ADC [7] Estimated at 2GHz given reported numbers

phase for the LO instead of 8 used by [25] and thanks to the 25% divider without additional logic, only $3.6mA/GHz$ are needed for LO generation-distribution.

Chapter 3

3G Integrated Duplexer front-end

In this Chapter a briefly introduction to the 3G integrated-duplexer solutions for mobile handset is presented (Section 3.1). Section 3.2 reports the concept of the hybrid transformer used for duplexing purpose. In Section 3.3 the proposed architecture is introduced and each building block is analysed. The prototype and simulations results are presented in Section 3.4 where a comparison with the state-of-the-art solutions is reported. Finally an overview on the system level solutions is introduced Section 3.5.

3.1 Integrated Duplexer architectures: State-of-the-art

While for 2G SAW-less receiver several architectures have been implemented, for 3G the first step has been taken only few years ago by Mikhemar et al. [39] adopting the well-known electrical-balance concept using the Hybrid Transformer (HT). This idea was commonly used in telephone handset to isolate the microphone from the earpiece and in telephone plant to cancel the echo-crosstalk and it has been well study for these purposes [40, 41].
The first integrated implementation [39] was a demonstrator with a HT composed by an autotransformer to prove the feasibility of such a device. The direct connection of the input LNA to the antenna was the major limitation for a real application due to the high voltage swing of the Tx signal, which was not supported.
The second step toward this architecture was presented in [42]. An input HT with

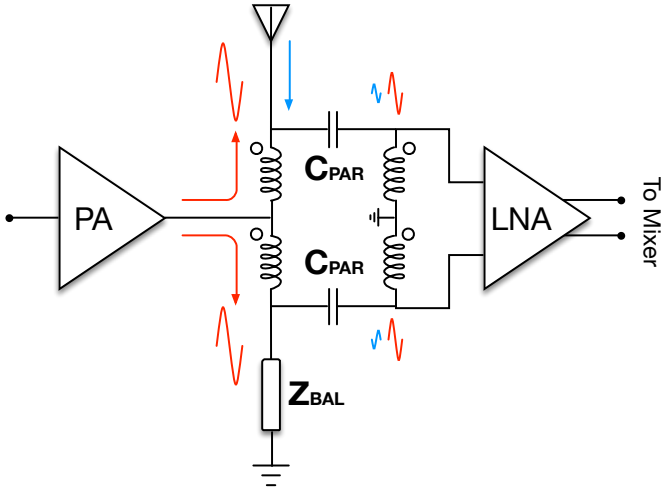


FIGURE 3.1: Two coils Hybrid transformer-based Integrated Duplexer.

two independent coils was described (but not really implemented) thus providing the necessary isolation for both small and high voltage swing between Tx and Rx. The isolation is provided discriminating between common-mode and differential voltage but, due to high coupling between the transformer coils, a large common mode Tx signal leaks to the Rx side as shown in Figure 3.1. This mechanism limits *de facto* the usability due to poor linearity performances of the LNA used (CS pseudo-differential architecture).
The last published step has been taken by Abdelhalem et al. [43, 44], doubling the input HT in such a way to cancel out the CM Tx signal at the Rx side (see Figure 3.2). The differential Power Amplifier (PA) creates two high voltage swing signals with opposite phases. When the leakage reaches the LNA side it cancel-out itself thanks to the phase shift. However the double HT not only requires more area and a differential PA but also requires an external BALUN. This sets a big limit of such an approach since in the current solutions the PA in not in the same substrate of the receiver and its output is single ended. However this implementation can be exploit if the receiver and PA are co-designed.

Since the matching is no more required, in [42–44] a noise matched common-source LNA has been adopted in order to reduce the overall NF. However, the pseudo-differential structure used requires a very low CM signal leakage.

This thesis will show how exploiting the current-mode approach with a fully differential LNTA as illustrated in Chapter 2, a single HT as in Figure 3.1 can be

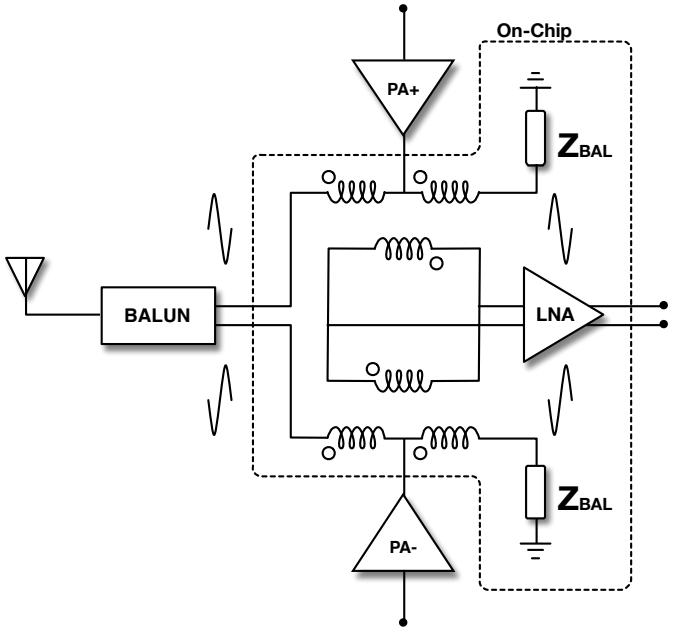


FIGURE 3.2: Fully Differential Integrated Duplexer.

used to achieve the required performances and potentially be used in high handset mobile phone. Despite a real device is under fabrication at time of this thesis submission, simulations results will be presented to validate the idea.

3.2 Hybrid Transformer

The Hybrid Transformer has been used for many years in the telephone plant for its particular features: impedance matching at a number of ports, conjugacy between groups of ports and the ability to split power in any desired proportion between two receiving ports without losses (considering an ideal HT). Thanks to these properties is possible to combine or split signals without any interaction [40]. Considering the ideal HT configuration of Figure 3.3 the impedance matching and bi-conjugacy condition are defined by:

$$R_D = r \cdot R_B \tag{3.1}$$

$$R_A = \frac{r}{1+r} R_B \tag{3.2}$$

$$R_C = \frac{1}{1+r} \left(\frac{N_2}{N_1} \right)^2 R_B \tag{3.3}$$

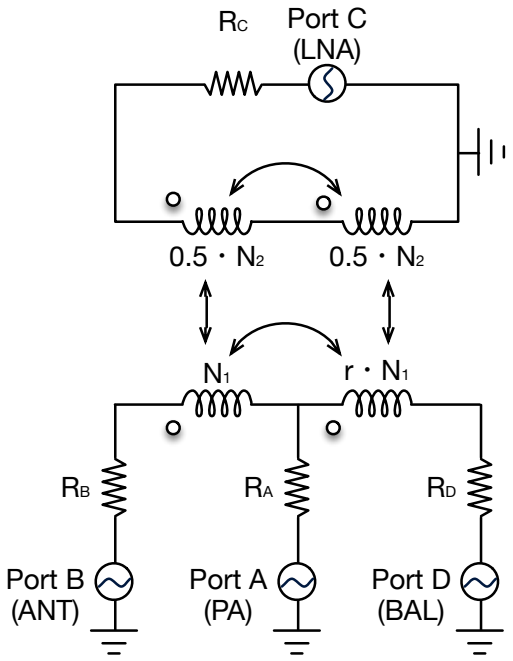


FIGURE 3.3: Ideal single core Hybrid Transformer.

In this scenario the *Port A* splits the signal on *Port B* and *Port D* creating a common-mode signal. It follows that, for an ideal transformer, *Port C* is isolated from *Port A* since only differential signal can be sensed by the secondary coil. In the same way *Port C* and *D* are isolated if *Port A* and *C* are well terminated. In this configuration the *Port A* can be used to inject the Tx signal while the *Port C* is suitable for LNA connection. The antenna can be placed either at *Port B* or *Port D* while the last available port needs to create the bridge balancing, matching the antenna impedance.
In matching condition is possible also to achieve a power splitting with no losses (for an ideal HT) instead of the typical 3dB of the power splitters.
Exciting the *Port A* and assuming an ideal transformer in bi-conjugacy condition the power is split on *port B* and *D* with a ratio expressed by:

$$\frac{P_B}{P_A} = \frac{r}{1+r} \tag{3.4}$$

$$\frac{P_D}{P_A} = \frac{1}{1+r} \tag{3.5}$$

Where P_A, P_B and P_D represent the power at *Port A*, *Port B* and *Port D* respectively. However since the antenna is connected only at one port (e.g. *Port B*), the power dissipated in the balancing impedance (BAL) of *Port D* is wasted and can

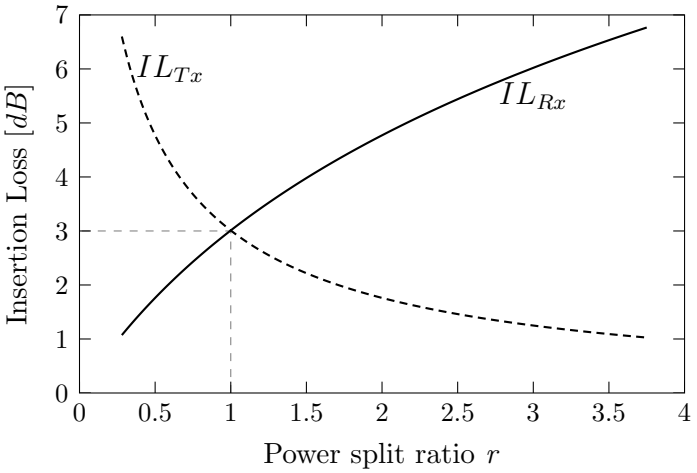


FIGURE 3.4: Insertion-loss trade-off of an ideal hybrid transformer.

be represented as an equivalent Insertion Loss (IL). It follows that for the Tx port the IL is given by:

$$IL_{Tx} = 10 \cdot \log\left(\frac{1+r}{r}\right) \tag{3.6}$$

while for Rx path is:

$$IL_{Rx} = 10 \cdot \log(1+r) \tag{3.7}$$

The Equations (3.6) and (3.7) show a trade-off that is plotted in Figure 3.4. Reducing the IL_{Tx} increases the PA efficiency but degrades the NF since the IL_{Rx} is directly added to the overall noise. When the power is equally split the Insertion Loss is 3 dB for both Tx and Rx.

3.3 Receiver Chain

The receiver chain adopted is a current-mode architecture as the one proposed in Chapter 2 for its excellent linearity performances. At the input a simple hybrid transformer (based on the one shown in Figure 3.1) combines the Tx and Antenna signals. The Tx signal is split equally on the antenna and the balancing network (r=1). It follows that, for an ideal HT, the NF will be increased by 3 dB due to the insertion loss as reported by Equation (3.7).
The antenna signal is sensed by the primary coil and fed to a noise-matched cross-coupled common-gate LNT that drives the cascade of a 25% duty-cycle mixer and a Rauch bi-quad TIA as depicted in Figure 3.5. As it will be shown, this solution

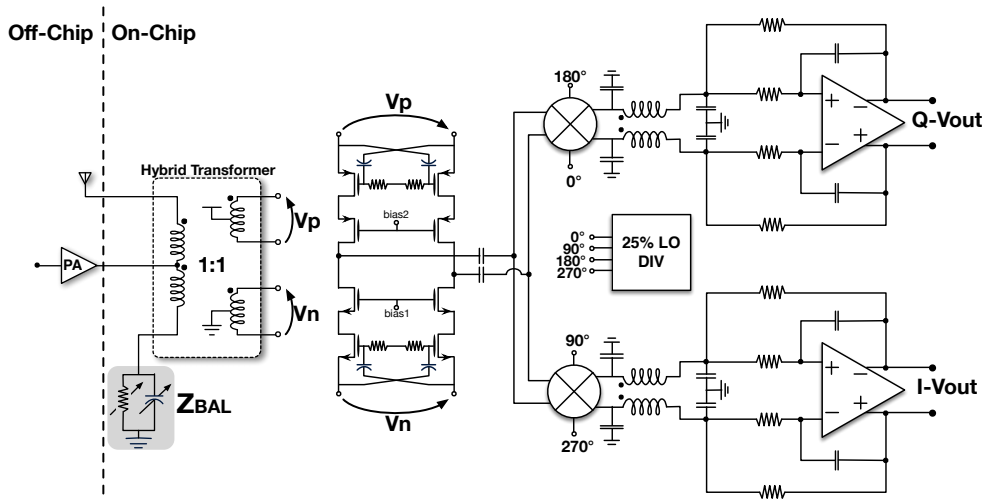


FIGURE 3.5: Current-mode duplexer-less receiver chain.

guarantees the linearity performances required by 3G standard even though a limited integrated duplexer isolation is achieved.

3.3.1 Noise matched Low Noise Transconductor Amplifier

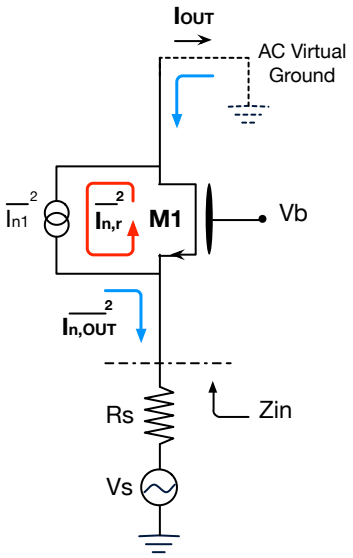


FIGURE 3.6: Equivalent MOS current-noise recirculation.

High linearity, high Common-Mode-Rejection (CMR) and low noise performances are required for 3G SAW-less implementation. A cross-coupled common-gate is used to meet the requirements. The common-gate topology is the most

linear configuration but the drawback is a poor NF due to the imposed matching condition [26]. When this condition is removed (only the SAW/Duplexer needs the impedance matching for a correct filtering) the linearity-NF trade-off is broken. The NF of a simple unmatched CG LNA, assuming a current-mode approach as shown in Figure 3.6, is given by:

$$NF_{CG,unmatch} = 10 \cdot \log\left(1 + \frac{\gamma}{gm \cdot Rs}\right) \tag{3.8}$$

Where γ is the MOS excess noise factor, Rs is the source resistance and gm is the MOS transconductance.
Thanks to the current-mode architecture (ideally no voltage swing at the output), the linearity is proportional to the gate-source voltage V_{GS} applied to the MOS transistor induced by the source voltage Vs that, for small signal analysis, is given by:

$$V_{GS} = -Vs \cdot \frac{1}{1 + gm \cdot Rs} \tag{3.9}$$

Both Equations (3.8) and (3.9) show the benefits of an increased MOS transconductance on both NF and voltage across the MOS transistor. Another intuitive view is the *"pipe"* concept [31]. Since the driving impedance is greater then the input impedance Z_{IN} (that is equal to $1/gm$ for an ideal MOS with a low output impedance load), the MOS transistor noise is obligated to recirculate in a proportion defined by the ratio between driving and input impedance as defined by the following Equation:

$$\overline{i_{n,OUT}}^2 = \left|\frac{1}{1 + gm \cdot Rs}\right|^2 \cdot \overline{i_{n1}}^2 \tag{3.10}$$

In the same way, since the non-linearities sources can be represented as current generators injecting the resulting products in parallel to the noise current-source $\overline{i_{n1}}^2$, the non-linearities should recirculate with the same proportion.
It follows that NF and IIP3 benefit from an increased gm at the cost of an increased power consumption. Indeed, assuming a MOS transistor operating in sub-threshold, the power dissipation is proportional to the gm of the MOS transistor itself. A strong trade-off is still present, since the final target is a mobile handset with limited power capability.

The proposed LNT structure is shown in Figure 3.7. While the input signal from the PA creates a common-mode voltage on both antenna and balancing network, the input signal from the antenna is split almost equally to the secondary coils of the transformer to fed a *p-n* class AB cross-coupled common-gate stage. As

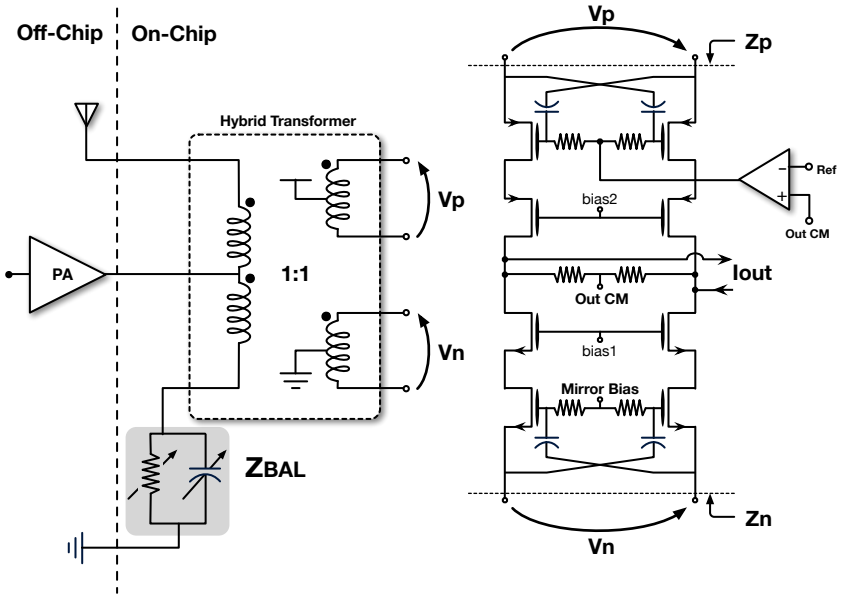


FIGURE 3.7: Proposed Low Noise Transconductor structure.

for the LNTA previously presented (Section 2.2), thanks to the input transformer, voltage swing above supply and below ground, class AB operation and low noise biasing are allowed.

In Chapter 2 has been shown that the transformer ratio defines the trade-off between NF and power consumption, which was dictated by the matching condition. Since is no more required, a transformer ratio can be choose to reduce the equivalent input impedance and benefits of a NF improvement with no power consumption penalties. The equivalent differential input impedance at the primary is given by:

$$Z_{IN} = \frac{Zn /\!\!/ Zp}{n^2} = \frac{\frac{1}{gm_n} /\!\!/ \frac{1}{gm_p}}{n^2} \tag{3.11}$$

Where n is the transformer ratio (for a transformer $1 : n$), the gm_n and the gm_p are the transconductance of the n and p MOS transistors respectively. Equation (3.11) shows that to reduce the input impedance, the turn ratio, for a transformer $1 : n$, should be maximized. However increasing the transformer ratio reduces the linearities performance since the MOS transistors are solicited with a larger voltage. Moreover a higher transformer ratio implies more parasitics capacitance between the primary and secondary coils leading to an increased Tx leakage.

Due to capacitive coupling between the transformer coils, a large CM signal leaks on the Rx side. Two mechanisms are exploit to reject this unwanted signal. The first is a high CM impedance (ideally infinite) provided by the cross coupled

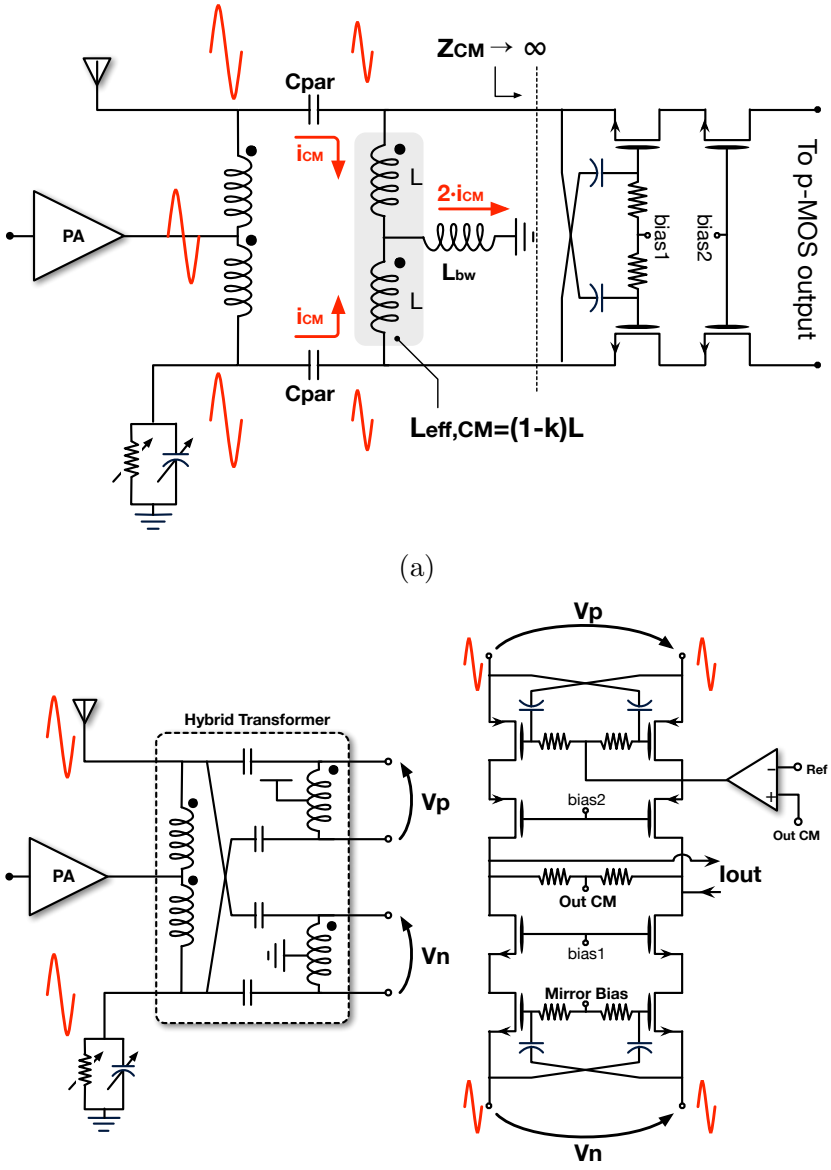


FIGURE 3.8: Common mode signal leaking rejection: (a) Infinite CM input impedance and (b) floating structure.

structure that force the current to flow into the ground. The common-mode current creates a flux opposite in the two half of the secondary winding lowering the equivalent impedance seen by the CM signal as shown in Figure 3.8(a), which is given by:

$$L_{eff,CM} = (1 - k) \cdot Lind \tag{3.12}$$

Where $Lind$ is the secondary coil inductor value, k is the autotransformer coupling and $L_{eff,CM}$ is the equivalent inductor for CM signal. Since the current flows also

into a bond-wire that connects the ground to the rest of the circuit, the CM voltage at the secondary is:

$$V_{cm} = j\omega \left(L_{eff,CM} + L_{bw}\right) \cdot 2I_{CM} \tag{3.13}$$

Where $L_{eff,CM}$ is the equivalent inductor for CM signal as given by Equation (3.12) and L_{bw} is the inductor representation of the bonding wire . Therefore, due to a finite CM impedance of the transformer ($k < 1$) and the large bonding wire inductor to connect the ground, a voltage swing to reject is still present.
The second mechanism takes advantage from the AC floating structure provided by the two secondary coils of the hybrid transformer. The common-mode signal leaks on both p and n MOS transistors as shown in Figure 3.8(b). If the LNTA is biased with high impedance and each MOS transistor has a floating well [10], the entire LNTA experiences the same swing with no current modulation or lifetime performances reduction. It follows that this structure can tolerate a higher voltage swing compared to the pseudo-differential used in [42–45] allowing the use of a single hybrid transformer.
Despite this approach can tolerate a higher CM signal, lowering the capacitive coupling between the transformer coils remains a main goal.

3.3.2 Integrated Hybrid Transformer implementation

The input transformer, as previously explained, sets the LNTA performances. Its noise is directly added to the overall noise degrading the NF. Since no impedance matching is required, the turn ratio impacts on the NF-consumption-linearity trade-off changing the equivalent input impedance. In addition, for the hybrid transformer implementation, common-mode signal coupling must be limited to prevent the leaking of the large Tx signal on the Rx side.
In the solutions proposed in [39, 42–44], the large transformer ratio required to lower the overall NF increases the common-mode leakage that, due to the pseudo-differential CS LNT used, it is not rejected, since no CMR is achieved. It follows that both signals, differential and common-mode, should be attenuated by the same amount before hitting the non-linear devices in order to relax the linearity requirements thus requiring a double HT [44]. On the other hand a fully-differential solution can tolerate a higher common-mode signal allowing the use of a single HT, however the topology adopted heavily impact on the performances required.

For the transformer implementation, stacked or coplanar configurations can be exploit. The first benefits of an higher coupling k but limits the achievable Q of primary or secondary coils due to technology implementation, as previously explained in Section 2.2.2. The second reduces the common-mode signal coupling and potentially maximizes the Q of both primary and secondary coils but degrades the overall NF due to a poor k [28].

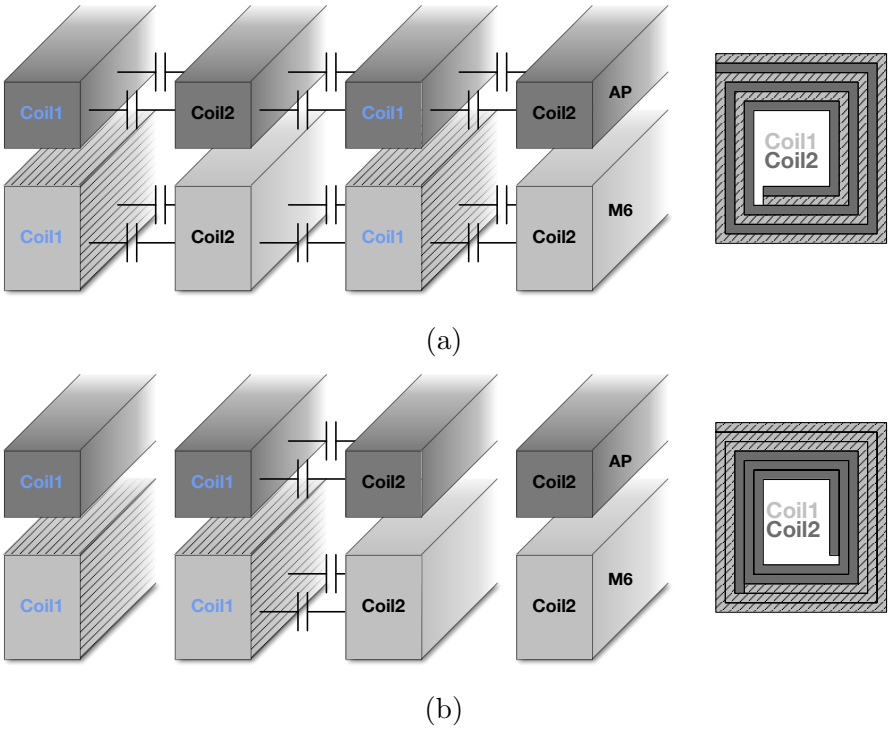


FIGURE 3.9: Section of a coplanar transformer with: (a) alternated coils (b) concentric coils.

From Equation (3.11) a ratio $n \geq 1$ is required to reduce the input impedance and hence to improve the NF. Using a low cost RF process with only one thick copper metal as the one used for the transformer described in Chapter 2, a coplanar implementation is more suitable in order to limit the capacitive coupling and maximize the Q.

The coplanar transformer can be implemented at least in three different way [28]: parallel conductor (Shibata) winding, inter-wound (Frlan) winding and concentric spiral winding. The first two solutions, utilizing alternated coils, maximize both differential (k) and common-mode (C_{PAR}) signals coupling while concentric spiral reduces the coupling minimizing the surface between primary and secondary as depicted in Figure 3.9. Since the Tx common-mode signal leakage is a major problem, the last solution has been implemented.

In order to maximize the Q of both primary and secondary coils, shorted AP and thick copper metal could be used (cross section shown in Figure 3.9). However, to reduce the equivalent coupling surface only one of them should be implemented using this technique. Considering the simplified circuit of Figure 3.10 and an ideal transformer, the output current-noise associated to the primary coil is given by:

$$\overline{i_{n,out}^2} = \left| \frac{4\, gm \cdot n}{1 + 4\, gm \cdot n^2 Rs} \right|^2 \cdot \overline{v_{n,1}^2} \tag{3.14}$$

While for the secondary coil is:

$$\overline{i_{n,out}^2} = \left| \frac{2\, gm}{1 + 4\, gm \cdot n^2 Rs} \right|^2 \cdot \overline{v_{n,2}^2} \tag{3.15}$$

Finally the noise of the secondary with respect to the primary is:

$$\overline{v_{n,2}} = \left| \frac{1}{2n} \right|^2 \cdot \overline{v_{n,1}^2} \tag{3.16}$$

Where $\overline{i_{n,out}^2}$ is the output current-noise, $\overline{v_{n,1}^2}$ and $\overline{v_{n,2}^2}$ represent the voltage noise of the primary and secondary coils respectively, n is the transformer ratio (for a $1:n$ topology) and Rs is the source resistance. From Equation (3.16) the noise of one secondary is lower than the noise of the primary for $n > 0.5$ but when considering a finite coupling coefficient k Equation (3.16) becomes:

$$\overline{v_{n,2}} = \left| \frac{1}{2\, k\, n} \right|^2 \cdot \overline{v_{n,1}^2} \tag{3.17}$$

For concentric spiral, coupling coefficients k as high as 0.6 have been reported [28]. It follows that from Equation (3.17), for a turn ratio $n \simeq 1$, the primary and one secondary could have almost the same impact on the overall noise.

Considering all the previous technology limitation and trade-off, a coplanar transformer with a turn ratio $n = 1$ and the secondary coils with AP and copper thick metal shorted has been implemented.
Figure 3.11 shows the layout of the implemented hybrid transformer. The two center turns constitute the primary winding while the two couple of outer and inner turns constitute the two secondary windings.

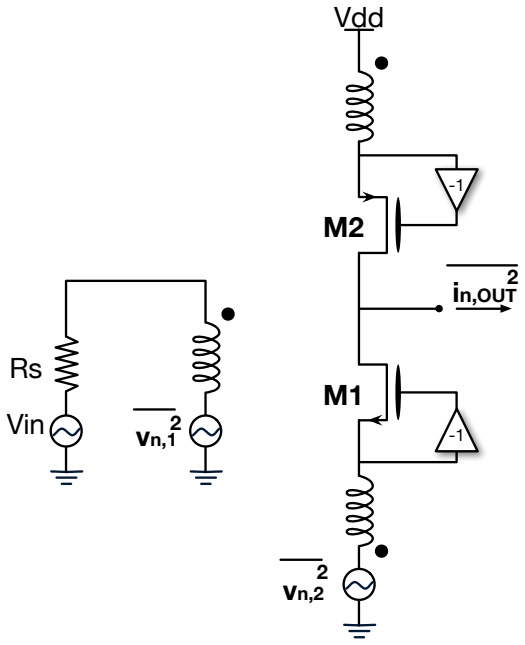


FIGURE 3.10: Cross-coupled CG LNTA simplified schematic.

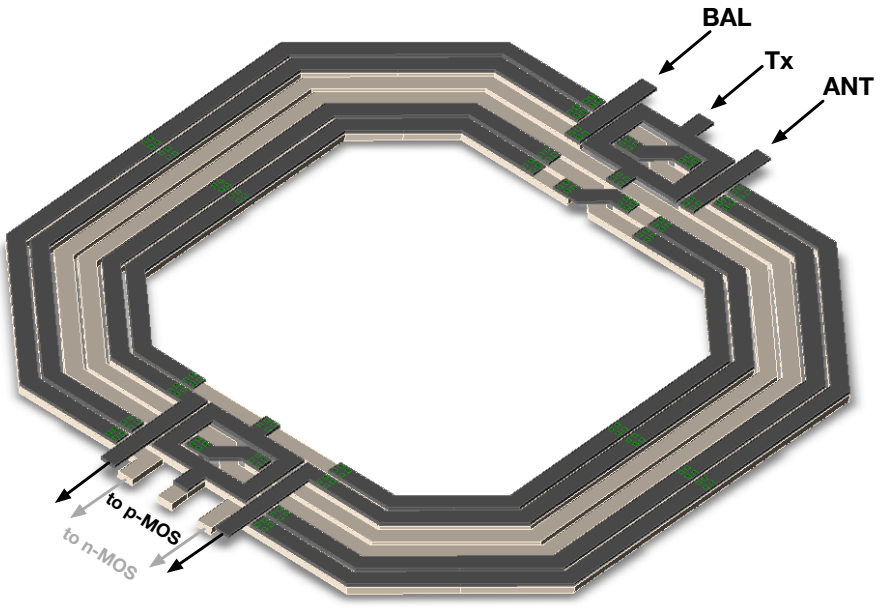


FIGURE 3.11: Layout of the proposed Hybrid Transformer.

3.3.3 Electrical Balance: High voltage network

The isolation between the Rx and the TX relies on a null differential voltage across the primary winding thanks to a balanced bridge composed by the antenna

(ANT) and Z_{BAL} impedance (BAL). Due to the unpredictable antenna impedance variations, unbalancing can occur. Therefore, the balancing network must be able to track the antenna impedance over the Tx and Rx bands. In the Tx band to suppress the huge Tx signal while in the Rx band to suppress the Tx noise.
A simple solution is represented by a parallel variable resistor and capacitor connected to ground. For the implementation, analog controlled impedance [43] or switch arrays [39] can be used. The first solution can ideally provide perfect balance but it also makes the optimum control voltages power level dependent [43]. The second has lower resolution due to the quantization steps but potentially a higher linearity.

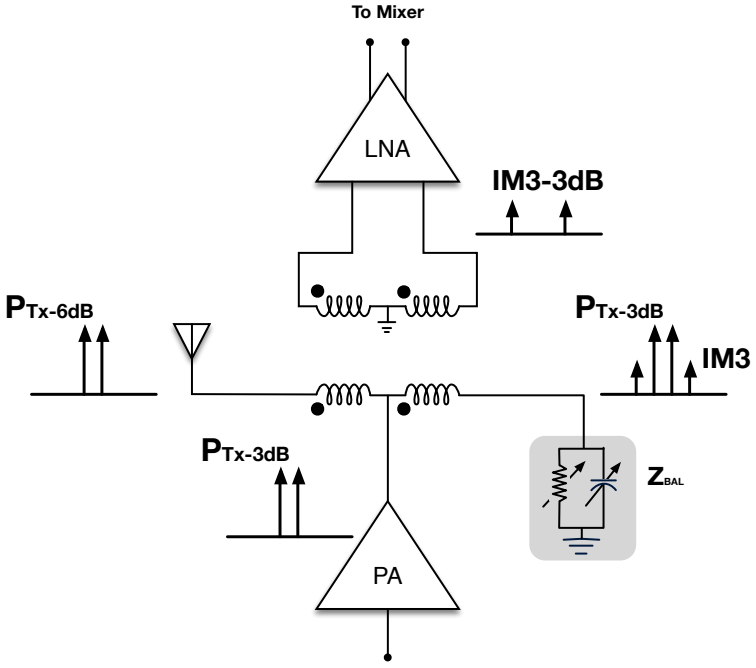


FIGURE 3.12: Balancing network non-linearities effect.

As illustrated in Figure 3.12 the balancing network non-linearities can produce unwanted IM3 tones that would leak back into the LNA input degrading the effective isolation [43]. Moreover, the balancing network is directly connected to the primary and no isolation is provided by the hybrid-transformer, hence the linearity requirements are the same as the antenna reported in Section 1.3.1.
Since switched-impedance can provide higher linearity, two banks of switched resistor and capacitor have been adopted to implement the variable balancing impedance. To handle the large voltage swing (up to 15V peak-to-peak) a stack of two thick-oxide switches with an AC-floating body can be used to guarantee a 10 years lifetime [45]. However in order to limit the non-linear behaviour due

to the switch resistance modulation, a stack of eight elements, as shown in Figure 3.13, has been implemented. Considering the resistor stack for example, each

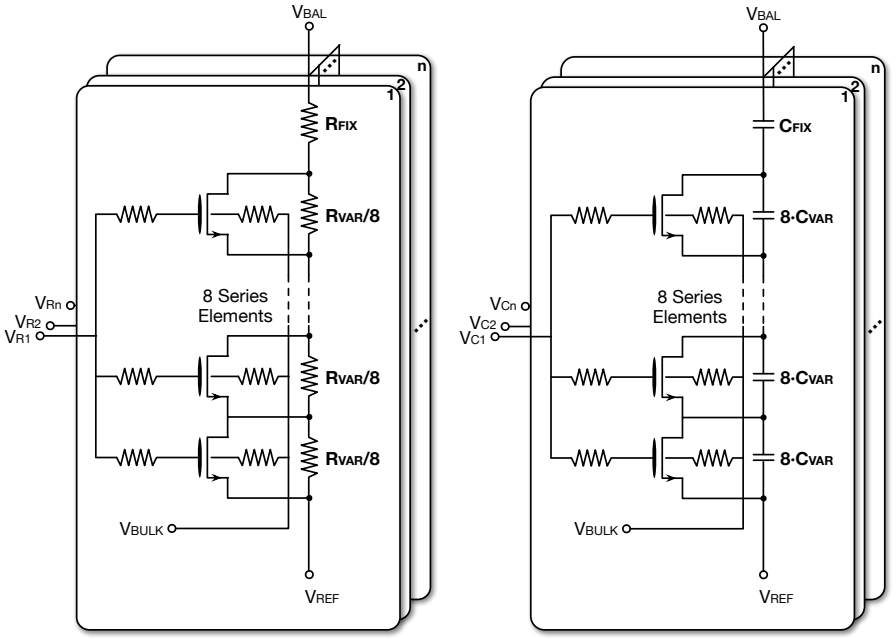


FIGURE 3.13: High voltage and High linear balancing network: (a) resistor stack (b) capacitor stack.

MOS transistor can short a resistor that is equal to $R_{VAR}/8$. The equivalent impedance of each stack seen between V_{BAL} and V_{REF} can be changed from R_{FIX} to $R_{FIX}+R_{VAR}$. The total impedance is the parallel of all the stacks. Considering n stacks of which x are shorted and y are not, the total real impedance is given by:

$$R_{tot} = \frac{xR_{FIX} \cdot yR_{VAR}}{xR_{FIX} + yR_{VAR}} \tag{3.18}$$

The same considerations and results can be applied to the capacitor bank giving the following equation:

$$C_{TOT} = x \cdot C_{FIX} + y \cdot C_{eq} \tag{3.19}$$

Where C_{eq} is the series of the fixed and variable capacitance and is defined by:

$$C_{eq} = \frac{C_{FIX} \cdot C_{VAR}}{C_{FIX} + C_{VAR}} \tag{3.20}$$

Since the voltage swing across each switch is divided by the number of series elements the linearity of each device improves and the overall IIP3 of the stack is given by:

$$IIP3_{STACK} = IIP3_{SW} + 20 \cdot \log N \tag{3.21}$$

Where $IIP3_{SW}$ is the IIP3 of a single switch and N is the number of series elements. Theoretically only MOS transistors could be used to sustain the entire voltage, however using a low-impedance (resistor or capacitor) in parallel with the switch helps distributing the voltage equally across all switches improving the linearity.
Due to the very demanding IIP3 requirements a fixed series resistance or capacitor is used to reduce the voltage swing across the switches stack and consequently reducing the non-linear products. However this approach limits the tuning range setting a strong trade-off.

To understand the limits and the amount of attenuation required before the stack extensively simulations have been carried out. A stack of 8 thick oxide MOS transistors in 28nm with 1.8V power supply capability has been used. The attenuation provided before the switches stack is proportional to the ratio of the fixed and variable impedance and is defined by:

$$ATT = 20 \cdot \log\left(1 - \frac{R_{FIX}}{R_{FIX} + R_{VAR}}\right) \tag{3.22}$$

Where R_{FIX} and R_{VAR} represent the fixed and switched impedances respectively. The simulated IIP3 as a function of the attenuation is reported in Table 3.1.
In the worst case an IIP3 up to 67.5dBm at the antenna must be achieved to meet

Table 3.1: IIP3 of the 8 stacked switches as a function of the attenuation provided

ATT [dB]	**IIP3 [dBm]**
-6	74
-3.5	69.2
-2.5	67
0	62.8

the 3G standard requirements. The total of the non-linearities is composed by the balancing network and receiver chain IM3 tones. Therefore, since on the Rx side is very hard to achieve good linearity without NF degradation or power consumption penalties, the balancing non-linearities should be negligible with respect to the rest of the chain. To meet this goal more than 73dBm of IIP3 must be achieved requiring an attenuation of at least 6dB as reported in Table 3.1.

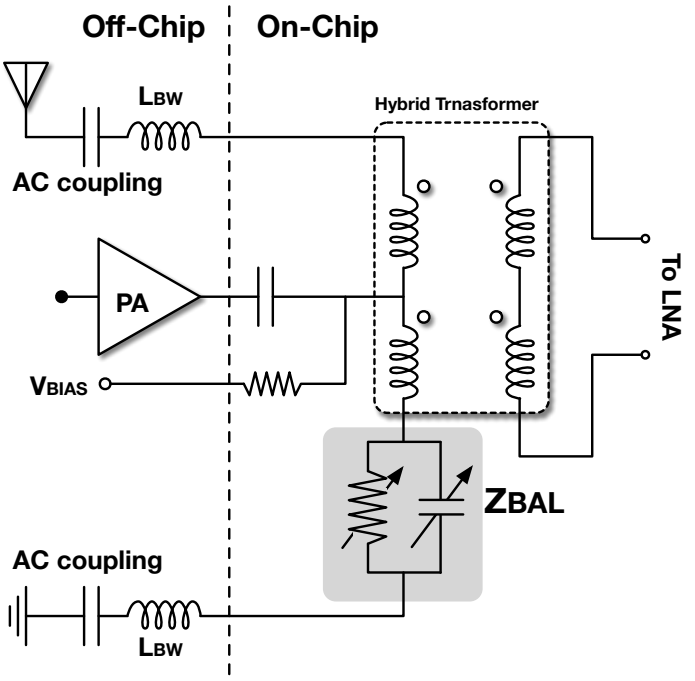


FIGURE 3.14: Hybrid transformer connection for high voltage swing capability.

In order to guarantee the correct state (ON or OFF) of all the switches of a stack, a bias voltage must be applied on the V_{REF} pin. In the capacitor bank this not represents an issue, since no DC current can flow but, on the other hand, in the resistor stack to avoid a high DC current that would lead to a lower linearity, an AC coupling is required.
In Figure 3.14 is shown the conceptual schematic of the implemented solution. The PA is AC coupled since a different DC voltage is required at the balancing impedance node. The ground and the antenna, for symmetry, are AC coupled to avoid a DC current and to limit the impedance mismatch.

Thanks to the AC coupling and a high number of series elements that reduce the voltage swing across the switches, It is possible to achieve the linearity requirements ensuring a lifetime of more than 10 years.

3.3.4 Resonant Mixer, Divider and Base Band

The output current of the LNTA is down-converted through I and Q passive mixers driven by a 25% duty-cycle LO. Due to the balancing impedance, at least 3dB of NF degradation is experienced requiring a reduction of the all the Rx chain blocks noise to be compatible with the current solutions (5 to 6dB of overall NF

are acceptable). In order to limit the noise folding and improve the harmonic rejection a resonant mixer, as the one presented in Section 2.3, has been adopted.

Although the CW blocker in 3G is much lower (-15dBm instead of 0dBm), the reciprocal mixing effect still can degrade the NF down-converting the PN of the LO. As reported in Section 1.2.2, for a SAW-less design, the phase-noise must be reduced by the same amount of filtering originally provided. It follows that the PN of the LO should be lower than -157dBc/Hz to minimize the SNR degradation. Since the LO generation and distribution are typically the most power hungry sections and the low PN requirement increases the power consumption of these blocks, a divider with an intrinsic 25% duty-cycle, as the one proposed in Section 2.3.3, can be used to limit the power dissipation.

High dynamic range for the BB stage is required to handle both in-band and out-of-band interferes without degrading the NF. In addition, the current-mode architecture adopted requires low input impedance in order to achieve high linearity. The BB proposed in Section 2.4 has been exploited setting the parameter to meet the 3G requirements. For simplicity no reconfigurability is implemented, however the same approach proposed in Section 2.4 could be used to cover the PVT variations. Moreover a filtering ADC [4] could be implemented to directly interface the analog section to the digital section.

3.4 Prototype and Simulation

A chip prototype in 28nm CMOS technology of the proposed Duplexer-less hybrid-transformer-based analog front-end was fabricated. Since at the time of this thesis submission the die is still under fabrication in Figure 3.15 is reported the layout of the proposed design. While the receiver chain operates with a supply voltage of 1.8V, the 25% duty-cycle divider uses a 1V supply. The LNTA draws about 6.5mA, 3mA for each branch of the core while the remaining is used for mirror/bias stages and common-mode feedback. The entire I and Q base-band consumes only 3.6mA. Each Rauch filter (I or Q path) has a feedback resistor with a nominal value of 3.5kΩ and 150Ω fixed series resistor (R_1). The feedback capacitance is 20pF while the input capacitance is composed by 170pF differential (C_{1D}) and 20pF single-ended (C_{1SE}). To simplify the integrated structure no tuning is implemented to change the gain, bandwidth or Q, therefore PVT variations

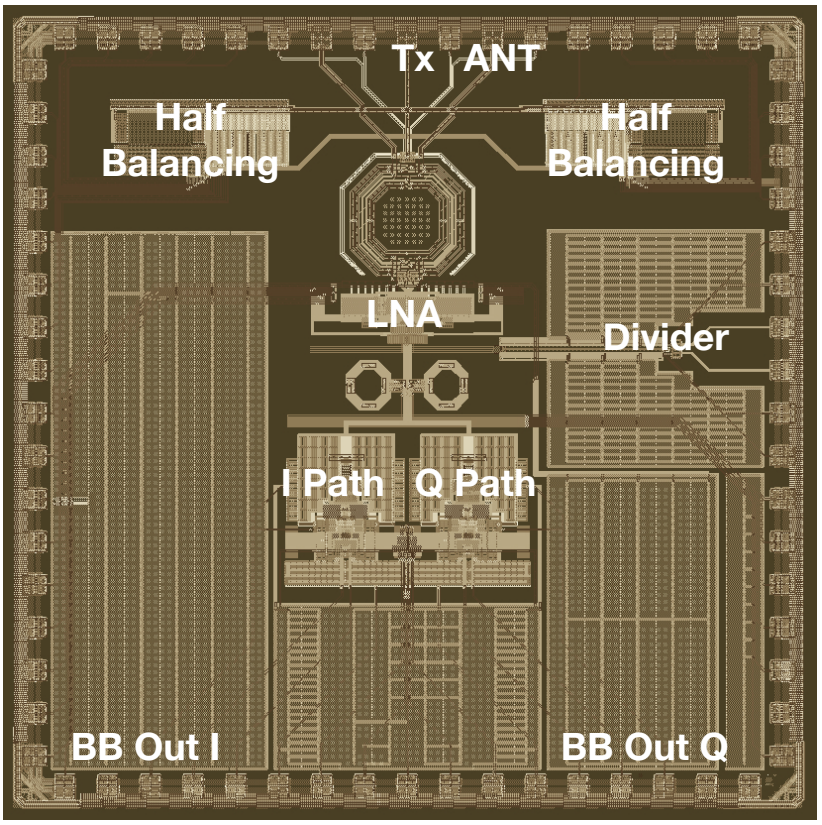


FIGURE 3.15: Layout of the proposed Duplexer-less analog front-end.

will be experienced. However this feature can be implemented in a second time without performances penalties.

The area required to integrate the entire structure is about 0.72mm^2. In Table 3.2 is reported the space occupation for each one of the chain building blocks. Thanks to a simpler HT, smaller area is used compared to the best of the art

TABLE 3.2: Building blocks space occupation

Building Block	**Area** [mm^2]
Balancing	0.245
Transformer	0.148
LNA	0.060
Resonant Mixer	0.075
BB	0.325

receiver chain [44]. Indeed in [43] smaller area was achieved (about 0.6mm^2) but only the LNA, without any mixer and BB, was implemented.

To perform the simulations a test-bench running under *Cadence® Spectre®* Circuit Simulator has been used. The input HT has been electromagnetic simulated by *EMX®* and its S-parameters included in the test-bench.

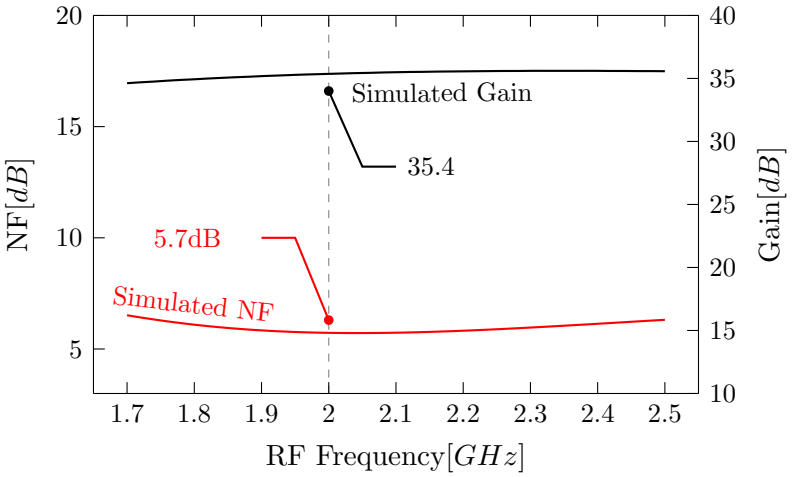


FIGURE 3.16: Simulated Gain and NF.

Figure 3.16 shows the gain and the NF of the receiver. The prototype has been designed to operate around 2GHz at which achieve the minimum NF of 5.7dB. The gain, as well as the NF, is almost flat all over the high bands (see Table 1.1) with an average value of 35.7dB. Since the Rauch stage filter-out the blockers and the Tx leakage residue, more gain can be provided adding further stages without any penalty in terms of linearity.

Even if the gain and NF are relatively wide-band the useful band is limited by the balancing achieved. The balancing impedance is connected to ground trough a bonding wire as shown in Figure 3.17. Such a network creates a resonance in the impedance response limiting the useful band. Figure 3.18 shows the differential voltage between the antenna and balancing nodes. This voltage represents the Tx leakage residue and *de facto* sets the maximum frequency-separation between Tx and Rx bands that is tolerable. When an ideal board-chip interface is considered (no bonding wire) a flat broadband balancing is achieved. On the other hand, when a more real network is analysed the relatively narrow band response limits the frequency range (e.g. 400MHz of Figure 3.18) in which the Tx signal can be satisfactorily balanced in both Tx and the Rx bands (e.g. 50dB of a good external Duplexer). If used outside this range, the unbalancing of the transmitter signal in the Tx band can lead to a breakdown of the LNA MOS transistors even if the Rx

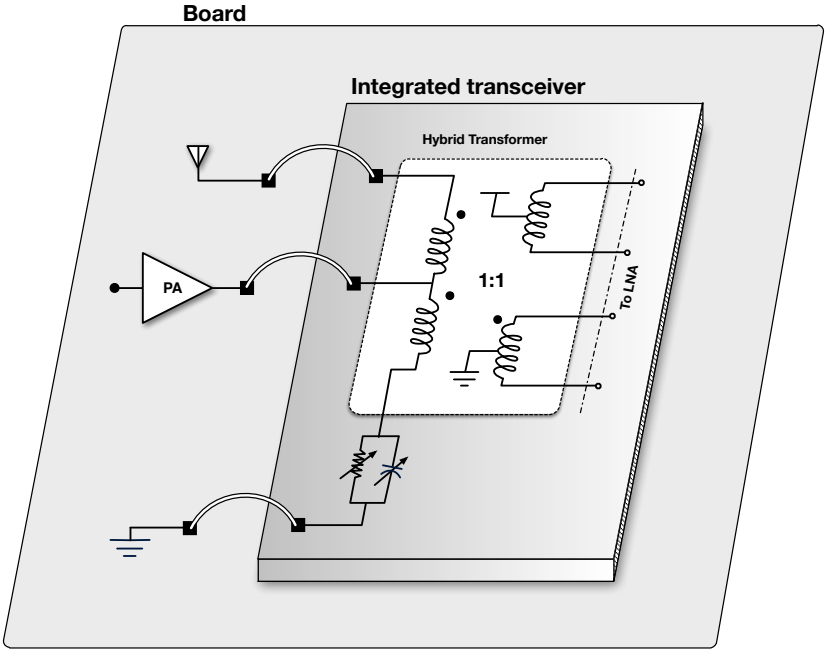


FIGURE 3.17: Board-Die bonding interface.

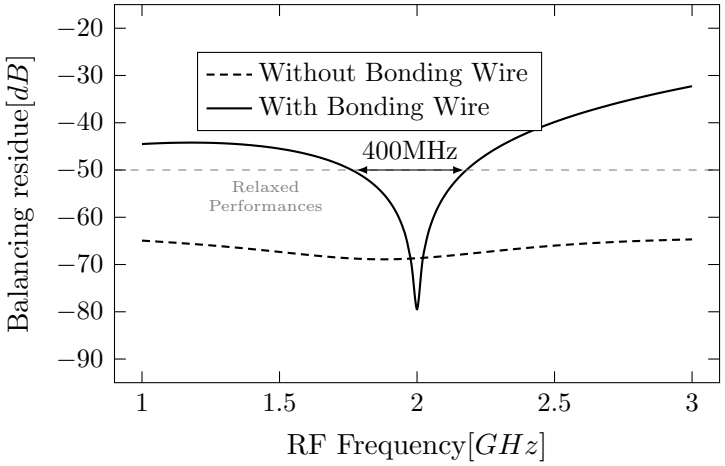


FIGURE 3.18: Simulated differential voltage between Antenna and Balancing nodes.

and Tx are electrically separated. It follows that the Tx signal must be balanced leaving the Tx noise leaking into Rx band degrading the NF.

Another limit to the usability is the antenna and balancing impedance mismatch that, due to either limited resolution of the Z_{BAL} or antenna impedance variations [45], can be present. The amount of mismatch tolerable and hence the Tx signal leakage acceptable depends on the chain intrinsic linearity, since a more

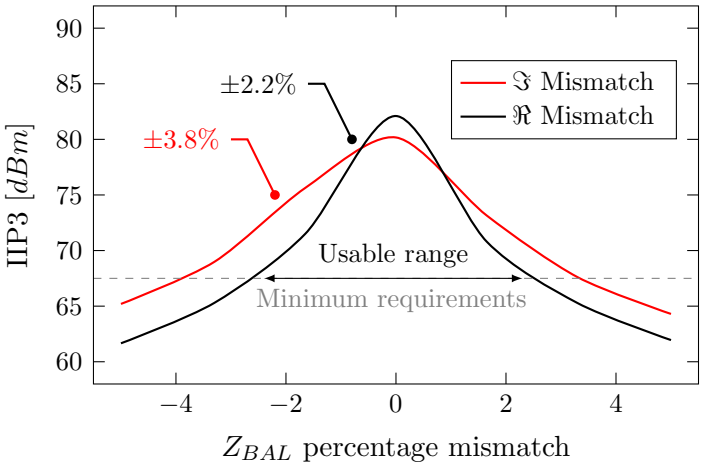


FIGURE 3.19: IIP3 variation as a function of the balancing impedance mismatch.

linear system can tolerate a higher leakage. As reported in Table 1.1 the IIP3 required, measured at the the antenna, is around 67.5dBm. Figure 3.19 shows the simulated IIP3 varying the mismatch percentage, with respect to the nominal value, of the resistor (Real component $\Re$) or capacitor (Imaginary component $\Im$) values of the balancing impedance network.

Thanks to the high linearity of the architecture, a mismatch up to ±2.2% of the resistor or up to ±3.8% of the capacitor is tolerable to meet the IIP3 requirements. However a higher resolution than the maximum mismatch acceptable is suitable to increase the robustness of the system, covering the spreads in fabrication and track the antenna impedance in a smoother way.

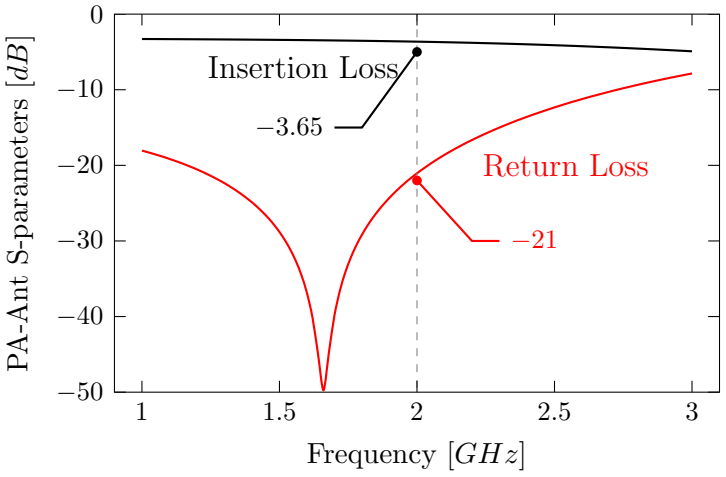


FIGURE 3.20: Simulated TX insertion and return loss.

Figure 3.20 reports the simulated insertion and return loss of the PA-antenna interface. At 2GHz the PA is well matched (-21dB of return loss) making it compatible with the current architectures. The insertion loss is 3.6dB, 3dB due to the balancing network and 0.6dB of the HT intrinsic loss. These values are comparable with the best of the art [43] but this amount of loss degrades the PA efficiency and is not very suitable since the PA is the most power hungry block of the transceiver. However a co-design of the Tx and Rx could potentially exploit the built-in impedance transformations [45]. Potentially an unmatched PA could be implemented increasing the efficiency hence restoring a level comparable to the current solutions.

TABLE 3.3: Comparison with recently published Hybrid Transformer-based receivers

Parameter	**[39] ISSCC2009**	**[43] MTT2013**	**[44] CICC2013**	**This Work**
Frequency [GHz]	1.5-2.5	1.7-2.1	1.7-2.2	1.8-2.2
Isolation in TX Band [dB]	> 50	> 50	> 50	> 50
Isolation in RX Band [dB]	> 50	> 50	> 50	> 50
Max. TX Power [dBm]	N.A.	27	27	27
TX Insertion Loss [dB]	4.2	4.7[1]	4.5[1]	3.65
Cascaded Noise Figure [dB]	7.4	6.7[1]	6.1[1]	5.7
Gain [dB]	24	18	45	36
Current Consumption [mA]	6	20	28.4[2]	10.1
Divider Consumption [mA]	N.A.	N.A.	-	6.5
Entire Receiver	no	no	yes	yes
Technology	40nm	90nm	65nm	28nm
Area [mm^2]	0.2	0.6	2.2	0.72

[1] Considering off-chip balun insertion loss of 0.8dB
[2] Converted in 1.8V supply

The performances of the hybrid transformer-based transceiver are summarized and compared to other state-of-the-art implementations in Table 3.3. All the structures cover more bands and well isolate the Rx from the TX but only the more recent ones handle the full power transmission. This work achieves the lowest Tx insertion loss and NF thanks to the simplicity of the HT implemented (single HT and low number of turns) and avoiding the external BALUN. Exploiting the *p-n* structure for the LNA and the intrinsic 25% duty-cycle divider, low power dissipation is required to meet the tough requirements. A small area is used thanks to the high linearity achieved that allows the use of a simpler HT compared to the

other receiver chain.
Even though the performances achieved are very promising, measurements results must validate the simulations run so far.

3.5 System level overview

Here a little overview and considerations about the system level implementation are reported. Although an extensively and in-depth study was not carried-out, since is not the purpose of this work, is still possible to analyse the main issues and advantages of the integrated-duplexer approach.

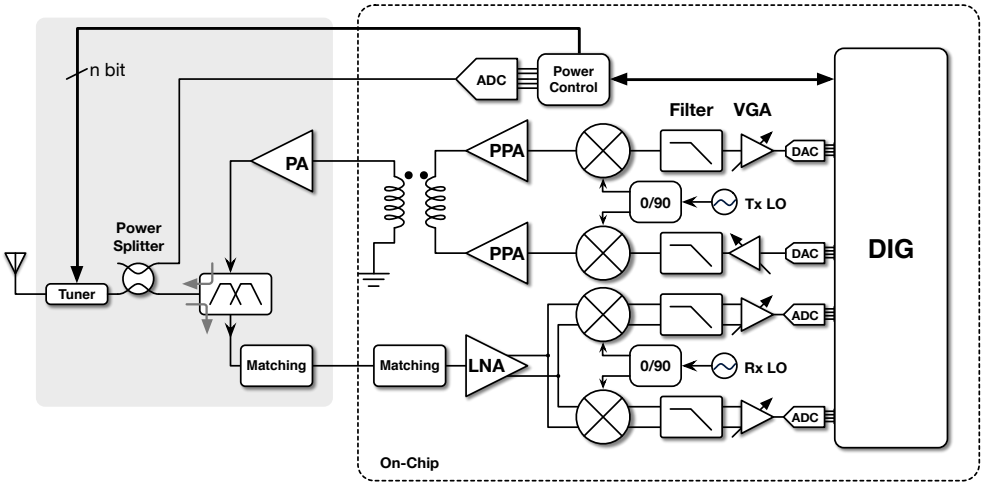


FIGURE 3.21: Typical platform for FDD access transceiver.

In Section 1.1 the global platform diagram block has been shown. The extensively use of Duplexer and SAW filters not only complicates the board but also increases the overall cost. However, focusing on FDD access like world, more components are required to guarantee the correct operation and high-end performances. In particular, as shown in Figure 3.21, a power splitter (typically 10dB splitter) senses the reflected power due to the impedance unmatching of the antenna and the Duplexer. This information is used, after the proper elaboration, to control the impedance tuner positioned between them.

In the previous works and in the proposed one, the balancing network is tuned in order to track the antenna impedance. This solution makes the testability easier since almost the correct impedance (50Ω) can be place outside for the tests. The fine-tuning provided by the integrated balancing network is used to achieve better

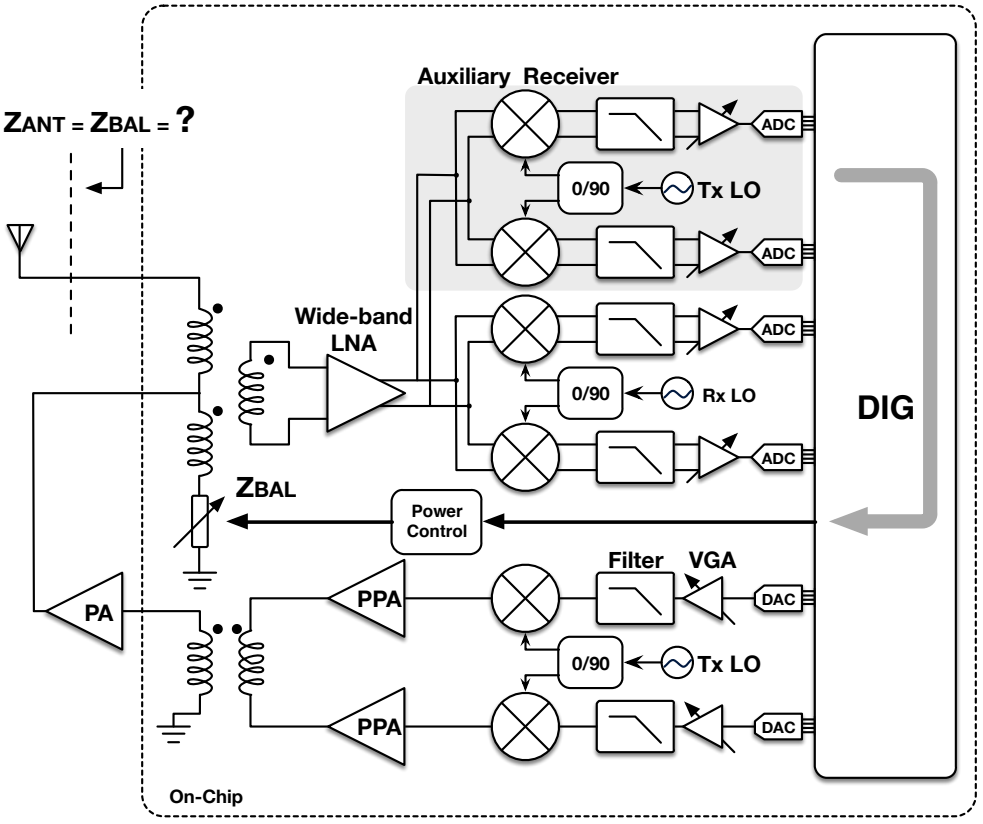


FIGURE 3.22: Possible platform for FDD access transceiver with integrated duplexer.

matching and to center the frequency.

During the full-duplex test (receive and transmit at the same time) a generator used to inject the receiver signal at the antenna port. The 50Ω impedance of the signal generator are used for the matching but some external network can be used to compensate the error introduced by the lines. Again the balancing network is sued for fine-tuning. In both cases, the matching is obtained minimizing the Tx output signal coming from the main receiver. However, in a hypothetical system implementation with the real antenna, the impedance should cover a wide range [45]. The information about the impedance mismatch must be very accurate and could be obtained by a dedicated auxiliary receiver properly designed to down-converts the residual Tx signal, as shown in Figure 3.22. However such an approach leads to a balanced network with an absolute value different from the optimum impedance required to maximize PA power efficiency.

Since the PA efficiency strictly depends on the load impedance (the parallel of the antenna and balancing impedances), the correct value should be restored. Two ways could be taken, the first is to use an external tuner as the one used in the

modern platforms with the cost and complexity associated, the second is shown in Figure 3.23.

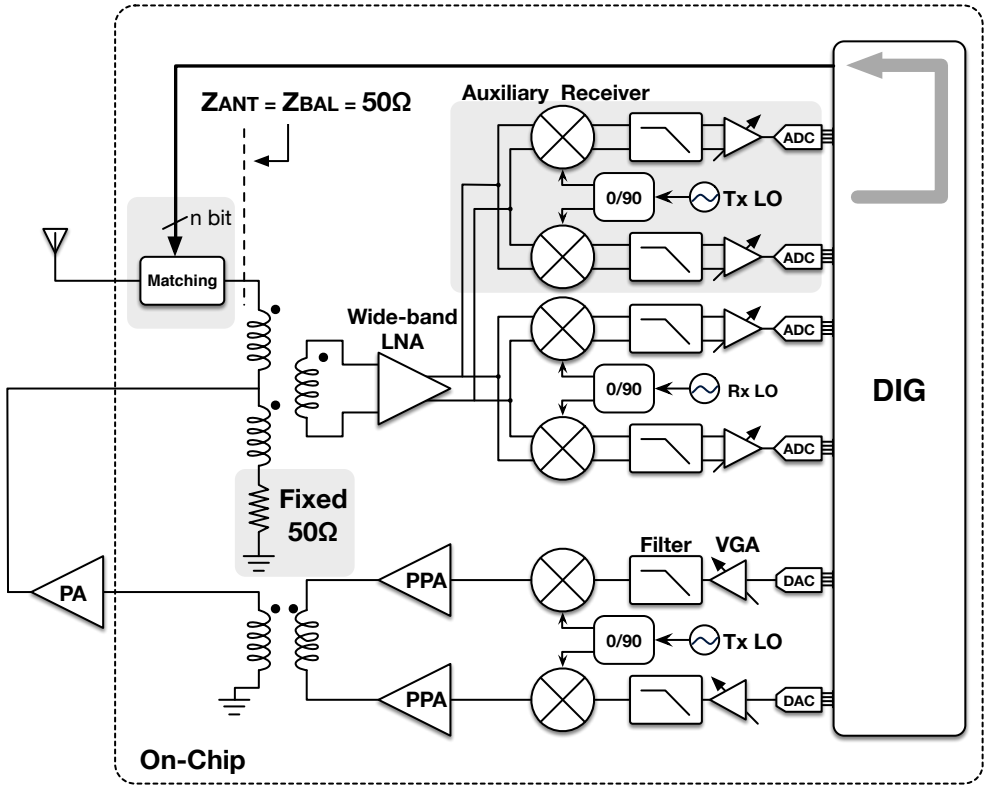


FIGURE 3.23: Possible platform for FDD access transceiver with integrated duplexer and fixed balancing impedance.

The balancing impedance is now fixed with a nominal value of 50Ω (some calibration to cover the PVT variations could still be implemented). This approach not only sets the right impedance value but also it doesn't require any external component since the matching impedance network could be placed inside the chip at the antenna port side. Moreover, in a long term view following the current trend to integrate the different part of the platform all together, if the PA is integrated with the transceiver it can be co-designed with the impedance value that maximize the efficiency and not the one that the SAW filters require (50Ω).

However, as stated before, this section does not presume to cover exhaustively the subject but anyway is a starting point for future works and study.

Conclusion

The increasing demand of speed data transfer capability in mobile smart phones is leading to more sophisticated and complex communication standards. The use of multiple bands and multiple antennas is becoming essential to satisfy the always more stringent requirements imposed by the new standards. The typical approach that uses external and bulky filters, adopted so far, is no more applicable due to the platform complexity and cost. Moreover the scaling down technology could be potentially limited due to pins counting. A one chip wide-band transceiver able to manage all the different standards with few input-output pins would be the best solution.
This thesis dealt with the two main and most diffused standards (2G and 3G), proposing two innovative solutions able to meet all the requirements and putting a new step in the SAW-less analog front-end receivers approach. Although is still far from a SDR architecture, this potentially allow the use of only one single integrated transceiver directly connected to the antennas trough a few switches to select the standard.

In Chapter 2 a wide-band SE blocker tolerant receiver suitable for use without a SAW filter in very demanding applications for 2G standard was described. The use of such a transceiver in high performances smart phones should give big savings in board size and overall BOM. Its key feature is the ability to meet very demanding specifications without requiring large power consumption and area while providing a very solid design thanks to the use of a differential signal path throughout the chip. The main limitation of the implemented prototype is a NF 1dB higher than expected due to a combination of effects, which limits its use in high-end terminals. A re-design of the balun and of the LNA ground connection should produce an antenna sensitivity better than that existing high-end transceivers.

With the same architecture, a fully differential transceiver suitable for FDD applications achieves almost 2dB better NF with the same power consumption and 15% less area due to the simpler transformer but it still requires an external duplexer.

In Chapter 3 a forward step has been taken. Using the high linear architecture proposed in Chapter 2, an integrated duplexer transformer-based receiver able to meet the tough 3G requirements without external duplexer was described. This solution not only should simplify the board complexity and give a big saving in the overall BOM but also finally allow the complete removing of external filters. Thanks to the high linearity of the implemented current-mode chain a simpler hybrid transformer and low power consumption can be exploit. Considering the overall NF of a typical architecture due to the insertion loss of a commercial Duplexer and power splitter and receiver chain noise, the proposed solution achieves comparable NF performances. On the other hand, the PA efficiency-drop due to the HT insertion loss remains the main limitation of this architecture. For a real product implementation the PA efficiency should be improved and an integrated antenna impedance-tracking loop should be implemented.
Although the simulated results are very promising compared with the state-of-the-art, measurements results must validate the performances achieved.

Appendix A

Impact of non-linearities products on SNR

The receiver chain aims to discriminate the tiny wanted signal amongst the huge interferes without a significant SNR degradation. In a typical receiver, which uses SAW filters, it means just a low NF requirement. However in a SAW-less design the amount of NF degradation could strongly depend on the level of the non-linear products that fall in band, which can be produced either by in-band and out-of-band blockers. While the firsts are very weak the seconds can be up to 0dBm (e.g. GSM) and can seriously impact on the receiver performances. To correctly define the requirements the first step is to determinate which tones could fall in band.
Considering a receiver block with a non-linear behaviour that can be represented by:

$$y(t) = a_1 \cdot x(t) + a_2 \cdot x^2(t) + a_3 \cdot x^3(t) \tag{A.1}$$

Where a_1, a_2, a_3 are the coefficients of the linear response, second-order non-linearity and third-order non-linearity respectively.
Assuming an input signal with only one tone as $x(t) = A \cdot \cos(\omega_0 t)$, Equation (A.1) becomes:

$$y(t) = \frac{a_2 A^2}{2} + (a_1 + \frac{3a_3 A^3}{4}) \cos(\omega_0 t) + \frac{a_2 A^2}{2} \cos(2\omega_0 t) + \frac{a_3 A^3}{4} \cos(3\omega_0 t) \tag{A.2}$$

If we consider that the blocker is not at Rx frequency, no one of these terms fall in the wanted band. However, since no more RF filtering is present, the receiver chain can still experience desensitization if the blocker is very powerful.

If we now consider an input signal composed by two tones as $x(t) = A_1 \cdot cos(\omega_1 t) + A_2 \cdot cos(\omega_2 t)$, Equation (A.1) becomes:

$$\begin{aligned} y(t) = {} & \frac{{A_1}^2 a_2}{2} + \frac{{A_2}^2 a_2}{2} + \\ & + \left(a_1 A_1 + \frac{3}{4} {A_1}^3 a_3 + \frac{3}{2} A_1 {A_2}^2 a_3 \right) \cos \omega_1 t + \left(a_1 A_2 + \frac{3}{4} {A_2}^3 a_3 + \frac{3}{2} {A_1}^2 A_1 a_3 \right) \cos \omega_2 t + \\ & + \frac{1}{2} {A_1}^2 a_2 \cos 2\omega_1 t + \frac{1}{2} {A_2}^2 a_2 \cos 2\omega_2 t + \frac{1}{4} {A_1}^3 a_3 \cos 3\omega_1 t + \frac{1}{4} {A_2}^3 a_3 \cos 3\omega_2 t + \\ & + \frac{3}{4} A_1 {A_2}^2 a_3 \cos(\omega_1 - 2\omega_2) t + \frac{3}{4} {A_1}^2 A_2 a_3 \cos(2\omega_1 - \omega_2) t + \\ & + \frac{3}{4} {A_1}^2 A_2 a_3 \cos(\omega_1 + 2\omega_2) t + \frac{3}{4} A_1 {A_2}^2 a_3 \cos(2\omega_1 + \omega_2) t + \\ & + A_1 A_2 a_2 \cos(\omega_1 - \omega_2) t + A_1 A_2 a_2 \cos(\omega_1 + \omega_2) t \end{aligned} \quad \text{(A.3)}$$

Which, if $\omega_1 \simeq \omega_2$, produce the spectrum shown in Figure A.1. Typically only the products at $2\omega_1 - \omega_2$ and $\omega_1 - 2\omega_2$ can fall in band causing the performances degradation since the interferes at ω_1 and ω_2 are close to the Rx band. It follows

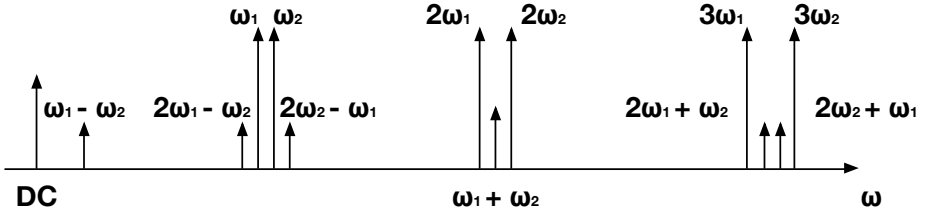


FIGURE A.1: Non-linearities products due to two input tones.

that tones due to third-order non linearities should be lower than the noise floor to be negligible or must be considered in the calculation.

Figure A.2 shows the test in which the non-linearities fall in band. The original SNR to pass the sensitivity test is represented by the difference, in dBm, of the wanted signal and noise-floor (S/N_{floor}). The Signal-to-Intermodulation-ratio, represented by $S/IM3$, considers the difference, in dBm, of the wanted signal and non-linearities that fall in band. When both effects are considered the equivalent SNR which define the final BER is given by:

$$SNR_{eq} = \left| \frac{S}{IM3 + N_{floor}} \right|_{dBm} \quad \text{(A.4)}$$

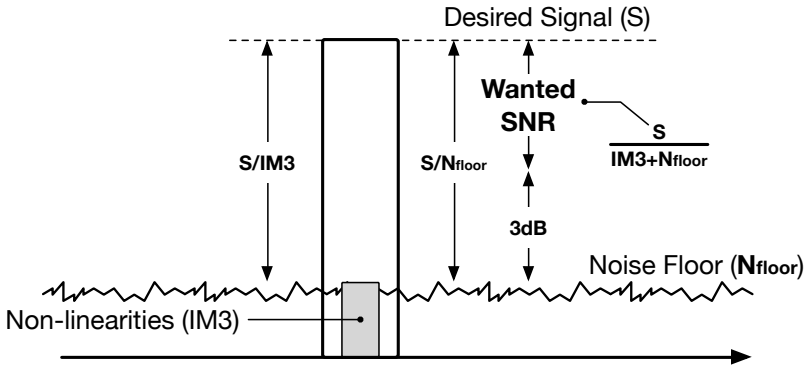


FIGURE A.2: Non-linearities impact on final SNR.

Both 2G and 3G define sensitivity level 3dB higher during the blocker test. If we consider that the noise-floor and the non-linearities have the same level, the equivalent SNR (SNR_{eq}) is 3dB lower than the sensitivity test and pass the blocker test. It follows that the NF degradation is completely due to the limited IIP3 of the receiver. However, when the blocker hits the receiver, the noise floor could increase due to either reciprocal mixing effect and gain compression causing the failure of the test.
Considering again the case of a fixed level of noise-floor, the $IM3$ components have the same power of the noise-floor and are expressed by:

$$IM3 = P_{tones} - N_{Floor} \tag{A.5}$$

Where all these quantities are expressed in dBm, P_{tones} is the power associated to the blockers that cause the non-linearities and N_{Floor} is power density of the noise at the antenna in the sensitivity test. It follows that the IIP3 required to meet the specifications is given by:

$$IIP3 = P_{tones} - \frac{IM3}{2} \tag{A.6}$$

Where again all the quantities are expressed in dBm and IM3 is defined as in Equation (A.5).

While for 2G standard only one tone is present in the out-of-band blocker test demanding high compression point, in 3G the simultaneously presence of the huge Tx signal and the blocker demands a high linear receiver (high IIP3) due to the IM3 tones that could fall in the Rx band.

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