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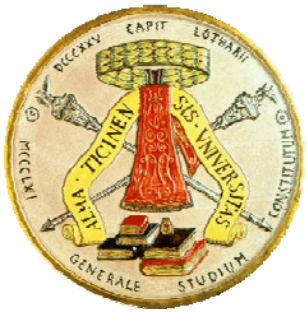

DOTTORATO DI RICERCA IN MICROELETTRONICA
XXIII CICLO

CIRCUITS AND ARCHITECTURES FOR 60 GHZ RECEIVER FRONT-ENDS IN CMOS TECHNOLOGY

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Introduction

The advances in complementary metal oxide semiconductor (CMOS) technology have made fully integrated RF CMOS transceivers a reality.
CMOS technology with relatively low production costs have been successfully used to implement all the RF functionalities for the existing and emerging wireless local-personal area networks (WLAN / WPAN) standards such as 802 .11 a / b / g, the ultra-wideband (UWB, 802.15.3a) and Bluetooth.
All these systems operate below 10GHz, where the frequency spectrum is reaching the congestion leading to the need to move towards the large and unused millimeter-wave bandwidth between 30GHz and 300GHz.
In 2001 the *Federal Communication Commission* (FCC) has made available a 7GHz "*unlicensed*" band between 57 and 64GHz for wireless communications and many research institutions and companies have begun to study new mm-w wireless systems.
Millimeter-wave system specifications are now almost completely standardized by the IEEE Task Group 3c, which was created in march 2005 and soon began working on drafting a protocol called IEEE 802.15.3c. This document had the proposal to uniquely set the allocation of operating bands, the specifics for the radio transmissions and performance standards that the transmission and reception equipment used should provide.
On October 2009 a final draft of this protocol, that defines an alternative physical layer operating in the mm-W band along with the necessary MAC changes to support this PHY, has been presented.
Millimeter-wave wireless communications allow high data rates (up to 6Gbps), higher integration levels, strong levels of frequency reuse and enhanced safety due to the strong amount of materials absorption at these frequencies. These features make this band suitable for a variety of applications such as high speed WLANs, wireless short-range systems for inter-vehicle and roadside to vehicle communications (IVC and RVC), broad-band services distribution (ITS's), optical fiber extension and LAN bridges.
The present thesis in particular addresses multi-Giga data-rates WLAN applications, that is high-speed internet access, wireless high speed file transfers, uncompressed exchange of information between TV, cameras, DVD and other appliances.
The design of mm-w systems for high speed WLAN presents many design challenges mainly related to the high operative frequencies, close to the cut-off frequency of the last technologies' transistors. A design approach based on different levels is of primary importance: device, building blocks, circuital topology and transceiver architecture have to be studied in parallel. Moreover, in order to fully account for the behaviour of active and passive devices up to 60GHz is necessary to carefully design, model and characterize these devices

(mos, varactors, inductors, capacitors and transmission lines). A careful optimization of the layout is also of primary importance to achieve good performances and represents, also from the standpoint of time required, an important part of the project.

Around 60GHz the design of any building block in the RF receive chain pose many design challenges. The research activity object of this thesis is focused on the design of high performances voltage controlled oscillators and low noise amplifiers operating in the mm-wave band.

The high operative frequencies, close to the transistor intrinsic cut-off frequency limits the active devices available power gain, making the design of both VCOs and LNAs more challenging . The necessity of employing nanoscale technologies to achieve the desired operation at mm-waves leads to reduced supply voltages and hence, limited headroom and linearity for LNAs. Lower intrinsic gain also decreases the margin for modeling errors and requires a careful prediction of device characteristics. Finally, reduced transistor gain means also less margin for process/temperature/voltage variations.

Operating the CMOS devices at frequencies close to the transistor f_t values also increases their intrinsic minimum noise factor, imposing the need to get as close as possible to this minimum.

Another important issue lies in the poor quality factor of passives at 60GHz which makes tradeoffs between the phase noise, tuning range and power consumption much more severe in VCOs and plays a crucial role in the achievable gain and bandwidth of LNAs.

In a mm-wave VCO the quality factor of capacitors, usually much lower that the inductor's one, dominates the overall Q of the tank; this is even more true for variable capacitance, both MOS varactors and switched metal-oxid-metal (MoM) capacitors, where additional losses are brought about by active device limitations such as gate resistance, finite channel conductance and parasitic drain/source capacitance.

The poor quality factors of passive elements limit the performances of the active devices and the difficulty in accurately modeling all the physical phenomena that affect their behavior, such as substrate coupling and skin effect, makes it extremely difficult to predict the actual circuit performances.

Furthermore, substrate coupling could easily bring the LNA to instability.

Millimeter-wave passive models for CMOS components are not readily available; therefore, extensive electromagnetic simulations must be performed on each single device.

It should be emphasized that accurate electromagnetic simulations on complex structures often require heavy computational tasks necessitating some layout simplifications to complete simulations in an acceptable time.

Also distributed effect must be taken into account: any interconnect within the circuit which is an appreciable size of a wavelength should be treated as transmission lines and accurately modeled. Transmission lines, therefore, become very important elements in the entire millimeter-wave portion of the radio, as they are widely used as both interconnects and to realize passive components, as an alternative to lumped inductors.

At 60GHz also metal dummies, needed to cover the required metal densities on the chip area, represent an important issue; for the sake of modeling accuracy at 60GHz, it is highly desirable to prefill all metal layers around inductors or t-lines, preventing further density enforcement which is beyond circuit designer's control. The effect of these prefillers on passives behavior must be verified through EM simulations.

In the designed VCOs and LNA, all these issues have been addressed with a proper choice of the most suited circuit topology and through a careful optimization of each active and passive device. Massive electromagnetic simulations and direct on-chip characterizations of active and passive devices has been carried out to accurately model all devices.

Some of these issues, such as limited achievable gain and high noise figure of 60GHz low noise amplifier and the strong sensitivity to device modeling, could be partly relaxed adopting a phased array based approach.

Integration of a complete phased array system in silicon results in substantial improvements in cost, size and reliability providing opportunities to perform on-chip signal processing and conditioning.

At the circuits level, the division of the signal into multiple parallel paths relaxes the power handling and noise requirements for each individual active devices. The higher SNR at the output together with the lower interference translate into higher channel capability, while the directivity of the transmit-receive pairs can result into higher frequency reuse ratios and consequently higher network capabilities.

In all phased array architectures, except the RF recombination one, LO distribution represents a difficult task, and, if a direct-conversion topology is chosen, also the I/Q LO generation becomes challenging. Quadrature LO generation typically degrades the generation system performances considerably if classical coupled-oscillators are exploited and the I/Q outputs of the coupled-VCOs must travel large distances to reach every single mixer in the array, thus experiencing significant losses and mismatches.

These problems could be largely overcome by combining the LO generation and distribution tasks through the use of a spatially distributed oscillator. I/Q LO signals have to be directly available at the spatially separated I/O LO ports of each direct down-conversion mixer without the need for a lossy distribution network.

In this thesis a spatially distributed LO generation system for a phased-array direct conversion receiver adopting the IF recombination approach is presented. It is based on the use of coupled rotary traveling wave VCOs.

Coupling between different RTWO loops is performed adopting an "hybrid" traveling-standing waves based structure: the $\lambda/2$ twisted closed loops support traveling waves and are physically connected using $\lambda/4$ transmission lines that support standing waves. These t-lines provide both coupling between different loops as well as DC bias.

Such an LO generation and distribution system, not only allows to provide good phase noise performances and good tuning capabilities, but also to reduce, tanks to the coupling mechanism, the overall LO generation and distribution system phase noise by a factor $10\log(N)$, if N loops are coupled. Furthermore the adopted coupling technique prevents spurious oscillation modes that arise if rotary travelling-wave VCOs are directly connected to

form a bigger loop which performs a total phase shift $\Phi_e=2K\pi$, or using other more conventional coupling techniques.

Chapter I reviews the main characteristics of millimeter-waves propagation, the main application fields and the emerging standards for mm-wave wireless communications.

The advantages and limitations of the different available technologies and some possible alternative architecture for a 60GHz front-end are discussed.

In **Chapter II**, after a brief introduction on the major challenges in designing mm-wave voltage controlled oscillators and the different circuital topologies suitable for 60GHz applications, the design and characterization of both a 53GHz low phase noise digitally-controlled oscillator and of a standing-wave voltage controlled oscillator operating in the 71-73GHz band (both implemented in 90nm CMOS technology) are presented.

Chapter III deals with the 60GHz LNA design; in the first section of the chapter 60GHz LNA challenges are discussed while in the second section are described the most widely used circuital topologies analyzing, for each solution, advantages and drawbacks . In the third section an analytical study for LNA noise figure minimization is reported and in the last section the design and characterization of a 60GHz low noise amplifier implemented in 65nm CMOS technology is described.

In **Chapter IV** the phased-array concept and the advantages and drawbacks of the various phased-array architectural approaches are presented. The LO distribution problem is then discussed.

The second part of the chapter focuses on the description of the proposed LO generation and distribution system.

The conclusions summarizes the major contributions of this thesis and suggest topics which merit further work.

_____ Chapter I _____

Transceivers for mmW Wireless Personal Area Networks

1.1 Wireless networks evolution
From 802.11 to UWB towards mm-W communications - The legislation in different countries – 60GHz standardization.
1.2 60GHz wireless transmissions opportunities
Millimeter Wave propagation - 60GHz wireless communications: main applications – Feasible link performances - Dual-band operation: 5-60GHz.
1.3 Receiver architecture choice
Alternative receiver architectures for 60GHz wireless transmissions – Antennas at 60GHz.
1.4 Front-end technology
Why silicon? – Transistor modeling
Conclusions

The viability of radio frequency communication systems has been demonstrated by several hundred years, and today the use of radio-frequency for broadband information transport over long distances is common, as shown by the proliferation of satellites orbiting the earth and microwave antennas scattered throughout the world.
The limited frequency spectrum available for radio transmissions and the need for ever higher data rates have brought to develop more advanced and sophisticated systems: the old coaxial cable transmission systems have been so replaced by fiber, which for several years has been the perfect answer to the needs of users.
In many large cities have been installed bundles of optical fiber capable of delivering high quantities of data. These were ideal for high capability transmission over long distances (eg transoceanic connections), but proved unsuitable, mainly due to high installation costs, for low-medium capacity links over short distances.

As a result, recent years have witnessed the birth of many new wireless "*point to point*" technologies, capable of providing even higher performances than those of the fibers and of supporting a wide variety of architectures.
These new technologies meet the following criteria:

- short range links ;
- High data rates;
- low costs;
- High security;

Many systems using new unallocated portions of the spectrum have been studied and developed, and in recent years the 60GHz band in particular, has became a center of gravity for academic and industrial research.
In July 2003 the IEEE 802.15.3 working group for WPAN began investigating the use of the 7GHz unlicensed spectrum at millimeter-Wave frequencies as an alternative physical layer (PHY) to enable very high data rate applications such as high-speed Internet access, wireless A/V(audio/video) cable replacement, wireless high speed file transfer e.g. download hour-long movie files within one minute, uncompressed exchange of information between TV, cameras, DVD and other appliances.
The targeted data rate for these applications is greater than 2Gb/s; although the excessively high path loss at 60GHz due to oxygen absorption precludes communications over distances greater than a few kilometers, short-range WPANs actually benefit from the attenuation, which provides extra spatial isolation, high levels of frequency reuse and higher implicit security.
In this chapter we will analyze in detail the characteristics and problems of 60GHz wireless transmissions: the first part will discuss the emerging standards and regulations in different countries; will be then described the most important characteristics of millimeter wave propagation and the main application fields.
Finally, will be discussed the possible alternative architectures for the realization of a 60GHz front-end and the advantages and limitations of the different available technologies.

1.1 Wireless networks evolution

1.1.1 From 802.11 to UWB towards mm-W communications

The advances over the past decade in complementary metal oxide semiconductor (CMOS) technology and the immense research effort in radio frequency (RF) CMOS circuit design techniques have made fully integrated RF CMOS transceiver a reality.
CMOS technology with relatively low production costs have been successfully used to implement all the necessary RF functionalities for the existing and emerging wireless local-personal area networks (WLAN / WPAN) standards such as 802 .11 a / b / g, the ultra-wideband (UWB, 802.15.3a) and Bluetooth.

All these systems [1] operate below 10GHz, where the frequency spectrum is now reaching the congestion; in the very next future will therefore be necessary to move towards the large and unused millimeter-wave bandwidth between 30GHz and 300GHz.
Already in 2001 [2], the *Federal Communication Commission* (FCC) has made available a 7GHz "*unlicensed*" band between 57 and 64GHz for wireless communications, and many research institutions and companies have begun to study new mm-W wireless systems.
mm-W system specifications are now almost completely standardized by the IEEE Task Group 3c, which was created in march 2005 and soon began working on drafting a protocol called IEEE 802.15.3c. This document outlines a proposal that specifies the allocation of operating bands, the specifics for the radio transmissions and performance standards that the transmission and reception equipment used should provide.
On October 2009 a final draft of this protocol has been presented [3]; IEEE Std 802.15.3c-2009 is an amendment to IEEE Std 802.15.3-2003 (reaffirmed in 2008) that defines an alternative physical layer operating in the mm-W band along with the necessary MAC changes to support this PHY.
The objective is to develop an alternative physical layer, in addiction to the existing 802.15.3 Wireless Personal Area Network, based on the use of UWB and Bluetooth.
These are "individual user based" networks which consist of a set of electronic devices that exchange information in an area of radius not exceeding 10 meters.
UWB has already enabled the creation of different links, such as wireless connections between personal computers and peripherals (screen, keyboard, printer, digital camera), transfer pictures from a DVD player to one or more televisions and synchronization of clocks electronic equipment, operating at data rates ranging from 110 Mb/s (for devices at a distance not exceeding 10 m) to 480 Mb/s (for devices placed at a distance of 2m), offering low power consumption.
The new WLAN based on the mm-W transmission [4] offer these and other services (HDTV, home theater etc. ..) at even higher data transfer rates up to 2Gb/s; they also allow high coexistence with all other microwave systems included in 802.15 family.

1.1.2 The legislation in different countries

The mm-Wave PHY operating frequency is within the 57.0–66.0 GHz range as allocated by the regulatory agencies in Europe, Japan, Canada, and the United States. This band will also be available in other areas where allocated by the regulatory bodies.
The regulatory 60GHz bands vary slightly from country to country, but have a large overlap as shown in Fig. 1.1 [3].

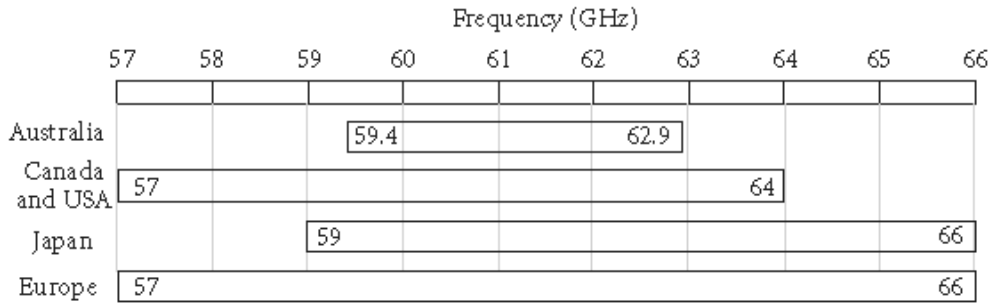

Figure 1.1.: Worldwide unlicensed 60GHz bands

Geographical Region	Power limit	EIRP limit	Regulatory document
USA-Canada	—	Maximum indoor EIRP: 27 dBm Mixiumum outdoor EIRP: 40 dBm	47 FCC 15.255
Europe	—	Maximum EIRP: 43 dBm	ETSI
Japan	Maximum output power: 10dBm Maximum bandwidth: 2,5 GHz	Maximum EIRP: 57 dBm	ARIB STD-T69ARIB STD-T74
Australia	Maximum output power: 10dBm	Maximum EIRP: 51,8 dBm	Radiocommunications Class License 2000

Table 1.1: Maximum transmitted power levels in selected geographical regions

Regulation for the 57-66GHz band allowing license exempted use, are specified in FCC 15.255 in USA, and CEPT Recommendation in Europe. The ETSI document TR 22-03 and ECC Report 114 ETSI DTR/ERM detail regulation issues in Europe, where the 59-63GHz band is mainly assigned to WPAN applications, while the band 63-64GHz is reserved for Intelligent Transportation systems (ITS).
The Millimeter Wave band Frequency Study Group (MWFSG) in Korea allocated the 57-64GHz spectrum to indoor WPAN's with a maximum transmit power of 10dBm. In Japan, the band is defined at 59-66GHz with similar power limits.

1.1.3 60GHz standardization

Standardization in the 60GHz wireless networks is currently under-developed by several industry consortia and international standard organizations [5].
WirelessHD is an industry-led effort to define a next generation wireless high-definition interface specification for consumer electronics products. The

consortium has completed the WirelessHD specification version 1.0 in January 2008.

Ecma International TC48 is also developing a standard for 60GHz technology for very high data-rate short range unlicensed communications to support bulk data transfer such as downloading data from a kiosk and high definition multimedia streaming. It has completed ECMA-387 specification in December 2008. ECMA-387 uses distributed MAC based on MBOA-MAC from WiMedia.

Wireless Gigabit Alliance (WiGig) is yet another effort to standardize 60GHz technology. The goal is to provide a single technology that can support instantaneous file transfers, wireless display and docking, and streaming high definition media on a variety of devices.

In addition, the IEEE 802.11 Very High Throughput (VHT) Study Group is actively studying 60GHz solution for future WPAN standards. In December 2008, Task Group TGad is approved as a result of the work pursued by VHT Study Group. TGad will define enhancement to the IEEE 802.11 standard for 60GHz band. While IEEE 802.15.3c is targeting WPAN, one of the distinct goals of IEEE 802.11 TGad is to maintain WLAN experience such as a larger coverage and backward compatibility to 802.11.

Interest in developing a millimeter wave alternative PHY began in the July 2003 IEEE meeting in San Francisco with the foundation of an interest group. A study group was formally created in the March 2004 IEEE 802 plenary meeting in Orlando and developed a project authorization request that was approved in March 2005.

The first meeting as a task group was in May 2005 in Cairns, Australia and the group worked steadily developing channel models and evaluation documents. The PHY modes were selected in November 2007 at the Atlanta meeting and draft progressed rapidly, entering working group letter ballot in June 2008. After three working group recirculation ballots, sponsor ballot started in March 2009. A total of three sponsor recirculation ballots were held, leading to approval of IEEE Std 802.15.3c-2009 by the IEEE-SA Standards Board on 11 September 2009.

IEEE Std 802.15.3c-2009 is an amendment to IEEE Std 802.15.3-2003 (reaffirmed in 2008) that defines an alternative physical layer operating in the millimeter wave band along with the necessary MAC changes to support this PHY [3][5].

The 802.15.3c WPAN (referred to as a *piconet*) allows a number of independent devices to communicate with each other. A piconet consists of several components, as shown in Fig. 1.2. The basic component of a piconet is devices (DEVs). In particular, one device is required to play the role of a piconet coordinator (PNC). The PNC is responsible to admit devices to be the members of the piconet, keep their information for maintaining the piconet, announce the existence of the piconet, and synchronize communications among devices in the piconet.

In order to address different market segments and realize the different usage models envisioned by the Task Group 3c, three different PHY layer are defined:

- single carrier mode (SC) PHY,
- high speed interface mode (HIS) OFDM OHY,

- audio/visual mode (AV) OFDM PHY.

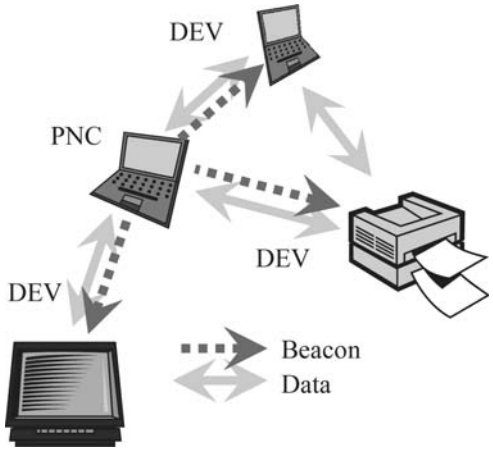

Figure 1.2: A pico-network in 802.15.3c WPAN

All these PHY use the channels defined in Table 1.2.
The center frequencies of these channels are 58.32GHz, 60.48GHz, 62.64GHz and 64.8GHz, and the *Nyquist* bandwidth of each channel is 1.728GHz. The first three channels are used in U.S.A., while the last three channels are used in Japan and Korea.

CHNL_ID	Start frequency	Center frequency	Stop frequency
1	57,240 GHz	58,320 GHz	59,400 GHz
2	59,400 GHz	60,480 GHz	61,560 GHz
3	61,560 GHz	62,640 GHz	63,720 GHz
4	63,720 GHz	64,800 GHz	65,880 GHz

Table1.2: Channellization

The **SC PHY** is designed for low-complexity and low-cost device implementation and has specified the different classes of modulation and coding schemes (MCSs) that enable to serve different wireless connectivity applications. The supported data rates defined by MCSs are categorized as shown in *Table1. 3*. Class 1 is specified to address the low-power low-cost mobile market while maintaining a relatively high data rate of up to around 1.5 Gbps. Class 2 and Class 3 are specified to achieve data rates of up to around 3 Gbps and over 3 Gbps, respectively, to support high-speed multimedia applications.
A frame for the SC PHY is composed of three major parts - preamble, header, and frame body (payload plus FCS) - as shown in Fig. 1.3. The preamble is used for frame detection, channel estimation, frequency recovery, and timing acquisition.
The header for frame control on the PHY and MAC layers is composed of a PHY header, MAC header, and header check sequence (HCS). Three types of preambles and headers - short, medium, and long - are used for transmitting

different kinds of data. The frame body is supported up to the length of 1 MBytes for frame efficiency in high speed data transmission [6].

Class	Data Rate	Modulation	Spreading	FEC
Class1	25,3 Mbps	2/π BPSK	64	RS(255,239)
	405 Mbps		4	
	810 Mbps		2	
	1620 Mbps		1	
	1300 Mbps		1	LDPC(672,504)
	432 Mbps		2	LDPC(672,336)
	864 Mbps		1	
Class2	1730 Mbps	2/π QPSK	1	LDPC(672,336)
	2590 Mbps			LDPC(672,504)
	3020 Mbps			LDPC(672,588)
	3230 Mbps			LDPC(1440,1344)
	3240 Mbps			RS(255,239)
Class3	3890 Mbps	2/π 8PSK	1	LDPC(672,504)
	5180 Mbps	2/π 16QAM	1	LDPC(672,504)

Table1.3: Supported data rates in SC PHY

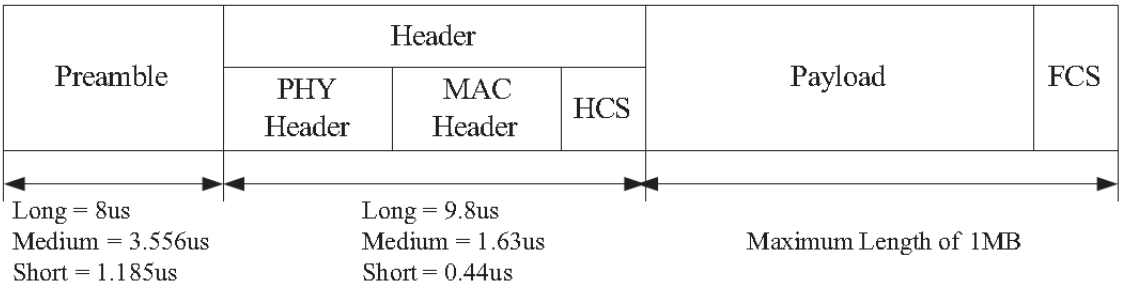

Figure 1.3: SC frame Format

High speed Interface (**HIS**) **OFDM** is designed for non-line-of-sight (NLOS) operation and uses orthogonal frequency domain multiplexing (OFDM). The HIS OFDM mode supports a maximum PHY data-rate up to 5.7 Gbps. It also supports a variety of modulation and coding schemes (MCSs) using different frequency-domain spreading factors, modulations, and LDPC block codes.

Audio/Video (AV) OFDM is designed for supporting uncompressed HD video streaming in a NLOS channel. It is implemented with two PHY modes, the high-rate PHY (HRP) and low-rate PHY (LRP), both of which use OFDM. To meet the multi-Gbps decoding throughput requirement, 2 RS encoders and multiple convolutional encoders are used.

A *mux* is used to multiplex the output of multiple encoded bits, followed by a bit *interleaver* and then mapped to QAM constellation points with Gray coding. Pilot and null tones are inserted to QAM symbols followed by standard operation to generate OFDM symbols.

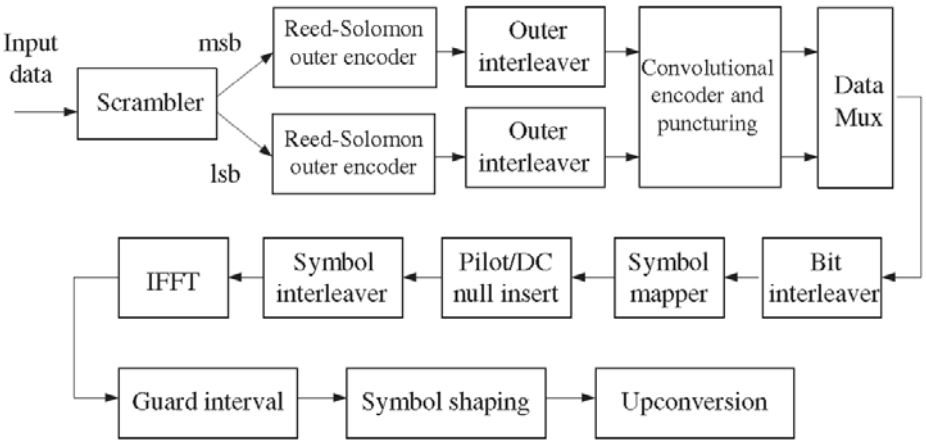

Figure 1.4: Implementation Block diagram of AV OFDM HPR PHY

All broadcast and multicast frames using the AV OFDM PHY are sent using the LRP mode. The LRP mode utilizes spatial diversity and repetition coding for the omni-directional and directional modes. Up to eight antenna directions or phased array patterns may be used that are identified by indices zero through seven. For omni LRPDUs, the repetition coding is implemented by repeating the OFDM symbol and its associated cyclic prefix four or eight times and sending each repetition with a different TX antenna direction or pattern. These antenna directions or patterns are selected such that the transmission covers the region of space that is of interest.

1.2 60GHz wireless transmissions opportunities

1.2.1 Millimeter Wave propagation

The millimeter wave spectrum at 30–300 GHz is of increasing interest to service providers and systems designers because of the wide bandwidths available for carrying communications at this frequency range. Such wide bandwidths are valuable in supporting applications such as high speed data transmission and video distribution.

Planning for millimeter wave spectrum use must take into account the propagation characteristics of radio signals at this frequency range.

While signals at lower frequency bands can propagate for many miles and penetrate more easily through buildings, millimeter wave signals can travel only a few miles or less and do not penetrate solid materials very well. However, these characteristics of millimeter wave propagation are not necessarily disadvantageous. Millimeter waves can permit more densely packed communications links, thus providing very efficient spectrum utilization, and they can increase security of communication transmissions.

Below the main features are reviewed of the wave propagation at 60GHz [7].

The frequency and distance dependence of the loss between two isotropic antennas (**Free-Space Losses**) is expressed in absolute numbers by the following equation:

$$L_{FSL} = \left(\frac{4 \cdot \pi \cdot R}{\lambda} \right)^2 \qquad (1.1)$$

where R is the distance between transmit and receive antennas, and λ is the operating wavelength.
After converting to units of frequency and putting them in decibels form:

$$L_{FSL\,dB} = 92.4 + 20\log(f) + 20Log(d) \qquad (1.2)$$

where *f* is the frequency in GHz and R is the "*line of sight*" (LOS) range between antennas in kilometers.
Even for short distances, the free-space losses can be quite high. This suggests that, for applications in the millimeter-wave spectrum, only short-distance communications links will be supported.
In the millimeter-wave bands additional loss factors come into play, such as **gaseous losses** and **rain** in the transmission medium.
Transmission losses occur when millimeter waves traveling through the atmosphere are absorbed by molecules of oxygen, water vapor, and other gaseous atmospheric constituents. These losses are greater at certain frequencies, coinciding with the mechanical resonant frequencies of the gas molecules. Fig. 1.5 gives qualitative data on gaseous losses. It shows several peaks that occur due to absorption of the radio signal by water vapor (H_2O) and oxygen (O_2). At these frequencies, absorption results in high attenuation of the radio signal and, therefore, short propagation distance. For current technology, the important absorption peaks occur at 24 and 60 GHz. The spectral regions between the absorption peaks provide windows where propagation can more readily occur. The transmission windows are at about 35, 94, 140, and 220 GHz.
The high atmospheric absorption at 60GHz makes this band an excellent choice for establishing satellites communication systems, as the earth's atmosphere acts as a shield preventing any kind of interception from the earth.

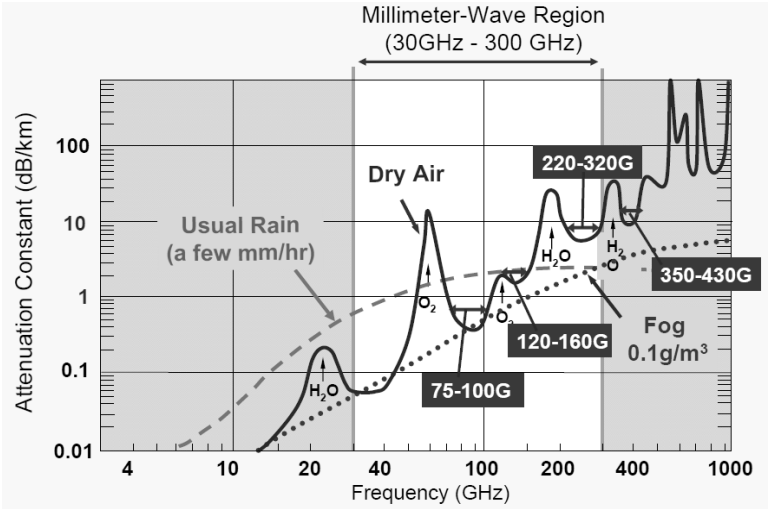

Figure 1.5:Atmospheric absorption of millimeter waves

Millimeter-wave propagation is also affected by rain. Raindrops are roughly the same size as the radio wavelengths and, therefore, cause scattering of the radio signal.
Fig. 1.6 shows the specific levels of attenuation caused by rain, depending on frequency and precipitation's levels: in very rainy days attenuation may even exceed 40-50dB/Km.
In areas of the world characterized by moderate rainfall, attenuation caused by rain is approximately twice that caused by the presence of oxygen (15dB/Km), while in regions where rainfall is more significant, the attenuation of signals due to refractive phenomenon is even three times higher than that due to atmospheric ones. So it is the rain, the primary factor limiting the maximum distance between receiver and transmitter at 60GHz.
Also foliage losses at millimeter-wave frequencies are significant. In fact, foliage loss may be a limiting propagation impairment in some cases. An empirical relationship has been developed (CCIR, Rpt 236-2), which can predict the loss. For the case where the foliage depth is less than 400m, the loss is given by:

$$L = 0.2 \cdot f^{0.3} \cdot R^{0.6} dB \qquad (1.3)$$

where f is the frequency in MHz, and R is the depth of foliage transversed in meters and applies for $R < 400$m.
For example, the foliage loss at 40GHz for penetration of 10m (which is about equivalent to a large tree or two in tandem) is about 19dB: this is clearly not a negligible value.

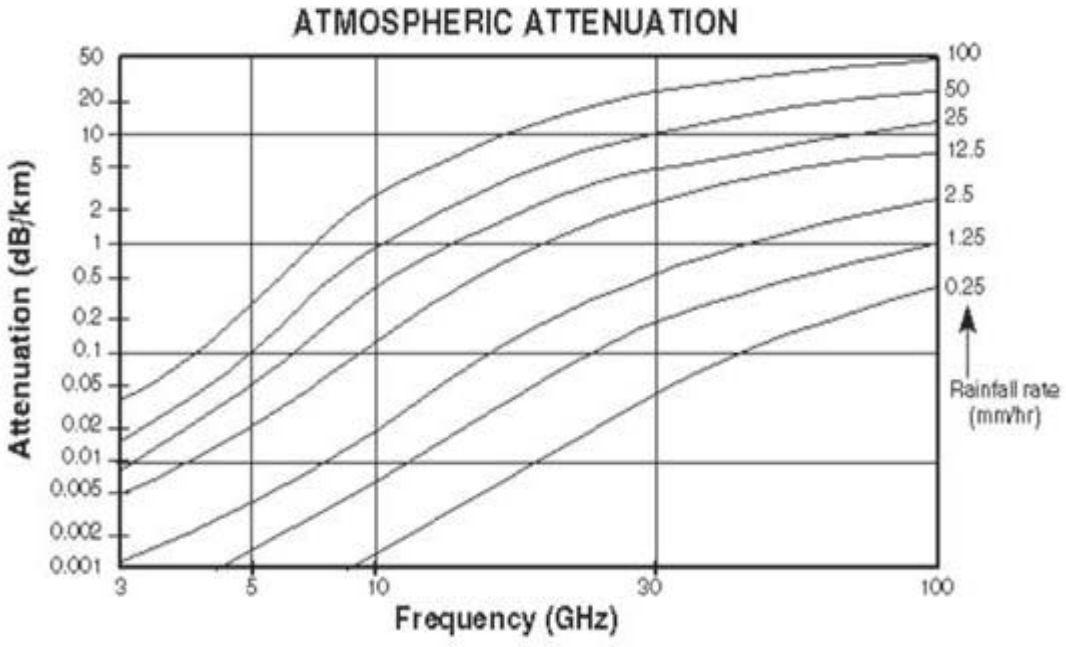

Figure1.6: attenuation due to rain

If there is no LOS path between the transmitter and the receiver, the signal may still reach the receiver via reflections from objects in proximity to the

receiver or via diffraction or bending. The short wavelengths of millimeter-wave signals result in low diffraction. Like light waves, the signals are subject more to shadowing and reflection. (shadowing makes it easier to shield against unwanted signals in communications systems.)
Normally, for non-LOS paths, the greatest contribution at the receiver is reflected power.
Reflections and the associated amount of signal diffusion are strongly dependent on the reflectivity of the reflecting material. Shorter wavelengths (higher frequencies) cause the reflecting material to appear relatively "rougher", which results in greater diffusion of the signal and less specular (i.e., direct) reflection. Diffusion provides less power at the receiver than specular reflected power.
In the past, all these aspects made transmission systems at 60GHz inadequate, but the criteria recently identified, including the need for short-distance transmission and high security, have meant that the new mm-W systems have become an ideal solution for emerging needs.
High absorption levels in the range of millimeter wave produce a sort of high spatial filtering effect; so, it becomes possible to reuse the same frequency in a limited region of airspace, and then have several radios operating in the same spectrum at short distances from each other (the minimum distance is 1-2 km), virtually eliminating the possibility that they interfere with each other.
Another important benefit of millimeter wave systems comes from the relationship between the wavelength of the signal and the size of antennas; to cope with the effects, sometimes unwanted, of atmospheric absorption radio links should use high gain antennas, so that it can transfer most of the signal transmitted to the receiving system: as frequency increase the wavelength of the signal becomes increasingly small, allowing relatively small size antennas to achieve the required gains.
For example, the size of an antenna required for a mm-W terminal which a gain of 40dB and a directivity of 1 ° is about one tenth of the size that should have an antenna operating at 6GHz with similar characteristics.
So at 60GHz, relatively small and low cost antennas offers high gains and well focused beams.

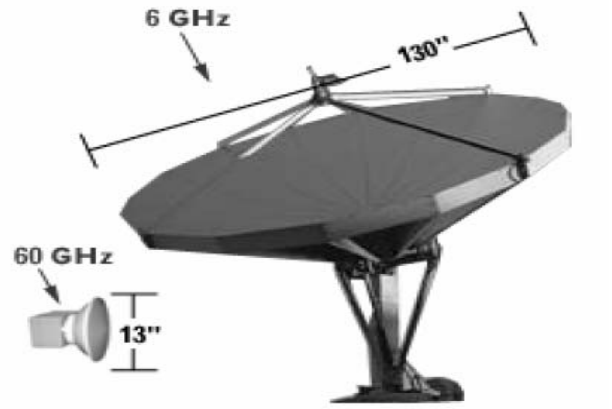

Figure 1.7: comparison between mm-W and microwave antennas sizes

Emissions from a mm-W system with high gain and directional antennas occupy a small portion of the surrounding airspace: therefore a signal transmitted to an antenna has minimal probability of interaction with a foreign receiver.
Similarly, an antenna with the same features will only receive the energy in the same direction in which it transmits, reducing the possibility of receiving an unwanted signal.

1.2.2 60GHz wireless communications: main applications

In summary, the main characteristics of mm-W communication systems are [4]:

• the high levels of power attenuation caused by the high rates of oxygen absorption and rain diffraction, resulting in an effect of "spatial filtering", which allows high levels of frequency reuse;

• the small size of antennas and radio frequency circuits;

• The high bandwidth availability which allows to obtain data rates never reached before.

These features make the millimeter wave band suitable for a variety of applications:

- **WLAN (home automation, offices, academic campus, etc..)**:

In the last decade, 802.11 based Wireless Local Area Networks (WLAN) technologies (also known as Wi-Fi) has enjoyed tremendous market adoption around the world, bringing the convenience of broadband wireless access to millions of users in the home, office and hot spots.
Within a short decade, the data rate of 802.11 family products have evolved at an amazing pace, from 1 Mb/s with the first generation of 802.11 products, to 11 Mb/s with 11 b, to 54 Mb/s with 11a/g, to up to 600 Mb/s with 11n MIMO products.
The next challenge going forward is to achieve multi-Gigabit data rates [8].
The abundance of bandwidth in the unlicensed 60 GHz band makes it feasible to achieve multi-Gigabit link throughput. Therefore, during the last years has been exploring possible solutions for the mm-W band as the next generation WLAN technologies.
Many different category of usage exist such as wireless displays, home distribution of video, rapid download and upload from and to a remote server, mesh or point-to-point backhaul traffic, campus or auditorium deployments and manufacturing floor automation.
Within each of the usage categories many detailed usage models were developed. These usage models cover a range of environments, including the home, office or enterprise, outdoor or hotspot, campus, and a factory floor.

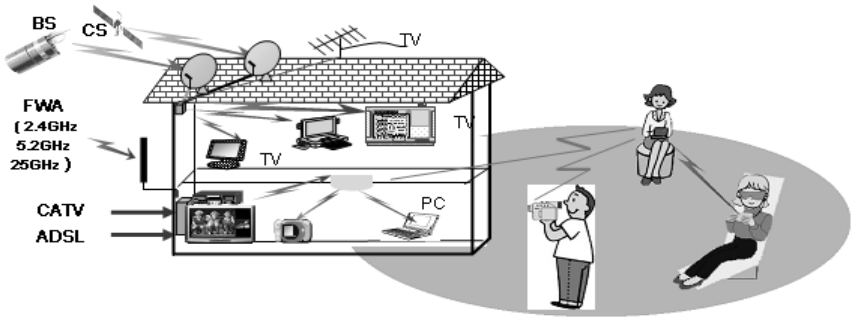

Figure 1. 8: 60GHz home automation

Home usages include short range and line-of-sight (LOS) (e.g. on a desk), medium range and mostly LOS (e.g. in a room), and long range and most likely non-line-of-sight (NLOS) (e.g. entire home). Similarly in the enterprise the coverage on a desk or in a cube would be short range and a conference room would be medium range. Dense enterprise deployments designed for higher capacity may be shorter range than the typical home environment.

Desktop display, TV, or projector requiring uncompressed video will require data rates exceeding 1 Gbps. For example, the data rate for uncompressed 1080p with 24 bits/pixel and 60 fps is 3 Gbps. Video distribution throughout the home will typically consist of lightly compressed video which is expected to be around 150 Mbps. Video streams may be distributed simultaneously around the home to different displays requiring the wireless network to be capable of much higher total throughput than anyone individual stream.

Usages like rapid sync-and-go or downloading movies or pictures from a camera require increasingly higher throughput as the quality and resolution increases. In the future with a 1 Gbps wireless link, copying a 30 GB video file will take 4 minutes and a few hundred picture files each 20 Mbytes in size will take one minute. For data networking applications such as file transfer or data backup, wireless technology must keep up with the continued increases in wired capability and most new computers today already come with Giga-bit Ethernet.

The biggest **challenge** for 60GHz is to cover the range for WLAN to which consumers have become accustomed. In some environments, such as construction with cement, it may not be possible to achieve typical WLAN coverage. However, in many WLAN environments, such as construction with drywall or fabric cubicle walls, the higher propagation loss of millimeter wave may be mitigated by high gain antennas, high transmit power, and a sensitive receiver.

Due to the small wavelength at 60 GHz, it is possible to fit many antenna elements on a small platform to create high gain antenna array. An antenna array with more than 20 elements achieving a gain more than 13 dBi is feasible. With an antenna array at both the transmitter and receiver would result in over 25 dB link budget gain.

Another key challenge that must be addressed in 60 GHz is link robustness. Due to high attenuation through obstructions, the link in 60 GHz is much more susceptible to breakage than another one at 2.4/5 GHz. In addition, the use of directional antenna makes a link very sensitive to moving object or

people, device mobility or just slight rotation. Hence, it is of paramount importance to design a MAC protocol that can deal with link breakages in an efficient manner.
A possible solution to this problem is to design a multipath MAC, wherein a joint PHY/MAC effort can be made so that the transmitter can keep more than one path to its intended receiver(s). This multipath feature is possible at mm-Wave frequencies as a result of the radio's beam-forming capabilities.
Another MAC challenge in 60 GHz is that it must support a high number of directions as compared to the number of associated devices.
The support of such high number of directions introduces significant challenges to the MAC, and possibly the most important of them all is the use of omni-directional transmissions for broadcast and multicast communication becomes extremely expensive given that the data rate must drop roughly proportional to the number of supported directions. Hence, the MAC design needs to minimize the use of low rate omni-directional transmissions and to fully exploit high-rate directional communication not only for data, but also for control and management functions.
The last key challenge is the support of an efficient contention-based random access mechanism.

- **Intelligent transort systems (ITS's)**

ITS's use information, transport, and communications technologies, in vehicles as well as within the infrastructure, to improve mobility while increasing transport safety, reducing traffic congestion, maximizing comfort, and reducing environmental impact.
In recent years, particular attention has been paid to wireless short-range systems for inter-vehicle and roadside to-vehicle communications (IVC and RVC, respectively), aiming at improving the safety and efficiency of traffic flow in different areas, such as urban environments and highways.
The role of the RVC network is that of supplying the user(the driver) with information related to weather forecasts, on a small and a large scale, parking availability, traffic conditions, etc. The IVC network, on the other hand, aims at allowing a direct exchange between vehicles of messages related to their position, speed, acceleration, and emergency situations (presence of fog, ice on the ground, accidents, etc.); hence, it could support the driver with local formation even in the absence of the fixed in infrastructure.
If a communication system able to allow both IVC and RVC is to be defined it is convenient to investigate a common standard protocol. In both cases, a packetized access to the medium is normally considered.
Different frequency ranges have been investigated or recommended for these systems, mainly the 5.8 GHz, 63.5 GHz, and infrared bands. Since IVC systems need short-range links to be exploited, due to the local significance of the information exchanged (position, speed, acceleration, presence of ice on the ground, etc.), the 63.5GHz band has some advantages with respect to 5.8 GHz.
In fact, also due to oxygen absorption in the 60–64 GHz frequency range GHz), a higher degree of spatial filtering can be obtained by using this bandwidth with respect to 5.8 GHz. On the other hand, unlike infrared

systems, by means of multipath propagation a communication link may exist at MMW even in non-line-of-sight (NLOS) conditions.
Moreover, the small size of antennas and RF circuits is of great interest since these components should be integrated (and hidden) in the structure of cars. For these reasons, the 63.5-GHz band is a strong candidate for the evolution of IVC and RVC systems for ITS applications. In both cases, by considering safety and/or congestion control, data rates are on the order of a few megabits per second.

- **Broad-band services distribution (ITS's)**

The use of mm-W band has recently been investigated also for the distribution of broad-band services to fixed user, such as in urban or sub-urban environments.
In fact, interactive video services (*IVS's*) and video on demand (*VoD*) are expected to became some of the most successful services in the emerging broad-band networks.

Other fields of application, less known but no less important are:

- **Fixed and mobile network nodes**

mm-W wireless technology can be used to meet the demands of the modern 3G, 2.5G and 802.11 telecommunications systems; in particular it can be incorporated to establish communications between the *Base Transceiver Station* (BTS) and *Base Station Controllers* (BSC).
For example, in Australia the band between 57.2 and 58.2GHz is already used and it allows to support data-rates even higher than hundreds of Mbit /s.

- **Optical fiber extension**

The Internet service providers can extend the communications network via fiber, making connections between their transmission unit and users close to them using the microwave technology: the wireless links are particularly attractive when connecting via fiber is not physically feasible or not feasible for cost reasons.

- **Temporary service restoring**

Radio reserves can provide a means for faster recovery of network service after adverse events such as the breaking of the fiber; the radio system can in fact be used as a temporary alternative for transmission via optical fiber, avoiding the service interruption while repairing the original link.

- **Reception problem solving**

Those who live in apartments in large buildings often fail to receive broadcasts via radio or satellite because of the presence of trees, buildings or other obstruction that blocks all or only part of the signal path.

To solve these problems in Japan, for example, has been created a system of reception / transmission called "*Vertically Connected Wireless Link*" (*VCWL*), based on millimeter wave technology; it consists of a transmitter placed on the building roof and directed downward, and a receiver mounted on the balcony, which receives signals in the band 59-66GHz and down-converts them into intermediate frequency signals, which are then sent to a de-modulator.

- **LAN bridges**

Using the band around 60Ghz it is possible to realize high-performance wireless links between LANs of different buildings placed, for example, in the same university campus or in the same hospital complex. These links offer:

- high bandwidth;
- excellent levels of data security;
- high availability.

- **Radio Local Area Network at 60GHz (RLANs)**

Today we are witnessing a strong increase in demand for bandwidth for RLANs applications in the 2.4GHz spectrum, which is expected to arrive soon to congestion: when it happens many systems RLANs will probably migrate to the band around 5GHz and subsequently to much higher frequencies.
This encouraged scientists worldwide to study new systems RLANs at frequencies in the millimeter wave band.

1.2.3 Feasible link performances

At 60 GHz there is much more free space loss than at 2 or 5 GHz since free space loss increases quadratically with frequency. In principle this higher free space loss can be compensated for by the use of antennas with more pattern directivity while maintaining small antenna dimensions.
When such antennas are used, however, antenna obstruction (e.g., by a human body) and mispointing may easily cause a substantial drop of received power, which may nullify the gain provided by the antennas. This effect is typical for millimeter waves because the diffraction of millimeter waves (i.e., the ability to bend around edges of obstacles) is weak. Regarding blocking effects, omni-directional antennas have an advantage in a reflective (e.g., indoor) environment since there they have the ability to still collect contributions of reflected power in the event of line of sight (LOS) obstruction.
Walls may considerably attenuate millimeter waves. The transmissivity strongly depends on material properties and thickness. At 60 GHz, transmissivity of glass may range from 3 to 7 dB, whereas attenuation through a 15 cm thick concrete wall can be as high as 36 dB. We may therefore expect concrete floors between stocks of a building to act as reliable

cell boundaries. This helps to create small indoor cells for hot spot communications. A typical/moderate inner wall consisting of multiple partitions of different materials (e.g., windows and doors), on the other hand, may be considered neither a reliable cell boundary nor a transparent medium. Due to the possible significant attenuation of inner walls, it will generally be necessary to have at least one access point per indoor environment (room, hall, corridor, etc.) to create a reliable shared medium.
A consequence of the confinement to smaller cells is that channel dispersion is smaller than values encountered at lower frequencies because echo paths are shorter on average. Rms delay spread may range from a few to 100 ns. It is expected to be highest if omnidirectional antennas are used in large reflective indoor environments. When, instead, high gain antennas are used, rms delay spread may be limited to a few nanoseconds only.
Movements of the portable station as well as movements of objects in the environment cause Doppler effects as frequency shift and spectrum broadening of the received signal. These Doppler effects are relatively severe at 60 GHz because they are proportional with frequency. If persons move at a speed of 1.5 m/s (walking speed), the Doppler spread that results at 60 GHz is 1200 Hz.
In order to allow flexible terminal use, the low position of the access point (antenna) necessitates measures to cope with the drop in received power due to LOS obstruction by a person or object. One measure is to apply macro diversity by switching to another access point as soon as the received signal drops below a certain threshold. However, this requires the use of more than one access point per room, which may increase the costs significantly, particularly when many small rooms have to be covered. A more attractive solution may be found in another direction, namely that of applying particular antenna patterns that may be adaptive to some extent (e.g., by applying beam switching). Lower medium-gain antennas may be preferred to high-gain antennas in order to avoid stringent antenna pointing and tracking requirements.

1.2.4 Dual-band operation: 5-60GHz

An additional measure against coverage limitations due to wall attenuation, but also against severe shadowing, is to operate the 60 GHz system in combination with a system that works at a much lower frequency. An obvious option to combine with is the 5 GHz WLAN system. As a matter of fact, this should be done in any case to achieve interoperability with the legacy 5 GHz WLAN [9].
In this multimode scenario the system always tries first to reach users at 60 GHz. Under nominal propagation conditions the user can exploit the resources of the 60 GHz system. As soon as the channel conditions worsen, say, as a result of (severe) shadowing or when the user walks in an area not covered by the 60 GHz system, the connection switches to the 5 GHz band. In this way the 5 GHz band serves as a fallback option and umbrella cell for 60 GHz cells.

The radio frequency (RF) select can be based on channel conditions, channel availability, user preferences, and connection parameters. Note preferences, and connection parameters. Note that the WLAN RF of 5 GHz is also utilized as intermediate frequency (IF) for the 60 GHz system. In order to minimize complexity of the baseband, functions are as much as possible the same for both systems. For instance, the 60 GHz system may utilize (multiples of) 64-subcarrier units.

1.3 Receiver architecture choice

1.3.1 Alternative receiver architectures for 60GHz wireless transmissions

Cost efficient RF solutions for high data rate transmission at 60 GHz still have to be determined. In this respect, some important choices have to be made which might by crucial for commercial success:

• choice of the 60 GH radio front-end architecture,

• choice of technology in which the radio front-end

should be implemented: GaAs, InP, Si, or SiGe.

With respect to the choice of the architecture of the60 GHz front-end radio there are, in principle, three options [10]:

• employing sub-sampling,

• employing direct conversion (i.e., “zero RF”),

• employing superheterodyning.

Employing analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC) directly at the antennas would make the complete RF and IF part obsolete. However, this option can be ruled out immediately because this would require ADC and DAC devices having 60 GHz bandwidth. Low-cost implementation of this in the medium term will be unfeasible. Apart from this approach, the sub-sampling receiver represents the “ultimate” solution for simple low power down conversion, which essentially consists of a sampling switch, clocked at a much lower frequency, and an A/D converter. The limitations of the sub-sampling approach, however, demonstrate some of the inherent problems in low power receiver implementations. In a sub-sampling receiver, image frequencies exist at integral multiples of the sampling rate and can alias into the band of interest. As a result, careful filtering prior to down-conversion is required. For example, down-conversion of an RF signal having a bandwidth of 500 MHz, would require a sample rate of at least 1 GHz, assuming a “*brick wall filter*”. In practice, the sample rate

will have to be much higher –at least 2 GHz- in order to minimize the finite bandwidth effects of the filter. It is questionable whether 2 GHz A/D conversion, with let-us-say 10 bit quantization, will become feasible in the medium term. This might be examined, in addition to the problem that the resulting signal-to-noise ratio of the down-sampled signal will inevitably be poorer than that of an equivalent system employing a mixer for down-conversion, due to the noise aliased from the bands between DC and the pass-band .

The main advantages of **direct conversion** are that it is uniquely well suited to monolithic integration, due to the lack of image filtering, and its intrinsically simple architecture. FSK modulated signals are especially well-suited to direct conversion, due to their low-signal energy at DC. However, the direct conversion receiver has not gained widespread acceptance to date, especially in high performance wireless transceivers, due to its intrinsic sensitivity to DC offset problems, even harmonics of the input signal, and problems related to the local oscillator such as LO I/Q generation, LO frequency division and LO distribution.
The generation of I and Q phases of the LO at 60 GHz entails two issues [11]: (a) quadrature operation typically degrades the phase noise considerably (because *two* core oscillators consume power, they must operate away from resonance frequency of the tanks, and they do not improve each other's phase noise) and (b) the comparatively low tank Q results in serious design tradeoffs.
LO frequency division, also proves problematic in this architecture: injection-locked and Miller dividers typically suffer from a narrow lock range if designed for 60 GHz.
LO distribution problems mean that the quadrature outputs of the VCO must travel a different distance to reach the I/Q mixer cores and the divider cores, thus experiencing significant loss and mismatch.
In fact, with no buffer following the VCO, the loss of these interconnects also degrades the phase noise.
One may wonder if these interconnects can be realized as low-loss T-lines having a controlled impedance and terminated properly at the destination. Since the characteristic impedance of on-chip T-lines hardly exceeds a few hundred ohms, such an approach would *load* the VCO with a low resistive component, drastically raising the noise floor or even prohibiting oscillation.
A buffer must therefore follow the VCO in this case. The use of a VCO buffer is also required by another effect: in a direct-conversion receiver, strong in-band interferers can leak from the RF to the LO port of the down-conversion mixers, thus injection-pulling the f_{LO} in the absence of a buffer.
DC offsets can be reduced using good design practices, but they cannot be eliminated completely, especially if *quadrature phase shift keying*(QPSK) or *gaussian minimum shift keying* is used since the spectra of these schemes exhibit a peak at DC. But when Orthogonal Frequency Division Multiplex (OFDM) is applied there may be a solution and that is to avoid the use of those subcarriers that, after conversion, correspond with, or will be close to, the DC component. This is just an example of a possible solution but there

might also be other solutions that exploit the particularities of the 60 GHz physical layer.

The last receiving architecture that we consider is s**uperheterodyne**, an example of which is shown in Fig. 1.9 (this is in fact a sliding IF architecture).
The receiver mixes the input with a nominal LO frequency of 40 GHz, generating an intermediate frequency (IF) of 20 GHz. The IF signal is then separated to quadrature phases and mixed with to produce the baseband outputs.

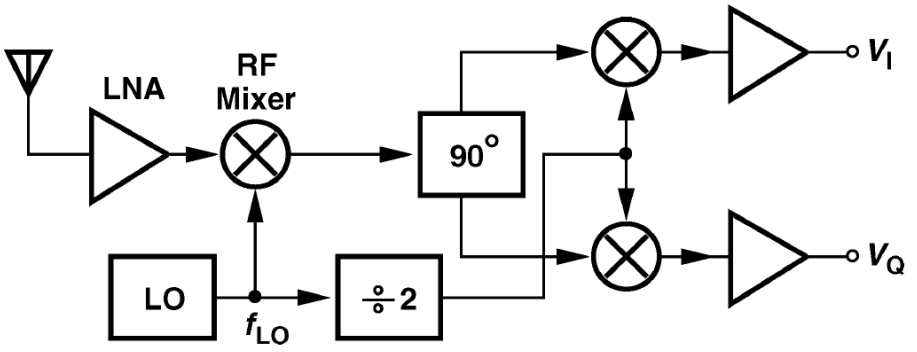

Figure 1.9: simple 60GHz RF superheterodyne architecture

The heterodyne architecture in Fig. 1.9 greatly simplifies the three LO-related tasks mentioned before: 1) generation occurs at 40 GHz with no need for quadrature phases; 2) frequency division also occurs at 40 GHz, permitting a broadband design; and 3) distribution of the differential 40GHz LO is much simpler than that of quadrature 60-GHz components. Note that no LO buffer is necessary as interferers in the vicinity of 55 GHz are suppressed by the selectivity of the front-end (including the antenna).

1.3.2 Antennas at 60GHz

Antennas

60 GHz antennas should feature the following properties [10]:

• low fabrication cost, readily amenable to mass production,
• light weight, low volume,
• high efficiency which implies low-loss feed,
• easy to integrate with MMIC RF front-end circuitry,
• covering the 59 – 66 GHz frequency band,
• eventually, circular polarization.

The requirements of low cost, low weight and low volume rule out many antenna structures: Obviously, the classical microwave aperture antennas of the type "*heavy metal*" are unsuitable. Also lens antennas cannot be used

because a lens is typically an expensive part and is not readily amenable to mass production. The well-known whip antenna with coaxial feed may be considered as too lossy and too expensive, in case it is applied at 60 GHz. A relatively new development is the application of *micro-electromechanical systems* (MEMS) in antenna structures, i.e., the use of small (chip-level) electromechanical parts that can be actuated by supplying a certain actuator voltage. Such antenna structures have the potential to become cheap and small. The current state-of-the-art is, however, that MEMS antennas cannot be used for our purposes, because of the high (25-100 volts) actuator voltage that is required to establish a significant movement. A related problem is that very thin hinges are required to achieve some flexibility of the moving part, which gives rise to ageing. Nevertheless, for the longer term when these problems are solved, MEMS may become of significance. In this respect, it should be noted that MEMS may also become significant for voltage controlled phase shifters to steer adaptive arrays.
For the shorter term, the only viable solution that remains is the use of **microstrip antennas**. Microstrip patch antennas feature all of the properties listed in the aforementioned list of required properties. Linear polarizations are possible with a straight forward feed structure. Patch antennas can also have circular polarization.
The application of circular polarization is considered because there are strong indications that channel delay spread is substantially lower in case circular polarization is used instead of linear polarization. Feed lines and matching networks can be fabricated simultaneously with the antenna structure. Finally, dual-frequency and dual-polarization antennas can be easily made. However, in general it can be said that microstrip antennas also have some limitations:

a) most microstrip antennas radiate into half-space,
b) low power handling capability (~100 W),
c) narrow bandwidth and associated tolerance problems,
d) radiation from feeds and junctions.

For our application, a) has little significance; An access point antenna should have high gain, whereas a portable station antenna should radiate in horizontal direction or slightly upwards, but not downwards. Limitation b) is of no significance at all because radiated power will never exceed 100 mW or so. The other limitations can be circumvented by taking suitable choices for, in particular, the dielectric constant ε_r and the thickness of the substrate. For 60 GHz, a substrate thickness of 100 μm is quite acceptable which is the typical thickness of GaAs and SiGe chip substrate. ε_r for GaAs and SiGe is about12 which yield a bandwidth of 2% and a radiation efficiency of 80%. Hence, a 60 GHz patch antenna integrated with the 60 GHz RF front-end might be a good option.
These antennas are often combined in electronically driven arrays, very beneficial as they can, from low directivity elements, imitate a directional antenna whose bearing can be controlled electronically. This electronic steering makes it possible to emulate antenna properties such as gain and directionality, while eliminating the need for continuous mechanical reorientation of the actual antennas (Fig. 1.10). Additionally, the parallel

nature of a phased array antenna transceiver alleviates the power handling and noise requirements for individual active devices used in the array. This makes the system more robust to the failure of individual components.

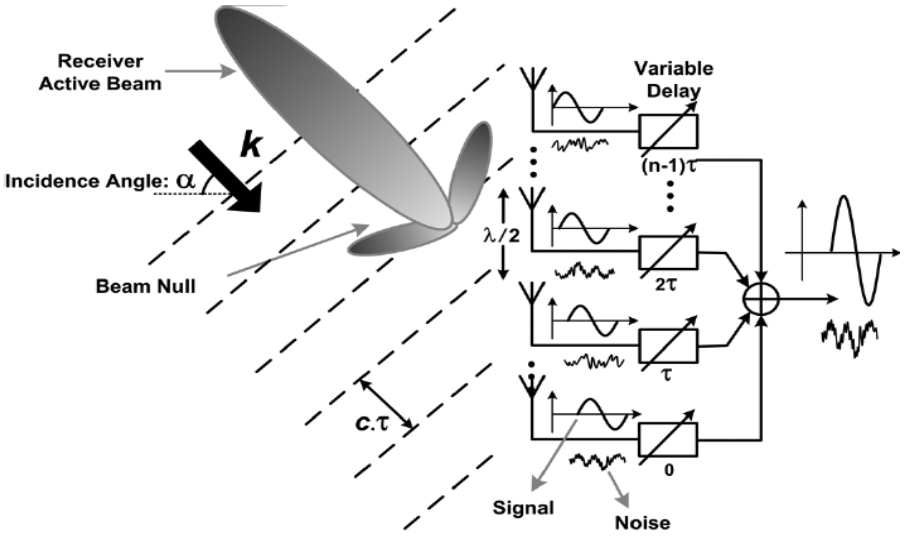

Figure 1.10: phased array receiver

In the past, such systems have been implemented using a large number of microwave modules, adding to their cost and manufacturing complexity.
A phased array transmitter or receiver consists of several signal paths each connected to a separate antenna [12]. The antenna elements of the array can be arranged in different spatial configurations; the array can be formed in one, two, or even three dimensions, with one- or two-dimensional arrays being more common.
The principle of operation of a phased array is similar for a receiver or a transmitter. In a phased array receiver, the radiated signal arrives at different times at each of the spatially separated antennas. The difference in the time of arrival of the signal at different antennas depends upon the angle of incidence and the spacing between the antennas. An ideal phased array receiver compensates for the time delay difference between the signals from different antennas and combines the signals coherently to enhance the reception from the desired direction(s), while rejecting emissions from other directions. Similarly, in a phased array transmitter, the signals in different elements are delayed by different amounts so that the signals add up coherently only in the desired direction(s). Incoherent addition of the signal in other directions results in lower radiated power in those directions.
Thus, in a phased array based system, the transmitter generates less interference at receivers that are not targeted, and the receiver is also capable of nulling out interferers as long as they do not originate from the same direction as the signal. Additionally, for a given power level at the receiver, the power that has to be generated is lower in a phased array transmitter than in an isotropic transmitter. In a transmitter with *m* elements, if each element radiates *P* watts, the total power that will be seen at the receiver in the desired direction is *P* watts. The m^2 improvement comes from the coherent addition of

the electromagnetic fields in the desired direction. For example, in the case of four-element transmitter, the total power radiated in the beam direction is 12 dB higher than the power radiated by each element.

1.4 Front-end technology

1.4.1 Why Silicon?

There are strong reasons not to consider silicon technologies for mm-wave applications [14].
Silicon comes up short in many comparisons to III-V semiconductors. Silicon carrier mobility is relatively low and so device-level FOMs of raw performance appear to be inferior. The silicon band-gap is relatively small and so voltage tolerance tends to be lower. Furthermore, highly-resistive or semi-insulating silicon substrates are difficult to achieve resulting in poorer isolation and higher losses in interconnects and passive devices. Each of these presents serious challenges to implementing mm-wave functions.
However, advances in silicon technology driven by high-performance digital applications, offer advantages to the mm-wave designer that might not be apparent on first consideration. Performance, quantified by f_T , f_{max} or NF_{min} for example, has dramatically increased with geometry scaling and technology enhancements in both CMOS and SiGe HBTs. Both CMOS and BiCMOS technologies have been used to demonstrate circuit functioning at frequencies in and above the K- band.
Until the early 2000's, the majority of mmWave research and product development had used III_V **Gallium Arsenide** (GaAs) based technology which is known to have the following merits [10]:

- high f_T and f_{max},
- low noise factor (<4dBm),
- higher breakdown voltages,
- excellent power added efficiency (< 60%),
- good linearity.

On the other hand, III-V compound semiconductors are characterized by relatively low integration levels and by module cost and size prohibitive for consumer mass market adoption.

Silicon *Heterojunction Bipolar transistors* (H**BTs**) feature many advantages compared to CMOS devices such as their lower *1/f* noise, the higher output resistance, the higher voltage capability for the same speed, and finally the reduced sensitivity of f_{max} to layout parasitics.
It is generally acknowledged that bipolar MMIC design is relatively easier and has better chance for a first-pass silicon success than CMOS design. One of the main reasons is that the bipolar model is simpler and better behaved; the layout effects of wiring parasitic, substrate contacts and proximity effects to adjacent devices have much less impact to the device performance in

bipolar than in CMOS. In CMOS, FET cell layout optimization and the accurate extraction of layout parasitic effects plays a big role in achieving good performance as well as model to hardware correlation.
The range of technologies on the market today offers HBTs featuring f_T ≥200GHz and f_{max} sometimes ≥300GHz (using self-aligned architectures).

CMOS technologies and their ability to follow Moore's low are the root of success of Si technologies. Continuous scaling, leading to always-increasing functional integration, is the driving force behind digital CMOS.
RF-CMOS, too, benefits from the gate down scaling with the improvement of main figures of merit that are f_T, f_{max} and NF_{min}: f_T as high as 150GHz are reached in the 65nm node.

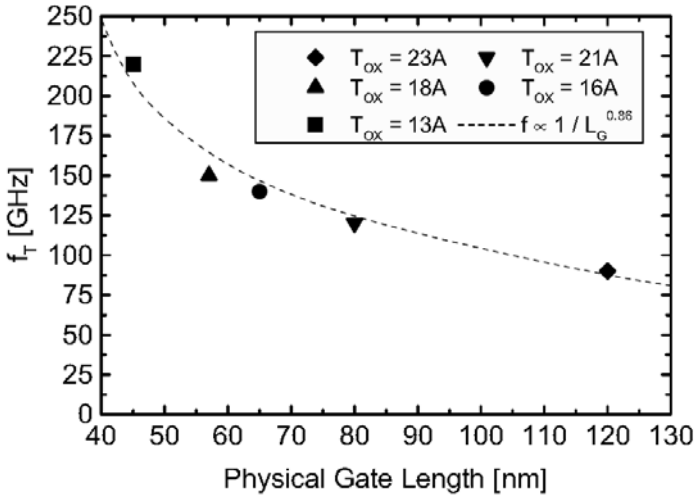

Figure 1.11

Equation 1.4 presents one way of calculating the transition frequency f_T for deep submicron technologies:

$$f_T \approx \frac{g_m}{2 \cdot \pi \cdot C_{gin} \cdot \sqrt{1 + 2\frac{C_{Miller}}{C_{gin}}}} \tag{1.4}$$

with g_m, the gate transconductance, and:

$$\begin{aligned} C_{gin} &= C_{gsi} + C_{overlap} + C_{fringing} \\ C_{Miller} &= C_{gdi} + C_{overlap} + C_{fringing} \end{aligned} \tag{1.5}$$

where:

- Cgsi, C_{dsi} are the equivalent capacitance induced by the source/drain field effect into the channel;

- $C_{overlap}$ is the equivalent capacitance given by the L_{DD} (low doped drain/source regions) diffusions under the gate.
- $C_{fringing}$ is the parasitic capacitance depending on the gate height and on the contact to gate distance.

As can be seen, f_T increases for reduced gate length devices thanks to higher transistor transconduttance; concerning the capacitive part, f_T is degraded by a high gate to drain capacitance.
From a theoretical point of view, the g_m is increasing with the reduction of the effective gate length. Nevertheless, for advanced deep submicron technologies this trend is not straightforward; the features limiting this evolutionary trend are the reduced gate oxide thickness which induces gate tunneling currents, the mobility degradation due to active zone doping increase and the source/drain equivalent series resistance increase given by low doped drain regions (L_{DD}).
Several process techniques have been developed in order to cope with this gm increase limitations; the hole mobility in PMOS transistors is increased by using 45° rotated devices and for the electron mobility in NMOS tensile liner films are used. In order to limit gate leakage and to further decrease the effective electrical gate length, high-K dielectrics are often used as a part of the gate material.

High f_{max} value have also been reported for CMOS devices, such as 200GHz on the 65nm node.
The f_{max} of CMOS devices, which should correlate to the performance of large signal operation blocks such as mixers, oscillators and power amplifiers, is very sensitive to layout parasitic and also to the choice of the transistor's finger width. It can be shown theoretically that f_{max} is independent of the number of fingers of a multi-finger MOS [13]; therefore, it is sufficient to only consider the optimal layout for a single finger.
This parameter is limited by resistive losses, the most significant being the gate resistance (R_G), series source/drain resistances (R_D,R_S), non quasi-static channel resistance (r_{nqs}), and resistive substrate network (R_{sb}, R_{db}, and R_{bb}).
By using narrow finger widths, the effect of the gate resistance can be made negligible compared to the other parasitic resistors. The polysilicon gate sheet resistance only affects how narrow the fingers must be made; therefore, with optimal layout, f_{max} is not limited by the gate resistance, but is primarily determined by the series source/drain resistances and substrate losses.

The noise parameter NF_{min} is also an important marker for the RF and mm-wave performances of an active device. The very low noise figure values, presented by deep submicron CMOS devices nowadays, are very difficult to measure with an excellent accuracy, as the de-embedding is very complex in the high frequency range.
For the MOS transistor, the following formula can be used to calculate the *NFmin* parameter :

$$NF_{\min} \approx 1 + \frac{f}{f_T}\sqrt{g_m \cdot \left(R_g + R_s\right)} \tag{1.6}$$

As it can be easily recognized, this parameter is strongly degraded by high gate and source parasitic resistances, thus being layout dependent.

Realizing a comparison between state of the art contemporary 130nm node SiGe:C HBT and 65nm node NMOS devices and using dimensions for the two devices which are suited geometries for mm-wave design, it may be admitted that both the bipolar and the NMOS device exhibit rather similar noise performances: the extrapolated minimum noise figure at 80GHz is around 2.3dB for both devices. Peak f_T *and* f_{max} are respectively 150GHz and 300GHz for MOS device while 200GHz and 250GHz for the bipolar one.
The MOS device has its peak f_T value of about 150GHz at a drain current density per unit width of 0.3mA/μm, while the equivalent value for the bipolar device is reached at a collector current density per emitter length of 1.9mA/μm.

1.4.2 Transistor modeling

Transistors and passives modeling at 60GHz is very complex. Firstly, models are extracted from very sensitive high frequency S-parameter measurement that suffer also from the de-embedding techniques that are not much optimized for these frequencies [14].
Moreover, intrinsic device effects negligible at lower frequencies must now be considered: the substrate effects have became very significant and have pronounced impact on the device performances; also effect such as short channel, tunneling leakage, STI (shallow trench isolation) stress induced and well proximity effects must be captured by the model [15].
The last reason for the 60GHz modeling complexity is due to the important role of the device layout, and this is more difficult to address. The device interconnections to the outside world introduce small inductors, resistors and capacitors to the model and dominate the performances of the device as the frequency increase.
In transistors interconnect a key role is played by the layout-related C_{GD} feedback capacitance, as we shall see in Chapter 3.
This makes it crucial to include these parasitic into the model. Each small finger of the device can be modeled with an " intrinsic" transistor model based on the quasi-static-equations whereas the interconnections between the fingers are captured by electromagnetic simulations and experimental techniques.
Since the precise layout details (connections to the gate, drain, source, and bulk, locations of the substrate contacts, etc..) have a major impact on the performances, models should be extracted only for fixed layouts and the transistors used in the circuit should be exactly the same previously characterized and modeled.
A test chip with a collection of different size PMOS and NMOS devices has been integrated in the 65nm CMOS technology from TSMC. The S-parameter of each device has been extracted using a 3-step de-embedding technique [16] (which will be discussed in the subsequent chapters) and has been compared to the BSIM model and a "custom" 60GHz model.

As an example, let's focus on a NMOS device with L_f=65nm, W_f=1μm and 30 total fingers. Fig. 1.12(a) shows the BSIM model of the transistor: the layout parasitic capacitors and inductors extracted using EM Agilent Momentum simulations and the gate resistance R_g, due to non-quasi-static effects are included. The model includes also other some elements (the capacitors $C_{gs'}$ $C_{ds'}$, the drain inductance $L_{d'}$ and the resistance $R_{ds'}$, in red) added to obtain a best fitting of the measurement; these parasitic elements are closely tied to the de-embedding structures used to extract the DUT S-parameters from the raw measurements data and are not easily predictable. From now we'll refer to this model as "ESBSIM"

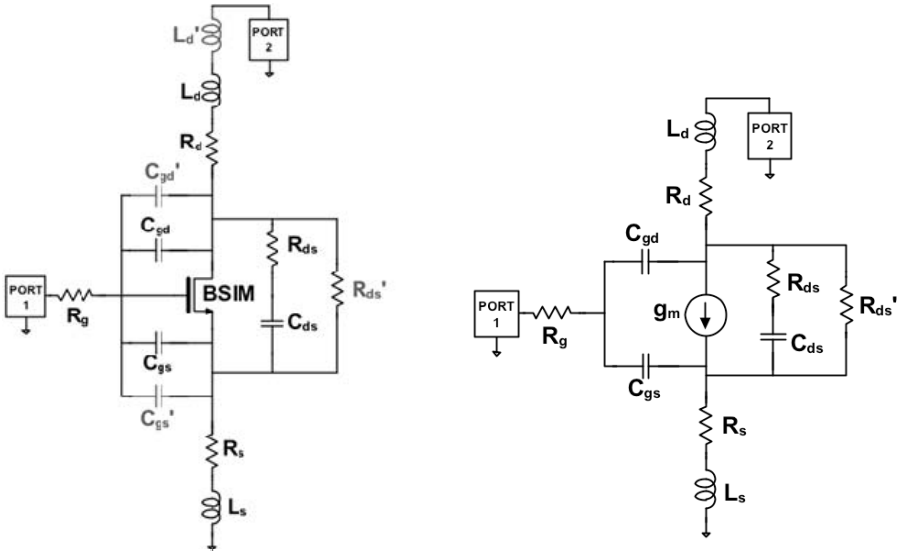

Figure 1.12: MOS "ESBSIM" model and AC model

A MOS AC model (Fig. 1.20-b) has been also realized by fitting the capacitances and inductances values through S-parameters measurements.
The values used in the two models for 1.2V bias voltage are reported in Tables 1.4 and 1.5.

	C_{gs} [fF]	$C_{gs'}$ [fF]	C_{gd} [fF]	$C_{gd'}$ [fF]	C_{ds}[fF]	L_s [pH]	L_d [pH]	$L_{d'}$ [pH]
ESBIM model	3,4	6	2,6	2	9	7,9	1,3	3
AC model	31	-	12	-	15	7,9	4,3	-

Table 1.4: MOS "ESBSIM" and AC models values

	R_g [Ω]	R_s [Ω]	R_{ds} [Ω]	$R_{ds'}$ [Ω]	R_d [Ω]	g_m [mS]
ESBIM model	6	2,2	4,1	1.66K	3	-
AC model	6	2,2	160	220	3	30,4

Table 1.5: MOS "ESBSIM" and AC models values

The comparison between the measured and de-embedded device S-parameter and those extracted from our models shows a good fitting, regarding S_{12}, S_{21} and the imaginary parts of Y_{11} ,Y_{22},Y_{12} ,Y_{21}. There are instead some discrepancies (that increase with frequency) in the real parts of Y_{22} and Y_{21}. This discrepancy is probably related to errors due to the chosen de-embedding technique. After all, this is the best result between those using other high frequency techniques for de-embedding proposed in literature.
The device shows a measured f_{max} of about 150GHz, a power gain G_P of about 10dB at 40GHz and an available gain G_A of about 7dB at the same frequency.

Conclusions

Millemeter-wave wireless communications allow high data rates (up to 2Gbps), higher integration levels, strong levels of frequency reuse and enhanced safety due to the strong amount of atmosphere's absorption at these frequencies.
The main application field of 60GHz wireless transmissions is nowadays represented by high speed WLAN, but they can also be used for intelligent transportation systems (ITS's), for broadband distribution services (LMDS's) for RLANs, for radars and many other applications.
A design approach based on different levels is of primary importance at 60GHz: device, building blocks, circuital topology and transceiver architecture have to be studied in parallel by the designer.
Moreover, in order to fully account for the behavior of active and passive devices up to 60GHz is necessary to carefully design, model and characterize these devices (mos, varactors, inductors, capacitors and transmission lines); a careful optimization of the layout is of primary importance to achieve good performances and represents, also from the standpoint of time required, perhaps the largest part of the project.
Despite all these aspects make the design of a 60GHz front end, particularly in CMOS technology, time-consuming and complicated, the high speed performance that today's CMOS technologies, such as 65nm CMOS from TSMC, are able to offer, are opening the door to their use for 60GHz front-end mass production .

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_____Chapter II_____

Design and characterization of millimeter wave voltage controlled oscillators

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2.1 Considerations on VCOs
High frequency VCO fundamentals – VCO Spec-sheet – Phase noise theory – Classes of VCOs for 60GHz applications– Millimeter wave VCO design challenges – Lumped LC tank VCO vs Standing wave oscillators.
2.2 Lumped LC Digitally controlled oscillator
Why digital control? – Noise sources in a ADPLL – Tuning Banks design – Oscillator core design – Phase Noise prediction – Experimental results
2.3 Standing wave voltage controlled oscillator
Transmission line resonator – Standing-wave oscillator design – Experimental results.

Conclusions

Even though Si technologies have enabled the implementation of VCO running at frequencies above 100GHz, the design of high performances oscillators operating in the mm-wave range continue to pose difficult challenges even today. These challenges mainly come from the poor quality factor of passives, in particular of variable capacitance, which dominates the resonator Q and from the high operative frequency, close to the transistor intrinsic frequency f_T and f_{max}, which limits the transistor available power gain.
Various approaches of LC tuned VCO have been studied and implemented for 60GHz applications; among them the most common are push-push, Colpitts and cross-coupled oscillators.
The most pervasive ones are LC-tank cross-coupled VCOs; the simple yet symmetric configuration facilitates high-speed and differential designs with large swings, reasonable tuning range, and lower consumption.
At 60GHz, the electrical wavelength λ is approximately 2.5mm, and transmission lines offer an alternative to inductors for the realization of passive elements: this is why at 60GHz the classical lumped LC tank can be replaced by properly designed transmission lines.

Although spiral inductors seem to be the preferred choice based on quality factor, variation of inductance over process, self-resonant frequency and chip area, there are several advantages of the shorted stub that are not captured by these electrical parameters.
Both solutions for 60GHz VCOs remain viable alternatives, with different advantages and drawbacks, as will be shown in the following discussion.
In the second section of this chapter a 53GHz low phase noise digitally-controlled lumped LC oscillator is presented. The oscillator was designed in the 90nm TSMC CMOS process, without advanced analog features and adopts a fully-digital control technique, making it compatible with all-digital frequency synthesis.
In the last section a standing-wave voltage-controlled oscillator (SWO), based on a shielded quarter-wave transmission line that operates in the band 71-73GHz is presented.
Some final considerations end this chapter.

2.1 Considerations on VCOs

2.1.1 High frequency VCO fundamentals

Oscillation behavior can be explained in different ways. A well-known model is shown in *Fig.2.1*, where an amplifier A(s) is placed in a feedback system. The overall transfer function is given by [1]:

$$H(s) = \frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1 + A(s)} \tag{2.1}$$

To make it oscillate at certain frequency ω_{osc}, we must satisfy the *Barkhausen criteria*:

$$\begin{aligned} &\left|A(j\omega_{osc})\right| = 1 \\ &\angle A(j\omega_{osc}) = 180° \end{aligned} \tag{2.2}$$

which governs all kinds of oscillators. These conditions are actually self-proven: a "stable condition" exactly implies "unity gain loop" and "total phase shift of 0°". Physically, oscillation initiates from white noise, an initial condition (charge on a capacitor), or a "kick", an input waveform with sufficient spectral content to excite the right half plane poles of the system. A loop gain greater than unity is set in actual designs (about 3) so as to start up the oscillation. While the energy at other frequencies decays eventually, the component at ω_{osc} survives and grows up until the effective loop gain drops to unity.
In most cases, an oscillator could became useful only if its frequency is tunable. The tuning range must be large enough to cover the overall bandwidth of interest with sufficient margin for process, temperature and supply variations.
Compared to wireless LAN systems at 2.4 or 5.2 GHz, the 60GHz indoor RF band for example, has 7-GHz unlicensed band available. The VCO must

accommodate as wide as 15% of the centre frequency, across which no serious deviation is allowed.

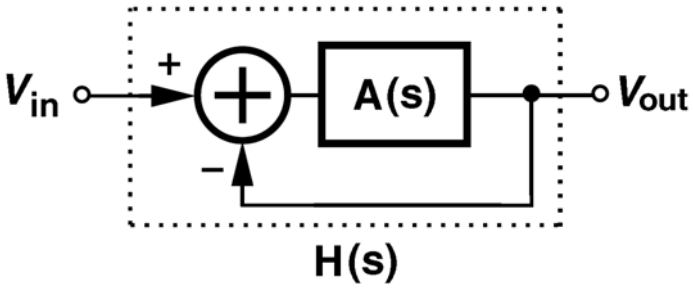

Figure 2.1: feedback system

2.1.2 VCO Spec-sheet

A part from a controllable frequency, the specification sheet of a VCO typically has the following entries [2]:

Center frequency: is the output frequency f_0 of the VCO with its control voltage at its center value.

Tuning range: is the range of output frequencies that the VCO oscillates at over the full range of the control voltage.

$$TR(\%) = 100 \cdot 2 \cdot \frac{f_{\max} - f_{\min}}{f_{\max} + f_{\min}} \qquad (2.3)$$

Tuning sensitivity: is the change in output frequency per unit chance in the control voltage, typically expressed in Hz/V (K_{VCO}). VCOs intended for frequency synthesis applications can have a nonlinear relationship between control voltage and oscillation frequency so that several values are quoted or min/max boundaries are given; non-linear characteristics cause a distortion of the received signal, if the oscillator is used in the receiver or frequency modulation if it is used in a transmitter. Also, in a PLL, the VCO gain must be kept as constant as possible, otherwise the loop phase margin suffers. Moreover, in a typical differential LC tank VCO and high K_{VCO} causes a strong *AM* to *PM* conversion and consequently flicker noise of the tail current appears as a relevant part of the phase noise [1].

Power consumption : specifies the DC power drain by the oscillator and its output buffer circuits.

Output Power: is the power the oscillator can deliver to a specified load. The variations of the output power over the tuning range is also specified.

Spectral purity: can be specified depending on the application, in the time domain in terms of jitter or in the frequency domain in terms of *phase noise*

or carrier/noise ratio. Noise sources- thermal, 1/f, supply or substrate interferences- cause changes in the amplitude and frequency of oscillation so that the output spectrum of the oscillator is not a pure tone but has noise sidebands; in the time domain this means that there is an amplitude variations and that the zero-crossing of the output waveform are not perfectly equally spaced in time, but they exhibit random variations around a nominal value which are referred to as jitter.
Phase noise represents a key performance measure of a VCO together with its power consumption.
A popular figure of merit (F.O.M) for oscillators summarizes these two important performance parameters, to make a fair comparison:

$$F.O.M = -L(\Delta\omega) + 20\log\left(\frac{\Delta\omega}{\omega_0}\right)^2 + 10\log\left(\frac{P_{DISS}}{1mW}\right) \qquad (2.4)$$

The second term is to neutralize the effect of offset in $L(\Delta\omega)$ while taking the centre frequency into account. The power consumption is calculated as dBm such that the unit of FOM remain the same as that of $L(\Delta\omega)$.

2.1.3 Phase noise theory

The phase noise has been the subject of numerous studies, many models have been developed for different types of oscillators, each based on assumptions rather restrictive and therefore applicable only to
a limited class of devices.
Most of these models consider the oscillator as a linear *time invariant* system (LTI) and analyzes the complete mechanism by which the noise from various sources translates into phase noise [3], [4]. In reality, any oscillator is a periodically time-varying system and its time-varying nature must be taken into account to permit accurate modeling of phase noise capable of proper assessment of the effects on phase noise of both stationary and even of cyclostationary noise sources [5].
The output of an ideal sinusoid oscillator may be expressed as:

$$V_{out}(t) = A\cos[\omega_0 \cdot t + \Phi] \qquad (2.5)$$

where A is the amplitude, ω_0 is the frequency, end Φ is an arbitrary, fixed phase reference.
Therefore, the spectrum of an ideal oscillator with no random fluctuations is a pair of impulses at $\pm\omega_0$.
In a practical oscillator, however, the output is more generally given by:

$$V_{out}(t) = A(t)f[\omega_0 \cdot t + \Phi(t)] \qquad (2.6)$$

where $A(t)$ e $\Phi(t)$ are now functions of time and f is a periodic function with period 2π: the spectrum of a practical oscillator has now sidebands close to the frequency of oscillation.

A signal's short-term instabilities are usually characterized in terms of the single sideband noise spectral density. It has units of decibels below the carrier per hertz (dBc/Hz) and is defined as:

$$L_{total}\ \{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}\left(\omega_0 + \Delta\omega, \Delta F\right)}{P_{carrier}}\right] \quad (2.7)$$

where $P_{sideband}(\omega_0+\Delta\omega,1\text{Hz})$ represent the single sideband power at a frequency offset of $\Delta\omega$ from the carrier with a measurement bandwidth of 1Hz. The advantage of this parameter is its ease of measurement. Its disadvantage is that it shows the sum of both amplitude and phase variations; it does not show them separately. However, it is important to know the amplitude and phase noise separately because they behave differently in the circuit. For instance, the effect of amplitude noise is reduced by amplitude limiting mechanism and can be practically eliminated by the application of a limiter to the output signal, while the phase noise cannot be reduced in the same manner.

The semi-empirical model proposed by **Leeson-Cutler** is based on an LTI assumption for tuned tank oscillators. It predicts the following behavior for phase noise [3],[4]:

$$\zeta_{total}\ \{\Delta\omega\} = 10 \cdot \log\left\{\frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right] \cdot \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \quad (2.8)$$

where F is an empirical parameter, K is Boltzmann's constant, T is the absolute temperature, P_s is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q_L is the effective quality factor of the tank with all the loading in place, $\Delta\omega$ is the offset from the carrier and $\Delta\omega_{1/f3}$ is the frequency of the corner between the $1/f^3$ and $1/f^2$ regions, as shown in the sideband spectrum of Figure 2.2.

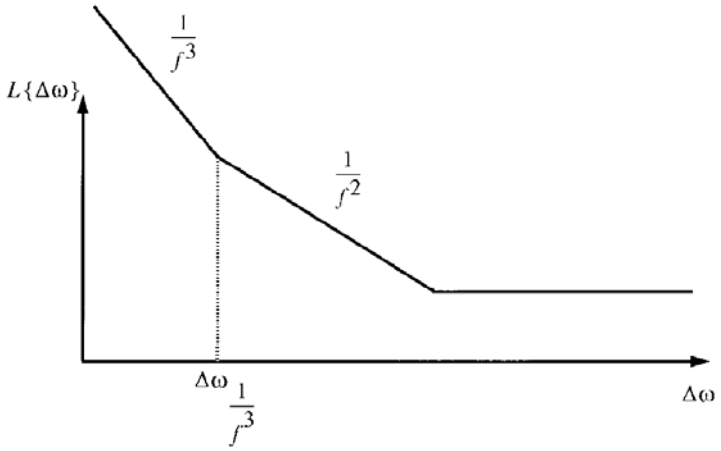

Figure 2.2: typical phase noise spectrum

The behavior in the $1/f^2$ region can be easily obtained by applying a transfer function approach as follows. The impedance of a parallel RLC, for $\Delta\omega << \omega_0$, is calculated to be:

$$Z(\omega_0 + \Delta\omega) \approx \frac{1}{G_L} \cdot \frac{1}{1 + j \cdot 2 \cdot Q_L \cdot \frac{\Delta\omega}{\omega_0}} \qquad (2.9)$$

where G_L is the parallel parasitic conductance of the tank.
For *steady-state* oscillation $G_m R_L=1$ should be satisfied; therefore, for a parallel current source, the closed loop transfer function of the oscillator shown in *Fig 2.3* is given by the imaginary part of the impedance:

$$H(\Delta\omega) = -j \frac{1}{G_L} \cdot \frac{\omega_0}{2 \cdot Q_L \cdot \Delta\omega} \qquad (2.10)$$

The total equivalent parallel resistance of the tank has an equivalent mean square noise current density of $\overline{i_n^2} / \Delta f = 4 \cdot k \cdot T \cdot G_L$.

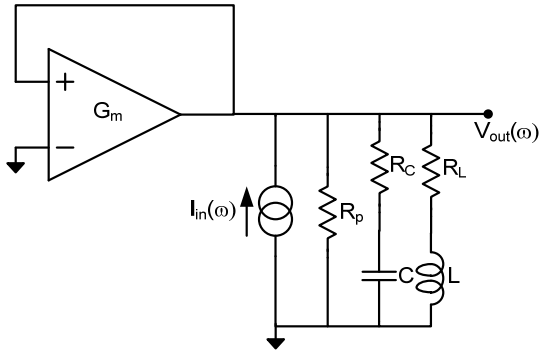

Figure 2.3: typical RLC oscillator

In addition, active device noise usually contributes a significant portion of the total noise in the oscillator. It is traditional to combine all the noise sources into one effective noise source, expressed in terms of the resistor noise with a multiplicative factor F, known as the device excess noise number. The equivalent mean square current density can therefore be expressed as $\overline{i_n^2} / \Delta f = 4 \cdot F \cdot k \cdot T \cdot G_L$. Unfortunately, it is generally difficult to calculate F *a priori*. One important reason is that much of the noise in a practical oscillator arises from periodically varying processes and is therefore cyclostationary. Hence F *and* $\omega_{1/f}$[3] are usually used as a *posteriori fitting* parameters on measured data.
Using the above effective noise current power, the phase noise in the $1/f^2$ region of the spectrum can be calculated as:

$$L_{total}\{\Delta\omega\} = 10 \cdot \log\left(\frac{\overline{v_{noise}^2}}{\overline{v_{sig}^2}}\right) = 10 \cdot \log\left[\frac{2 \cdot F \cdot k \cdot T}{P_s} \cdot \left(\frac{\omega_0}{2 \cdot Q \cdot \Delta\omega}\right)^2\right] \qquad (2.11)$$

Note that the factor of 1/2 arises from neglecting the contribution of amplitude noise. Although the expression for the noise in the $1/f^2$ region is thus easily obtained, the expression for the $1/f^3$ portion of the phase noise is completely empirical.
As such, the common assumption that the$1/f^3$ corner of the phase noise is the same as the 1/f corner of device flicker noise has no theoretical basis.

In 1998, **Hajimiri** [5] introduced a new model for phase noise, taking into account its time-varying nature and was therefore able to overcome the limitations of the Leeson Model.
To get to the basic equations of the model is necessary to introduce some preliminary notions.
An oscillator can be modeled as a system with inputs (each associated with one noise source) and two outputs that are the instantaneous amplitude and excess phase of the oscillator *A(t)* and *Φ(t)*. Noise inputs to this system are in the form of current sources injecting into circuit nodes and voltage sources in series with circuit branches. For each input source, both systems can be viewed as single-input, single-output systems. The time and frequency-domain fluctuations of A(t) and Φ(t) can be studied by characterizing the behavior of two equivalent systems shown in Fig. 2.4

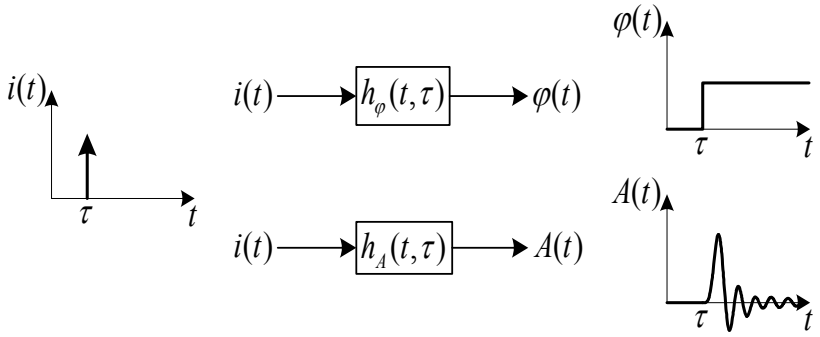

Figure 2.4 Phase and amplitude impulse response model

Consider the specific example of an ideal parallel LC oscillator shown in Figure 2.5. If we inject a current impulse *i(t*) the amplitude and phase of the oscillator will have responses similar to that shown in Figure 2.6.
The instantaneous voltage change ΔV is given by:

$$\Delta V = \frac{\Delta q}{C_{tot}} \qquad (2.12)$$

where Δq is the total injected charge due to the current impulse and C_{tot} is the total capacitance at the node. Note that the current impulse will change only the voltage across the capacitor and will not affect the current through the inductor.
It can be seen from Fig. 2.6 that the resultant change in *Φ(t)* and *A(t)* is time dependent. In particular, if the impulse is applied at the peak of the voltage

across the capacitor, there will be no phase shift and only an amplitude change will result. On the other hand, if this impulse is applied at the zero crossing, it has the maximum effect on the excess phase and the minimum effect on the amplitude.

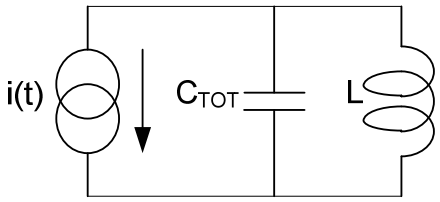

Figure 2.5: parallel LC tank

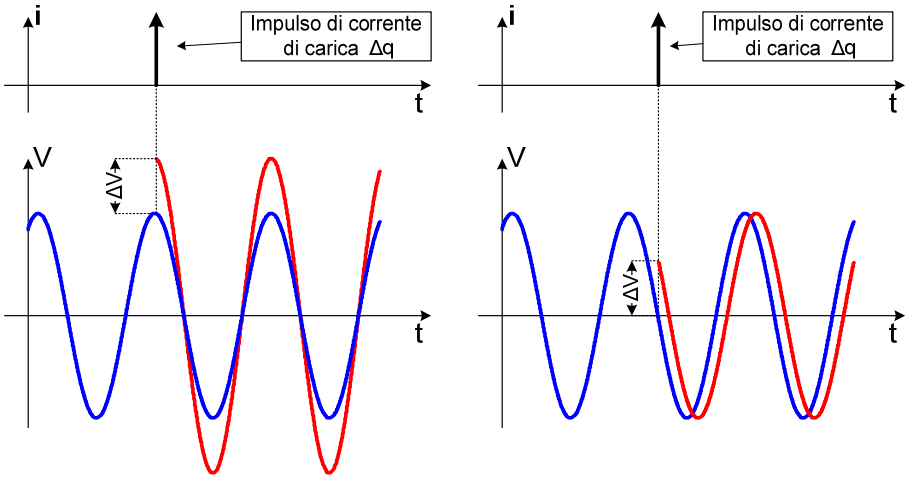

Figure 2.6:time-variant responce

It is critical to note that the current-to-phase transfer function is practically linear even though the active elements may have strongly nonlinear voltage-current behavior.

The amount of excess phase is proportional to the ratio of the injected charge to the maximum charge swing across the capacitor . Furthermore the impulse response for the first system of Fig. 2.4 is a step whose amplitude depends periodically on the time when the impulse is injected. Therefore, the unit impulse response for excess phase can be expressed as:

$$h_{\Phi}(t,\tau)=\frac{\Gamma(\omega_0\tau)}{q_{\max}}u(t-\tau) \qquad (2.13)$$

where $u(t)$ is the unit step and $\Gamma(x)$ is the *Impulse Sensitivity Function (ISF)*; It is a dimensionless, frequency and amplitude independent periodic function with period 2π, which describes how much phase shift results from applying a unit impulse at time $t=\tau$.

To illustrate its significance, the ISF's together with the oscillation waveforms for a typical *LC* and ring oscillator are shown in Fig.2.7.

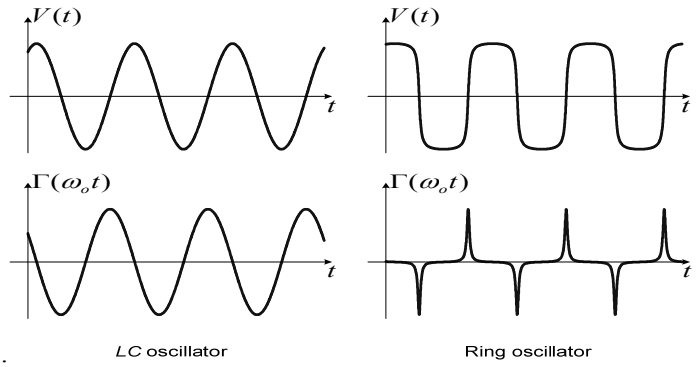

Figure 2.7: ISF examples

Given the ISF, the output excess phase $\Phi(t)$ can be calculated using the superposition integral:

$$\Phi(t) = \int_{-\infty}^{+\infty} h_{\Phi}(t,\tau) i(\tau) d\tau = \frac{1}{q_{\max}} \int_{-\infty}^{t} \Gamma(\omega_0 \tau) i(\tau) d\tau \quad (2.14)$$

where *i(t)* represents the input noise current injected into the node of interest. Since the ISF is periodic, it can be expanded in a Fourier series:

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \vartheta_n) \quad (2.15)$$

where the coefficients c_n are real-valued coefficients, and θ_n is the phase of the *n*th harmonic.
Using the above expansion in the superposition integrak, and exchanging the order of summation and integration, we obtain:

$$\Phi(t) = \frac{1}{q_{\max}} \left[\frac{c_0}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) \cos(n\omega_0 \tau) d\tau \right] \quad (2.16)$$

Equation (2.16) allows computation of Φ(t) for an arbitrary input current injected into any circuit node, once the various Fourier coefficients of the ISF have been found.
Once known $\Phi(t)$, in order to calculate the phase noise a phase-voltage conversion it should be done. the conversion of device noise current to output voltage may be treated as the result of a cascade of two processes. The first corresponds to a linear time variant (LTV) current-to- phase converter, while the second is a nonlinear system that represents a phase modulation (PM), which transforms phase to voltage (*figure 2.8*).

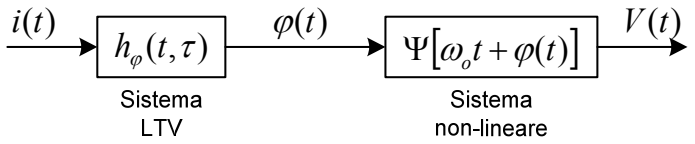

Figure 2.8: current-phase-voltage conversion scheme

Given a current noise $i_n(t)$, it can be shown that the components of noise near integer multiples of the oscillation frequency are transformed into close-in phase noise weighted by the coefficients c_n.
The oscillator internal flicker noise sources give rise to the region $1/\Delta\omega^3$ of the phase noise, whereas the components of white noise gives rise to the region $1/\Delta\omega^2$; the white noise floor phase noise is instead due additive white noise at the bottom of the oscillator output.

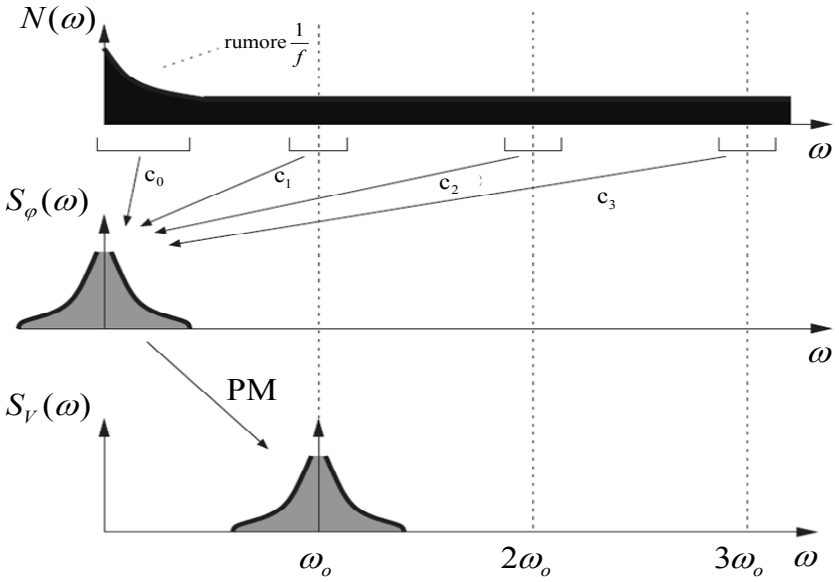

Figura 2.9: noise *down-conversion*

To carry out a quantitative analysis of the phase noise sideband power, now consider an input noise current with a white power spectral density $\overline{i^2_n}/\Delta f$.
The total single sideband phase noise spectral density in dB below the carrier per unit bandwidth due to the input noise source is given by:

$$L\{\Delta\omega\} = 10\log\left(\frac{\frac{\overline{i^2_n}}{\Delta f}\cdot\sum_{n=0}^{\infty}c^2_n}{8\cdot q^2_{\max}\Delta\omega^2}\right) \qquad (2.17)$$

now, according to *Parseval*'s relation we have:

$$\sum_{n=0}^{\infty}c^2_n = \frac{1}{\pi}\cdot\int_0^{2\pi}\left|\Gamma(x)\right|^2 dx = 2\Gamma^2_{rms} \qquad (2.18)$$

where Γ_{rms} is the rms value of $\Gamma(x)$. As a result:

$$L\{\Delta\omega\} = 10\log\left(\frac{\Gamma^2_{rms}}{q^2_{\max}}\cdot\frac{\overline{i^2_n}/\Delta f}{4\cdot\Delta\omega^2}\right) \qquad (2.19)$$

The device noise in the flicker noise dominated portion of the noise spectrum can be described by:

$$\overline{i^2_{n,1/\Delta f}} = \overline{i^2_n} \cdot \frac{\omega_{1/f}}{\Delta\omega} \qquad (\Delta\omega<\Delta_{1/f}) \tag{2.20}$$

Equation 2.20 together with Eq. 2.19 result in the following expression for phase noise in the $1/\Delta\omega^3$ portion of the phase noise spectrum:

$$L\{\Delta\omega\} = 10\log\left(\frac{{c_0}^2}{{q^2}_{\max}} \cdot \frac{\overline{i^2_n}/\Delta f}{4\cdot\Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2.21}$$

It should be noted that, unlike the *Leeson* model predicts, the $1/\Delta\omega^3$ corner of phase noise is smaller than the $1/f$ corner of the device.
According to Hajimiri, they are bound by the following relation:

$$\omega_{1/\Delta\omega 3} = \omega_{1/f} \cdot \left(\frac{c_0}{2\cdot\Gamma_{rms}}\right)^2 \approx \omega_{1/f} \cdot \frac{1}{2} \cdot \left(\frac{c_0}{c_1}\right)^2 \tag{2.22}$$

where c_0 depends on the waveform and can be significantly reduced if certain symmetry properties exist in the waveform of the oscillator.
In addition to the periodically time-varying nature of the system itself, another complication is that the statistical properties of some of the random noise sources in the oscillator may change with time in a periodic manner. These sources are referred to as cyclostationary; thermal noise of a resistor is an example of a stationary noise source.
S white cyclostationary noise current $i_n(t)$ can be decomposed as:

$$i_n(t) = i_{n0}(t)\cdot\alpha(\omega_0 t) \tag{2.23}$$

where $i_n(t)$ is a white ciclostationary process, $i_{n0}(t)$ is a white stationary process and $\alpha(\omega_0 t)$ is a deterministic periodic function describing the noise amplitude modulation.
The LTV model described above can be easily modified to take into account this aspect simply replacing $\Gamma(x)$ with an effective ISF, connected with the first according to this equation:

$$\Gamma_{eff}(x) = \Gamma(x)\cdot\alpha(x) \tag{2.24}$$

where $\alpha(x)$ can be easily derived from device noise characteristics and operating point.

2.1.4 Classes of VCOs for 60GHz applications

In general, there are almost three different classes for controlled oscillators on silicon ICs: ring oscillators, relaxation oscillators and tuned oscillators.
Ring oscillators consist of an odd number of single-ended inverters or an even-odd number of differential inverters with the appropriate connections. Relaxation oscillators alternately charge and discharge a capacitor with a

constant current between two threshold levels while tuned oscillators contain a passive resonator- LC tank or transmission line resonator, that serves as the frequency setting element.

The first two realizations are very easy to integrate on a monolithic IC and are very compact. Their frequency is controlled by a current or voltage and linear tuning characteristic can be obtained. Moreover, frequency tuning can be done over several orders of magnitude; tuned oscillator are harder to integrate primarily because of the lack of high quality passive inductors in standard IC technologies and because of their large size. However, they have a much higher frequency stability and spectral purity, thanks to the high quality factor of the passive resonator; relaxation and ring oscillators are typically very sensitive to noise in the switching thresholds and charging current end for this reason are not typically used at very high frequencies.

Various approaches of LC tuned VCO have been studied and implemented for 60GHz applications; among them the most common are push-push, Colpitts and cross-coupled oscillators.

Push-push approach has similar technical advantages as the doubler one, while it can be realized in a more compact form [6]; in this topology the outputs of two oscillators coupled in anti-phase are combined to yield a strong second harmonic output signal: the two sub-oscillators operate at one-half of the output frequency achieving higher resonator quality factor and lowering the parasitic effect than the fundamental oscillator approach. It also allows to extend the useful frequency range of available transistor technologies even beyond their maximum oscillator frequency. Moreover, this oscillator has such advantages as doubled output power from two sub-oscillators and reduced load pulling effect due to virtual ground formation at the output.

Push-push topology also allows locking the oscillator in a PLL loop using static or dynamic divider operating at the fundamental frequency instead of at the second harmonic.

The drawback of this topology is, however a more complicated design: the circuit principle usually requires a large-signal analysis to verify odd-mode operation of the sub-circuits and the bias networks has to properly be designed with respect to two critical frequencies.

Another important VCO approach widely used in high speed systems is the **Colpitts** oscillator which, with its simple oscillator core, has been the most favored topology for low noise design [7], [8].

Compared to the most widely used cross-coupled structures, the Colpitts oscillator provides a good potential in phase noise performance owing to its larger energy transfer efficiency; despite the above advantage, it needs higher required gain for reliable start-up and its single-ended nature makes it more sensitive to common-mode noise sources such as substrate and supply voltage. Differential Colpitts architectures which combine the advantages of complementary cross- coupled oscillator and the standard Colpitts one has been proposed, able to obtain optimal noise performances while solving the problems mentioned above.

As already mentioned, **LC-tank cross-coupled VCOs** are the most pervasive ones in high-speed systems [1], [9], [10]; the simple yet symmetric configuration facilitates high-speed and differential designs with large swings,

reasonable tuning range, and lower consumption. The plain structure also allows low-supply operation, even below 1V. Depending on the inductor and varactor Q, the cross-coupled oscillator can also achieve sufficiently low phase noise for mm-W applications.

A typical realization of a cross-coupled VCO is presented in Figure 2.10, where the pairs M_1-M_2 provides negative resistance $-2/g_{m1,2}$ to compensate for the tank losses (R_p). At resonance, these two resistances cancel each other and the oscillation frequency is given by:

$$\omega_{osc} = \frac{1}{\sqrt{L \cdot C_P}} \tag{2.25}$$

where L and C_P denote loading inductor and parasitic capacitance at the output nodes, respectively, and M_3-M_4 the MOS varactors.

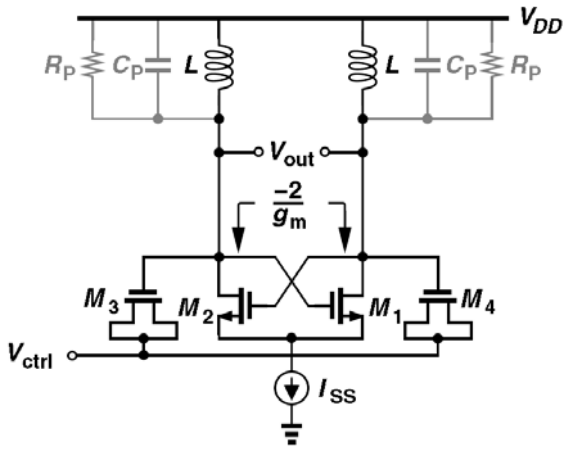

Figure 2.10: classical cross-coupled VCO schematic

Many variants to the original structure can be applied to improve the VCO performances; For example, a complementary PMOS-NMOS cross-coupled approach offers higher transconductance for a given current, which results in faster switching of the cross-coupled differential pair. It also offers better rise and fall-time symmetry, which results in a smaller $1/f^3$ noise corner. Also, the dc voltage drop across the channel is lower and therefore it alleviates the problems related to velocity saturation and high γ. The main drawback of complementary approach is the degradation of the tuning range due to the extra parasitic capacitance related to PMOS devices.

The tail current I_{SS} can also be removed to accommodate low-supply voltage operations, but at a cost of higher supply sensitivity; alternatively a tail capacitor can be placed in parallel to the current generator: it helps lowering phase noise because it acts changing the duty cycle of the waveform and so reducing the drain current (and the drain current noise) of the differential pair during the zero-crossing of the tank differential voltage.

It also acts attenuating the high frequency noise of the tail-current source I_{SS} so that up-conversion of *1/f* noise remain the only relevant noise component of noisy tail current.

A drawback of a VCO based on a cross-coupled differential pair is that a dedicated output signal buffer is always needed. A 50Ω buffer at mm-Wave frequencies is not straightforward in CMOS and usually shows a significant attenuation. Thus, although a 60GHz VCO is feasible in CMOS, buffering and distribution of its output signal is complex: this problem is believed to be the main bottleneck in CMOS, and limits the integration density at mm-Wave frequencies.
For frequencies above 10GHz, the **travelling wave oscillator** (RTWO) is considered as a good alternative to the classical LC-tank oscillator; it, in fact, combines the advantages of both the conventional LC tank oscillator and ring oscillator and allows to obtain multiple phases while keeping low power consumptions because the wave energy re-circulates within the loop as opposed to energy loss during charging/discharging through transistors in conventional designs.
These oscillator topology will be in depth studied in the last chapter of this thesis.

2.1.5 Millimeter wave VCO design challenges

The first challenge in designing high performance 60GHz VCOs comes from the high operative frequency, close to the transistor intrinsic frequency f_T and f_{max}, which limits the transistor available power gain [11].
The second challenge lies in the poor quality factor of passives at 60GHz: well-designed symmetric spiral inductors exhibit a Q of about 10 at 5GHz, but, according to electromagnetic Momentum simulations, a Q of no more than 30 at 60GHz. Attributed to substrate losses, this saturation of the inductor Q makes the design of mm-wave oscillators quite difficult. Since the Q does not scale by a factor of 12 from 5GHz to 60GHz, the tradeoffs between the phase noise, the tuning range, and the power dissipation become much more severe. Also, the Q of varactors falls below that of inductors at millimeter-wave frequencies and dominates the tank quality factor.
The third challenge is related to the tuning range. To achieve a certain tuning range, the maximum and minimum values of the tank capacitance should meet a certain ratio γ:

$$\gamma = \frac{C_{v-\max} + C_p}{C_{v-\min} + C_p} = \frac{1+\beta+\alpha}{1+\beta-\alpha} \tag{2.26}$$

where the parasitic capacitance C_p is parallel with the varactor C_v capacitance. C_p includes capacitance from the transistors in the cross-coupled pair and the buffer stage, and parasitic capacitance related to interconnect lines; parameters α and β respectively represent the varactor tuning ratio and the ratio of parasitic capacitance to varactor capacitance: $\alpha = \left(C_{v-\max} - C_{v-\min}\right)/\left(C_{v-\max} + C_{v-\min}\right)$ and $\beta = 2C_p/\left(C_{v-\max} + C_{v-\min}\right)$.
According to (2.26), the tuning range can be increased either by increasing α or by decreasing β; α can be increased by an inherent physical trade-off in the varactor between its tuning ratio and its Q, while β can be decreased by reducing the capacitive loading from the buffer stage, or by increasing the

varactor value. Reducing the capacitive loading will result in less output power. To increase output power an additional amplifying stage should be added, which will unavoidably increase the DC power consumption. On the other hand, increasing the varactor value will decrease the tank impedance, so larger negative-resistance transistors will be needed, otherwise the start-up condition may not be satisfied.

In addition, increasing the varactor value will deteriorate the tank quality factor Q_{tank}, thus causing the increasing of phase noise.

Another important challenge is the very large oscillator gain (K_{VCO}) and the worse reactive linearity. The large K_{VCO} is caused by a large required tuning range in a low supply voltage. In mm-wave oscillators, nonlinear transistor capacitance like C_{gs} and C_{ds} becomes a large portion of the tank capacitance, thus deteriorating the tank reactive linearity further. The above factors make the oscillator very sensitive to the AM noise and the noise from the control voltage and the power supply.

2.1.6 Lumped LC tank VCO's vs Standing wave oscillators

At frequencies above 1GHz, on chip inductors are commonly used. With increasing frequency, the quality factor of inductors usually increases, making on-chip inductors attractive for many microwave applications. At 60GHz, the electrical wavelength λ is approximately 2.5mm, and transmission lines offer a viable alternative for the realization of passive elements; an inductor for 60GHz applications can be realized as a spiral inductor or from a transmission line shorted at its end, also known as shorted stub.

Although the spiral inductor seems to be the preferred choice based on quality factor, variation of inductance over frequency, self-resonant frequency and chip area, there are several advantages of the shorted stub that are not captured by these electrical parameters. Given the quasi-transverse electromagnetic mode of propagation, transmission lines are capable of realizing precise vales of small reactance and are inherently scalable in length. Also, the well-defined ground return path significantly reduces magnetic and electric field coupling to adjacent structures: for circuits with multiple on-chip inductors, it is difficult to avoid coupling between the inductors and provide a low-impedance ground to the active circuit without sacrificing the inductor Q, while realizing inductors from shorted stubs allows to minimize coupling between inductors, even if these other inductors are placed next to each other. Thus, shorted-stub inductors are much simpler to use in practical design. Their lower sensitivity to substrate interference also reduces the important problem of oscillator pulling.

Finally T-lines (usually CPS) structures are easier to be modelled using the familiar differential LRCG network described in the first chapter.

The λ/4 (*l*) SWO, depicted in figure 2.11, is the most compact SWO configuration [12]. In this SWO a differential transmission line is connected to a pair of cross-coupled inverters at one end and is shorted at the other end: energy injected as forward waves by the cross-coupled inverters is reflected

into reverse waves at the short and in steady state the forward and reverse waves superpose to form standing waves.

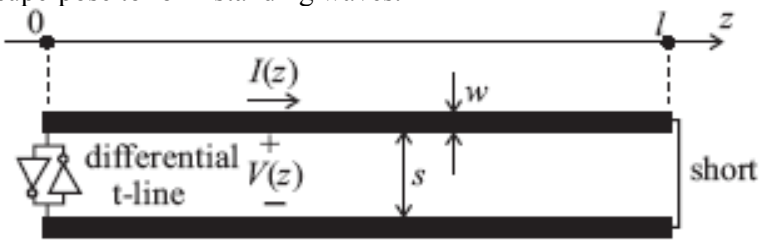

Figure 2.11: classical SWO oscillator

Standing waves are unique in that the current and voltage amplitude vary with position along the line while their phase remains constant; this important feature allows both to reduce skew in clock distribution systems and to adapt the T-line loss characteristics to the amplitude variations through *tapering* to reduce loss and improve phase noise significantly [13].
Another way to improve the stub Q is to shield the t-line using shielding bars realized in the lower metal layer M1 (*slow-wave* t-lines) [14].
Finally it must be observed that the input impedance of a distributed resonator has an high impedance not only at its fundamental frequency, but also at its harmonics; therefore, a square-wave current injected into the resonator creates a near-square wave voltage into the distributed tank. These harmonic content increases the voltage slope and mitigates PN due to the differential noise: this suggests the potential advantage of the SWO against the LC-VCO.
In the next two sections of this chapter the design, implementation and characterization of both a mm-wave LC lumped tank VCO and a mm-wave SWO will be presented.

2.2 Lumped LC Digitally Controlled oscillator

2.2.1 Why digital control?

In this section a low phase and quantization noise 50GHz LC digitally controlled oscillator (DCO) architecture that deliberately avoids any use of analog tuning is presented. This DCO is suitable for high performances mm-W digital frequency synthesizers.
A digital approach allows to obtain an higher Q (hence lower phase noise) of the tank without compromising the achievable tuning range, compared to analog tuning solutions, which can moreover result, for high tuning ranges, in an excessively high tuning sensitivity K_{VCO}.
All Digital phase locked loops (ADPLLs) for high frequency applications have become more attractive than analog PLLs also because of their fast-locking time, better controllability and better compatibility over different processes. Moreover they present an high degree of programmability, the possibility of using algorithms able to correct the non-idealities of the mixed signal blocks and the ability to simulate their behaviour using useful advanced tools such as *Matlab* and VHDL. Finally, an all digital approach

allows to obtain a reduction of the power dissipation and of the silicon area thanks to the absence of the analog loop filter that usually takes up much space.
Figure 2.12 shows the block diagram of a ADPLL-based frequency synthesizer.

Figure 2.12: ADPLL block diagram

In a ADPLL the classical phase detector is replaced by a *time to digital converter* (*TDC*) which makes a sort of analog to digital conversion by making a comparison between the fronts of the two input signals and producing at its output a digital word proportional to the temporal delay between them; this digital word controls the operating frequency of the DCO which, in turn, makes a sort of digital to analog conversion because it goes working at different frequencies depending on the digital control word.

2.2.2 Noise sources in a ADPLL

An all digital PLL features only two intrinsic noise sources represented by the two mixed-signal blocks: the DCO and the TDC.
This also compares favourably with the traditional *charge-pump PLL*, in which every component represents a potential noise source.
Besides the intrinsic noise, both in the DCO and in the TDC, it must also be taken into account the effects of quantization: the TDC samples the delay time between two signals, generating the so called *time quantization noise* (*TQN*).
Each time the oscillator phase is compared with the reference phase, the measurement introduces an error that can be seen as an additive noise on the DCO control signal. A major source of measurement error is the finite precision of the TDC (time resolution). The TDC, as already said, operates producing a digital code that represents the measured time difference once every reference cycle (T_{REF}). The least significant bit *LSB* of this "analog-to-digital" conversion represent the TDC time resolution $\Delta\tau$.
Given $\Delta\tau$ and assuming that the noise is equally distributed between the DC and the sampling frequency F_{ref} [15],[16], it is possible to calculate the quantization noise over time:

$$S_T = \frac{\Delta T^2}{12}\frac{1}{f_{REF}} \tag{2.27}$$

The time error results in a phase error $\Delta\phi = 2\pi f_0 \Delta T$, where f_0 is the DCO oscillator frequency.

The resulting time quantization noise is given by the following equation:

$$S_\phi = \frac{T_{REF}}{12}\left(2\pi f_0 \Delta T\right)^2 \tag{2.28}$$

DCO finite frequency resolution Δf also leads to phase noise. In fact, since the oscillator frequency is never exactly equal to a multiple of the reference, the frequency error is integrated by the loop, producing a phase error known as frequency quantization noise (*FQN*).
Also the FQN can be calculated assuming it is equally distributed from de DC to the sampling frequency f_{REF}:

$$S_f = \frac{\Delta f^2}{12}\frac{1}{f_{REF}} \tag{2.29}$$

The angular frequency error is $\Delta\omega = 2\pi\Delta f$, hence:

$$S_\omega = \frac{\Delta f^2}{12}\frac{(2\pi)^2}{f_{REF}} \tag{2.30}$$

and the phase error is the integral of the angular frequency error, hence ($\Delta\phi = \Delta\omega / s$):

$$S_\phi = \frac{\Delta f^2}{12}\frac{(2\pi)^2}{f_{REF}}\left(\frac{1}{2\pi f}\right)^2 = \left(\frac{\Delta f}{f}\right)^2 \frac{T_{REF}}{12} \tag{2.31}$$

Assuming *Δf* equal to 2MHz and T_{REF} equal to 20ns, a FQN of -102.3dBc/Hz at 10MHz offset from the carrier results, which is higher than what can be achieved in terms of thermal-induced phase noise using the designed DCO.
The frequency quantization noise can be further lowered adopting *sigma delta noise-shaping techniques* [15]; for instance, using a 2nd-order sigma delta modulation at 500MHz, FQN, given the same *Δf* would be lowered to -147.8dBc/Hz at 10MHz offset from the carrier. So a target *Δf* of 2MHz has been assumed.

2.2.3 Tuning banks design

As already said, one of the major shortcomings in the implementation of LC-tank oscillators at mm-waves frequencies is the low quality factor (Q) of the capacitors, that usually dominates the overall Q of the resonator; this is even more true for variable capacitance, both MOS varactors and switched Metal-oxide-metal (MoM) capacitors, where additional losses are brought about by active device limitations such as gate resistance, finite channel conductance and parasitic drain/source capacitance.
To better cope with technology limitations at high frequencies, as opposite to a previous implementation at 10-GHz [17], the capacitor bank was segmented into three sections [18] (coarse, intermediate and fine tuning sections), implemented with different structures (figure 2.13): tuning range an Q are the primary drivers for the coarse-tuning bank, while small minimum capacitance step represents the main requirement for the fine-tuning bank. Extending the tuning range of the fine-tuning bank up to the frequency resolution of the coarse-tuning section with some margin would require more than 100 elements resulting in an exceedingly large tuning structure: the intermediate

tuning bank has the function of bridging the gap between the coarse and fine tuning sections, without oversizing the whole tuning structure. This allows not only to reduce the overall size of the circuit but also to minimize the parasitic inductance that would hinder oscillation above 50GHz.

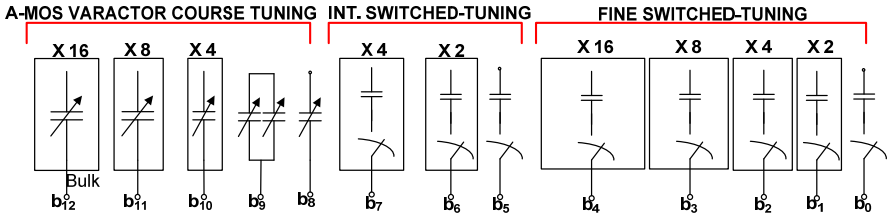

Figure 2.13: Tuning banks

The coarse and intermediate sections are intended to be used in the starting phase of the locking algorithm, similarly to what is done in analog PLLs when the VCOs uses switched tuning, while the fine tuning bank is used in the normal operation (steady state) of the PLL.

For the **coarse tuning** section, two different tuning devices have been compared: the NMOS in n-well accumulation-mode (a-MOS) varactor, switched between the extremes of its C-V characteristic, and the NMOS transistor operated as a switch [19]. To compare the two device, a variable-capacitance figure of merit (FoM_C) has been used:

$$FoM_C = \frac{1}{\omega_0 \cdot R_{ON} \cdot C_{OFF}} \tag{2.32}$$

where ω_0 is the oscillation frequency, R_{ON} is the resistance of the device when it exhibits the maximum value of capacitance (corresponding to the accumulation region for the varactor) while C_{OFF} is the minimum capacitance; in this, both quality factor and tuning capability (C_{MAX}/C_{MIN}) are taken into account.

Since at the time of design, a scalable model of the a-MOS varactors was not available in the technology design kit (90nm TSMC) a custom scalable *Verilog-A* model has been developed on the basis of the device model of an a-MOS varactor with fixed device size (finger width of 1.6µm, channel length of 400nm), by means of a scalable physical model of the device [20].

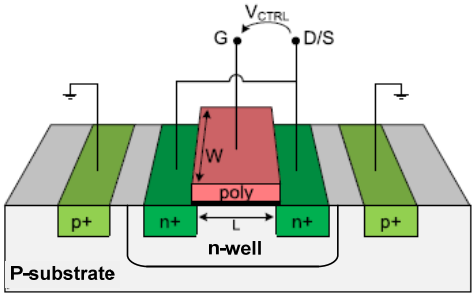

Figure 2.14: a-MOS cross section

Figure 2.14 shows the cross-section of an accumulation MOS varactor: it can be observed that it is physically identical to a classical PMOS transistor,

except that the presence of the n-well diffusion; the gate and the two n^+ contacts inside the n-well are the controlling electrodes.
By applying a positive voltage between the gate and the n-well the surface is accumulated and the device capacitance equals the oxide one; if the applied voltage is reversed then the surface layer is depleted and the series capacitance decreases. The minimum value of capacitance is reached when the voltage difference between the electrodes equals the threshold voltage.
In table 2.1 are summarized the simplified equations used to extract the device scalable model.

Depletion	Accumulation
$C = \left[\frac{\varepsilon_{ox} \cdot \varepsilon_s}{\varepsilon_{ox} \cdot x_d + \varepsilon_s \cdot t_{ox}} \cdot (W \cdot L) \right]$	$C = \frac{\varepsilon_{ox}}{t_{ox}} \cdot (W \cdot L)$
$R = \frac{R_{\square poly} \cdot \left(\frac{W}{L}\right) + R_{\square well} \cdot \left(\frac{L}{W}\right)}{12}$	$R = \frac{R_{\square poly} \left(\frac{W}{L}\right) + \frac{R_{\square well}}{1+a} \cdot \left(\frac{L}{W}\right)}{12}$ $a = 12 \cdot R_{\square well} \cdot (V_{GS} - V_{th}) \cdot \mu_n \cdot C_{ox}$

Table 2.1: a-MOS simplified equations

Based on this approximate varactor model and on the switch device model, a comparison of the two structures has been carried out for different device sizes. In a 90nm CMOS technology, depending on the chosen channel length (L_f) and finger width (W_f), the a-MOS varactor or the switched-*MoM* capacitor features an higher FoM_C. At W_f=1μm and L_f=100nm the a-MOS varactor reaches the maximum FOM_C, equal to 128 at 50GHz, that is approximately three time grater then the MOS switch's maximum one, even neglecting the bottom-plate capacitance of the latter.
As shown in figure 2.15, according to our model, the a-MOS varactor (sized for optimum FOM_C) features an equivalent capacitance which goes from a minimum of about 0.42fF to a maximum value of 1.49fF, resulting in a tuning capability (C_{MAX}/C_{MIN}) of about 3.5. The device shows the maximum series resistance of about 45ohm in the depletion region.
Based on the result of the two devices FOM_C comparison, the a-MOS varactor with W_f=1μm and L_f=100nm has been used for the coarse tuning section, while custom-designed MoM capacitors were used to achieve a finer frequency resolution than would be attainable using a minimum-sized a-MOS varactor.
The coarse tuning bank is formed by 31 identical a-MOS, controlled by a 5-bit binary word; according to our approximate model this should cover a frequency range of about 3.2GHz with a frequency resolution equal to 104MHz.

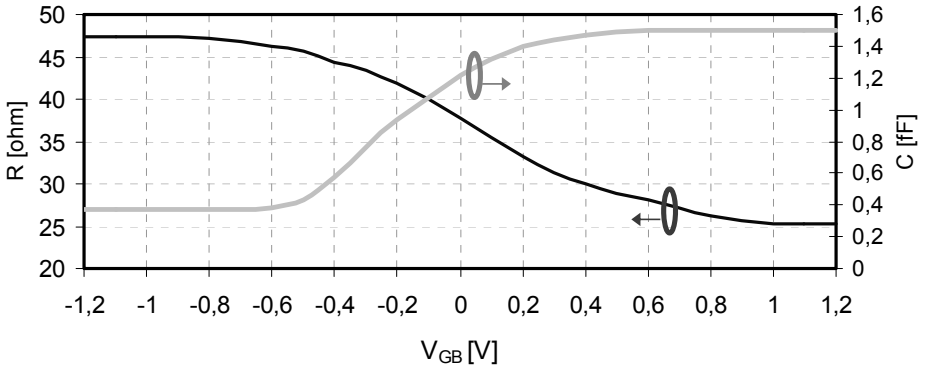

Figure 2.15: a-MOS R and C vs V_{GS}

The **fine tuning** bank manages relatively small values of capacitance therefore the Q of its elements has a little influence on the oscillator's phase noise and it doesn't matter so much; the main target of this bank is instead to achieve a frequency resolution as high as possible (around 2MHz). In order to obtain such small capacitive steps (ΔC=10aF) a switched tuning arrangement is exploited: MOS transistor are here used as switches that trigger on and off a series capacitor, ideally without losses.
The switched tuning topology has been used in a not-conventional manner: as a matter of fact, each MOS switch has been sized (Wf=0.12μm, L_f=100nm) so that its cut-off parasitic capacitance (C_{OFF}=176aF) dominates over the *MoM* nominal one. Only adopting this solution makes possible to obtain the required ΔC of about 10aF. In order to cover with some margin the required frequency range 31 identical *MoM* capacitors with series NMOS switches has been used; switches are controlled by a 5-bit thermometer code to ensure monotonicity and reduce non-linearity (moving from one digital configuration to the next one always only one element of the bank change its state, see Appendix 2).
Figure 2.16 shows the physical implementation of two adjacent elements of the bank: a single top layer (M_6) is used for all capacitors while the bottom plate of each capacitor is implemented as a metal stack (M_4-M_1), connecting to the NMOS transistor switch.
The total capacitance seen at node A when both the two switches are turned on or off is given by:

$$C_{OFF} = 2\left(\frac{C_{MoM}\cdot\left(C_{SUB}+C_{OFF}\right)}{C_{SUB}+C_{OFF}+C_{MoM}}\right)+C_2 \qquad (2.33)$$

$$C_{ON} = 2\left(\frac{1+\omega_0^2\cdot R_{ON}^2\cdot\left(C_{MoM}+C_{SUB}+C_{ON}\right)\cdot\left(C_{ON}+C_{SUB}\right)}{1+\left[\omega_0\cdot R_{ON}\cdot\left(C_{SUB}+C_{ON}+C_{MoM}\right)\right]^2}\right)+C_2 \qquad (2.34)$$

where C_{ON} and C_{OFF} respectively represent the capacitance of each MOS switch on its ON or OFF state.
Obviously, the physical implementation plays a key role in obtaining the desired delta: the metal layers to be used, the optimal sizing of each element

and the minimum distance between two adjacent plates have to be chosen carefully. The optimization of the bank has been performed by means of electromagnetic simulations with *Integrand Software* (EMX), based on simplified circuital model accounting for the main capacitive and resistive terms that influence the ΔC.

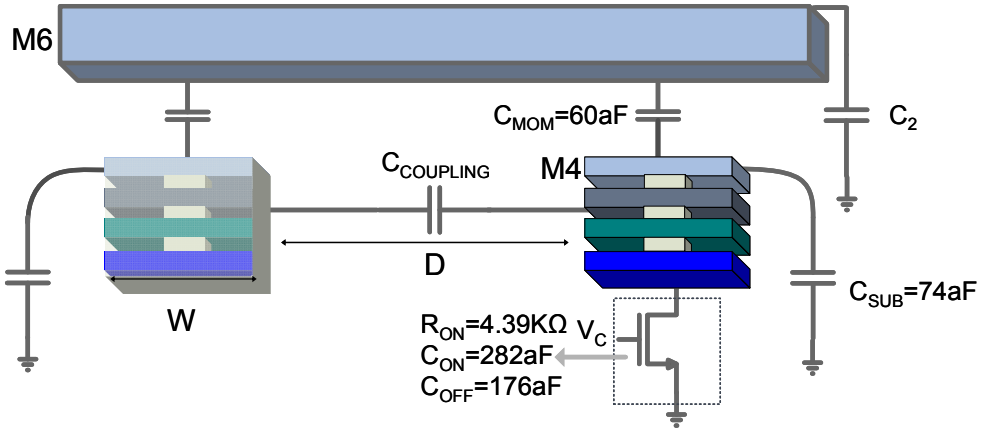

Figure 2.16: layout of the two adjacent fine tuning elements

The optimization's results have shown that with a top-bottom capacitance (C_{MOM}) in the order of 60aF, a bottom-ground capacitance (C_{SUB}) of about 74aF and a minimum-sized switch, a capacitive step in the order of 9.5aF is obtained. This is achieved using square capacitive elements with a side of W=0.27μm (which is also the minimum allowable by technology design rules), spaced of 0.6μm one from each other.

The unavoidable coupling between adjacent cells causes a non-linearity in the code-to-frequency characteristic: this effect is represented in the circuital model (Figure 2.16) by the capacitance $C_{COUPLING}$. This coupling effect influences the value of the delta only if the two switches that control adjacent capacitive elements are in a different state (one switched on and the other turned off) because otherwise $C_{COUPLING}$ is between two nodes at the same voltage.

In the real overall structure each capacitive element is surrounded by 8 identical capacitive units; the effect of coupling is stronger in two opposite cases:

- the central element is switched on while all the surrounding elements remain in the OFF state;
- the central element is switched off while all the surrounding elements remain in the ON state.

These two cases have been analyzed through electromagnetic simulations resulting in a maximum error caused by coupling which remains however lower than 1/9 LSB.

To test the robustness of the project is necessary not only to analyze the effect of coupling on delta, but also of geometrical variations caused by technology process spread; process spreading may cause a variation in the capacitive plates area(horizontal variations) and in the thickness of the metal and dielectric layers (vertical variations), determining a chance of C_{MOM}, $C_{COUPLING}$ and C_{SUB} values.

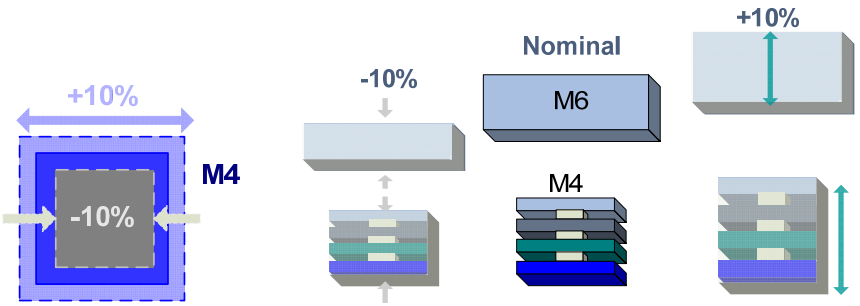

Figure 2.17: horizontal and vertical geometrical variations

With regard to horizontal variations, has been considered two opposite worst cases: +/- 10% of percentage variation in capacitive plate side (L).
The first plot in figure 2.18 shows that this variations causes, according to simulations, a corresponding ΔC error which goes from +1% to -0.7% that can be neglected.

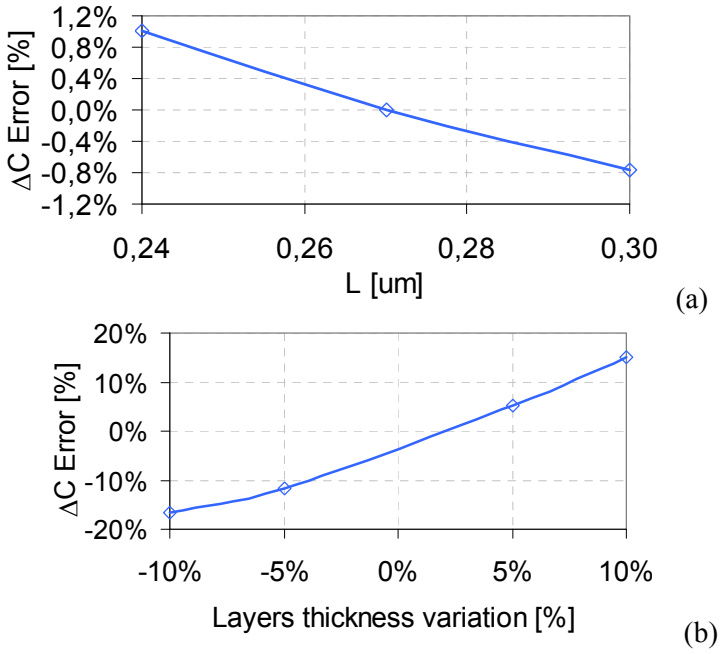

Figure 2.18: process spreading effect

(a) horizontal variations (b) vertical variations

From the second plot is evident that a more significant ΔC variation comes from vertical variations: a percentage variation of +/-10% in the layers thickness causes a ΔC deviation of about +/- 15%; quantitatively, ΔC goes from a nominal value of 9.54aF to respectively 8.1aF and 11aF, hence the maximum variation remains lower than 1/5 LSB demonstrating that robust operation is ensured.
Also the **intermediate tuning** bank exploits a switched tuning arrangement: the overall structure consist of 7 capacitors controlled by means of a 3bit binary word.
The complete layout of this bank is depicted in figure 2.19: capacitive elements are now realized in an inter-digitized manner, using the technology

layers M_5 and M_4. Switches are located underneath the M_1 plate of each capacitor.

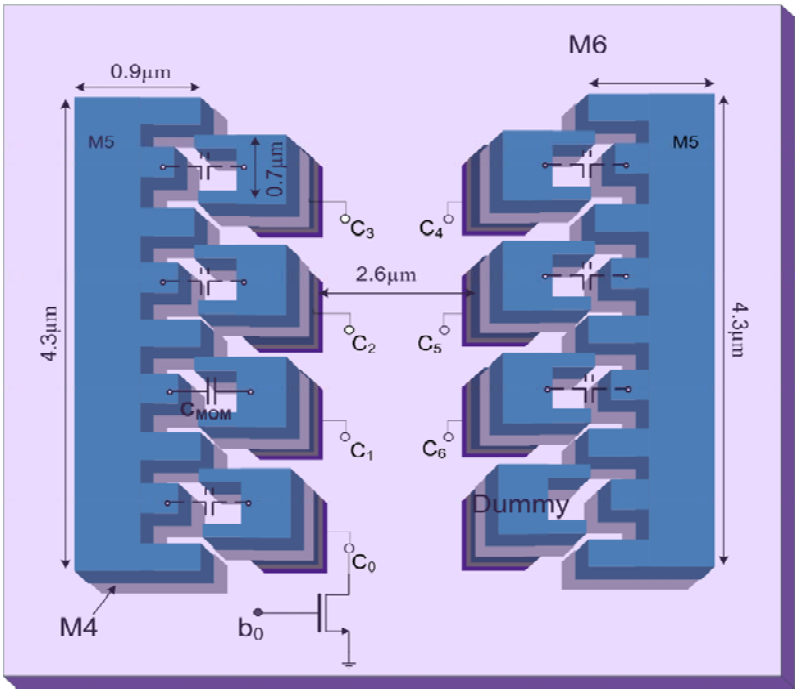

Figure 2.19: intermediate tuning bank

The physical realization has been performed, also for this bank, by means of electromagnetic simulations of the structure, based on a simplified circuital model which is, in principle, the same used for the fine tuning bank design.
The size of the MOS switches has been chosen in order to obtain a theoretical frequency resolution of roughly 15MHz (which corresponds to a single-ended ΔC of about 220aF) whit a physical structure as small as possible:

$$\left(\frac{W}{L}\right)_{Switch} = \left(\frac{0.2\mu m}{100nm}\right) \Rightarrow \begin{cases} R_{ON} = 2.6K\Omega \\ C_{OFF} = 204aF \end{cases} \qquad (2.35)$$

Also in this case, coupling between adjacent cells determines a non-linearity in the code-to-frequency characteristic which remains always lower that 1/5 LSB.

2.2.4 Oscillator core design

The oscillator core, as shown in figure 2.20, consists of a complementary NMOS-PMOS cross-coupled pair that generates the negative resistance required to sustain oscillation. The use of a complementary topology allows to achieve near double current efficiency as compared to the single-pair topology because during each half period the same dc current is exploited both by NMOS and by PMOS transistors, producing a reduction of the required MOS g_m. This enhances the oscillator efficiency while keeping the low-voltage transistors, including the a-MOS varactors, always below V_{DD}.

A further improvement of the power efficiency derived from the typical Class-C nature of the current waveform in this topology: transistors operate with a <50% duty cycle, resulting in a more efficient energy restoration.

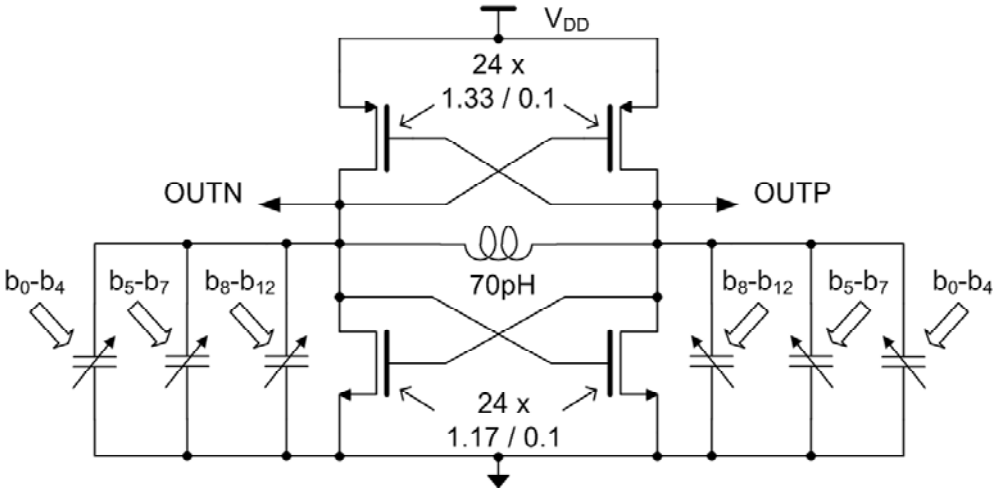

Figure 2.20: DCO schematic

Furthermore, with the a-MOS varactors gates biased around $V_{DD}/2$ and a rail-to-tail voltage swing, close to maximum tuning of the varactors is achieved without requiring the control voltage, connected to the a-MOS source/drain terminals, to swing above V_{DD}.
This topology also allows to have an additional degree of freedom in the design and layout of the pair.
The lack of the tail generator allows an easier self-biasing of the differential pair and the maximization of the oscillation amplitude while removing, at the same time, a relevant source of thermal and flicker noise.
In practice, this oscillator operates intrinsically near the limit between the current-limited and the voltage-limited regions; this allow to maximize phase noise, but the lack of the tail generator on the other hand, makes the oscillator more sensitive to the power supply noise. This problem has been partly removed by heavily filtering it on the control board used for measurements.
The core transistors have been sized according to the main targets of minimizing phase noise and complying with the oscillation start-up condition with some margin ($g_m R_{TANK}=3$), while taking into account layout related parasitics. For a given total device width, reducing the finger width helps lowering gate resistance, but increases device perimeter and interconnect parasitic capacitances. In order to minimize layout parasitic, PMOS and NMOS transistors were laid out with the same number of fingers (each transistor is made up of 24 fingers). The finger widths have also been chosen in order to optimize the f_{MAX} of the pair (fingers size is reported in Fig 2.20). The expected overall fixed capacitance contributed by the active devices, including interconnect parasitic, is approximately 90fF.
In order to minimize parasitic series inductances, the coarse tuning varactors were laid out right beside the active devices, as shown in figure 2.21. The single-turn inductor, physically implemented on the top metal layer (M_6), has been optimized for maximum Q and to facilitate the placement of active core

and capacitor arrays. Even if the inductor design theoretically becomes simpler as the operating frequency increases (because inductor Q is proportional to frequency), the designer must pay attention because at mm-W frequencies there are many relevant energy loss mechanisms and coupling mechanisms that must be considered and carefully modelled to obtain accurate simulations; for example, inadequate capacitance modelling could bring a shift in the simulated DCO oscillation frequency of at least 10%. The losses in silicon substrate are reduced minimizing the inductor footprint (outer diameter and line width W), while series losses caused by the finite conductivity of M_6 are reduced by increasing W: a trade-off between these two goals has been done. An accurate inductor circuit model has been derived from *Agilent-Momentum* EM simulations. The inductor layout and its circuital double-π model [21], valid in the frequency range 50-70GHz, are reported in Fig. 2.21. Inductance value is about 70pH, with a differential Q of 19 at 60GHz.

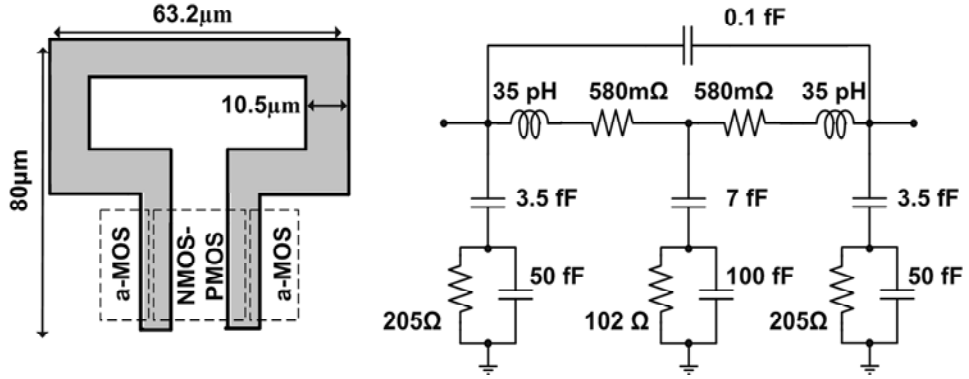

Figure 2.21: Layout and equivalent circuit model of the inductor

2.2.5 Phase noise prediction

With respect to the DCO phase noise a quite simple analytical prediction has been done making use of Hajimiri's and Lee's phase noise theory based on the impulse sensitivity function (ISF) concept.

On the basis of this theory, has widely discussed in section 2.1.3, the $1/f^2$ phase noise at the angular frequency offset $\Delta\omega$ is given by:

$$L(\Delta\omega) = 10\log\left(\sum_n \frac{\Gamma^2_{n,rms}\cdot \overline{i^2_n}/\Delta f}{2\cdot {q_{\max}}^2\cdot(\Delta\omega)^2}\right) \qquad (2.36)$$

where q_{max} is the maximum amount of signal charge loaded into the tank capacitance, i_n is a generic white current noise source, and Γ_n is the (effective) ISF related to i_n. Assuming a sinusoidal waveform $V(\Phi)= A\ sin(\Phi)$ across the tank capacitance, the ISF associated with the tank parallel resistance R_P is given by $\Gamma_{Rp}= cos(\Phi)$.

The symbolic expressions for the *ISF* of all MOS channel-current noise sources can be found in terms of the known $\Gamma_{Rp}(\Phi)$ by analysing the simplified small-signal circuit of the oscillator in Fig. 2.22 and applying the definition of ISF as the excess of phase generated by a current impulse

injected into the oscillator in parallel with the respective noise source. In practice, the "transfer function" of each single current noise source towards the differential output of the DCO must be evaluated.

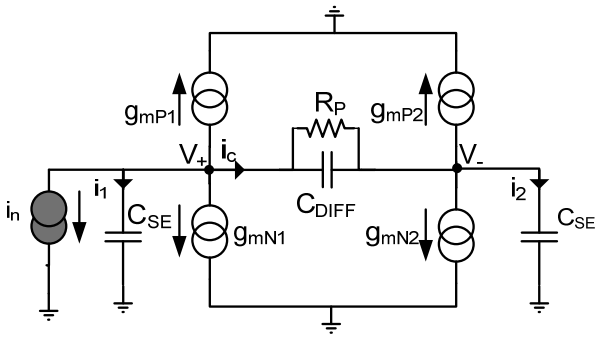

Figure 2.22: DCO small-signal circuit

In Fig. 2.22 C_{SE} and C_{DIFF} represent respectively the total single-ended capacitance and the total differential capacitance seen by the tank. C_{SE} is due to MOS parasitics, to DCO buffer capacitive load (20fF single- ended) and to many other causes; this single-ended capacitance isn't negligible at such high frequencies because only the complementary NMOS-PMOS cross-coupled pair introduces a parasitic capacitance in the order of 70fF that is about 50% of the total tank capacitance.
The DCO C_{SE} and C_{DIFF} has been estimated practically through AC analysis of the circuit resulting in $C_{SE} \approx 161$ fF and $C_{DIFF} \approx 45$ fF.
By applying the *Thevenin* theorem at the two output nodes V_+ and V_- this system of equations can be written:

$$\begin{cases} i_c = sC_{DIFF} \cdot (V_+ - V_-) \\ i_c = g_{mP2} \cdot V_+ + g_{mN2} \cdot V_+ + i_2 \\ i_n + i_c + i_1 + g_{mP1} \cdot V_- + g_{mN1} \cdot V_- = 0 \end{cases} \tag{2.37}$$

where:

$$\begin{aligned} i_1 &= sC_{SE} \cdot V_+ \\ i_2 &= sC_{SE} \cdot V_- \end{aligned} \tag{2.38}$$

Resolving the system we obtain:

$$V_+ - V_- = -\frac{i_n \cdot (sC_{SE} + G_2)}{s^2 C^2_{SE} - G_2 G_1 + sC_{DIFF} \cdot (2sC_{SE} + G_1 + G_2)} \tag{2.39}$$

where $G_1 = g_{mN1} + g_{mP1}$ e $G_2 = g_{mN2} + g_{mP2}$.
So we obtain that the equivalent noise current source in parallel to the tank R_p due to the thermal noise of a generic transistor is given by:

$$i_{n,R_{p\_EQ}} = sC_{eq}\cdot\left(V_+ - V_-\right) = -\frac{i_n\cdot\left(sC_{SE}+G_2\right)}{s^2C^2_{SE} - G_2G_1 + sC_{DIFF}\cdot\left(2sC_{SE}+G_1+G_2\right)}\cdot\left(\frac{C_{DIFF}\cdot C^2_{SE}}{C_{DIFF}+2C_{SE}}\right)\cdot s$$

$$Z(s) = \frac{i_{n\mathrm{Re}q}}{i_n} = -\frac{\left(sC_{SE}+G_2\right)}{s^2C^2_{SE} - G_2G_1 + sC_{DIFF}\cdot\left(2sC_{SE}+G_1+G_2\right)}\cdot\left(\frac{C_{DIFF}\cdot C^2_{SE}}{C_{DIFF}+2C_{SE}}\right)\cdot s \tag{2.40}$$

This equation is not longer valid when C_{SE} is zero.
Therefore, considering $s \to \infty$, the ISF associated with a generic MOS channel-current noise sources is:

$$\Gamma_{in} = \Gamma_{R_P}\cdot\frac{C_{DIFF}\cdot C_{SE}}{\left(2C_{DIFF}+C_{SE}\right)\cdot\left(C_{DIFF}+2C_{SE}\right)} \tag{2.41}$$

and it is the same any MOS is considered.
From Eq. 2.41 can be noticed that the ISF is independent on MOS g_m and it goes zero if the ISF associated with R_P goes zero or if C_{DIFF} or C_{SE} are equal to zero (this can't never happen in real cases). It also tends to be lower when a capacitance dominates over the other one.
So, from this analysis, it can be deduced that at high frequency (f_{osc}> 10GHz), since C_{SE} can't be zero, it is profitable, in order to reduce MOS contribution to phase noise, to make C_{SE} as high as possible with respect to C_{DIFF}.
Once given the ISF associated with a generic MOS channel current noise source and the power spectral density associated with this source ($\frac{\overline{i^2_n}}{df} = 4\cdot K\cdot T\cdot\gamma\cdot g_m$) its contribution to phase noise can be easily found applying Hajimiri's equation.
In order to make a quantitative prediction of phase noise contributors in our DCO the oscillation period has been quantized (n time samples) and the g_m, ɣ of each MOS and the ISF_{Rp} have been extracted from simulations in connection with each single time sample.
Once known some sampled values of the different noise contributions, their rms values are computed in this way:

$$\frac{i^2_n}{df}_{RMS} = \sqrt{\frac{\sum_{i=1}^{n}\left(\frac{i^2_n}{df}_i\right)^2}{n}} \tag{2.42}$$

Fig. 2.23 shows the plot of $\Gamma_{Rp}(\Phi)$ as a function of time, over an oscillation period *T*. *The* $\Gamma_{Rp}(\Phi)$ samples has been obtained through transient circuital simulations, injecting a current impulse with an amplitude *A* of 1mA and a width ΔT of about 500fs (after a time for oscillation's stabilization of about 0.5ns) in parallel to the tank inductance, and verifying the corresponding generated time shift (*dt*).
Once known *dt* , the $\Gamma_{Rp}(\Phi)$ corresponding sample is given by:

$$\Gamma_{R_P} = \frac{dt}{\Delta q} \tag{2.43}$$

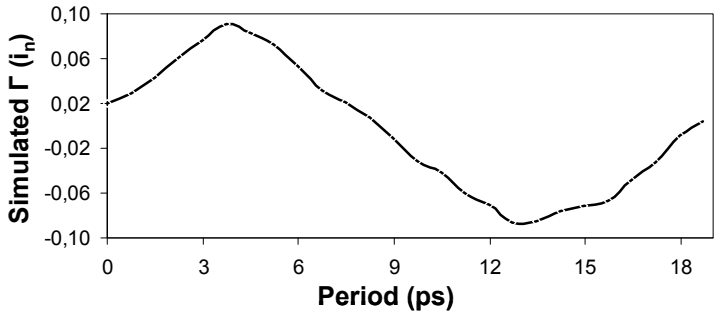

Figure 2.23: simulated $\Gamma_{Rp}(\Phi)$

From this theoretical analysis it results that the major contributor to phase noise (44%) is the thermal noise of the tank resistance R_P (480Ω), that sums up all the resistive parasitic terms associated with the tuning system and the inductor. Each NMOS of the switching pair contributes 15% of total phase noise, while each PMOS contributes 12.6%: these theoretical results are conforming to the simulated ones (43.9% R_p, 15.6% NMOS, 12.1% PMOS).

2.2.6 Experimental results

The test chip has been designed and implemented in TSMC 90nm CMOS process with 6 levels of metal and ultra thick top metal. A chip micrograph is reported in Fig. 2.24. Bias and control pads are located on the top (not shown), while the two outputs, suitable for on-chip measurement with GSG probes, are in the lower portion. The chip, including all pads, measures 1078 x 760 μm^2, but most of the chip area is occupied by the output buffer, which is only required for testing purposes. The core circuit area is only 106 x 83 μm^2.

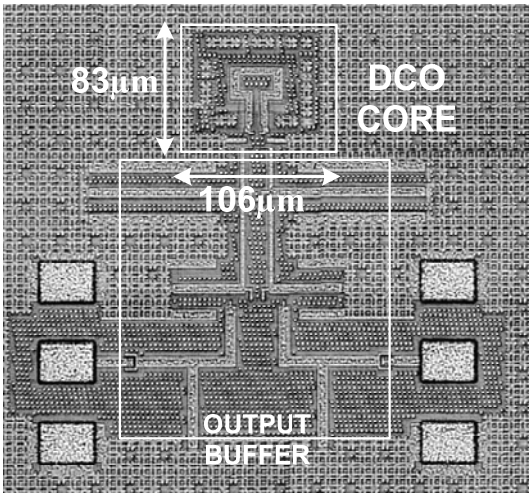

Figure 2.24: Die microphotograph

The measurement setup for the DCO characterization is reported in Fig. 2.25. The oscillator was characterized on-chip by directly probing its output in single-ended configuration. The outgoing signal from the probes is down-

converted by means of a Wisewave V-band mixer, driven by a 51-53GHz local-oscillator provided by an Agilent E8527D generator. In order to improve phase noise measurement accuracy, an intermediate-frequency amplifier on a custom-made board is used to boost the signal level. Phase noise is finally measured using an R&S FSUP signal analyzer using the cross-correlation method. FSUP uses a phase-locked loop to synchronize an internal reference source to the device under test (DUT) frequency, and a phase detector measures the noise level at different offset frequencies; outside the loop bandwidth phase noise is caused only by the DCO.
The lack of the tail current generator in this design makes the oscillator more sensitive to disturbances on the power supply. This has been addressed during testing using two separate boards: one small-sized microwave board where the chip is down-bonded and large bypass capacitors are used to heavily filter the supply and control lines; one larger control board that is used to generate and process the control signals.

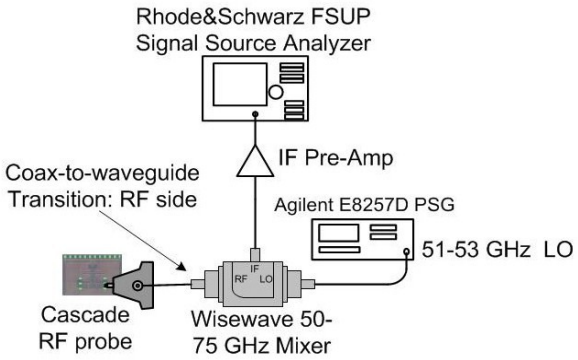

Figure 2.25: Experimental setup for the DCO characterization

The measured tuning range of 2 GHz, is lower than predicted due to underestimation of the depletion capacitance of the a-MOS varactor by the approximate model used in this work. This underestimation has been verified through a post-design device characterization, which has been carried out from S-parameter measurement on dedicated on-wafer test-structures using three steps de-embedding procedures (see. Appendix 1). For the sick of accuracy, device capacitance as a function of the voltage between the gate electrode and n-well has been derived carrying out measures on devices with a different number of fingers (10, 20 and 30) an comparing the obtained capacitive curves.
We have not been able to extract the value of the varactor series resistance because the whole impedance was too close to the edge of the Smith chart; probably, using DUT with a much larger number of fingers it would have been possible to extract it.
Fig. 2.26 clearly shows the device depletion capacitance (pre-characterization) under-estimation by our pre-characterization model: the measured varactor tuning capability C_{MAX}/C_{MIN} is around 1.89.
A new correct model has been made on the bases of this device characterization and the new model has been used to compare the simulated and measured DCO performances.

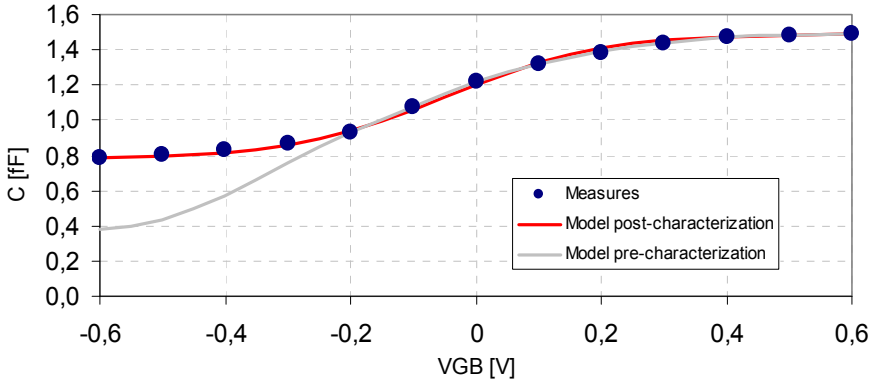

Figure 2.26: varactor characterization

The measured DCO coarse-tuning average frequency step is 64 MHz, with less than 50-MHz differential non-linearity (DNL). Fig. 2.27 shows a very good agreement between measures and simulation carried out using the post-characterization varactor model. The effective varactor tuning capability, deduced from DCO measurements, is nearly the same predicted by the model: this, not only guarantees the correctness of the varactor model, but also indicates that the varactor capacitive curve is fully exploited.

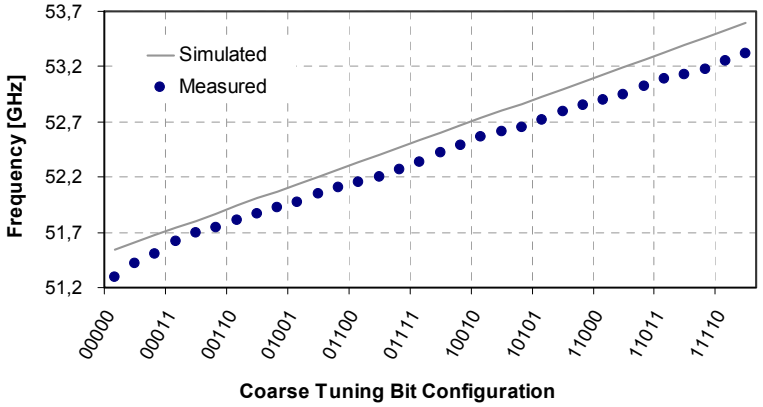

Figure 2.27: course-tuning measured and simulated performances

The intermediate tuning section shows a tuning range of 102 MHz, an average frequency step of 14 MHz and a DNL of less than 3 MHz. The frequency range covered by the fine tuning section is 54 MHz, with an average step of 1.8 MHz. Accurate direct measurements of the individual fine frequency steps were not possible using the aforementioned setup. Therefore, an indirect measurement has been carried out taking advantage of the thermometer-code control to toggle a single capacitor at a time, performing a narrow-band digital frequency modulation. This results in a pair of sidebands around the carrier (see Appendix 3) with relative amplitudes proportional to the frequency step that can be easily measured using the spectrum analyzer. The modulating frequency must be chosen carefully in order to minimize unwanted effects due to on-board parasitics on the ground and control lines, and such that the narrow-band assumption is satisfied. A modulating frequency between 30-40MHz has been chosen. Due to an implementation mistake in the control board only a sub-set of the fine-tuning capacitors could

be tested. The measured frequency step is equal on average to 1.78 MHz, consistently with the direct measurement carried out between the extremes of the tuning code, with a maximum deviation of 200 kHz.

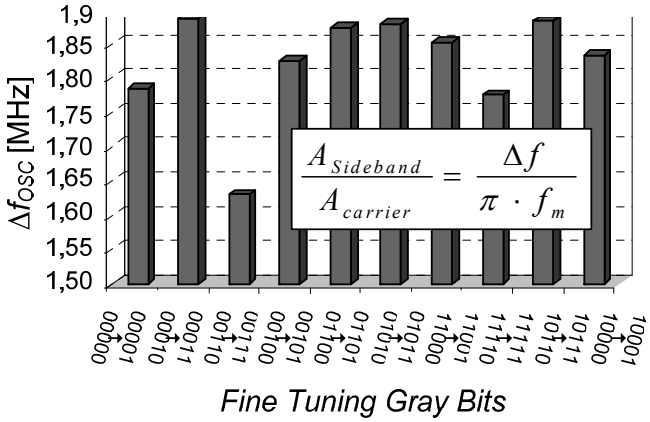

Figure 2.28: Fine-tuning frequency step measurements results

The measured phase noise at the center of the tuning range is reported in Fig. 2.29. The phase noise at 10-MHz offset from the carrier results -116.5 dBc/Hz and remains substantially flat over the tuning range.

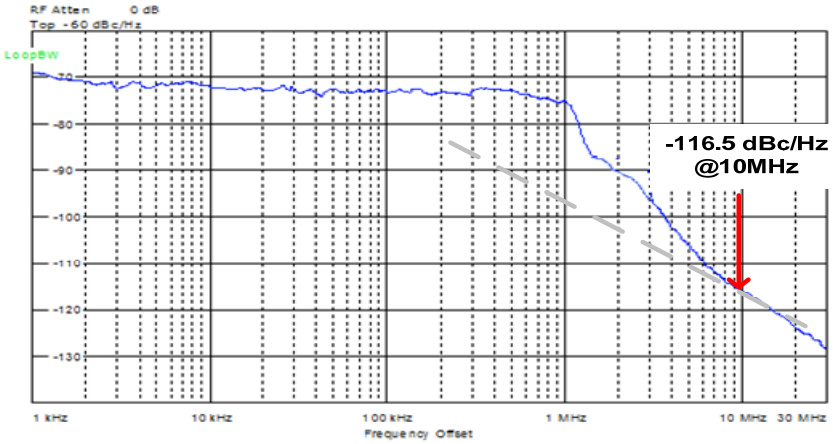

Figure 2.29: Measured phase noise at 52.45GHz oscillation frequency

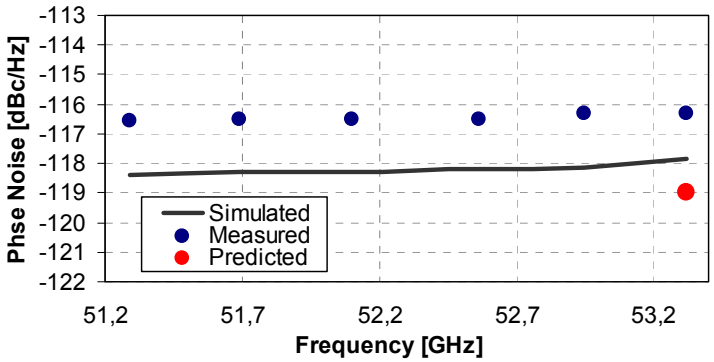

Figure 2.30: Measured, simulated and predicted DCO phase noise

The DCO core consumes 2.34 mW, when operated with a 1.2 V supply and presents a figure-of-merit (FoM) of -187.2 dBc/Hz, which compares favorably with other LC oscillators operating in this frequency range. In Fig. 2.31 the FoM of the proposed DCO is compared with other published LC-tank and standing-wave oscillators (SWO) operating in the mm-wave frequency range.

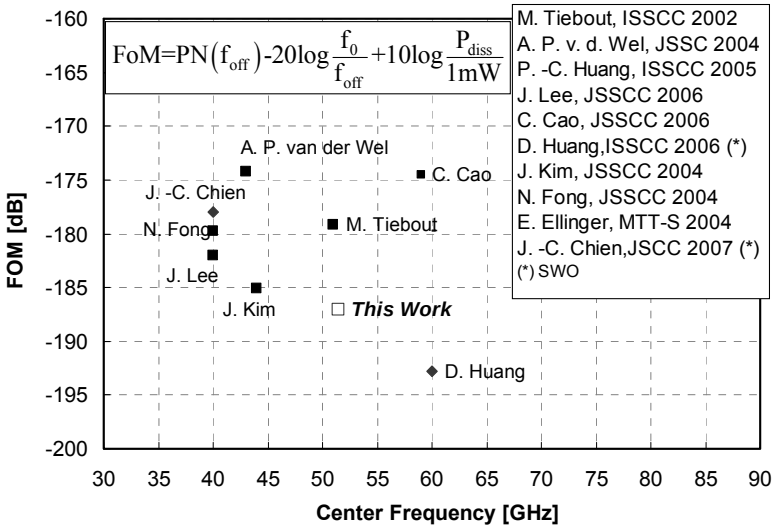

Figure 2.31: Millimeter-wave oscillators *FoM* comparison

2.3 Standing-wave voltage controlled oscillator

As said in section 2.1.6, at 60GHz, the electrical wavelength λ is approximately 2.5mm, and transmission lines offer a viable alternative for the realization of passive elements.

Transmission lines are capable of realizing precise values of small reactance, are inherently scalable in length and the well-defined ground return path significantly reduces magnetic and electric field coupling to adjacent structures. Their lower sensitivity to substrate interference also reduces the important problem of oscillator pulling.

A 71.5-73.5GHz standing wave oscillator based on a shorted λ/4 transmission line has been designed, implemented and characterized [22]. The silicon technology used is the same TSMC 90mn used for the DCO implementation.

It must be noted that the initial aim was to design an oscillator working around 60GHz, but for causes that will be explained in the final paragraphs of this section, the measured SWO center oscillation frequency is about 72.5GHz. The oscillator tuning range covers part of the 71-76GHz band, known as E-band which is used, together with the 81-86GHz and 92-95GHz bands, for point-to-point high-bandwidth communication link.

2.3.1 Transmission line resonator

It is well known that a transmission line terminated with a short circuit or with an open circuit behaves like a resonator.
For instance, a parallel type of resonance can be achieved using a short-circuited transmission line that has an electrical length of λ/4 at the desired oscillation frequency. At the resonance, the line behaves as a parallel LC tank with:

$$R_{tank} = \frac{Z_0}{\alpha l} = \frac{4QZ_0}{\pi} \quad C_{tank} = \frac{\pi}{4\omega_0 Z_0} \quad L_{tank} = \frac{1}{\omega_0^2 C_{tank}} \tag{2.44}$$

The quality factor (Q) is a function of the propagation coefficient (β) and of the attenuation per unit-length (α):

$$Q = \omega_0 R_{\text{tank}} C_{\text{tank}} = \frac{\pi}{4\alpha l} \underset{\substack{l=\pi/2\beta \\ \text{at resonance}}}{=} \frac{\beta}{2\alpha} \tag{2.45}$$

The differential transmission line is here implemented in the form of a differential coplanar strip-line (CPS) as shown in Fig. 2.32, on the top metal layer M_6.

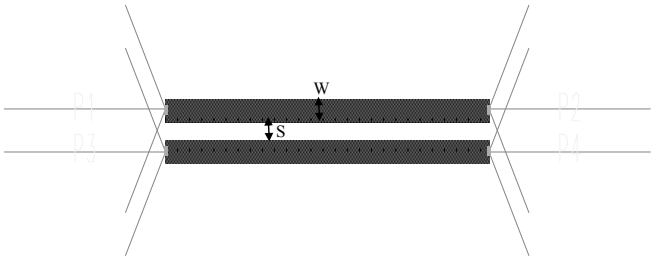

Figure 2.32: Overhead view of an integrated coplanar strip-line

The line parameters can be extracted from the simulated S-parameters as obtained by the EM solver (*Agilent Momentum*).
By recalling that the ABCD representation of a transmission line with propagation constant γ and characteristic impedance Z_0 is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh \gamma l & Z_0 \sinh \gamma l \\ \dfrac{\sinh \gamma l}{Z_0} & \cosh \gamma l \end{bmatrix} \tag{2.46}$$

the parameters of interest (i.e., odd mode propagation constant[1], differential impedance and multi-section differential RLGC parameters per unit-length) can be calculated as [23]:

[1] $\operatorname{arccos h}(x) = \ln\left(x + \sqrt{x^2 - 1}\right)$

$$\gamma = \frac{1}{l}\left[\ln\left(A+\sqrt{A^2-1}\right)\right]$$
$$Z_0 = \sqrt{\frac{B}{C}} \qquad [\Omega]$$
$$\alpha = \mathrm{Re}[\gamma] \qquad [Neper/m]$$
$$\beta = \mathrm{Im}[\gamma] \qquad [Radian/m] \tag{2.47}$$
$$R = \mathrm{Re}[\gamma \cdot Z] \quad [\Omega/m]$$
$$L = \frac{\mathrm{Im}[\gamma \cdot Z]}{2\pi f} \quad [H/m]$$
$$G = \mathrm{Re}[\gamma/Z] \quad [S/m]$$
$$C = \frac{\mathrm{Im}[\gamma/Z]}{2\pi f} \quad [F/m]$$

The transformation from s- to ABCD-parameters has been done using standard textbook formulas. The R,L,G and C values extracted can be used to build the familiar multi-sectional equivalent model in order to use the line even in time domain circuit simulations (Fig. 2.33).

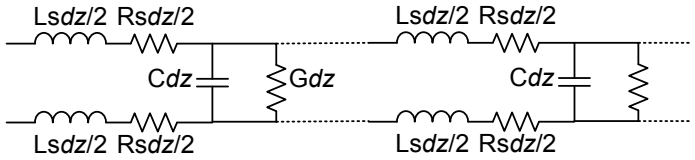

Figure 2.33: differential RLCG model of the coplanar strip-line

To find the optimal topology for the CPS, the metal width (W) and separation (S) are swept between 2µm and 60µm and 5µm and 30µm, respectively. The line length is kept constant and equal to 100µm. The results of Momentum simulations are given in Fig. 2.34.

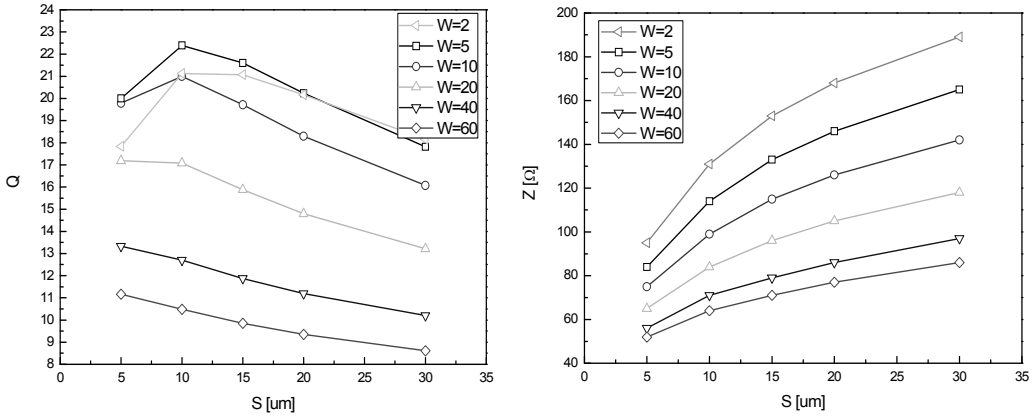

Figure 2.34: Quality-factor and differential impedance of the T-line

The highest quality factor (≈22.4) is achieved with a line width of 5μm and a conductors spacing of 10μm. This is somehow expected due to the combined effect of skin and proximity effects and silicon substrate conductivity (10 S/m). Indeed, at such high frequencies, the effective cross section is strongly limited by the skin effect thus canceling the benefits of increasing the line width for lowering series losses. Increasing the line width only results in an increase of shunt losses with a consequent reduction of the quality factor.
The quality factor of the CPS has been improved by shielding the transmission line by means of floating metal strips located underneath the guiding structure realized on the lowest metal layer M_1 [14] (Fig. 2.35). The distance between two consecutive bars has been set to 1μm in order to minimize the field penetration.
Shielding the resonator from the underlying substrate has two beneficial effects. Primarily, the shunt losses are virtually eliminated thus enhancing the quality factor of the transmission line. Secondly, the effective zero potential plane causes the separation of the electric and magnetic energies that results in slow-wave propagation [24]. This is because, while the magnetic fields permeate the entire substrate, the electric fields are virtually stopped at the floating bars boundary so that the transmission line inherits a capacitance in accordance with the small distance between the trace and the bar. The complete penetration of magnetic fields implies that the inductance is not expected to change while the shunt capacitance is increased resulting in a reduced velocity of signal propagation. The reduction of the signal velocity makes possible to achieve the same phase shift of an unshielded structure but with a reduced line length.

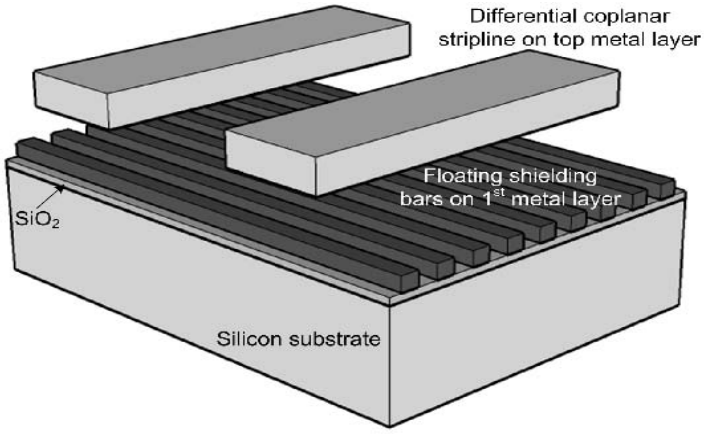

Figure 2.35: Shielded CPS principle

In Fig. 2.36, the characteristics of the shielded CPSs are presented. Interestingly, the structure that, for the unshielded line, achieved the lowest Q is now the one with the better performances. This can be explained by inspecting the values of the RLGC lumped model, in particular the shunt loss element G_p. In an unshielded structure, the presence of the semi-conductive substrate makes large stripes correspond to large values of G_p. For those

structure, the electric quality factor is much lower than the magnetic one so that the overall Q is low.

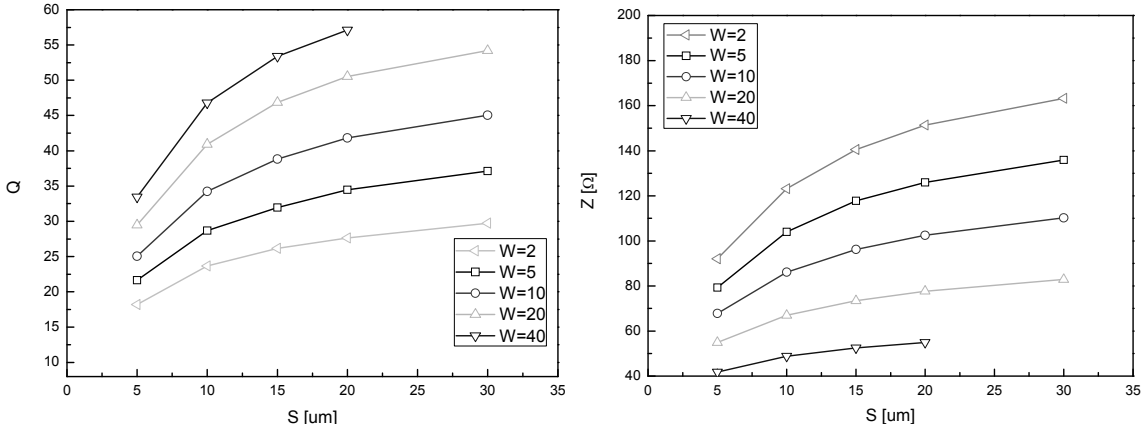

Figure 2.36: Quality-factor and differential impedance of the shielded T-line

When shielding is present, the substrate is practically electrically isolated and shunt losses are determinate by the silicon oxide losses, that are some order of magnitude lower than silicon ones. Lower shunt losses directly results into higher electrical Q making the parallel of the singular Q equal to the magnetic one.

The width (W) and spacing (S) of the CPS have been initially chosen aiming for the maximum Q. The quality factor increases as the lines separation and width increase; in fact, as the spacing increases, the magnetic quality factor increases due to higher inductance per unit-length, while resistive losses are reduced using wider lines. The presence of the bars is essential to achieve this behavior since it strongly reduces substrate-related electric losses, that, has already described, would be dominant at 70GHz.

Concerning the characteristic impedance, increasing the line separation S, for a given width, will increase the line impedance until it will saturate when two lines are far enough to neglect the mutual electric and magnetic coupling.

The shielding bars have also been exploited to control the resonant frequency by means of varactors that periodically load the original CPS: as shown in Fig.2.37 the gate of each varactor is connected to the signal line through a vertical metal via stack, while the source and drain are connected to each bar and to a control signal.

The equivalent circuit of a unit-cell of the CPS is shown in Fig 2.37c, where R,L,C and G are the equivalent circuit elements of the unloaded line and C_{var} represent the variable capacitors. The variable MOS capacitance alters the phase propagation velocity and hence the resonant frequency. The relation between resonance frequency and the loading capacitance, for N_{cell} cascaded unit-cells, is given by:

$$f_{osc} = \frac{v_p}{4l} = \frac{1}{4 \cdot N_{cell} \cdot d \cdot \sqrt{L \cdot \left(C + C_{\text{var}}\right)}} \qquad (2.48)$$

while the phase shift of a unit cell is given by:

$$\delta\phi = 2\pi f \sqrt{L \cdot \left(C + \frac{C_{\text{var}}}{d} \right)} d \tag{2.49}$$

where L and C are the inductance and capacitance per unit-length of the unloaded CPS, $l=Nd$ is the total line length and d is the size of each cell, 2μm in this design.

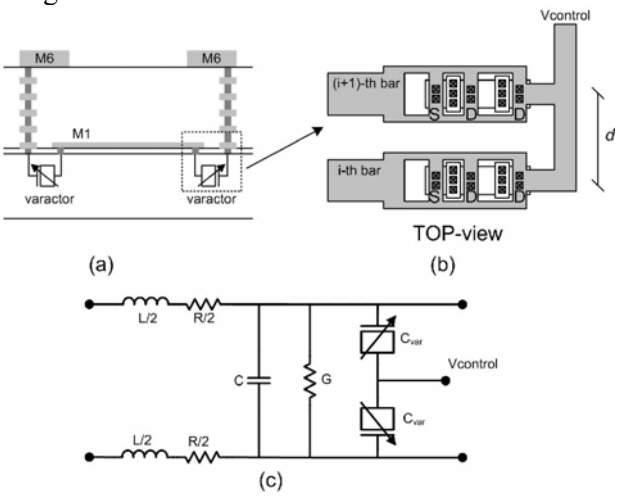

Figure 2.37: (a) Cross-section of a shielded CPS periodically loaded with varactors. (b) Top view of the varactor area. (c) Equivalent circuit of a CPS unit cell.

For a varactor-loaded transmission line it is possible to define two useful parameters, namely the capacitance loading factor (x_C) and the capacitance ratio (y), which are defined as:

$$x_C = \frac{C_{\text{var}}^{\max}}{d}$$
$$y = \frac{C_{\text{var}}^{\min}}{C_{\text{var}}^{\max}} \tag{2.50}$$

where $C_{\text{var}}^{\min}$ and $C_{\text{var}}^{\max}$ are the minimum and maximum variable capacitance in each cell.

By equating the phase shift of the unit section at the minimum and maximum resonance frequencies, it is possible to express the frequency ratio f (f_{max}/f_{min}) as a function of the capacitance ratio and loading factor:

$$f \approx \sqrt{\frac{1+x_C}{1+x_C \cdot y}} \tag{2.51}$$

Once x_C is calculated from (2.51), the length of the line can be calculated as[2]:

[2] The distance between consecutive floating shielding bars, and then the points where varactors can be connected is fixed and d can be assumed constant and equal to 2 μm.

$$l = N_{cells} \cdot d \tag{2.52}$$

where N_{cells} is the number of unit cells that are required for a phase shift of $\pi/2$:

$$N_{cells} = \frac{\pi}{2 \cdot \delta\phi_{\min}},\ \delta\phi_{\min} = 2\pi f_{\min} d\sqrt{L_{\min} C_{\min}}\sqrt{1+x_C} \tag{2.53}$$

The derived calculation can effectively capture the phase-shifting nature of a generic loaded TL, but it does not account for other effects that are unavoidably present when the resonator is used into the oscillator: for example, the presence of the MOS capacitance at one of the terminations demands a line shortening. Fig.2.38 illustrates this concept.

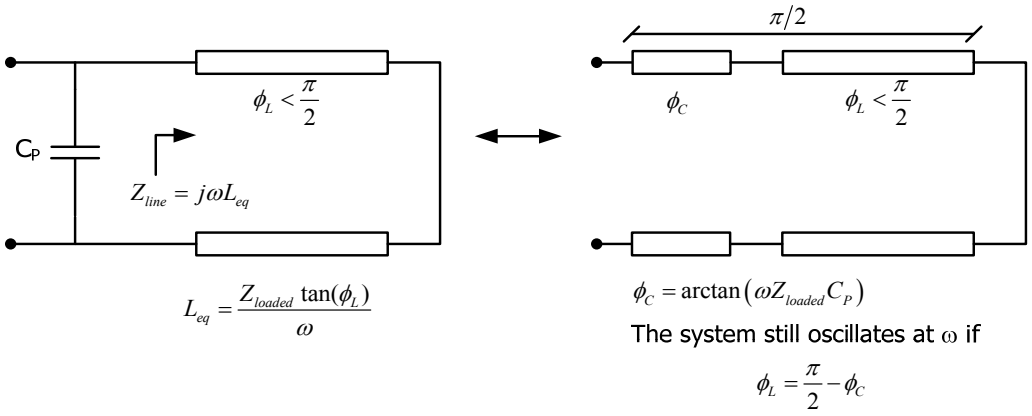

Figure 2.38: effects of termination

The value of x_C that fulfills the tuning range condition can be obtained by numerically solving this new tuning range condition:

$$\Phi \cdot f \approx \sqrt{\frac{1+x_C}{1+yx_C}} \quad \Phi \triangleq \frac{1-\frac{2}{\pi}\Phi_C\left(f_{\min}\right)}{1-\frac{2}{\pi}\Phi_C\left(f_{\max}\right)} \tag{2.54}$$

where Φ_C represents the additional equivalent phase shift caused by the MOS loading.

The varactors were realized as NMOS transistors: having the gate biased around V_{DD}, the source and drain terminals tied together to the control voltage and the bulk connected to ground, the NMOS transistors operates as inversion-mode varactors [25].

When the line is loaded by MOS varactors, their finite Q will impact the overall quality factor of the resonator. This is because, while the magnetic quality factor is not affected by the varactor loading, the electrical one is dominated by it, resulting into a lower quality factor of the overall structure.

Furthermore, the characteristic impedance of the loaded CPS decreases according to the following relation:

$$Z_L = \sqrt{\frac{L}{C + \frac{C_{\text{var}}}{d}}} = \frac{Z_{unloaded}}{\sqrt{1 + \frac{C_{\text{var}}}{C \cdot d}}} \tag{2.55}$$

Hence, for a given desired characteristic impedance, a smaller line width must be selected, further reducing the overall Q. The selected line dimensions, i.e., W=5um and S=30um, were chosen to obtain the desired loaded impedance and the optimum loaded Q (about 16). A higher quality factor is expected if accumulation-mode varactors are used instead of NMOS transistors.

2.3.2 Standing-wave oscillator design

In Fig. 2.39a the oscillator schematic is reported. The resonator was implemented using the CPS described above. The necessary bias voltage for the oscillator is provided from the middle of the CPS short-circuit terminations, that is a differential zero-voltage point. Notice that the parasitic capacitance of the cross-connected couple and the non-zero length of the short-circuit termination effectively resulted into a shortening of the CPS with respect to the ideal length of $\lambda/4$. The circuit is operated with V_{DD}=1.2 V and the control voltage varies between 0 and V_{DD}. The transistor channel length is equal to the minimum allowed by the technology (i.e., 100 nm) while the width has been chosen from circuit simulation aiming for the maximum f_{MAX} and it has been found to correspond to 2μm.
Circuit co-simulations in the Agilent ADS environment of the whole oscillator made of the CPS resonator, the varactors and the two cross-coupled connected MOS transistors (M_1 and M_2, in Fig.2.39a), together with the analytical approach based on eq.2.52-2.54 have been used to size the varactors, the number of fingers of the transistors and the CPS length to meet center frequency and tuning range requirements. The final result of the analysis is 24 unit-cells (that gives an overall CPS length of only 48μm), inversion-mode NMOS varactors with W=6 X 1μm, L=0.165μm and transistors with W=8 X 2μm.

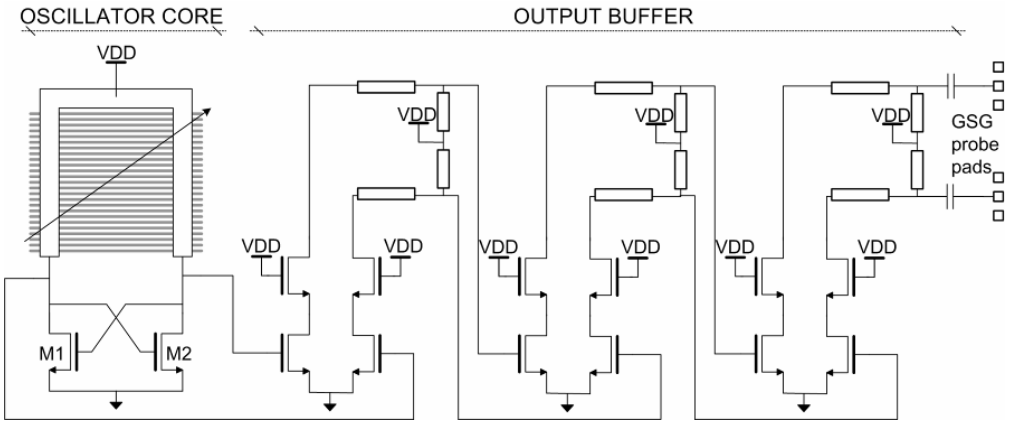

Figure 2.39: Voltage-controlled standing-wave oscillator principle and output buffer schematic.

In order to provide enough output power and to avoid loading the oscillator core directly with the RF probes, the same buffer used for the DCO testing (Fig. 2.39b) consisting of three cascaded differential amplifiers with

transmission line inter-stage matching networks has been included. The first stage of the buffer has been sized aiming for a maximum capacitive load for the oscillator equal to 10fF, while the intermediate and the last stage dimensions are optimized for maximum output power.

2.3.3 Experimental results

A test chip for the SWO has been designed and implemented in TSMC90nm CMOS process with ultra-thick top metal. A die micrograph is given in Fig. 2.40. It looks nearly the same die micrograph of the DCO described in the previous section. This is because the two cores have nearly the same size, much lower compared with that of the output buffer (the same for the two oscillator) used for characterization purposes. Also in this case, bias and control pads are located on the top while the two outputs, that are suitable for on-chip measurement with coplanar GSG probes, are in the middle. The chip measures 1078 X 780 μm^2. A close-up view of the oscillator core is also given: the effective circuit area is here only 120 X 80 μm^2.

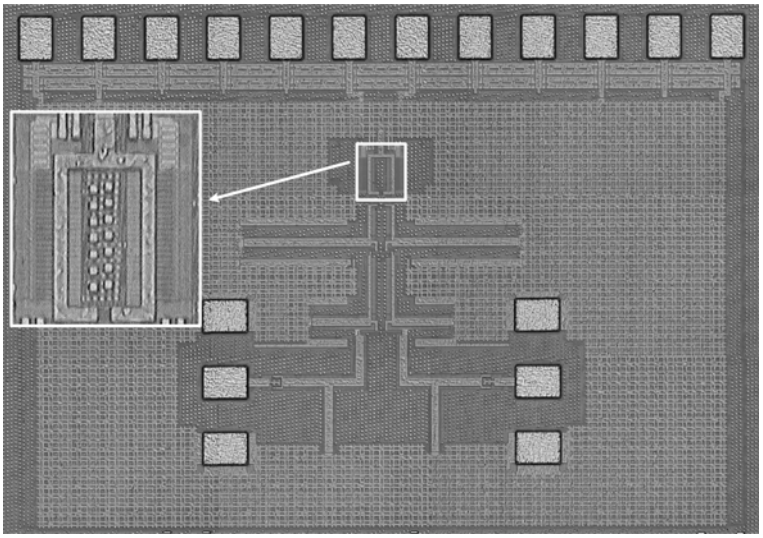

Figure 2.40: Die photo of the test chip in 90nm CMOS

The measurement setup realized for the oscillator characterization is reported in Fig. 2.41.
The outgoing signal from the probes is first down-converted by means of a Wisewave V-band mixer with a 70 GHz LO provided by an Agilent E8527D generator. Then, a second down-conversion feeds the signal to the same low-frequency custom-made amplifying board used to test the DCO, that consists of two commercially available low-noise op-amps with bias and stabilization networks.
Also in this case, the board was found to be necessary since the output buffer did not provide the expected power for an accurate characterization due to cable and down-conversion mixer losses. The phase noise and the tuning curves are finally measured by the R&S FSUP signal analyzer.

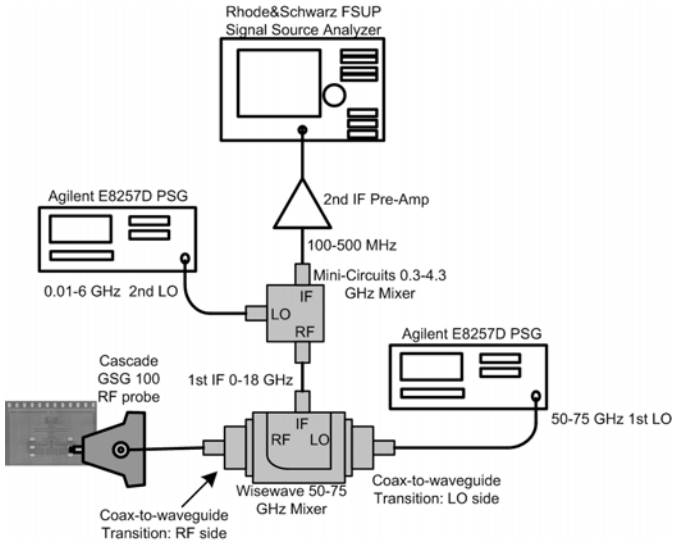

Figure 2.41: Experimental setup for the VCO characterization

The oscillation frequency as a function of the control voltage is given in Fig. 2.42.

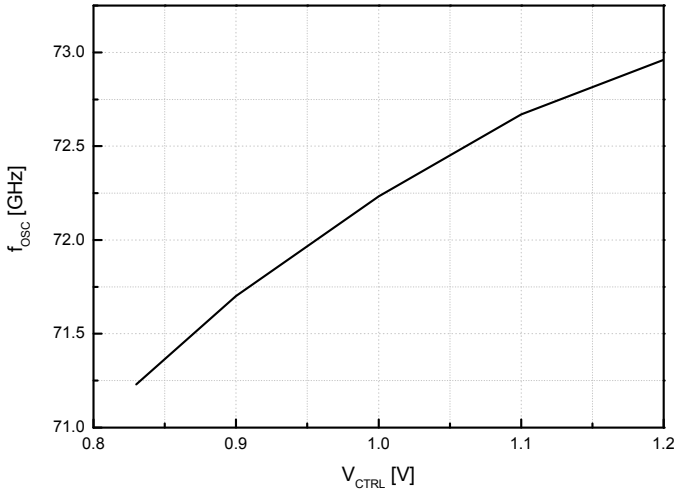

Figure 2.42: Measured oscillation frequency versus tuning voltage

As already said, the target was to obtain a tuning range of nearly 7GHz around 60GHz, but the measured tuning range results of about 2GHz around 71.5GHz. Analysis post-characterization have shown that this discrepancy is due to excessive and not predicted losses of the varactors when operated in maximum capacitance mode; these high frequency not predicted losses result in a lower varactor Q and lower oscillation amplitude. This, combined with large signal operation effects reduces the capacitance ratio and the effective loading factor, as described in Fig.2.43: the voltage amplitude along the line is not constant ranging from a maximum at the active couple nodes to a minimum in proximity of the end of the line and this non-uniformity affects the effective varactor capacitance along the line so that the oscillation

frequency becomes different from the resonance frequency of the original loaded line.
In order to account for high-frequency losses, a lumped resistance (R) has been added in series with the gate of the library varactor model.
The oscillation frequency has been simulated as a function of the control voltage for different loss resistances R.
Fig. 2.44 shows that adding a series resistance of nearly 100Ω simulations and measures agree.

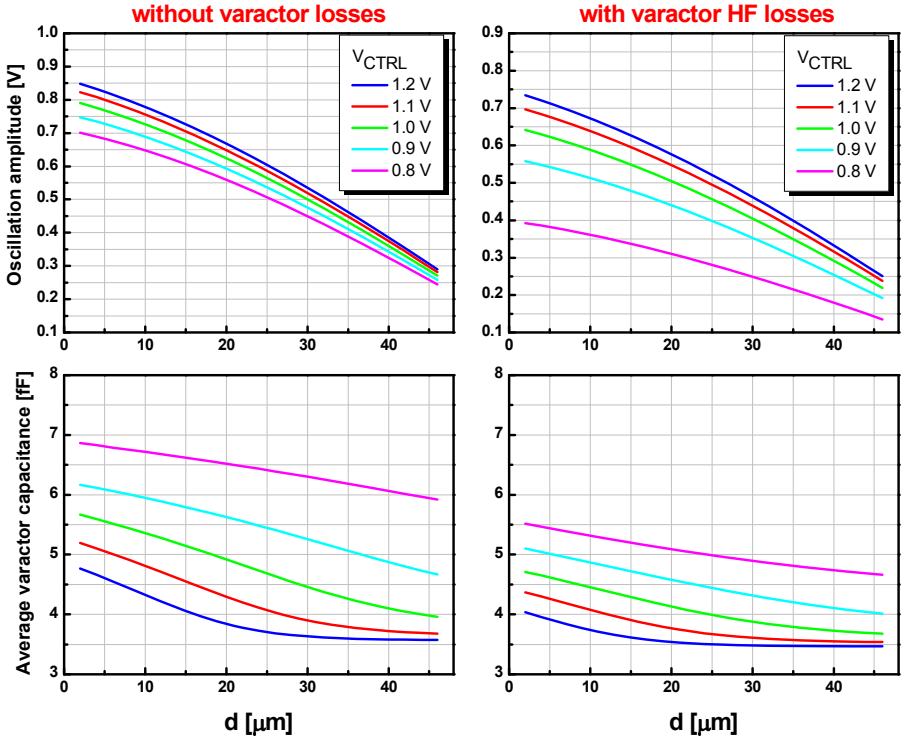

Figure 2.43: combined effect of large signal operation and lower varactor Q

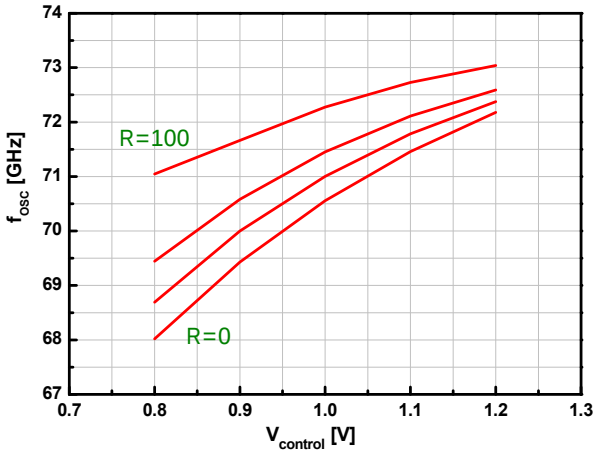

Figure 2.44: f_{osc} vs $V_{control}$ for different R values

For a center frequency of 72GHz, the measured phase noise log plot is given in Fig. 2.45.

In Table 2.2, the designed SWO is compared to some published VCO that operates in the similar frequency range by using as a metric the same FOM used for DCO performances comparison.

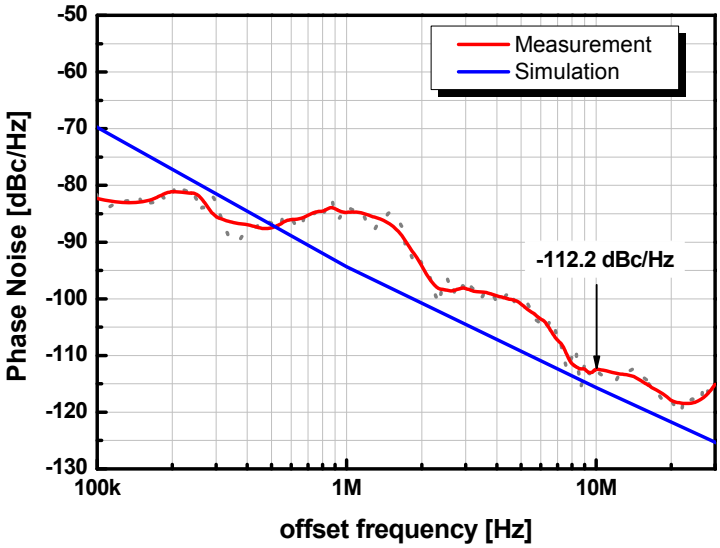

Figure 2.45: Measured phase noise for 72GHz oscillation

VCO [ref]	f0 [GHz]	PN [dBc/Hz]	Pdiss [mW]	FoM [dBc/Hz]
Kim [5]	**70.2**	**-106.14 @ 10 MHz**	**5.4**	**-175.7**
Makon [6]	**74**	**-97@ 1 MHz**	**770**	**-165.5**
Li [7]	**72**	**-102.5@ 1MHz**	**290**	**-175**
This work	72	-112.18@ 10 MHz	19.2	-176.5

Table 2.2: comparison with published I-band VCOs

The VCO core consumes 19mW when operated with a 1.2 V supply and presents s *FoM* of -176.5dBc/Hz.

Conclusions

High performances oscillators operating in the mm-wave range continue to pose difficult challenges even today. In these chapter, after a brief introduction on VCOs fundamentals (VCOs principle, phase noise theory and types of VCOs), have been listed and analyzed the main challenges in designing a mm-W VCO.
Has been shown that one of the major shortcomings in the implementation of millimeter-waves frequencies oscillators is the low quality factor of the capacitors, that usually dominates the overall Q of the resonator. This problem has be addressed in the 53GHz lumped LC DCO described in the second section, by segmenting the capacitor bank into three sections, implemented with different structures. Tuning range and Q are the primary

drivers for the coarse tuning bank, while small minimum capacitance step is the main requirement for the fine tuning bank.
In the voltage controlled 71-73GHz SWO presented in the last section, the problem of low capacitive quality factor has been instead addressed using, as a resonator, a short-circuited λ/4 shielded differential coplanar strip-line. Shielding, by preventing the electric field form penetrating into the substrate, allows to improve the resonator Q. The line is periodically loaded with varactors, to obtain the desired tuning.
The size of the two oscillators cores is nearly the same. The DCO has a measured phase noise of -116.5dBc/Hz and consumes 2.34mW, resulting in a figure of merit of -187.2 dBc/Hz, which compares favorably with the SWO, that presents instead a *FoM* of -176.5dBc/Hz.
However the two oscillators were designed with different active devices and varactors, hence a definitive comparison between the two approaches cannot be derived.

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_____Chapter III_____

Design and characterization of a millimeter wave low-noise amplifier

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3.1 60GHz Low-Noise Amplifiers: what's different?
Transistors closer to cutoff – Passives performances, distributed effects and parasitic at 60GHz – Substrate coupling and dummies effects.
3.2 60GHz LNA architectural approaches
Inductive source degeneration principle – Is cascode a good choice at 60GHz? – Millimeter wave state of the art.
3.3 Analytical study for noise figure minimization
Noise figure minimization for a simple MOS device – Noise figure minimization for the inductive source degeneration stage.
3.4 mm-wave LNA design and characterization
The LNA design– The LNA characterization.

Conclusions

Power gain, noise figure, linearity, stability, impedance matching and power dissipation are universal requirements for LNAs and are still valid in the mm-wave frequency band. The basic design methodologies at 60 GHz are not all that different than those at much lower frequencies, but the used circuit topologies are different to account for the fundamental differences of 60 GHz design compared to lower frequency design.
The operating frequencies much closer to transistors cutoff (lower gain and higher noise), the presence of signals with small wavelengths resulting in distributed effects within actual components of the circuit, the strong parasitics and dummies effects and finally the problems related to strong substrate coupling are some of the most important challenges in the 60GHz LNA design.
The topologies most widely used in the design of mm-wave low noise amplifiers are the simple common source stage usually degenerated through a source series inductance whose presence is rarely explicit but always intrinsically connected to the circuit physical implementation and the cascode solution.

In our design the inductive source degeneration topology is chosen for each LNA stage since it represents an excellent solution to obtain at the same time good noise performances and a satisfactory input impedance matching.
Furthermore, the analytical noise study performed starting from the generic two-port microwave network noise analysis and extended to the source inductive degeneration stage allows us to make the noise minimization task practically independent from the impedance matching requirements.
Instability is prevented, in our design, by adopting a differential topology which, besides being less susceptible to parasitic feedback loops, is more robust to common-mode noise.
The input and output pad capacitances are exploited for the matching of the LNA input and output to 50Ω so that pad de-embedding is not required during measurements.
Matching networks are designed taking into account losses, bandwidth and physical implementation criteria.
For all networks an "hybrid" approach is adopted: both spiral inductors and transmission lines are massively used, mainly because T-lines arise naturally from inductors interconnect, but also in order to exploit the advantages of both approaches.
In the first section of this chapter 60GHz LNA challenges are discussed and in the second sections are described the most widely used circuital topologies analysing, for each solution, advantages and drawbacks.
In the third section the analytical theory for LNA noise minimization is reported and in the last section the LNA design and its characterization are described.

3.1 60GHz Low-Noise amplifiers: what's different?

The fundamental goal of a low-noise amplifier (LNA) is to provide gain to the input signal, while adding very little noise. Since the LNA is the first gain stage in a receiver path, its noise figure dominants that of the overall system. Afterwards the subsequent receiver stages add noise to an already amplified signal, leading to a much better signal-to-noise ratio that an un-amplified signal.

The key performance requirements of the 60GHz low-noise amplifier (LNA) are power gain, noise figure, linearity, stability, impedance matching, power dissipation, bandwidth, and design robustness to process/voltage/temperature variations. These basic requirements are universal for LNAs, and as will be shown, the basic design methodologies at 60 GHz are not all that different than those at much lower frequencies. The circuit topologies, however, will be different to account for the fundamental differences of 60 GHz design compared to lower frequency design, which are (1) designing using transistors operating much closer to their cutoff frequencies, (2) operating with signals with small wavelengths resulting in distributed effects within actual components of the circuit, (3) designing with parasitic elements which represent a much larger portion of the total admittance or impedance on a given node, (4) designing considering the effects of substrate coupling and of dummies [1].

3.1.1 Transistors closer to cutoff

Achieving good performances for a mm-W LNA is non-trivial since operating the CMOS devices at frequencies close to the transistors' f_t values reduces their intrinsic gain and increases their noise factor. The necessity of employing nanoscale technologies to achieve the desired operation at mm-waves leads to reduced supply voltage and hence, limited headroom and linearity. Lower intrinsic gain also decreases the margin for modeling errors and requires careful prediction of device characteristics.

Furthermore the actual active device performance is highly layout dependent: extrinsic parasitic such as gate, source and substrate resistance and feedback capacitance are the ultimate factors in determining the maximum frequency of activity (f_{max}).

A useful way to estimate *the maximum available power* gain G_{MAG} is based on the definition of f_{MAX}:

$$G_{MAG} \approx 20 \cdot \log\left(\frac{f_{MAX}}{f_0}\right) \tag{1}$$

where f_0 is the operating frequency and f_{MAX} is the unity power-gain frequency. Note that this is valid only near cut-off where the available power gain in the transistor is equal to the *maximum available g*ain. At lower frequencies, the transistor has enough gain to be potentially unstable; thus, the suitable power-gain metric is the *maximum stable gain* (*MSG*) which no longer has the 20db/dec slope. As an example, a transistor with an f_{MAX} of 240 GHz should have a G_{MAG} of approximately 12 dB at 60GHz.

As a result of the lower available gain per transistor, multi-stage topologies are likely required to provide enough gain to suitably deemphasize the noise contribution from the mixer and subsequent stages. Multi-stage amplifiers consumes more power and area, have poorer linearity, and have more internal nodes that require stability checks. Reduced transistor gain means also less margin for process/temperature/voltage variations; using wideband matching networks provides more stability in the face of process and corner variations and more predictable performance especially for narrowband design techniques.

As already mentioned, operating the CMOS devices at frequencies close to the transistors' f_t values increases their noise factor as can be easily understood by observing equations 2 and 3, which show the minimum noise figure of a simple MOS transistor as a function of the operating frequency and the deviation from this minimum caused by a deviation of 50% from the optimum noise impedance Z_{opt} (3).

$$NF_{MIN} \cong 1 + 0.94 \cdot \frac{\omega_0}{\omega_t} \tag{2}$$

$$NF_{DEV} \cong F_{MIN} + 0.75 \cdot \frac{\omega_0}{\omega_t} \tag{3}$$

Increasing the operating frequency not only the achievable minimum noise figure increases, but there is also an increasingly large deviation from this

minimum for a constant impedance deviation from the optimum noise impedance: this imposes at 60GHz the need to get as close as possible to this minimum.

To obtain good performances the LNA design should provide simultaneous noise and impedance matching; failing to make the noise match and power match coincident results in either sub-optimal input return loss or sub-optimal noise figure. Noise figure calculations which directly compute F for a 50Ω source obscure the existence and relevance of Z_{opt} and hide the fundament trade-off which exists between noise and power matching.

3.1.2 Passives performances, distributed effects and parasitics at 60GHz

For deeply scaled processes with cutoff frequencies close to or beyond 100GHz, the performance of the passive elements plays a very crucial role in the achievable gain and BW; the poor quality factors of passive elements at 60 GHz limit the performances of the active devices and the difficulty in accurately modeling all the physical phenomena that affect their intrinsic behavior, such as substrate coupling and skin effect, and the interconnecting lines behavior makes it extremely difficult to predict the actual circuit performances.

Millimeter-wave passive models for CMOS components are not readily available. Therefore, extensive electromagnetic simulations must be performed on inductors, t-lines, capacitors and every single interconnection in order to create sufficiently reliable circuital equivalent models.

It should be emphasized that accurate electromagnetic simulations on complex structures requires too high computational tasks and it is necessary to make some simplifications or to separate them into sub-structures separately simulated. As will be discussed in Section 3.3.1, measurements on the single pad structure have shown that these simplifications lead to inaccuracies that are unacceptable.

Distributed effects must also be considered in the design of passives when the wavelength of the operation frequency becomes comparable with the dimensions of the on-chip structures; one implication of the distributed regime is that any interconnect within the circuit which is an appreciable size of a wavelength should be treated as a transmission line and accurately modeled. Transmission lines, therefore, become a very important elements in the entire millimeter-wave portion of the radio, as they are used as both interconnects and to realize passive components. A final implication (or benefits, actually) of operating in the distributed regime is that many traditional microwave structures now become viable on-chip; thus, the 60 GHz circuit designer has a wider pallet of devices at his disposal, each with certain trade-off.

3.1.3 Substrate coupling and dummies effects

A major challenge posed to mm-wave design in silicon is that crosstalk and coupling between high frequency components can be significant due to the semi-resistive substrate. Substrate coupling not only makes difficult to

accurately model and predict the behavior of passives, but it could also easily lead to the LNA instability.

To prevent this potential instability designers often use cascode stages or adopt a differential topology which makes the LNA less susceptible to parasitic feedback loops formed through the ground or bias paths because of the semi-resistive substrate.

In most nano-scale CMOS processes, layouts are subject to strict pattern density rules to ensure density of layout patterns stays within a certain range for each metal layer.

If the measured densities are too low (or too high), metal fillers (or holes) with predefined shapes are automatically generated [2], until no density violation is detected. This alter passive elements characteristics, especially at higher frequencies, thus interfering with the design and modeling of passive devices.

For the sake of modeling accuracy at 60GHz, it is highly desirable to *prefill* all metal layers around inductors or t-lines. Using a sufficiently dense array of small fillers and holes can prevent further density enforcement (which is beyond circuit designer's control), thus guaranteeing design repeatability. Such dummies prefillers can be an array of lines or squares and must be sufficiently small (compared to the t-line or inductor size) in order to minimize image currents and granularity effects. These dummies should also be placed as far as possible from the device, and possibly not below the signal line.

The effect of these layers on some differential coplanar transmission lines (widely used for our LNA design) has been tested through electromagnetic simulations: long dummies parallel to the signal lines has been placed and simulated (Figure 3.1), revealing that both the quality factor Q and the characteristic impedance Z_0 suffer non negligible changes (even 10%) due to the presence of dummies. This dummies in fact induce significant image currents, thus decreasing the line inductance and increasing line losses.

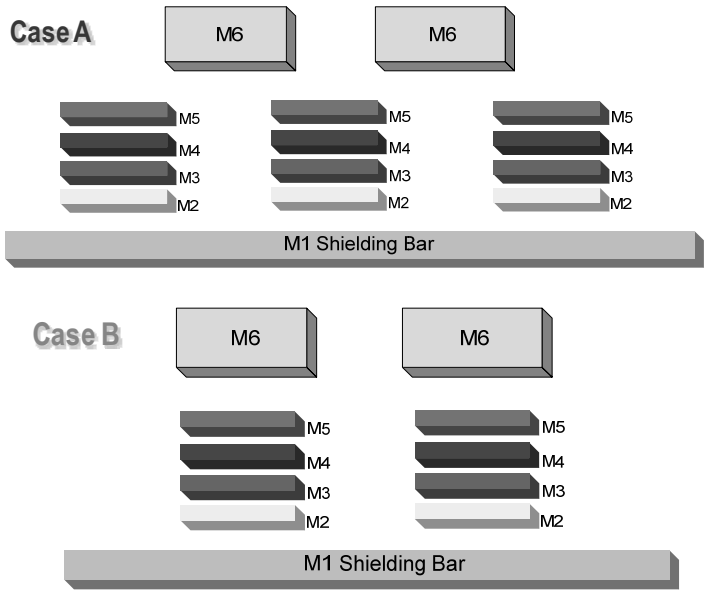


Figure 3.1: dummies effects on T-lines

Diff T-line W=2µm S=28µm	$Z_{0\text{-}DIFF}$[Ω]	Q	θe [deg]
Nominal Value	129	11,6	8,0
Case A	120	8,6	9,4
Case B	124,6	10,1	8,8

Table 3.2: dummies effects on T-lines

As will be widely discussed later, t-lines periodic shielding (slow-wave effect) not only allows to improve the t-lines performances, but can also be exploited in order to cover the required metal densities below the signal line, without requiring for an additional post-design dummies placement.

3.2 60GHz LNA architectural approaches

The topologies most widely used in the design of low noise amplifiers are the common gate and the common source stages both of them with or without cascade loads.

At millimeter wave frequencies **common gate** amplifiers are seen much less frequently despite the fact that they provide an active broadband input impedance match. The downside of the common gate amplifier is much lower power gain and much higher noise which make them not much attractive at 60 GHz. Intuitively, the full drain noise flows into the input circuit without attenuation due to the unity current gain and, under the input match condition, $1/g_m = R_S$, the drain current contributes nearly equal noise to the output as the source.

The constraint that the input matching requires on the transconductance value inevitably sets also a constraint on the overall LNA transconductance gain G_m:

$$G_m = \frac{g_m}{1 + g_m \cdot R_S} = \frac{1}{2} \cdot g_m = \frac{1}{2 \cdot R_S} \tag{4}$$

and on the noise factor given by [1][2]:

$$F = 1 + \frac{\gamma}{\alpha} \tag{5}$$

where γ is the coefficient of channel thermal noise and α is given by:

$$\alpha \triangleq \frac{g_m}{g_{d0}} \tag{6}$$

For long channel devices α=1 and γ=2/3, while for short channel devices γ can be much greater than 1 and α can be much less than 1: accordingly, the minimum theoretical noise figure tend to be around 3dB or greater in practice and there is no way to reduce it unless noise-cancelling techniques are adopted.

A more attractive and widely used solution at mm-wave frequencies is to employ inductive source degeneration, which is discussed in the next section.

3.2.1 Inductive source degeneration principle

In Figure 3.2 the inductive source degenerated stage is shown: an inductance L_s is placed between the source terminal and ground to provide the narrowband circuit behavior, while the gate series inductance has the exclusive function of cancelling the imaginary part of the input impedance and of setting the resonance frequency once L_s is chosen to satisfy the matching criterion [3],[4].
A simple analysis of the input impedance shows that:

$$Z_{IN} = \frac{1}{C_{gs}} + s \cdot \left(L_s + L_g \right) + \omega_T \cdot L_s \tag{7}$$

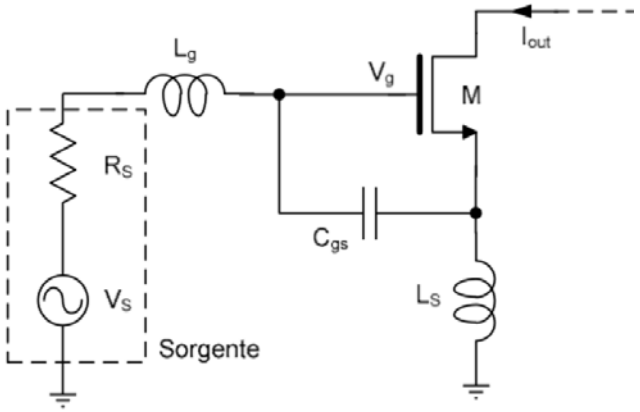


Figure 3.2: inductive source degeneration

At the series resonance of the input circuit, the impedance is purely real and proportional to L_s.
The degree of the input matching achievable at frequencies adjacent to the resonance one f_0 depends on the selectivity of the input resonant network , namely on its quality factor Q_{IN} defined as:

$$Q_{IN} = \frac{1}{2 \cdot \pi \cdot f_0 \cdot C_{gs} \cdot \left(R_S + \omega_T \cdot L_s \right)} \tag{8}$$

a lower quality factor brings a more constant input impedance around the resonance frequency, thereby increasing the bandwidth in which $|S_{11}| < -10$dB.
The input network circuit parameters so determine the resonant frequency, the input impedance at resonance and the matching bandwidth.
The transconductance gain is given by:

$$\left| G_m \right| = \left| \frac{i_{OUT}}{v_s} \right| = \frac{g_m}{\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 \cdot Q_{IN}} + 1} \tag{9}$$

where $\omega_0 = 2\pi f_0$.
One of the main advantages of this topology for narrow-band applications is that the resonance of the input network allows for an high in-band transconductance gain that, at resonance is given by:

$$|G_m| = g_m \cdot Q_{IN} = \frac{1}{2 \cdot R_S} \cdot \frac{\omega_T}{\omega_0} \qquad (10)$$

In wide-band applications the quality factor must be maintained smaller in order to obtain matching all over the required frequency range, with consequent limitations on gain.
The source inductive degeneration topology may encounter stability problems due to the capacitance C_{GD} between gate and drain terminals of the MOS device, which provides a retroactive coupling between the input and output ports. In fact, if you are supposed to connect a resonant RLC load to the drain of the device, at those frequencies at which the resonant load has an inductive behavior, the real part of the input admittance is negative, producing a state of potential instability.
Furthermore, C_{GD}, loading the output of the device, causes a gain reduction and results in a reduction of the resonant frequency.

3.2.2 Is cascode a good choice at 60 GHz?

As just said, the source inductive degenerated topology is an excellent solution at 60 GHz, but it suffer of potential instability and poor reverse isolation due to the gate-drain capacitance. So, ways to prevent this instability have to be found. Many reported mm-wave CMOS amplifiers use cascode devices which can be made unconditionally stable at the operating frequency, making the design more robust and simplifying matching networks.
At lower frequencies, the main reason for using a cascode transistor is the increase in gain. At mm-wave frequencies, the major benefit is a reduction of the reverse gain S_{12} which in turn results in an increase of the MSG for a given frequency, and which lowers the frequency for which the stability factor *k* becomes larger than one (unconditionally stable device) [1].

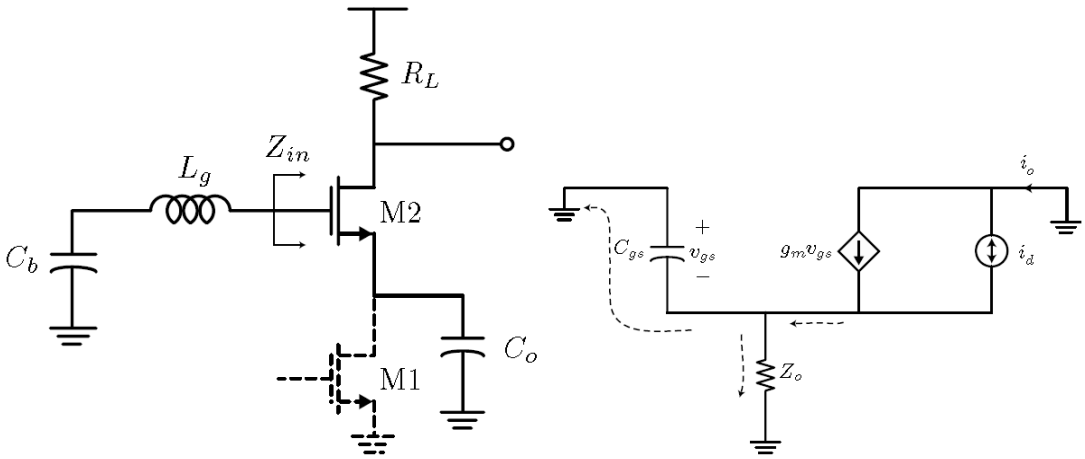


Figure 3.3: The high-frequency degeneration of cascode device produces noise and potential instability.

Regular cascode device, however, have a large parasitic capacitance on the inter-stage node: this capacitance will short-circuit the small signal current at

higher frequencies, thus reducing the actual gain of the cascade structure. With reference to Fig. 3.3, to calculate the contribution of the cascode device to the noise of the transistor, we can see that the noise has two paths to ground, one through the transistor itself and one through the load, which produces output noise.
When the impedance looking into the transistor is much smaller than the current through the load, which occurs at lower frequencies, the current circulates through the transistor and has virtually no impact on the output noise. However, as the impedance of the transcunductance stage drops due to the capacitance at the shared junction node, the current divides and an appreciable fraction flows to the output:

$$i_o = i_d \cdot \frac{1/g_m}{1/g_m + Z_o} = i_d \cdot \frac{1}{1 + g_m \cdot Z_o} \tag{11}$$

$$\overline{i_o^2} = \overline{i_d^2} \cdot \left| \frac{1/g_m}{1/g_m + Z_o} \right|^2 = \overline{i_d^2} \cdot \left| \frac{1}{1 + g_m \cdot Z_o} \right|^2 \tag{12}$$

At low frequencies $Z_o \approx r_o$, which makes the noise contribution small. At higher frequencies, $Z_o \approx 1/j\omega C_{gs}$, which shows that at frequencies approaching the device f_T, the noise contribution increase appreciably.
Also the stability of cascode amplifiers at mm-w frequencies requires special considerations, particularly due to the high frequency capacitive degeneration on the cascode device due to the output capacitance of the trasconductance stage. As shown in Fig.3.3, the impedance looking into the gate of the top transistor at high frequencies is easily shown to be:

$$Z_{in} = \frac{1}{j\omega C_o} + \frac{1}{j\omega C_{gs}} - \frac{g_m}{\omega^2 C_{gs} C_o} \tag{13}$$

which means that in order to make the circuit stable, enough resistance must be present at the gate node at frequencies where the input impedance has a negative real part.
To summarize, at frequencies well below the f_t of transistors, cascode topologies provide a good noise figure, good input matching, and high reverse isolation. At higher frequencies, on the other hand, the pole at the cascode node shunts a considerable portion of the RF current to ground, thereby lowering the gain and raising the noise contributed by the cascode device. Furthermore, unconditional stability is not so ensured and the very small degeneration and gate series inductance inductances required for input matching make the circuit sensitive to package parasitic.
Another solution for preventing instability is to adopt a differential topology. A differential topology, besides being less susceptible to parasitic feedback loops that can cause instability, is more robust to common-mode noise (from power and ground) and is less susceptible to instabilities due to bond wire inductances. Furthermore, since fully balanced circuits form virtual ground nodes, the physical ground connection is much less problematic for differential circuits; this is a big benefit in mm-wave design since it is difficult to realize low impedance ground planes in a modern IC process.

Finally, differential amplifiers have an higher output swing, which is beneficial in improving the dynamic range.
The only downside of differential topology is the doubling of current and the requirement to operate with differential signals.

3.2.3 Millimeter-wave LNA State of the art

In recent years, several LNAs operating in the millimeter waves band have been reported; among them many are CMOS implementations. In Table 3.2 are reported some of the latest CMOS projects and for each one are summarized the performances in terms of gain, noise and power dissipation. The chosen LNA topology is also noted down.

Author	Technology	Frequency (GHz)	Gain (dB)	P_{diss} (mW)	NF_{MIS} (dB)	γ	Topology
Sanduleanu [5]	90 nm	50	25,00	109,0	3,5	2,65	3 cascode stages
Martineau [6]	65nm	80	2,01	22,0	4,5	3,64	1 common source stage
Yao, Voinigescu [7]	90nm	60	14,60	24,0	4,5	4,24	2 cascode stages - L between GC and SC
Niknejad [8]	90nm	104	9,30	22,0	6,0	5,29	2 common source stages
Martineau [6]	65nm	80	7,20	70,0	5,7	5,43	3 common source stages
Ellinger [9]	90nm SOI	26-42 (-3dB BW)	11,90	28,6	3,6	5,50	single cascode stage
Varonen [10]	65nm	60	11,00	104,0	5,6	7,02	3 common source stages
Pellerano [2]	90nm	64	0,63	31,4	6,5	7,42	Cascode stage
Tsai, Wang [11]	130nm	42	20,00	32,0	6,3	7,73	3 Common source stages
Wang - Lin - Min [12]	130nm	57	24,70	79,0	8,0	8,48	3 cascode stages
Varonen[10]	65nm	42	14,30	60,0	6,0	9,54	2 common source stages
Niknejad - Doan [13]	130nm	60	11,00	54,0	8,8	16,18	3 cascode stages
Janssen [14]	65nm	63	10,00	35,0	3,8	3,55	2 stage CS
R. R. Severino [15]	65nm SOI	60	6,00	15,6	3,6	3,44	1 cascode stage
B. J. Huang [16]	65nm	58	16,00	10,0	4,5	5,02	2 stages cascode
W.H. Lin [17]	90nm	57	13,00	4,9	6,3	7,45	3 CS stages

Table 3.2: mm-w LNAs state of the art

The comparison between the different implementations is here carried out through the so-called " *noise-added coefficient* ", given by the expression:

$$\gamma = \left(NF_{MIS} - 1\right) \cdot \frac{f_T}{f_0} \qquad (14)$$

where NF_{MIS} is the measured noise figure on a linear scale $NF_{MIS} = 10^{\left(NF_{MIS\_dB}/10\right)}$ and f_0 is the LNA maximum gain frequency.
This coefficient allows to make a fair comparison of the noise performances, taking into account also the operating frequency.
One common aspect to most reported implementations is the extensive use of transmission lines for matching networks, interconnect wiring and bias networks. Usually, transmission lines lengths are kept much shorter than λ/4 in order to reduce losses and minimize the noise contributions at the input of the amplifier.
T-lines are preferred to spiral inductors since they are easier to model and provide well defined return currents and higher isolation: inaccurate return current loops in matching networks leads to mistuned amplifiers and sub-

optimal performances. On the other hand, spiral inductors allow to obtain a significant area saving and larger quality factors and are sometimes preferred. To overcome the area problems of t-lines, slow-wave transmission lines are often used: they in fact can be considerably smaller than their conventional counterparts and exhibit high Q values. They also allow to easier fulfill the metal density requirements.
In many works, finger *MoM* capacitors are used for ac-coupling of the input and output as well as between stages. They are also used as bypass capacitors for the DC feed lines. These capacitors exhibit high mm-wave quality factors with almost no impact on the circuit performances and their non ideal behavior (they behave inductively at 60 GHz due to their low self-resonance frequency) don't cause any issue as long as they are well modeled and used as part of matching networks to shorten the length of transmission lines.
The DC-decoupling capacitors and the pad capacitance are usually considered as part of the matching networks so that no de-embedding of the pad capacitances has to be performed after the measurements.
Extensive electromagnetic simulations are always performed in order to accurately model parasitic and distributed effects of passives and interconnections.
In many cases for the LNA design are almost solely used t-lines, inductors, capacitance and MOS devices taken from libraries of measurement-based devices.
The topology most widely used consists of one or more cascode stages. In some cases, a series inductor is placed between the drain terminal of the common source stage and the source terminal of the common-gate stage in order to cancel the effect of the central cascode pole and thus to increase its f_T.
Equally frequent is the use of 2 or 3 common-source stages. The presence of the degeneration inductance on the source of the various devices is rarely expressed, but it must be considered intrinsically connected to the circuit physical implementation.

3.3 Analytical study for noise figure minimization

3.3.1 Noise figure minimization for a simple MOS device

In order to evaluate the minimum noise figure for a generic LNA topology the analytical expression of the noise figure for a single MOS device must be initially determined. To do this, the MOS device is treated as a general two-ports microwave network.

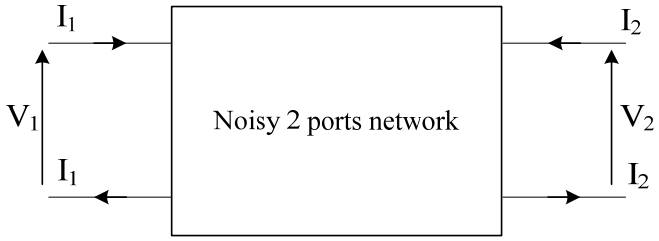


Figure 3.4: generic 2 port noisy network

In Fig 3.4 is shown the principal scheme of a four-pole with internal noise sources [18]. The electrical behavior of this four-pole will be described by two linear equations between the input voltage and current V_1 and I_1 and the output voltage and current V_2 and I_2. This system can be represented by the equivalent circuits of Fig 3.5, where the noisy network of Fig 3.4 is replaced by a noise-free but otherwise unchanged four-pole together with the noise current sources i_1 and i_2 or the noise voltage sources v_1 and v_2, with an inner infinite (zero) impedance.

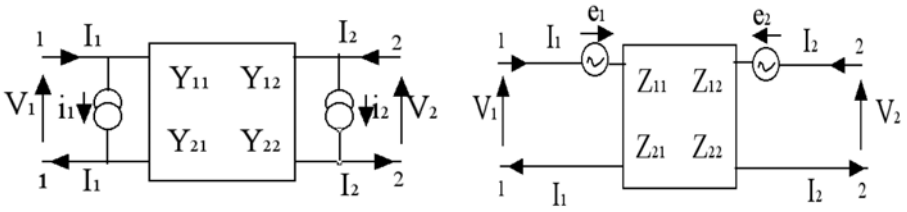


Figure 3.5: generic 2 port noiseless network

In order to characterize the noise qualities of this four-pole this chain matrix can be written:

$$\begin{cases} I_1 = Y_{11} \cdot V_1 + Y_{12} \cdot V_2 + i_1 \\ I_2 = Y_{21} \cdot V_1 + Y_{22} \cdot V_2 + i_2 \end{cases} \tag{15}$$

or

$$\begin{cases} V_1 = Z_{11} \cdot I_1 + Z_{12} \cdot I_2 + e_1 \\ V_2 = Z_{21} \cdot I_1 + Z_{22} \cdot I_2 + e_2 \end{cases} \tag{16}$$

Is now possible to make a further simplification, by moving, with a proper transformation, all noise sources at the input of the network through the use of the current noise source i_n and the voltage noise source e_n (Fig. 3.6).

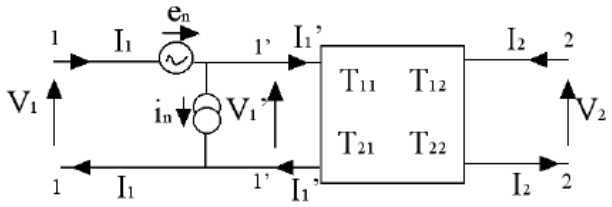


Figure 3.6: generic 2 port noiseless network with input noise sources

The transformation rules that allow to switch from the representation of Fig. 3.5 to that of Fig. 3.6 are:

$$\begin{cases} e_n = -\dfrac{i_2}{Y_{21}} \\ i_n = i_1 - i_2 \cdot \left(\dfrac{Y_{11}}{Y_{21}} \right) \end{cases} \qquad \begin{cases} i_n = -\dfrac{e_2}{Z_{21}} \\ e_n = e_1 - e_2 \cdot \left(\dfrac{Z_{11}}{Z_{21}} \right) \end{cases} \tag{17}$$

Normally a correlation exists between the two noise sources i_n and e_n; to explicit this correlation the noise current i_n can be divided into one part non correlated to e_n (i_u) and a second part fully correlated i_c which must be proportional to e_n. As factor of proportionality having the dimension of an

admittance (impedance) the complex correlation admittance (impedance) is introduced, related to the well known correlation coefficient *c*:

$$c = \frac{\overline{i_n \cdot e_n^*}}{\sqrt{\overline{|i_n|^2} \cdot \overline{|e_n|^2}}}, \quad Y_C = c \cdot \sqrt{\frac{\overline{|i_n|^2}}{\overline{|e_n|^2}}}, \quad Z_C = c \cdot \sqrt{\frac{\overline{|e_n|^2}}{\overline{|i_n|^2}}} \tag{18}$$

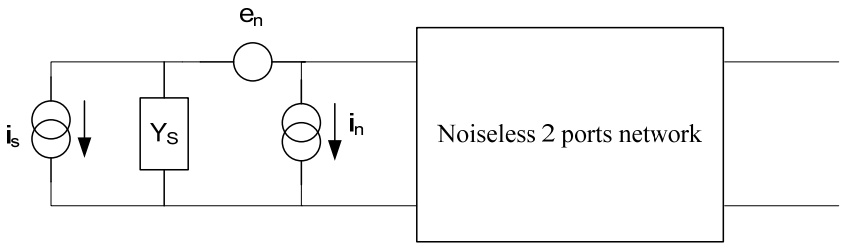


Figure 3.7: generic 2 port network with input noisy signal

Assuming now the presence of an input noisy signal with a source admittance Ys (Fig.3.7) the noise factor of the generic network can be written as:

$$F = 1 + \frac{\overline{i_u^2} + |Y_c + Y_s|^2 \cdot \overline{e_n^2}}{\overline{i_s^2}} \tag{19}$$

From eq. 19 can be seen the presence of three independent noise sources, each of which can be treated as a thermal noise generated by an equivalent resistance or conductance:

$$R_n = \frac{\overline{e_n^2}}{4 \cdot k \cdot T \cdot \Delta f} \qquad G_u = \frac{\overline{i_u^2}}{4 \cdot k \cdot T \cdot \Delta f} \qquad G_s = \frac{\overline{i_s^2}}{4 \cdot k \cdot T \cdot \Delta f} \tag{20}$$

Replacing these resistances and conductances in the eq. 19, deriving the resulting noise factor with respect to Y_s and equaling the numerator to zero the conditions for obtaining the minimum noise are analytically found:

$$\begin{cases} B_s = -B_c = B_{opt} \\ G_s = \sqrt{G_c^2 + \dfrac{G_u}{R_n}} = G_{opt} \end{cases} \tag{21}$$

The minimum noise factor is given by:

$$F_{\min} = 1 + 2 \cdot R_n \cdot \left[G_{opt} + G_c \right] = 1 + 2 \cdot R_n \cdot \left[\sqrt{G_c^2 + \frac{G_u}{R_n}} + G_c \right] \tag{22}$$

To derive the equivalent noise resistance R_n for a MOS device is sufficient to relate the MOS channel thermal noise with the voltage noise source e_n taking into account that Y_{12} equals the MOS g_m.
Using the first equation in (17) and inserting the analytical expression for the channel thermal noise spectral density we obtain:

$$\overline{e_n^2} = \frac{\overline{i_{nd}^2}}{g_m^2} = \frac{4 \cdot k \cdot T \cdot \gamma \cdot g_{d0} \cdot \Delta f}{g_m^2} \tag{23}$$

and

$$R_n = \frac{\overline{e_n^2}}{4 \cdot k \cdot T \cdot \Delta f} = \frac{\gamma \cdot g_{d0}}{g_m^2} = \frac{1}{g_m} \cdot \frac{\gamma}{\alpha} \tag{24}$$

The same thing can be done to relate the noise current i_n with the induced gate current noise [4] .
From the system of equations:

$$\begin{cases} i_1 = i_g \\ Y_{11} = j\omega C_{gs} \\ Y_{21} = g_m \end{cases} \tag{25}$$

from the second equation in (17) we obtain:

$$i_n = i_{ngu} + i_{ngc} + i_{nd} \cdot \frac{j\omega C_{gs}}{g_m} \tag{26}$$

where the induced gate current noise is seen as the sum of two term: i_{ngu} which is completely uncorrelated to i_{nd} and is given by the induced gate current noise as reported *by Van Der Ziel* [19] and i_{ngc} which is instead correlated with the MOS channel thermal channel noise.
The correlation admittance Y_c of eq.18 is now given by:

$$Y_c = \frac{\frac{j\omega C_{gs}}{g_m} \cdot \overline{i_{nd}^2} + c\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}}{\frac{\overline{i_{nd}^*}}{g_m}} \tag{27}$$

Now, inserting the expressions for the various noise spectral densities [20] the final expression of $Y_c = B_c$ is obtained (G_c=0):

$$Y_c = j\omega C_{gs} \cdot \left(1 + \alpha \cdot |c| \cdot \sqrt{\frac{\delta}{5\gamma}}\right) \tag{28}$$

From the uncorrelated part of the induced gate current noise i_{ngu} it is possible to derive also the conductance G_u:

$$G_u = \frac{4 \cdot k \cdot \Delta f \cdot \delta \cdot g_g \cdot \left(1 - |c|^2\right)}{4 \cdot k \cdot T \cdot \Delta f} = \omega^2 \cdot C_{gs} \cdot \left(1 - |c|^2\right) \cdot \frac{\delta^2}{5 \cdot g_{d0}} \tag{29}$$

Replacing the G_u, Y_c and R_n expressions for the MOS transistor in the general equation for the minimum noise factor (Eq. 22) it's easy to obtain the minimum noise factor for a single MOS device:

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \cdot \frac{\omega}{\omega_T} \cdot \sqrt{\gamma \cdot \delta \cdot \left(1 - |c|^2\right)} \tag{30}$$

The optimum source admittance is now given by:

$$\begin{cases} B_{opt} = -\omega \cdot C_{gs} \cdot \left(1 + \alpha \cdot |c| \cdot \sqrt{\dfrac{\delta}{5\gamma}}\right) \\ G_{opt} = \omega \cdot C_{gs} \cdot \alpha \cdot \sqrt{\dfrac{\delta}{5\gamma}\left(1 - |c|^2\right)} \end{cases} \tag{31}$$

The minimum noise factor for the MOS transistor is thus independent on its size and results proportional to the ratio between the operating frequency and the MOS cutoff frequency.
Substituting the values of the technological parameters for the 65nm CMOS technology ($\alpha \approx 1$, $\gamma \approx 1$, $\delta \approx 4/3$, $g_{d0} \approx g_m$, $|c| \approx 0.4$), the noise factor and the optimum admittance can be expressed only as a function of C_{gs}, g_m and ω:

$$\begin{cases} B_{opt} = -1.2 \cdot \omega \cdot C_{gs} \\ G_{opt} = 0.47 \cdot \omega \cdot C_{gs} \\ F_{\min} \approx 1 + 0.94 \cdot \dfrac{\omega}{\omega_T} \end{cases} \tag{32}$$

Repeating all these analytical steps in terms of the two port network impedances, the following conditions on the source impedance for minimum noise are found:

$$\begin{cases} X_{opt} = \dfrac{1 + \alpha \cdot |c| \sqrt{\dfrac{\delta}{5\gamma}}}{\omega \cdot C_{gs} \cdot \left(1 + 2\alpha \cdot |c| \cdot \sqrt{\dfrac{\delta}{5\gamma}} + \alpha^2 \left(\dfrac{\delta}{5\gamma}\right)\right)} \\ R_{opt} = \dfrac{\alpha \cdot \sqrt{\dfrac{\delta}{5\gamma}} \cdot \sqrt{1 - |c|^2}}{\omega \cdot C_{gs} \cdot \left(1 + 2\alpha \cdot |c| \cdot \sqrt{\dfrac{\delta}{5\gamma}} + \alpha^2 \left(\dfrac{\delta}{5\gamma}\right)\right)} \end{cases} \tag{33}$$

3.3.2 Noise figure minimization for the inductive source degeneration stage

Exploiting the analytical treatment of noise described in the previous paragraph, we can now perform a similar analysis on the inductive source degeneration stage; however now the whole analysis is carried out by imposing as starting hypothesis the impedance matching condition: $Zs = Z_{IN}^*$. Z_S is the impedance related to the input signal and Z_{IN} is the LNA input impedance.
From Eq. 7, without considering the gate series inductance L_g the source inductive degeneration stage input impedance is given by:

$$Z_{IN} = \frac{1}{C_{gs}} + s \cdot L_s + \omega_T \cdot L_s \tag{34}$$

and by imposing the noise matching conditions on the input resistance derived in the previous paragraph (Eq 33):

$$\omega_T \cdot L_s = R_{opt} = \frac{r_{opt}}{\omega \cdot C_{gs}} \tag{35}$$

where the normalized resistance r_{opt} is given by:

$$r_{opt} = \frac{\alpha \cdot \sqrt{\frac{\delta}{5\gamma}} \cdot \sqrt{1-|c|^2}}{\left(1 + 2\alpha \cdot |c| \cdot \sqrt{\frac{\delta}{5\gamma}} + \alpha^2 \left(\frac{\delta}{5\gamma}\right)\right)} \approx 0.28 \tag{36}$$

From equation 35 a new normalized parameter l_s can be introduced, which is in practice equal to $_{ropt}$:

$$l_S = L_S \cdot \omega \cdot \omega_T \cdot C_{gs} \approx L_S \cdot g_m \cdot \omega \tag{37}$$

if now we consider also the physical presence of the non-noisy gate series resistance R_{NQS} related to the induced gate noise from channel charge fluctuations, in order to achieve as possible likely analytical results at high frequencies:

$$R_{NQS} = \frac{1}{5 \cdot g_m} \tag{38}$$

the new input total resistance R_{IN} is given by:

$$R_{IN} = R_{NQS} + \omega_T \cdot L_s \tag{39}$$

also this resistance has been expressed as a function of a normalized resistance r_{NQS}:

$$R_{NQS} = \frac{r_{NQS}}{\omega C_{gs}} \tag{40}$$

and by equaling eq. 38 and 40, this normalized resistance is given by:

$$r_{NQS} = \frac{1}{5} \cdot \frac{\omega}{\omega_T} = 0.05 \tag{41}$$

now, by imposing the noise matching conditions derived in the previous paragraph as a function of the normalized parameters l_s and r_{nqs}:

$$\begin{cases} R_S = \dfrac{l_S + r_{NQS}}{\omega \cdot C_{gs}} \\ X_S = -\left(\dfrac{l_S}{\omega_T \cdot C_{gs}} - \dfrac{1}{\omega \cdot C_{gs}}\right) \end{cases} \tag{42}$$

It is now possible to find the noise factor expression as a function of l_s and r_{NQS}, taking as initial hypothesis this input impedance matching.

The noise sources which are taken into account are the source resistance thermal noise, the MOS channel thermal noise and the correlated and uncorrelated parts of the induced gait noise.
The spectral densities of these noise sources are here summarized:

$$\begin{cases} \overline{i_{n,d}^2} = 4 \cdot k \cdot T \cdot \gamma \cdot g_m \\ \overline{i_{n,gc}^2} = 4 \cdot k \cdot T \cdot \dfrac{\delta}{5 \cdot g_m} \cdot |c|^2 \cdot \omega^2 \cdot C_{gs}^2 \\ \overline{i_{n,gu}^2} = 4 \cdot k \cdot T \cdot \dfrac{\delta}{5 \cdot g_m} \cdot \left(1 - |c|^2\right) \cdot \omega^2 \cdot C_{gs}^2 \\ \overline{e_S^2} = 4 \cdot k \cdot T \cdot R_S \end{cases} \tag{43}$$

Concerning the effect on the output noise of the uncorrelated part of the induced gate noise, it is simply given by the product of the i_{ngu} spectral density and the square module of the transfer function of the induced gate noise, that is:

$$T_{ig} = \frac{\omega_T}{2\omega} \cdot \left(\frac{1}{l_S + r_{NQS}} - j \frac{l_S + 2 \cdot r_{NQS}}{l_S + r_{NQS}} \right) \tag{44}$$

The effect on the output noise of the correlated part of the gate noise is instead found by expressing i_{ngc} as a function of i_{nd}:

$$\overline{i_{ngc}^2} = |c|^2 \, \overline{i_{ng}^2} = |k|^2 \, \overline{i_{nd}^2} \tag{45}$$

where *k* is therefore:

$$|k| = |c| \cdot \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} = |c| \cdot \sqrt{\frac{\delta}{5\gamma}} \cdot \frac{\omega}{\omega_T} \tag{46}$$

Basing on this dependence a new transfer function for the channel thermal noise is used, which takes into account also the correlated part of the gate noise:

$$|T_{id,OUT}| = |T_{id}| + |k| \cdot |T_{ig}| \tag{47}$$

where T_{id} is:

$$T_{id} = \frac{1}{2} \cdot \frac{l_S + 2 \cdot r_{NQS}}{l_S + r_{NQS}} \tag{48}$$

Finally, the transfer function for the R_S thermal noise is:

$$T_{R_S} = -j \frac{g_m}{2 \cdot \left(l_S + r_{NQS}\right)} \tag{49}$$

Now, substituting the various terms in:

$$F_{DEG\_IND} = 1 + \frac{|T_{ig}|^2 \cdot \overline{i_{ngc}^2} + |T_{id,OUT}|^2 \cdot \overline{i_{nd}^2}}{|T_{R_S}|^2 \cdot \overline{e_S^2}} \tag{50}$$

we obtain the noise factor of the source inductive degeneration stage under impedance matching conditions:

$$F_{DEG\_IND} = 1 + \frac{1}{l_S + r_{NQS}} \left[\frac{\delta}{5} + \left(l_S^2 + 4 \cdot r_{NQS}^2 + 4 \cdot l_S \cdot r_{NQS} \right) \cdot \left(\gamma + 2 \cdot |c| \cdot \sqrt{\frac{\gamma\delta}{5}} + \frac{\delta}{5} \right) \right] \cdot \frac{\omega}{\omega_T}$$

Deriving the noise factor with respect to l_S and equaling the numerator to zero the value of l_S for minimum noise figure is obtained:

$$l_{S,opt} = \sqrt{\frac{1}{2} \cdot r_{NQS}^2 + \frac{\delta}{5\gamma + \delta + 2 \cdot \sqrt{5} \cdot |c| \cdot \sqrt{\gamma\delta}}} - r_{NQS} = 0.35 \qquad (52)$$

The minimum noise factor is:

$$F_{MIN} = 1 + 1.52 \frac{\omega}{\omega_T} \qquad (53)$$

At 60GHz and considering the cutoff frequency f_T=235GHz the minimum achievable noise figure is 1.42dB.

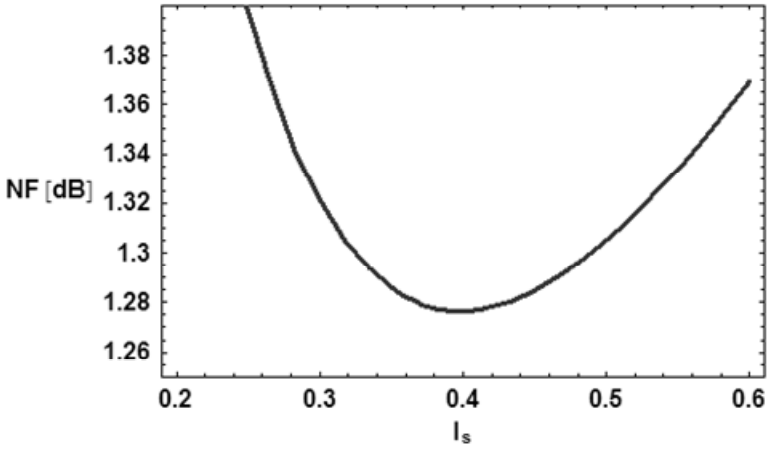


Figure 3.8: NF versus l_S

In Fig. 3.8 the NF as a function of l_S is reported: the NF values around the optimum doesn't differ so much from the minimum one. Thus choosing l_S values slightly lower or higher doesn't affect significantly the LNA noise performances.

To summarize, the degeneration inductance L_S has been normalized to the MOS size through a dimensionless parameter l_S and the NF has been minimized only as a function of this new parameter: in this way, an l_S optimum that achieves the NF_{min} is obtained. This parameter depends on the product g_m*L_S: this allows to obtain simultaneous noise minimization and input impedance matching because once L_S is chosen in order to meet the impedance matching requirements, the noise optimum is reached acting on the transistor size.

Once the optimum l_S has been found is therefore necessary to find the most appropriate combination of L_S and g_m, depending on power dissipation, matching networks bandwidth considerations and so on. These aspects will be deepen in the next section.

The BSIM4.5 model of the devices is not sufficiently accurate at high frequencies since, for example, it only includes the gate resistance due to poly, which is only a minimal part of the total mm-waves gate resistance. As a consequence, an AC and a noise custom models of the MOS device have been used for simulations: all the parameters which have been included in our models have been expressed as a function of the number of fingers N, considering a single finger size of W_f= 1μm and L_f=65nm.
These models also achieve to verify the analytical noise study (based on a simplified device model) and to prove that it still remains valid for device models with different levels of accuracy. For example, using a device model which includes besides the gate-source capacitance also the gate-drain capacitance and using for the circuit noise optimization the results of our simplified noise study, the simulated LNA noise figure differs from the expected one of only 0.1dB. Thus, until the capacitance C_{gd} is much lower that C_{gs} we can say that the analytical noise study is valid.

3.4 mm-wave LNA design and characterization

3.4.1 The LNA design

As widely discussed in paragraphs 3.2.1 and 3.3.2, inductive source degeneration represents an excellent solution to obtain at the same time good noise performances and a satisfactory input impedance matching.
Furthermore, tanks to our analytical noise study the noise minimization task and the impedance matching requirements become practically independent one from each other because once the optimum l_S has been found, and consequently the noise optimum is reached, one can choose the L_S value to obtain impedance matching (through an input matching network) and then, acting on the transistor size the noise optimum is maintained.
As said before, once the optimum l_S has been found is necessary to find the most appropriate combination of L_S and g_m, depending on power dissipation criteria and matching networks bandwidth and losses considerations.
Besides the noise and power dissipation tasks, also the LNA stability problems has to be taken into account. The use of cascode to improve stability has been rejected based on the considerations made in paragraph 2.2.2: at 60GHz, the pole at the cascode node shunts a considerable portion of the RF current to ground, thereby lowering the gain and raising the noise contributed by the cascode device. Not even stability is ensured: at high frequencies, since the input impedance of a capacitively degenerated device (the cascode one) has a negative part, a high Q parasitic inductance at the gate of the cascode can form a Colpitts oscillator.
Instability has been prevented, in our design, by adopting a differential topology: the LNA presents a single-ended input/output, but internally it works in a differential manner. A passive balun picks up the single-ended input signal and generates an output differential signal (output signals are ideally 180° out of phase one from each other), making at the same time a 50Ω to 25Ω impedance transformation. The balun has been used mainly to prevent measurement problems: measurement of a differential circuit in fact , especially at high frequencies, turns out to be quite difficult. This differential

topology, besides being less susceptible to parasitic feedback loops, is more robust to common-mode noise (from power and ground). Furthermore, since fully balanced circuits form virtual ground nodes, the physical ground connection is much less problematic for differential circuits.
In Fig. 3.9 the passive balun schematic and its layout implementation are reported: the red lines surround the spiral inductor, the black lines surround the finger MoM capacitors and the green lines refer to interconnections.
An identical mirrored passive balun is used at the LNA output.

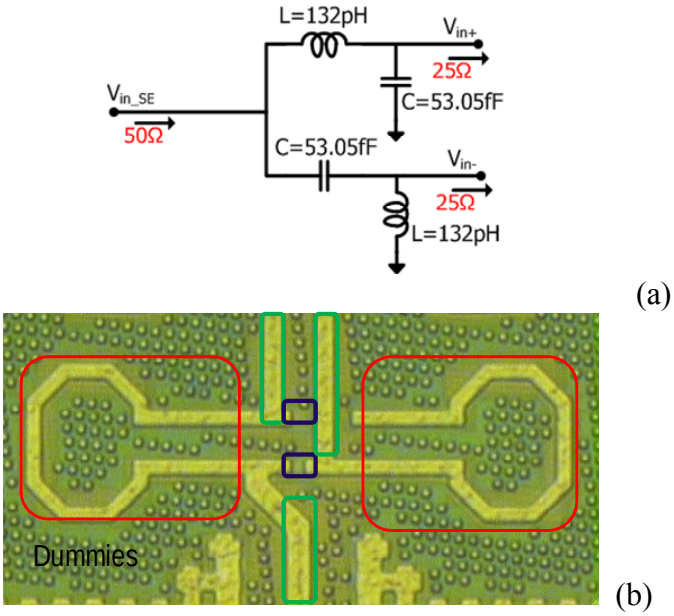


Figure 3.9: passive balun schematic (a) and layout (b)

The balun schematic consists of a simple network of L's and C's. The values of L and C, reported in Fig. 3.9, are given by:

$$L = \frac{\sqrt{2R_S \cdot R_L}}{\omega} \qquad C = \frac{1}{\omega \cdot \sqrt{2R_S \cdot R_L}} \tag{54}$$

where R_S and R_L represents respectively the input single-ended resistance and the output resistance on each branch.
The balun layout as been segmented into sub-sections and each sub-subsection, properly prefilled with dummies to reach the local density requirements, as been electromagnetically simulated using Agilent Momentum. Thus, the S-parameter blocks extracted from EM simulations of the various sub-sections, has been properly connected and used in the LNA schematic for circuital simulations.
The simulated losses (S_{21}) of the implemented balun are shown in Figure 3.10: around 60GHz losses are nearly 1.1 dB.
In our design, the input and output pad capacitances are exploited for the matching of the LNA input and output to 50Ω: this means that pad de-embedding is not required during measurements.
Pads are shielded using a M_1 (lower metal) plate with proper holes in order to satisfy metal density rules: this shield allows to minimize substrate coupling

and consequently to obtain higher pad quality factors. Both floating M_1 shield and grounded shield has been evaluated, through EM simulations, in terms of quality factor.
The comparison shows that, as can be seen in Figure 3.11, while at lower frequencies grounded shielding allows higher pad quality factors, at mm-wave frequencies is more convenient to keep the shield floating: quality factors higher by a factor of nearly 2.5 (Q_{FS}≈8, Q_{GS}≈20) are obtained with floating shielding if compared with the grounded solution.
At 60GHz the floating shielded pad capacitance is nearly 50fF.

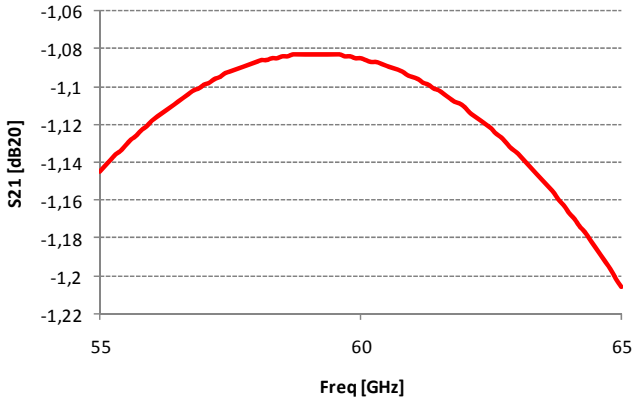


Figure 3.10: passive balun losses versus operating frequency

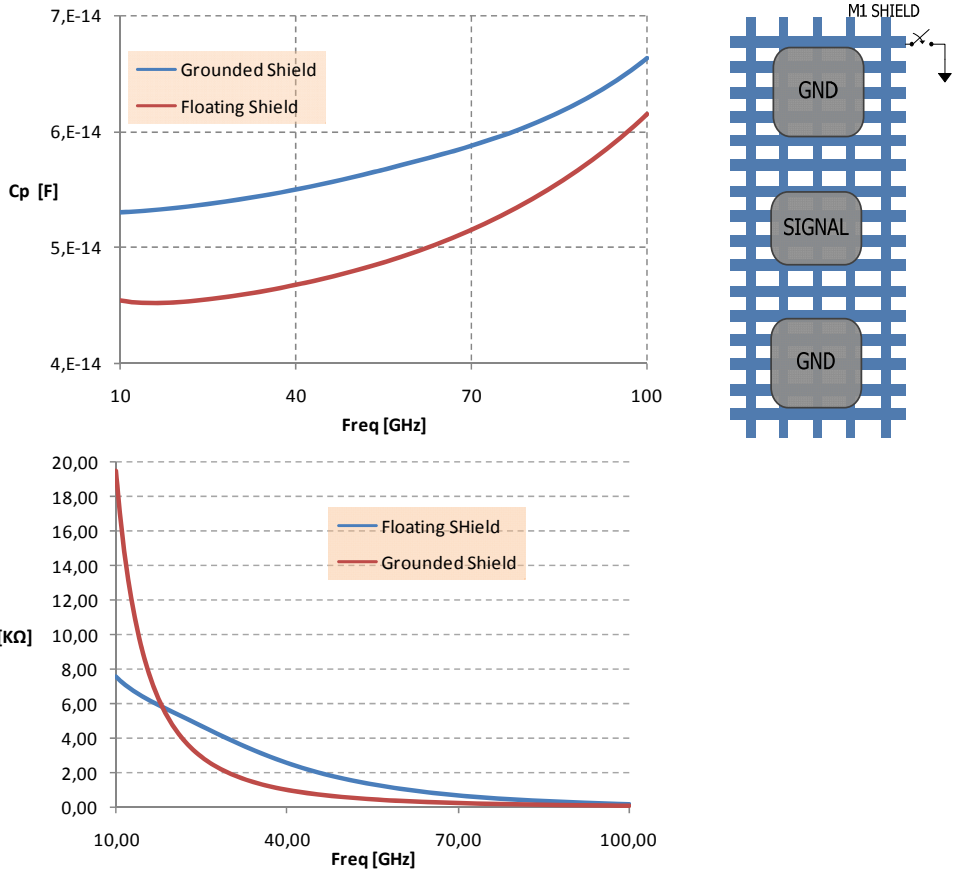


Figure 3.11: floating shield vs grounded shield

The 50fF input/output pad capacitance has been resonated with a parallel inductor partly in order to obtain a protection from the electrostatic discharges (*ESD* protection), but mainly in order to realize an high impedance level at the LNA input and consequently to minimize the device size and its power dissipation; in fact, resonating the pad capacitance with a series inductor would give origin to a low-pass L matching network, resulting in a forced impedance transformation from 50Ω to nearly 26Ω.

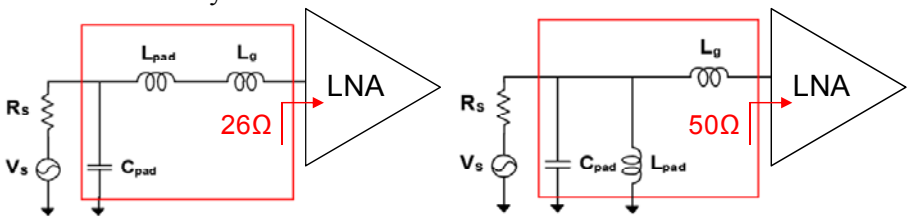


Figure 3.12: input network choice

As a matter of fact, using a low-pass L matching network, the series inductance value L_s is set by the resonance condition:

$$\omega_{RIS} = 2\pi \cdot 60 \cdot 10^9 = \sqrt{\frac{1 - L_S / \left(C_{PAD} \cdot R_S^2\right)}{L_S \cdot C_{PAD}}} \tag{55}$$

and consequently the LNA input resistance is forcedly given by the equation:

$$R_{IN-LNA} = \frac{L_S}{C_{PAD} \cdot R_S} \tag{56}$$

where R_S is the 50Ω source resistance.
The resonated pad physical implementation and its circuital model extracted from EM simulations are reported in Fig.3.13.

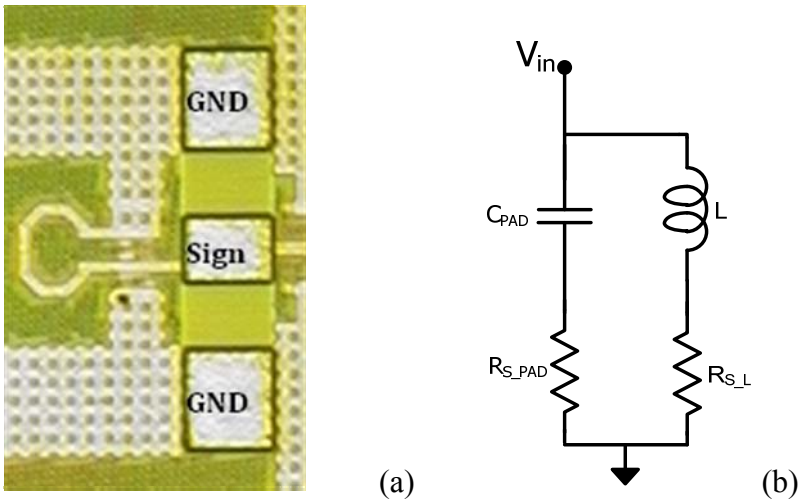


Figure 3.12: resonated pad layout (a) and circuital model (b)

where C_{PAD}=49.5fF, L=140pH, R_{S_PAD}=2.7Ω and R_{S_L}=1.3Ω: according to the simulations results, the pad resonance frequency is nearly 62GHz and the resonated pad quality factor is nearly 13 for an equivalent simulated pad loss of about 0.5dB.
The LNA schematic is reported in Figure 3.13: it is composed by five identical inductive source degeneration stages connected together and with the input/output baluns through appropriate matching networks.

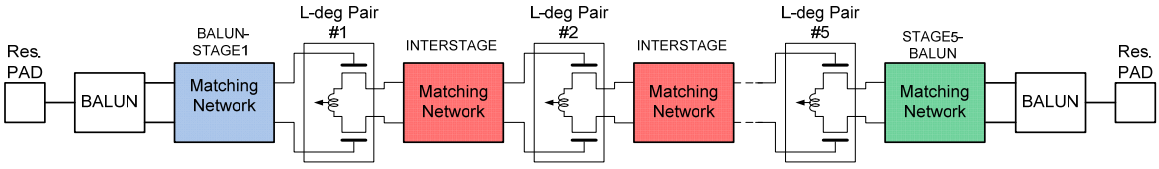


Figure 3.13: LNA schematic

The inductive source degeneration stages are sized for optimum noise performances, according to the analytical noise study results of paragraph 3.3.2. As already mentioned, once the optimum l_S has been found, it is necessary, in order to find the most appropriate combination of L_S and g_m, to take into account some different aspects related to power dissipation criteria and matching networks bandwidth and losses considerations. Larger devices (larger g_m) typically allow for smaller matching networks (shorter t-lines) resulting in reduced losses and higher overall gain of the complete LNA. For this reason, it is advantageous to use a large MOS device: the noise figure doesn't depend directly on the device size at first order, but larger devices tend to give better NF due to lower losses in the matching network.
The maximum device size is set by the feasibility of the input matching network itself. In fact, a too large device makes the input matching network more challenging, since the 50Ω source impedance would have to be matched to an impedance with a smaller imaginary part (larger capacitance) and a real part much smaller than 50Ω. This would translate into narrowband matching [21] and higher sensitivity to modeling and process variations.
Furthermore, a too large device size leads to an high power dissipation.
Based on these criteria, a degeneration single-ended inductance of nearly 50pH and a device transconductance of about 20mS are chosen.
The MOS device is laid out of 21 fingers with L_f=65nm and W_f=1μm; gates are connected on one side to avoid metal overlap between gate drain, thereby minimizing C_{GD}. The drain and source are fed from opposite sides to further minimize C_{GD} , C_{GS} and the drain-to-source capacitance C_{DS}: this would bring an improvement both in the device *MSG* and in its f_T.
Sufficiently many vias are used at all levels connections to ensure their relative contributions to extrinsic gate and drain resistances are small.
Matching networks have been designed taking into account losses, bandwidth and physical implementation criteria.
For all networks an "hybrid" approach has been adopted: both spiral inductors and transmission lines are massively used, mainly because T-lines arise naturally from inductors physical connection (they must be placed at a sufficient distance to avoid mutual coupling phenomena) and also in order to exploit the advantages of both practical approaches.

T-lines provide better defined return currents, higher isolation and most importantly a wide range of inductance values to be realized by simply adjusting the length of the line. Very small inductance values can be obtained, which are difficult to realize using classical inductors with a reasonably high quality factor. Finally, transmission lines can be used for impedance matching with more predictable parameters because every single session of a t-line of any length is fully modeled by four real numbers RLGC. Accurate modeling of spiral inductors instead is not a simple task.

Inductors, on the other hand, allow a significant area saving and generally offer higher quality factors.

In our design, differential t-lines are implemented in the form of a differential coplanar strip-line (CPS); the quality factor of the CPS has been improved by shielding the transmission line by means of floating metal strips located underneath the guiding structure realized on the lowest metal layer M_1 (as it was done for the SWO design). The distance between two consecutive bars has been set to 1μm in order to minimize the field penetration (Fig. 3.14).

The array of floating metal strips allows increasing the specific capacitance of the transmission-line without decreasing the specific inductance, such that the resulting phase velocity is effectively reduced. This reduces the length of the t-line required to implement a specific phase shift, resulting in area saving. Slow-wave lines offer the additional advantage of partially shielding the electric field from the lossy substrate (higher t-line Q) and also make it easier to satisfy metal density rules.

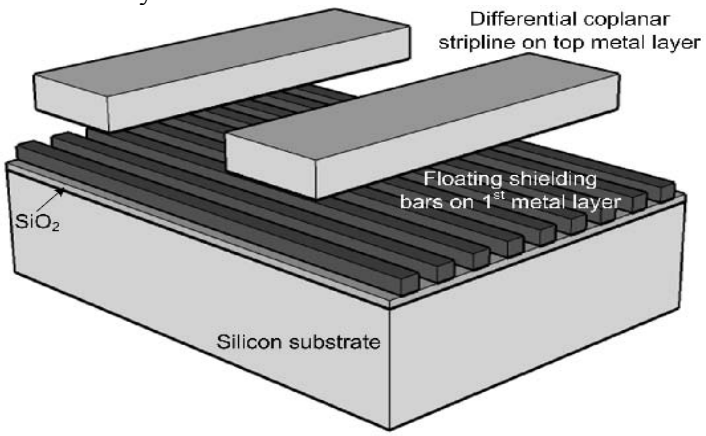


Figure 3.14: differential shielded CSP

All the inductors have been implemented in the higher metal level (M_6) and have been optimized, for high Q values, through extensive EM simulations.

Series capacitors are used for the ac-coupling of the input and output stages and are also exploited to reduce the equivalent value of series inductance (when they are in series with inductance). Capacitors placed in parallel with inductors have the opposite purpose: they increase the equivalent inductance values synthesized by the parallel LC network, allowing to use real inductance value not too high (which are difficult to implement with high quality factors).

Only finger *MoM* capacitors are used because they exhibit high mm-wave quality factors with almost no impact on the circuit performances and their non ideal behavior (they behave inductively at 60 GHz due to their low self-

resonance frequency) don't cause any issue as long as they are well modeled and used as part of matching networks to shorten the length of transmission lines.

Bias voltages are brought to the various MOS devices through some virtual ground nodes: in fact, they represent low impedance points and are suitable for bias insertion (see Fig. 3.15).

Matching networks show, from EM simulations, losses between 1 and 1.8dB and bandwidths of about 10GHz around 60.

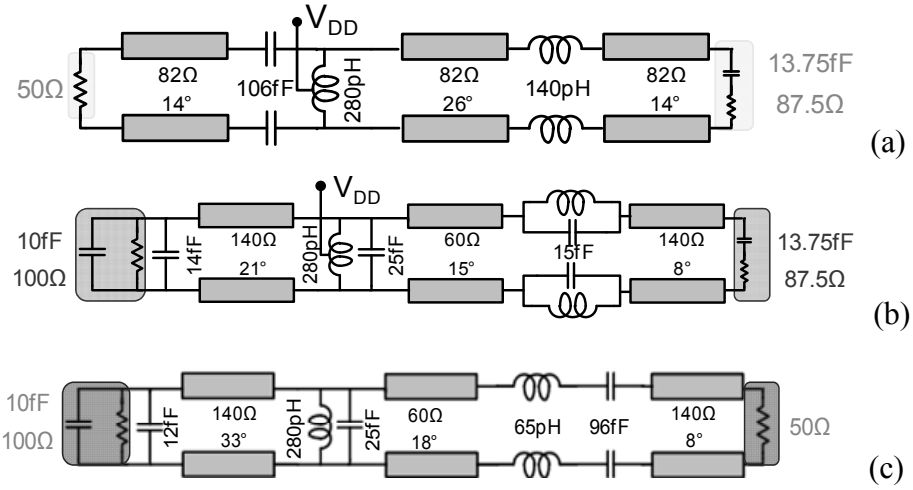


Figure 3.15: input matching network (a), inter-stage matching network (b) and output matching network (c).

3.4.2 The LNA characterization

The LNA test chip has been designed and implemented in TSMC 65nm CMOS process with 6 levels of metal and ultra thick top metal. A chip micrograph is reported in Fig. 3.16. Bias pads are located on the bottom side, while the LNA input/output, suitable for on-chip measurement with GSG probes, are located on the left-right sides. The chip, including all pads, measures 2750 x 510 μm^2.

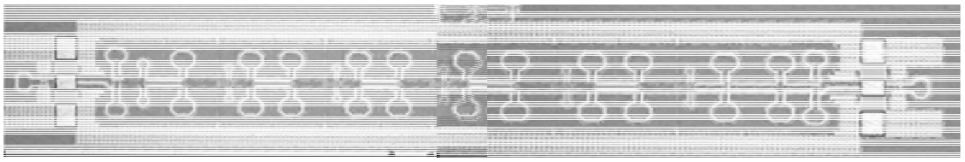
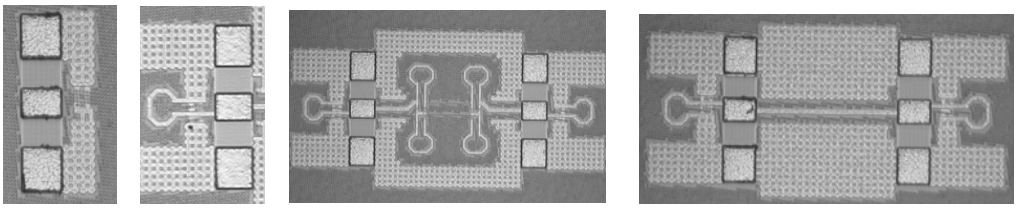


Figure 3.16: LNA micrograph

Our test chip includes, besides the overall LNA, other stand-alone structures (see Fig. 3.17) among which the simple GSG shielded pad (a), its resonated version (b), the resonated pad in a back-to-back configuration (c) and the passive balun in a back-to-back configuration as well (d). These structures

have been integrated in order to experimentally verify their circuital models used during simulation (extracted from electromagnetic simulations) and eventually to help us understanding the overall circuit behavior.



(a) (b) (c) (d)

Figure 3.17: other integrated stand-alone structures

Both the LNA and the other simple structures has been characterized on-chip, by directly probing their inputs and outputs through an high frequency probe-station. It has been opportunely connected to a network analyzer and after the de-embedding procedure carried out using a calibration substrate, the S-parameters of the various two-ports networks has been extracted.

While the measurements results on the simple shielded pad structure show a discrete agreement with simulations, experimental results on the resonated pad presents strong discrepancies with simulations: the pad measured resonance frequency is nearly 55GHz, 7GHz lower than the simulated one, and the measured pad quality factor is lower than predicted of a factor 1.7. The values of the resonated pad circuital model, extracted from measurements, are: C_{PAD}=55fF, L=151pH, R_{S_PAD}=2.22Ω and R_{S_L}=5Ω. The inductance quality factor is the pad parameter that deviates mostly from the simulated one.

These discrepancies are probably largely due to some simplifications performed in order to electromagnetically simulate the structure in an acceptable time and with a sufficiently accurate mesh. Is also likely that the strong reduction of the inductor quality factor is due to further automatic metal density enforcement in the inductor surrounding area.

In the resonated pad back-to-back configuration the input and output pads are connected through a single-ended transmission line with a characteristic impedance of 50Ω and an electrical length of nearly 80°: based on EM simulations, the t-line losses are nearly -0.85dB.

Once the t-line losses amount is known, from the S_{21} measurements on the overall back-to-back structure, it's easy to obtain that the measured resonated pad loss is nearly 0.5dB.

The back-to-back balun test structure (see. Fig 3.18) consist of the input/output resonated pads, the input/output baluns and a differential transmission line with 1.3dB associated losses used to connect the two mirrored sides of the structure.

The extracted experimental data show a good agreement both in the balun S_{11} and regarding its losses which are nearly 1.2dB: therefore it seems that breaking up the structure into sub-structures EM simulated separately and properly connecting the S-parameter blocks extracted from EM simulation for circuital simulations is the most appropriate method.

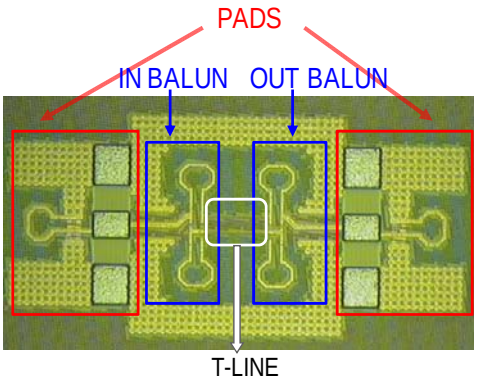


Figure 3.18: back-to-back balun structures

Concerning the LNA characterization, measurements results show a relevant discrepancy with simulations, both in the LNA power gain and mainly in the input matching. In Figure 3.19 are reported the predicted gain (black line) and the measured one (red line) as a function of frequency: the maximum measured gain not only is lower than predicted of about 10dB, but also shifted at lower frequencies (from 60 to 53GHz). The measured input impedance is much lower than the expected 50Ω as can be seen from Fig. 3.20.

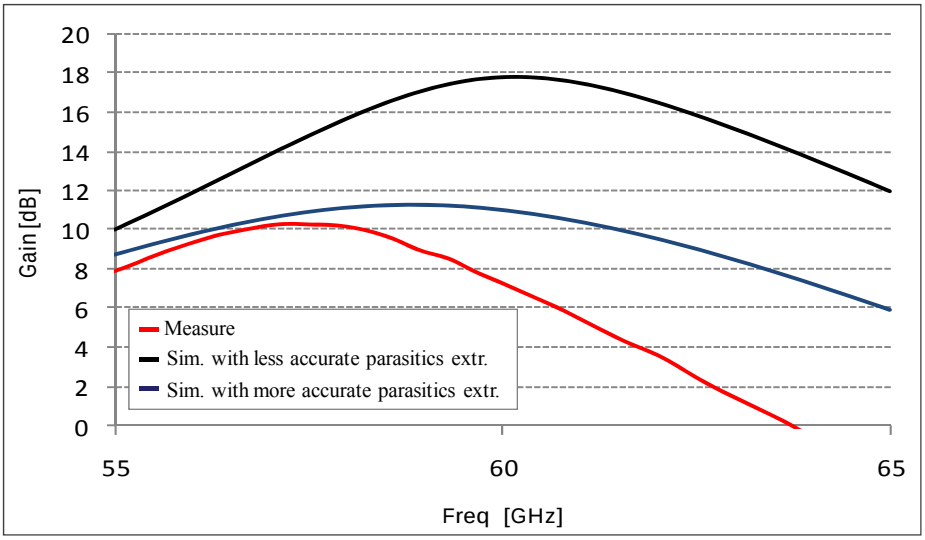


Figure 3.19: LNA gain comparison

Analysis post layout showed that the gain discrepancy is mainly caused by inaccurate extraction of layout parasitic strictly related to the local active device connections. The blue line in figure 3.19 shows that a more accurate post-layout extraction of these parasitic allows to get closer to the experimental results. Further discrepancies from the expected LNA performances are probably related to dummies effect on passive networks and, as said before, to forced simplifications during EM simulations.

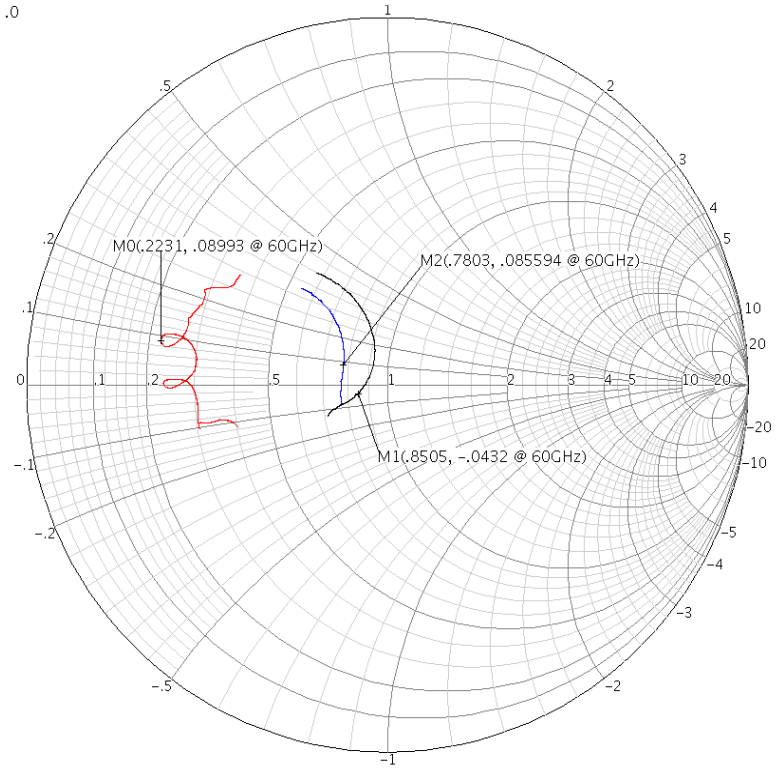


Figure 3.20: LNA input matching

Conclusions

60GHz low noise amplifier design has been extensively discussed in this chapter.
Many of the considerations given in the first two sections, regarding the most suitable 60GHz LNA topologies and how to face the main design challenges, are then directly applied in our design.
Extensive electromagnetic simulations have been performed during design in order to try to accurately model parasitic and distributed effects of passives and interconnections, which hardly affect the LNA performances. Despite this accuracy attempt, simplifications performed in order to electromagnetically simulate the structures in an acceptable time and with a sufficiently accurate mesh, has caused a strong deviation of measurement results from the expected ones. Also further automatic metal density enforcement in the pad and matching networks area has probably worsen the experimental LNA performances.
It might have been appropriate to use, for the LNA design, solely t-lines, inductors, capacitance and MOS devices taken from libraries of measurement-based devices as done for some successful LNA reported implementations.

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Chapter IV

LO generation and distribution system design for a 60GHz baseband recombination phased-array receiver

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For a wide range of emerging applications in the 60GHz spectrum the use of multiple antennas with beam steering capabilities represents a key enabling technology.

Integration of a complete phased array system in silicon results in substantial improvements in cost, size and reliability providing opportunities to perform on-chip signal processing and conditioning.

At the circuits level, the division of the signal into multiple parallel paths relaxes the power handling and noise requirements for each individual active devices. The higher SNR at the output together with the lower interference translate into higher channel capability, while the directivity of the transmit-receive pairs can result into higher frequency reuse ratios and consequently higher network capabilities.

In all phased array architectures, except the RF recombination one, LO distribution represents a difficult task, and, if a direct-conversion topology is chosen, also the I/Q LO generation becomes challenging. Quadrature LO generation typically degrades the generation system performances considerably if classical coupled-oscillators are exploited and the I/Q outputs of the coupled-VCOs must travel large distances to reach every single mixer in the array, thus experiencing significant losses and mismatches.

These problems could be largely overcome by combining the LO generation and distribution tasks through the use of a spatially distributed oscillator. I/Q LO signals have to be generated and directly available at the spatially separated I/O LO ports of each direct down-conversion mixer without the need for a lossy distribution network.
In this chapter a spatially distributed LO generation system based on the use of coupled rotary travelling wave VCOs is presented. In such a VCO multiple-phase signals are easily available by tapping off the signals from different positions on the transmission line easily providing accurate high frequency quadrature signal generation from a single VCO.
Furthermore, the distributed nature of the oscillator allows to absorb the transistors parasitic capacitances into transmission lines alleviating tuning range limitations and phase noise degradation.
Coupling between different RTWO loops is here performed adopting an "hybrid" travelling-standing waves based structure: loops are physically connected at the circuited ends of $\lambda/4$ transmission lines which are connected to each loop at two opposite corners to provide the DC bias. By virtue of the injection locking mechanism, loops are forced to work at the same oscillation frequency.
In the first section of this chapter the phased array concept and the advantages and drawbacks of the various phased array system architectures are described. The LO distribution problem is than presented.
The second section concerns the description of our proposed LO generation and distribution system: the single rotary traveling wave oscillator design is first presented than the adopted coupling mechanism is widely described.

4.1 mm-wave phased array receivers

4.1.1 Phased array principle

Complementary metal-oxide semiconductor (CMOS) is the dominating technology for most wireless products below 10GHz. This dominance has been achieved by reliability, low cost, and high device count advantages of CMOS compared to the other semiconductor technologies such as SiGe and GaAs. Today, with the aggressive scaling of gate length, CMOS technology is pushing further into the mm-wave region. Moreover, CMOS is the most promising technology for system-on-chip design, because it enables integration of the analog RF circuits as well as the digital signal processing and baseband circuits in the lowest possible area, which leads to a lower cost and compact solution. Therefore, the nano-scale CMOS technology, such as 65nm, offers commercial mm-w solutions for short range and high data rate applications.

However, several system and circuit level challenges must be met, such as the lack of efficient and low cost antennas and packaging solutions, the severe path losses, the low output power and nonlinearity of power amplifiers and the limited achievable gain and high noise figure of low noise amplifiers at 60GHz.
For a wide range of emerging applications in the 60GHz spectrum the use of multiple antennas with beam steering capabilities is a key enabling technology to address most of this challenges.
Integration of a complete phased array system in silicon results in substantial improvements in cost, size and reliability.
At the same time, it provides numerous opportunities to perform on-chip signal processing and conditioning, without having to go off-chip, leading to additional saving in cost and power. At the circuits level, the division of the signal into multiple parallel paths relaxes the power handling and noise requirements for individual active devices used in the array, as will be discussed later; this also makes the system more robust to the failure of individual components.
Multiple antenna phased arrays imitate the behavior of a single directional antenna whose bearing can be controlled electronically; this electronic steering makes it possible to emulate antenna properties such as gain and directionality, while eliminating the need for continuous mechanical reorientation of a directive antenna.
A phased array receiver consists of several signal paths each connected to a separate antenna. The antenna elements of the array can be arranged in different spatial configurations [1]: the array can be formed in one, two, or even three dimensions, with one- or two-dimensional arrays being more common.
As shown in Fig. 4.1, an ideal phased array receiver compensates for the time delay difference between the signals from different antennas and combines the signals coherently to enhance the reception from the desired direction(s), while rejecting emissions from other unwanted directions. Thus the receiver is capable of nulling out interferers as long as they don't originate from the same direction as the signal [2].
The radiated signal arrives at different times at each of the spatially separated antennas; the time delay difference between two adjacent elements is related to their distance d and the signal angle of incidence with respect to the normal ϑ by:

$$c \cdot \tau = d \cdot \sin \vartheta \tag{1}$$

where c is the speed of light. In general, the signal arriving at the first antenna element is given by:

$$S_0(t) = A(t) \cdot \cos\left[\omega_c \cdot t + \varphi(t)\right] \tag{2}$$

where $A(t)$ and $\varphi(t)$ are the amplitude and phase of the signal and ω_c is the carrier frequency.
The signal received by the nth element can be expressed as:

$$S_n(t) = S_0(t - n\tau) = A(t - n\tau) \cdot \cos\left[\omega_c \cdot t - n \cdot \omega_c \cdot \tau + \varphi(t - n \cdot \tau)\right] \tag{3}$$

The equal spacing of the antenna elements is reflected as a progressive phase difference $\omega_c\tau$ and a progressive time delay τ in *A(t)* and *φ(t)*.

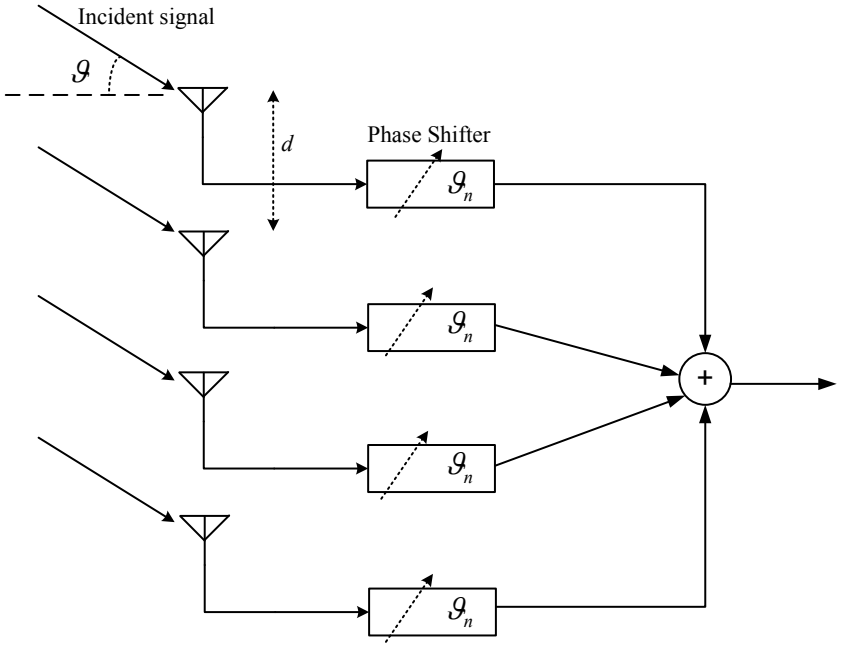

Figure 4.1: A generic phased array architecture

Adjustable time-delay elements τ'_n can compensate the signal delay and phase difference simultaneously. The combined signal $S_{sum}(t)$ can be expressed as:

$$\begin{aligned} S_n(t) &= S_{sum}(t) = \sum_{n=0}^{n-1} S_n\left(t-\tau_n'\right) \\ &= \sum_{n=0}^{n-1} A\left(t-n\cdot\tau-\tau_n'\right)\cos\left[\omega_c\left(t-n\cdot\tau-\tau_n'\right)+\varphi\left(t-n\cdot\tau-\tau_n'\right)\right] \end{aligned} \tag{4}$$

For $\tau'_n = -n\tau$ the total output power signal is given by:

$$S_{sum}(t) = n\cdot A(t)\cdot\cos\left[\omega_c\cdot t+\varphi(t)\right] \tag{5}$$

For narrow-band systems, the true-time delay necessary in each element of the phased array can be approximated by a phase shift because *A(t) and φ(t)* chance slowly relative to the carrier frequency, i.e., when τ is much less than the symbol period, we have:

$$\begin{aligned} A(t) &\approx A(t-n\cdot\tau) \\ \varphi(t) &\approx \varphi(t-n\cdot\tau) \end{aligned} \tag{6}$$

Thus, the phase shifter provides a phase shift to each *n*th signal path which, to add the signals coherently, should be given by:

$$\vartheta_n = n\cdot\omega_c\cdot\tau \tag{7}$$

This approximation leads to some signal dispersion, due to the non-constant group delay, which increases as the bandwidth of the signal increases. This dispersion translates to a higher bit error rate (BER). However, for the bandwidths of interest in this work (0.88GHz around 60GHz) this error is relatively low.

4.1.2 Phased array sensitivity improvement

As mentioned, a phased array system relaxes the noise requirements for individual active devices used in the array and improves the overall sensitivity [3].
For a given receiver sensitivity, the output SNR sets an upper limit on the noise figure of the receiver. If we consider the n-path phased array receiver shown in Fig.4.2, since the input signal add coherently, the combined output is given by:

$$S_{out} = n^2 \cdot G_1 \cdot G_2 \cdot S_{in} \tag{8}$$

where G1 and G2 correspond to the gains before and after signal combining.

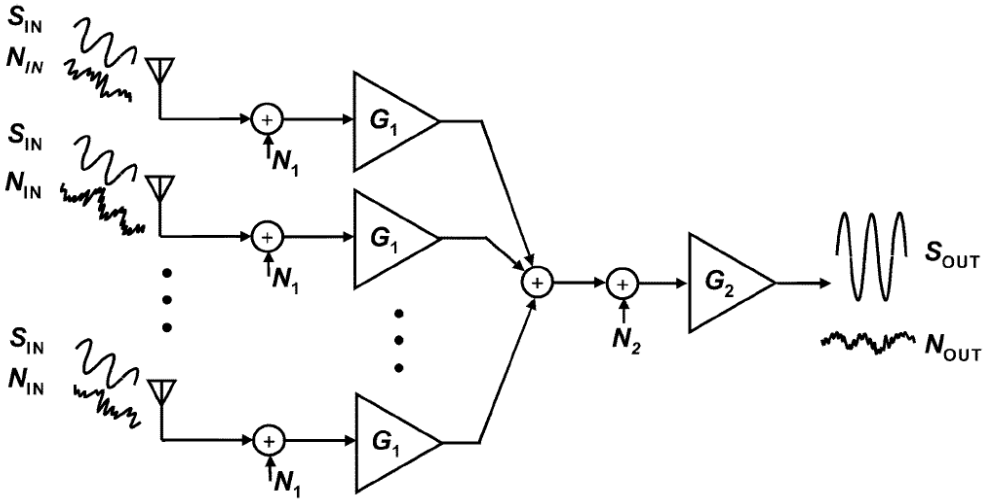

Figure 4.2: Phased array SNR improvement

In general, the amount of SNR improvement in a phased array receiver depends on the nature and location of the objects in the environment that generate noise, correlation between such noise generators, multipath effects, coupling between antenna elements, input impedance mismatch and the antenna beam pattern. Assuming that the antenna noise contributions in different elements are uncorrelated, the output total noise power is given by:

$$N_{out} = n\left(N_{in} + N_1\right) G_1 \cdot G_2 + N_2 \cdot G_2 \tag{9}$$

where N_1 and N_2 are the input referred noise contributors of the stages corresponding to gains G_1 and G_2, and N_{in} is the noise at the input of each antenna.
Thus, compared to the output SNR of a single-path receiver, the output SNR (S_{out}/N_{out}) of the array can be improved by up to a factor *n* depending on the noise and gain contribution of different stages.

To simplify now consider G_2=1. The array noise factor F can be expressed as:

$$F_{array} = \frac{S_{in}}{N_{in}} \cdot \frac{n\left(N_{in} + N_1\right) \cdot G}{n^2 \cdot G \cdot S_{in}} = \frac{F_{\text{single\_receiver}}}{\text{n}} \qquad (10)$$

Thus an n-element receiver can improve the sensitivity by 10log(n) in decibels compared to a single-path receiver. For instance, if the noise from the antennas is uncorrelated, an eight-path phased array can improve the receiver sensitivity of 9dB.
The higher SNR at the output together with the lower interference translate into higher channel capability, while the directivity of the transmit-receive pairs can result into higher frequency reuse ratios and consequently higher network capabilities.
Furthermore, the noise requirements relaxation on each single receiving chain could also allow us to remove the LNA from each chain, without leading to an intolerable performance degradation.
This is only an hypothesis, but if it could be done all the challenges related to the hardly predictable parasitics and dummies effect on matching and gain performances of a 60GHz LNA (see chapter III) would be overcome.

4.1.3 Phased array configurations

As mentioned, for narrow-band application, controllable phase shifters are needed to compensate for the phase shift between the input signals in order to add them coherently.
There are four basic possibilities to perform beamforming, depending mainly on where the phase adjustment is performed. These configurations, which are shown in Fig. 4.3, are known as RF phase-shifting (a), local oscillator phase shifting (b), IF or baseband phase shifting (c) and digital beamforming phased array [4].
In the RF phase shifting architecture, different RF path are phase shifted and then combined at RF frequency. The combined signal is then down-converted, using a single mixer, to the IF or baseband.
In this architecture the spatial filtering of the undesired signals is performed at the combination point prior the mixer. Hence, the upper dynamic range requirements of the mixer are relaxed and the level of unwanted in-band inter-modulations after mixer decreases. Furthermore, only one mixer is needed, leading to area saving and overcoming the important problem related to LO distribution.
The design of the phase shifters (they must perform low and constant insertion loss and high phase linearity versus control voltage) in silicon, however, remains a challenge in this architecture together with the lossy signal recombination at RF frequencies [5].
The main advantage of the LO phase shifting architecture (Fig. 4.3(b)) over the RF phase shifting is that the phase shifter losses, non-linearity and noise performance do not directly affect the receiver performance. Furthermore the signal combination can be performed at baseband frequency, which imposes

less challenges. However, the number of components (mixers) is larger leading to more silicon chip area and higher costs. Besides, since the combining of signals and beamforming are performed after mixers, in-band intermodulations are stronger, leading to more stringent linearity requirements for the mixers.

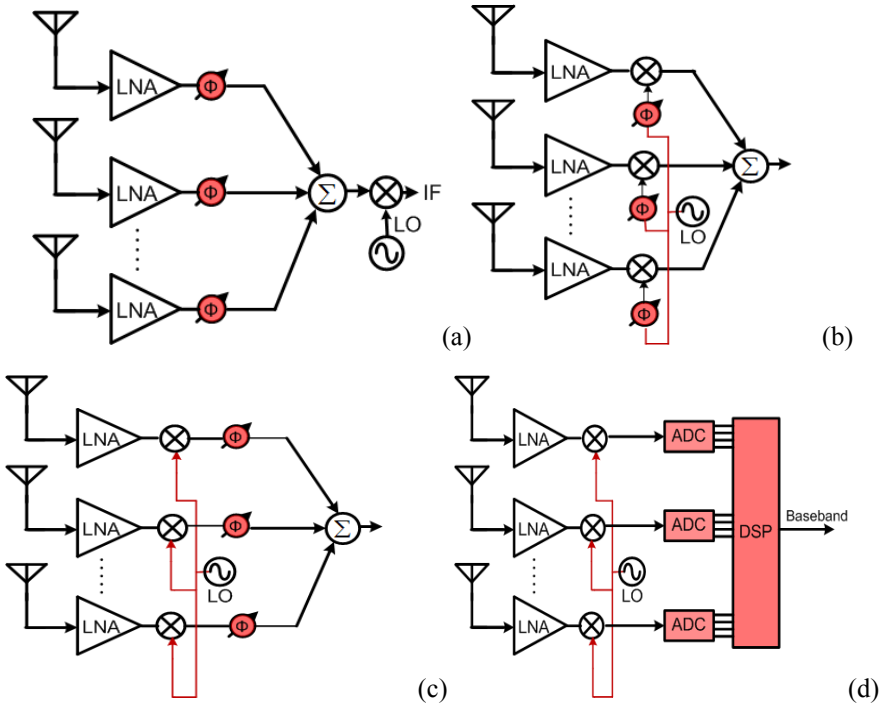

Figure 4.3: Phased array configurations: (a) RF phase shifting , (b) LO phase shifting, (c) IF phase shifting, and (d) digital beamforming array.

Another downside of this approach is that the large LO signal needs to be routed and distributed to the different antenna paths, leading to issues concerning cross-talk, phase coherence and increased power dissipation.
In the phase shifting architecture of Fig. 4.3(c), the phase shifters are placed at the first IF stage. The phase-shifted IF signals are combined before downconversion to baseband. As compared to RF phase shifting architecture, some of the challenges in phase shifter design are relaxed. However, since it needs a large number of mixers, this architecture is not a proper option for low cost and low power phased array receiver. Furthermore, LO distribution continues to represent a challenge.
If a direct-conversion architecture is considered, phase shifting and signal combining are performed entirely at the analog baseband. It is a more robust design because it is less sensitive to parasitic than mm-Wave circuits. In this case, the beamformer must fits in a direct downconversion receiver which yields baseband I and Q components for the received signal at each path. Those signals must be individually phase-shifted and combined to generate a single beamformed I/Q output.
At baseband phase shifters can be easily implemented using digitally controlled variable-gain current amplifier (VGAs) [6].

Figure 4.3(d) illustrates the digital array architecture: down-converted to a suitable IF frequency, each RF path is digitized by an analog-to-digital converter (ADC) and all outputs are passed to a digital signal processing (DSP) unit, which execute all tasks of beamforming and recovering the desired signal from the undesired interferences.
The dynamic ranges of mixers and ADCs must be high enough to withstand the probable strong interferences. In case of WPAN, since the data rate may exceed 2Gb/s, very high-speed ADC's are required and to accommodate the required dynamic range each ADC must have a large number of bits which increases the ADC cost and power consumption extensively.

4.1.4 LO distribution problem

In all architectures, except the RF recombination one, LO distribution represents a difficult task. If we consider a direct-conversion receiver as the prime candidate also the problems related to LO generation must be mentioned. The generation of I and Q phases of LO at 60GHz entails two issues: (a) quadrature operation typically degrades the phase noise considerably if classical coupled-oscillators are exploited and (b) the comparatively low tank Q results in serious design trade-offs [7].
Concerning the LO distribution problem, the quadrature outputs of the coupled-VCOs must travel large distances thus experiencing significant losses and mismatches which, with no buffer following the VCO, further degrade phase noise.
These problems could be largely overcome by somehow combining the LO generation and distribution tasks through the use of a spatially distributed oscillator. I/Q LO signals have to be generated and directly available at the spatially separated I/O LO ports of each direct down-conversion mixer without the need for a lossy distribution network. In practice the network that distributes the LO has to be formed by the oscillator itself: this can be done through the use of coupled rotary travelling wave VCOs.
Once the n-paths signals are down-converted at analog baseband they can be individually phase-shifted and combined to generate a single beamformed I/O signal through the use of variable gain current amplifiers (VGAs) and transimpedance amplifiers (TIAs) as done in [6].
This kind of phased array receiving architecture, with such an LO distribution system, would allow both to improve the overall receiver sensitivity by a factor $10\log(n)$, by virtue of phased array coherent combination properties, and to reduce, at the same time, the LO phase noise by the same factor, since in principle, for an n-path phased array receiver, n identical coupled oscillator are exploited. This aspect will be widely discussed and proved in the following paragraphs.
The I/Q down-conversion mixer topology we intend to use is a current-driven passive mixer with baseband differential feedback cascode amplifier (Fig. 4.4), optimized both to provide a low input impedance and to achieve the lowest possible output noise.
These mixer topology has been chosen mainly because MOS switches are always in triode region making the overall circuit more robust to high

frequency device modeling errors. This topology also allows good linearity and no flicker contribution by the mixer switches.
The MOS switches size and their gate DC bias are chosen considering both the RF input impedance needed to facilitate the input matching, the minimization of the switches gate capacitance which directly affects the VCO tuning range and the noise figure minimization.

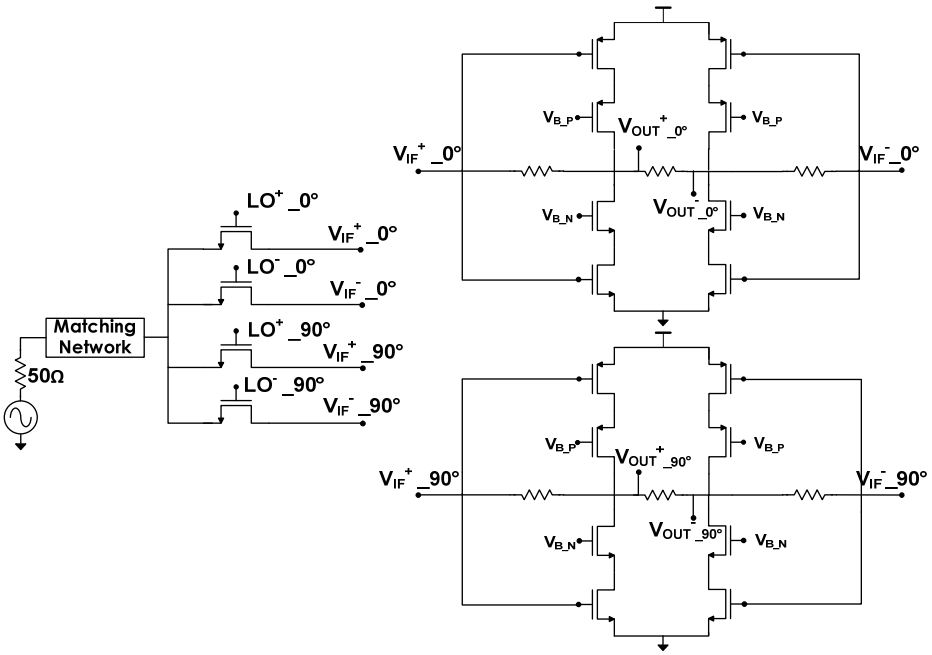

Figure 4.4: I/Q current-driven passive mixer schematic

A transmission-line based broadband input matching network provides and S_{11}<-13dB over a bandwidth of about 28GHz around 58GHz providing design robustness to process, voltage and temperature parameter, but mainly overcoming problems related to not perfect modeling and excessive sensitivity to the device models itself.
In the following paragraphs the LO generation and distribution design will be widely discussed.

4.2 The LO distributed approach

4.2.1 Travelling wave oscillators principle

As mentioned in the previous section, multiphase oscillation signals (also I and Q) are classically generated by active coupling between two identical LC-tank oscillators [8], [9]. However, the presence of the coupling transistors substantially increases the capacitive loading of the tank, causing significant degradation in the operating frequency and the phase noise, especially for applications at the millimeter-wave regime.

An alternative to this approach which allows to greatly improve the multi-phase VCO performances is the use of distributed rotary travelling wave oscillators (RTWOs).
While the LC voltage-controlled oscillator (LC-VCO) is widely used in RF oscillators, the wave-based oscillators and in particular rotary travelling wave oscillators have gained recent interest as possible alternatives.
Among a variety of wave-based oscillator, the rotary travelling wave oscillator has the unique property of sustaining a traveling wave while achieving low power and low phase noise. Since the signal propagates in one direction along the transmission line, multiple-phase signals are easily available by tapping off the signals from different positions on the transmission line: this is extremely useful for easily obtaining accurate high frequency quadrature signal generation from a single VCO [10].
The typical circuit topology of the RTWO is illustrated in Fig. 4.5.

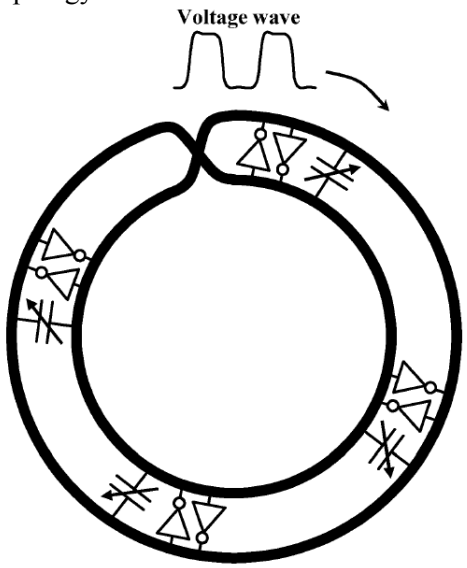

Figure 4.5: Typical circuit topology of an RTWO

A twisted differential transmission line forms a closed loop for the required feedback. Such a structure can be viewed as a distributed amplifier whose output is fed back to its input with 180° phase rotation to satisfy Barkhausen's criteria (360° total phase shift). As a distributed amplifier achieves a higher gain-bandwidth product by absorbing the parasitic capacitances of transistors into transmission lines, correspondingly in a distributed oscillator transistor parasitic are distributed into coupling transmission lines to alleviate tuning range limitations of VCOs.
Distributed cross-coupled inverters compensate for the loss of the transmission line in order to give a loop gain higher than unity and voltage variable capacitors can be insert to adjust the frequency of operation. Start up can occur in either direction, but in the steady state, the direction of propagation will have been determined by the path that offered the lowest losses. Once the wave becomes established, it takes little power to sustain it, because unlike a ring oscillator, the energy that goes into charging and discharging MOS gate capacitance becomes transmission line energy, which is recirculated in the closed electromagnetic path.

Furthermore, the differential mode (odd mode) of propagation provides well-defined "go" and "return" path which gives predicable inductance characteristics in contrast to the uncertain return-current path for single-ended signal distribution.

4.2.2 Coupling issue

As said in the previous section, the problems related to I/Q LO generation and distribution in a baseband recombination based phased array receiver can be largely overcome by somehow combining the LO generation and distribution tasks through the use of a spatially distributed oscillator. This approach avoids the use of lossy distribution networks in which a large portion of the power would be "wasted", leading to high phase noise.

I/Q LO signals have to be generated and directly available at the spatially separated I/O LO ports of each direct down-conversion mixer.

As just mentioned, through the simple rotary travelling wave loop of fig. 4.5 accurate high frequency quadrature signal generation can be easily obtained. However, a way to provide the different I/Q LO signals to the various I/Q LO ports of the *n* parallel mixers used in the phased array receiver must be found. These LO signals must have well defined phase relationships, i.e. either all in phase or with fixed phase shifts. This concept is qualitatively described in Fig. 4.6.

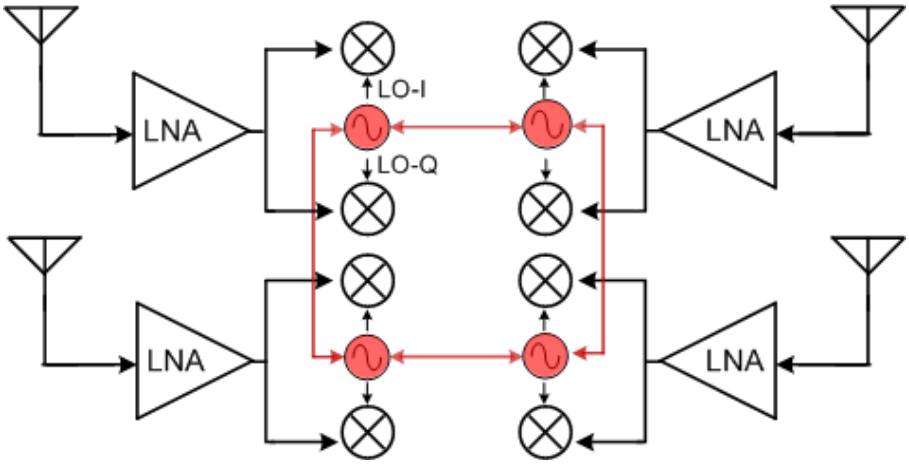

Figure 4.6: LO distribution concept

Starting from the single RTWO loop, such a "synchronized" LO can be performed in different manners, some of that are shown in Fig. 4.7.

In both cases four RTWO loops are coupled through transmission lines, creating a bigger loop which contains some 45° branches of the original loops. The total phase shift around the big loop must be $\Phi_e=2K\pi$, where K can be 1,2,3 etc. In the distribution systems reported in Fig. 4.7 K=2 giving a total phase shift of 720°. Note that in any differential t-line section which forms the loop a travelling wave is sustained.

Also a single twisted loop (2N+1)π/2 long could be used for the same purpose.

In such types of distribution systems multiple oscillation modes become possible and the only way to remove or at least reduce the unwanted modes (lower or higher harmonics) is to perform a sort of g_m shaping to ensure that the negative resistance provided by cross-coupled pairs is sufficiently high to sustain oscillation only at the desired frequency.

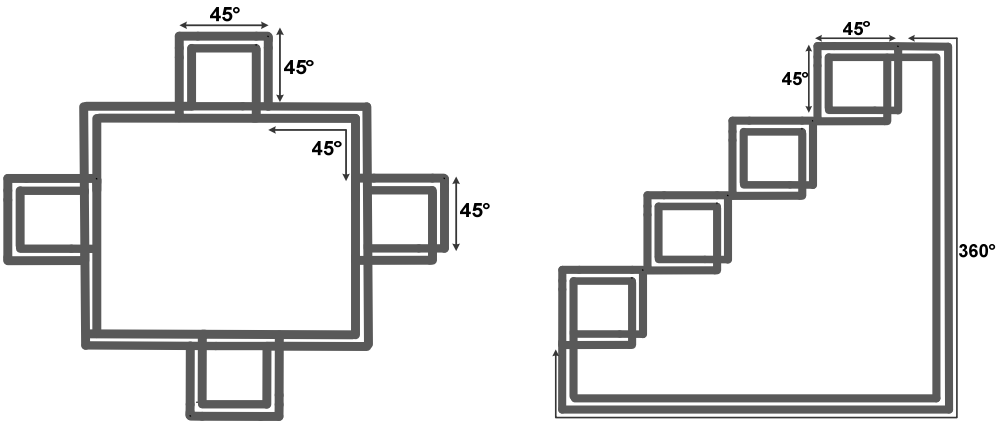

Figure 4.7: large signal effects

Techniques similar to those used for harmonics removal in crystal oscillators can be used [11]. Cross-coupled pairs can be modified adding a series LC network in parallel to the gate-source capacitance and a shunt LC network between the source terminal and ground. This approach, with a proper LC sizing, allow to perform a band-pass g_m shaping around the desired frequency.

This type of g_m shaping however leads, if the frequencies that must be suppressed are relatively close to the desired one, to a strong reduction of the in-band g_m which causes, given the already strong line- lengthening performed by MOS devices, great challenges for the single-loop design .

In our design this problem is overcome by adopting an "hybrid" travelling-standing wave structure: the travelling wave loop, formed by 4 identical loaded t-line 45° branches plus one twist to obtain a total phase shift of 2π, is biased through the insertion of two shorted λ/4 transmission lines.

The bias current of the TWO core is provided at the short-circuited ends of these t-lines, which are connected to the main loop at two opposite loop corners in order to maintain symmetry, as shown in Fig. 4.8.

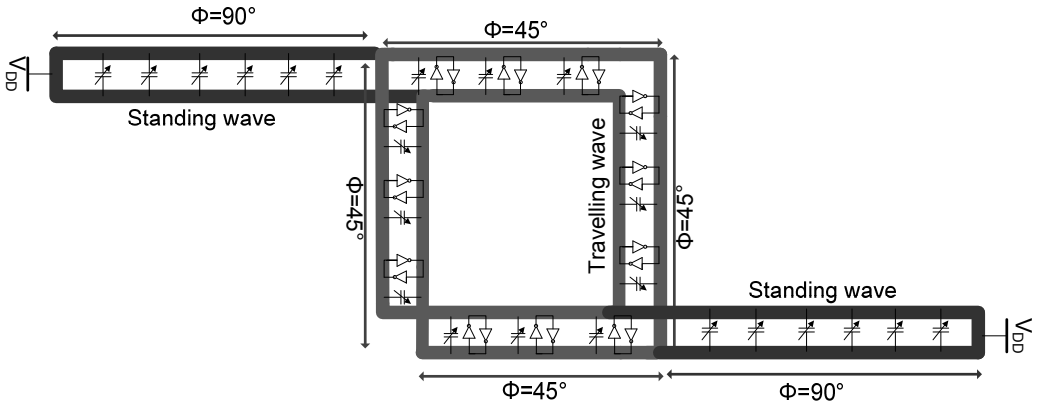

Figure 4.8: single loop hybrid RTWO-SWO

In practice, two standing wave oscillators are physically connected to the rotary travelling wave loop and, due to the injection locking mechanism, are forced to work at the same oscillation frequency: the overall structure thus behaves as a single oscillator. By virtue of this injection locking mechanism, coupling between different RTWO loops is performed through these λ/4 transmission lines.

As will be most widely described in the next sections, loops are physically connected at the circuited ends of the λ/4 shunt transmission lines through the insertion of a coupling resistances R_C. This resistance is required only to provide the bias current to the various loops and, as will be explained in detail in the following paragraphs, it hinders the coupling mechanism: if this resistance would ideally be infinite, not only the two loops would be synchronized, but they would work perfectly in-phase (this is why R_C is omitted in Fig. 4.9).

This connection gives rise to a sort of "virtual shorting" of each λ/4 t-line, such that each line sees the wave coming from the other connected λ/4 t-line towards the connection as its own incident wave after reflection at the virtual short (Fig.4.9).

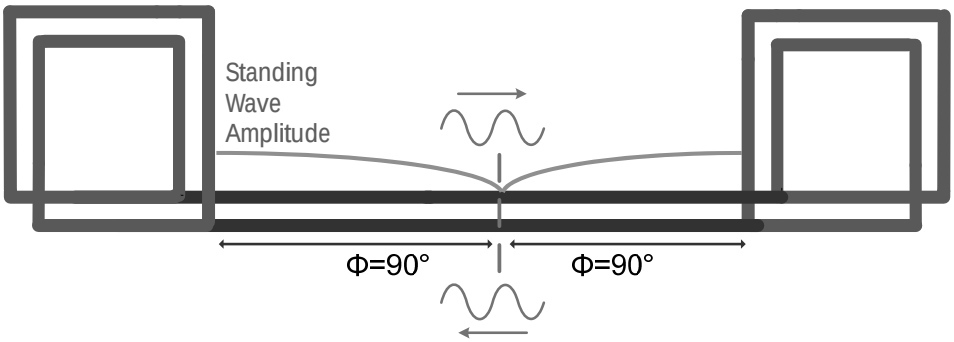

Figure 4.9: virtual shorting

The single loop design is discussed in the next section.

4.3 LO generation and distribution system design

4.3.1 Single RTWO loop design

As said in section 4.2.1, in a distributed oscillator transistor parasitic are distributed into coupling transmission lines alleviating tuning range limitations and phase noise degradation. To take advantage of this important property as much as possible the cross-coupled active devices needed to compensate for line losses must be distributed along the loop to the higher possible degree. This allow to consider active devices as part of the line, to create a "new line" with changed parameters avoiding strong discontinuities that would be inevitably formed concentrating the negative resistance in one place along the loop. Such a discontinuity would give origin to strong reflection phenomena leading to the formation of a standing wave
Another important consideration has to be made regarding the need to connect at some points along the loop line the I/Q LO ports of the passive mixer; since each of the differential LO port of the mixer (in reality a buffer is interposed between VCO outputs and the LO mixers port, as will be shown at the end of the chapter) exhibits a differential capacitance C_{MIX} of about 20fF, about 40fF of total differential capacitance (20fF for the I port and other 20fF for the Q port) has to be accommodated along the loop without creating strong discontinuities and trying to chance as less as possible the "loop shape".
To avoid discontinuities creation in the points where the mixer LO ports are connected, part of the differential t-line forming the loop must be replaced by series lumped inductors plus the capacitive mixer loading (Fig 4.10 (a)): the lumped inductors values L_S are chosen on the basis of the unloaded t-line parameters and C_{MIX} value in order to "*emulate*" the T-line behavior in a lumped manner.

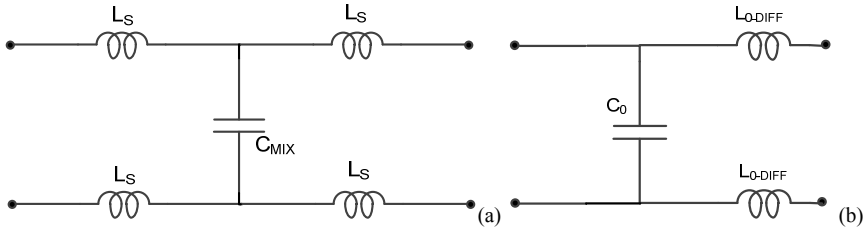

Figure 4.10: (a) lumped manner T-line behavior emulation, (b) ideal T-line modeling

In particular, given the unloaded differential T-line model of Fig. 4.10 (b) the lumped inductance value L_S is given by:

$$L_s = \frac{L_{0-DIFF}}{2} \cdot \frac{C_{MIX}}{C_0} = Z_0^2 \cdot \frac{C_{MIX}}{4} \qquad (11)$$

where Z_0 is:

$$Z_0 = \sqrt{\frac{2 \cdot L_{0-DIFF}}{C_0}} \tag{12}$$

Observing Eq. 11 it's easy to understand that the higher C_{MIX}/C_0 is the higher is the value of L_S that must be added and consequently the higher is the portion of the differential t-line that must be eliminated in order to maintain a 360° phase shift around the loop.

If a too high portion of the line has to be sacrificed to connect the LO mixer ports, the distributed nature of the TRWO comes failing at the cost of lower overall performances and, even if a traveling wave would still be sustained it would become in practice impossible to physically lay-out the loop because the t-line available length wouldn't be sufficient even to realize the loop corners.

Thus the capacitance per unit-length C_0 of the differential T-line used to lay-out the loop must be sufficiently high to minimize the total physical width of the differential line given by $2W+S$ (see Fig. 4.11). This ensure to obtain relatively high t-line aspect ratios K:

$$K = \frac{l}{2 \cdot W + S} \tag{13}$$

even over t-line lengths l in the order of 45°, making easier to lay-out the loop and ensuring minimal coupling between the parallel branches of the loop.

To maximize the capacitance per unit-length means to minimize the t-line characteristic impedance Z_0; notice that lowering the unloaded t-line Z_0 leads to high power dissipation.

The differential t-line has been designed and optimized with the aid of several Agilent Momentum EM simulations on different t-line structures. The shielded t-line approach used for the SWO and the LNA designs (chapters II and III) is exploited also in this case. Now, however shielding is performed by means of floating metal strips located underneath the guiding structure realized on the metal layer M_5. The distance between two consecutive bars has been set to 1µm in order to minimize the field penetration.

The use of floating M_5 metal strips allows to obtain the desired t-line characteristics in terms of C_0, Z_0 and Q with a thinner structure (with an higher aspect ratio K) if compared to the classical M_1 shielding solution .

The designed t-line is shown in Fig. 4.11.

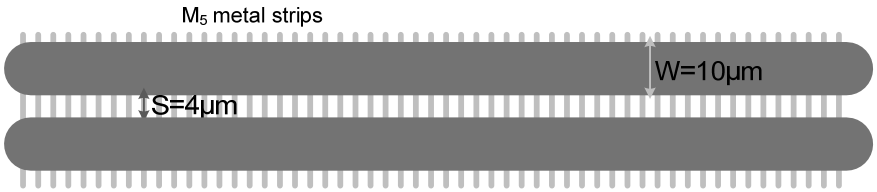

Figure 4.11: the designed shielded differential t-line

The t-line, properly prefilled with dummies to reach the local density requirements, has been electromagnetically simulated: it exhibits a characteristic impedance Z_0 of about 42Ω, a capacitance per unit-length C_0 of 1.09fF and a differential inductance $L_{0\text{-}DIFF}$ per unit length of nearly 0.9pH. The simulated quality factor Q is 15.5.

Obtaining similar values with a M_1 shielded t-line would require W= 32μm and a spacing between lines S of 8μm resulting in a exceedingly large structure.
A circuital model for each 1° (with corresponds to a physical length of nearly 4.5μ) of line has been extracted from EM simulation and used for Cadence circuital simulations (Fig 4.12).

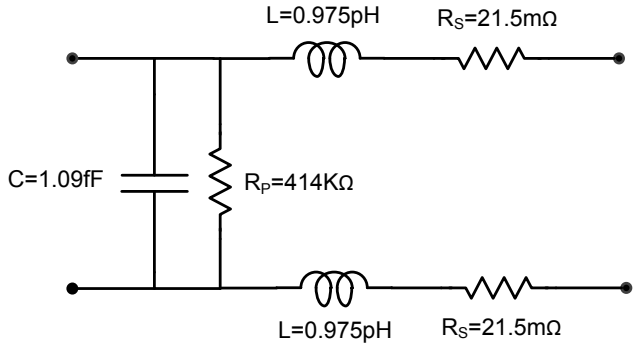

Figure 4.12: circuital t-line modeling

As just said, λ/4 shunt t-lines are used to bias the loop and perform coupling. Keeping the length of these lines the highest possible is very important in order to be able to provide the LO signal to the I/Q LO mixer ports of all the receiving paths of the phased array system. For this reason these t-lines are periodically loaded only with varactors, while the negative resistance needed for shunt t-line losses compensation is provided by over-sizing the cross-coupled pairs distributed along the loop.
For design porposes, the loop differential transmission line is segmented into N identical blocks formed by 2° of unloaded transmission line plus properly sized cross-coupled NMOS active device: each single segment circuital model is shown in Fig. 4.13.

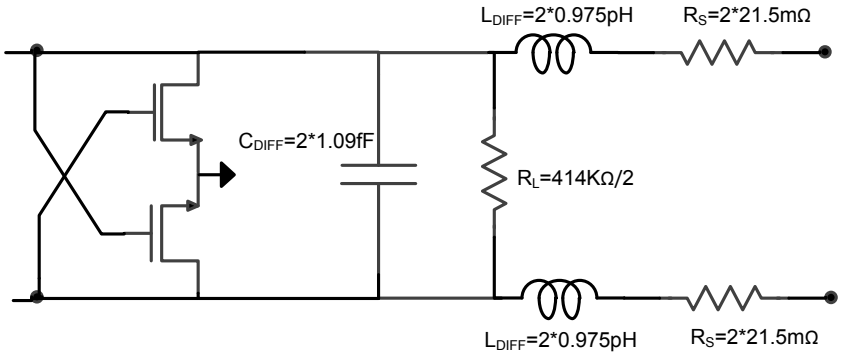

Figure 4.13: Single line segment model

The phase velocity v_p of the wave travelling along the loop is given by:

$$v_p = \frac{1}{\sqrt{C_0 \cdot L_{0-DIFF}}} \qquad (14)$$

where C_0 and $L_{0\text{-}DIFF}$ are respectively the differential capacitance and differential inductance per unit-length of the line.

The wave after one lap is inverted due to the twist. Thus, two laps are needed to complete one cycle.
The oscillation frequency than can be given as:

$$f_0 = \frac{v_p}{2 \cdot l} = \frac{1}{2 \cdot l} \cdot \frac{1}{\sqrt{L_{0-DIFF} \cdot C_0}} = \frac{1}{2 \cdot N \cdot \sqrt{L_{DIFF} \cdot C_{DIFF}}} \quad (15)$$

where N is the number of needed segments and C_{DIFF} and L_{DIFF} are the total capacitance and inductance associated with each single segment.
To start with, the dimensions of the cross-coupled active devices of each segment must be set.
The total equivalent resistance seen looking into any section of the loop is given by:

$$R_P = \frac{1}{\left| g_{LOSS} - g_m \right|} \quad (16)$$

As the g_m of the active pairs increases from zero, the total parallel resistance increases and becomes infinite if $g_m=g_{LOSS}$ (unity loop gain). If the g_m is further increased R_P becomes negative and its absolute value tends to decrease as the g_m increases.
To obtain a loop gain of nearly 2.5:

$$R_P = \frac{1}{g_{LOSS} - 2.5 g_{LOSS}} \rightarrow R_P = \frac{2}{3} \frac{1}{g_{LOSS}} \quad (17)$$

each cross-coupled pair must perform a g_m of nearly 1.05mS.
To perform such a g_m value the NMOS devices in each line section are one finger devices with L_f=65nm and W_f=450nm.
The equivalent capacitance related to the active devices for each sections, dominated by the device oxide one C_{OX}, is approximately 3.4fF, that is about 60% of the total segment capacitance.
Since the total phase shift around the loop increases with the total capacitance, MOS loading translates in a strong line-lengthening: according to eq.15 the numbers of segments for each 45° loop branch must be reduced to maintain the same oscillation frequency from 32 to 20, which corresponds to a line shortening of nearly 17° (equal to the MOS loading equivalent lengthening).
As already explained, the loop oscillation frequency is proportional to the phase velocity of the sustained travelling wave (Eq. 14). So the most straightforward way of performing oscillation frequency tuning is to change the wave phase velocity by periodically loading the t-line with varactors: the idea is to load each single line segment of Fig.4.10 with the same variable varactor capacitance amount.
Thus, the maximum and minimum oscillation frequency are analytically given by:

$$f_{Max} = \frac{1}{2 \cdot N \cdot \sqrt{L_{DIFF} \cdot \left(C_{DIFF} + C_{MOS} + C_{MIN} \right)}} \quad (18)$$

$$f_{Min} = \frac{1}{2 \cdot N \cdot \sqrt{L_{DIFF} \cdot \left(C_{DIFF} + C_{MOS} + C_{MAX} \right)}} \quad (19)$$

where C_{MOS} is the fixed capacitance amount given by active devices, while C_{MIN} and C_{MAX} are respectively the total minimum and maximum differential varactor capacitance.

Since the design kit of the used 65nm TSMC CMOS technology doesn't provide scalable MOS varactor models for the accumulation MOS varactor explained in chapter 1, a custom scalable *Verilog-A* model has been developed on the bases of experimental data.

The varactor characterization has been carried out from S-parameter measurement on a dedicated on-wafer test-structures using three steps de-embedding procedures (see. Appendix 1). Device capacitance, as a function of the voltage between the gate electrode and n-well, has been derived carrying out measures on 60 fingers devices with different finger sizes.

The measured capacitive curve of a 1-finger a-MOS varactor device with finger length L_f=60nm and finger width W_f=0.5μm is shown in Fig.4.14. The device performs a small-signal C_{MAX}/C_{MIN} of nearly 1.8.

We have not been able to extract the value of the varactor series resistance probably because the whole device impedance is too close to the edge of the Smith chart; maybe using DUTs with a much larger number of fingers it would have been possible to extract it.

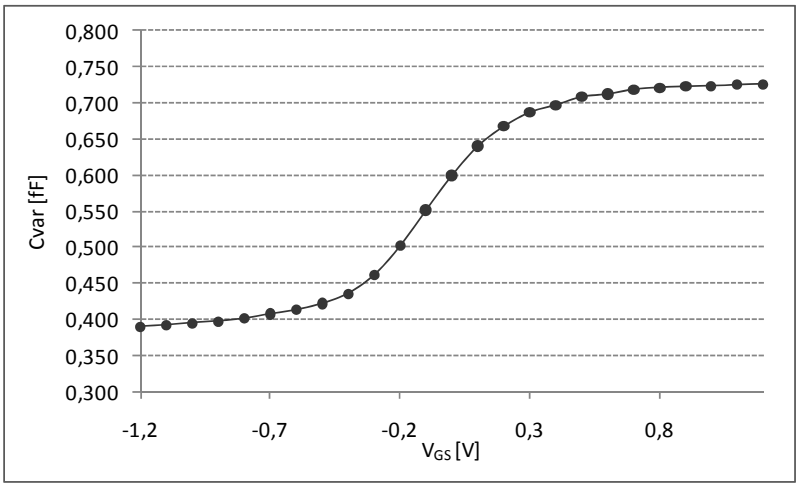

Figure 4.14: Measured varactor capacitive curve

Exploiting the hyperbolic tangent function an analytical curve which perfectly fits the measured data samples has been found:

$$C_{VAR} = 0.558\,fF + 0.168\,fF \cdot \tanh\left[(V_{GS} + 0.1) / 0.4 \right] \quad (20)$$

and a *Verilog-A* model for the 1-finger varactor lossless capacitance has been created on the bases of this fitting function.

A fixed value resistance has been added in series to the capacitance *Verilog-A* model supposing a conservative minimum varactor quality factor Q of nearly 10.
How to find the number of varactor finger N_f in each loop section required to obtain a tuning range of nearly 8GHz around 60?
Since the varactor Q is independent on the number of parallel varactor fingers, the minimum quality factor of the total varactor capacitance in each cell remains nearly 10. Since the unloaded t-line Q is about 15 and the ever present parasitic resistance of cross-coupled pair tends to reduce the equivalent loaded t-line Q further, it can be supposed that the required transconductance value, once the varactors are added to the loop, is nearly doubled. In reality, the cross-coupled pair size has been more than doubled because the g_m has to be sufficiently high to compensate with some margin also for the losses of the varactors which load the two shunt λ/4 t-lines.
Based on these considerations each cross-coupled pair has been re-sized to obtain a g_m of nearly 3.5mS; two fingers devices with L_f=65nm and W_f=750nm ensure this g_m value.
The transistors size increase leads to a further equivalent line-lengthening: since the equivalent capacitance related to the active devices for each sections is now nearly 8.5fF, once according to Eq.15, the numbers of segments for each 45° loop branch must be further reduced from 20 to nearly 13.
Once known the number of segment N, from eq. 18 and 19 the number of varactor fingers N_f required in each line segment to obtain the desired tuning range can be found by:

$$f_{Max} = 64GHz = \frac{1}{2 \cdot N \cdot \sqrt{L_{DIFF} \cdot \left(C_{DIFF} + C_{MOS} + N_f \cdot C_{finger-MIN}\right)}}$$
$$f_{Max} = 56GHz = \frac{1}{2 \cdot N \cdot \sqrt{L_{DIFF} \cdot \left(C_{DIFF} + C_{MOS} + N_f \cdot C_{finger-MAX}\right)}} \quad (21)$$

where $C_{finger-MIN}$ and $C_{finger-MAX}$ are respectively the minimum and maximum varactor finger capacitance.

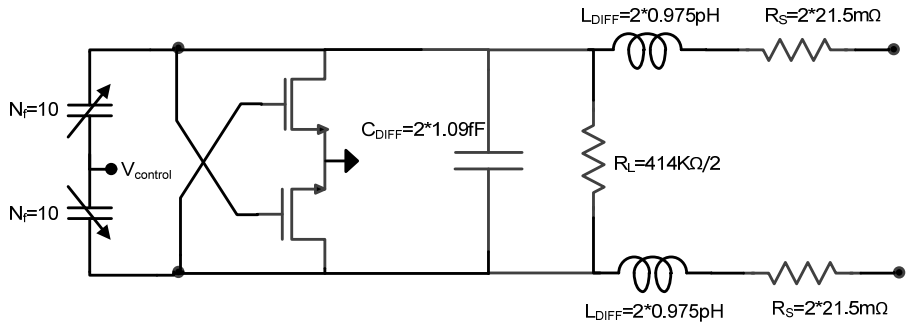

Figure 4.15: Final circuital model of each line section

Based on Eq. 21, the required number of varactor fingers for each loop section is approximately N_f=10. The final circuital model of each cell is shown in Fig. 4.15.

To obtain for the shunt λ/4 t-lines nearly the same tuning range, ensuring injection locking, 8 varactor fingers need to be placed each 2° of line.
As already said at the very beginning of this paragraph, about 40fF of total differential capacitance, 20fF for the I Mixer LO port and other 20fF for the Q port, has to be accommodated in some points along the loop.
In order to "emulate" in a lumped manner the behavior of the transistors and varactors loaded transmission line the "mixer/buffer block" of Fig. 4.10(a) must be modified by adding in parallel to the mixer differential capacitance C_{MIX} a cross-coupled pair and varactors fingers with the correct proportionality ratio: since C_{MIX}/C_{DIFF} is about 10 both the number of varactor fingers N_f and the cross-coupled devices size must be 10 times higher than those contained in each t-line section.
In Fig. 4.16 the mixer cell schematic is reported.

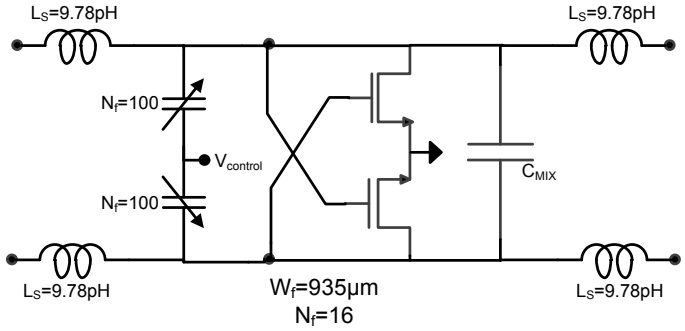

Figure 4.16: final mixer-buffer cell

The two mixer cells insertion needs for a proper line shortening: the number of section *N* for each 45° loop branch has to be reduced from 13 to 8.
The simulated RTWO tuning range goes from a minimum frequency of nearly 57.5 GHz to a maximum one of about 64.8GHz.
The phase noise at the highest oscillation frequency is reported in Fig. 4.17.

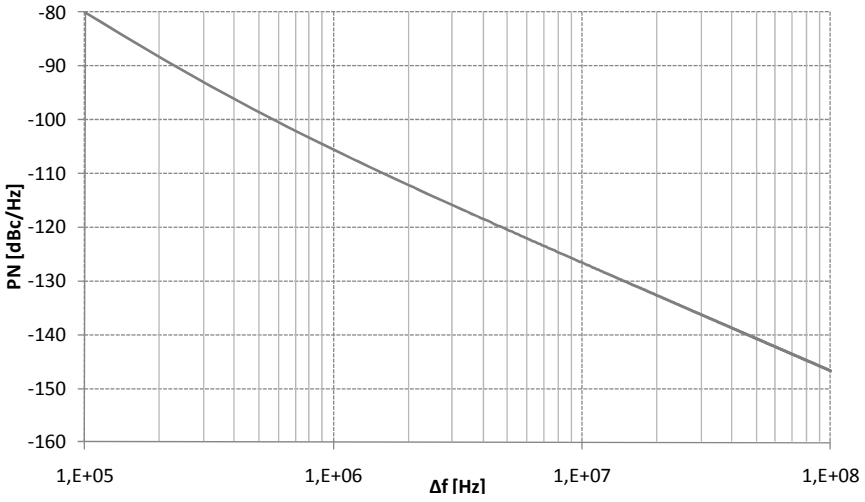

Figure 4.17: RTWO phase noise

The phase noise at 10-MHz offset from the carrier results nearly -126.7 dBc/Hz. The RTWO consumes nearly 30.5mW when operated with a 1.2V supply and presents a figure of merit of -188 dBc/Hz:

$$FOM = -PN(\Delta f) + 20 \cdot \log\left(\frac{f_0}{\Delta f}\right) - 10 \cdot \log(P_{DISS}) \approx -188 dBc/Hz \quad (22)$$

The fact that the simulated tuning range is slightly lower than expected, based on the varactor C_{MAX}/C_{MIN} ratio, is due to the large signal effects: the large oscillating signal in fact is directly applied to the gates of varactors changing instantly during the oscillation period the actual voltage V_{GS} across the varactors.

Fig. 4.18 clearly shows that progressively increasing the sinusoid amplitude the effective tuning range C_{MAX}/C_{MIN} tends to fall more and more, from the initial value of 1.84 (blue dotted line) until it reaches a value of nearly 1.6 if a sinusoid with a 2.4V peak-to-peak differential amplitude is applied (red line).

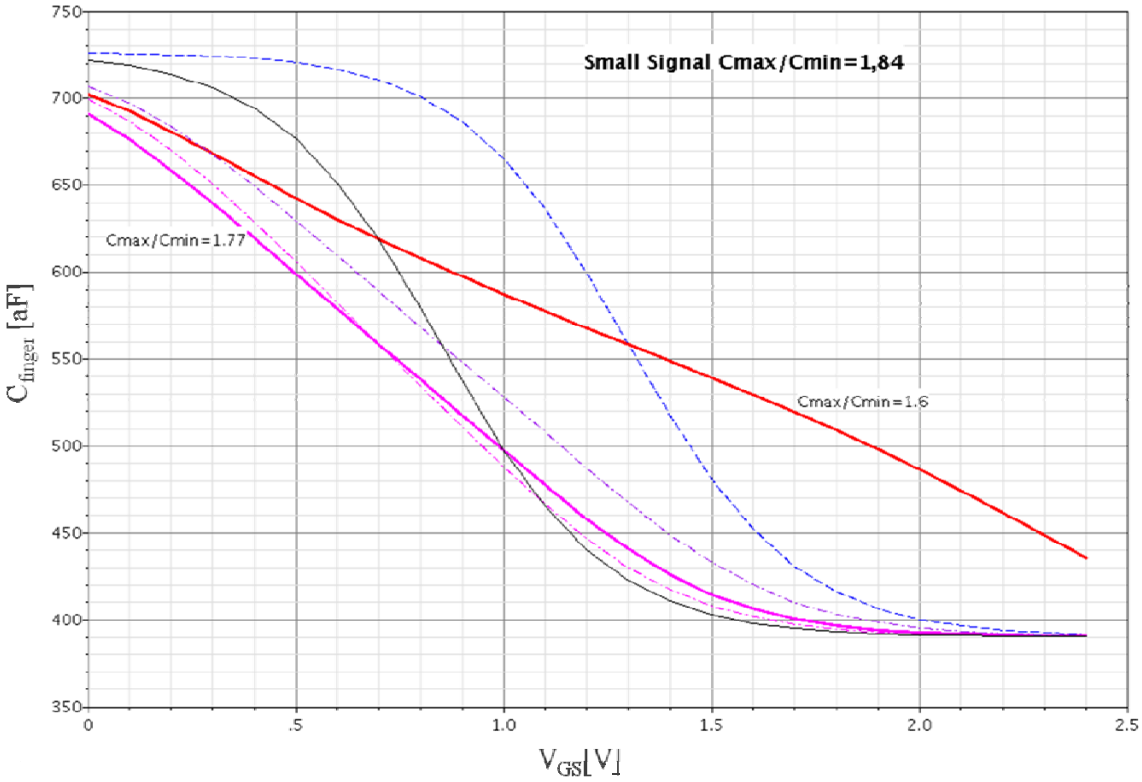

Figure 4.18: large signal effects

4.3.2 Hybrid TRWO-SWO loops coupling

As mentioned in section 4.2.2, the bias current of the TWO core is provided at the short-circuited ends of two λ/4 shunt transmission lines which are

connected to the main loop at two opposite loop corners, giving rise to and "hybrid" TWO and SWO structure.
These shunt standing wave transmission lines, by virtue of the injection locking mechanism, are exploited to perform loops coupling avoiding multiple oscillation modes generation.
Loops are physically connected at the circuited ends of the λ/4 shunt transmission lines through the insertion of the coupling resistances R_C, which is used only to provide the DC bias to each loop. (Fig. 4.19).
The lines connection gives rise to a sort of "virtual shorting" of each λ/4 t-line, such that each line sees the wave coming from the other connected λ/4 t-line towards the connection as its own incident wave after reflection at the virtual short.
If R_C is set to zero, each loop works independently one from each other. The higher the R_C value is the strongest the coupling effect becomes.

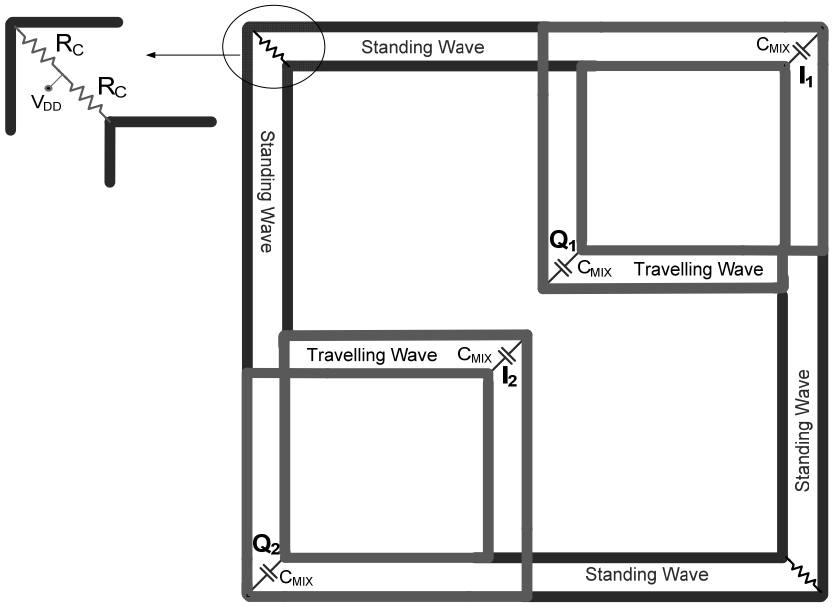

Figure 4.19: coupling mechanisms

To understand R_C effects on phase noise performances let's focus on the loops connection (Fig 4.20): if the phase shift ΔΦ between the two signal travelling from each loop towards R_C is exactly zero no signal current flows through the coupling resistance and its value doesn't impact the overall phase noise.

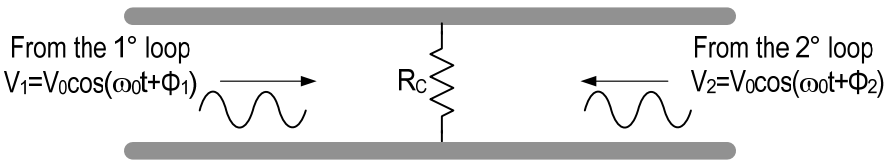

Figure 4.20: coupling mechanisms

In a real implementation, ΔΦ is higher than zero due to loading mismatches between the loops which are placed far from each other on the chip area. Once

this mismatch exists the consequent ΔΦ depends on the R_C value, as shown in Fig. 4.21.

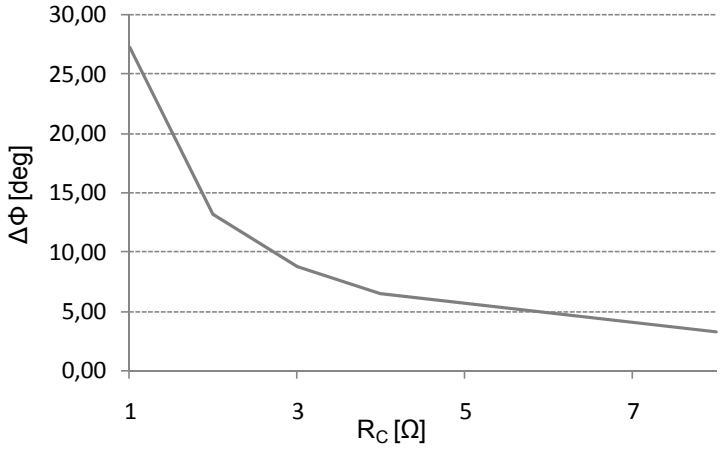

Figure 4.21: ΔΦ vs coupling resistance value

Assuming a 5% loading mismatch between loops, which corresponds to a frequency shift $\Delta f/f_0$ of about 1%, they begin to look each other for $R_C \geq$ 500mΩ. Fig. 4.22 shows that the overall system phase noise remain relatively low as the R_C value increase.
The dc power dissipation instead strongly increases with R_C. Thus, in order to maximize the system FOM, it is convenient to choose the lowest R_C value that ensures locking, with a phase shift sufficiently low (< 2°).

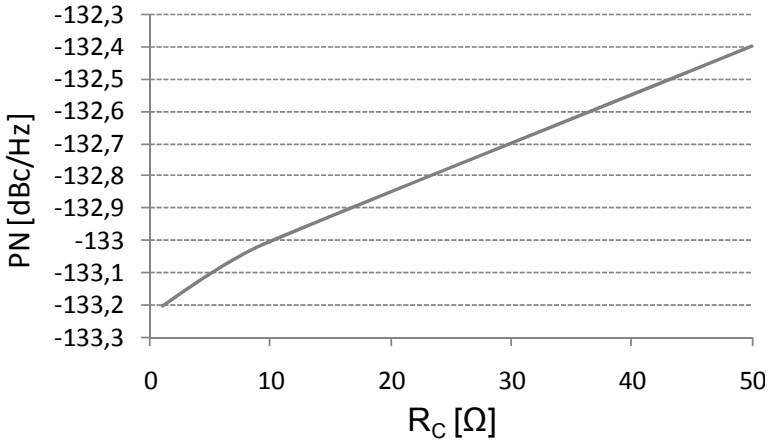

Figure 4.22: PN vs R_C

Figure 4.23 clearly shows the $10\cdot\log(N)$ improvement in phase noise due to the coupling mechanism. The overall figure of merit (FOM), as expected, remains nearly constant as the number of coupled loops N is increased. The simulated phase noise (at 10MHz from the carrier) at the maximum oscillation frequency for a single loop, two coupled loops and 4 coupled loops are respectively -126.6, -129.6 and -132.4dBc/Hz.

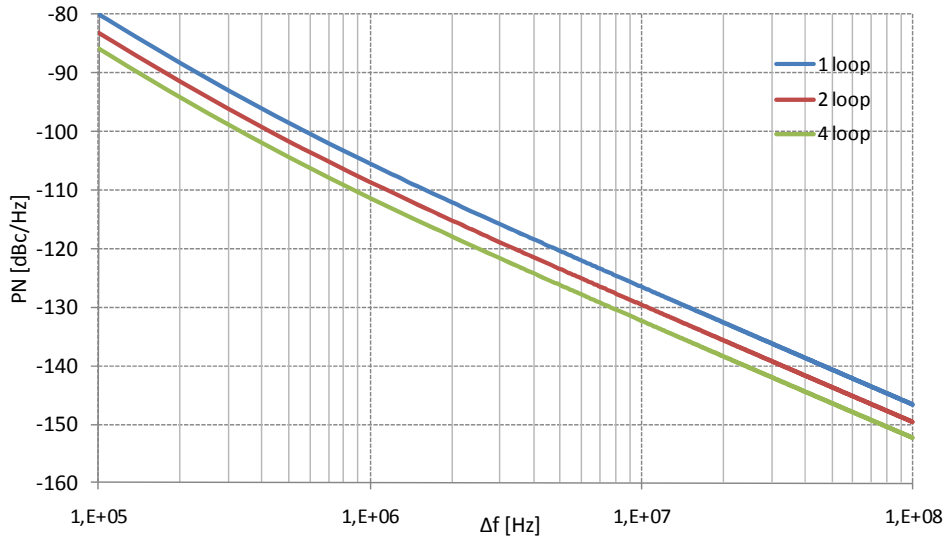

Figure 4.23: Phase noise improvement

As shown in Fig. 4.24, the obtained figure of merit compares favorably with the current state of the art, including standing wave VCOs, multi-phase rotary wave VCOs and classical LC-tank oscillators.
In Table 4.1 the performances of the designed generation and distribution system are compared with those of some LO generation and distribution systems published in recent years, designed for phased array systems based on the LO phase shifting approach.

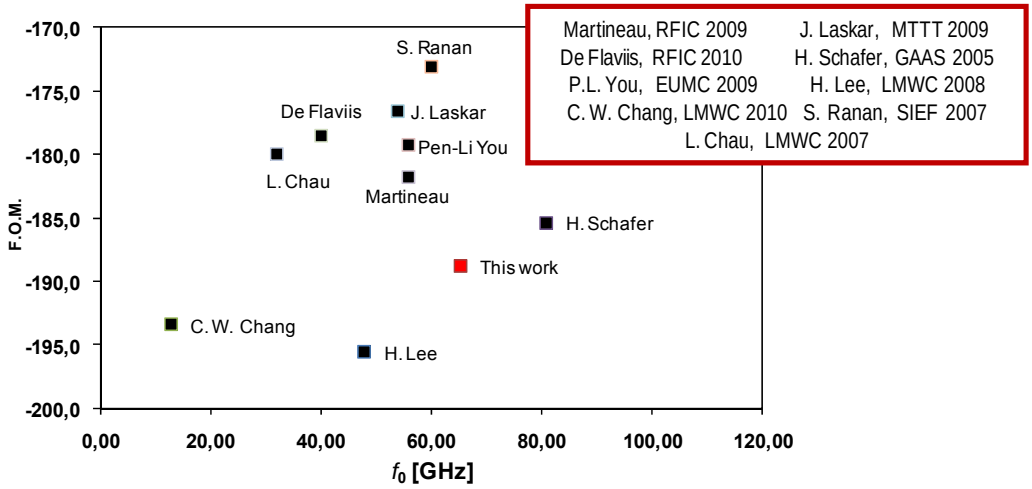

Figure 4.24: VCO FOM comparison

	Phase noise [dBc/Hz] @ 10MHz	P_{DISS} LO Generation	P_{DISS} LO Distribution	F.O.M. [dBc/Hz]	f_{osc} [GHz]
A. Hajimiri, JSSC 2006	-115	65,5	130	-166,41	52
Y. Rolain, JSSC 2008	-107	22,7	43,6	-162,76	50
This work	-130,6	68,2		-188,57	65,37

Table 4.1: LO generation and distribution systems FOM comparison

4.3.3 Amplitude control and buffer design

Simulations reveal a strong variations in the oscillation amplitude at the two extreme oscillation frequencies: the peak-to-peak differential oscillation amplitude is nearly 1.6V at 57.5GHz and about 2.4V at 64.5GHz. This is mainly due to the fact that the varactor quality factor changes with the control voltage V_C at the source/drain terminal.
This amplitude variation must be removed somehow adjusting amplitude as the oscillation frequency chances.
An amplitude control is of primary importance because variations in the amplitude of the LO signal at the passive mixer LO port translate into strong variations in the input mixer impedance causing a strong worsening of the input matching and a consequent performance reduction for the overall system.

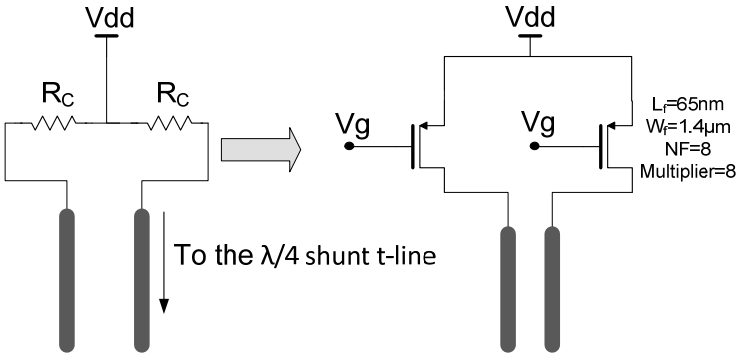

Figure 4.25: amplitude control

In fig. 4.25 the adopted solution for performing amplitude control is reported: the coupling resistances R_C are replaced by PMOS current generators.
PMOS devices are sized both in order to give R_C equivalent values sufficiently high to obtain phase shifts between adjacent loops lower than 2 degree and such that, for V_g values ranging from 0 to 0.6V, all the desired oscillation amplitudes range is covered (see Fig. 4.26).

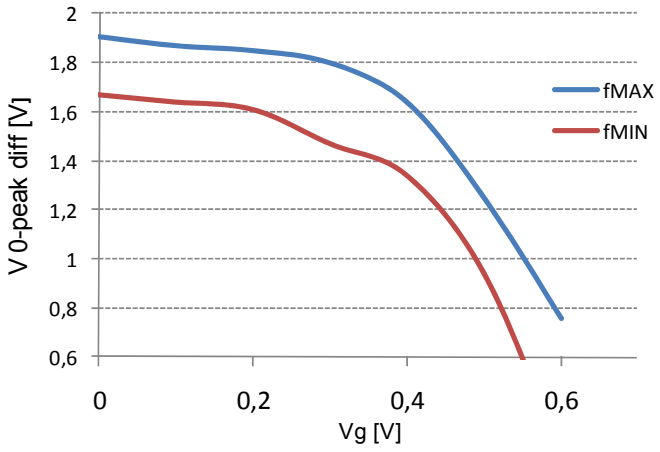

Figure 4.26: amplitude control

Vg [V]	f_{osc} [GHz]	PN @ 10MHz [dBc/Hz]	F.O.M. [dBc/Hz]
0,6	65,67	-124,30	-188,50
0,5	65,37	-127,60	-188,58
0,4	64,93	-128,60	-187,84
0,3	64,61	-129,4	-188,05
0,2	64,45	-129,7	-188,12
0,1	64,36	-129,9	-188,20
0	64,3	-130	-188,25

Table 4.2: f_{osc}, PN and F.O.M vs V_g @ f_{MAX}

Vg [V]	f_{osc} [GHz]	PN @ 10MHz [dBc/Hz]	F.O.M. [dBc/Hz]
0,6	57,22	-115,6	-178,95
0,5	57,17	-126,00	-185,75
0,4	57,07	-128,00	-185,74
0,3	57,03	-128,38	-185,62
0,2	57	-128,83	-185,52
0,1	57	-128,8	-185,39
0	56,99	-128,9	-185,38

Table 4.3: f_{osc}, PN and F.O.M vs V_g @ f_{MIN}

In Table 4.2 and 4.3 are reported the single loop oscillation frequency, phase noise and figure of merit as a function of V_g at both oscillation frequency extremes.

As just mentioned in section 4.3.1, a buffer is inserted between each LO differential output (I and Q) and the mixers LO ports.

The use of buffers is required because in a direct-conversion receiver, strong in-band interferers can leak from the RF to the LO port of the down-conversion mixers, thus injection-pulling the LO in the absence of the buffer. Each buffer consists of a common source stage loaded by a λ/4 shorted t-line. The common source stage, in a fully differential configuration, both provides some gain to the LO input signal and performs some isolation between its input and output ports. The load is in practice a standing wave oscillator which is injection locked to the input LO signal. In order to make the design more robust to the effect of layout parasitics and ensure locking, the same t-line structure used for the rotary-traveling wave oscillator loop is exploited (see Fig. 4.28). The standing-wave VCO is designed in order to maximize the "*potential*" tuning range of its self-oscillation: the VCO doesn't start oscillating of any input signal is injected on the common-source gates because it has not a sufficiently high intrinsic loop gain, but when the LO signal is on (with a proper amplitude) the standing-wave oscillator is locked and starts oscillating. The obtained locking range is of nearly 17GHz around 60, with a resulting upper and lower limit bonus of about 3GHz over the LO tuning range.

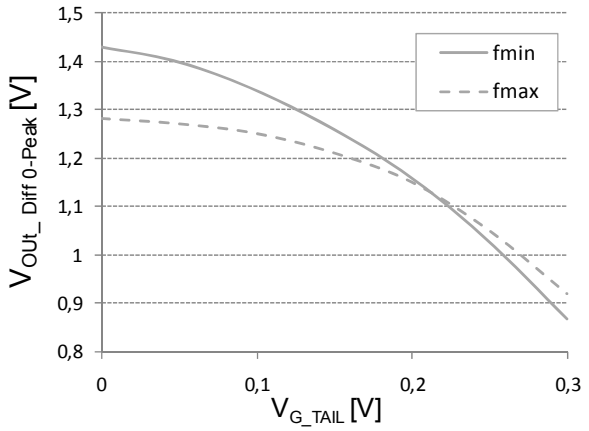

Figure 4.27: 2nd amplitude control

A further amplitude control is inserted at the buffer level: also in this case a PMOS current generator placed at the circuited end of the λ/4 transmission line is controlled, ideally controlling its gate voltage $V_{G\text{-}TAIL}$, to provide different DC current levels to the circuit.

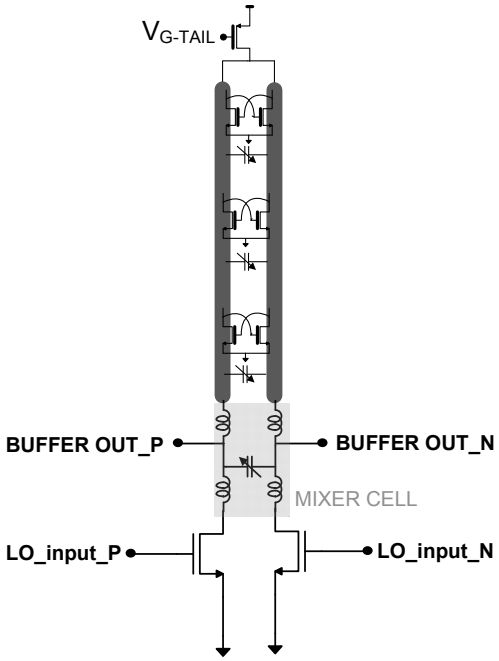

Figure 4.28: VCO Buffer

Conclusions

In this chapter a mm-wave travelling wave based LO generation and distribution system for a phased-array direct conversion receiver adopting the IF recombination approach has been proved. Such a system is formed by an array of N identical receivers using I/Q LO signals with well defined phase relationships, i.e. either all in phase or with fixed phase shift. In our

architecture, such a "synchronized" LO is created and directly brought to the mixer LO inputs using coupled rotary travelling wave VCOs.

Coupling between different RTWO loops is performed adopting an "hybrid" travelling-standing waves based structure: loops are physically connected at the circuited ends of λ/4 transmission lines which are connected to each loop at two opposite corners to provide the DC bias. By virtue of the injection locking mechanism, loops are forced to work at the same oscillation frequency.

This approach allows both to improve the phased-array receiver sensitivity by a factor 10Log*N* after to the recombination of *N* received signals and to reduce the LO phase noise by a factor 10Log*N* since *N* identical coupled oscillators are used. The 10log*N* improvement in the LO phase noise has been proved thought simulations: the simulated phase noise (at 10MHz from the carrier) at the maximum oscillation frequency for a single loop, two coupled loops and 4 coupled loops are respectively -126.6, -129.6 and -132.4dBc/Hz. The figure of merit of the overall LO distribution system remains constant as the number of coupled loops increases.

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Conclusions

Millimeter-wave wireless communications allow high data rates (up to 6Gbps), higher integration levels, strong levels of frequency reuse and enhanced safety due to the strong amount of atmosphere's absorption at these frequencies.

The main application field of 60GHz wireless transmissions is nowadays represented by high speed WLAN, but they are also exploited for intelligent transportation systems (ITS's), broadband distribution services (LMDS's) RLANs, radars and other applications.

In this thesis has been widely shown that a design approach based on different levels is of primary importance at 60GHz: device, building blocks, circuital topology and transceiver architecture have been studied in parallel.

Massive electromagnetic simulations and direct characterizations on dedicated test chips of active and passive devices has been carried out to try modeling devices as accurately as possible.

The chip area surrounding inductors and t-lines has been properly prefilled with dummies to reach the local density requirements and dummies effect has been verified through EM simulations. Some simplifications on complex layout structures, such as the balun and the resonated pad used in the LNA design, and on the actual metal prefillers pattern have proven necessary.

The BSIM 4.5 model of active devices has shown to be not sufficiently accurate at such high frequencies: for instance, it only includes the gate resistance due to poly, which in reality represents only a minimal part of the total mm-waves gate resistance. These inaccuracies are inacceptable especially with regard to the LNA design where a strong sensitivity to device modeling has been proven. This is why AC and noise custom models, also based on devices characterization, has been used for simulations.

A careful optimization of the layout has been carried out both for the LNA and VCOs implementations, particularly aimed at minimizing interconnections and realizing low impedance ground planes: from the standpoint of time required optimal layout has represented a large part of the projects.

Despite all these aspects make the design of a 60GHz front end, particularly in CMOS technology, time-consuming and complicated, the high speed performance that today's CMOS technologies, such as 65nm CMOS from TSMC, are able to offer, are opening the door to their use for 60GHz front-end mass production .

The issue of low passives quality factors has been addressed in the 53GHz lumped LC DCO, described in the second chapter, by segmenting the capacitor bank into three sections, implemented with different structures: tuning range and quality factor represent the primary drivers for the coarse

tuning bank, while small minimum capacitance step is the main requirement for the fine tuning bank.

In the voltage controlled 71-73GHz standing wave oscillator the problem of low capacitive quality factor has been instead addressed using, as a resonator, a short-circuited $\lambda/4$ shielded differential coplanar strip-line. Shielding, by preventing the electric field form penetrating into the substrate, allows to improve the resonator Q. Slow-wave lines make also it easier to satisfy local metal density rules. Particular emphasis in both cases has been given to the design of the resonator s and some guidelines have been drawn.

With regard to the DCO phase noise an analytical phase noise prediction, based on Hajimiri's theory, has been carried out. From this study a strategy for minimizing the phase noise in mm-wave VCOs has been derived and its effectiveness has been proved through circuital simulations.

The DCO showed a measured phase noise of -116.5dBc/Hz and consumes 2.34mW, resulting in a figure of merit of -187.2 dBc/Hz that was, at the time of publication, the best FoM ever reported for mm-wave VCOs. The DCO measured frequency resolution is of about 2MHz. The circuit, implemented in a digital 90nm CMOS process, shows very good efficiency and enables to employ fully digital frequency control in the frequency synthesizer.

The measured phase noise of the SWO at 72GHz is nearly -122.2dBc/Hz and its figure of merit is -176.5dBc/Hz.

The two oscillators have been designed with different active devices and varactors, hence a definitive comparison between the two approaches cannot be derived: this thesis shows however that both solutions remain viable alternatives at 60GHz.

Concerning the 60GHz low noise amplifier, many of the considerations given in the first two sections of chapter III, regarding the most suitable 60GHz LNA topologies and how to face the main design challenges, have been directly applied in the LNA design.

In our design, the inductive source degeneration topology has been chosen for each amplification stage because it represents an excellent solution to obtain contemporary good noise performances and a satisfactory input impedance matching.. Thanks to an analytical noise minimization study, widely discussed in the second section of the chapter, the noise minimization task and the impedance matching requirements become practically independent one from each other.

Instability, due to substrate coupling, has been prevented by adopting a differential topology, which, besides being less susceptible to parasitic feedback loops, is more robust to common-mode noise. Furthermore, since fully balanced circuits form virtual ground nodes, the physical ground connections has resulted much less problematic.

The input and output pad capacitances and the DC-decoupling capacitors have been considered as part of the matching networks so that no de-embedding of the pad capacitance has been necessary after measurements.

Each amplification stage has been sized, in terms of g_m and degeneration inductance L_S, taking into account noise minimization and power dissipation criteria for active devices, and bandwidth and losses considerations for matching networks.

Matching networks instead have been designed taking into account losses, bandwidth and physical implementation criteria. An "hybrid" approach has been adopted for all passive network: both spiral inductors and t-lines are massively used to exploit the advantages of both practical approaches.

Extensive electromagnetic simulations has been performed during design in order to try to accurately model parasitic and distributed effects of passives and interconnections, which hardly affect the LNA performances. Despite this accuracy attempt, simplifications performed in order to electromagnetically simulate the structures in an acceptable time and with a sufficiently accurate mesh, has caused a strong deviation of measurement results from the expected ones. Also further automatic metal density enforcement in the pad and matching networks area has probably worsen the experimental LNA performances.

It might have been appropriate to use, where available, solely t-lines, inductors, capacitance and MOS devices taken from libraries of measurement-based devices as done for some successful LNA reported implementations.

The LNA implementation showed that a common weakness of millimeter-wave IC designs, in particular if a scaled technology at an early stage of development, with only partial information of the process and of the device's "analog" performances is used, is the excessive sensitivity to the device models itself.

This issue, together with the limited achievable gain and the relatively high noise figure of 60GHz low noise amplifier, could be partly relaxed adopting a phased array based approach.

In the last chapter of this thesis a mm-wave travelling wave based LO generation and distribution system for a phased-array direct conversion receiver adopting the IF recombination approach has been proved. Such a system is formed by an array of N identical receivers using I/Q LO signals with well defined phase relationships, i.e. either all in phase or with fixed phase shift. In our architecture, such a "synchronized" LO must be created and directly brought to the mixer LO inputs: this is done in our proposed architecture, using coupled rotary travelling wave VCOs.

Coupling between different RTWO loops is performed adopting an "hybrid" travelling-standing waves based structure: loops are physically connected at the circuited ends of $\lambda/4$ transmission lines which are connected to each loop at two opposite corners to provide the DC bias. By virtue of the injection locking mechanism, loops are forced to work at the same oscillation frequency.

Such an LO generation and distribution system, not only shows good phase noise performances and good tuning capabilities for each single loop, but also allows to reduce, tanks to the coupling mechanism, the overall LO generation and distribution system phase noise by a factor $10\log(N)$, if N loops are coupled. The $10\log N$ improvement in the LO phase noise has been proved thought simulations: the simulated phase noise (at 10MHz from the carrier) at the maximum oscillation frequency for a single loop, two coupled loops and 4 coupled loops are respectively -126.6, -129.6 and -132.4dBc/Hz. The figure of merit of the overall LO distribution system is -188.6dBc/Hz and remains constant as the number of coupled loops increases.

Appendix 1

Three-step high-frequency De-embedding method

Designing RF circuits requires accurate models to describe the RF behavior of the devices used in the circuit.

For example, to model the RF behavior of MOS transistors, compact models, like BSIM4 or equivalent circuit-based models can be used. Their model parameters are extracted from S-parameter measurements on dedicated on-wafer test-structures. These RF test-structures not only consist of the actual device-under-test(DUT) for which the model parameters need to be extracted, e.g., a MOSFET, a bipolar transistor, or a passive component, but also of parasitic components that largely influence the electrical behavior of the DUT. The parasitic components mainly originate from the contact pad, which connects the RF measurement probe and the silicon wafer, and from the metal interconnections between these contact pads and the DUT. In order to model the RF behavior of the DUT accurately, the influence of the parasitic components must be subtracted from the measurements on the test- structure. The procedure to correct for the influence of the on-wafer parasitic components is called de-embedding.

After de-embedding, the correct S, Y, or Z-parameters of the DUT are obtained.

The de-embedding method used for our DUTs S-parameter extractions is based on a three-step open-short$_1$-short$_2$-through [1] technique.

The basic assumption in this de-embedding procedure is that the RF test-structure and the corresponding de-embedding structures can be represented schematically by the circuits shown in Fig. 1(a) and (b), respectively.

The electrical behavior of the DUT is influenced by the parasitic admittances G_1, G_2, and G_3, and the parasitic impedances Z_1, Z_2 and Z_3 .

The purpose of the de-embedding technique is to calculate the values of the unknown parasitic components. This is accomplished by measuring the S-parameters of the on-wafer de-embedding structures and converting them to Y–parameters.

For example, the parameters Y_{11} and Y_{12} of the open structure are given by:

$$Y_{11-OP} = G_1 + \frac{1}{\left(Z_1 + Z_2 + \frac{1}{G_3}\right)} \qquad (1)$$

$$Y_{12-OP} = -\frac{1}{\left(Z_1 + Z_2 + \frac{1}{G_3}\right)} \tag{2}$$

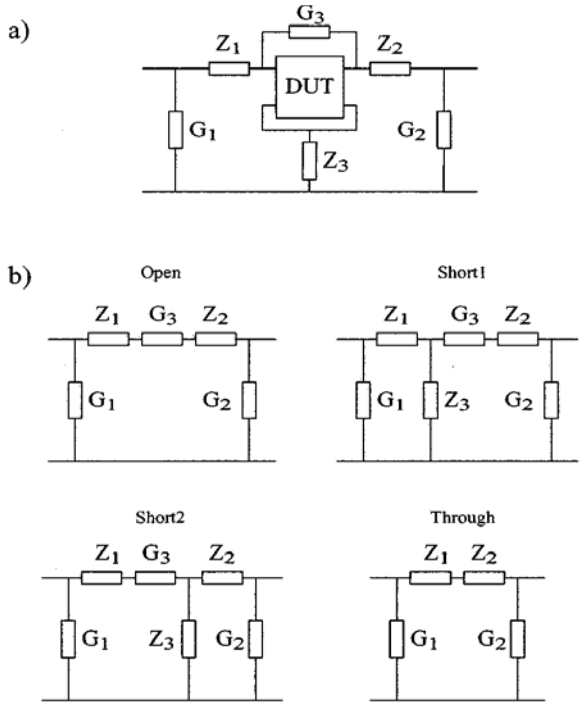

Figure 1: (a) Equivalent circuit of the RF test-structure (b) Equivalent circuits of the de-embedding structures

from which the value of G_1 can be calculated as $G_1 = Y_{11\_OP} + Y_{12\_OP}$.
In the same way all the other parameters can be calculated:

$$\begin{aligned} G_1 &= Y_{11\_OP} + Y_{12\_OP} \\ G_2 &= Y_{22\_OP} + Y_{12\_OP} \\ G_3 &= \left(-\frac{1}{Y_{12\_OP}} + \frac{1}{Y_{12\_THR}}\right)^{-1} \end{aligned} \tag{3}$$

$$\begin{aligned} Z_1 &= \frac{1}{2}\cdot\left(-\frac{1}{Y_{12\_THR}} + \frac{1}{Y_{11\_SH1} - G_1} - \frac{1}{Y_{22\_SH2} - G_2}\right) \\ Z_2 &= \frac{1}{2}\cdot\left(-\frac{1}{Y_{12\_THR}} + \frac{1}{Y_{11\_SH1} - G_1} - \frac{1}{Y_{22\_SH2} - G_2}\right) \\ Z_3 &= \frac{1}{2}\cdot\left(-\frac{1}{Y_{12\_THR}} + \frac{1}{Y_{11\_SH1} - G_1} - \frac{1}{Y_{22\_SH2} - G_2}\right) \end{aligned} \tag{4}$$

Now that the values for G_1 up to Z_3 are known, the measured S-parameters can be de-embedded. This is done in three consecutive steps:

$$
\begin{aligned}
Y_A &= Y_{meas} - \begin{pmatrix} G_1 & 0 \\ 0 & G_2 \end{pmatrix} \\
Y_B &= Y_A - \begin{pmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{pmatrix} \\
Y_{DUT} &= Y_B - \begin{pmatrix} G_3 & -G_3 \\ -G_3 & G_3 \end{pmatrix}
\end{aligned}
\tag{5}
$$

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Appendix 2

Gray-to-thermometer decoder

From the Gray code 5 bits ($G_{4\text{---}0}$) control word the thermometer code which controls the 31 elements of the fine-tuning bank has been obtained through a digital circuit that performs the following steps:

$$P_1 = G_0 + G_1$$

a) $$P_2 = G_1$$

$$P_3 = \overline{\overline{G_1} + G_0}$$

$$T_1 = P_1 + G_2$$

$$T_2 = P_2 + G_2$$

$$T_3 = P_3 + G_2$$

b) $$T_4 = G_2$$

$$T_5 = \overline{\overline{G_2} + P_3}$$

$$T_6 = \overline{\overline{G_2} + P_2}$$

$$T_7 = \overline{\overline{G_2} + P_1}$$

This iteration has a recursive nature.

Appendix 3

ΔC measurement technique

In order to measure the effective ΔC, we drive the control signal of the switches controlling the fine tuning capacitors bank and observe the sidebands induced in the output spectrum. This is in practice equivalent to a direct frequency modulation.
Obviously the modulating frequency must be higher than the PLL loop bandwidth.
A frequency modulated signal can be written as:

$$v_o(t) = A \cdot \cos \vartheta(t) = A \cdot \cos(\omega \cdot t + \phi) \tag{1}$$

Instantaneous frequency is:

$$f = f_C + \Delta f \cdot m(t) \tag{2}$$

where f_C is the carrier frequency and *m(t)* is the modulating index.
The phase is given by:

$$\vartheta(t) = 2\pi f_C t + 2\pi\Delta f \int_0^t m(\tau)\, d\tau \tag{3}$$

The FM modulated signal is:

$$v_o(t) = A\left[\cos(2\pi f_c t)\cos\left(2\pi\Delta f \int_0^t m(\tau)d\tau\right) - \sin(2\pi f_c t)\sin\left(2\pi\Delta f \int_0^t m(\tau)d\tau\right)\right]$$

Assuming the modulating signal to be a square wave:

$$m(t) = \begin{cases} 1/2 & 0 < t < T_m/2 \\ -1/2 & T_m/2 < t < T_m \end{cases} \tag{5}$$

We can approximate it with a Fourier series:

$$m(t) = \sum_k \frac{2}{k\pi}\cos(k\omega_m t) \tag{6}$$

Where *k* is odd only and a fixed phase shift was overlooked. Assuming $|m| < 1/4$, we can approximate the output signal with the following expression (NARROWBAND FM):

$$v_O(t) = A\left[\cos(\omega_c t) - \sum_k \frac{2\Delta f}{k\pi f_m}\sin(k\omega_m t)\sin(\omega_c t)\right] \quad (7)$$

Considering only the first harmonic:

$$v_O(t) = A\left[\cos(\omega_c t) - \frac{2\Delta f}{\pi f_m}\sin(\omega_m t)\sin(\omega_c t)\right] \quad (8)$$

Recalling that *sinx siny= ½ (cos (x-y) –cos (x+y))*

$$v_O(t) = A\left[\cos(\omega_c t) + \frac{\Delta f}{\pi f_m}\cos\left[(\omega_c + \omega_m)t\right] - \frac{\Delta f}{\pi f_m}\cos\left[(\omega_c - \omega_m)t\right]\right] \quad (9)$$

Hence each harmonic component of the modulating signal results in two sidebands.

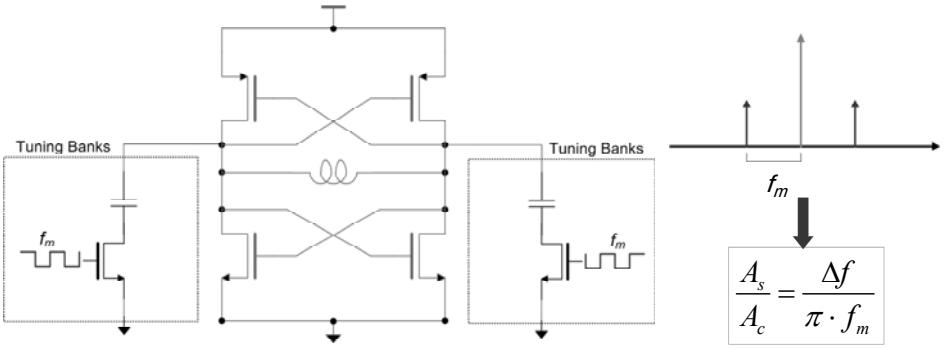

Figure 1: ΔC derivation

The ratio of the amplitude of the first sidebands to the carrier is:

$$\frac{\Delta f}{\pi f_m} \quad (10)$$

If a digitally-controlled oscillator has a frequency resolution Δf and is controlled with a clock frequency f_m, a spur with a relative amplitude as above will appear in the oscillator spectrum. For instance, with a frequency resolution of 1MHz and 100MHz clock frequency, a spur will appear at 100 MHz offset from the carrier, with a relative amplitude of -50dBc.