

Universita' degli studi di Pavia

Department of Electronic Engineering



Ph.D. Thesis in Microelectronics

XXVII Cycle

Low power-noise emission LTE class A/B transmitters

Supervisor:

Chiar.mo Prof. Rinaldo Castello

Ph.D. Dissertation of:

Elisa Maria Emilia Girani

Supervisor:

Chiar.mo Prof. Franco Maloberti

To Ivan because he has always been by my side,

Index

Introduction	9
Chapter 1 - Transceiver Overview	14
1.1 The Long Term Evolution Standard	16
1.2 TX performances	19
1.2.1 Output Power	19
1.2.2 Intermodulation	20
1.2.3 The Adjacent Channel Leakage Ratio (ACLR).....	22
1.2.4 Out-Of-Band noise emission	25
1.2.5 The Error Vector Magnitude (EVM)	28
Chapter 2: Transceiver design	32
2.1 Gilbert Mixer	35
2.2 Passive Voltage Mixer.....	37
2.3 Voltage mode approach vs Current mode approach	42
Chapter 3 :A Transmitter	45
with Current-Mode Approach	45
3.1 Current mode transmitter	46
3.2 Class A/B variable current mirror.....	47
3.3 Measurements Results	50
Chapter 4: A low power/noise emission LTE fully class A/B transmitter	55
4.1 Overall architecture.....	56
4.2 Starting Point Structure	56
4.3 CLASS B DAC introduction.....	60
4.3.1 DAC replicas.....	60
4.4 First OTA Structure	67
4.5 Output closed-loop stage.....	73
4.6 Pole-zero doublets compensation.....	74
4.7Up-conversion Stage.....	77
4.8 Out-of-band noise performances.....	78
4.9 Simulation Overall structure and reconfigurability.....	79
4.11 Simulation results	80
Chapter 5: Challenges and possible solutions to issues of the current mode approach	87
5.1 Programmable load impedance	88
5.2 Simulation results and comparison with the previous topology	91

5.1 Lo disoverlap : Problem description and possible solutions..... 93

5.2 Carrier Leakage..... 97

5.3 Calibration Algorithm 99

Conclusions 101

Appendix: Ahuja vs Miller compensation..... 103

 Where does the improved stability come from? 107

Bibliography..... 110

List of Figures

Figure 1.1: RF transceiver for mobile communications	15
Figure 1.2: IMD3 representation with two tones signal	23
Figure 1.3: Spectrum representation with four tones signal.....	23
Figure 1.4: output Spectrum.....	24
Figure 1.5 : output spectrum, calculated ACLR.....	25
Figure 1.6: Block diagram of an RF transmitter with the minimum out-of-band noise of the TX at the different nodes	26
Figure 1.7 : WCDMA TX noise floor requirements.....	28
Figure 1.8: Error vector, magnitude error and phase error	29
Figure 1.9 : EVM representation for a 4QAM signal.....	30
Figure 2.1 FSM and GMSK signal circuit generation	32
Figure 2.2: a) QPSK signal b) QPSK circuit generation.....	33
Figure 2.3: Constant and non constant envelope signal in time and frequency domain	34
Figure 2.4: a) Cartesian transmitter block diagram, b) polar transmitter block diagram	34
Figure 2.5: Active Gilbert mixer schematic	36
Figure 2.6 : Schematic of the transmitter that implements a passive mixer	37
Figure 2.7: Expansion coefficient vs bias voltage	39
Figure 2.8: Passive mixer, switched capacitor effect	41
Figure 3.1: conceptual block diagram of the TX proposed in [13-14].....	46
Figure 3.2 : schematic of the state of the art of TX proposed in [13-14].....	47
Figure 3.3 : Filtering class A/B conditioner	48
Figure 3.4 : Schematic of the TX proposed in [13].....	49
Figure 3.5: Current consumption vs output power	50
Figure 3.6: Diagram of ACLR (ACLR1 and ACLR2)vs output power with different input signals	51
Figure 3.7 Out-of band noise at different frequency offsets.....	51
Figure 4.1 : Block diagram of the new proposed structure	56

Figure 4.2 : Typical schematic of a transmitter with a high linear transconductor (R_{in}) with a driving current independent from I_{bias}	57
Figure 4.3: Baseband implemented with a high linear transconductor	58
Figure 4.4: Schematic of the transmitter with a high linear transconductor (R_{in}) with a driving current independent from I_{bias}	58
Figure 4.5: Schematic of the transmitter with a second order filtering stage	59
Figure 4.6: Diagram of the entire transmitter chain, from the digital DAC code to the analog signal sent to the antenna	60
Figure 4.7: Signal $x(t)$ sampled in the time domain and his spectrum.....	60
Fig 4.8: Classical class-A DAC architecture. a) Full scale current signal Input code $a_0, \dots, a_5 = 111111$; $I_{OUT} = +I$ b) Zero level current signal Input code $a_0, \dots, a_5 = 000111$; $I_{OUT} = 0$	62
Fig 4.9: Classical class-B DAC architecture. a) Input code $a_0, \dots, a_5 = 111111$; $I_{OUT} = +I$ b) Input code $a_0, \dots, a_5 = 000111$; $I_{OUT} = 0$	63
Fig 4.10: Classical class-B DAC n-only topology architecture with full scale current signal and zero level current signal configuration	64
Figure 4.11 : Schematic of the digital processing of the DAC thermometric code to change the class A signal into a class B signal	65
Figure 4.12 : Schematic of the digital processing of the DAC binary code to change the class A signal into a class B signal	66
Figure 4.13: Configuration of the first OTA structure with the PN input structure and the push-pull output structure	67
Figure 4.14: First OTA structure.....	68
Figure 4.15: Frequency response of the first OTA	69
Figure 4.16: Bias output reference for the first OTA	71
Figure 4.17: Schematic of the first OTA	72
Figure 4.18: Bias output reference for the first OTA	73
Figure 4.19: Schematic of the output baseband loop.....	74
Figure 4.20: Magnitude and phase response for the output OTA	75
Figure 4.21: Magnitude and phase response for the output OTA	75
Figure 4.22: Output OTA schematic.....	76
Figure 4.23: up-conversion stage	77

Figure 4.24: Base band stage with all the noise contributors.....	78
Figure 4.25: Complete structure proposed of the I path (or Q parth).....	79
Figure 4.26: Reconfigurability of the cut-off frequency of the filter	80
Figure 4.27: Graphic of the current consumption vs output power and comparison with the state-of-the-art	81
Figure 4.28: Graphic of the ACLR vs output power and comparison with the state-of-the-art.....	81
Figure 4.29: Baseband noise contributors at 30MHz offset from the carrier.....	82
Figure 4.30: Baseband noise contributors at 190MHz offset from the carrier.....	82
Figure 4.31: Baseband noise contributors at 400MHz offset from the carrier.....	83
Fig 5.1: Programmable load impedance created using two set of switches at the two sides of the primary coil	88
Fig 5.2: Schematic of an impedance transformer.....	89
Figure 5.3: Balun configuration when ϕ_2 is high and ϕ_1 is low, the impedance seen at the primary is about 30Ω	90
Figure 5.4: Balun configuration when ϕ_2 is low and ϕ_1 is high, the impedance seen at the primary is about 120Ω	90
Fig. 5.5 Current consumption: proposed solution vs the transmitter in [13]	92
Fig. 5.6 ACLR VS output power	92
Figure 5.7: LO disoverlap effect on the V_{drain} and V_{source} of the regulated cascode	94
Figure 5.8: Design of a possible circuit that can be implemented in order to regulate the LO overlap/disoverlap in order to achieve better linearity	95
Figure 5.9: Typical shape of the LO leakage at the output of the transitter.....	97
Fig. A.1(a): two stage op-amp with miller compensation.....	103
Fig. A.1(b): two stage op-amp with miller compensation, equivalent mode	104
Fig. A.2: two stage op-amp with ahuja compensation, equivalent mode	105
Fig. A.3: a) Ahuja configuration b) Miller configuration	107

List of Tables

Table I: 3G and 4G: the different standard specifications	17
Table II: Comparison with voltage mode TX	52
Table III: Current mode Tx comparison	53
Table IV : comparison between the new structure and the state-of-the-art	93

Introduction

Communication (from Latin *cum*= *with* and *munire* = *link/join*, meaning "to share") is the activity to transfer information. In a simple model, often referred as the transmission model or standard view of communication, information or content is sent from a transmitter to a receiver. However the presence of the receiver does not necessarily imply the assumption complete information: this, in fact, depends on both the effectiveness of the channel, above all, by the result of the interpretation (meaning reverse) of the message by the recipient. Social scientists Claude Shannon and Warren Weaver structured this model based on the following elements:

1. An information source, which produces a message.
2. A transmitter, which encodes the message into signals.
3. A channel, to which signals are adapted for transmission.
4. A receiver, which 'decodes' (reconstructs) the message from the signal.
5. A destination, where the message arrives.

The strengths of this model are simplicity, generality, and quantifiability. Telecommunication is communication at a distance by technological means, particularly through electrical signals or electromagnetic waves. The objective of an Radio Frequency (RF) transceiver is to transmit and receive information. We envision that the transmitter (TX) somehow processes the voice or data signal and applies the result to the antenna. Similarly, the receiver (RX) senses the signal picked up by the antenna and processes it so as to reconstruct the original voice or data information. While for the receiver the most important role is to reconstruct the signal and filter it from the overall noise and blockers in the most linear way, from the transmitter point of view the most important role is to transmit a very large signal (compared to the received one) in a precise frequency range and it must not interfere with other communication channels. Starting from that there is a technical problem: how accurately can the message be transmitted? In wireless communications the channel is often modeled by a random attenuation (known as fading) of the transmitted signal, followed by additive noise. The attenuation term is a simplification of the underlying physical processes and captures the change in signal power over the course of the transmission. The noise in the model captures external interference and/or electronic noise in the receiver.

One unwanted factor in telecommunication systems is the noise typically present in the communication channel and in electronic devices receiving and processing the downstream transmission. Such noise corrupts the useful signal in a manner often adding augmentation, therefore able to alter the correct flow of information between the transmitter and the receiver. Another disturbing factor could be the possible interference due to other signals leaking into the wanted band. Since in the real world is not possible to drop to zero the signal power at the edge of the bandwidth of the signal so part of the out-of-band emission can leak in other channels. The risk is corrupting other signal reception and recovery. In particular, the risk is higher for the receiver (RX) that is integrated in the same chip of the transmitter and is working in Frequency Division Duplex (FDD) mode: the TX out-of-band leakage is directly coupled to the RX path through the finite duplexer isolation, corrupting the received signal. Another issue to take into account is leakage that must be very low

since the attenuation is not infinite. To satisfy these requirements usually a Surface Acoustic Wave (SAW) filter is inserted between the on-chip transmitter and the external power amplifier, but, in order to save costs, the trend of the last years is to remove all the components that can not be integrated like the bulky SAW filter. Therefore the out-of-band emission must be very low to not compromise the performances of the receiver integrated on the same chip.

Besides all the other requirements, power consumption is always an issue since RF transmitters are devices that rely on battery. This aspect is very important especially for transmitters, where the power efficiency is very low. While advances in semiconductor technologies have driven continuous integration of features and services into portable devices, power consumption is now the major limiting factor on computational complexity and the ability to communicate over long distances. Therefore in the last years there is a pushing in increasing the efficiency of the transmitter circuits, especially of the power amplifier (PA). In addition to power consumption, it's now apparent that energy consumption is an important metric for transmitter circuit. Energy consumption more accurately predicts the battery life, especially when a portable device operates with a wide range of output powers. Energy consumption is a very important metric because it considers the probability of use of the different output power's ranges also because in this way it's possible to distribute the power consumption budget in a better way according to the statistic on the energy consumption over the range of output power. All these aspects described above are only general ones, but the process of to realize a RF transmitter involves also more important practical matters.

The design of an RF transmitter first requires to understand and define the standard for the RF applications analyzing the structure of the signal and the bandwidth. From that it's possible to define the value of the performance parameters that have to be set as a goal involving also a margin in order to be sure to not fail the goal. After these first observations the second step is to look at the different structure that it's possible to encounter for the RF transmitters and from all of that deciding what's the best circuit able to satisfy the specification always keeping in mind the power consumption aspect. The next step is to decide the class of operation for the transmitter. Usually this is decided in order to reduce the power consumption of the device according to the trade-off between linearity or noise. For this reason usually a class A/B is used since it's more power saving in comparison to a class A transmitter and more linear in comparison to a simple class B up-converter thanks to a smoother change of slope. Finally it's possible to start with the implementation of the new structure that should be able to achieve better performances in comparison to the state-of-the-art. The steps of realization involve the use of the cadence tool for the simulation and the use of Laker tool for the layout aspect.

In chapter one, I'll discuss about the Long Term Evolution (LTE) standard and the measurements parameters with focusing on out-of-band noise contributor.

In chapter two, I'll describe the state-of-the-art transmitters discussing about the two most important groups of RF transmitters and describing the benefits of a class A/B transmission.

In chapter three, I'll analyze the novel structure proposed as the new state-of-the-art looking at the implementation and looking at the simulated and the measured results.

In chapter four, I'll show the possible implementations to recover the possible problems of the current mode transmitters in order to enhance the linearity and make a trade-off between efficiency and linearity.

Chapter 1 - Transceiver Overview

In this chapter the transmitter parameters are analyzed starting from the communication standard description to the different quality factor specifications (adjacent channel leakage ratio, out-of-band noise, EVM). New communication standard are created in order to satisfy higher data rates needs. The parameter specifications are fundamental in order to understand the quality of the signal and of the device. In this way we are able to understand if the transmitter is able to support the different communication standards and which kind of condition of power consumption, area and cost are required to support them.

Nowadays high performance mobile phones manage different standards, Second Generation (2G), Third Generation (3G), Fourth Generation (4G), to meet the multiple needs of the users such as: fast data transfer, power saving and territory coverage. Switching from one standard to another is possible to meet all the requirements with only mobile handset. The number of frequencies and the coexistence of multiple standards put some challenges/limits to the platform performances and cost. Indeed, high performance wireless transmitters invariably use external SAW filters to attenuate out-of-band noise and leakage before they reach the Low-Noise Amplifier (LNA) input in order to not desensitize the receiver. For Time Division Duplexing (TDD) systems such as Global System for Mobile communications (GSM) related to 2G standard, isolation between transmitter and receiver is provided by the TX/RX switch and not by the SAW. On the other hand, in FDD systems like Wideband Code Division Multiple Access (W-CDMA), related to 3G standard, the external SAW performs both filtering and duplexing.

Both, FDD and TDD, have multiple operation bands [1, 2], from 400MHz up to 2.4GHz, which require almost one filter for each band. For new LTE releases, 10 and higher, up to 8 antennas for MIMO are contemplate [3-4] to meet the high data rate demand, so the number of passive components could explode.

Each block in Fig. 1.1 contains a great many functions, but we can readily make two observations:

- (1) The TX must drive the antenna with a high power level so that the transmitted signal is strong enough to reach far distances.
- (2) The RX may sense a small signal (e.g., when a cell phone is used in the basement of a building) and must first amplify the signal with low noise. We now architect our transceiver as shown in Fig.

1.1 where the signal to be transmitted is first applied to a “modulator” or “up-converter” so that its center frequency goes from zero to, f_c . The result drives the antenna through a Power Amplifier. On the receiver side, the signal is sensed by a LNA and subsequently by a “down-converter” or “demodulator” (also known as a “detector”).

The up-conversion and down-conversion paths are driven by an oscillator, which itself is controlled by a “frequency synthesizer.”

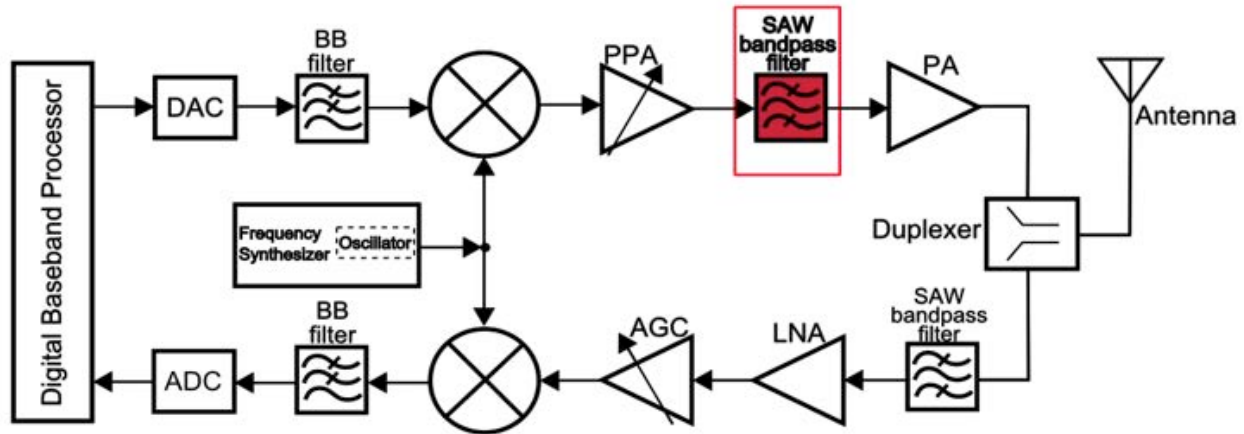


Figure 1.1: RF transceiver for mobile communications

In most parts of the world, use of transmitters is strictly controlled by law because of the potential for dangerous interference with other radio transmissions (for example to emergency communications). Transmitters must be licensed by governments, under a variety of license classes depending on use: (broadcast, marine radio, Amateur etc.), and are restricted to certain frequencies and power levels. In some classes each transmitter is given a unique call sign consisting of a string of letters and numbers which must be used as an identifier in transmissions. The operator of the transmitter usually must hold a government license, such as a general radiotelephone operator license, which is obtained by passing a test demonstrating adequate technical and legal knowledge of safe radio operation.

The presence of different signals, also working on the same frequency band, makes difficult the work of the receiver that has to recognize the wanted signal among the other ones and among their out-of-band emissions and the overall noise and interferes. However the most critical situation of coexistence is always the one of a receiver and a transmitter that are working in a FDD operation on the same mobile device. In fact if we look to a typical mask of interferers for mobile communications FDD standards when designing a front-end, we can see that one of the most critical interferer is given from the transmitter itself. As the cellular standards evolve from 2G to 2.5G, 3G, and 4G for higher data rate, the modulation schemes also evolve from constant envelope modulation to non-constant envelope modulation, with larger bandwidth as well as the increased Peak-to-Average Ratio (PAR). In a non-constant envelope modulation scheme a Cartesian transmitter followed by a linear PA is usually adopted, because of clean spectrum and low system complexity. In practice the noise contributed by the PA is negligible.

However, this architecture suffers from the noise generated by the modulator, this is a drawback since there is the aim to eliminate the SAW filter between the transmitter and the PA. In fact the SAW filter is a bulky external and expensive element into the cell phone board. Moreover a SAW filter is needed almost for every working band since, in order to be effective, they have to be narrowband. Therefore the elimination of the SAW filter is a very important issue since a lot of them has to be implemented on the board and their contribution to the overall chip cost is not negligible. From those assumptions, one of the key challenges in 2.5G/3G/4G transmitter design is to achieve the lowest TX out-of-band noise floor without sacrificing power consumption. This issue is very important since the isolation is not infinite and leakage from the transmitter can propagate into the RX-path. Moreover the transmitter chain must be linear enough to deliver a 64QAM OFDM signal to the antenna with acceptable distortion.

1.1 The Long Term Evolution Standard

In 1909 Guglielmo Marconi received the Nobel prize. Marconi's success was the practical and commercial realization of wireless telegraphy – the art of sending messages without wires – thus exploiting for the first time the amazing capability for wireless communication built into our universe. While others worked on wireless telephony – the transmission of audio signals for voice communication – Marconi interestingly saw no need for this. He believed that the transmission of short text messages was entirely sufficient for keeping in touch.

Nearly 100 years after Marconi received his Nobel prize, the involvement of thousands of engineers around the world in major standardization initiatives such as the 3rd Generation Partnership Project (3GPP) is evidence that the same unceasing toil of research workers and engineers continues apace.

While the first mobile communications standards focused primarily on voice communication, the emphasis now has returned to the provision of systems optimized for data. This trend began with the 3rd Generation WCDMA system designed in the 3GPP, and is now reaching fulfillment in its successor, the Long-Term Evolution. LTE [2] – [5] was the first cellular communication system optimized from the outset to support packet-switched data services, within which packetized voice communications are just one part. Thus LTE can truly be said to be the heir to Marconi's heritage – the system, unknown indeed to the luminaries of his day, to which his developments have led.

LTE commonly marketed as 4G LTE, is a standard for wireless communication of high-speed data for mobile phones and data terminals. It is based on the GSM/ Enhanced Data rates for GSM Evolution (EDGE) and Universal Mobile Telecommunications System (UMTS)/High Speed Packet Access (HSPA) network technologies, increasing the capacity and speed using a different radio interface together with core network improvements.

LTE is the natural upgrade path for carriers with both GSM/UMTS networks and CDMA2000 networks. The different LTE frequencies and bands used in different countries will mean that only

multi-band phones will be able to use LTE in all countries where it is supported.

Although marketed as a 4G wireless service, LTE (as specified in the 3GPP Release 8 and 9 document series) does not satisfy the technical requirements the 3GPP consortium has adopted for its new standard generation, and which were originally set forth by the International Telecommunication Union Radiocommunication (ITU-R) organization in its International Mobile Telecommunication

Table 1: 3G and 4G: the different standard specifications

Generation	3G	4G
Technology	UMTS,HSDPA, HSUPA	LTE
Uplink (theoretical)	5.7Mbps	50Mbps
Downlink(theoretical)	14Mbps	100Mbps
Max Bandwidth	5MHz	20MHz

(IMT)-Advanced specification. However, due to marketing pressures and the significant advancements that High Speed Packet Access (HSPA+) and LTE bring to the original 3G technologies, ITU later decided that LTE together with the aforementioned technologies can be called 4G technologies. A comparison between the 3G and 4G performances are summarized in Table I. The LTE Advanced standard formally satisfies the ITU-R requirements to be considered IMT-Advanced. To differentiate LTE Advanced and Worldwide Interoperability for Microwave Access (WiMAX)-Advanced from current 4G technologies, ITU has defined them as "True 4G".

The Long Term Evolution of UMTS is one of the latest steps in an advancing series of mobile telecommunications systems. The use of cells enabled the capacity of a mobile communications network to be increased substantially, by dividing the coverage area up into small cells each with its own base station operating on a different frequency.

The uppermost evolution track is that developed in the 3rd Generation Partnership Project (3GPP), which is currently the dominant standards development group for mobile radio systems and is described in more detail below.

During the '90s, GSM was studied to carry real time services, with data services only possible over a circuit switched modem connection with very low data rates. The first step towards an IP based packet switched solution was made with the evolution from GSM to GPRS using the same air interface and access method, TDMA (Time Division Multiple Access).

Within the 3GPP evolution track, three multiple access technologies are evident: the 'Second Generation' GSM/GPRS/EDGE family was based on Time- and Frequency- Division Multiple Access (TDMA/FDMA); the 'Third Generation' UMTS family marked the entry of Code Division Multiple Access (CDMA) into the 3GPP evolution track, becoming known as Wideband CDMA (owing to its 5 MHz carrier bandwidth) or simply WCDMA in order to reach high data rates and data

volume; finally LTE has adopted Orthogonal Frequency-Division Multiplexing (OFDM), which is the access technology dominating the latest evolutions of all mobile radio standards.

In continuing the technology progression from the GSM and UMTS technology families within 3GPP, the LTE system can be seen as completing the trend of expansion of service provision beyond voice calls towards a multiservice air interface. This was already a key aim of UMTS and GPRS/EDGE, but LTE was designed from the start with the goal of evolving the radio access technology under the assumption that all services would be packet-switched including voice, rather than following the circuit-switched model of earlier systems.

LTE requires an OFDM method which is a multicarrier technology subdividing the available bandwidth into a multitude of mutual orthogonal narrowband subcarriers.

The new Evolved Packet system (EPS) is purely IP based: real time services and datacom services are carried by IP protocol. The IP address is allocated when the mobile is switched on and released when switched off. LTE is able to reach even higher data rates and data volumes compared to the previous standards. High order modulation (up to 64QAM), large bandwidth (up to 20MHz, starting from 1.4MHz) and Multiple Input Multiple Output (MIMO) transmission in downlink is part of the solution. The highest theoretical data-rate is 170Mbps in uplink and, with MIMO approach, the rate can reach 300Mbps in the downlink.

Discussion of the key requirements for the new LTE system led to the creation of a formal ‘Study Item’ in 3GPP with the specific aim of ‘evolving’ the 3GPP radio access technology to ensure competitiveness over a ten-year time-frame. Under the auspices of this Study Item, the requirements for LTE Release 8 were refined and crystallized, being finalized in June 2005.

They can be summarized as follows:

- reduced delays, in terms of both connection establishment and transmission latency;
- increased user data rates;
- increased cell-edge bit-rate, for uniformity of service provision;
- reduced cost per bit, implying improved spectral efficiency;
- greater flexibility of spectrum usage, in both new and pre-existing bands;
- simplified network architecture;
- seamless mobility, including between different radio-access technologies;
- reasonable power consumption for the mobile terminal.

It can also be noted that network operator requirements for next generation mobile systems were formulated by the Next Generation Mobile Networks (NGMN) alliance of network operators [5], which served as an additional reference for the development and assessment of the LTE design. Such operator-driven requirements have also guided the development of LTE-Advanced.

To address these objectives, the LTE system design covers both the radio interface and the radio network architecture.

The idea to use OFDM modulation is perfect in order to achieve very high spectral efficiency, but requires fast processors due to:

- High peak-to-average power ratio
- Poor power efficiency

- High requirements on linearity
- Worst noise condition (with a given peak worst SNR)

All these point would lead to an increasing of the battery consumption and to very expensive handsets. Therefore the design of the TX structure for the more recent standards is a key and very challenging aspect in order to reduce the cost of the device.

1.2 TX performances

1.2.1 Output Power

RF power measurements take many forms, depending on the RF transmitter design and application. The RF output may be a simple continuous wave (CW) signal, a pulse, an analog modulated signal, or a complex digitally modulated transmission, such as an IQ or orthogonal frequency division multiplexing (OFDM) waveform. Very important is the maximum output power which can be seen as a counterpart of the receiver sensitivity. Among the types of RF power measurements, the steady state RF power of a CW tone is perhaps the simplest. Peak power, such as the overshoot of an RF pulse or IQ waveform, is the maximum value over some period of time. The power measurement can be averaged across a time period, such as across a series of RF pulses, yielding the average power. RF power can be integrated over a frequency band, as is the case for many mobile communication signals. Digitally modulated signals tend to be noise-like in nature and often have specified average and peak power values.

Modulation formats generally exhibit trade-offs between bandwidth efficiency, power efficiency, and detectability. In today's mobile communications, all three parameters are important because they determine the capacity, the talk time, and the maximum range, respectively.

An instrument commonly used to measure RF power is a spectrum analyzer. With these more complex RF instruments, engineers can measure the individual spectral components across frequency. The absolute power measurement accuracy is not outstanding, typically ± 0.5 to ± 2.0 dB. However, the relative power accuracy (or amplitude linearity) is excellent. Therefore, calibrating at a given frequency with a known power level, from a signal generator, for example, results in corrected power measurements that are accurate across a dynamic range greater than 100dB.

High-performance RF instruments, including vector signal analyzer and vector network analyzers, can measure magnitude and phase, offering the potential for greater error correction and measurement accuracy.

A very important feature of CDMA signals is the crest factor [6], defined as $\epsilon = 10 \log(P_{\text{peak}}/P_{\text{average}})$, P_{peak} being the 99.9% limit of the instantaneous-power distribution. The mean power of the signal is P_{average} . Depending on the number of the code channel transmitted simultaneously on one carrier frequency the crest factor can range from 4.5dB (1 code channel) to 11dB (128 code channels, similar to band limited white noise). The crest factor is also a function of

the selected codes. Compared to sinusoidal signals (epsilon=3dB) CDMA signals require higher linearity to prevent compression or clipping of the signal.

With a perfect RF transmitter, the only signal transmitted would be the signal of interest. However, unwanted signals are a consequence of real-world transmitter design trade-offs. Cost, performance, and other requirements influence the final product. These unwanted signals fall within three broad categories: harmonic, intermodulation, and spurious (spurs).

Signals that are integer multiples of the main carrier signal are said to be harmonically related. Leading sources of these signals are amplifiers used in the transmitter. These signals may be low enough in amplitude so they aren't considered significant. Or, they may be far enough away in frequency that they can be reduced with filtering. Harmonics are easy to detect because their frequency is predictable. For example, the harmonic content of a signal at 1 GHz, can be found at 2 GHz, 3 GHz, and so on.

Spectrum or vector signal analyzers with their excellent linearity and relative power accuracy are good instruments to identify the frequency and relative power of unwanted signals. Power meters on the other hand are typically not used because they are broadband with limited dynamic range. In an RF transmitter, unwanted signals represent wasted RF power that's not going into the desired transmission. This results in a variety of consequences including lower efficiency, excessive heat, reduced battery life. The best plan of action is to perform proper analysis during the design phase to identify and mitigate unwanted signals from the transmitter.

1.2.2 Intermodulation

Intermodulation (IM) or intermodulation distortion (IMD) is the amplitude modulation of signals containing two or more different frequencies in a system with nonlinearities. The intermodulation between each frequency component will form additional signals at frequencies that are not just at harmonic frequencies (integer multiples) of either, but also at the sum and difference frequencies of the original frequencies and at multiples of those sum and difference frequencies.

The theoretical outcome of these non-linearity can be calculated by generating a Volterra series of the characteristic, while the usual approximation of those non-linearity is obtained by generating a Taylor series.

A one-tone input signal [7] ($V_{IN} = E \sin \omega_1 t$) produces harmonic distortion, a two-tone input signal produces harmonic distortion and intermodulation distortion.

The non-ideal characteristics of an amplifier can be described by using the Power Series Expansion:

$$V_{out} = K_0 + K_1 (V_{in}) + K_2 (V_{in})^2 + K_3 (V_{in})^3 \dots \quad (1)$$

$$V_{in} = E_1 \sin \omega_1 t + E_2 \sin \omega_2 t \quad (2)$$

Combining equations 1 and 2 results in the following identity:

$$V_{out} = K_0 + K_1 (E_1 \sin \omega_1 t + E_2 \sin \omega_2 t) + K_2 (E_1 \sin \omega_1 t + E_2 \sin \omega_2 t)^2 \quad (3)$$

$$+ K_3(E_1 \sin \omega_1 t + E_2 \sin \omega_2 t)^3 + \dots$$

The first term (K0) represents the DC offset of the amplifier, the second term is the fundamental signal. The subsequent terms represent the distortion of the amplifier. The second IMD can be found by analyzing the third term of Equation 3.

$$K_2(V_{in})^2 = K_2 (E_{12} \sin 2\omega_1 t + E_{22} \sin 2\omega_2 t + 2E_1 E_2 \sin 2\omega_1 t (\sin \omega_2 t)) \quad (4)$$

Remembering that $[\sin^2 x = (1 - \cos 2x)/2]$ and $[\sin(x)\sin(y) = (\cos(x - y) - \cos(x + y))/2]$ and substituting into

Equation 4 provides:

$$K_2(V_{in})^2 = K_2 \frac{(E_{12} + E_{22})}{2} - \left(\frac{K_2}{2}\right) (E_{12} \cos 2\omega_1 t + E_{22} \cos 2\omega_2 t) + 2K_2 E_1 E_2 (\cos(\omega_1 t - \omega_2 t) - \cos(\omega_1 t + \omega_2 t)) \quad (5)$$

The first and second terms in Equation 5 represent DC offset and second-order harmonics. The third term is the second-order IMD. This exercise can be repeated with the fourth term of Equation 3 to study third-order effects.

$$K_3(V_{in})^3 = K_3 (E_{13} \sin 3\omega_1 t + E_{23} \sin 3\omega_2 t + 3E_{12} E_2 \sin 2\omega_1 t (\sin \omega_2 t) + 3E_1 E_{22} \sin \omega_1 t (\sin 2\omega_2 t)) \quad (6)$$

Utilizing the identities, $\sin 3x = 1/4(3\sin x - \sin 3x)$ and $\sin^2 x \sin y = 1/2(\sin y - 1/2(\sin(2x + y) - \sin(2x - y)))$, Equation 6 reduces to:

$$K_3(V_{in})^3 = \left(\frac{3K_3}{4}\right) (E_{13} \sin \omega_1 t + E_{23} \sin \omega_2 t + 2E_{12} E_2 \sin \omega_2 t + 2E_{22} E_1 \sin \omega_1 t) + \quad (7a)$$

$$+ \left(\frac{K_3 E_{23}}{4}\right) (E_{13} \sin 3\omega_1 t + E_{23} \sin 3\omega_2 t) + \quad (7b)$$

$$+ \left(\frac{3K_3 E_{12} E_2}{2}\right) (\sin(2\omega_1 t - \omega_2 t) - 12 \sin(2\omega_1 t + \omega_2 t)) + \quad (7c)$$

$$+ \left(\frac{3K_3 E_{22} E_1}{2}\right) (\sin(2\omega_2 t - \omega_1 t) - 12 \sin(2\omega_2 t + \omega_1 t)) \quad (7d)$$

Term (a) from Equation 7 represents amplitude offset at the fundamental frequencies. Term (b) signifies the third-order harmonics. Term (c) and (d) represent third-order IMD. The result clearly indicates that IMD and crossmodulation only occur on a curved transfer characteristic with cubic terms like term (c) and (d) in Equation 7. In contrast a transfer characteristic with a linear and signals.

Therefore it's demonstrated that intermodulation is caused by non-linear behavior of the signal processing (physical equipment or even algorithms) being used. Intermodulation is rarely desirable in radio, as it creates unwanted spurious emissions, often in the form of sidebands. For radio transmissions this increases the occupied bandwidth, leading to adjacent channel interference, which can reduce audio clarity or increase spectrum usage. It should not be confused with harmonic

distortion (which has common musical applications), nor with intentional modulation (such as a frequency mixer in super heterodyne receivers) where signals to be modulated are presented to an intentional nonlinear element (multiplied) (see non-linear mixers such as mixer diodes and even single-transistor oscillator-mixer circuits).

Intermodulation products are signals generated by nonlinear interactions in the transmitter components. Mixers and amplifiers are an example of a circuit component with nonlinear behavior. The mixer outputs the sum and difference of the two input signal frequencies. In RF transmitters, the output is filtered to isolate the higher frequency sum in a process known as up-conversion. In this way, through one or more up-conversion stages, the low-frequency baseband information can be translated to the final RF frequency for transmission. Unfortunately, mixers also provide a host of other signals including combinations of the input signals and their harmonics, as well as leakage of the input signals to the output. The frequency and amplitude of the intermodulation products change with changes in the input signals. With careful analysis, intermodulation products can be predicted, making it possible to minimize their impact.

Spurs can occur at any frequency and power level from sources such as leakage and electromagnetic interference. The unpredictable nature of spurious signals makes them more challenging to detect and remove. Empirical and analytical methods along with good design practices are the best tools to minimize their impact.

1.2.3 The Adjacent Channel Leakage Ratio (ACLR)

The Adjacent Channel Leakage Ratio is the basic measure of the linearity of the transmitter.

The ACLR of any general purpose RF device, whether a mixer, amplifier, isolator, or other device, is frequently dominated by the 3rd-order intermodulation distortion (IM3) of the device. The relationship between the IM3 performance and the output intercept point (OIP3) parameter of the device can be derived. A formula for the prediction of the ACLR performance as a function of this IM3 performance parameter is derived in the following lines.

$$IMD3 = 2(OIP3 - PO) \quad (8)$$

A convenient way to look at the source of ACLR degradation in an RF device is to model the wideband carrier spectrum as a collection of individual CW subcarriers. Each of these subcarriers would carry a fraction of the total carrier power. The following figure illustrates such a model, Figure 2.1 shows the IMD3 for the two tones signal while Figure 2.2 shows the four tones signal case.

The continuous RF carrier is modeled in this case by four individual CW subcarriers, each of which has one-quarter of the power of the total broadband carrier. The subcarriers are distributed in equal intervals across the carrier bandwidth.

The IMD3 component from subcarriers 1 and 3 has an IMD3 distortion product at an equal frequency spacing from carrier 1. This generates the second IM product to the left of the carrier spectrum. Similarly, the IMD3 from subcarriers 1 and 4 produces a distortion product farther out from the carrier edge.

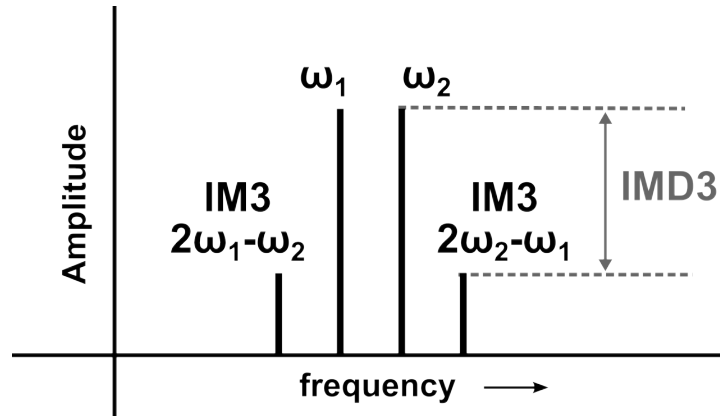


Figure 1.2: IMD3 representation with two tones signal

It is useful to note that there also are other IMD products present here. Subcarriers 2 and 4 produce IM3 products, which fall directly on top of the IMD product from subcarriers 1 and 2. This summation effect forces the IMD products closer to the center of the adjacent channel range to be higher in magnitude than those IMD products farther away from the edge of the RF carrier, producing the characteristic "shoulders" that appear in an ACLR distortion spectrum.

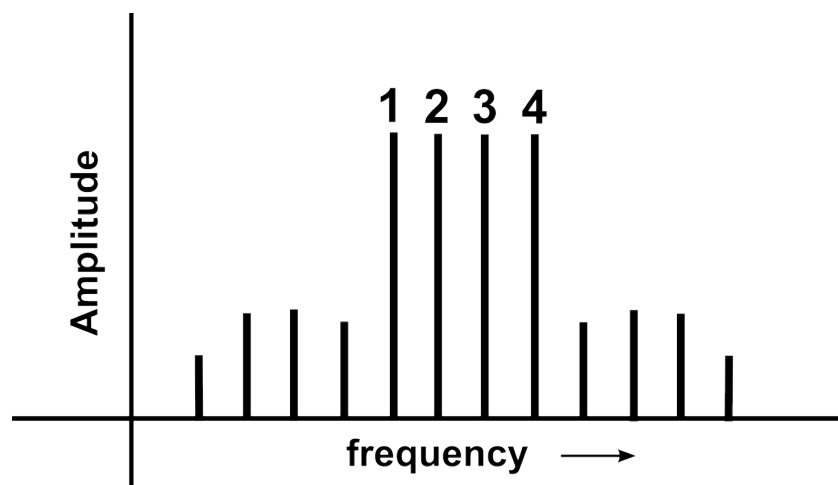


Figure 1.3: Spectrum representation with four tones signal

The ACLR for a carrier adjacent to the last carrier in the contiguous collection of wideband carriers rides on the high shoulders of the IMD3-induced distortion response. This causes the ACLR for a multicarrier case to be considerably worse than that for a single-carrier system. Again, this effect can be quantified and used to accurately predict the ACLR performance of single or multiple wideband carriers. This basic approach is used to predict the ACLR performance RF devices from the OIP3 specification alone. ACLR (also ACPR, Adjacent Channel Power Ratio) is a very important specification in WCDMA systems for transmitter, especially the power amplifier.

It is defined as the ratio of the power in the adjacent channel to the power in the user (wanted) channel:

$$ACLR = \frac{\int_{f_0-\Delta BW/2}^{f_0+\Delta BW/2} PSD(f)df}{\int_{f_0-3\Delta BW/2}^{f_0-3\Delta BW/2} PSD(f)df} \quad (9)$$

The equation showed in (9) is referred to the ACLR1 since it's the ratio between the power of the signal over the power of the adjacent channel, usually also the ACLR2 is measured as the ratio between the wanted signal over the power of the alternate adjacent channel. Figure 1.4 and 1.5 show the spectrum, the channels and how the ACLR was extrapolated from the simulations.

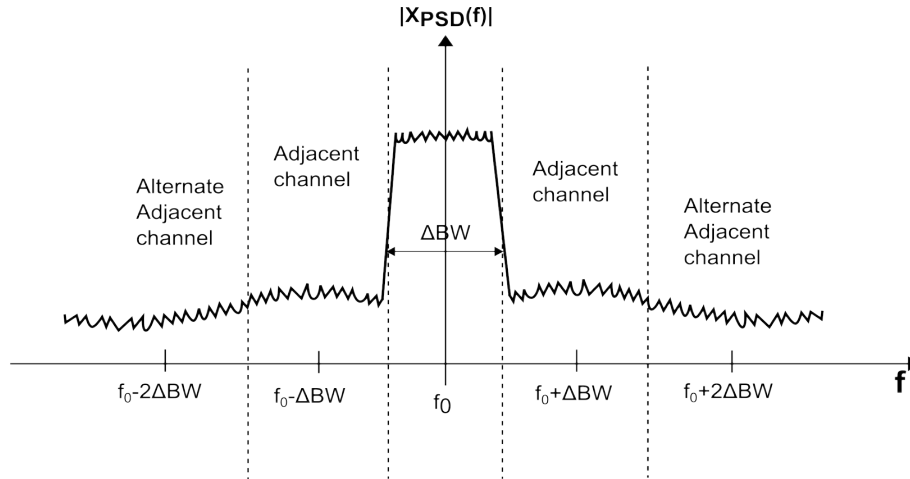


Figure 1.4: output Spectrum

This effect occurs with broadband signals and is caused by the odd terms of the transfer function of the building block.

The cubic term in the nonlinearity causes a broadening of the spectrum to approximately three times of the original bandwidth, thus leaking into the lower and upper adjacent channel.

Another metric to take into account is the ACLR2 that is relative to the ratio between the power of the signal channel over the power of the alternate adjacent channel.

For what concerns Cadence simulation, due to the difficulty in simulate the circuit with a modulated signal, the ACLR simulation are made with a multi-tone test with the same PAR and RMS of the communication standard taken as a reference. A simplified ACLR can be simulated with a multitone (4 tones) test calculating the ratio between the signal tones and the out-of-band intermodulations tones:

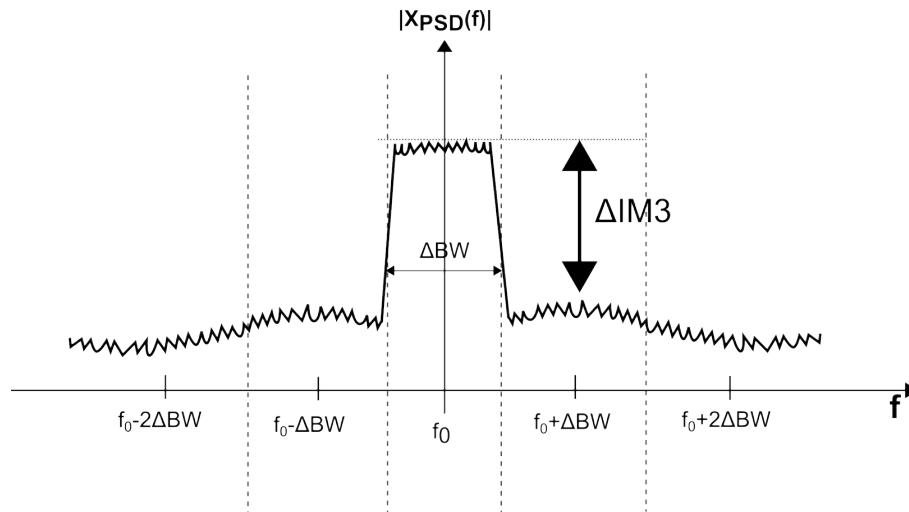


Figure 1.5 : output spectrum, calculated ACLR

To achieve high linearity:

1. assign most of gain to last PA stage
2. minimize the number of stages in the TX chain
3. current- mode approach

1.2.4 Out-Of-Band noise emission

Presently, there is widespread interest in pursuing a single-chip, handheld, wireless transceiver implemented in complementary, metal-oxide-semiconductor (CMOS) technology. A key component of such a system would be the power amplifier (PA), and several workers have recently described implementations of CMOS PAs. However, most of these designs, such as those described in [8], were intended for constant-envelope modulation schemes, and are hence intrinsically very nonlinear. For nonconstant-envelope modulation schemes, nonlinearity can cause severe regrowth in the spectral sidebands and an increase in the transmitted error-vector magnitude. In such cases, stringent requirements are placed on amplifier linearity. At the same time, to prolong battery life, the power amplifier must also operate at reasonable levels of efficiency.

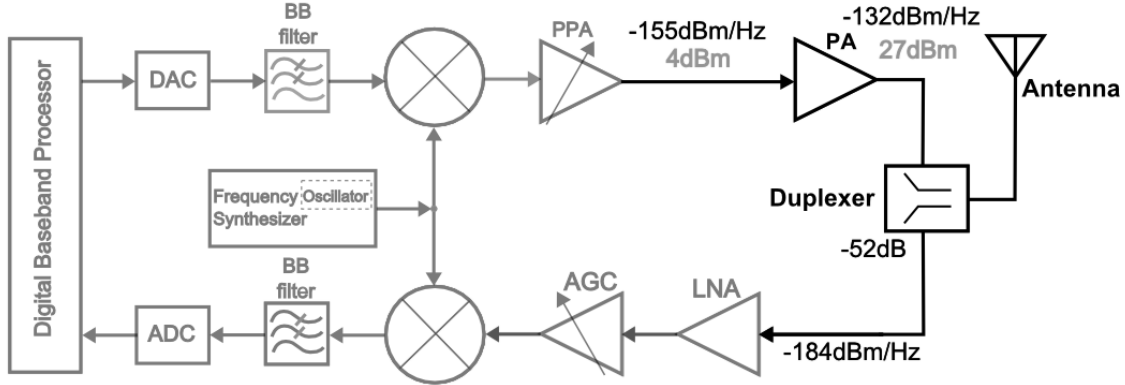


Figure 1.6: Block diagram of an RF transmitter with the minimum out-of-band noise of the TX at the different nodes

To meet the simultaneous requirements of high linearity and reasonable efficiency, power amplifiers in nonconstant-envelope systems are often operated in a class-AB mode; the linearity can be superior to that in class-B or higher operation and the efficiency is superior to that in class-A operation. Of particular importance is the nonlinearity of the class-AB amplifier; while more linear than a class-B or higher amplifier, the intrinsic linearity obtained in class-AB operation is often still insufficient to meet required specifications. While many external linearization techniques are known [9], they are complex and inconvenient for handset applications, and it is thus important that the intrinsic amplifier linearity be made as high as possible.

The goal of a Transmitter is to send a signal taking into account two aspects:

- Concentrate the power into the signal band (band efficiency)
- Manage the coexistence of a receiver and transmitter integrated in the same chip
- Power efficiency

While in receivers the in band noise is an issue, for the transmitters it's important to look at the out-of-band noise. In order to not degrade the performance of the receiver integrated in the same chip.

In WCDMA and LTE applications the transmitter noise floor requirement is determined by three factors: allowed RX sensitivity loss caused by the TX to RX leakage at the RX frequency, 3GPP emissions mask, and the co-existence requirement. Figure 1.6 shows the transceiver block diagram with the different value of out-of-band noise, output power and duplexer isolation typical for these applications.

The noise floor of the receiver, supposing matched input impedance, is given by:

$$10\text{Log}\left(\frac{kTR_a}{50\Omega \cdot 1mW}\right) = -174\text{dBm/Hz} \quad (10)$$

Where k is the Boltzmann constant, T the room temperature in kelvin and R_a the antenna resistance typically equal to 50Ω .

In order to not desensitize the RX path, the TX noise in WCDMA has to be low at the RX band in comparison to the noise floor, due to limited TX-to-RX isolation from the duplexer. The RX sensitivity desensitization caused by the TX noise at the RX frequency can be shown as:

$$Desensitization_{dB} = 10\log_{10}\left(1 + 10^{\frac{N_{tx}+N_{rx}}{10}}\right) \quad (11)$$

Where N_{tx} denotes the received TX noise before the LNA, N_{rx} is the RX input referred noise before the LNA. N_{rx} can be further calculated by:

$$N_{rx} = -174 + IL_{switch} + IL_{duplexer_rx} + NF \quad (12)$$

Where IL_{switch} is the insertion loss of the antenna switch, $IL_{duplexer_RX}$ is the RX insertion loss of the duplexer, and NF is the receiver noise figure (without accounting the loss of the switch and the duplexer). The required TX noise floor with respect to the maximum output power can be derived by

$$N_{tx_dBc/Hz} = N_{PA} - P_{PA} = (N_{TX} + ISOL_{TX2RX}) - (P_{ANT} + IL_{switch} + IL_{duplexer_{TX}}) \quad (13)$$

Where N_{PA} is the total TX noise after the PA, P_{PA} represents the maximum output power after the PA, $ISOL_{TX2RX}$ is the duplexer TX-to-RX isolation at the RX frequency, is the maximum output power at the antenna (24dBm in WCDMA), and $IL_{duplexer_TX}$ is the duplexer TX insertion loss. Given typical 0.8 dB switch insertion loss, 1.5 dB duplexer RX insertion loss, 1.1dB duplexer TX insertion loss, and 47dB duplexer TX to RX isolation at the RX frequency, the calculated TX noise floor is -158dBc/Hz, targeting only 0.5dB RX sensitivity desensitization with respect to a 2.5dB RX noise figure in commercial product.

Another aspect to take into account is that when transmitting at 1920MHz in WCDMA band 1, the nearest frequency offset to the DCS band (1805MHz to 1880 MHz) is 40MHz. At this offset typical WCDMA duplexers only offers few dB attenuation. To comply with 3GPP emissions mask, which restricts the emission power to be lower than -71dBm/100kHz, the TX noise at 40MHz offset is expected be lower than -148dBc/Hz (with 3 dB margin).

Moreover the coexistence of other applications such as GPS, WLAN, FM, and TV-on-mobile with WCDMA applications in the same mobile platform imposes stringent requirement on the TX far-out noise floor as well as the spectrum purity. As one use case that GPS has to co-exist with WCDMA, the WCDMA TX noise floor requirement at the GPS band can be derived by:

$$\begin{aligned} \frac{N_{tx_dBc}}{Hz} = N_{PA} - P_{PA} = \\ (N_{TX} - CF + IL_{switch} + ATT_{duplexer} + ATT_{PA}) \\ - (P_{ANT} + IL_{switch} + IL_{duplexer_{TX}}) \end{aligned} \quad (14)$$

Where N_{TX} represent the received WCDMA TX noise at the GPS antenna, CF is the coupling factor between the WCDMA antenna and the GPS antenna, $ATT_{duplexer}$ is the duplexer attenuation at the GPS band, and ATT_{PA} is the GPS band attenuation offered by the PA matching network. Targeting 0.25 dB sensitivity loss in a GPS receiver with totally 3 dB noise figure (including 1 dB insertion loss from the GPS SAW filter), the calculated WCDMA TX noise floor at the GPS band is -158 dBc/Hz, given -12dBc coupling factor, 36dB $ATT_{duplexer}$, 3dB ATT_{PA} , 0.8 dB switch loss, and the same duplexer loss aforementioned. On account of the three factors defining the noise floor, the overall noise floor requirement for WCDMA band 1 is plotted in Fig. 1.7.

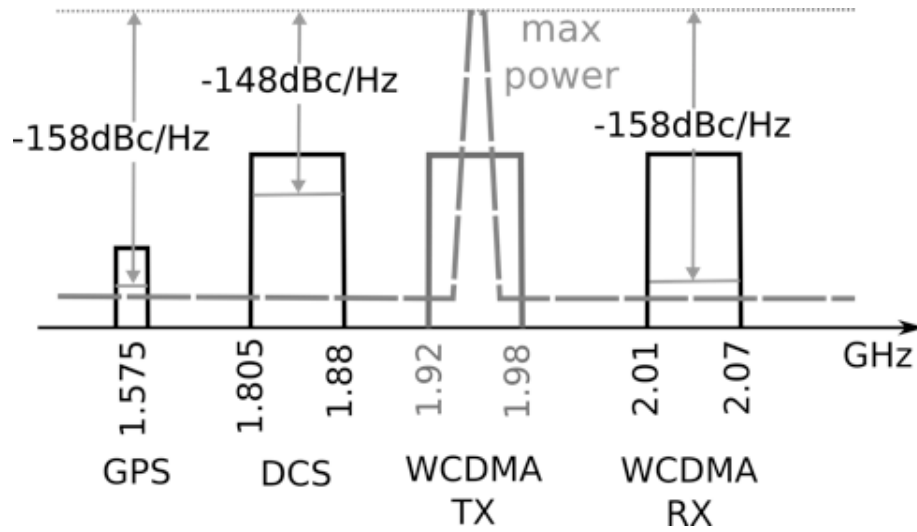


Figure 1.7 : WCDMA TX noise floor requirements

In addition to the noise floor requirement, the error vector magnitude (EVM) is also becoming a tough requirement for 3G/4G applications. In WCDMA, the EVM is defined to be below 17.5% over the transmit power from 24dBm to 20dBm. As evolving to HSPA (high speed packet access) mode, the EVM has to be lower than 6%.

To minimize the interference to neighboring channels, an adjacent channel leakage ratio (ACLR) has to be lower than -33dBc at 5MHz offset, and lower than -42dBc at 10 MHz offset in WCDMA. To compensate the near-far effect, the WCDMA transmitter needs to provide more than 74dB of gain control with 1dB steps.

1.2.5 The Error Vector Magnitude (EVM)

The error vector magnitude (EVM) is a measure used to quantify the performance of a digital radio transmitter or receiver. A signal sent by an ideal transmitter or received by an ideal receiver would have all constellation points precisely at the ideal locations, however various imperfections in the implementation (such as carrier leakage, low image rejection ratio, phase noise etc.) cause the actual

constellation points to deviate from the ideal locations. Informally, EVM is a measure of how far the points are from those ideal locations.

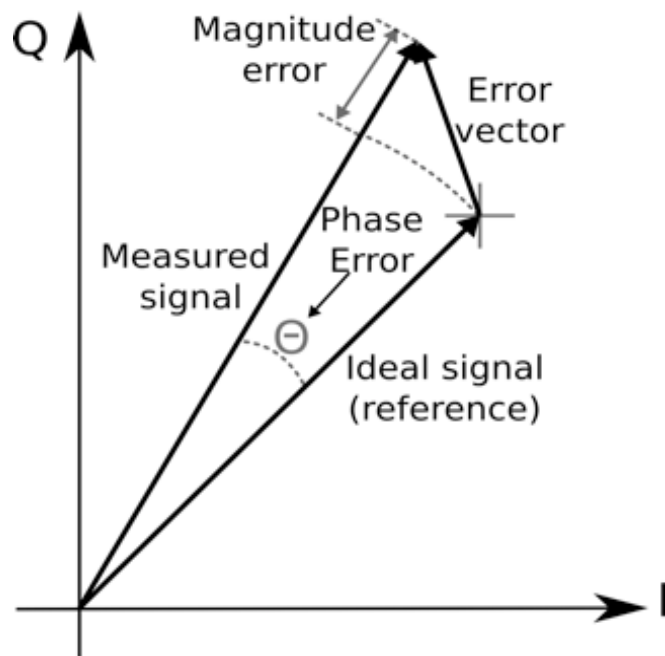


Figure 1.8: Error vector, magnitude error and phase error

EVM is usually used to benchmark the quality of the modulated signal in digital communication systems. It measures the distortion both in magnitude and phase. The EVM degradation is caused by a lot of factors, including the inter-modulation, IQ imbalance, phase noise and dc offset. Each factor will dominate under different conditions.

For high and moderate output power, the main contributor to a large EVM is the image signal caused by IQ imbalance in the LO and baseband signal.

Noise, distortion, spurious signals, and phase noise all degrade EVM, and therefore EVM provides a comprehensive measure of the quality of the radio receiver or transmitter for use in digital communications. Transmitter EVM can be measured by specialized equipment, which demodulates the received signal in a similar way to how a real radio demodulator does it. One of the stages in a typical phase-shift keying demodulation process produces a stream of I-Q points which can be used as a reasonably reliable estimate for the ideal transmitted signal in EVM calculation.

An error vector is a vector in the I-Q plane between the ideal constellation point and the point received by the receiver. In other words, it is the difference between actual received symbols and ideal symbols. The average power of the error vector, normalized to signal power, is the EVM. For the percentage format, root mean square (RMS) average is used.

The error vector magnitude is equal to the ratio of the power of the error vector to the RMS power of the reference. It is defined in dB as:

$$EVM(dB) = 10\log \left(\frac{P_{error}}{P_{reference}} \right) \quad (15)$$

where P_{error} is the RMS power of the error vector. For single carrier modulations, $P_{reference}$ is, by convention, the power of the outermost (highest power) point in the reference signal constellation. More recently, for multi-carrier modulations, $P_{reference}$ is defined as the reference constellation average power.

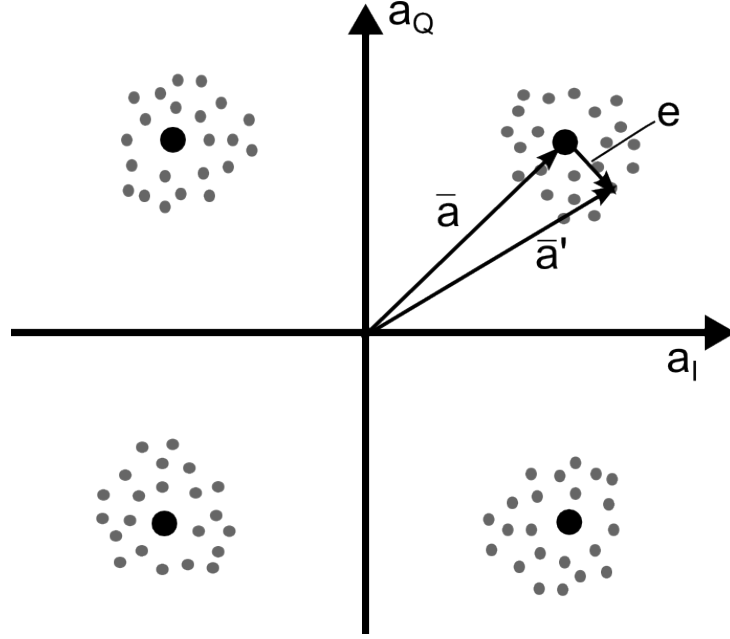


Figure 1.9 : EVM representation for a 4QAM signal

EVM is defined as a percentage in a compatible way:

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{reference}}} * 100\% \quad (16)$$

A more accurate way to see this define EVM as the mean square error between the samples of the actual and ideal signals, normalized by the average power of the ideal signal.

The EVM can be mathematically expressed as:

$$EVM = \sqrt{\left[\frac{E\{|\bar{a}'(k_1) - \bar{a}(k_1)|^2\}}{E\{|\bar{a}(k_1)|^2\}} \right]} = \sqrt{\left[\frac{E\{|\bar{e}(k_1)|^2\}}{E\{|\bar{a}(k_1)|^2\}} \right]} \quad (17)$$

Chapter 2: Transceiver design

The design of RF transmitters for wireless application entails many challenges at both architecture and circuit levels. The number of off chip components, the type of modulation schemes the restrictions on the unwanted emissions and the trade-off between the output power efficiency and the linearity directly impact the choice of the transmitter topology and the implementation of each circuit block [8-9]. This chapter provides an overview of the different transmitter topology for wireless communication, from the constant envelope to the non-constant one, analyzing the polar and Cartesian transmitter and discussing about topology with passive or active mixers.

An RF transmitter performs modulation, up-conversion, and power amplification, with the first two functions combined in some cases.

Transmitter design requires a solid understanding of modulation schemes because of their influence on the choice of such building blocks as up-conversion mixers, oscillators, and power amplifiers (PA).

In this section, are briefly described two commonly-used modulation formats and their design implications.

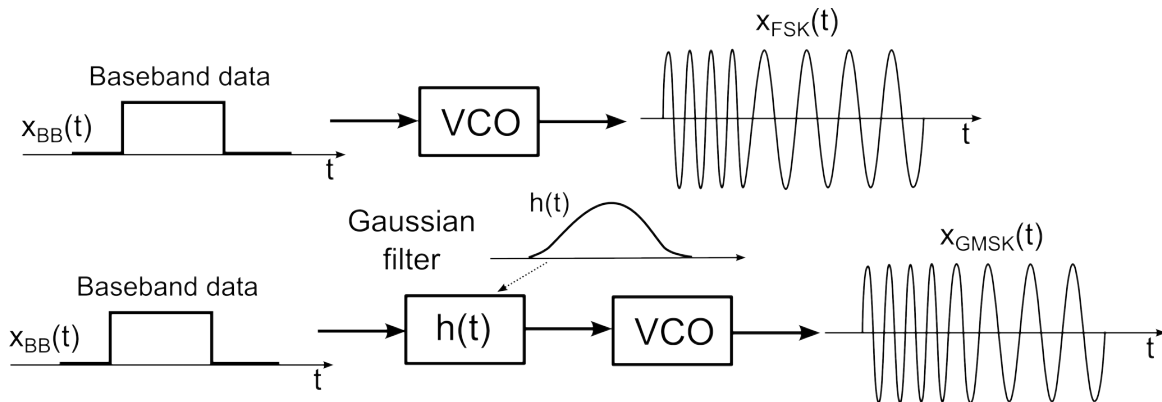


Figure 2.1 FSM and GMSK signal circuit generation

The design of transmitters deals with primarily the trade-off between bandwidth efficiency and power efficiency, an issue arising from the properties of “constant-envelope” (or “nonlinear”) and “variable- envelope” (or “linear”) modulation schemes [10]. A modulated signal $z(t) = A \cdot \cos[\omega_c t + \phi(t)]$ has a constant envelope if A does not vary with time.

Such a waveform carries information in only the zero-crossing points and can therefore be processed by a nonlinear power amplifier with high power efficiency. A simple example is binary frequency shift keying (BFSK), whereby the baseband rectangular pulses are directly applied to a voltage-controlled oscillator (VCO) Fig. 2.1.

In this case, $\phi(t) = K_{VCO} \int x_{BB}(t) dt$, where K_{VCO} is the gain of the VCO and x_{BB} the base band signal.

While exhibiting a constant envelope BFSK signal occupy a relative wide spectrum, partly owing to the abrupt frequency jumps introduced by sharp edges of the baseband pulses. If the frequency changes more smoothly from one bit to the next, then the required bandwidth decreases.

To this end, Gaussian minimum shift keying (GMSK) alters the shape of the baseband pulses so as to vary the frequency gradually. As shown in Fig.2.1 the baseband data are first applied to the Gaussian filter, thereby generating smooth edges at the input of the frequency modulator.

The resulting output is expressed as:

$$x_{GMSK}(t) = A \cos[\omega_c t + K_{VCO} \int x_{BB} * h(t) dt] \quad (18)$$

Where $h(t)$ is the impulse response of the Gaussian filter.

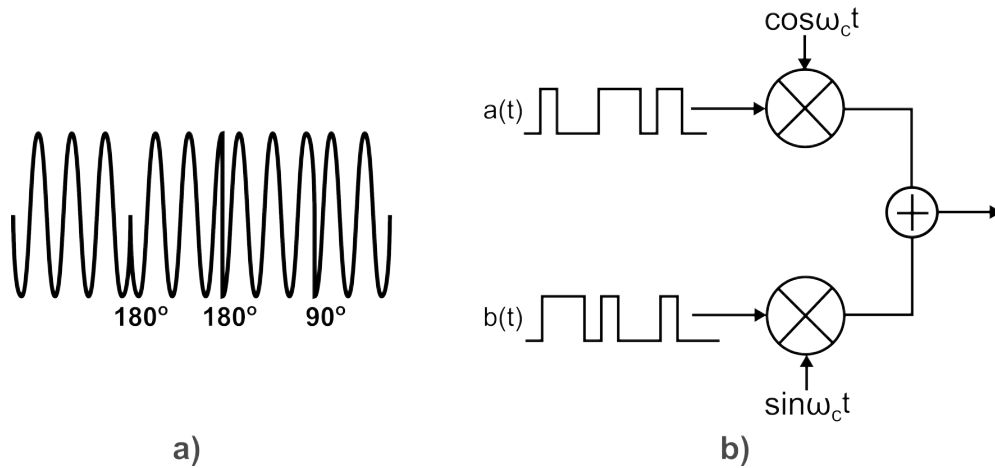


Figure 2.2: a) QPSK signal b) QPSK circuit generation

GMSK lends itself to non linear amplification, however the Gaussian shaped pulses suffers from overlap in the time domain, introducing intersymbol interference.

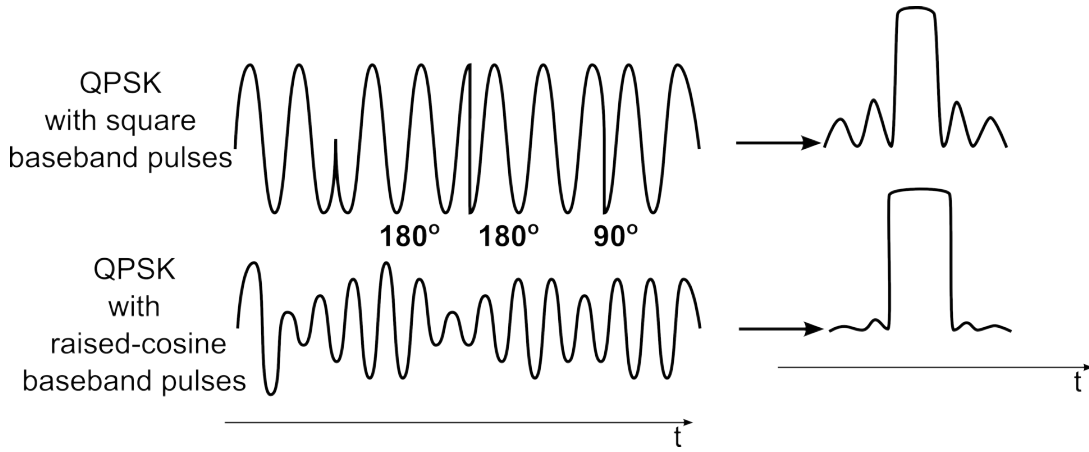


Figure 2.3: Constant and non constant envelope signal in time and frequency domain

Variable envelope signals are also used in many communication system. Such signals can be expressed as $x(t) = A(t)\cos[\omega_c t + \varphi(t)]$ where $A(t)$ is the envelope. The variation of $A(t)$ with time is undesirable but typically inevitable in linear modulation schemes designed to occupy a small bandwidth.

Considering a quadrature phase shift keying (QPSK) waveform with abrupt phase jumps showed in Fig.2.2. Expressed as $x(t) = a(t)\cos\omega_c t + b(t)\sin\omega_c t$ where $a(t)$ and $b(t)$ are sequence of rectangular pulses, the signal can be generated as shown in Fig.2.3 indicating the output spectrum is of the form $[\sin(\pi T_s f)^2]/(\pi T_s f)^2$, where T_s denotes the width of one pulse. Such a waveform can be amplified non linearly without corruption the information, but it consumes bandwidth. In order to tighten the spectrum of QPSK waveforms, the baseband pulses are altered from a rectangular form to a shape exhibiting a more compact spectrum. A popular format in “raised-cosine” filtering, where each bit is represented by a sinc-like waveform.

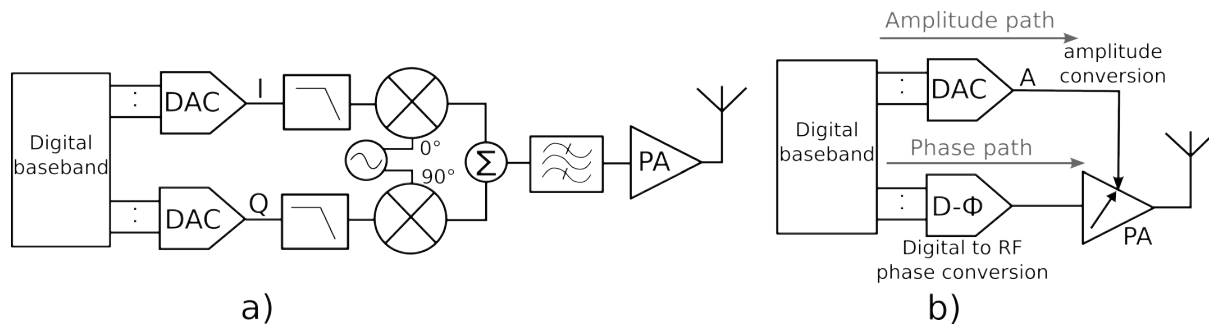


Figure 2.4: a) Cartesian transmitter block diagram, b) polar transmitter block diagram

QPSK with raised cosine filtering occupies less bandwidth but has variable envelope. If such a signal is applied to a non linear PA then the output exhibits high power on the adjacent channel possibly violating the emission mask requirements of the standard. For this reason this kind of signals require linear power amplifiers. In current EDGE and WCDMA transmitter design the zero-IF Cartesian architecture is widely adopted. However, in addition to that, there are also the polar and the envelope-tracking configuration. Such architecture uses dynamic voltage regulation to increase average efficiency of the power amplifier (PA) across the expected operating power range.

As shown in Fig. 2.4, in the Cartesian transmitter the baseband signal is split into I-path and Q-path. After the low-pass filters (LPF) the IF signals are up-converted to RF by the Gilbert mixer. The summed RF signal is amplified by the PA driver before driving the external PA. Compared to the direct digital RF transmitter, there is no aliasing spurs thanks to the use of LPF. In contrast to the polar architecture, there is no spectral regrowth issue. However, in conventional designs it suffers from the high noise generated by the Gilbert mixers, necessitating either a TX SAW filter between the transmitter and the PA or relative high current consumption. This section describes the state of the art of transmitter with active and passive mixers. The state of the art for cartesian transmitters with passive voltage mixer shows how this can replace the Gilbert mixer, leading to a possible improvement in the performances in terms of power consumption, noise floor, linearity, LO leakage and EVM but also shows the different drawbacks that request still the use of the active mixer.

2.1 Gilbert Mixer

Active mixers are the most common choice for up-conversion in transmitters [11-14]. These mixers isolation essentially eliminates IQ crosstalk.

As shown in Fig. 2.5, in the Gilbert mixer (active current mixer), the voltage input is first converted to current, and then up-converted to RF by the multiplier.

The up-converted I/Q output currents are summed at the RF output. In practice most of the noise is generated by the voltage to current (V-I) conversion circuit.

Without taking into account the noise in the switches, the noise in the Gilbert mixer can be approximated as:

$$N^2 = \left(\frac{4}{\pi}\right)^2 4kT\gamma g_m R_p^2 + 4kTR_p = \frac{4kT\gamma G^2}{g_m} + \frac{kTG}{g_m} \quad (19)$$

Where $G = 4/\pi g_m R_p$, G is the voltage gain of the Gilbert mixer. In the Gilbert mixer the maximum output swing is constrained by the linearity requirement, while the input IF voltage swing is preferred to be relatively high for larger SNR. Consequently the voltage gain is fixed. To lower the noise in the Gilbert mixer, the only choice is to increase g_m and lower the load impedance, leading to increased power consumption. In a real implementation tens of mA currents have to be consumed, in order to meet the noise floor requirements in EDGE and WCDMA.

The V-I conversion performed by the transconductor not only generates considerable noise, but also degrades linearity even if there are different solutions that can be implemented to enhance the performance of the V/I conversion before the mixer.

In addition, the mismatch of I/Q V-I conversion gives rise to an image, which degrades the transmitter EVM. The I/Q DC current offset also causes LO leakage to RF, which again deteriorates the EVM at low output level. Note that circuits with feedback topology can be employed to enhance the linearity of the V-I conversion, but at the price of reduced voltage headroom or noise performance.

Another drawback of the Gilbert mixer is that it does not favor the scaling-down of CMOS processes. To achieve the desired linearity, a high supply voltage is still preferred in the Gilbert mixer. To avoid DC offset calibration, large sized input transistors are necessary, which do not shrink as the process scaling-down.

The Gilbert up-conversion mixer might be replaced by a passive current mixer that allows for a low supply voltage, as it happens in the receiver design.

For this reason the first attempt in the research of a novel high linear and power saving structure was a transmitter that implemented a passive mixer and took advantage of the use of high linear current mirror configuration.

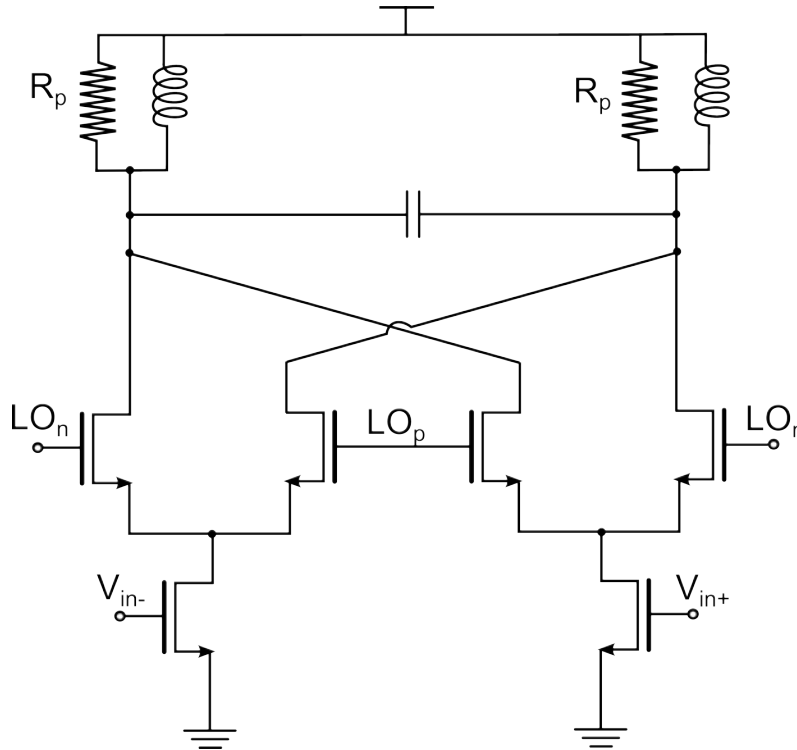


Figure 2.5: Active Gilbert mixer schematic

However, since a V-I conversion circuit is needed to convert the voltage output of LPF to the current input of the mixer, the problem caused by the V-I conversion still exist. There are also other problem arising in the use of passive mixers and they will be discussed in the next paragraph with also the description of the first structure analyzed.

2.2 Passive Voltage Mixer

The first type of transmitter studied and analyzed was a current transmitter in which the core of the modulator was a passive voltage mixer driven by 25% duty-cycle LO. The idea came from a work published by Xin He and Van Sinderen [15] presented at the ISSCC 2009 and also described in [16-17]. Passive mixers, although now common in receivers, are not widely used in transmitter architectures. This because, unlike an active mixer, in a passive mixer there is no reverse isolation.

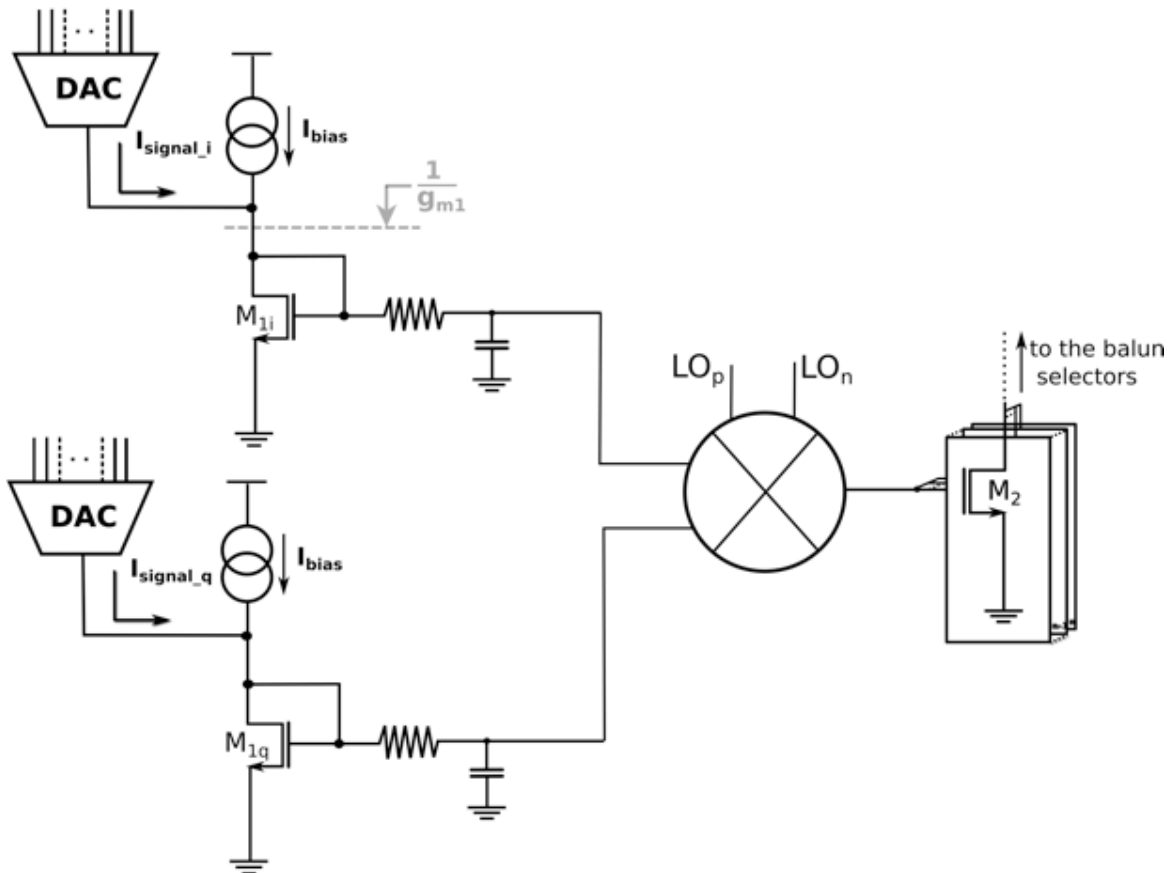


Figure 2.6 : Schematic of the transmitter that implements a passive mixer

As a result of this lack of reverse isolation, a passive mixer translates baseband impedances seen from its baseband side to the RF and vice versa through frequency shifting. But there are also other drawbacks described in detail in the next lines.

Despite that the new idea showed that in comparison to the conventional approaches employing Gilbert mixers, the use of a passive voltage mixer resulted in significantly improved performance in terms of the output noise, linearity, LO leakage, EVM, and the power consumption in the transmitter. Delivering 4dBm WCDMA output power at 1950 MHz, the transmitter prototype fabricated in a 45 nm CMOS achieved 48dBc ACLR at 5 MHz offset, 71dBc ACLR at 10 MHz offset, 54dBc LO leakage, and 1.36% EVM, while consuming only 26mW. The measured noise floor at 4dBm output is 159dBc/Hz at the frequency offset above 40 MHz, which is sufficient to safeguard the WCDMA RX band, the DCS band, and the GPS band without needing a TX SAW filter. In this case however the transmitter was driven in voltage mode at the input of the mixer, the DAC was not integrated in the chip.

For the new type of transmitter proposed, instead, the idea was to integrate all the transmitter, from the DAC to the baluns, as it's shown in Fig. 2.6, the structure is designed to be a full class AB transmitter composed by a current mirror with a filter and passive mixer in between.

The driver amplifier is focused on the good linearity with relatively low ACLR, especially for a large output signal. It is realized by cancelling the IM3 product at a large output power.

M_2 also provides a gain control range. Compared to traditional class AB transmitter, the structure can provide linearity optimization over a specific input region and hence be more flexible.

The amplifier is sliced into a number of identical cells to provide different gains. For high gain mode, all slices are turned on and consume the largest power. For the other gain settings, some of the slices are shut down. To achieve a 6 dB gain control step with a small step error, careful simulation is done to decide on the number of slices.

The analysis of this structure starts looking at the linearity of the structure at low frequency so without adding the passive mixer.

Without the passive mixer we can have a simple current mirror with an RC filter in between. The current at the drain of M_2 can be derived as follows:

$$I = I_{dc} + G_m v_{gs} + \frac{G'_m}{2!} v_{gs}^2 + \frac{G''_m}{3!} v_{gs}^3 + \dots \quad (20)$$

Where $G_m = \frac{dI}{dV_{gs}}$, $G'_m = \frac{d^2I}{d^2V_{gs}}$ and $G''_m = \frac{d^3I}{d^3V_{gs}}$

Equation (20) and Figure 2.7 show the Taylor expansion of the I–V characteristic of a transistor. The coefficient of the 3rd order term, G''_m , toggles from negative to positive with different DC biases.

With careful design on the bias current and W/L aspect ratio, IM3 generated from M_1 could be cancelled out by the one from M_2 and reduce the IM3 to a very tiny value at a certain bias region.

However this condition is very vulnerable to PVT variation and also the presence of the passive mixer alters the operation point due to the switched capacitor effect. Moreover the driving impedance of the passive filter is $1/g_m$ that is signal dependent altering the linearity of the input signal.

As shown in Fig. 2.8, the passive voltage consists of four switches driven by 25%-duty-cycle LO. By switching on/off the switch transistors through the quadrature-phased LO, the IF quadrature input voltages V_{I+} , V_{I-} , V_{+I+} , and V_{+I-} are sequentially sampled to the voltage mixer output, which sees an open load. Such operation leads to a direct quadrature voltage modulation. Because of the high impedance at the RF output, ideally there is no AC or DC current.

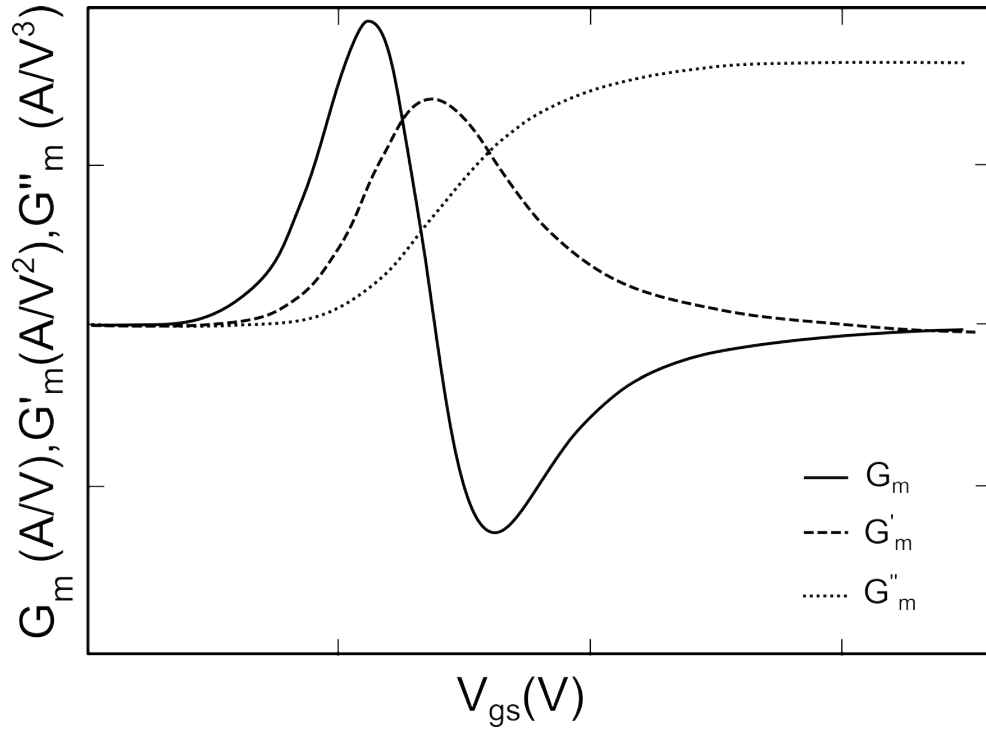


Figure 2.7: Expansion coefficient vs bias voltage

The operation of the voltage up-conversion mixer can be simply illustrated by the behavior of one-tone test in the time domain. Apparently it contains both the desired fundamental harmonic and unwanted higher-order harmonics. The conversion gain and the level of harmonics can be derived in the frequency domain. Equation 21 presents the corresponding Fourier series of the LO waveforms with 25% duty cycle. Combining the Fourier series in the complex domain yields the equivalent expression:

$$LO = \frac{2\sqrt{2}}{\pi} (e^{j\omega_{LO}t} + \frac{1}{3}e^{-j3\omega_{LO}t} + \dots) \quad (21)$$

Which indicates a conversion gain of -0.9dB for the fundamental frequency. There is no even-order harmonics because the sign of the second order is same and they are cancelled out after subtraction. This analysis is valid for the single-ended voltage mixer. For the differential voltage mixer, the

conversion gain is 6dB higher. In contrast to the conventional Gilbert mixer driven by 50%-duty-cycle LO, the passive voltage mixer using 25%-duty-cycle LO exhibits 3 dB higher conversion gain.

The proposed voltage mixer achieves superior performance over Gilbert mixers in terms of power consumption, noise floor, linearity, LO leakage, and EVM. Not taking into account the V-I conversion, the noise generated by the voltage mixer is mainly determined the thermal noise of the switches' on-resistance R_{ON} , given by:

$$N^2 = 4 \cdot 4KTR_{on}D = 4KTR_{on} \quad (22)$$

Where D is the LO duty cycle (25% here). R_{on} can be further calculated by:

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \quad (23)$$

Where V_{gs} is the gate source voltage, V_{th} is threshold voltage, W and L are the width and the length of the switch transistors, respectively. Without accounting the noise contribution from the LO, the mixer output spot noise N_{mixer} with respect to the maximum RMS output power P_{RMS_max} can be expressed as

$$\begin{aligned} N_{\frac{mixer_{dBc}}{Hz}} &= \frac{N_{mixer}}{P_{RMS_max}} = \\ &= 10 \log \frac{4kTR_{on}}{V_p^2} + PAR = \\ &= 10 \log \frac{4kTL}{V_p^2 \mu C_{ox} W (V_{GS} - V_{TH})} + PAR \end{aligned} \quad (24)$$

Where V_p is the peak swing of the voltage mixer output, and P_{par} is the peak average ratio in dB of the modulated signal. In the voltage mixer the peak swing is constrained by the linearity requirement, which is similar to the case in the Gilbert mixer.

The thermal noise of the switch transistor is much smaller than the noise generated in the V-I conversion in the Gilbert mixer. Given 10Ω switch-on resistance in each mixer switch, 0.25V single-ended peak swing, and 4dB PAR, the calculated noise floor is -172dBc/Hz, leaving enough margins for the targeted noise floor level without a TX SAW filter. With the scaling-down of CMOS processes, the size of the switches can be further shrunk, resulting in reduced noise as well as power consumption in the LO generation circuit.

Moreover, without V-I conversion the voltage mixer introduces much less I/Q mismatch, leading to improved EVM. LO leakage is also reduced, since it is mainly caused by the capacitive mismatch in the switches. There is no need for DC offset calibration, which is often implemented in the Gilbert mixer.

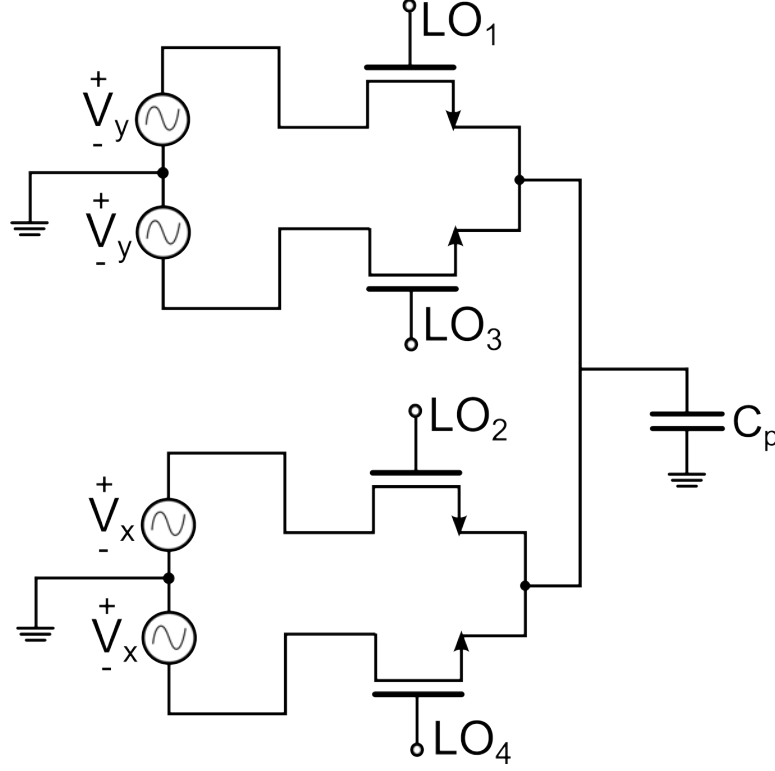


Figure 2.8: Passive mixer, switched capacitor effect

In reality a V/I conversion circuit still exist because usually the passive voltage mixers are followed by a PPA and then by the PA so a I/Q mismatch is possibly present. Moreover the conversion gain is lower in comparison to the gilbert mixer.

But despites a lot of advantages there are also some drawbacks, one of these is the switched capacitor effect.

Note that the parasitic capacitances are charged at the rate of the LO to the input voltage V_y , then to the V_x , $-V_y$ and finally $-V_x$ every cycle.

The total charge transferred during a period is given by :

$$Q_{tot} = C_p V_y - C_p V_x - (-C_p V_y) + (-C_p V_x) = 2C_p (V_y - V_x) \quad (25)$$

The net current is given by

$$I_x = \frac{Q_{tot}}{T_{LO}} = 2C_p (V_y - V_x) f_{LO} \quad (26)$$

Since there are two differential pairs connected to the op-amp terminals in parallel, the total charge is twice. So the effective resistance seen at this node is given by:

$$R_p = \frac{V_y - V_x}{2I_x} \quad (27)$$

The effective resistance is therefore given by:

$$R_p = \frac{1}{4f_{LO}C_p} \quad (28)$$

This is the switched capacitor resistor.

Another issue that regarding this structure is related to the current mirror. The performance of the simple two-transistor mirror is limited by the characteristics of a single MOS transistor. The output resistance is controlled directly by channel length modulation (and other short channel effects) affecting the achievable maximum linearity. For this reason a high compliance current mirror with regulated cascode was choose. The concept of the regulated cascode is to use feedback to ensure that the drain of the mirror transistor is held at some constant voltage in a feedback loop. However in this case this represents a problem because while before the mixer the gain stage in feedback needs only a limited bandwidth (few hundreds of megahertz) for the high frequency part (represented in Fig. 2.6 by the MOS M_2) the gain stage in feedback needs a higher bandwidth (at least few Gigahertz) in order to properly work as a regulated cascode and maintain the high linearity of the structure but this is not feasible at least without high current consumption. This, with the other issues described above, determined the decision to prefer a structure that implements an active current mirror.

2.3 Voltage mode approach vs Current mode approach

From what it has been analyzed before two are the main groups in which we can divide the RF cartesian transmitters:

- TX chain using voltage-mode baseband with a passive voltage mixers
- TX chain using current-mode baseband with an active current mixer.

The main difference between mixer types is that the active mixer consumes power, whereas the passive one does not. From the RF metrics point of view, the main difference is in the linearity performance and the required LO drive level. In order to switch properly, the passive mixer, in practice, demands a full rail LO signal. However, the linearity performance is superior as compared to the active mixer if we compare as stand alone device without the interaction of other parts of the circuit.

The first type of mixer can lead to five major problems:

- I and Q crosstalk since the two paths are superimposed at his output
- The switched capacitor effect of the input capacitance of the pre-power amplifier increase area and power consumption of the driver.
- Non-linearities and EVM degradation due to high signal swing necessary for high SNR on the passive mixer.
- Large LO drive, almost rail to rail
- Low conversion gain in comparison to the active mixer

The advantages of the passive mixer are:

- Very good linearity
- No current consumption
- No 1/f noise (because there is no DC current)
- Small area

On the other hand, TX chains using active current mixers do not suffer from the problems raised by the use of passive mixers, but the main drawback of this structure is the V/I conversion before the mixer that introduces noise and non-linearity and to reduce these problem needs a increasing in power consumption.

So in summary the advantages are:

- No switched capacitor effect
- Good isolation between I and Q path
- Small LO drive (usually the LO signal has an amplitude of 1.2V p-p for devices with 1.8V of Vdd)
- High conversion gain

The drawbacks of this structure are:

- High current consumption of the stage in order to reduce the out-of-band noise and increase the linearity
- Not very adaptable for scaled technologies since for high output power a relative high Vdd is need to satisfy the linearity requirements
- Bigger area in comparison to the passive mixer
- Presence of the LO leakage at the antenna

For the novel transmitter structure described in this work an active mixer was implemented because, despite the drawbacks, it's able to satisfy all the requirements needed for LTE transmission with relative low power consumption and area.

Chapter 3 :A Transmitter with Current-Mode Approach

A 55nm CMOS current-mode transmitter for multistandard wireless communications (including LTE) that requires only 1.5mm² (with 4 output ports) is described [13-14]. The circuit is considered the state-of-the-art for the novel structure presented in chapter 4. The circuit is made up of two portions: a class A/B up-converter and a baseband that includes DAC, VGA, low-pass filter (two Biquad plus a passive first order) and class A/B signal conditioner. Combining a third order filter with the class A/B conditioner results in a reduction of both current consumption and RX-band noise injection. For LTE10, the consumption is 96mW and 34mW at 4dBm and at -10dBm output power, respectively. The complete transmitter gives -158dBc/Hz RX-band noise injection at 30MHz offset.

In direct-up transmitter architectures, the baseband signal can be up-converted to the RF by using either voltage or current mixers. In the first case, the most promising approach operates in the voltage-mode and is implemented with a quadrature passive up-converter driven by a filtering stage, followed by pre-power amplifier (PPA). In the second case, the most efficient solution is based on a current power mixer, where the up-converter has also the role of a pre-power amplifier.

When a voltage passive mixer is adopted, the input capacitance of the PPA appears as a switched-capacitor (SC) load. This increases the area and power consumption of the baseband (BB) since such load can be driven only lowering the output impedance of the last stage of the BB to reduce I and Q interaction. Furthermore, the mixer's switches must bear a large voltage swing without introducing non-linearity or degrading EVM.

Current-mode transmitter solutions are immune from SC loading and I and Q cross-talk. However, since the BB section generally still operates in voltage-mode, an additional linear V-I conversion stage is needed to drive the current-mode mixer. This makes voltage and current-mode solutions comparable in terms of power/area cost.

The transmitter considered as the state of the art is a transmitter where the signal can be completely processed in the current domain from the DAC to the mixer output.

The transmitter is an evolution of the one reported in [12], where the filter used to minimize out-of-band noise and to remove DAC replicas is merged with the mirror stage that drives the class A/B power mixer. The result is a TX chain with high efficiency and lower RX-band noise (especially for narrow spacing) compared to the state of the art of 4G cellular transmitters.

3.1 Current mode transmitter

A conceptual block diagram of the proposed in [13-14] transmitter is shown in Fig. 3.1 while the complete schematic is shown in figure 3.2.

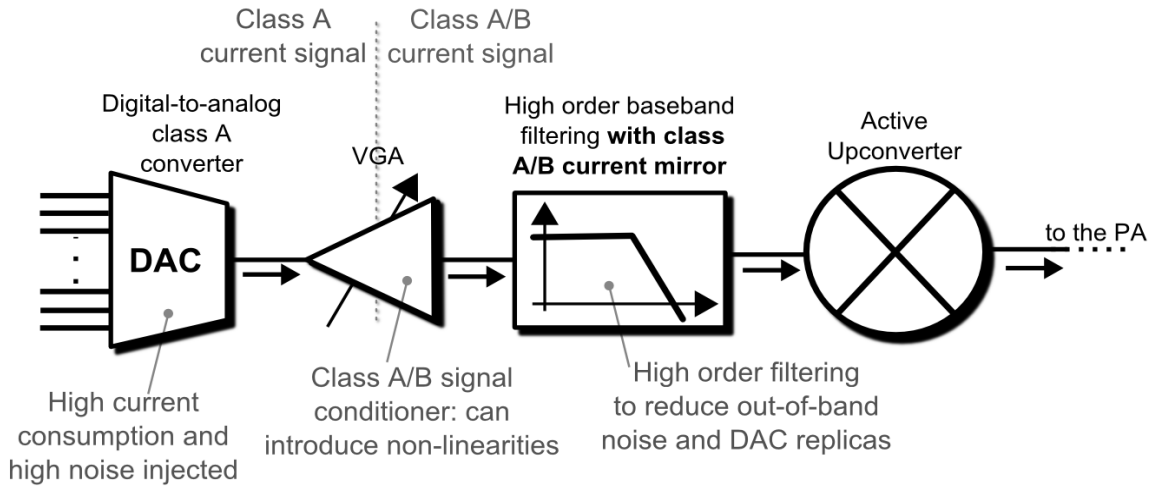


Figure 3.1: conceptual block diagram of the TX proposed in [13-14]

The output signal provided by a current-steering DAC is buffered, scaled up and sent to a current driven third order filter that provides the class A/B output current to the power mixer.

Compared to the solution reported in [12], the wideband V-I converter at the end of the TX chain is transformed in a current driven filtering stage.

So the main in purpose of the structure proposed in [12] is to eliminate the V/I conversion stage since the block of a voltage-mode connected with a current-mode up-converter must be a linear V-I converter, there is no space for another active biquad at the end of the chain. Second there is the need to move the filter at the end of the baseband chain in order to filter the DAC replicas, non linearity and out-of-band noise with a single filtering stage as it is already done in the voltage mode transmitters.

Moving the filter in the last building block of the baseband chain not only potentially reduces power consumption (having merged two blocks into a single one) but also provides sharper filtering for the out-of-band noise of the baseband. This becomes crucial in SAW less applications when the TX-band and RX-band spacing is narrow and the signal channel large (e.g. LTE10 Band17, LTE20 Band20).

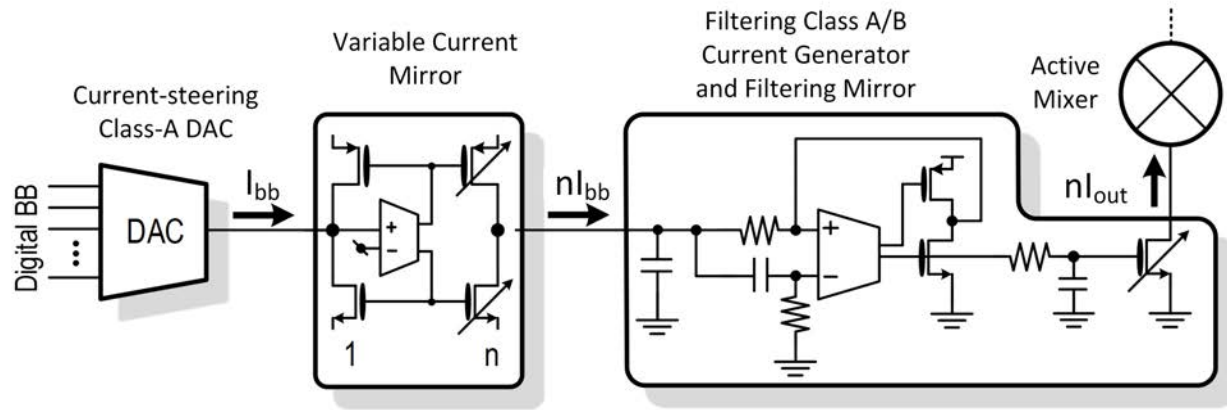


Figure 3.2 : schematic of the state of the art of TX proposed in [13-14]

3.2 Class A/B variable current mirror

The first stage of the TX chain is a variable gain current mirror that buffers the DAC output. The mirror, operated in class A/B for better power efficiency, minimizes the voltage swing at the output of the DAC to increase its linearity, has a large output impedance to drive the following stage in current and allows gain control.

A two-stage class A/B OTA drives the gates of a push-pull stage, realizing a boosted diode connection where the input impedance is lowered by a factor equal to the loop gain.

The input current is then mirrored to the output through a scaled replica of the input branch.

This block however is a significant noise contributor and can introduce non-linearity. The solution to overcome these problems will be explained in the next chapter where an implementation without the need of a class A/B conditioner will be described.

The core of the transmitter is the filtering signal conditioner that drives the power mixer in class A/B (Fig. 3.2). This block derives from the V-I converter proposed in [12]. The converted current is absorbed by the OTA output stage and fed to the mixer in a way that corresponds to an N-only class A/B transconductor [12].

The state-of-the-art current-mode TX chain, on the contrary, does not need any V-I converter, while the N-only class A/B transconductor is still necessary. The OTA is then used to implement an active inductor that creates a second order low-pass transfer function as it's shown in Fig.3.3.

The inductive behavior is obtained creating a high-pass virtual short between the terminals of the input resistor R_1 .

This reduces the high-frequency components of the current absorbed by the OTA. The virtual short is realized adding a high pass filter (C_2R_2) between the terminals V_{in} and the inverting input V_- of the OTA (Fig. 3.3).

At low frequency all the input current is absorbed by the OTA (neglecting C_1 for the moment) since C_2 is an open circuit and terminal V_+ is virtually shorted to ground. On the contrary, above the cut-off frequency $1/R_2C_2$, V_+ becomes equal to V_{in} and the two terminals of the resistor are virtually shorted preventing any flows of current into the OTA. A capacitor C_1 is then added at the input, leading to a second order filtering profile with an in- band gain of one, and I and Q given by:

$$\omega_0 = \frac{1}{\sqrt{R_1C_1}\sqrt{R_2C_2}} \quad (29)$$

$$Q = \frac{\sqrt{R_2C_2C_1}}{\sqrt{R_1}(C_1+C_2)} \approx \frac{\sqrt{R_2C_2}}{\sqrt{R_1C_1}} \quad \text{if } C_1 \gg C_2 \quad (30)$$

To manage multiple wireless standards using the same architecture, the ω_0 must be reconfigurable. Its value should be as close as possible to the signal bandwidth (in trading-off with EVM, area and linearity) to perform the maximum filtering. Equations (29) and (30) show that it is possible to change without changing the Q factor (i.e. maintaining the same filter shape).

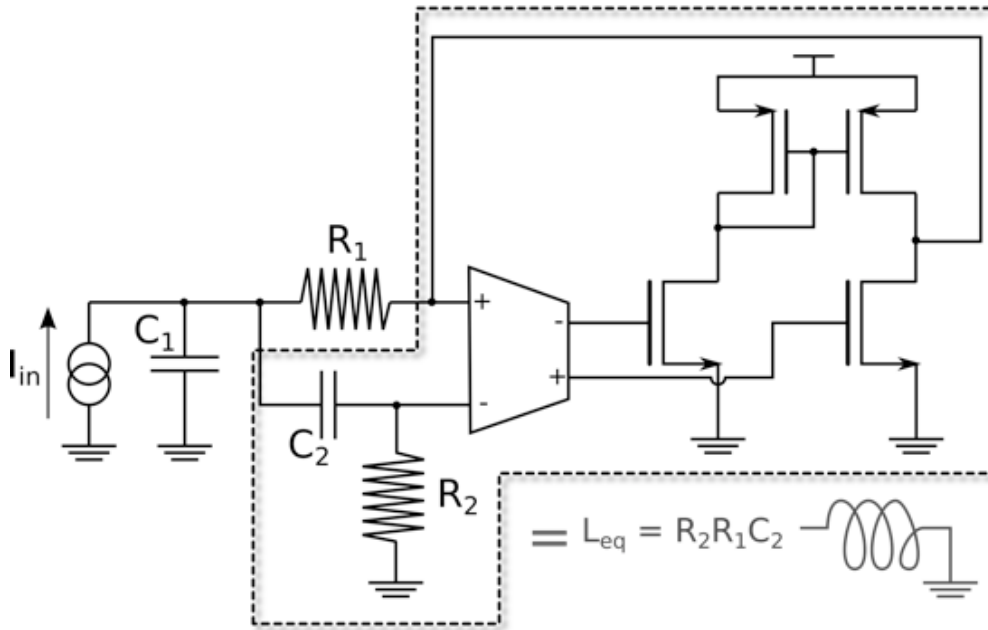


Figure 3.3 : Filtering class A/B conditioner

Moreover, ω_0 and Q are not affected by the signal level since they are only a function of passive elements. In [18], a similar current-mode approach in the BB filtering was proposed for 3G standard, but the filter parameters were related to MOS transconductance (g_m) values. Since, to improve the signal-to-noise ratio (SNR), the swing is usually maximized, the g_m varies substantially with the signal level.

Time-variance of g_m makes the filter signal-dependent causing distortion and degrading the EVM.

This issue will be dominant also in new TX structure and will be discussed in the next chapter.

While in a receiver the filters should be placed at the beginning of the analog chain to eliminate the interferers, in a transmitter the filtering should be done at the end of the BB to minimize its out-of-band noise and non-linearity. This is easily implementable in a voltage-mode transmitter [15], [16-17] and it was also proposed for the 3G current-mode transmitter in [18].

However, when using a voltage-mode approach in BB and a power mixer as in [12], [19], a V-I converter is required just before the up-converter. The noise of the V-I converter and that of the preceding block is not filtered. Therefore, to lower out-of-band noise, the power consumption of the BB stages is usually scaled-up toward the mixer. Moving the main filter in the last stage of the chain makes the noise of the preceding stages negligible making this solution potentially better than the one described in [12], [19] for out-of-band noise while saving some power.

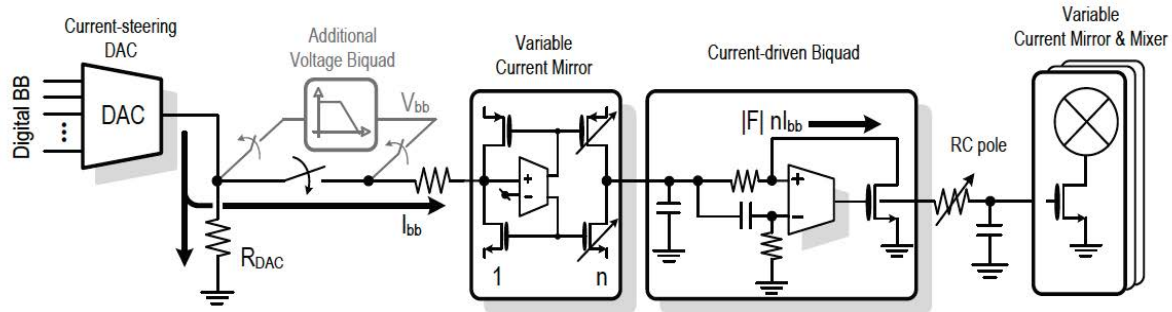


Figure 3.4 : Schematic of the TX proposed in [13]

The new filtering stage becomes the main noise contributor of the TX. However, since it is derived from the V-I converter of [12], its noise (which was already minimized and accounted for) remains practically unchanged. Indeed, the OTA and R_1 (Fig. 3.3) inject the same out-of-band noise as before, while R_2 , the only noisy element added, has a low-pass transfer function to the output and does not contribute significantly to the overall output noise.

The current-mode transmitter was implemented in a 55nm CMOS technology and tailored to 4G applications. A block diagram of the entire TX chain (I path-only) is shown in Fig. 3.4. To verify its advantages, the new solution was realized modifying the previous voltage-mode BB [12] while keeping the same DAC and the same class A/B power mixer.

To be compatible with the voltage output DAC and to be able to insert in the chain (for some critical standards) an additional biquad (as it is done in the previous design [12]), a V-I converter after the

DAC is required. This is done putting a resistor in series to the variable-gain mirror input which behaves as a virtual ground thanks to the large loop gain of the OTA. The variable mirror feeds the filtering class A/B conditioner that realizes a 3rd order low-pass filter thanks to the additional real pole that was already present in the final mirror. Finally, the output current is up-converted via the class A/B power mixer that delivers power to different baluns, according to the transmission band [12].

The full transmitter features either a 3rd or a 5th order Butterworth filter depending on the selectivity required for coexistence with other wireless standard. In both cases, reconfigurability (as a function of the target standard) of the cut-off frequency is implemented. For the former case, the entire chain is operated in class A/B, leading to high efficiency. This is not the case when a 5th order filter is used.

However, acting on the DAC oversampling (at very little cost in scaled--down technologies) it should be possible to use the fully class A/B (3rd order) chain for all cases with a further benefit in power consumption and out-of-band noise. Finally, in-band gain control is implemented changing the geometric factor of the current mirrors.

3.3 Measurements Results

Fig. 3.5 shows the current drawn from the 1.8V supply for the entire chain (excluding DAC) versus transmitted power in Band2 for 3G and 4G (LTE10 and LTE20). This is almost independent of the standard and at low power (below -10dBm) is always less than 20mA. The difference between 3G or LTE10 and LTE20 is due to a larger OTA current, required to drive the last RC passive filter when its pole is tuned.

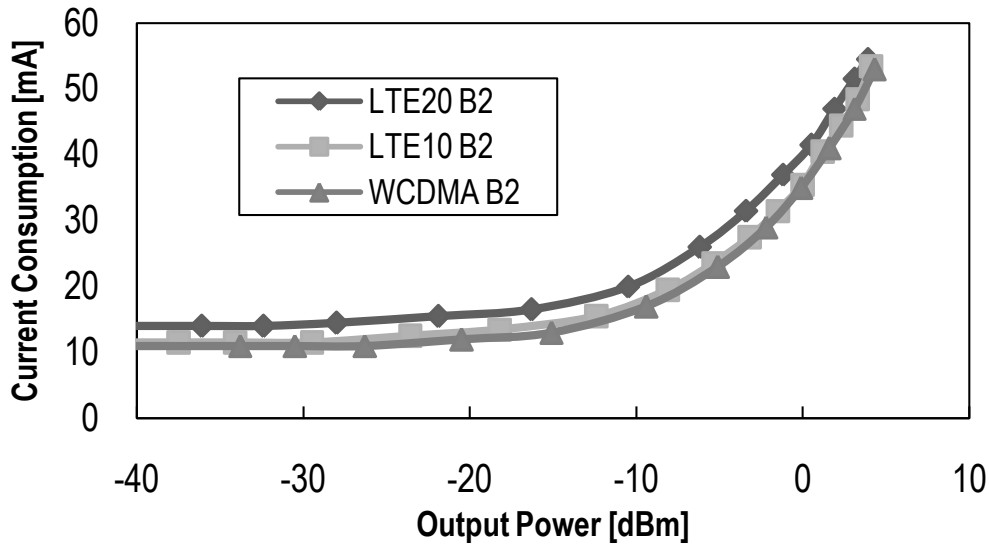


Figure 3.5: Current consumption vs output power

Fig. 3.6 also shows ACLRs measurements for 3G, LTE10 and LTE20 for Band2 for the left-side of the RF signal, which has a worse behavior than the right-side. ACLRE-UTRA1 and ACLR1 stay below -42dBc and -45dBc (for 4G and 3G) up to 4dBm while for the ACLR2 the range of values is between -53 to -57dBc.

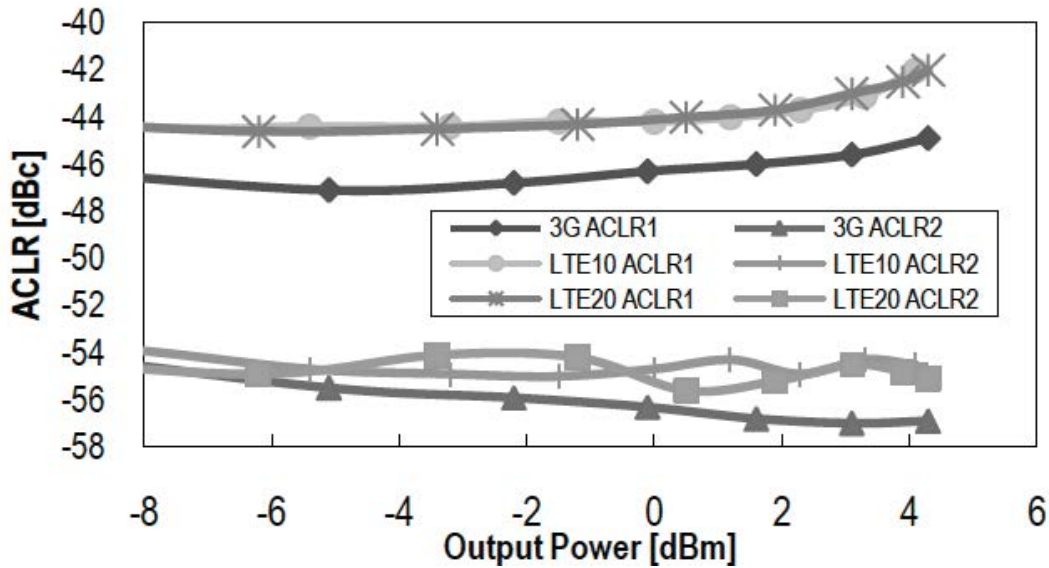


Figure 3.6: Diagram of ACLR (ACLR1 and ACLR2) vs output power with different input signals

At low power the linearity is limited by the baseband, while at higher power by signal compression in the up-converter.

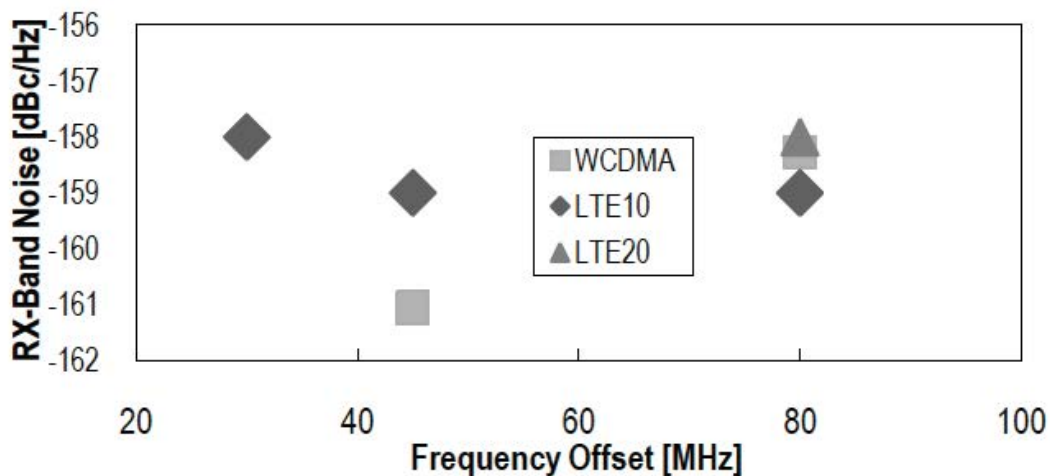


Figure 3.7 Out-of band noise at different frequency offsets

Fig.3.7 Shows the out-of-band noise performances where is possible to see that the requirements where satisfied even for the most stringent specification (-158 dBc @ 30 MHz offset) , the lowers out-of-band noise is registered for the WCDMA standard at 45 MHz offset from the carrier.

RX-band noise measurements for 4G standard have been made with transmitted signals composed of partial Resource Block (RB), as specified by 3GPP, while in the 3G case the full signal was used. The TX output was fed to the antenna port of a duplexer tuned to the target band and measurements were done on the RX port (with the TX port terminated on 50Ω), de-embedding the duplexer and cable attenuations. In this way, the transmitted signal was sufficiently suppressed by the stop-band of the duplexer to make it possible to measure the RX-band noise without saturating the spectrum analyzer.

The results for the bands with the most critical TX-RX offsets are reported in Fig. 3.6, at 0dBm output power. The worst case is the LTE10 Band17, with a TX-RX offset of 30MHz, where the transmitter shows -158dBc/Hz.

Table II: Comparison with voltage mode TX

Parameter	Units	[12]			This work		
Standard	-	LTE10	LTE10	LTE20	LTE10	LTE10	LTE20
Band	-	5	10	2	5	17	2
Output Power	dBm	2.45	0.4	2.6	2.8	0.2	3.1
ACLR E-UTRA1/2	dBc	-41.4	-41	-38.4	-43.4	-44	-43
@output power		-63	-67	-59	-54.9	-57.4	-54.5
EVM @output power	%	1.7	1.9	2.4	1.4	1.4	1.4
Consumption @ Output power	mW	111.2	101.2	126.4	97	90	93
RX-band noise @ Output power (frequency offset)	dBc/Hz	-160.5 ^a (45M)	-159 ^a (30M)	-162.5 ^a (80M)	-159 ^b (45M)	-158 ^b (30M)	-158 ^c (80M)
Supply Voltage	V	1.1/2.5			1.8		
Chip Area	mm²	0.98			1.06 ^d		
CMOS Technology	nm	40			55LP		

(a) Carrier-to-Noise ratio; (b) measured with 20RB; (c) measured with 50 RB; (d) without DAC, TT biquad and two baluns

A comparison with the state-of-the-art for 4G transmitters is given in Table II and Table III. Table II compares with a voltage-mode transmitter [12] for similar output powers and TX-RX offsets. Our solution shows better ACLRE-UTRA1 and less power consumption and, featuring only one (at 1.8V) supply as opposed to two (at 1.1V and 2.5V), is less costly.

Table III: Current mode Tx comparison

Parameter	Units	[19]	[11]	This work	[19]	[11]	This work
Standard	-	LTE10			LTE20		
Band	-	3.7	6	6	4	6	6
Output Power	dBm	3.7	4	4	4	4	4
ACLR E-UTRA1/2 @4dBm	dBc	-40.3	-44	-42	-40.3	-40.9	-42.5
EVM @0dBm	%	NA	-55	-54.5	NA	-55	-54.8
Consumption @ 4dBm	mW	0.66	1.8	1.8	1.05	1.4	1.4
Consumption @ -10dBm	mW	186	101	96	199	101	98
RX-band noise @ Output power (frequency offset)	dBc/Hz	56	39.5 ^a	34	70	39.5 ^a	36
Supply Voltage	V	-155 (30M)	-154 (30M)	-158 (30M)	-157 (120M)	-155 (80M)	-158 (80M)
Chip Area	mm²	1.55/2.7	1.8	1.8	1.55/2.7	1.8	1.8
CMOS Technology	nm	5.06	1.3	1.5	5.06	1.3	1.5
		90	55LP		90	55LP	

(a) ISSCC 2013 visual supplement [11]

RX-band noise is generally a bit larger for our implementation. However, in [12] the noise testing condition used (1MHz baseband tone) is not 3GPP compliant and can give significantly better results. Chip area is less than 10% larger in our implementation, but using an older technology.

Table III compares with two recent current-mode transmitters. Compared to [12], this solution shows an improvement of 4dB in LTE10 and 3dB in LTE20 in the RX-band noise and requires, respectively, about 3mA and 2mA less current thanks to the new BB. In LTE10, the corresponding improvement, although very small at 4dBm, is already about 16% at -10dBm and exceeds 25% at very low output power. On the other hand, area is increased by about 15%.

Compared to [12], a better RX-band noise and ACLR is present, worse EVM with a drastic power consumption (especially at high output power) and area reduction. Finally, also in this case the use of a single supply as opposed to two reduces costs. However this structure does not satisfy the linearity requirements above 4.5 dBm, in the next chapter a novel structure able to improve the linearity performances and the current consumption below 0dBm will be introduced.

Chapter 4: A low power/noise emission LTE fully class A/B transmitter

A current-mode transmitter for multi-standard wireless communications (including LTE) is described [20]. To limit both current consumption and RX-band noise a complete class A/B approach (from the DAC to the up-converter) is followed. The circuit is made up of three portions: a baseband that includes class B DAC and a second order low-pass filter (an active first order and a passive first order) combined with a class A/B up-converter. For LTE10 the current consumption (from a 1.8V regulated supply) is 47.5mW at 0dBm and 27.37mW at -6dBm output power respectively. The complete transmitter gives -160.5dBc/Hz RX-band noise injection at 30MHz offset (band 5 for LTE 10).

In this chapter a transmitter that operates entirely in class A/B is presented. The transmitter is an evolution of the state-of-the-art described in chapter 3 and presented in [13-14] conceptually shown in Fig. 3.1 whose operation is as follows.

The class A DAC drives (through a variable mirror) a current-driven stage that generates the class A/B current signal for the mixer while simultaneously implementing a second order filter. The output current I_{out} is delivered to the power mixer via a programmable current mirror that includes a passive filter between its input and output transistors. The variation of the bandwidth of the passive filter introduces a trade-off between noise emission and linearity.

The new transmitter proposed (Fig.4.1) allows the elimination of the class A/B conditioner by using a class B DAC instead of the class A DAC of the previous structure. In the proposed transmitter the following improved circuits are introduced: class B DAC, highly linear noise filtering current mirror and programmable output balun. The result is an improved linearity with simultaneously reduced power consumption in back-off and reduced RX-band noise for narrow frequency offset compared to state of the art 4G transmitters.

4.1 Overall architecture

A conceptual block diagram of the transmitter is shown in Fig. 4.1.

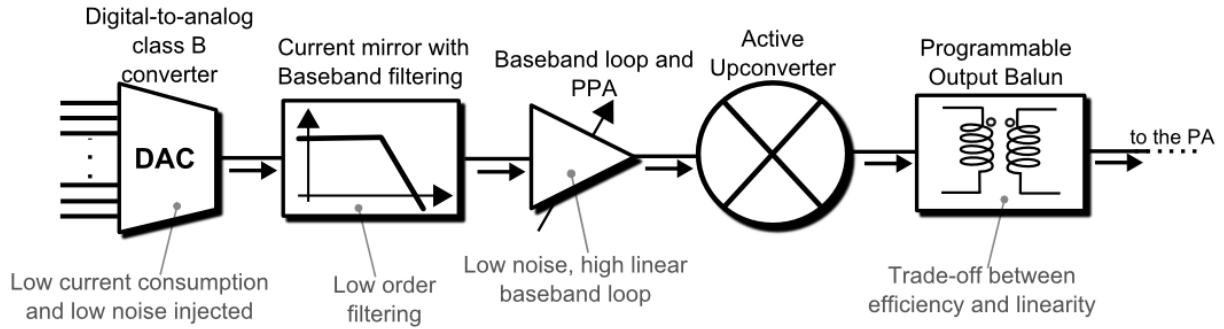


Figure 4.1 : Block diagram of the new proposed structure

The base band signal, provided by a class B current-steering DAC, is sent to the cascade of an active and a passive first order filter. The filter output modulates the voltage across a baseband loop with a programmable resistor whose current is sent to the power mixer and then to the output through a balun. All the baseband is pseudo-differential. The new structure is able to satisfy the LTE requirements with a second order filter thanks to the all class A/B operation and to the structure able to injected low out-of-band noise.

4.2 Starting Point Structure

The starting point to introduce the building blocks is a traditional analog baseband for an active mixer and here is shown in Figure 4.2. The DAC is a class B DAC and it is implemented in current-mode and mirrored trough M1 and M2 in order to achieve high linearity before the mixer. The I-V conversion is implemented with diode created with the first MOS (M1) that the first stage of a simple current mirror. After passing through a first order passive filter, the signal is then mirrored on the second MOS (M2). The mirror factor is variable according to the needed output power. This structure should be able to satisfy the requirements for LTE transmission for the out-of-band noise and the linearity thanks to the current mirror that is, for definition, a high linear circuit and, thanks to this high linearity, the cut-off frequency of the passive filter can be placed very close to the signal bandwidth edge or also ideally in band satisfying the noise requirement with a simple first order filter. Always keeping in mind that, when the filter cut-off frequency is very close to the signal band

a digital pre-compensation is needed in order to not degrade the EVM and to compensate the droop of the higher frequency signal tones.

In this way however for high signal swing the channel modulation effect is not negligible and introduces non linearity, moreover the RC filter doesn't let the circuit work as a linear current mirror and the driving impedance of the filter is equal to $1/g_{m1}$, an impedance that is signal dependent and therefore not linear.

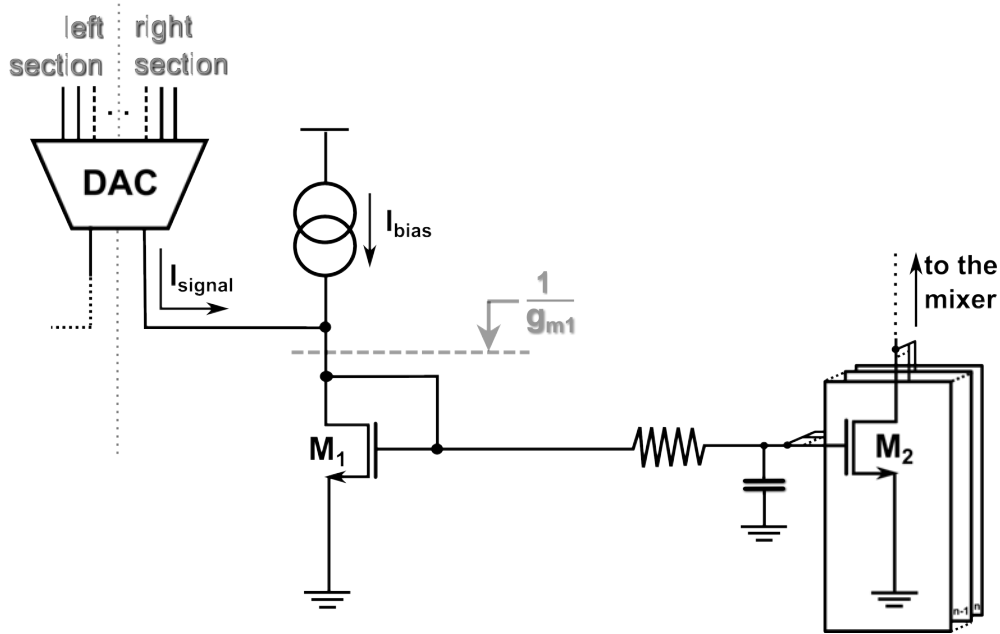


Figure 4.2 : Typical schematic of a transmitter with a high linear transconductor (R_{in}) with a driving current independent from I_{bias}

This is also the main limit of the transmitters described in chapter 3 since the linearity of the current mirror with the RC pole is limited. Moreover this structure imposes a trade-off between the maximum cut-off frequency of the filter that, if exceeded, can introduce non linearity, but a larger one can not filter the out-of-band noise and the DAC replicas in an efficient way.

Therefore, in order to be high linear, there is the need of high linear transconductor and a driving current independent from I_{bias} .

In order to satisfy this requirements the signal coming from the DAC is sent to a first resistor that makes a linear V/I conversion as it's shown in Figure 4.3.

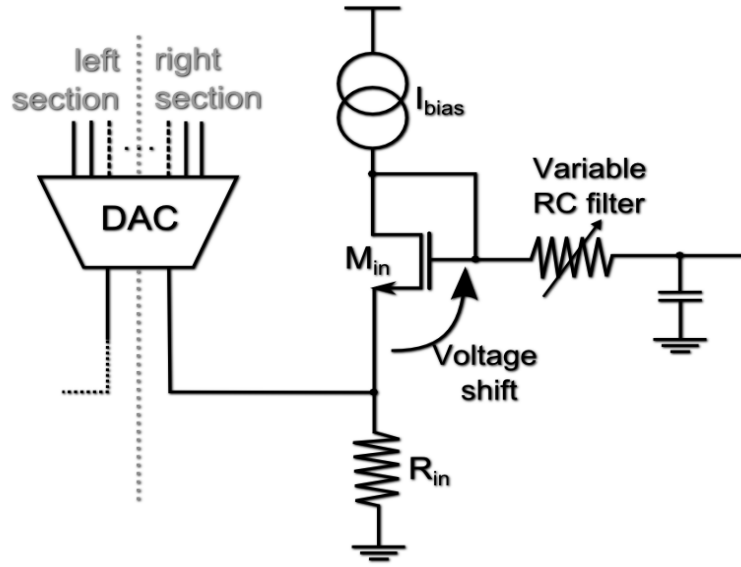


Figure 4.3: Baseband implemented with a high linear transconductor

In this way the V/I conversion is linear because the value of the resistor is signal independent. The voltage signal at the gate of the transistor M_{in} is expressed by the equation 31.

$$V_{gate} = (I_{in} + I_{bias})R + V_{GS} \quad (31)$$

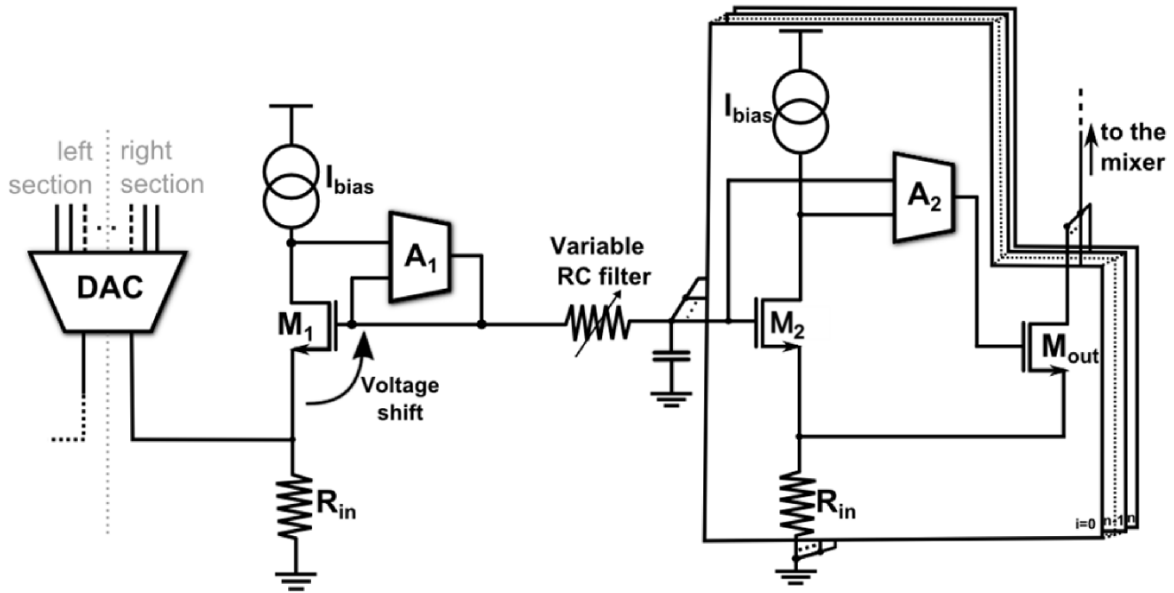


Figure 4.4: Schematic of the transmitter with a high linear transconductor (R_{in}) with a driving current independent from I_{bias}

However the driving impedance of the RC pole is $1/g_{min}$ that is signal dependent. Moreover the slew rate depends on I_{bias} and on the value of the capacitor. To overcome this problem an OTA is inserted in the path between the drain and the gate of M_1 as it is shown in Fig. 4.4.

The gate and the drain of M_1 and M_2 are virtually shorted in order to perform a high linear current mirror. Thanks to A_1 the bias current is forced to flow on M_1 and the driving impedance is now equal to $r_{OTA}/(1+g_{m1}r_{0A})$ where r_{OTA} is the output impedance of the OTA and $g_{m1}r_0$ is the gain of M_1 . This impedance is no more signal dependent.

The first resistor (R_{in}), that implements the I/V conversion, is fixed, the signal is then mirrored on a second resistor that is variable (R_{in}/n) in proportion to the variable current mirror that drives the active mixer and then sent to the active mixer through M_{out} .

The main use of the loop with a second OTA (A_2) is to force the signal to follow on M_{out} with high linearity.

To transform this baseband into a baseband with a second order filtering two step are necessary:

- First, an OTA that implements the current mirror's first stage as his own first stage and based on a pn structure is introduced after a current steering DAC.
- Second, the resistor of the current mirror's first stage is eliminated so now the voltage drop of R_{in} is recreated with the voltage drop on the feedback resistor.

In this way the out-of-band noise is lowered thanks to a second order filtering stage instead of a simple first order. Due to the high linearity of the structure the filter can be moved very close to the signal bandwidth to increase the filtering effect, the schematic is shown in Figure 4.5.

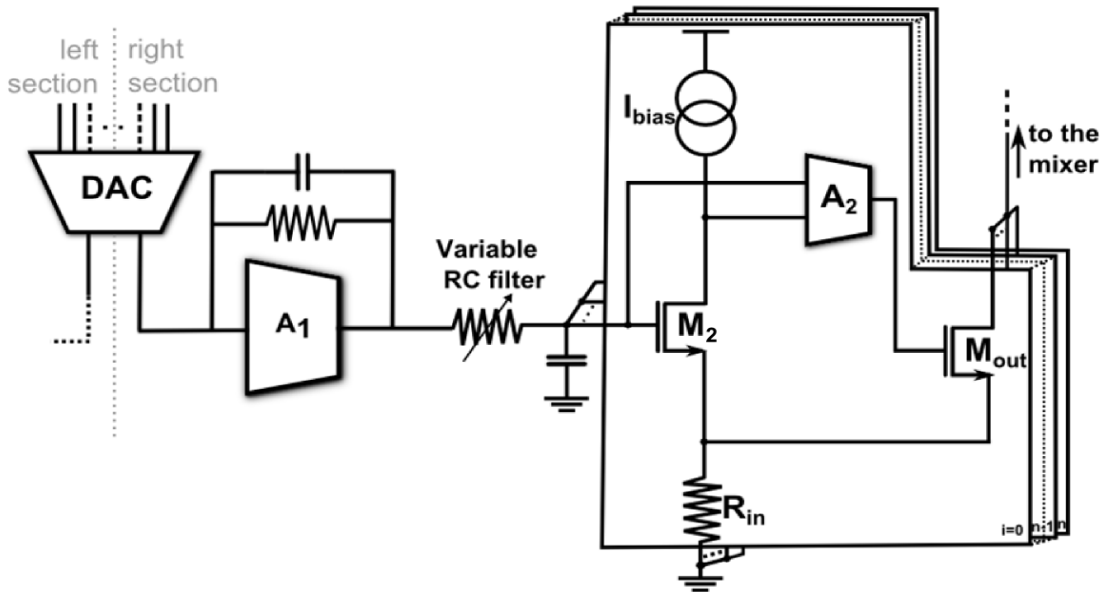


Figure 4.5: Schematic of the transmitter with a second order filtering stage

Due to the EVM possible issue, an equalization of signal can be done by acting on the code that drives the DAC compensating in this way the droop due to the filtering stage.

4.3 CLASS B DAC introduction

4.3.1 DAC replicas

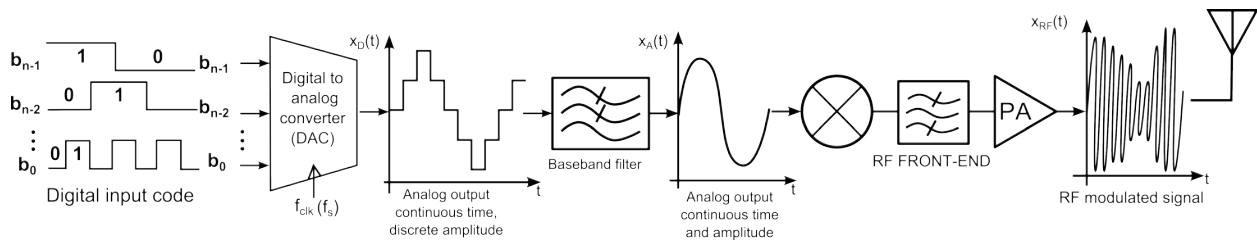


Figure 4.6: Diagram of the entire transmitter chain, from the digital DAC code to the analog signal sent to the antenna

The analog section of a transceiver is the part that interfaces the signal with the digital world. The baseband processing of the signal is instead entirely digital. Hence, an Analog to Digital Converter (ADC) is necessary in the receiver chain while a Digital to Analog Converter (DAC) is the interface of the transmitter chain as it's shown in Fig. 4.6.

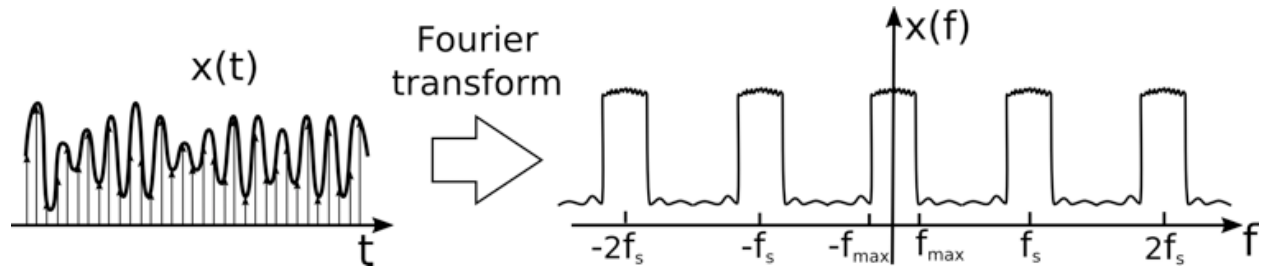


Figure 4.7: Signal $x(t)$ sampled in the time domain and his spectrum

In the transmitter the band limited signal $x(t)$ [21] with spectral components beyond a frequency f_{max} equal to zero like the one in Figure 4.7.

The signal can be completely reconstructed from a set of uniformly spaced discrete-time samples, given from the digital baseband to the DAC, if the samples are taken with a sampling rate f_s :

$$f_s \geq 2f_{max} \quad (32)$$

This is known as the uniform sampling theorem and the sampling rate $f_s = f_{max}$ is called the Nyquist rate.

Suppose an analog waveform $x(t)$ with a Fourier Transform $X(f)$ equal to zero for $|f| > f_{max}$ and sampled in the time domain. Ideally, sampling $x(t)$ means taking the product of $x(t)$ with aperiodic train of impulses $x_\delta(t)$ defined as:

$$x_\delta(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT_s) \quad (33)$$

where T_s is the sampling period and $\delta(t)$ is the Dirac delta function.

In Figure 4.7 is reported the sampled version of $x(t)$ denoted as $x_s(t)$. It can be expressed as:

$$x_s(t) = x(t)x_\delta(t) = \sum_{n=-\infty}^{+\infty} x(t)\delta(t - nT_s) = \sum_{n=-\infty}^{+\infty} x(nT_s)\delta(t - nT_s) \quad (34)$$

The signal spectrum of $x_s(t)$ can be obtained by the equation above. In fact, using convolution, the Fourier transform of the sampled signal $X_s(f)$ can be rewritten as the convolution of $X_f(f)$ and the Fourier transform $x_\delta(f)$ ($X_\delta(f)$):

$$X_s(f) = X(f)X_\delta(f) = X(f) * \left[\frac{1}{T_s} \sum_{n=-\infty}^{+\infty} \delta(f - nf_s) \right] = \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} X(f - nf_s) \quad (35)$$

using the frequency domain form of the impulse train:

$$X_\delta(f) = \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} \delta(f - nf_s) \quad (36)$$

The spectrum $X_s(f)$ of $x_s(t)$ is exactly the same as X_f of the original signal $x(t)$, to within a constant factor ($1/T_s$). Moreover the spectrum repeats itself in frequency every f_s as despised in Figure 4.7.

A real DAC is not able to provide ideal impulses at his output. In fact, his output can be seen as an impulse followed by a sample and hold that keeps the value of the impulse for a period of T_s . The mathematical representation is the convolution of the sampled impulse train $x(t)x_\delta(t)$ with a unity amplitude rectangular pulse $p(t)$ of width T_s :

$$x_s(t) = p(t) * [x(t) \sum_{n=-\infty}^{+\infty} \delta(t - nT_s)] \quad (37)$$

This results in the function represented in Equation 37. His Fourier transform is the product of the Fourier Transform $P(f)$ of the rectangular pulse and the spectrum of the impulse sampled sequence:

$$X_s(f) = P(f) \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} X(f - nf_s) \quad (38)$$

where $P(f) = T_s \text{sinc}(fT_s)$. Therefore, considering $P(f)$, it's easy to understand that the signal replicas at multiples of sampling frequencies are now filtrated trough a sinc function.

However the filtering is not sufficient since the replicas could fall, when transmitted, in other bandwidth where other standards are or where the receiver (integrated in the same chip) is working. Of course, increasing the DAC sampling rate f_s would push the replicas at higher frequency, but at power consumption costs.

Hence, the usual strategy in the transmitter chains is to insert a filtering block (usually with higher order) that eliminates the DAC replicas and it is traditionally placed right after the converter.

The design of an extremely high SNDR and DR base-band requires an accurate work of reduction of all the possible noise sources, both dominants but also non-dominant ones, to achieve the best possible noise figure performance if the block is used in a complete transmission chain (or the lowest absolute noise value if the block is assumed as a stand-alone one).

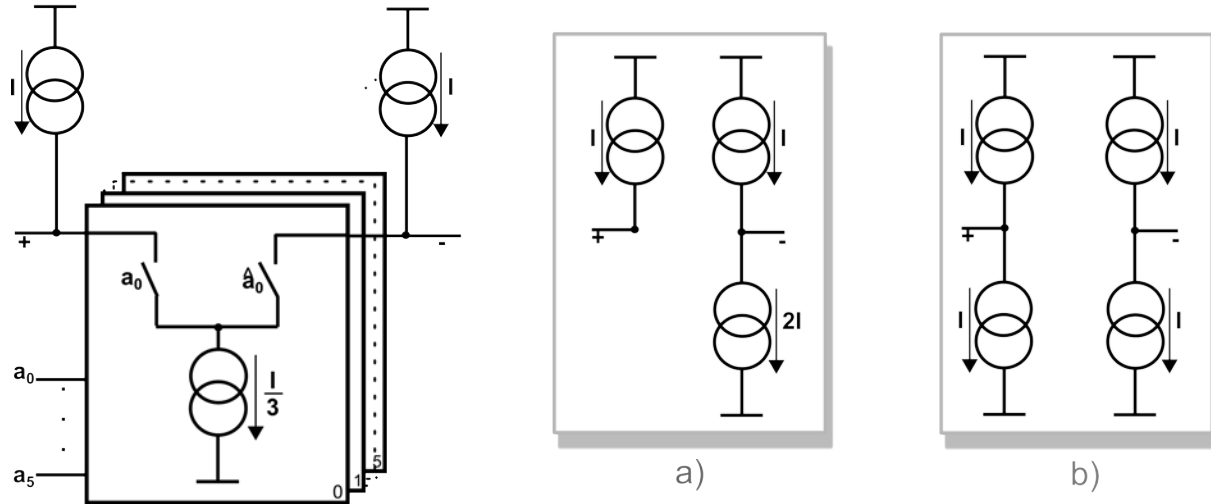


Fig 4.8: Classical class-A DAC architecture. a) Full scale current signal Input code $a_0, \dots, a_5 = 111111$; $I_{OUT} = +I$ b) Zero level current signal Input code $a_0, \dots, a_5 = 000111$; $I_{OUT} = 0$

Also the DAC is a source of thermal noise, basically the noise sources are the current generators. For a current-steering architecture, the noise of each cell of the DAC is given by:

$$i_{noise_cell}^2 = 4kTg_{mDAC} \left(2\gamma \frac{V_{LSB}}{V_{OV}} \right) \quad (39)$$

where V_{OV} is the overdrive voltage of the MOS transistor implementing the cell current generator and V_{LSB} is the voltage at the input of the quantizer that corresponds to one LSB.

In the following, two different DAC topologies are compared [Figs. 4.8 and 4.9] both based on a six-level thermometric architecture (just for simplicity). In both cases, there are seven possible output levels ranging from $+I$ to $-I$ with a minimum step of $I/3$.

The first DAC is operated in class A and is shown in Fig. 4.8 for the fully differential case. Each output signal is the difference between a fixed current supplied from the positive rail (equal to full scale) and that of six current sources (injected into the negative rail) that can be switched to either one of the output nodes. The elementary DAC cell is a differential pair connected to the positive or to the negative output driven by one bit of the code. Fig. 4.8(a) shows how the positive full-scale output current ($+I$, $-I$) is obtained for the DAC code $a_0, \dots, a_5 = 111111$, while Fig. 4.8(b) shows how the zero output current is obtained for the code $a_0, \dots, a_5 = 000111$. The latter case can be representative of the sensitivity condition.

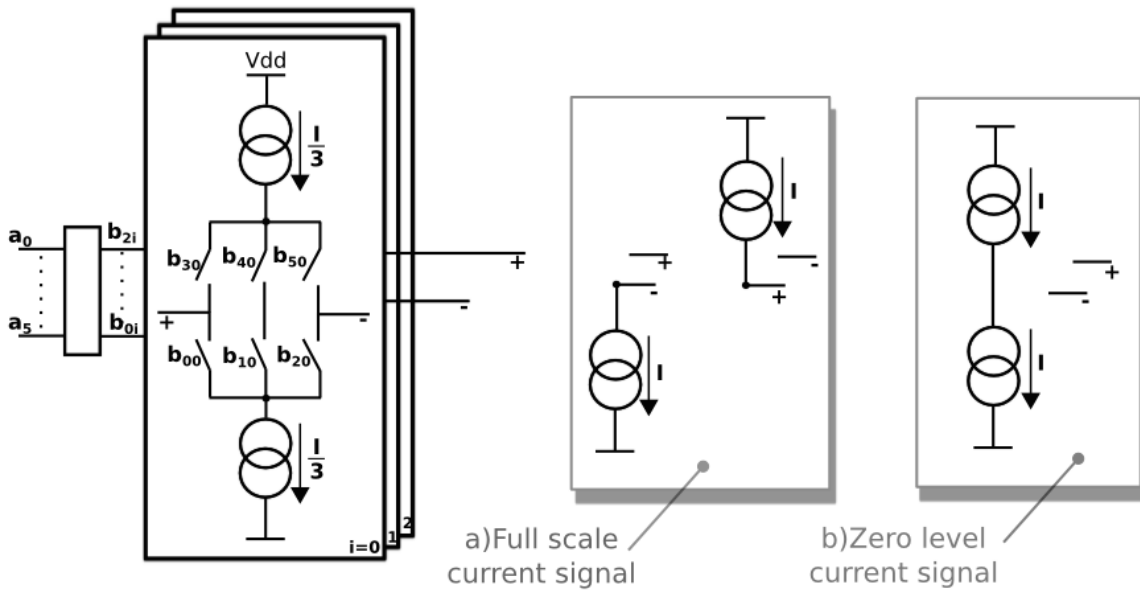


Fig 4.9: Classical class-B DAC architecture. a) Input code $a_0, \dots, a_5 = 111111$; $I_{OUT} = +I$ b) Input code $a_0, \dots, a_5 = 000111$; $I_{OUT} = 0$

At sensitivity, in fact, a very small signal is present at the input of the quantizer (with its added noise), and statistically, for a high percentage of time, only the middle code drives the DAC input.

The second topology, showed in Figure 4.9, is a push-pull structure [22] that injects or absorbs current without any fixed bias connected directly to the output. The proposed class-B concept uses three-way current-switching cells at the cost of a higher number of switches and more complexity in the driving logic. The controls b_0 – b_5 of each elementary cell are obtained from a_0 – a_5 through a simple digital logic.

The elementary cell uses four switches to send the current taken from the positive rail either to the positive or to the negative output and viceversa for the current taken from the negative rail. In addition, two extra switches (connected to a fixed node) are added, making it possible to switch off

the cell while maintaining the current generators always in the ON state. Not only the cells pull and push the current but also they can be put in a rest condition. For the $I/3$ signal level, only one cell is driven in ON state. The $2I/3$ signal level is realized with two cells in the ON state, while the full-scale current requires all the three cells in ON state. The positive full-scale ($+I$, $-I$) and the zero current levels are shown in Fig. 4.9(a) and 4.9(b), respectively. In the latter case, all cells are switched off from the output nodes, therefore contributing zero noise.

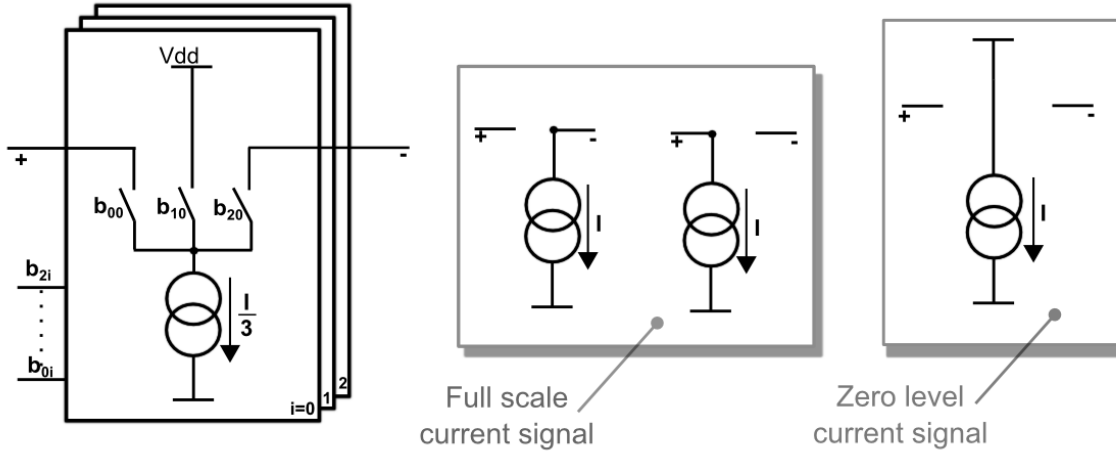


Fig 4.10: Classical class-B DAC n-only topology architecture with full scale current signal and zero level current signal configuration

In a traditional class A DAC approach, the DAC noise depends on the DAC full-scale current, which is in turn given by the level of the interferers that have to be handled as input scenario, by the baseband. This situation is not modified even in the absence of the blockers when the amount of the full scale is used in a very limited percentage, to handle the input signals. The class B DAC manages in breaking the dependence of the injected noise on the full-scale current in the no-interferer condition.

In the new structure the DAC proposed is based on an n-type (sink only) topology that feeds directly the two virtual grounds of the pseudo-differential active first order filter.

It uses a segmented architecture with the 4 most significant bits thermometric and the 6 less significant bits binary. A total of 26 switchable current sources are required whose conceptual structure is shown in Fig. 4.10. A generic current source (binary or thermometric) can be diverted either to the positive or negative filter input or to the supply. An almost negligible extra complexity is required by the triple switch compared with a class A DAC but the total area of the current sources is halved also compared to Fig.4.9 case.

To generate the current signal a class B DAC is used [20]-[22] resulting in reduced noise emission and power saving. In fact a class B DAC requires less power, directly produces the required signal for the mixer and has a lower noise emission especially for signals with a high peak to average power

ratio (PAPR) as in LTE. This avoids the need for a dedicated class A/B signal conditioner in front of the mixer thereby saving power, eliminating a significant noise contributor and reducing distortion compared to the solution proposed in [13].

With large interferers, all the DAC cells are in the ON state and contribute to the overall noise. In this situation, however, also, the noise requirements are less critical. When the input signal decreases, less current is required, and less cells are turned on. In the limit of a very small input signal (sensitivity test), almost zero noise is injected by the DAC.

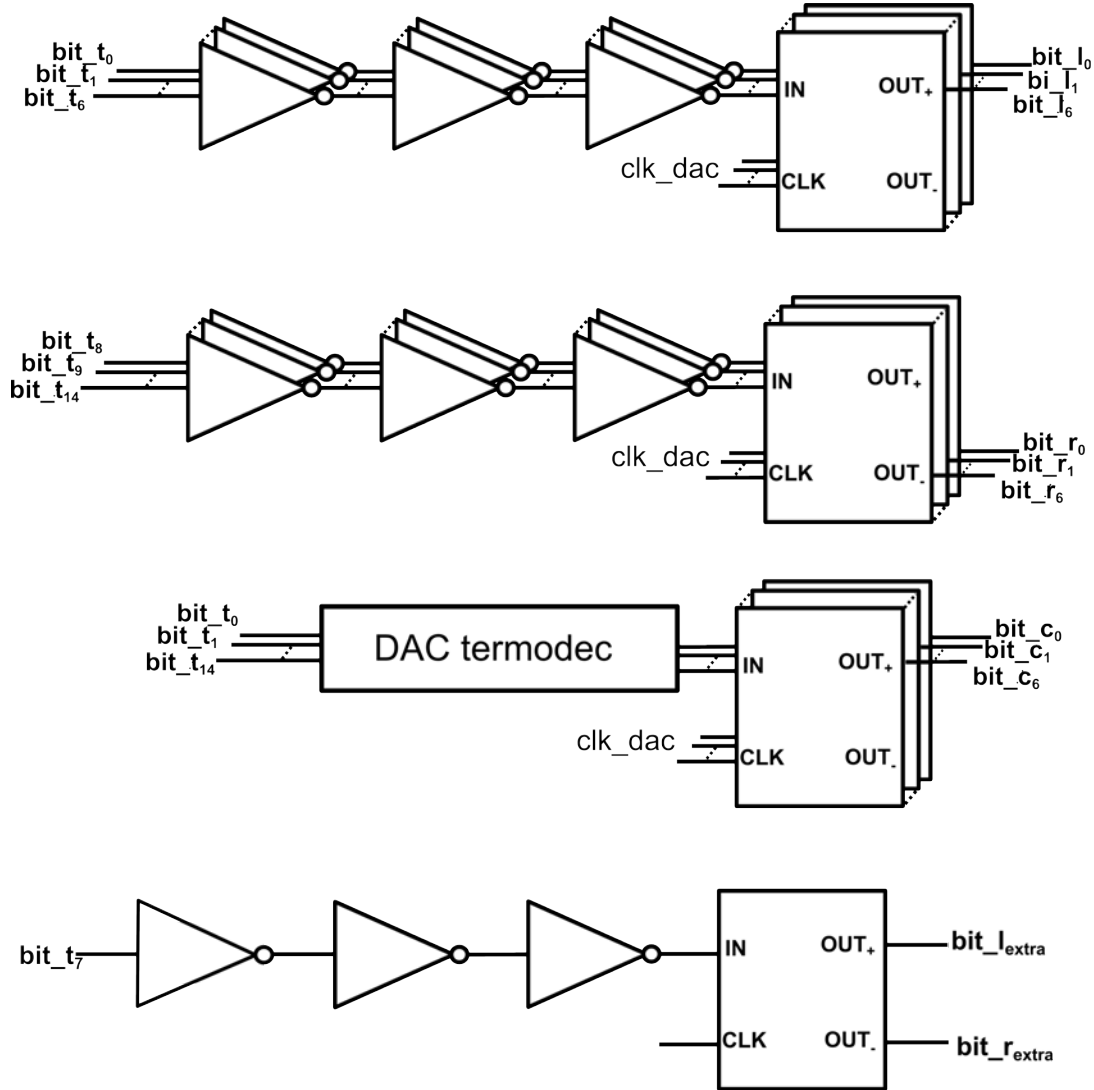


Figure 4.11 : Schematic of the digital processing of the DAC thermometric code to change the class A signal into a class B signal

The DAC structure is recreated from the DAC proposed in the previous chapter. Therefore, in order to reuse the same code, there is the need of a digital re-elaboration in order to change the driving code from a class A to a class B code. In fact the original code goes from 0 (the minimum of a full scale sinusoide) going to 512 (the zero level current code) ending with 1024 (the positive full scale signal).

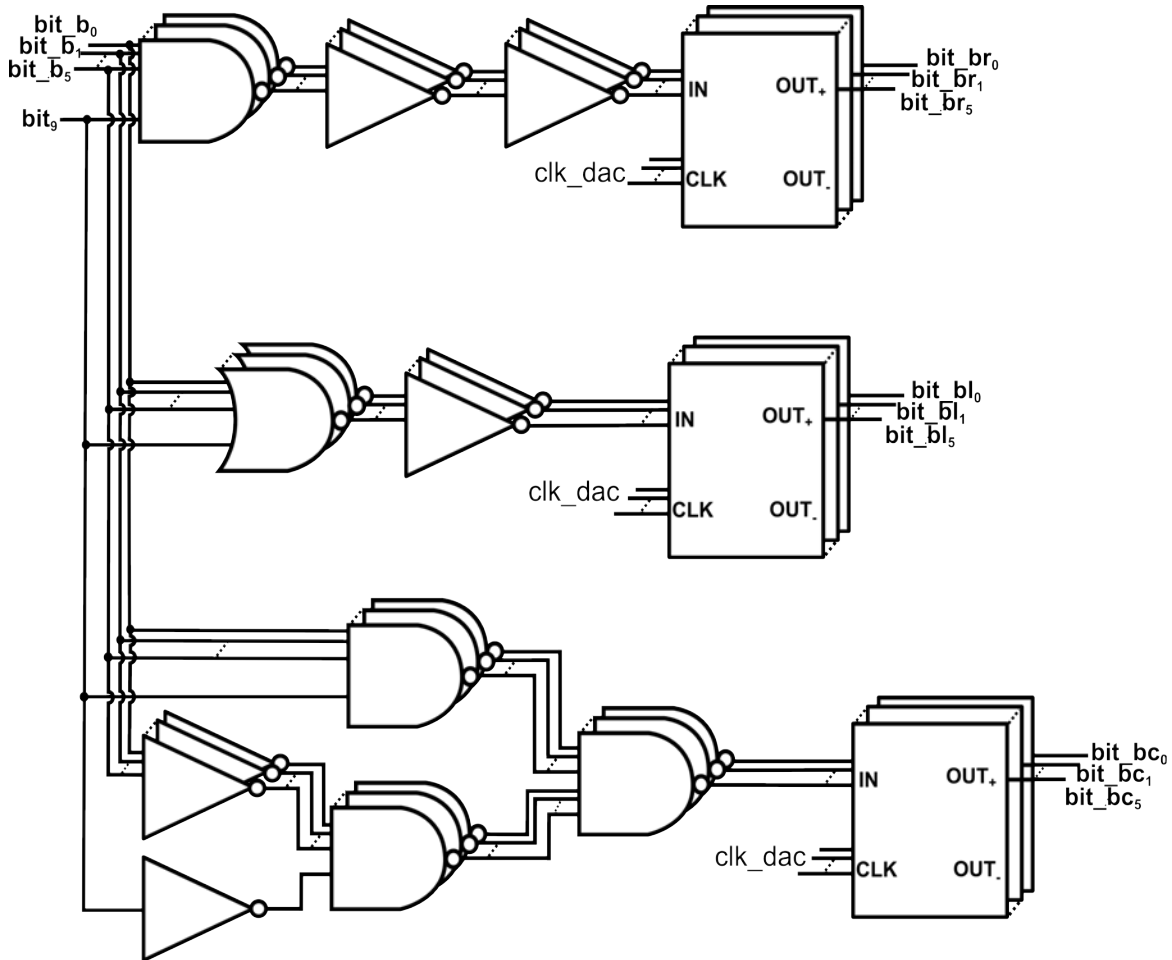


Figure 4.12 : Schematic of the digital processing of the DAC binary code to change the class A signal into a class B signal

Moreover the new DAC structure implements a third switch so to create the new logic there is also this aspect to take into account. For what concerns the thermometric code (Figure 4.11) the first seven bits are used to drive the left switch while the 8th bit (the middle one) is the so called “special

bit". This one is used to drive two switches that divert the current (equal to half LSB current) needed to adjust the output waveform and also its linearity. In this case the third switch is not present therefore the current equal to half LSB is always present in the right or left side.

The thermometric bits from the 9th to the 15th are used to drive the right switches in complementary way in comparison to the left switches but with equal delays. All the thermometric bits are specifically combined in order to properly drive the central switches.

A similar approach is used for the binary code (Figure 4.12) but in this case the special bit is not present. Moreover in this case the approach to create the new code is to compare it with the last bit since the last bit is the one related to the middle of the waveform. So if the 10th bit is 1 the waveform is in the positive side, while if it's 0 the waveform is in the lower side. From that is possible to recreate the absolute value of the code and than split it to the positive path or negative path for the I and Q sides.

Of course for the implementation of the logic the delay time of the inverters, NAND and NOR has been taken into account in order to have the same delay for every path maximizing the linearity of the output signal. The realization of the DAC was completed by adding the third switch and maintaining the same dimentions of the current sources.

4.4 First OTA Structure

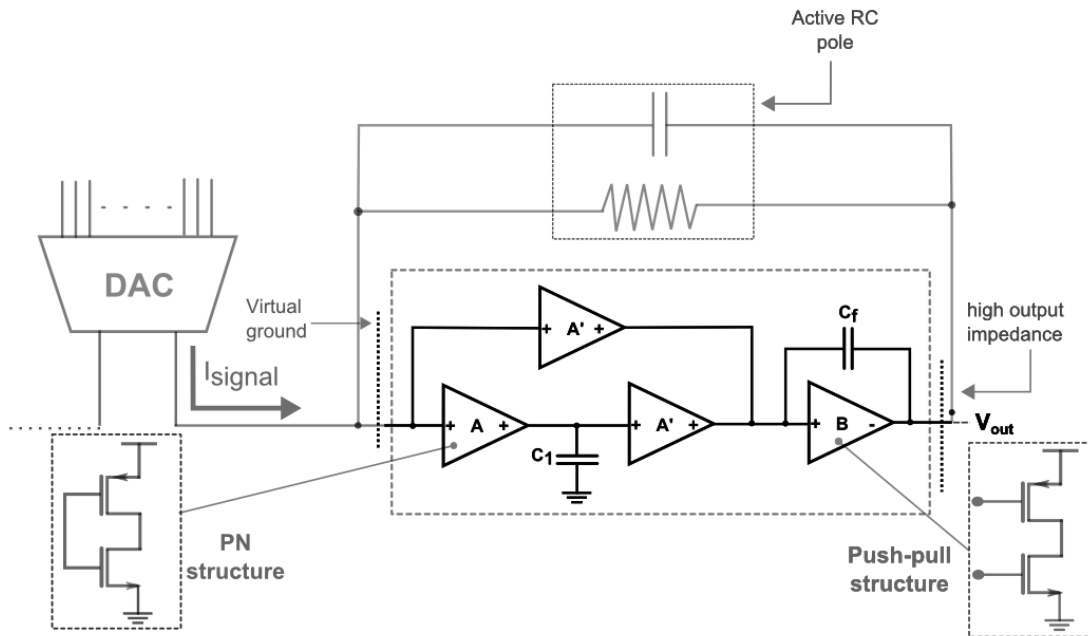


Figure 4.13: Configuration of the first OTA structure with the PN input structure and the push-pull output structure

Linear CMOS techniques have achieved significant progress over the last five years to provide high-performance low-power analog building blocks like operational amplifiers (op amp), comparators, buffers, etc. These circuits have demonstrated comparable performance to their bipolar counterparts at much less silicon area and power dissipation, thus enabling single chip implementations of complex filtering functions, A/D and D/A conversions with quite stringent specification. Due to relatively simple circuit configurations and flexibility of design, CMOS technology has an edge over NMOS technology and is gaining rapid acceptance as the future technology for linear analog integrated circuits, especially in the telecommunication field. The most important building block in any analog IC is the op amp of which numerous implementations have been reported in both the technologies.

The active filter must drive the following passive filter with very low impedance over the bandwidth of interest to ensure good linearity and accurate frequency response. Furthermore its input noise should be small since it reaches the output unfiltered. The structure of the first OTA is proposed in Fig. 4.14.

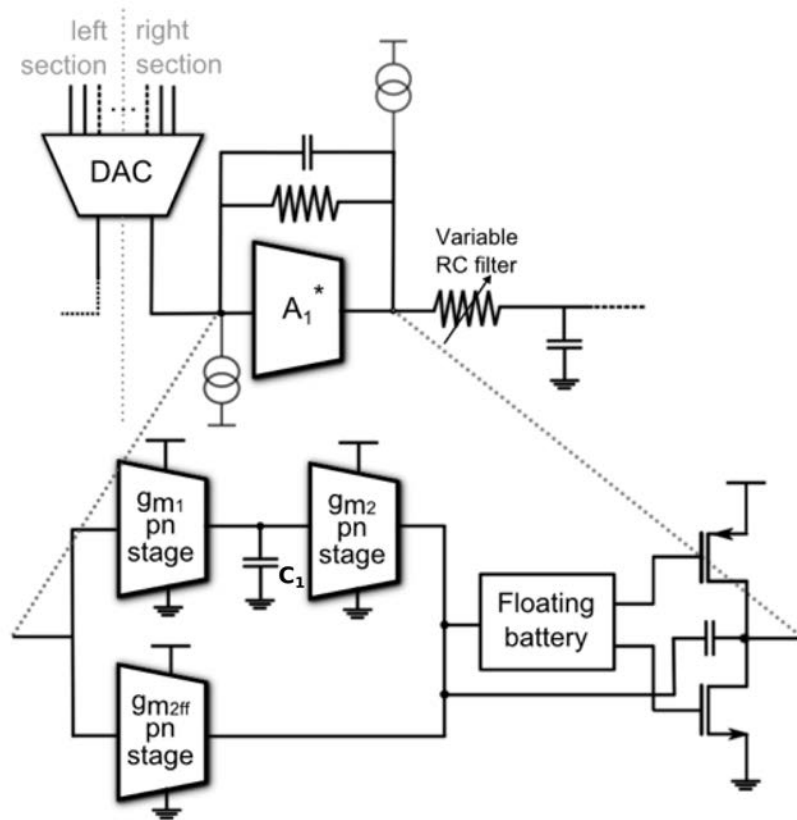


Figure 4.14: First OTA structure

The single ended OTA uses a three stage feed-forward topology. The architecture of the first OTA is made of two paths:

- The main path creates a high gain for low frequency
- The feed forward path acts at high frequency when the gain of the main path starts to get lower

This gives a much larger effective bandwidth thanks to the 40dB/decade in band slope in its frequency response. In addition, the OTA uses a novel input structure that looks like a simple common source n-only stage at low frequency and becomes a complementary p-n structure at high frequency. This allows to lower the noise (by a factor of two) where it counts i.e. at the duplexer frequency for a given power consumption. Finally the OTA uses a push pull (class A/B) output stage to drive the large capacitive load caused by the passive filter in a linear and efficient way.

The variable gain is implemented changing the mirror factor and the feedback resistance.

The input virtual ground is used to inject a current signal coming from the DAC but also to perform a linear I-V conversion.

A possible way to decrease the input slew-rate caused by the large voltage swing at the gate of the output transistors is to increase the gain between the virtual ground and the output in the frequency range of the signal thereby reducing any additional distortion caused by slewing. One way to achieve this goal is to implement an amplifier with an open loop frequency response that displays a slope of 40dB per decade while approaching the unity gain frequency as shown in Fig.4.15.

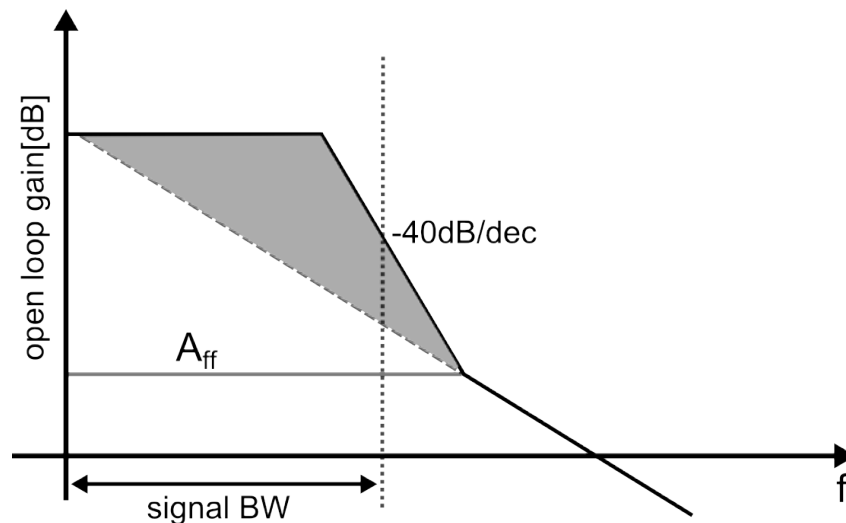


Figure 4.15: Frequency response of the first OTA

This can be achieved using a tree stage amplifier with feed forward path as shown in Fig.4.14. In this way the three-stage amplifier (main path) is no longer nested Miller compensated. As a consequence the pole at the output of the first stage is moved to a much higher frequency since C_l no longer sees any Miller multiplication effect. Of course, the frequency response associated with the main amplifier is very close to be unstable (in practice it would be so) because at the unity gain bandwidth the slope is -40dB per decade. However stability is ensured thanks to the auxiliary gain path g_{mff} placed in parallel with the input stage. The zero produced by the feed-forward path when placed sufficiently before the unity gain frequency (typically at a ω between $1/3$ and $1/2 \omega$ -unity) restores the -20dB per decade slope at the crossing point, and thus stability is guaranteed.

The value of the cut-off frequency of both filters can be programmed to satisfy all standards supported (2, 3 and 4G). The filtered signal directly drives the gate of the first MOS of the output closed-loop stage that feeds the mixer as shown in figure 4.16.

A traditional approach for the OTA is the dominant pole solution. Since the maximum LTE signal has a bandwidth of about 10MHz, if we want a gain of at least 40dB at 10MHz the needed bandwidth for a single pole OTA should be about 1GHz. This actually is not possible due to the parasitic capacitance and resistance. Therefore, in order to achieve high gain for relatively high frequency with a good bandwidth and phase margin a multipath structure is preferred.

The frequency response is shown in Figure 4.15. The main path creates high gain at low frequency, the feed forward path acts at higher frequency when the gain of the main path starts to get lower. Two low frequency poles allow the frequency response to get lower with a slope of 40dB/dec, at higher frequencies the transfer function shows a zero that enables the increase of bandwidth and phase margin. Since the structure presents a single ended input and output therefore the system is stable only in feedback configuration.

As it can be seen in Fig. 4.14 two stages, g_{m1} and g_{m2} , form the main path, while g_{m2ff} creates the feed forward path. The last part with the floating battery and the push-pull stage are common for both the paths. For simplicity we can call the push-pull structure as g_{m3} . C_1 is the capacitor between g_{m1} and g_{m2} while C is the capacitor in feedback over g_{m3} . The low frequency path $H_{LF}(s)$ and the high frequency path $H_{HF}(s)$ are defined as:

$$H_{LF}(s) = \left(\frac{g_{m1}R_1}{1+sC_1R_1} \right) \left(\frac{g_{m2}R}{1+sRC(1+g_{m3}R_3)} \right) (g_{m3}R_3) \quad (40)$$

$$H_{HF}(s) = \left(\frac{g_{m2ff}R}{1+sRC(1+g_{m3}R_3)} \right) (g_{m3}R_3) \quad (41)$$

where R_1 is the output impedance of g_{m1} , R is the equivalent output impedance of g_{m2} and g_{m2ff} , R_3 the out of the output stage. So considering the total transfer function $H(s) = H_{LF}(s) + H_{HF}(s)$ and approximating $1 + g_{m4}R_4 \approx g_{m4}R_4$ we have:

$$H(s) = g_{m3}R_3 \left(\frac{g_{m1}R_1}{1 + sC_1R_1} \right) \left(\frac{g_{m2}R}{1 + sRC(1 + g_{m3}R_3)} + \left(\frac{g_{m2ff}R}{1 + sRC(1 + g_{m3}R_3)} \right) \right)$$

$$\approx \frac{g_{m1}g_{m2}RR_1 + g_{m2ff}R}{(1 + sC_1R_1)(1 + sRC(1 + g_{m3}R_3))} \left(1 + s \frac{g_{m2ff}g_{m2ff}}{g_{m1}R_1g_{m2} + g_{m2ff}} \right) \quad (42)$$

If $g_{m1}R_1g_{m2} \gg g_{m2ff}$ we have

$$p_1 = -\frac{1}{C_1R_1} \quad p_2 = -\frac{1}{CRg_{m3}R_3} \quad z = -\frac{g_{m1}g_{m2}}{g_{m2ff}C_1}$$

For what it concerns the DC working point is defined only by the input stage of the OTA since the DAC does not provide any. In particular this DC voltage is the one that provides the matching between the M_2 and R_{out} (Fig.4.16) branch and the input stage of the OTA (M_1 R_{in}). To limit the noise of the first stage, R_{in} is eliminated and the voltage drop over the R_{in} is recreated trough the feedback resistor and two current generators on his sides.

However the noise of the first stage OTA is still an issue since it goes directly to the output and it must be minimized in order to make the feedback resistor the dominant contributor of the noise of the OTA (Fig. 4.16) the DC current I_{dc1} (Fig.4.17) is about 250uA so considering 100mV of overdrive we have $g_m \approx 2I_{bias}/V_{ov} \approx 5mS$ while for I_{dc2} and I_{dc3} the current consumption is 50uA with the dimensions of the transistor properly scaled.

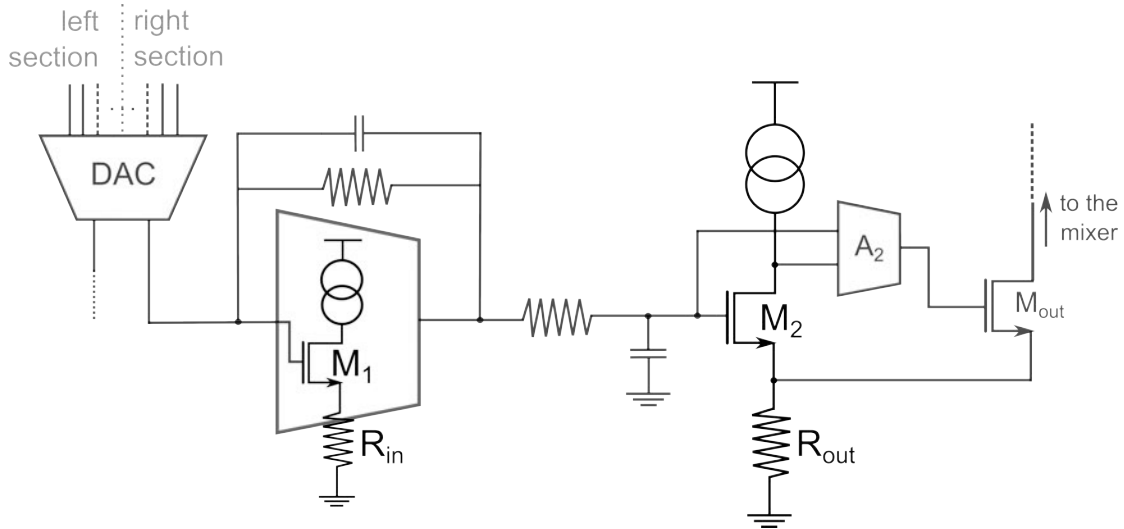


Figure 4.16: Bias output reference for the first OTA

The input transistor of the OTA has to match his W/L and I_{bias} (possibly scaled) with M2 to provide the correct matching. The entire schematic of the first OTA is shown in Fig.4.17 while the Figure 4.18 shows the current reference used to create the matching with the floating battery and the output push pull stage.

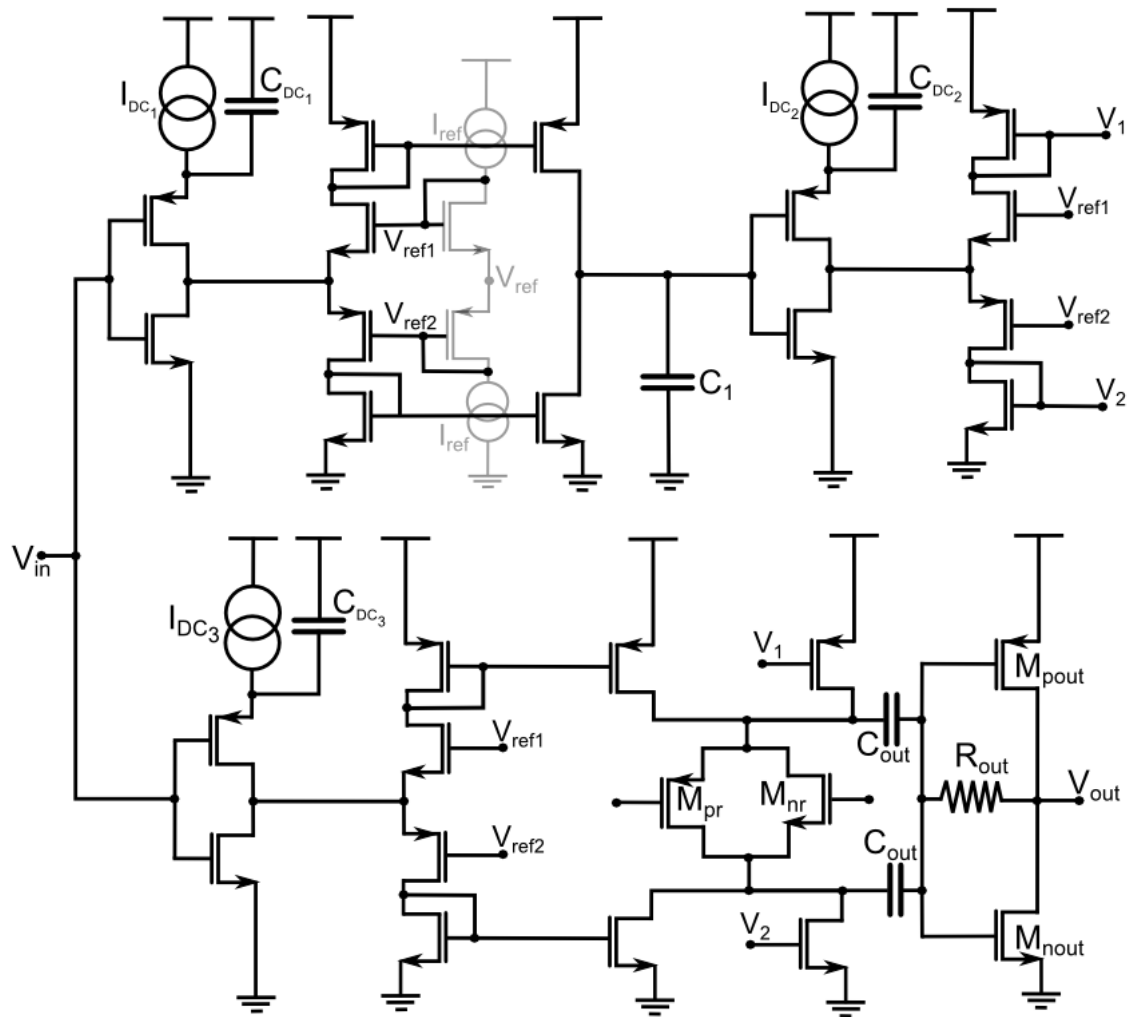


Figure 4.17: Schematic of the first OTA

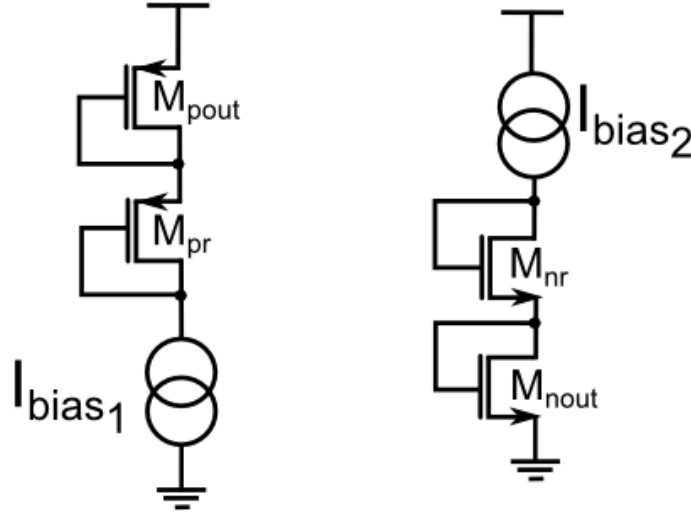


Figure 4.18: Bias output reference for the first OTA

4.5 Output closed-loop stage

The last stage of the base band is a loop made up by a first MOS (M_2) that acts like a fixed battery, a resistance R_{out} that creates the V-I conversion, a second MOS (M_{out}) that acts like a regulated-cascode and an OTA connected as shown in Fig.4.19.

The OTA (A_2) has three effects. First, it forces M_1 to always remain in saturation while carrying a constant current I_{bias} transferring the input signal to the degeneration resistance with a constant level shift (equal to the V_{GS}). Second, it forces M_2 to absorb the entire signal current flowing in R_{out} and deliver it to the power mixer. Third it increases the output impedance of the circuit making M_2 a regulated cascode. The OTA has two in band poles-zero doublets to enhance its effective bandwidth while preserving good phase margin. The baseband voltage signal is converted to current by resistor R_{out} . Changing the value of R_D the output power can be programmed in a very linear fashion. Accurate gain control over a 48dB range is realized by programming in 6dB steps.

The closed loop architecture has therefore a much more linear V/I transfer function compared to a simple current mirror [12] where voltage compression and expansion occurs. As a consequence a very narrow passive filter can be used to strongly filter out the noise of the previous stages, without degrading linearity (the transfer function droop is compensated in the digital domain). This is key to meet the required out of band noise emission especially for narrow TX to RX band separation.

The output of the closed-loop stage provides a class A/B current for the power mixer. The result is a regulated cascode configuration that ensures excellent linearity and provides accurate gain programmability.

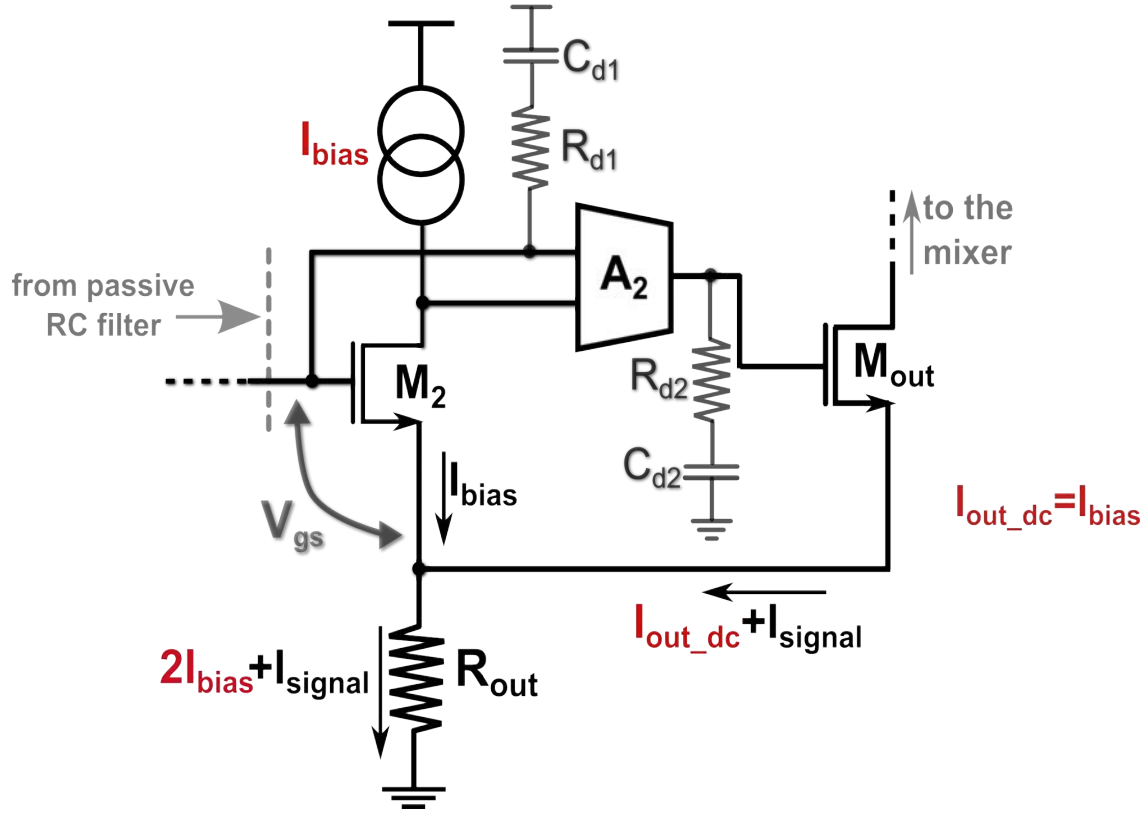


Figure 4.19: Schematic of the output baseband loop

The mixer is the same as the one used in [12]-[13] i.e. a Gilbert like cell where, however, the switching devices are operated in the linear region. One out of several cascode devices, at the output of the mixer, can be selected to send the up-converted signal to the proper balun (depending on the desired band). A sliced architecture is used for the entire output branch (degeneration resistance, output MOS, OTA, mixer and balun selector) made up of 20 identical unitary cells that can be turn on or off one at the time to control the emitted power in a very linear way.

4.6 Pole-zero doublets compensation

The output OTA schematic is designed specifically to be stable with the different current configurations and number of stages. To do so an OTA with two poles-zero doublets is designed. The RC zero depends on the number of stages. This is done in order to maintain stable the loop even with low number of stages, the most critical situation. The baseband loop it's useful to maintain high linearity before the mixer. However this structure is challenging for the stability issue. In fact changing the mirror ratio also the stability conditions can change in particular this aspect is trivial for low mirror ratio where the phase margin stats to decrease.

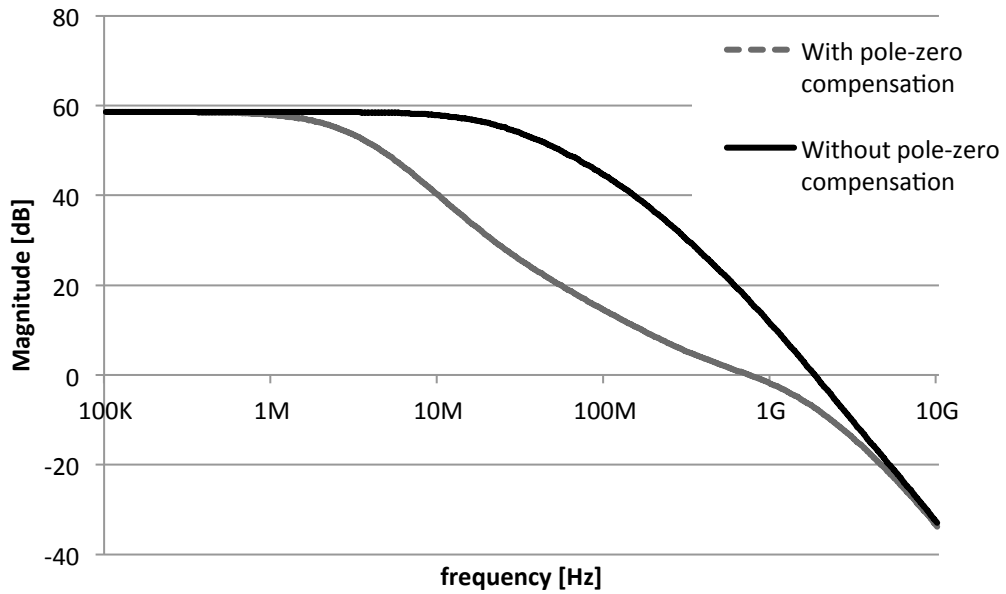


Figure 4.20: Magnitude and phase response for the output OTA

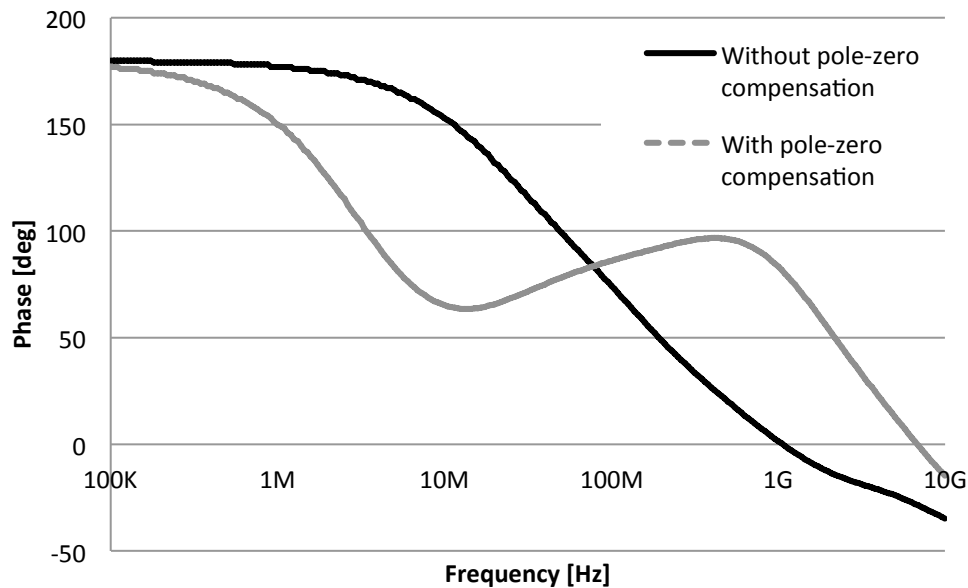


Figure 4.21: Magnitude and phase response for the output OTA

The second OTA has to be designed with high Gain/Bandwidth product (GBW) in order to recycle the noise into the loop and not bring it up to the active mixer and then to the output. At the same

[illegible]

The solution proposed implements a pole-zero compensation in order to achieve quite high bandwidth and increase the phase margin with relatively low power consumption and a simple two stage op amp.

The principle of the pole-zero compensation is relatively simple: the presence of a zero followed by a second pole enable to increase the bandwidth without sacrificing the phase margin and without introduce any additional stages. This structure fits perfectly the need of the baseband loop of relative high bandwidth and phase margin with low power dissipation. The only aspect to take into account is that the bandwidth slightly changes with the mirror ratio, therefore a trimming of the frequency of the zero is needed in order to maintain a good phase margin as it's shown in Figure 4.22 while the magnitude and phase of the transfer function before and after the pole-zero compensation are shown in Fig 4.20 and 4.21 respectively.

4.7 Up-conversion Stage

The structure of the upconversion stage is unchanged from the previous structure described in chapter 3 and is shown in Fig. 4.23.

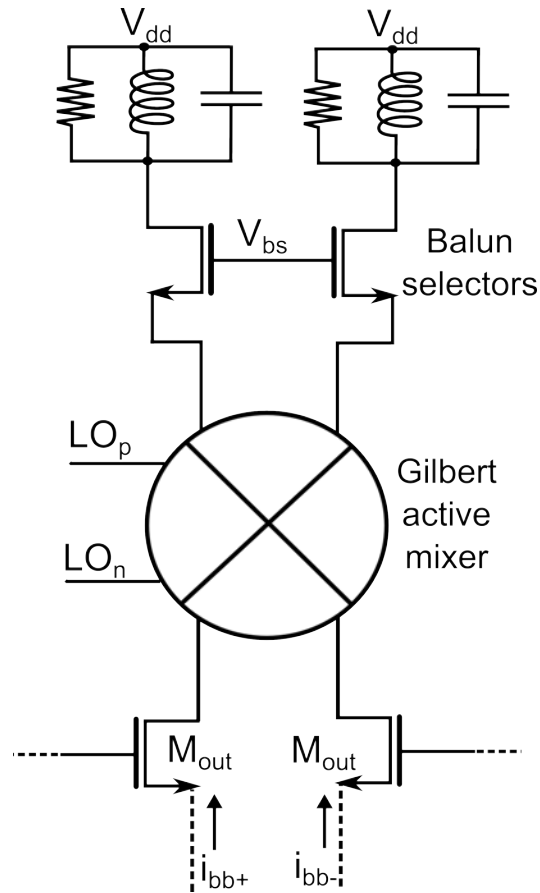


Figure 4.23: up-conversion stage

The upconversion stage presents the classical gilbert cell driven by the LO with 50% of duty cycle, after the mixer, the balun selectors are present in order to drive the signal to the proper balun. The balun selectors and the mos of the gilbert cell are scaled in proportion to the mirror ratio that changes also the dimensions of the the baseband loop MOS (M_{out}) and the resistor.

The frequency of the LO can be changed in order to cover all the 3G, 4G frequency bands.

Five baluns are present in order to cover all the different transmission bands.

4.8 Out-of-band noise performances

One of the most interesting results that this circuit can achieve is the low out-of-band noise even at low frequency offset. This is possible thanks to the high linearity of the baseband that allows the reduction of the cut-off frequency very close to signal bandwidth edge.

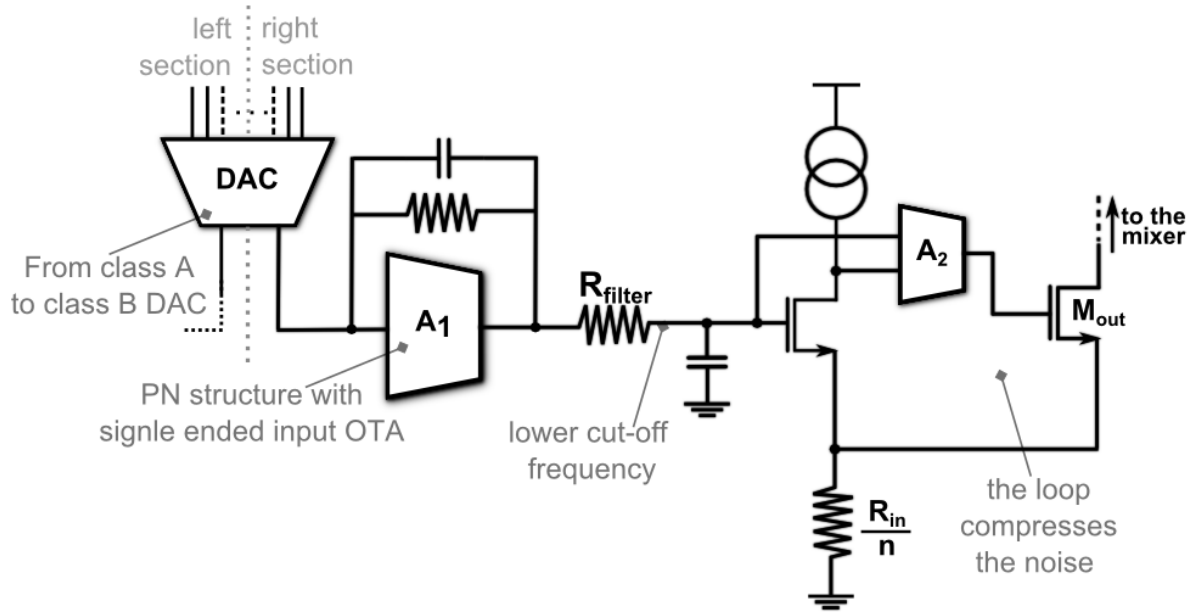


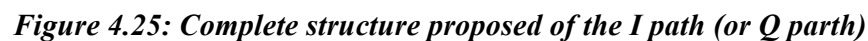
Figure 4.24: Base band stage with all the noise contributors

The plot shows the out-of-band noise emission the SNR reached is about 160.5 dBm/Hz

This paragraph reports the noise contributors of the baseband chain and the reason why this structure is able to inject less noise in comparison to the state of the art , also reported in Figure 4.24:

- The DAC goes from class A to class B
- Thanks to high linearity the filter cut-off frequency can be lowered in a position very close to the edge of the signal bandwidth in this way given a certain filtering order the out of band filtering is more effective. For the LTE10 the cut-off frequency is about 6MHz and 12MHz for the LTE20.
- The structure of the first OTA is specifically designed in order to reduce the out-of band noise emission with a PN structure with single ended input for the first OTA. Moreover the push pull structure of his last stage allows the possibility to increase the value of the capacitor.

- #### 4.9 Simulation Overall structure and reconfigurability



Low power-noise emission LTE class A/B transmitters – Chapter 4

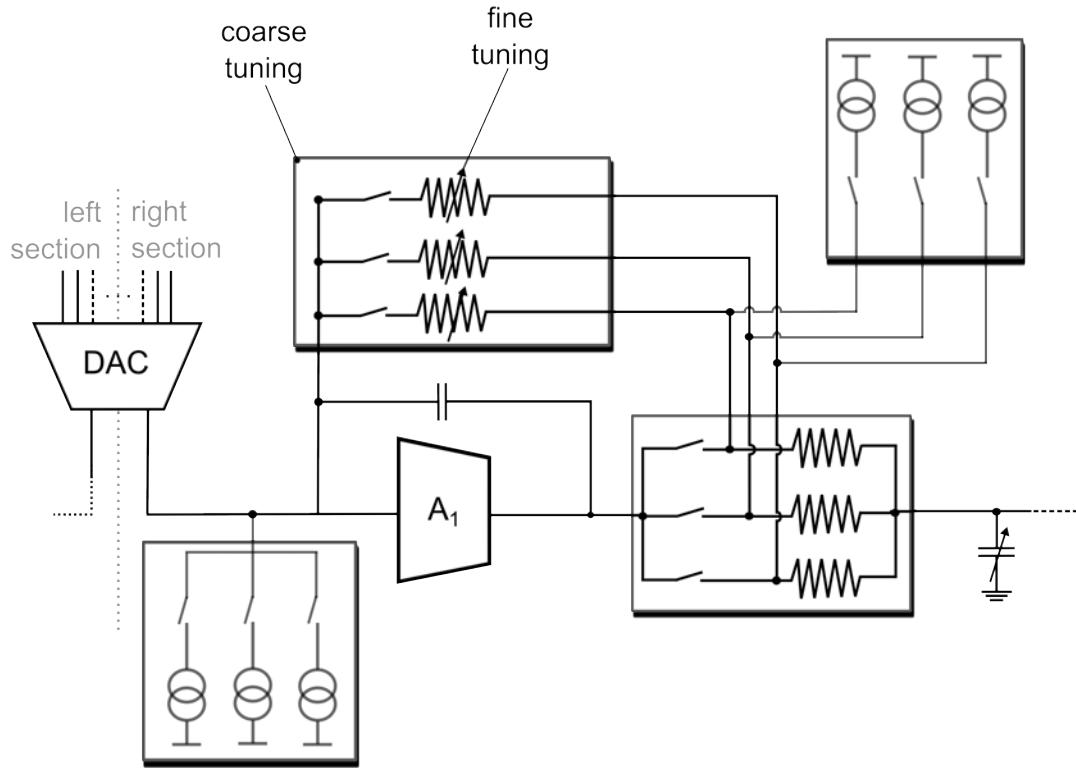


Figure 4.26: Reconfigurability of the cut-off frequency of the filter

4.11 Simulation results

The plots (Fig.4.27-4.28) show the comparison with the previous structure. The current consumption (Fig. 4.27) of the old one is reported for the high gain configuration and low gain configuration, in the new transmitter proposed, instead, high power configuration and low power configuration are not presents, and the current consumption varies only with the mirror ration. While in comparison to the high gain configuration the new solution is always winning for the low power configuration comparison an elaborated discussion is needed: although at high power the new transmitter uses more current, below 0dBm (where consumption is crucial) the current saving is relevant. The

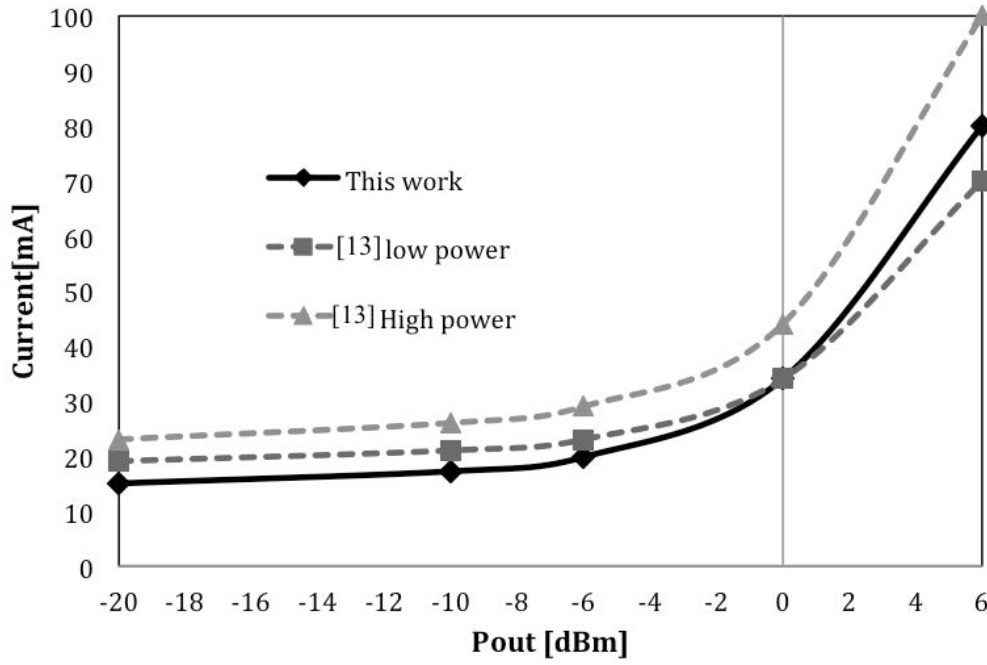


Figure 4.27: Graphic of the current consumption vs output power and comparison with the state-of-the-art

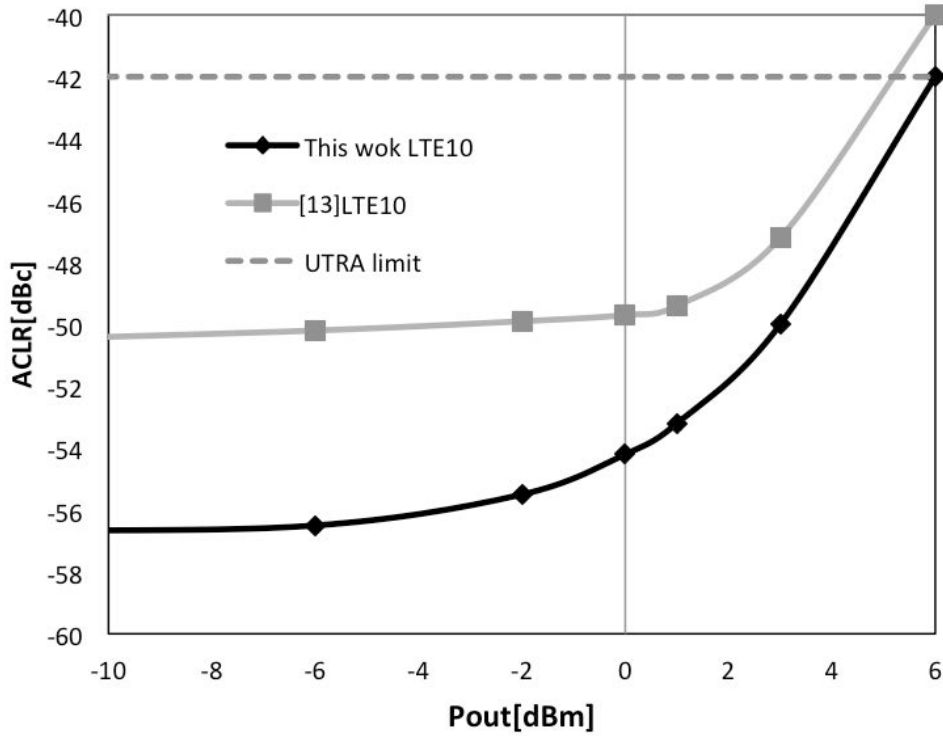


Figure 4.28: Graphic of the ACLR vs output power and comparison with the state-of-the-art

improved efficiency in back-off is also due to a simpler base band chain. The value reports the current of the I and Q path together excluding the DAC. The higher power consumption above 0dBm is not crucial since the high output power condition is statistically unlikely, moreover this drawback

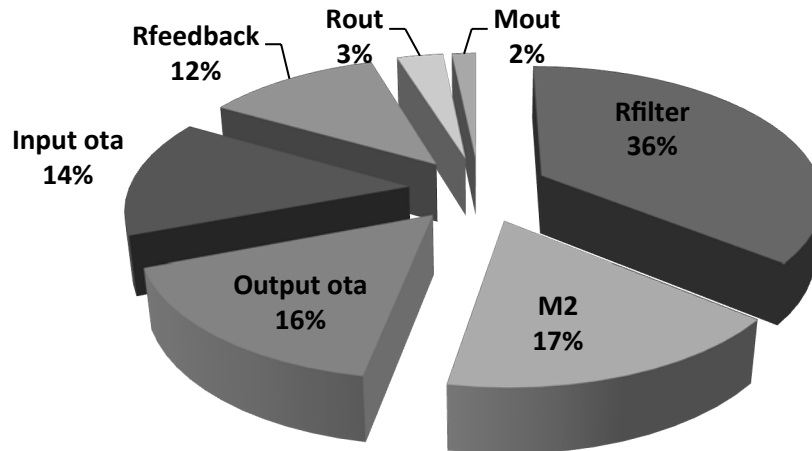


Figure 4.29: Baseband noise contributors at 30MHz offset from the carrier

is repaid with higher linearity as it's shown in figure 4.28. From this figure it can be seen how the

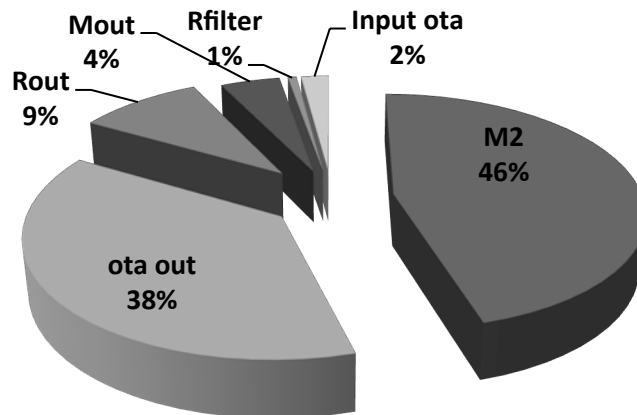


Figure 4.30: Baseband noise contributors at 190MHz offset from the carrier

specifications are respected in all the cases, while for the plot of the state-of-the art ACLR the specs

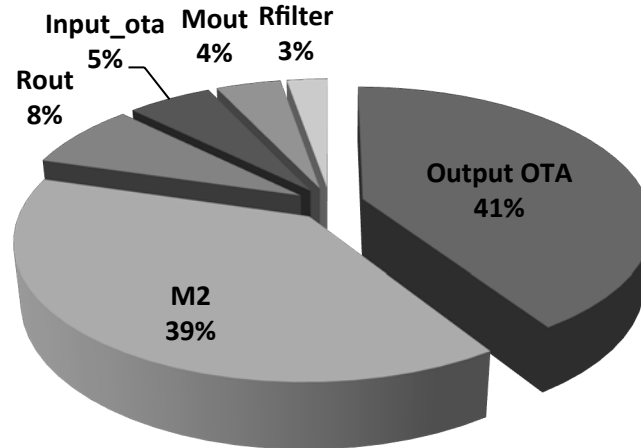


Figure 4.31: Baseband noise contributors at 400MHz offset from the carrier

are not satisfied above 5dBm, at low output power (below -2dBm) the linearity improvement is about 7dB.

For what it concerns the out-of-band noise at 30MHz (Figure 4.29) offset from the carrier (the most challenging specification for the out-of-band noise) the overall out-of-band noise is about -159.5dBc/Hz. As it can be seen from the graph the dominant contributor is the resistor of the RC Filter that is to say that all the active elements are not dominant, consequence of a good design and dimensioning of the circuit. The other dominant contributors are related to the stage before the mixer, especially the MOS M_2 (Fig. 4.16) that acts like a fixed battery and the second OTA, both are noises un-filtered.

As the offset start to increase the noise coming from the baseband loop starts to dominate even if it does not explode or increase in comparison to the 30MHz offset situation, The diagram shows the noise contributors for 190MHz offset (Figure 4.30) where the dominant contributors are related to the baseband loop. The overall contributors produces an out-of-band noise equal to -163,5 dBc/Hz.

Even at 400MHz (Figure 4.31) the noise doesn't grow above -163.5dBc/Hz, the trend of the 190MHz still exist. Since the baseband loop is the dominant contributor and its noise is unfiltered the only way to limit the out-of-band noise is to increase the current consumption of the stage, this is the reason why it's also the most power hungry stage.

4.12 Layout and prototype realization

The chip was realized in 55nm reusing the padding, the baluns and the digital stages of the structure proposed in chapter 3.

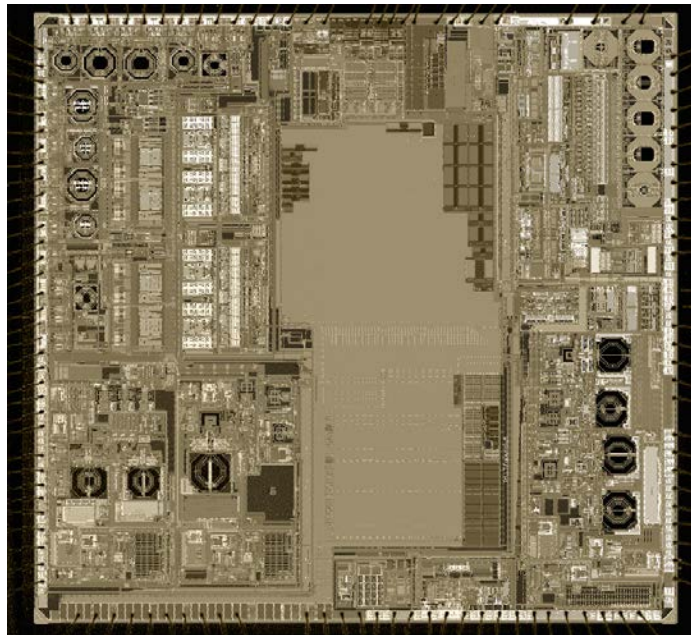


Figure 4.32: Image of the entire chip

As shown in Figure 4.32 the chip integrates also a pll, a receiver and an auxiliary receiver. The Transmitter is placed on the upper right side of the figure, the central part is occupied by the digital stages. In Figure 4.33 is shown the layout of the transmitter and where the DAC, the baseband and the RF part are placed in an area of about 3mm.

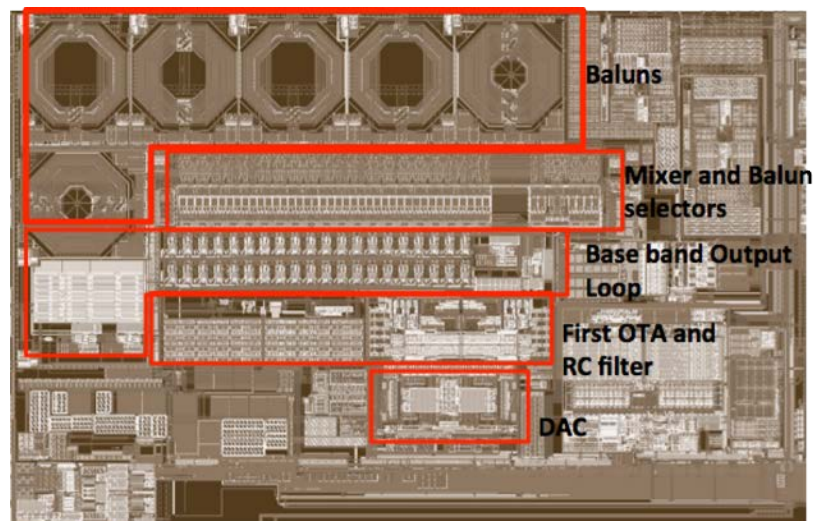


Figure 4.33: Layout of the transmitter

Unfortunately the first attempt to measure the chip was failed due to a wrong cross connection related to a bias reference of the first OTA. As a consequence the OTA didn't produce the correct gain, but only a really low one, also the DC operating point was shifted at higher voltage (close to Vdd) increasing the current consumption on the RF path. For this reason the output didn't produce the correct signal at the output, but only a really low one (about -50dBm) .

A FIB process was implemented to correct the connections, but due to the low rate of success, only one of the two path (I and Q) was fixed with quite good success.

For the Q path the different operating point , due to the wrong fix, produced a big tone (of about 0dBm) at the LO frequency increasing also the distortion of the signal.

To overcome this problem a DAC calibration of the output DC current was done resulting in a reduction of the carrier leakage tone and a reduced distortion.

The results is an improvement in linearity of about 10dB, and a reduction of the LO leakage tone of about 20dB with a tone at the same frequency.

This is one of the few measurement since the part fixed arrived only one week before the end of the Ph.D. contract, we are still waiting the second part to be fixed. However this plot shows that, even if it has to be properly fixed, the circuit is able to generate the signal and is able to improve the signal linearity.

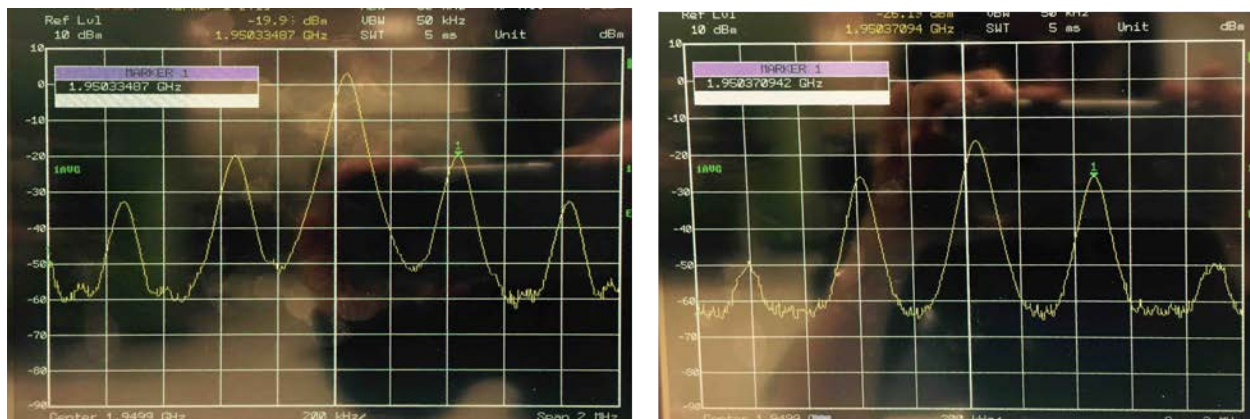


Figure 4.34: Spectrum before (left) and after (right) the DC calibration

Chapter 5: Challenges and possible solutions to issues of the current mode approach

A current-mode transmitter for multi-standard wireless communications has various advantages but there are also some drawbacks. The most important one is the high power consumption of the V/I conversion before the mixer and moreover the difficulty in making a trade-off between efficiency and linearity.

Another problem usually not analyzed is the LO overlap/disoverlap that can reduce the power sent at the output degrading the overall efficiency. To solve these problems two implementations are proposed: a programmable output balun in order to make a trade-off between efficiency and linearity and a programmable duty cycle between the two LO signals in order to recover the LO overlap/ disoverlap.

Another problem usually not analyzed is the carrier leakage, here the problem is described with also a possible solution.

An important specification for a transmitter is its efficiency i.e. the ratio between the power delivered to the load and the power dissipated. For a constant supply voltage, maximum efficiency implies minimum average current consumption. This can be achieved operating in class A/B and maximizing the output swing since a large voltage swing for a given output power corresponds to a high load impedance which in turn implies low signal current. On the other hand, as the swing is increased, the output starts to compress which degrades linearity, e.g. Adjacent Channel Leakage Ratio. Therefore there is a trade-off between efficiency and linearity.

One solution to achieve both high linearity and high efficiency is by adapting polar techniques. The phase and amplitude of the signal are processed independently and combined in the power amplifier (PA): the constant envelope phase component drives the input of a nonlinear and high efficiency PA, while the amplitude component is used to modulate the supply voltage of the PA [23]. In this way, the RF PA always operates in voltage saturation, where high-energy efficiency is achieved.

The bandwidth expansion, originating from the nonlinear transformation between the Cartesian and the polar representation of the signal, causes challenges for both supply and phase modulation in

polar systems. It is quite difficult to handle the arising wide bandwidth of for e.g. a 20MHz LTE signal with traditional supply regulators while still maintaining high-energy efficiency. As an alternative, a digitally modulated power amplifier (DPA) can be adopted [23]), which modulates the amplitude component by turning ON and OFF an array of gain cells according to the required instantaneous output power. For the phase modulation, quadrature upconversion using an RF-DAC can be employed to cover high bandwidths and provide a digital interface to baseband as well.

5.1 Programmable load impedance

For Cartesian transmitters with non constant envelope output compression dominates distortion near maximum power when, however, power consumption is less critical because such a condition, being statistically unlikely, has a small effect on average consumption. In this case a small load impedance should be used exchanging power dissipation for linearity. On the other hand, in back-off, output compression is negligible but efficiency is paramount being statistically very likely. In this case a high load impedance should be used exchanging linearity for lower power dissipation.

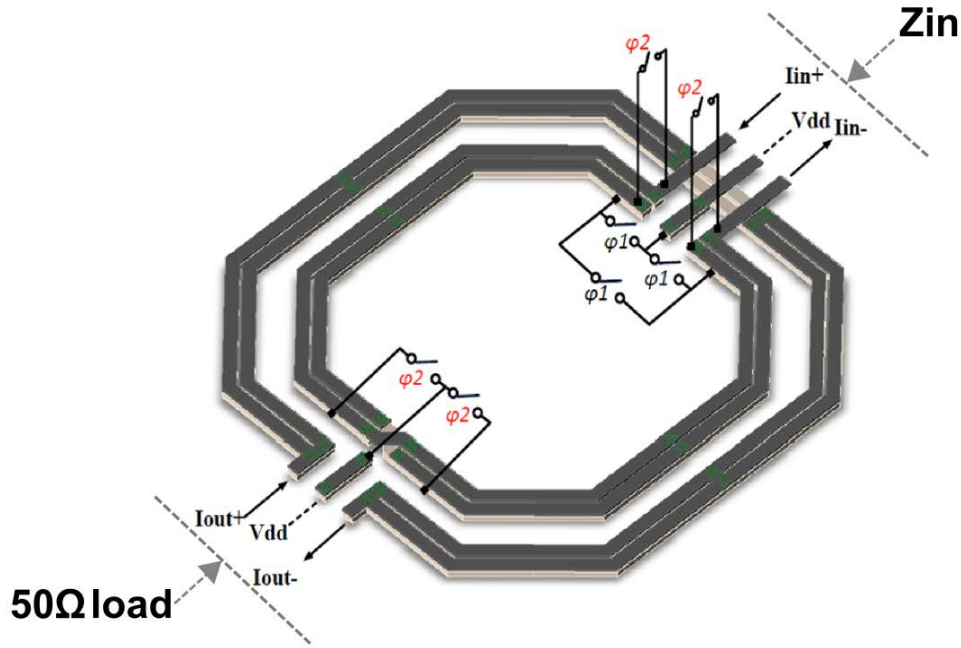


Fig 5.1: Programmable load impedance created using two set of switches at the two sides of the primary coil

To satisfy both cases programmable load impedance with output power should be implemented. This can be achieved, at least conceptually, acting on the turn ratio of the balun through two sets of switches connected to the two sides of the primary coil as shown in Fig 5.1.

A planar monolithic transformer [24] is constructed from inter-wound of metal layer and here in shown in figure 5.1 while the conceptual schematic is shown in figure 5.2.

Magnetic flux produced by current i_p flowing into the primary winding at terminal P induces a current in the secondary winding that flows out of terminal S . This produces a positive voltage across a load connected between terminals S and $\bar{S}$. The main electrical parameters of interest to a circuit designer are the transformer turns ratio n and the coefficient of magnetic coupling k_m . The current and voltage transformations between windings in an ideal transformer are related to the turns ratio by the following equation:

$$n = \frac{v_s}{v_p} = \frac{i_p}{i_s} = \sqrt{\frac{L_s}{L_p}} \quad (43)$$

Where the primary and secondary voltages (v_p , v_s) and currents (i_p , i_s) are defined in Fig. 5.2, and L_p , L_s are the self-inductances of the primary and secondary windings, respectively. The strength of the magnetic coupling between windings is indicated by the k -factor, as :

$$k_m = \frac{M}{\sqrt{L_p L_s}} \quad (44)$$

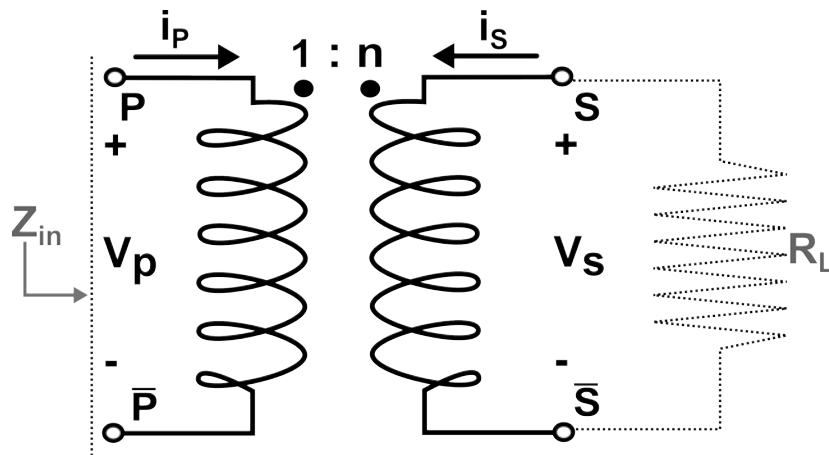


Fig 5.2: Schematic of an impedance transformer

Where M is the mutual inductance between the primary and secondary windings. The self-inductance of a given winding is the inductance measured at the transformer terminals with all other windings open-circuited. If the magnetic coupling between winding is perfect (i.e., no leakage of the magnetic

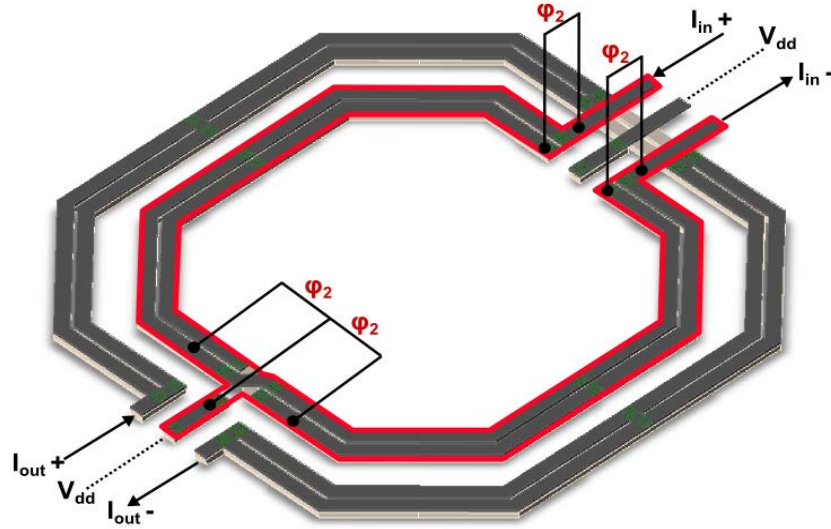


Figure 5.3: Balun configuration when ϕ_2 is high and ϕ_1 is low, the impedance seen at the primary is about 30Ω

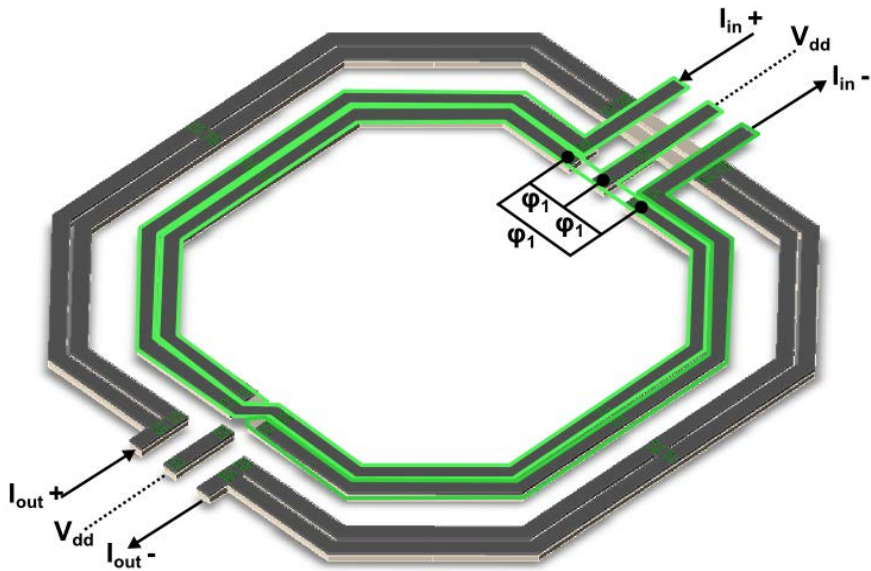


Figure 5.4: Balun configuration when ϕ_2 is low and ϕ_1 is high, the impedance seen at the primary is about 120Ω

flux), k_m is unity, while uncoupled coils have a k -factor of zero. A practical transformer will have a k -factor somewhere between these two extremes. Since the materials used in the fabrication of an IC chip have magnetic properties similar to air, there is poor confinement of the magnetic flux in a monolithic transformer and $M < \sqrt{L_p L_s}$. Thus, the k -factor is always substantially less than one for a monolithic transformer, however, coupling coefficients as high as 0.9 are realizable on-chip. For the idea implementation a planar structure is chosen since a perfect magnetic coupling is not needed and a k_m with a value of about 0.8 is sufficient. The configuration was simulated using ideal switches. Obviously in real implantation the presence of the switches can bring to Q degradation even if the switched are put in point of the coil at minimum swing in order to limit the signal degradation.

According to [24], acting on the balun turns of the transformer is possible to charge the impedance seen at the primary which is defined as:

$$Z_{in} = \frac{R_L}{n^2}$$

When ϕ_2 is high (corresponding switch on) and ϕ_1 is low (corresponding switch off) the turn ratio (n) is one while the transformer ratio ($n_{eq} = n/k$) is 1.25 as it's shown in Figure 5.3. In this condition, considering a 50Ω load, the impedance seen at the primary is equal to about 30Ω.

When ϕ_2 is low (switch off) and ϕ_1 is high (Figure 5.4) the primary coil has two turns instead of one so the turn ratio and the transformer ratio are halved making the impedance at the primary about 120Ω.

5.2 Simulation results and comparison with the previous topology

To compare the proposed and old transmitter in a fair way, simulations in the same conditions are performed for both cases. Fig. 5.5 compares current consumption (I and Q branches excluding the DAC) versus output power for the two transmitters. The old one [13] sees a constant impedance Z_1 at the primary while the new one (by changing the balun turn ratio at 0dBm) sees $Z_1/2$ above 0dBm and $2Z_1$ below. Although at high power the new transmitter uses more current, below 0dBm (where consumption is crucial) the current saving is relevant. The improved efficiency in back-off is also due to a simpler base band chain.

The latter aspect is dominant below -30dBm where the new solution uses about half of the current of the previous one.

Fig. 5.6 compares ACLR versus output power for the two transmitters. Also in this case the effect of

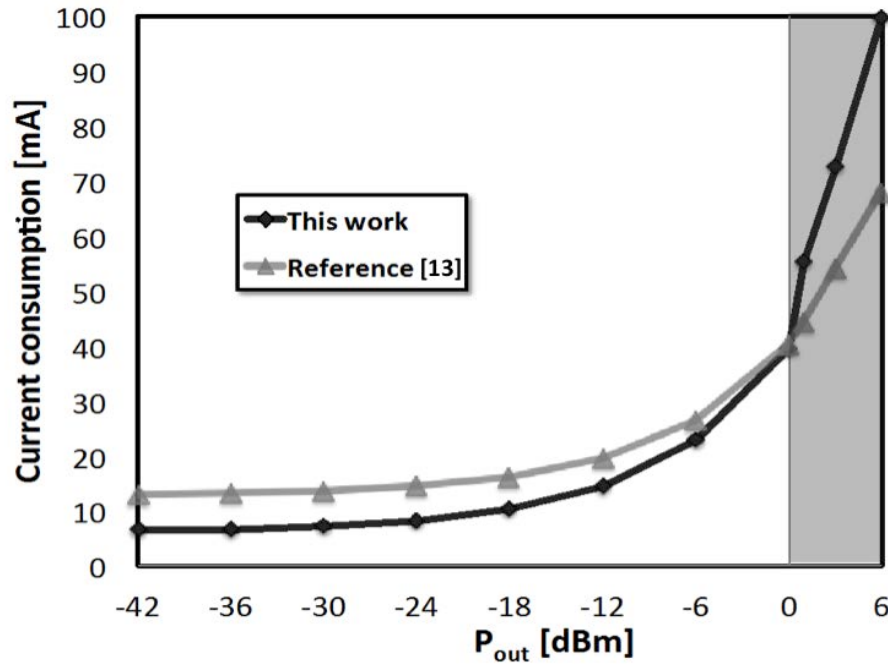


Fig. 5.5 Current consumption: proposed solution vs the transmitter in [13]

switching the output impedance is clearly visible. The combination of a more linear base band and of

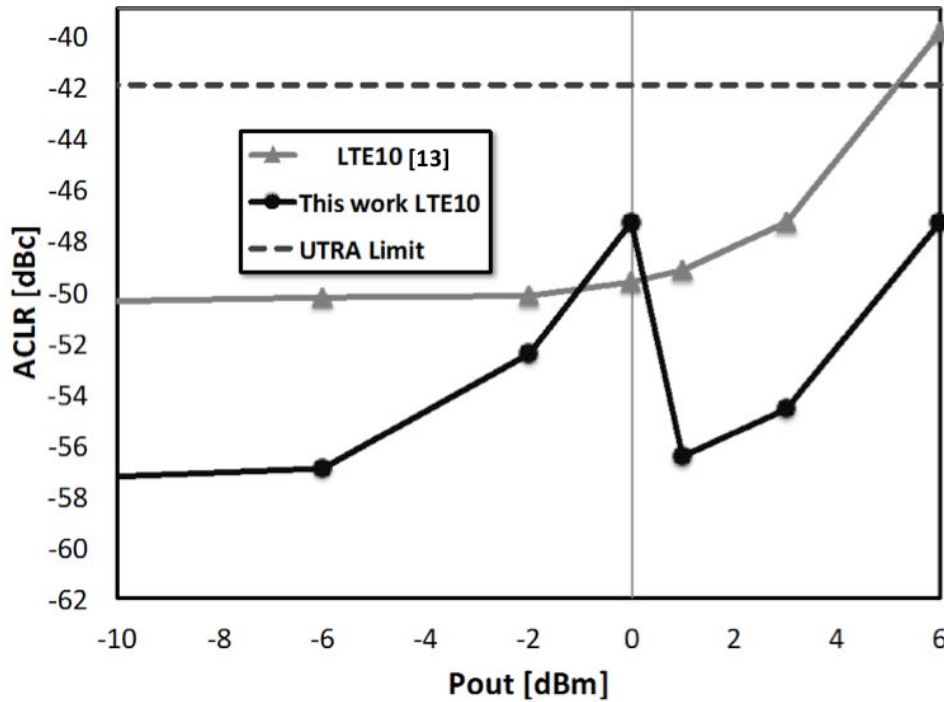


Fig. 5.6 ACLR VS output power

the reduced compression at the output gives an improvement of more than 7dB at maximum power and of about 7dB below -6dBm. More important, while the old one fails to meet the target spec of -42dBc above about 5dBm, the new one has a margin of more than 5dB in all cases.

Table IV : comparison between the new structure and the state-of-the-art

	[13] LTE10	This work	[13] LTE20	This work
Max output power	6dBm	6dBm	6dBm	6dBm
ACLR@ 6dBm [dBc]	-39.9	-47.8	-40	-47.9
ACLR@ 0dBm [dBc]	-49.6	-47.8	-49.7	-47.9
Consumption @ 0dBm	72.6mW	71mW	74.6mW	72.2mW
Consumption @ -10dBm	34mW	28.8mW	36mW	30mW
Consumption @-30dBm	24.5mW	13mW	26.5mW	14.2mW
RX Noise @0dBm	-158 @30MHz	-159 @30MHz	-158 @80MHz	-160.5 @80MHz
RX Noise @6dBm	-158.6 @30MHz	-160.8 @30MHz	-158.6 @80MHz	-161.5 @80MHz
Supply [V]	1.8	1.8	1.8	1.8
Technology	55nm LP	55nm LP	55nm LP	55nm LP

Table IV compares performance for the two transmitters. Noise emission is given for Band 5 for LTE10 and Band 20 for LTE20 (the most critical ones). The new solution gives about 2.8dB and 3.5dB improvement respectively allowing the elimination of the external SAW. Counter intermodulation is also significantly improved.

5.1 Lo disoverlap : Problem description and possible solutions

One of the possible problem related to the use of the active mixer is the presence of the LO disoverlap/overlap than can cause linearity degradation for the presence of high impedance when the both LO signal are at zero and for I and Q crosstalk when every MOS of the gilbert mixer are on. The situation is described in Figure 5.7. Different are the possible solutions, one of those is to use high Q band-pass filters, but they are difficult to implement on a chip.

Three are the main solutions to this problem. The first exploits the use of a sine wave-like LO signal that drives a linear multiplier. However, high linearity analog multiplier design is challenging, while providing only modest output power compared to the switching mixers. Also, flexible wideband sine-wave LO-generation is nontrivial, and the LO amplitude is critical, as it should not drive the LO input of the multiplier into its non linear region. second approach is to use switching mixers, which do produce LO harmonics, but cancel harmonics via multiple mixer paths exploiting different phases or different phase and amplitude. These mixers can achieve sufficient suppression, multiple accurate phases of the LO and/or the baseband have to be generated, but digital clocks can be used. Still there are limits on the number of phases that can be realized especially at high frequency, also the power dissipation is another concern.

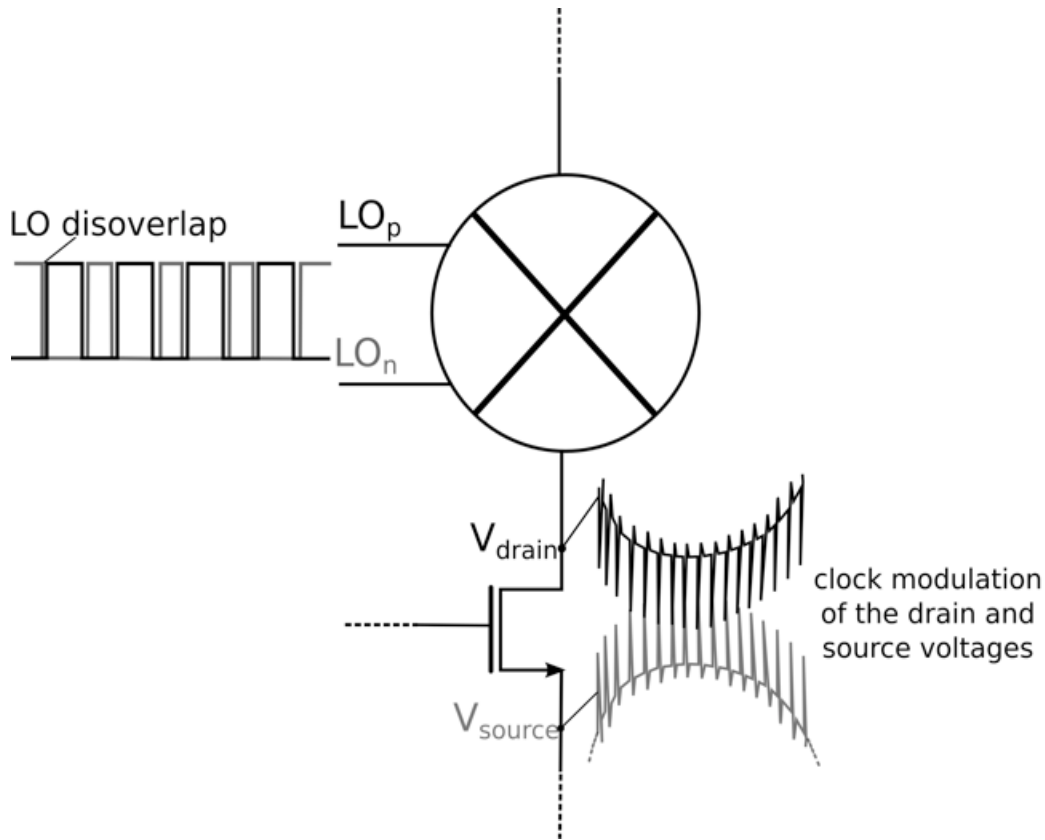


Figure 5.7: LO disoverlap effect on the V_{drain} and V_{source} of the regulated cascode

A third way to clean the transmitter spectrum is obviously to apply filters. However, frequency-agile transmitters would require flexible tunable RF filters, which are difficult to implement, especially for high Q. Passive LC filters are linear, but high Q inductors are problematic, certainly at low RF frequency and require large chip area. Active filter techniques can be used to suppress higher order harmonics, but handling sufficient power [25]. On the other hand, low Q passive RC filters are suitable for on-chip integration as well as being linear and power efficient, but generally do not provide sufficient suppression.

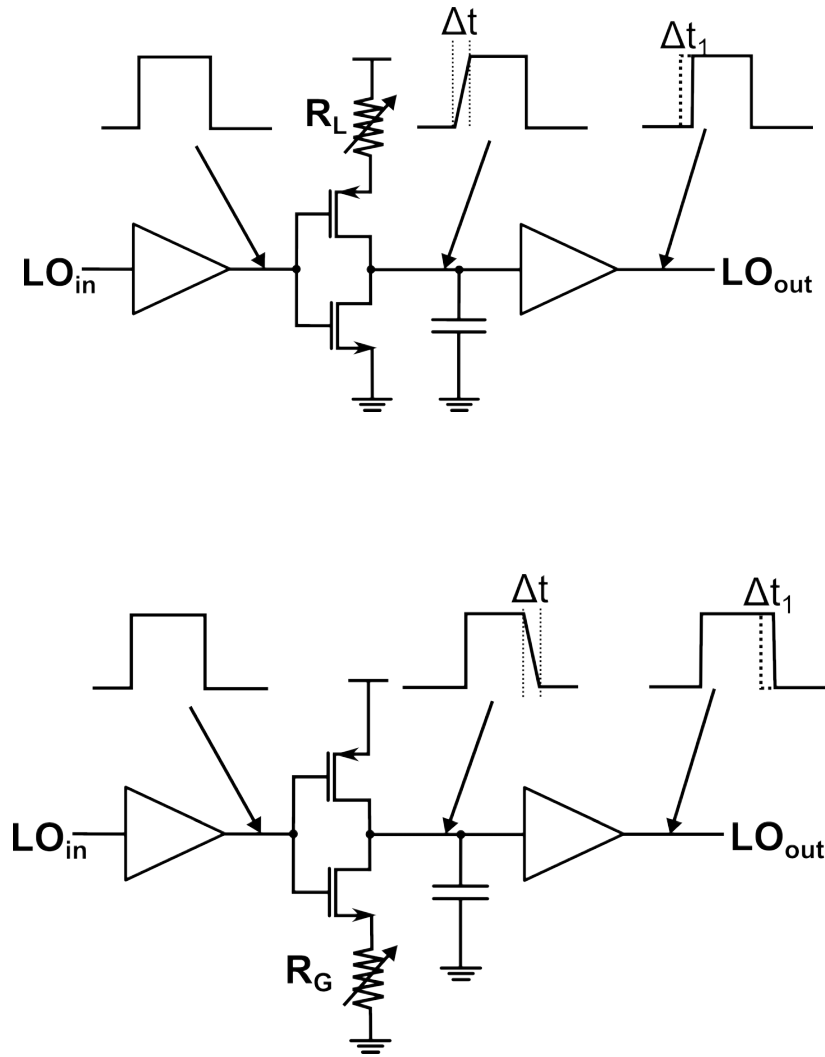


Figure 5.8: Design of a possible circuit that can be implemented in order to regulate the LO overlap/disoverlap in order to achieve better linearity

Another possible solution is to change the duty cycle of one of the two LO signals that drive the active mixer. The circuit is implemented by using an inverter with a variable load between vdd and the source of the p-mos as shown in Fig. 5.8.

The disoverlap can be detected by a simple logic that enables the circuit that recover Lo disoverlap when both LO signals are close to zero like an OR or a NOR. With the same logic can be detected the LO overlap. The circuit in the two cases is slightly different as it's shown in Figure 5.8.

The 50% LO signal is buffered and then an inverter with controllable rising edge delay drives the last buffer stage. The control is accomplished via a tunable resistor that can be implemented with a triode PMOS transistor. For control proposes, monotonic control is desired, which is realized controlling the gate voltage of the triode transistors by an intrinsically monotonic resistor ladder DAC. In order to estimate the delay caused by the inverter combination, we will calculate the charge current for capacitor present after the inverter in Fig. 5.8. The current through the PMOS transistor degenerated by a resistance R_L can be coarsely modeled as

$$I = \frac{\beta}{2} (V_{in} - IR_L - V_{TH})^2 \quad (45)$$

Here, R_L is the resistance of the triode transistor as given by :

$$R_L = \frac{1}{\beta_T(V_{GSMP} - V_{TH})} \quad (46)$$

and $\beta = \mu_P C_{OX} \left(\frac{W}{L}\right)$

Expanding the current expression results in :

$$\frac{\beta}{2} \left(I^2 R_L^2 - I \left(2R_L V_{IN0} + \frac{2}{\beta} \right) + V_{IN0}^2 \right) = 0 \quad (47)$$

where $V_{IN0} = V_{IN} - V_{TH}$, saving the quadratic equation of (47) results in

$$I = \frac{V_{IN0}}{R_L} + \frac{1}{\beta R_L^2} \left(1 - \sqrt{1 + 2V_{IN0}\beta R_L} \right) \quad (48)$$

This current can be used to estimate the delay due to the triode PMOS by the following equation:

$$t_d = C_{IN} \frac{\Delta V}{I} \quad (49)$$

where is the rise time delay, C_{in} is the capacitance at the input of the last buffer and ΔV is taken as $V_{DD}/2$, the point where the last buffer switches. The same calculation could be done with the inverter with the resistor R_G applied to the source of the NMOS.

This is an easy way to control the LO disoverlap, the limit of the improvement is only due to the finite steps of the trimming. This is trivial especially for high frequency LO.

5.2 Carrier Leakage

For applications requiring a wide gain control range, a severe drawback of the Direct Up-Conversion (DUC) architecture is carrier leakage [26], which is determined by offset and matching. A typical spectrum of the carrier leakage is shown in Figure 5.9 where a tone at the LO frequency is clearly visible with a peak power of about -35dBm. It does not scale down with the output signal unless gain control is mostly implemented at RF, which is difficult when the gain range exceeds 70dB. Even if the baseband and modulator are well balanced and carrier leakage is low relative to the full output, transmitter performance is compromised at lower gain. Carrier leakage will peak out of the signal band and cause EVM to exceed the specification. On the other hand, as excessive carrier leakage can violate the power accuracy requirement and limit channel capacity, because at low gain the channel power will be set by the carrier power alone.

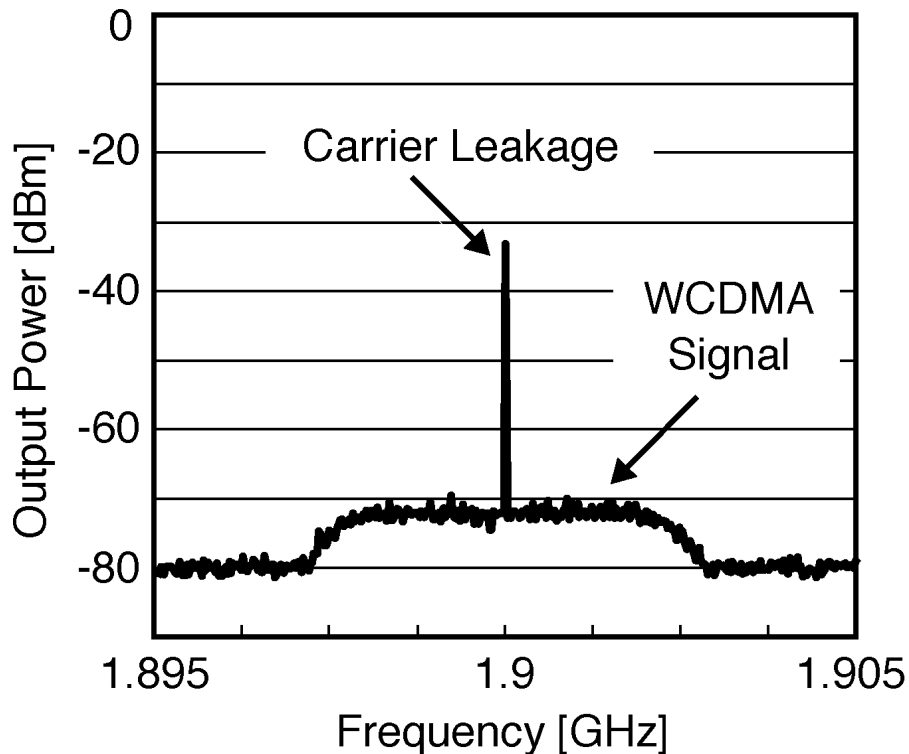


Figure 5.9: Typical shape of the LO leakage at the output of the transitter

Circuit techniques to suppress carrier leakage therefore hold the key to a high integration level through the DUC architecture. The DC offset in the Baseband (I and Q channels) causes carrier leakage and will degrade the modulation accuracy of the transmitted signal. This can be explained by following simple example [4]. Assuming that the DC offsets in the base-band I and Q channels are ΔI_{dc} and ΔQ_{dc} , respectively, the BB signals, $a'_I(t)$ and $a'_Q(t)$, in the I and Q channels are represented by:

$$a'_I = I(t)\cos\varphi(t) + \Delta I_{DC} \quad (50)$$

$$a'_Q = Q(t)\sin\varphi(t) + \Delta Q_{DC} \quad (51)$$

Where $I(t)$ and $Q(t)$ are the amplitudes of the I and Q base-band signals and $\varphi(t)$ is the phase of the corresponding I and Q base-band signals.

At the output of the modulator, the I and Q quadrature signals turn into a signal with an IF or RF carrier, and it can be expressed as:

$$f_{Tx}(t) = a'_I \cos\omega_c t - a'_Q \sin\omega_c t \cong A(t)\cos[\omega_c t + \varphi(t)] + \Delta_{dc} \cos(\omega_c t + \Delta\theta) \quad (52)$$

Where ω_c is the carrier angle frequency $\omega_c = 2\pi f_c$, $A(t)$ is obtained from a'_I and a'_Q as:

$$A(t) = \sqrt{I^2(t)\cos^2\varphi(t) + Q^2(t)\sin^2\varphi(t)} \quad (53)$$

$\varphi(t)$ represents phase modulation equal to:

$$\varphi(t) = \tan^{-1} \left(\frac{Q(t)\sin\varphi(t)}{I(t)\cos\varphi(t)} \right) \quad (54)$$

Δ_{dc} and $\Delta\theta$ are the overall DC offset of the I and Q channel and the phase shift respectively:

$$\Delta_{dc} = \sqrt{\Delta I_{dc}^2 + \Delta Q_{dc}^2} \quad (55)$$

and

$$\Delta\theta = \tan^{-1}(\Delta Q_{dc}/\Delta I_{dc}) \quad (56)$$

The last term on the right side of the carrier leakage is also called carrier feed through (CFT). Here we define the ratio of the carrier leakage power to the desired signal transmission power as the carrier suppression C_s in dB:

$$C_s = 10 \log \frac{P_{CFT}}{P_{Tx}} = 20 \log \frac{V_{CFT_rms}}{V_{Tx_avg}} \quad (57)$$

It is clear that the rms voltage of the carrier leakage is equal to

$$V_{CFT_rms} = \Delta_{dc}/\sqrt{2} \quad (58)$$

The DC offset in the base-band I and Q channels causes carrier feed through, but this is not the only root cause of this problem. The modulator and the frequency up-converter may cause carrier leakage too because the isolation between the LO port and the RF/IF port of these devices is finite around -30dBc depending on design and IC processing technology.

5.3 Calibration Algorithm

The goal of the digital calibration algorithm is to find the minimum carrier power. A rather time-consuming and resource-wasting way is to measure the carrier power at all possible calibration settings and select the minimum. All the cause of carrier leakage can be compensated through applying a proper DC offset to the IF signal path of I/Q modulator. Since carrier leakage and calibration currents are very small, all devices operate in their linear region around their operating points. Neglecting the non-linearity of the calibration current DACs, positive and negative offset currents can be applied to both I/Q path and they are translated to the same carrier power, resulting in a symmetrical calibration characteristic. The calibration current can be applied directly from the DAC or acting on the gates of dedicated voltage or current sources, the accuracy will be determined by the current/voltage source of the LSB of the calibration stage.

Conclusions

As the communication evolve from 2G to 3G and 4G the signal change from a constant envelope modulation to non-constant envelope modulation to increase bandwidth efficiency, this trend however bring to reduced efficiency in mobile transmitters. Moreover the specifications become more stringent both for the linearity and out-of-band noise aspects.

For the new structure proposed an active up-converter was chosen thanks to his qualities such as the absence of the switched capacitor effect, the good isolation between I and Q path, the small LO drive and the high conversion gain in comparison to the LO signal of a passive mixer.

While the purpose of the state-of-the-art structure was to process the signal totally in current mode to reduce the non linearity of the V/I conversion stage, for the new structure the main goal is to process the signal entirely in class A/B. In this way in fact, less noise is produced leading to a reduction of the filtering order. Moreover, in comparison to a simple class B, the signal is more linear while preserving a better efficiency in comparison to a class A signal.

The structure included:

- A class B DAC with a particular implementation with a third switch in order to inject less noise at zero level current
- A novel baseband structure with an active filter and a passive RC pole. For the first filtering stage, a three stage opamp with also a feed forward path was implemented with an ahuja compensation to increase the phase margin.
- A baseband loop in order to transfer the signal to the mixer with high linearity. The loop implements also a second OTA with a pole-zero doublets to improve the stability for the different mirror ratio.

The circuit has been simulated with good results both for out-band-noise and linearity improving the performances in comparison to the state-of-the-art resulting in an improvement of the current consumption for output powers below 0dBm.

Also an analysis of the trade-off between efficiency and linearity for the RF transmitters implementing active mixer has been made. From this analysis, considering the implementation of a switchable primary coil of the balun, simulations have been made both in ads and cadence. The results show and significant increase of the ACLR above 0dBm and a power consumption improvement below 0dBm.

Moreover the issues regarding the LO disoverlap/overlap and LO leakage has been considered and analyzed describing also the possible solutions.

Appendix: Ahuja vs Miller compensation

Linear CMOS techniques have achieved significant progress over the last five years to provide high-performance low-power analog building blocks like operational amplifiers (op amp), comparators, buffers, etc. These circuits have demonstrated comparable performance to their bipolar counterparts at much less silicon area and power dissipation, thus enabling single chip implementations of complex filtering functions, A/D and D/A conversions with quite stringent specification. Due to relatively simple circuit configurations and flexibility of design, CMOS technology has an edge over NMOS technology and is gaining rapid acceptance as the future technology for linear analog integrated circuits, especially in the telecommunication field. The most important building block in any analog IC is the op amp of which numerous implementations have been reported in both the technologies .

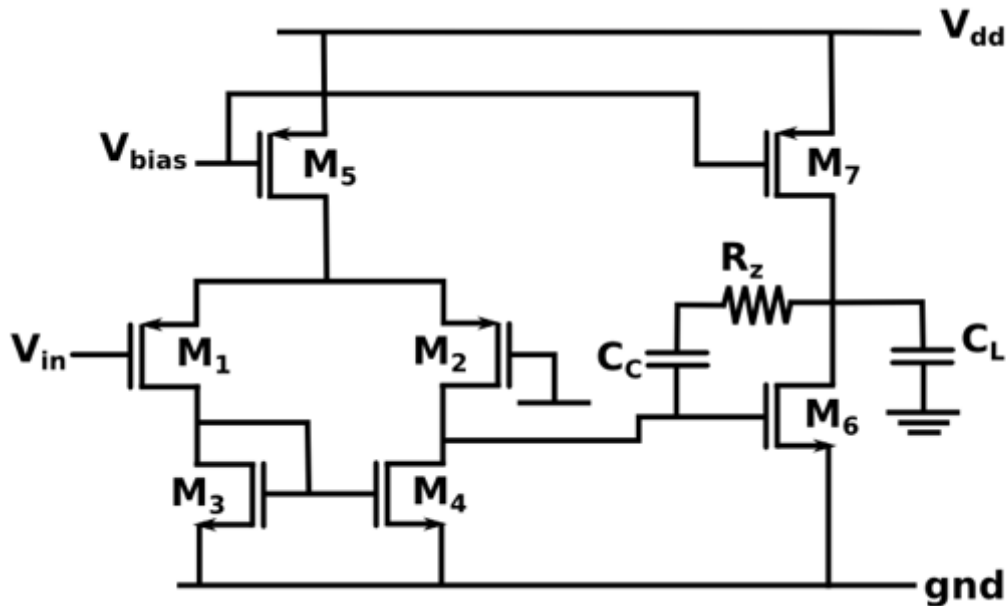


Fig. A.1(a): two stage op-amp with miller compensation

The most commonly used op amp configuration in CMOS has two gain stages, the first one being the differential input stage with single-ended output, and the second one being either class A or class AB inverting output stage. Each stage typically is designed to have gain in the range of 40 to 100. Fig.

A.1(a) shows the circuit configuration while its first-order ac equivalent model is shown in Fig. A.1(b). This configuration is most suitable for internal usage in the IC for driving capacitive loads only. Briefly, transistors M1 to M5 form the input differential stage and M6 and M7 form the output inverting gain stage. The series RC network across the second gain stage provides the frequency compensation for the op amp. This circuit, previously analyzed by many authors displays a dominant pole, two complex high frequency poles, and a zero which can be moved from the right half plane to the left half plane by increasing the compensating resistor value R_z .

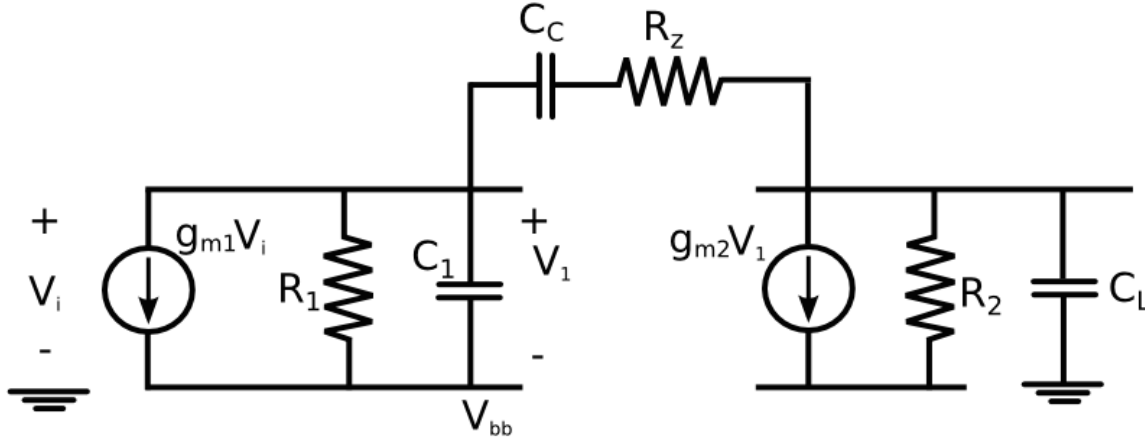


Fig. A.1(b): two stage op-amp with miller compensation, equivalent mode

This is pictorially shown in Fig. 1(b). Due to feed forward path with no inversion from the first stage output to the op amp output provided by the compensation capacitor at high frequencies, the op amp performance shows the following degradations:

- 1) The op amp stability is severely degraded for capacitive loads of the same order as compensation capacitor (C_L must be less than $g_{m2}C_C/g_{m1}$ to avoid second pole crossover of the unity gain frequency).
- 2) In case of p-channel MOS transistors for the input differential stage, the negative power supply displays a zero at the dominant pole frequency of the op amp in unity gain configuration. The zero boosts the magnitude but lags the phase, worst combination for stability. This results in serious performance degradation for sampled data systems which use high-frequency switching regulators to generate their power supplies. (In the case of n-channel MOS transistors for the input differential pair, it is the positive supply which shows similar degradation).

The circuit technique proposed by Ahuja [27] overcomes both of these limitations.

The technique is based on removing the feed forward path from the first stage output to the op amp output.

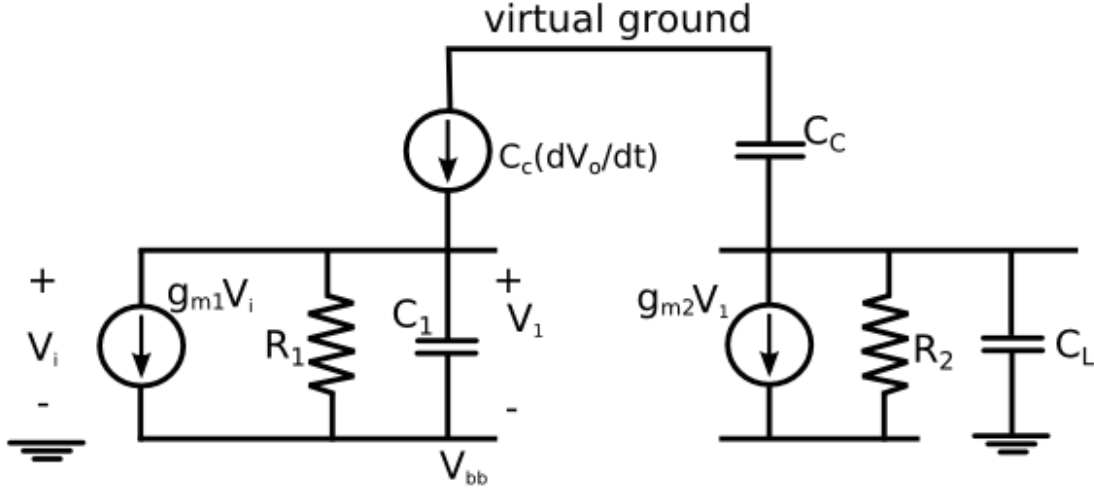


Fig. A.2: two stage op-amp with ahuja compensation, equivalent mode

The circuit shown in Figure A.2 has a current $C_c(dV_o - V_1)/dt$ flowing into the first-stage output. If one can devise a circuit where only $C_c dV_o/dt$ current flows into the first stage output, one would have eliminated the feedforward path while still producing a dominant pole due to the Miller effect. The only difference is that Miller capacitance is now $A_2 C_c$ rather than $(1 + A_2) C_c$ where A_2 is the second-stage voltage gain. Thus, the conceptual ac equivalent of such a circuit is shown in Fig. 2(a). Here the compensation capacitor is shown to be connected between the output node and a virtual ground (or ac ground), while the controlled current source having the same value as $C_c dV_o/dt$ charges the first-stage output.

The detailed derivation of the gain is shown below.

$$V_o = -g_{m2} V_1 \left(\frac{1}{sC_c} \parallel R_2 \parallel \frac{1}{sC_L} \right) = \frac{g_{m2} R_2 V_1}{sR_2(C_c + C_L) + 1} \quad (59)$$

$$V_1 = (sC_c V_o - g_{m1} V_1) \left(\frac{1}{sC_1} \parallel R_1 \right) = (sC_c V_o - g_{m1} V_1) \frac{R_1}{sC_1 R_1 + 1} \quad (60)$$

The gain is obtained by substituting (60) into (59):

$$V_o = \frac{-g_{m2} R_2}{sR_2(C_c + C_L) + 1} \left(\frac{sC_c R_1 V_o}{sC_1 R_1 + 1} - \frac{g_{m1} R_1 V_1}{sC_1 R_1 + 1} \right) = \frac{-sC_c g_{m2} R_1 R_2}{[sR_2(C_c + C_L) + 1](sC_1 R_1 + 1)} V_o + \frac{g_{m1} g_{m2} R_1 R_2 V_1}{[sR_2(C_c + C_L) + 1](sC_1 R_1 + 1)} \quad (61)$$

Rearranging

$$V_o \left[1 + \frac{sC_c g_{m2} R_1 R_2}{[sR_2(C_c + C_L) + 1](sC_1 R_1 + 1)} \right] = \frac{g_{m1} g_{m2} R_1 R_2}{[sR_2(C_c + C_L) + 1](sC_1 R_1 + 1)} V_1$$

$$\frac{V_o}{V_1} = \frac{g_{m1} g_{m2} R_1 R_2}{[sR_2(C_c + C_L) + 1](sC_1 R_1 + 1) + sC_c g_{m2} R_1 R_2} \quad (62)$$

Expanding the denominator:

$$\frac{V_o}{V_1} = \frac{g_{m1} g_{m2} R_1 R_2}{s^2 R_2 R_1 C_1 (C_c + C_L) + s[sR_2(C_c + C_L) + R_1 C_1 + g_{m2} R_1 R_2 C_c] + 1} \quad (63)$$

To obtain the poles, we can factor the denominator by comparing it with the usual template

$$\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right) = \frac{s^2}{\omega_{p1} \omega_{p2}} + \left(\frac{1}{\omega_{p1}} + \frac{1}{\omega_{p2}}\right) s + 1 \quad (64)$$

The resulting poles are in the LHP and real. Assuming that they are widely spaced ($\omega_{p2} \gg \omega_{p1}$), we can approximate them as:

$$\omega_{p1} = \frac{1}{R_1 C_1 + R_2(C_c + C_L) + g_{m2} R_1 R_2 C_c} \quad (65)$$

$$\omega_{p2} = \frac{R_1 C_1 + R_2(C_c + C_L) + g_{m2} R_1 R_2 C_c}{R_1 R_2 C_1 (C_c + C_L)} \quad (66)$$

If $R_1(g_{m2} R_2 C_c) \gg R_1 C_1, R_2(C_c + C_L)$, we can further approximate the two poles to:

$$\omega_{p1} \approx \frac{1}{g_{m2} R_1 R_2 C_c} \quad (67)$$

$$\omega_{p2} \approx \frac{g_{m2} C_c}{C_1(C_c + C_L)} \quad (68)$$

The AC equivalent model is based used was based on the assumption that gm3 is large and the source of M3 can be approximated by a virtual ground. If gm3 is not large, the derivation results in complex poles and also an extra zero. Also, there is more than one way to implement the Ahuja compensation .

Where does the improved stability come from?

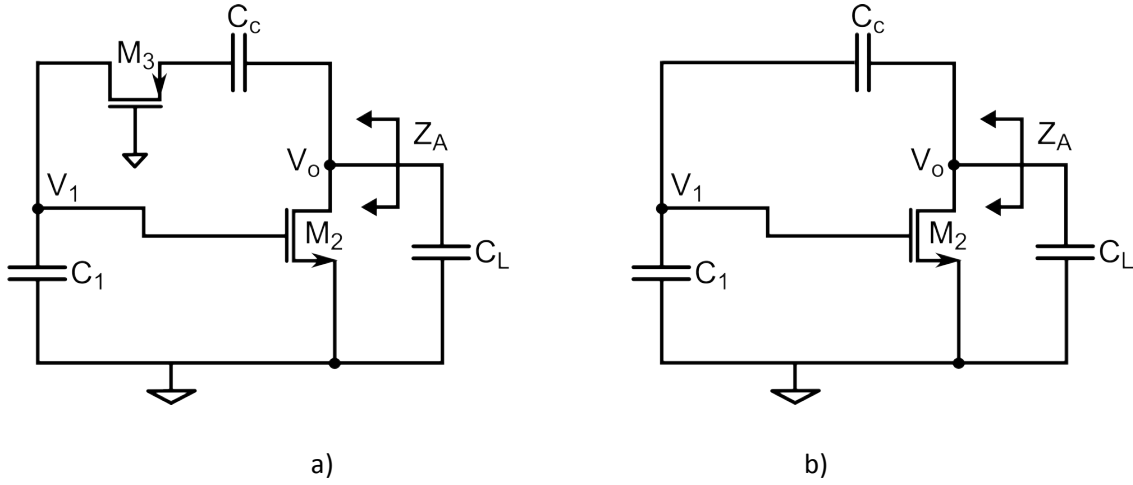


Fig. A.3: a) Ahuja configuration b) Miller configuration

In Miller compensated opamps in figure A.1a (for the moment, $R_z=0$), the resistance at the output node is can be approximated by $1/g_{m2}$ (assuming $C_1 \ll C_c$; C_L), and the non-dominant pole is:

$$\omega_{p2} = \frac{g_{m2}}{C_L} \frac{C_c}{C_c + C_1} \approx \frac{g_{m2}}{C_L} \quad (69)$$

In the case of Ahuja compensated opamps (figure A.3(a)), transistor M3 acts like a current buffer, taking the current generated, $sC_c V_o$, and pushing it through $1/sC_1$ to give a voltage gain.

$$\frac{V_1}{V_o} = \frac{C_c}{C_1} \quad (70)$$

This voltage gain e effectively amplifies g_{m2} of transistor M₂ leading to an impedance of

$$Z_A = \frac{1}{g_{m2}} \frac{C_1}{C_c} + \frac{1}{sC_c} \quad (71)$$

It can be shown that for such an arrangement, the open-loop gain of the op amp is given by

$$A = \frac{-A_1 A_2}{1 + (R_1 C_1 + R_2 C_L + R_2 C_c + A_2 R_1 C_c) s + s^2 R_1 R_2 C_1 (C_c + C_L)} \quad (72)$$

where $A_1 = g_{m1}R_1$ is the DC gain of the first stage and $A_2 = g_{m2}R_2$ is the DC gain of the second stage.

Notice that there is no finite zero in this circuit and that both the poles are real and are widely spaced.

$$P_1 \cong \frac{1}{(g_{m2}R_2)C_C R_1} \quad (73)$$

$$P_2 \cong \frac{g_{m2}C_c}{C_1(C_C + C_L)} \quad (74)$$

Assuming the internal node capacitance C_1 being much smaller than the compensation capacitor C_C or the load capacitance C_L , the unity gain frequency W_1 is still given by g_{m1}/C_C . This results in

$$\frac{P_2}{W_1} = \frac{g_{m2}}{g_{m1}} \frac{C_C}{C_1} \frac{C_c}{(C_C + C_L)} \quad (75)$$

Taking some typical design values of a two-stage amplifier as given by

$$\frac{g_{m2}}{g_{m1}} = 10, C_c = 5pF, C_1 = 0.5pF, \frac{P_2}{W_1} \geq 5 \quad (76)$$

the ahuja compensation technique can drive up to 100pF capacitive load as compared to 10pF capability of the commonly used RC technique as shown in Fig. A.1(a), Thus, the ahuja technique offers an order of magnitude improvement in capacitive load capability for the same performance. The improvement factor is given by C_c/C_1 , where C_1 can be reduced by careful layout and design of the first stage.

Bibliography

- [1] Sesia S. et al. LTE – The UMTS Long Term Evolution: From Theory to Practice, Wiley, 2nd edition, 2011
- [2] <http://www.3gpp.org/LTE>
- [3] Razavi B. RF Microelectronics, Prentice Hall, 2nd edition, 2011
- [4] Gu, Q., RF System Design of Transceivers for Wireless Communications, Springer, First Edition, 2006
- [5] Sesia S., Toufik I., Baker M. “LTE - The UMTS Long Term Evolution: From Theory to Practice”, Wiley edition, 2011
- [6] Pretl, H., Maurer, L., Schelmbauer, W., Weigel, R., Adler, B., Fenk, J., Linearity considerations of WCDMA front-ends for UMTS
- [7] Christian Henn, Burr-Brown International, Intermodulation distortion (IMD)
- [8] D. Su and W. McFarland, “A 2.5 V, 1-W monolithic CMOS RF power amplifier,” in Proceedings of the IEEE Custom Integrated Circuits Conference, pp. 189–190, May 1997.
- [9] S. C. Cripps, RF Power Amplifiers for Wireless Communications. Boston, MA: Artech House, 1999.
- [10] Razavi, B., "RF transmitter architectures and circuits," Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999 , vol., no., pp.197,204, 1999
- [11] Giannini, V.; Ingels, M.; Sano, T.; Debaillie, B.; Borremans, J.; Craninckx, J., "A multiband LTE SAW-less modulator with -160dBc/Hz RX-band noise in 40nm LP CMOS," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International , vol., no., pp.374,376, 20-24 Feb. 2011
- [12] Rossi, P.; Codega, N.; Gerna, D.; Liscidini, A.; Ottini, D.; Yong He; Pirola, A.; Sacchi, E.; Uehara, G.; Chao Yang; Castello, R., "An LTE transmitter using a class-A/B power mixer," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International , vol., no., pp.340,341, 17-21 Feb. 2013

- [13] Codega, N.; Liscidini, A.; Castello, R., "A low out-of-band noise LTE transmitter with current-mode approach," ESSCIRC (ESSCIRC), 2013 Proceedings of the , vol., no., pp.283,286, 16-20 Sept. 2013
- [14] Codega, N.; Rossi, P.; Pirola, A.; Liscidini, A.; Castello, R., "A Current-Mode, Low Out-of-Band Noise LTE Transmitter With a Class-A/B Power Mixer," Solid-State Circuits, IEEE Journal of , vol.49, no.7, pp.1627,1638, July 2014
- [15] Xin He; Van Sinderen, J., "A 45nm low-power SAW-less WCDMA transmit modulator using direct quadrature voltage modulation," Solid- State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International, vol., no., pp.120,121,121a, 8-12 Feb. 2009.
- [16] Xin He; van Sinderen, J., "A Low-Power, Low-EVM, SAW-Less WCDMA Transmitter Using Direct Quadrature Voltage Modulation," Solid-State Circuits, IEEE Journal of , vol.44, no.12, pp.3448,3458, Dec. 2009
- [17] Xin He; van Sinderen, J.; Rutten, R., "A 45nm WCDMA transmitter using direct quadrature voltage modulator with high oversampling digital front-end," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International
- [18] Cassia, M. et al., "A Low-Power CMOS SAW-Less Quad Band WCDMA /HSPA /HSPA+ /1X/ EGPRS Transmitter," Solid-State Circuits, IEEE Journal of, vol.44, no.7, pp.1897,1906, July 2009.
- [19] Oliaei, O. et al., "A multiband multimode transmitter without driver amplifier," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International, vol., no., pp.164,166, 19-23 Feb. 2012.
- [20] Girani, E.; Codega, N.; Castello, R., "A low power/noise emission LTE fully class A/B transmitter with a programmable output balun," Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on , vol., no., pp.802,805, 7-10 Dec. 2014
- [21] Gu, Q; "RF system design of transceivers for wireless communications," Springer International edition
- [22] Sosio, M.; Liscidini, A.; Castello, R., "A 2G/3G Cellular Analog Baseband Based on a Filtering ADC," Circuits and Systems II: Express Briefs, IEEE Transactions on , vol.59, no.4, pp.214,218, April 2012
- [23] Junqing Guan; Aref, A.F.; Negra, R., "Analysis of design specification for digital polar RF transmitter at system and architectural level," Radio and Wireless Symposium (RWS), 2012 IEEE , vol., no., pp.443,446, 15-18 Jan. 2012

- [24] Long, J.R., "Monolithic transformers for silicon RF IC design," Solid-State Circuits, IEEE Journal of , vol.35, no.9, pp.1368,1382, Sept. 2000
- [25] Subhan, S.; Klumperink, E.A.M.; Ghaffari, A.; Wienk, G.J.M.; Nauta, B., "A 100–800 MHz 8-Path Polyphase Transmitter With Mixer Duty-Cycle Control Achieving ≤ -40 dBc for ALL Harmonics," Solid-State Circuits, IEEE Journal of , vol.49, no.3, pp.595,607, March 2014
- [26] Brenna, G.; Tschopp, D.; Rogin, J.; Kouchev, I.; Qiuting Huang, "A 2-GHz carrier leakage calibrated direct-conversion WCDMA transmitter in 0.13- μ m CMOS," Solid-State Circuits, IEEE Journal of , vol.39, no.8, pp.1253,1262, Aug. 2004
- [27] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," IEEE Journal of Solid State Circuits, vol. 18, no. 6, pp. 629-633, December 1983.