Current-Mode High Sensitivity CMOS Hall Magnetic Sensors

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To

my parents, brothers, sisters and my wife

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Acronyms

1/f	Flicker Noise
3D	Three Dimensional
ABS	Anti-lock Braking system
ADC	Analog to Digital Converter
AMR	Anisotropic Magneto-Resistance
ASIC	Application Specific Integrated Circuit
CAD	Computer Aided Design
CAGR	Compound Annual Growth Rate
CM	Current-Mode
CMFB	Common Mode FeedBack
CMOS	Complementary Metal Oxide Semiconductor
CS	Current Spinning
DAC	Digital to Analog Converter
FEM	Finite Element Modeling
GBW	Gain BandWidth
GMR	Giant Magneto-Resistance
IC	Integrated Circuit
IVC (I/V)	Current to Voltage Converter
IMC	Integrated Magnetic Concentrator
LPF	Low Pass Filter
MEMS	Micro Electro Mechanical System
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MUX	Multiplexer
NLE	Non-Linearity Error
NMR	Nuclear Magnetic Resonance
OpAmp	Operational Amplifier
PCB	Printed Circuit Board
PM	Phase Margin
RRL	Ripple Reduction Loop
SCF	Switched Capacitor Filter
SNR	Signal to Noise Ratio
SQUIDs	Superconducting Quantum Interface Devices
VCM	Voltage Common Mode
VM	Voltage Mode
VHS	Vertical Hall Sensor
VLSI	Very Large Scale Integration

Chapter 1
Introduction

Abstract The interest in magnetic sensors has significantly increased in recent years thanks to attractive advantages in various applications. In fact, magnetic sensors are more and more used not only for automotive and compass applications but also in a large variety of biomedical systems. This enormous popularity is the main driving force for the development of many state-of-the-art architectures with good trade-off between higher sensitivity, low offset and low power dissipation. Moreover, sensors may exhibit high residual offset due to the imperfections of their building blocks and can also result in a challenging system because it involves analog and digital issues for its study, design and implementation. This thesis focuses on the description of several solutions in current-mode situation for horizontal and vertical Hall magnetic sensors. All of the proposed architectures, supported by many simulation results with COMSOL Multiphysics, explore design strategies to reduce the offset and improve the sensitivity without affecting the overall performance of the sensors. Three prototypes have been integrated in a standard 0.18-μm CMOS technology. The measurement results of these prototypes not only confirm the effectiveness of the sensors but also provide to the reader with a more general overview of the design strategies used to accomplish the major goal of this work: design for maximum sensitivity.

1.1 Motivation and Objectives

Hundreds of millions of magnetic sensor devices are produced every year for use in a wide variety of applications [1]. The analysts forecast the Global Magnetic Sensors market to grow at a CAGR [1] of 7.21 percent over the period 2013-2018. One of the key factors contributing to this market growth is the increasing usage in automotive and electronic compasses. The Global Magnetic Sensors market has also been witnessing the miniaturization of magnetic sensors. However, the increasing cost of automotive systems could pose a challenge to the growth of this market [2].

[1] Compound Annual Growth Rate

Figure 1.1 presents the typical ranges of application of the main magnetic sensors and shows the role of Hall effect sensor between them. Very small magnetic fields, usually biomagnetic fields, are measured using SQUID (Superconducting Quantum Interface Devices) sensors. Above 0.1 nT, fluxgate sensors can be used. These are much smaller and detect the vector value. But in order to obtain the best parameters, it should be very carefully manufactured. In the range around the Earth's magnetic field, the anisotropic magnetoresistance (AMR) and giant magnetoresistivity (GMR) sensors are much cheaper. Inductive sensors (search coils), which can be used over a very wide range of values – from very small pT range to very large magnetic fields, from DC (when sensor is moved) to GHz bandwidth, exhibit special features [3].

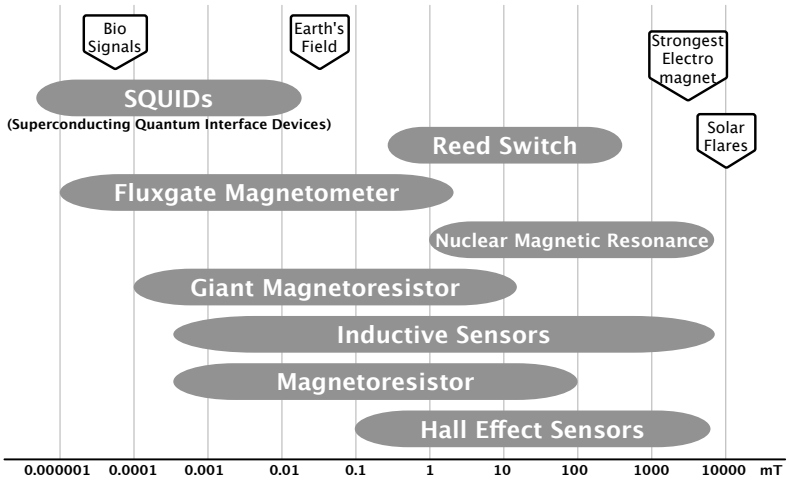

Fig. 1.1 The range of application of the main magnetic field sensors [4].

Large magnetic field is almost exclusively measured by Hall effect sensors. Hall effect sensors have been the workhorse magnetic sensor for decades. Hall sensors are based on the Hall effect transduction principle and measure either constant or varying magnetic field. They have a magnetic field sensitivity range from tens of μT to more than 1 T and have a die size less than one millimetre. Their performance, size and low cost have made them the most popular type of magnetic devices. This is even more true since Hall sensors are easily integrated in modern commercial CMOS technologies.

Fig. 1.2 shows the diversity of Hall effect sensors applications. They are widely used in:

- Biomedical: Anesthesia delivery systems, sleep apnea machines, infusion, insulin or syringe pumps, dental equipment [5]
- Automotive: ignition timing, antilock braking systems (ABS), E-Valve actuators

- Computers: commutation for brushless fans, disk drive index sensors
- Industrial controls: temperature and pressure sensors, speed sensors, position and level sensing, current sensors
- Consumer Devices: exercise equipment, cell phones, compass.

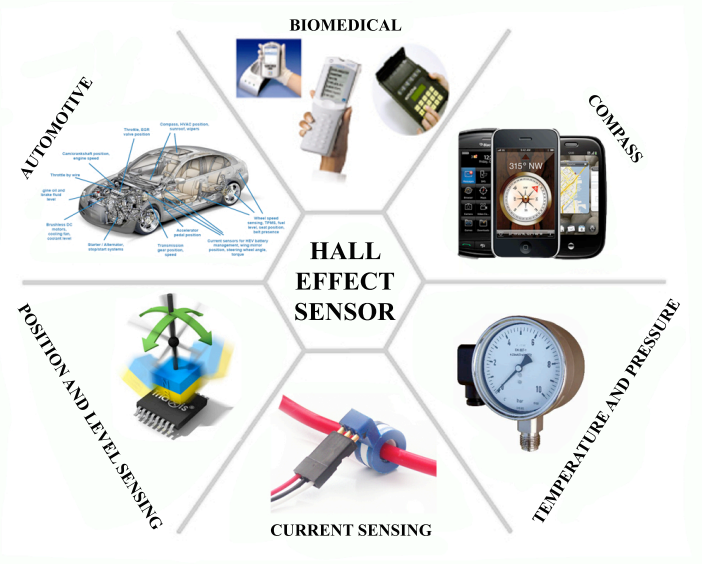

Fig. 1.2 Various application of the Hall devices.

The motivation for this thesis work is to explore the features and limits of the current-mode Hall sensors in both horizontal and vertical method. In order to complete this study, three levels have been considered:

1. The sensor device level,
2. The analog front-end circuit level,
3. The system level topology with optimization of analog building blocks.

On the sensor device level, several shapes and geometries of sensor plates have been simulated and investigated. Between them the cross-shaped plate has been selected because of its symmetrically use of current spinning technique used for offset reduction. The model has been developed in current-mode for saving power and improving the sensitivity. The current-mode sensor has been simulated at first using COMSOL Multiphysics. After that the sensor device model has been then implemented in Verilog–A description language, for behavioural simulations in the Cadence environment.

On the analog front-end circuit level, the readout circuit consists of an Op-Amp that behaves like an integrator, the bias circuits of two Hall plates, current spinning switches and the common mode feedback (CMFB).

On the system level, the novel topologies facilitated have been investigated by examining the features of the current-mode Hall sensors. This level focuses on system analysis, including considerations about overall noise, power consumption, sensitivity and offset. There is a trade-off between the number of sensor contacts and the residual offset of the sensor device.

The aforementioned motivations lead us to the specifications of three Hall magnetic sensor prototypes, as summarized in Table 1.1. Regarding PVHALLREADOUT, a horizontal Hall sensor with twin cross-shaped and its analog interface using a 0.18-μm has been implemented. The measured offset is lower than 50 μT, while it has a sensitivity better than 1660 V/A/mT@25-kS/s. In the second prototype, PVVHSSENSOR, four different geometries vertical Hall sensor have been integrated. However, in the third chip, PVVHSREADOUT, an integrator readout circuit has been added as a current to voltage (V/I) converter. The power dissipation in all fabricated prototypes are in the order of tens of μW.

Table 1.1 Research Target

Chip Name	Classes	Sensor Type	Technology
PVHALLREADOUT	Horizontal	Twin Cross-Shaped	TSMC 0.18 μm CMOS
PVVHSSENSORS	Vertical	Four 4-Folded 3-Contact	GF 0.18 μm CMOS
PVVHSREADOUT	Vertical	A 4-Folded 3-Contact	GF 0.18 μm CMOS

1.2 Thesis Overview and Summary of Results

This thesis assumes that the reader has a basic knowledge on analog circuit design, layout and is familiar with the main features, concepts and principles of operation of magnetic sensors. Fig. 1.3 summarizes the general structure of this work, which is organized as follows.

Chapter 2 overviews the basic physics behind the Hall effect sensors. A comparison between the sensor performance when they are biased in voltage-mode and current-mode is given. The sensitivity and offset of the sensor are defined and the effects of imperfections on the sensor performance are summarized, including temperature and geometry variations. Furthermore, horizontal and vertical Hall sensors are compared. The magnetic sensor characteristics including sensitivity, offset, noise and nonlinearity are discussed. At the end, state-of-the-art CMOS magnetic Hall sensors regarding sensitivity improvement and offset reduction are investigated, while afterwards their applications are mentioned.

Chapter 3 describes a current-mode horizontal Hall magnetic sensor. The current-mode approach is explained in more detail in this chapter. The current spinning tech-

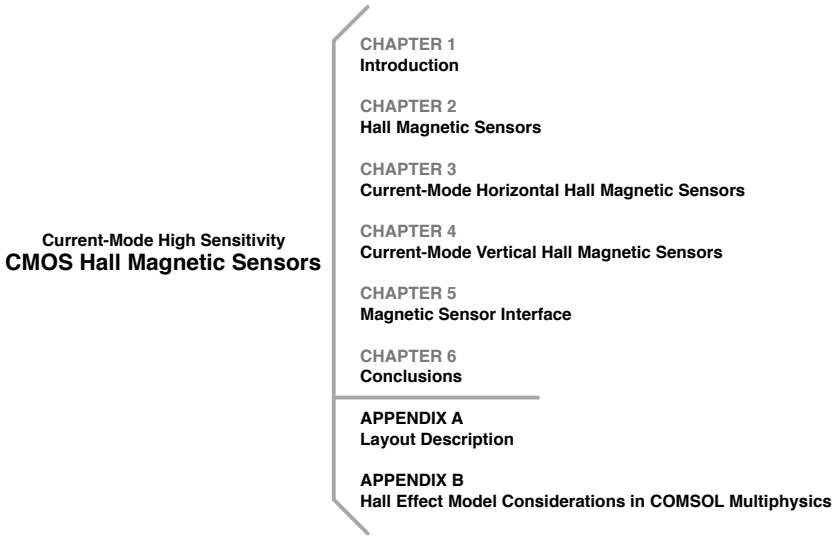

Fig. 1.3 Thesis structure.

nique and Implementation of the related switches are then described. The chapter ends with the simulation and measurement results of the fabricated prototype.

Chapter 4 investigates the feasibility to design a vertical Hall sensor in current domain. The device sensor is realized by the four-folded vertical sensor plate. Simulations results, obtained in two different environments, are compared and discussed. COMSOL results are validated with respect to the electrical behavior of an 8-resistor Verilog-A model implemented in Cadence environment. The implementation of the four different geometries of 4-folded 3-contact vertical Hall sensor device, sensor biasing circuit and proper digital control unit is expressed next.

Chapter 5 explains the magnetic sensor analog front-end, which comprises the current to voltage (I/V) converter, fully differential amplifier and chopper stabilization. In following, a switched-capacitor filter and needed digital unit of microsystem are presented. The chapter ends with measurement and experimental results.

Chapter 6 covers the general conclusions resulting of this thesis work.

Additional material is included in two appendices. **Appendix–A** focuses on the layout and schematic diagrams of the main blocks of the prototypes described in Chapter 3, 4 and 5. **Appendix–B** deals with consideration notes about simulation an horizontal magnetic Hall sensor in COMSOL software.

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Chapter 2
Hall Magnetic Sensors

Abstract In this chapter a short background about Hall effect and Hall magnetic sensors is provided, with a detailed description of the considered devices: horizontal and vertical Hall plates. The current-mode technique and its comparison with the voltage-mode technique are then discussed. Next, the state-of-the-art in Hall magnetic sensors is given. This is followed by an overview of the characteristics of the Hall magnetic sensors in CMOS technology. Applications of the Hall magnetic sensors are presented at the end of the chapter.

2.1 The Hall Effect

The Hall effect was discovered by Dr. Edwin Hall in 1879. Dr. Hall found that when a magnet was placed with its field flowing perpendicular to the face of a thin rectangle of gold through which current was owing, a difference in potential appeared at the opposite edges. He found that this voltage was proportional to the current flowing through the conductor, and the flux density or magnetic induction perpendicular to the conductor. When a current-carrying conductor is placed into a magnetic field, a voltage will be generated, perpendicular to both the current and the field. This principle is known as the *Hall effect*. Fig. 2.1 illustrates the basic principle of the Hall effect. It shows a thin sheet of semiconducting material (Hall plate) through which a current flows. The output connections are perpendicular to the direction of the current. When no magnetic field is present, the current distribution is uniform and no potential difference is seen across the output. When a perpendicular magnetic field is present, a Lorentz force is exerted on the current. This force disturbs the current distribution, resulting in a potential difference (voltage) across the output. This voltage is the Hall voltage (V_{Hall}).

The magnitude of V_{Hall} is directly proportional to the applied field B and the voltage and current biasing is given by

$$V_{Hall} = G\frac{w}{l}\mu_H V_{Bias} B = S_{V_V} V_{Bias} B \tag{2.1}$$

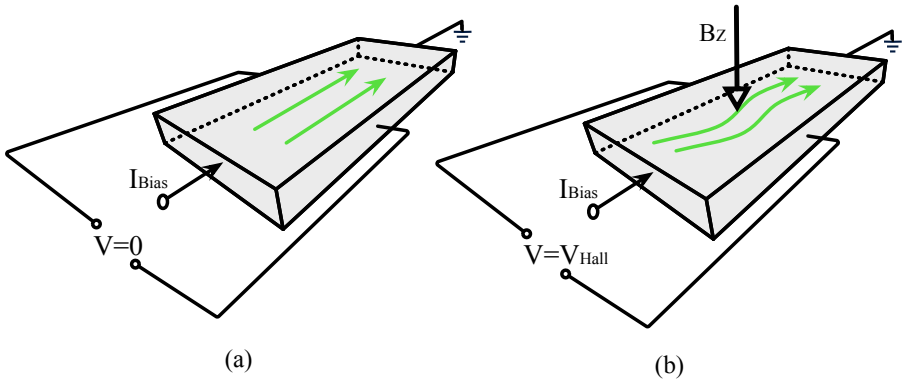

Fig. 2.1 A rectangle Hall plate in presence of (a) no magnetic field and (b) a perpendicular magnetic field (B_z).

$$V_{Hall} = G\frac{r_H}{n.e.t} I_{Bias} B = S_{V_I} I_{Bias} B \tag{2.2}$$

respectively. Here, G is the geometrical correction factor, w and l stand for the width and length of the plate, μ_H is the Hall mobility of majority carriers, V_{Bias} is the total bias voltage, r_H is the Hall scattering factor, n is the carrier concentration, e is the electron charge, t is the tickness of the n-well implantation, I_{Bias} is the total bias current and B is a external magnetic field.

Moreover, S_{V_V} represents the voltage-related voltage-mode sensitivity and S_{V_I} is the current-related voltage-mode sensitivity, which will be explained in detail in subsection 2.5.1. The voltage-related voltage-mode sensitivity S_{V_V} depends on the geometry and the Hall mobility, which is strongly temperature dependent. The current-related voltage-mode sensitivity S_{V_I} is inversely proportional to the carrier concentration n. It is fairly stable in temperature for the plate doping density between 10^{15} and 10^{17} cm^{-3} and in the operating temperature range of many applications nowadays [2].

The current-mode Hall sensor principle is described in the following.

2.2 Hall Effect Devices

2.2.1 Geometry

The term Hall Effect devices is used in order to describe all solid-state electron devices whose principle of operation is based on the Hall effect. Hall devices which are similar to the one that Hall had used in order to discover this effect, today are called *Hall Plates*. Fig. 2.2 shows some typical shapes of Hall plates. The bridge shape (c) is a good approximation of a long Hall device and allows relatively large contacts.

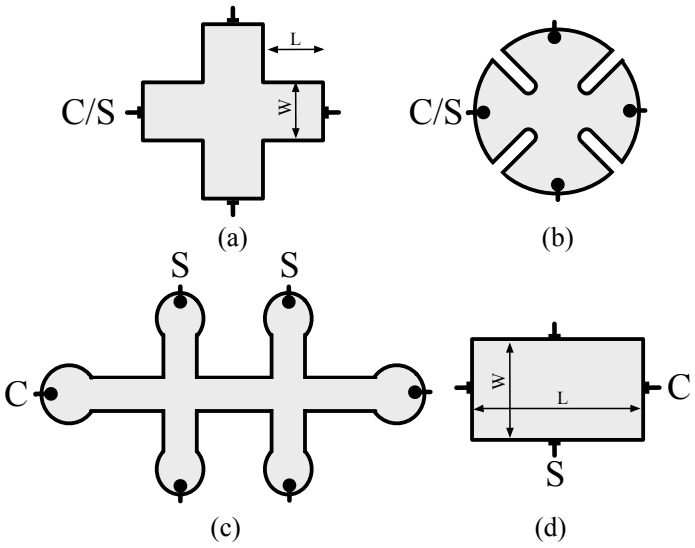

Fig. 2.2 Various shapes of Hall plates: (a) Cross-shaped, (b) Van der Paw shape, (c) Bridge shape and (d) Rectangle shape. C are the current contacts, S the sense contacts and C/S indicates that the two types of contacts are interchangeable [2].

The parasitic effects from the contact resistance and the heating can therefore be minimized. The cross-shaped (a) and the Van der Paw shape (b) are of particular interest. They offer the advantages of a high geometrical correction factor ($G \simeq 1$), a simple and compact geometry and a invariant shape for rotation through $\pi/2$. The current and the sense contacts could be switched without changing the global symmetry. This four-fold symmetry is favourable for the application of offset voltage compensation techniques like the spinning current technique (see 2.5.2.1). This geometry also allows a better definition of the active part centre.

2.2.2 Material

The choice of the proper material for the Hall plate is of crucial importance. From Eq. 2.1, one can conclude that the Hall effect will be favoured in materials with high mobility and also low conductivity. Metals show low mobility and high conductivity and are therefore not a good choice. The sensors are usually prepared from n-type semiconductors where the dominant charge carriers are electrons having much higher mobility than holes. Suitable candidates are intrinsic elements like Si and III-V compounds like InSb, InAs and GaAs. The III-V compounds combine high carrier mobility and reasonable value of conductivity. Silicon has moderate electron mobility but is compatible with the integrated circuit technology. This makes this material very attractive for the realization of Hall sensor chips.

Table 2.1 Gap and mobility of semiconductors at 300 K used to build a Hall plate [6].

Material	E_g[eV]	$\mu_n[cm^{-2}V^{-1}s^{-1}]$	n $[cm^{-3}]$	$R_H[cm^3C^{-1}]^a$
Si	1.12	1500	2.5×10^{15}	2.5×10^{3}
InSb	0.17	80000	9×10^{16}	70
InAs	0.36	33000	5×10^{16}	125
GaAs	1.42	85000	1.45×10^{15}	2.1×10^{3}

[a] R_H is calculated for a given level of doping

Table 2.1 gives the values of the energy gap E_g and the mobility at room temperature of various semiconductors used for Hall plates. R_H is also calculated for a given doping density [5].

2.3 Horizontal vs. Vertical CMOS Hall Devices

The conventional Hall plates are parallel to the chip surface; so considering a chip as an ocean in which a Hall plate floats, such a Hall plates are called *horizontal*. In other words, the horizontal Hall effect device, has an horizontal plate toward the semiconductor substrate and measures the magnetic field, B_Z, perpendicular to the sensor plate surface, as shown in Fig. 2.3(a). The active region of the device is compatible with the layers readily available in CMOS technologies. The surface of integrated horizontal Hall devices is on the order of tens of μm^2. Their current-related sensitivities (S_{V_I}) range from $150 \sim 400\ VA^{-1}T^{-1}$, while typical voltage-related sensitivities (S_{V_V})[1] are $5 \sim 7\ \%T^{-1}$ [9]. Via special implantation techniques sensitivity values up to $S_{V_I} = 2400\ VA^{-1}T^{-1}$ [12] can be obtained. They can be easily cointegrated with signal conditioning electronics in many CMOS Hall effect sensors.

However, a horizontal Hall device, as any Hall device, suffers from offset voltage and low frequency noise. The spinning current method, as a means for offset and low frequency noise reduction, is highly efficient in symmetrical devices. The CMOS Hall sensors based on horizontal Hall devices with current spinning technique feature high resolution, a residual offset as low as 2 μT was reported in [7] and [11].

Recently, there has been growing interest in vertical Hall sensors (VHS). They are sensitive to the in-plane component of the magnetic field, B_Y, and detect the magnetic field in the plane of the sensor plate, as shown in Fig. 2.3(b), as was first reported in [8]. Several geometries have been studied in [11], [13], [19] and [21]. However, the sensitivity of vertical Hall devices is low. Values published for voltage-related sensitivity in the literature are $4\ \%T^{-1}$, $1.2\ \%T^{-1}$ and $1.16\ \%T^{-1}$, as reported in [10], [21] and [20], respectively. Typical current-related sensitivities (S_{V_I}) range from $100 \sim 400\ VA^{-1}T^{-1}$ is reported in [10].

[1] $V/(VT) = (T)^{-1}$

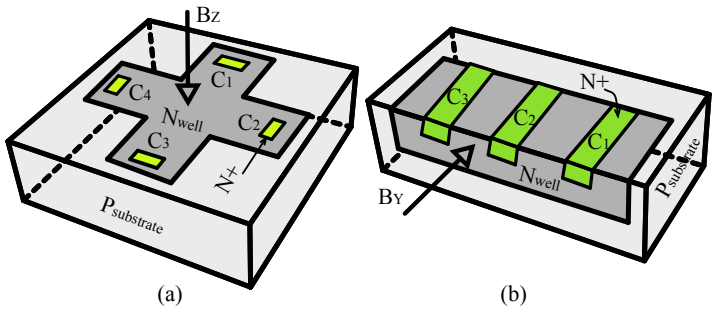

Fig. 2.3 (a) Horizontal Hall effect device and (b) three contacts vertical Hall device cross-sections in CMOS technology.

Various geometries of CMOS vertical Hall devices have been also studied with spinning current method for offset reduction, such as 3-contact four-folded [20], 4-contact (4C) [22], 5-contact (5C) [8], and 6-contact (6C) [10], as shown in Fig. 2.4.

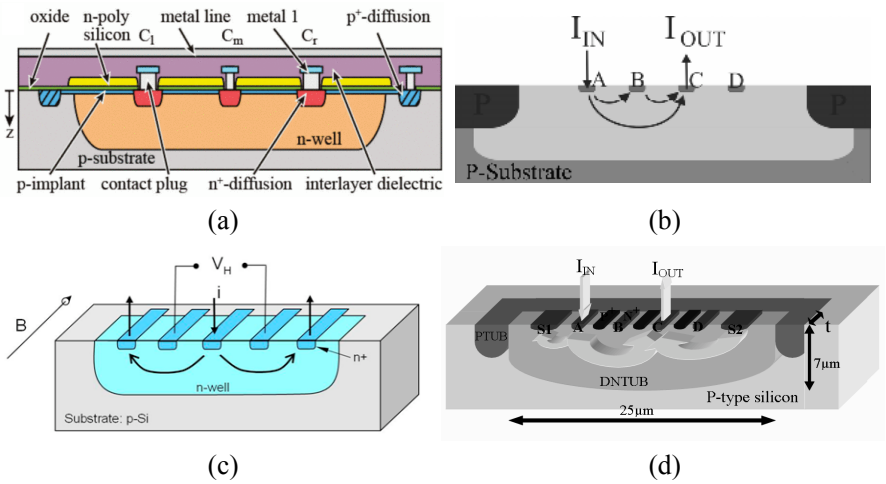

Fig. 2.4 (a) 3-contact, (b) 4-contact (4C), (c) 5-contact (5C), and (d) 6-contact (6C) vertical Hall devices in CMOS technology.

2.4 Current-Mode vs. Voltage-Mode Technique

Typically, Hall plates are used in voltage-mode. This means that the magnetic field to be measured is converted into an output voltage. The idea behind a current-mode Hall sensor is to have current and not voltage as an output signal.

The physical structure of the proposed current-mode Hall sensor is exactly the same of existing devices, with the same possibility of compensating the offset caused by mismatch (current spinning method). The difference is in the way the signals are driven and extracted.

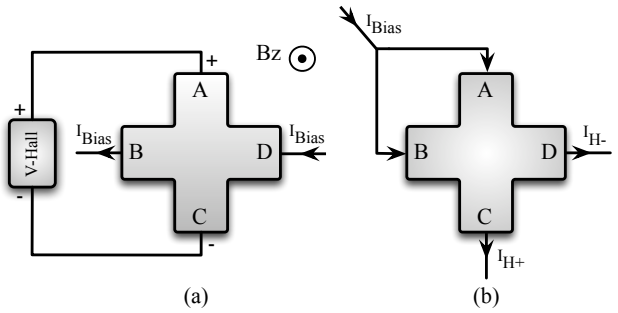

Fig. 2.5 (a) Hall plate operating in voltage-mode. (b) Hall plate working in current-mode.

Consider the device of Fig. 2.5(a); the sensor bias current I_{Bias} flows from one arm to the other in front (the symmetrical structure is for current spinning). A magnetic field B_z gives rise to the Hall voltage across the two orthogonal arms. Here, it is commonly accepted that the Hall voltage can be calculated from Eq. (2.2).

The connection realized in the scheme of Fig. 2.5(b) injects the current laterally in two consecutive arms and a magnetic field causes an unbalancement of the two output currents. A difference of these output currents could be represented by an equivalent current source of a Hall current, I_{Hall}. The current-mode Hall sensor principle has been already described in [2], where it has been found that the Hall current is

$$I_{Hall} = \mu_H \frac{w}{l} B.I_{Bias} \tag{2.3}$$

Here, μ_H is the Hall mobility of majority carriers, I_{Bias} is the total bias current, B is a normal magnetic field and $\frac{w}{l}$ is the width-to-length ratio of the plate.

This mode of operation has been extensively studied to estimate the benefit of the current-mode approach. The output currents (I_{H+}, I_{H-}) are calculated as:

$$I_{H+} = \frac{I_{Bias}}{2} + \frac{I_{Hall}}{2} \tag{2.4}$$

$$I_{H-} = \frac{I_{Bias}}{2} - \frac{I_{Hall}}{2} \tag{2.5}$$

The Hall current (I_{Hall}) is also proportional to the external magnetic field (B_z), biasing current of the Hall plate (I_{Bias}) and magnetic resistance coefficient (β). This current, for the cross-shaped Hall plate, can be expressed as:

$$I_{Hall} = \frac{\beta B_z I_{Bias}}{1 - (\beta B_z)^2} \tag{2.6}$$

here, β is magnetic resistance coefficient in presence of a magnetic field and is calculated as:

$$\beta = \frac{R_{(B_z)} - R_{(B_z=0)}}{R_{(B_z=0)} B_z} \tag{2.7}$$

where $R_{(B_z=0)}$ and $R_{(B_z)}$ define the Hall plate resistance in absence and presence of an external magnetic field, respectively.

The higher resolution in the low magnetic fields is one of the benefits of the current-mode Hall sensors using high mobility plate. Another benefit is that by using current-mode approach, the number of terminals can be reduced. Therefore, in order to integrate, the ultimate miniaturization of the system will be easier. Due to the general trend in microelectronics towards miniaturization and thanks to these advantages, the current-mode Hall sensor is bound to become more popular in the future.

2.5 Magnetic Sensors Characteristics

In all applications of Hall magnetic sensors, such as positioning, current sensing, medical and proximity switching, the most important characteristics are magnetic sensitivity, offset-equivalent magnetic field, $1/f$ noise-equivalent magnetic field, signal-to-noise ratio (SNR) and linearity.

For an ac magnetic signal above the $1/f$ noise region, the signal-to-noise ratios of equivalent Hall plates in the voltage-mode and current-mode Hall sensor are similar [2]. For a DC and low frequency magnetic field, a voltage-mode Hall sensor in which the current spinning technique is applied, is capable of reducing the offset and $1/f$ noise. For the first time an equivalent technique applicable in the current-mode Hall sensor has been presented in [23] and will be thoroughly explained in the following.

2.5.1 Sensitivity

The magnetic sensitivity is influenced by the biasing conditions. In other words, the magnetic sensitivity of a voltage-biased Hall sensor is proportional to the product

(Hall mobility)×(bias voltage), whereas in current-biased Hall sensor it is proportional to the product (Hall coefficient/thickness)×(bias voltage). Thus current-biased Hall plates are not very temperature-dependence. Indeed, the proposed current-mode Hall sensor is a current-biased circuit and has much smaller temperature-dependent in compare to voltage-biased Hall sensor [2].

A detailed description of a voltage-mode Hall sensor can be found in [2] and [24]. Magnetic Hall sensors are biased in two alternative *voltage-mode* and *current-mode* schemes. In voltage-mode, a sensor is biased by a voltage (V_{bias}) or a current (I_{bias}) and in presence of a magnetic field, it generates a voltage (V_{Hall}) at the output. This V_{Hall}, as already mentioned in Eq. 2.2, for the bias current can be defined as

$$V_{Hall} = G\frac{r_H}{n.e.t} I_{bias} B \tag{2.8}$$

where n is the doping, r_H the Hall factor, G the geometrical correction factor of Hall voltage, e the elementary carrier charge, B external magnetic field and t is thickness of the sensor plate. By using $V = R_{in}.I$, the Hall voltage can be expressed in terms of the bias voltage [2]:

$$V_{Hall} = G\frac{w}{l}\mu_H V_{bias} B \tag{2.9}$$

here, μ_H and $\frac{w}{l}$ denote the Hall mobility of majority carriers and width-to-length ratio of the sensor plate.

In case of current-mode condition, the sensor is biased by current and when exposed to an external magnetic field, it produces an output current. This output current as already discussed, is called the *Hall current* that can be defined from Eq. (2.3).

The absolute sensor sensitivity efficiency for the translation of the magnetic field into the Hall voltage or Hall current, depends on the biasing conditions. It is described for voltage-mode by the sensitivity S_{A_V} with

$$S_{A_V} = \frac{V_{Hall}}{B} \quad [V/T] \tag{2.10}$$

whereas absolute sensitivity for current-mode is given by the sensitivity S_{AI} with

$$S_{A_I} = \frac{I_{Hall}}{B} \quad [A/T] \tag{2.11}$$

The relative sensitivity is defined as the ratio of the absolute sensitivity and a bias quantity (voltage or current). Table 2.2 shows the sensitivity equations for Hall magnetic sensors. Two equations are used to evaluate the performance of the voltage-mode Hall sensor. The first is the current-biased voltage-mode Hall sensitivity S_{V_I}, which is proportional to the sensor bias current, I_{bias}, the Hall voltage, V_{Hall}, and the applied perpendicular external magnetic field, B. The units are $V\ .\ A^{-1}.\ T^{-1}$ *(volt /(ampere . Tesla))*. The second equation describes the efficiency of a Hall device by its voltage-biased voltage-mode Hall sensitivity S_{V_V} in terms of *per tesla* $(V/(V.T)) = T^{-1}$. In this equation, V_{bias} denotes the supplied bias voltage. The voltage-biased voltage-mode sensitivity S_{V_V} can be defined by

Table 2.2 Sensitivity of Horizontal Hall Magnetic Sensors in Voltage-Mode and Current-Mode conditions

Mode	Sensitivity	Unit
Current-Biased Voltage-Mode	$S_{V_I} = \left\lvert \frac{V_{Hall}}{I_{bias} \times B} \right\rvert$	$[V/AT]$
Voltage-Biased Voltage-Mode	$S_{V_V} = \left\lvert \frac{V_{Hall}}{V_{bias} \times B} \right\rvert$	$[V/VT] = T^{-1}$
Current-Mode	$S_I = \left\lvert \frac{I_{Hall}}{I_{bias} \times B} \right\rvert$	$[A/AT] = T^{-1}$

$$S_{V_V} = \frac{S_{V_I}}{R_{in}} \tag{2.12}$$

The current-mode magnetic sensitivity is used to evaluate the performance of current-mode Hall sensors, which is defined as the third equation in Table 2.2. Here I_{bias} is the sensor bias current, I_{Hall}, the Hall current. In this way, the units are also defined *per tesla* $(A/(A.T)) = T^{-1}$ and are the same as in voltage-biased voltage-mode units.

Current-mode Hall sensors show better sensitivity compared to voltage-mode [7]. In order to show the efficiency of current-mode approach, a Wheatstone bridge model of cross-shape Hall sensor has been used. The applied magnetic field alters the current flow in the body sensor and this gives rise to a variation of the sheet to body resistance in the device. At the macro level we can model the sensor as a bridge of resistances as shown in Fig. 2.6. Four resistors model the DC electrical relationship between the input and output nodes. The applied magnetic field changes the value of resistors by ΔR_V, as shown in the figure.

Since the voltage-mode and the current-mode of operation define different boundary conditions, the magnetic field would affect differently the current flow in the device and, therefore, the bridge resistors variation. The study requires 2D simulations. Here, in order to obtain first approximation results we suppose the same resistor change in both modes of operation.

For the voltage-mode case (Fig. 2.6-a) it results

$$V_{O1} = \frac{V_{bias}}{2R}(R - \Delta R_V) \tag{2.13}$$

$$V_{O2} = \frac{V_{bias}}{2R}(R + \Delta R_V) \tag{2.14}$$

The differential Hall voltage is given by

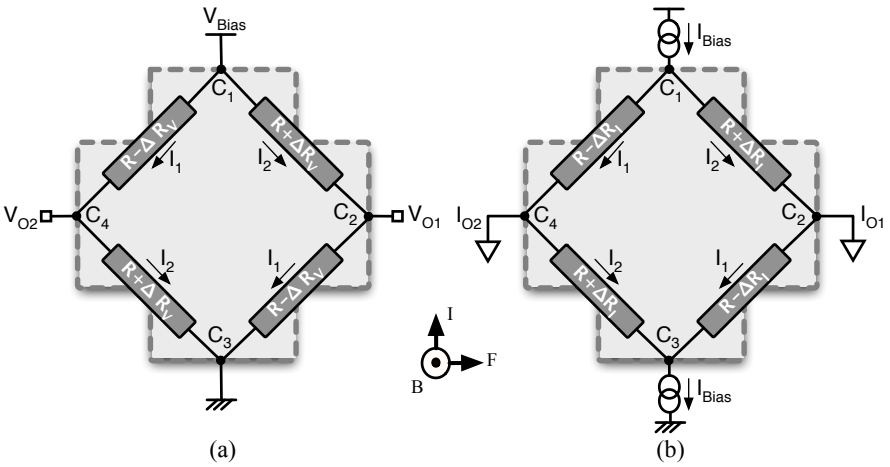

Fig. 2.6 Wheatstone bridge model of cross-shape Hall sensor in (a) voltage-mode and (b) current-mode configuration.

$$V_{Hall} = V_{bias} \frac{\Delta R_V}{R} \tag{2.15}$$

For the current-mode Hall sensors (Fig. 2.6-b) a bias current is injected into a terminal (C_1) of the Hall plate, and the same bias current is drawn from opposite terminal (C_3). The output terminals (C_2 and C_4) are at the same ground voltage. The differential output currents are given by

$$I_1 = \frac{V_{C1}}{(R - \Delta R_I)} \tag{2.16}$$

$$I_2 = \frac{V_{C1}}{(R + \Delta R_I)} \tag{2.17}$$

that yield the differential Hall current as

$$I_{Hall} = I_{bias} \cdot 2 \cdot \frac{\Delta R_I}{R} \tag{2.18}$$

Therefore, the sensitivity in the current-mode with equal change of the resistors in the model is twice larger than the voltage-mode. There is another side benefit in having current as output variable. Its integration over a capacitance for a defined period of time determines an output voltage with a gain factor proportional to the integration time. This is a simple way to amplify the signal by using a single fully differential operational amplifier.

A possible mismatch of the voltages of the output nodes causes an offset in the output signal. This limit can be compensated for by a suitable control in the electronic interface.

2.5.2 Offset

The offset of a Hall device is the output voltage when no magnetic field is present $V_{OS} = V_{out} \cdot (B = 0\ T)$. According to sensitivity (Table 2.2), the offset equivalent magnetic field, B_{OS}, is defined by

$$B_{OS} = \frac{V_{OS}}{Absolute\ Sensitivity} \quad [T] \tag{2.19}$$

For the direct measurement of this value, the sensor has to be put into a shielded region in order to exclude all present magnetic fields. The main causes of offset are related to a structural asymmetry of the active part (errors in geometry, non uniform doping density, contact resistance, etc.). Furthermore, the piezoresistance effect and alignment errors of the sense contacts influence offset value. The typical value of offset equivalent magnetic field for a Hall device fabricated in a silicon integrated technology is 5~50 mT [11].

In order to reduce the offset of the output signal, there are several techniques such as; orthogonal coupling of Hall devices and current spinning. The orthogonal coupling of Hall devices is based on pairing of an even number of Hall devices and biasing them orthogonally [25], as shown in Fig. 2.7(a) for two cross-shaped Hall plates [9]. The offset voltage is dependent on geometry of a Hall device, whereas, the Hall voltage and subsequently sensitivity are independent functions. As a result, the outputs of the devices can be connected so, that the respective Hall voltages are averaged while offset voltages are cancelled out.

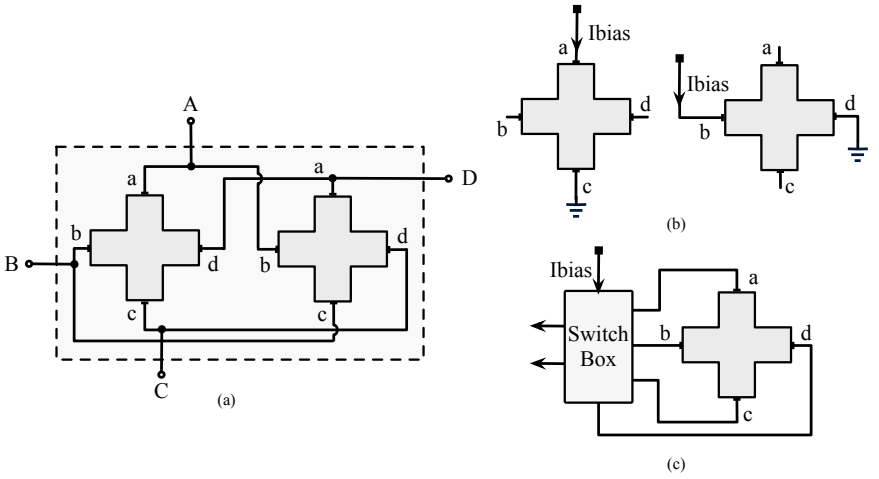

Fig. 2.7 (a) Orthogonal coupling of two cross-shaped Hall plates. (b) The biasing and sensing are altered using the symmetry of the Hall plate. (c) The current spinning technique: the biasing and sensing contacts are switched periodically in order to modulate either the Hall voltage or the offset [9].

In the following subsection, another method of offset voltage cancelation named *current spinning* technique is described. It is also known as the connection-commutation, switched Hall plate or dynamic method. The orthogonal coupling and current spinning technique can be combined in an array of Hall devices, as presented in [26]. The remaining offset after the offset reduction techniques are applied, is referred to as residual offset.

2.5.2.1 Current Spinning Technique

The spinning current technique allows to strongly reduce the offset of Hall sensors, [8]. The use of the symmetric Hall plate enables to apply the current spinning technique. As shown in Fig. 2.7(b), the current spinning interchanges periodically the output and supply terminals of the Hall plate so that the input bias injecting point is rotated in each state whereas the offset appears at the output terminals. The plate is clocked with several phases and the output signals are summed. Normally, the spinning switches for the periodic change of biasing and sensing contacts are known as the switch box, as shown in Fig. 2.7(c). Using this technique, the Hall plate offset can be reduced to about 50 ∼100 μT.

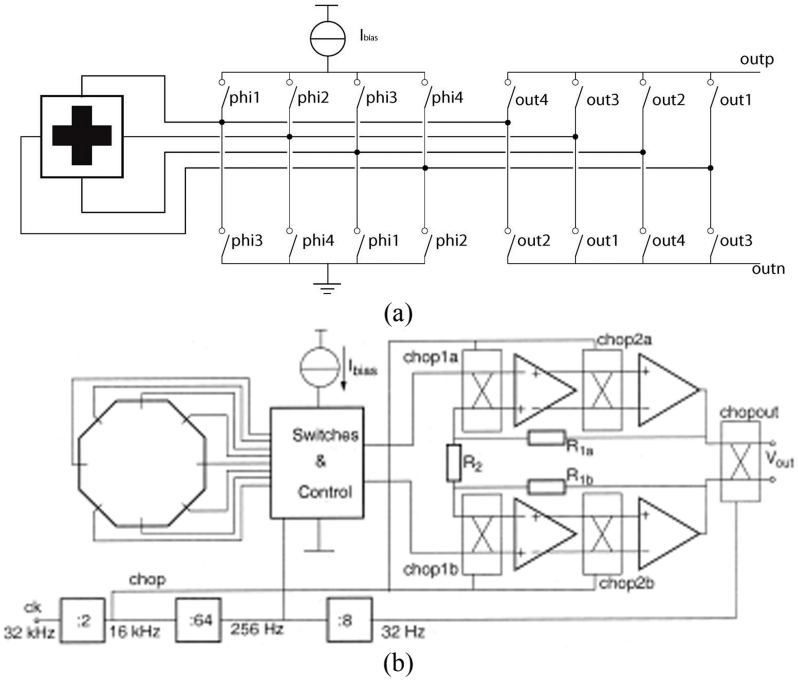

Fig. 2.8 (a) Applying the current spinning technique to 4-contact and (b) 8-contact horizontal Hall sensors (reprinted from [32] and [28]).

Depending on the number of different biasing phases there are a 2-phase spinning system using two different biasing states of the sensor, a 4-phase spinning using four phases, or even 8-phase spinning with eight biasing modes. Fig 2.8(a) shows an implementation of current spinning in a 4-contact Hall sensor with four phases, reported in [32]. Fig 2.8(b) illustrates an octagonal Hall plate that required the eight phases current spinning, reprinted from [28]. For CMOS integrated Hall plates, offset values of several hundreds of μT are generally reported for a 2-phase current spinning circuit. For 4-phases and 8-phases current spinning offset fields of 25 μT and 5 μT are reported in [32] and [28], respectively. In order to further reduce the offset of the Hall plate, four spinning-current Hall plates were orthogonally coupled to form a quad Hall plate structure in [7], as shown in Fig. 2.9. Orthogonally coupled Hall plates are parallel coupled Hall plates in both current supporting contacts and Hall voltage contacts; however, the current direction in the Hall plates differs by 90°. Such a structure instantaneously compensates for offset due to mechanical stress, and combined with the spinning-current method, reduces the offset to 3.65 μT.

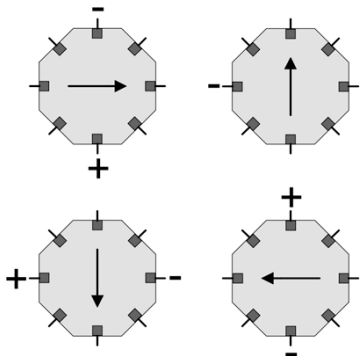

Fig. 2.9 Four phases of a quad current spinning Hall plate for reduce the offset (reprinted from [7]).

The current spinning technique can also compensate the 1/f noise of the sensor. Usually the switching frequency should be bigger than the noise corner frequency in order to obtain a good compensation of the 1/f noise.

The possibility to apply the current spinning to vertical Hall sensors has been reported in [29] and [31]. Fig. 2.10 shows the four phases for a 5-contact vertical Hall sensor, reprinted from [31]. Furthermore, the current spinning technique is used for current-mode vertical Hall sensors in [30] (see 4.2.3).

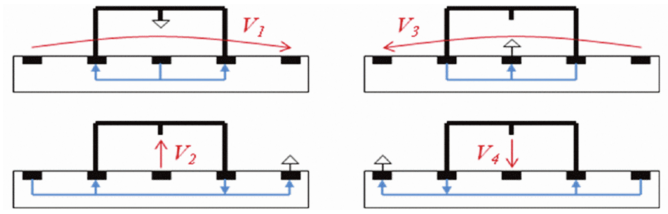

Fig. 2.10 Spinning-current technique applying to 5-contact vertical Hall sensor (reprinted from [31]).

2.5.3 Noise

The output voltage of a Hall sensor shows in general random fluctuations called noise. That means that a noise voltage V_N is superposed with the Hall voltage and sensor offset. The sensor output V_{out} becomes therefore

$$V_{out} = V_{Hall} + V_{off} + V_N \tag{2.20}$$

The noise in a Hall sensor is due to thermal noise, generation-recombination noise and 1/f noise [2]. The main sources of noise are internal, for example, resistance of the sensor is the source of *thermal Johnson noise* V_{nT} while semiconductor junction is the source of shot noise I_{ns}:

$$V_{nT} = \sqrt{4kTR\Delta f} \tag{2.21}$$

$$I_{ns} = \sqrt{2qI\Delta f} \tag{2.22}$$

where

k is the Boltzman constant and,

q is the electron charge [3].

Due to the fact that the noise depends on the frequency range Δf, usually the spectral density $S(f)$ of the noise is defined as

$$S(f) = \frac{V_n^2}{\Delta f} = (\frac{V_n}{\sqrt{\Delta f}})^2 \tag{2.23}$$

Therefore, a *unit* of noise can be determined as V^2/Hz, or a noise equivalent magnetic field as $nT/\sqrt{Hz}$.

A convenient way to describe the noise properties of a magnetic sensor is in terms of resolution, which is also called detection-limit. A high resolution can be achieved in a large Hall device made of high-mobility material and low 1/f noise parameter when it operates at high power level.

More details of these noise sources, which can be minimized with good laboratory practice and experiment design or through suitable compensation techniques, are described in Appendix A.

2.5.4 NonLinearity

Magnetic Hall sensors show an almost linear response for magnetic fields up to 1 Tesla. The nonlinearity describes the real measurement result deviation from the best ideal linear fit. It is used to evaluate the accuracy of the sensor. A good review of nonlinearity problems on Hall sensors is given in [33] and [34].

The nonlinearity in the Hall sensors is due to current-related sensitivity, material non-linearity, geometrical nonlinearity and nonlinearity caused by the junction field effect. The current-related nonlinearity will appear in a magnetic sensor if its sensitivity depends on the magnetic field. The junction field effect non-linearity depends on the device structure, on the biasing conditions and the magnetic field [13].

The nonlinearity error (NLE) in the voltage-mode Hall sensor is also defined as

$$NLE_V = \left| \frac{V_{Hall} - V_{Hall}(0)}{V_{Hall}(0)} \right| \times 100\% \tag{2.24}$$

where V_{Hall} is the measured value of the Hall voltage and $V_{Hall}(0)$ is the calculated value based on the slope of the straight line obtained by the best fit to the output characteristic.

In the same way, the nonlinearity error (NLE) in the current-mode Hall sensor can be specified as

$$NLE_I = \left| \frac{I_{Hall} - I_{Hall}(0)}{I_{Hall}(0)} \right| \times 100\% \tag{2.25}$$

where I_{Hall} is the measured value and $I_{Hall}(0)$ is the calculated value of the Hall current.

2.6 State-of-the-art in CMOS Hall Magnetic Sensors

Hall effect sensors have been the workhorse magnetic sensor for decades. Over the last few years two major achievements were carried out in the development of Hall sensors in CMOS technology: increase of magnetic sensitivity and reduction of offset. Therefore, the future of the Hall devices will depend on the *sensitivity improvement* and *offset reduction*. These two achievements are discussed in detail for vertical and horizontal Hall magnetic sensors in this section.

2.6.1 Sensitivity Improvement

The sensitivity performance of vertical and horizontal Hall sensor has already been explained in 2.5.1. In horizontal Hall sensors, current-biased voltage-mode sensitivities (S_{V_I}) range from $150 \sim 400\ VA^{-1}T^{-1}$, while typical voltage-biased voltage-mode sensitivities (S_{V_V}) are $2.5 \sim 5\ \%T^{-1}$.

On the other side, vertical Hall sensors presented in literature exhibit current-biased voltage-mode sensitivities (S_{V_I}) ranging from $100 \sim 400\ VA^{-1}T^{-1}$, and typical voltage-biased voltage-mode sensitivities (S_{V_V}) are $1 \sim 4\ \%T^{-1}$, all of them dealing with voltage as output quantity.

Various geometries of CMOS horizontal and vertical Hall devices have been studied and investigated for increasing the sensitivity, such as [14], [15], [16], [17] and [18] for the horizontal case, and 3-contact four-folded [20], 4-contact (4C) [22], 5-contact (5C) [8], 6-contact (6C) [10] and [21] for vertical Hall devices. Table 2.3 summarizes the sensitivity performances for state-of-the-art Hall devices.

Table 2.3 Sensitivity Comparison of Horizontal and Vertical Hall Magnetic Sensors

Reference	Sensor Type	Sensor Plate	Sensitivity [%T]
[14]	Horizontal	Five Strips	4.6
[15]	Horizontal	N-well and MOS	3
[16]	Horizontal	N-well Resistor	2.5
[17]	Horizontal	N-Well	2.9
[18]	Horizontal	Octagonal	4.5
[19]	Vertical	5-Contact	1.52
[20]	Vertical	3C Four-Folded	1.72
[21]	Vertical	2D 5-Contact	4.3
[10]	Vertical	5-Contact	4

2.6.2 Offset Reduction

Already in 2.5.2.1 some of state-of-the-art works that use the current spinning technique in order to achieve offset reduction have been discussed. The offset of a Hall effect magnetic sensor system is the sum of the uncanceled offsets of a Hall device and the signal conditioning electronics. The typical offset equivalent magnetic field of a Hall device realized in silicon integrated technology is $5 \sim 50$ mT. It can be reduced by some techniques, such as current spinning, to lower than 100 μT.

Table 2.4 Offset Comparison of Horizontal and Vertical Hall Magnetic Sensors

Reference	Sensor Principle	Offset [μT]
[32]	Orthogonally parallel	25
[7]	Four orthogonally coupled	3.65
[36]	Five-octagon IMC	10
[37]	Two pairs of orthogonally coupled	<200
[38]	Differential Hall probes	10

Table 2.4 summarizes and compares most low-offset CMOS Hall sensors reported in literature. In [32], sensor offset has been canceled before amplification by means of a triple ripple reduction loops (RRL) scheme. The offset of Hall-plates in [7] is reduced to the 10 μT level by the current spinning method and is also instantaneously reduced by orthogonally coupling four Hall-plates. Again in [36], by the current spinning principle, the signal voltage is separated by the offset voltage through modulation. Therefore, Hall plate offset and amplifier offset are suppressed. Chopping techniques and current spinning have been also used in [37] to reduce the influence of the undesired offset. A current spinning Hall scheme and analog chopping is used in [38] to reduce the offset.

2.7 Applications of Hall Magnetic Sensors

Sensing the presence or position of an object are two of the most widespread applications in which Hall sensors are used [39]. Magnetic field sensors are well suited to this kind of application. In the following, a number of ways to use Hall magnetic sensors to perform a sensing function will be discussed.

One of the major drivers in this market is the increasing usage of magnetic sensors in automotive and electronic compasses. The Automotive and Electronics industries are the largest end-users of magnetic sensors. Magnetic sensors provide safety as they are used in power trains, air bags, air pressure controls, and fuel systems. The increasing demand for smartphones and tablets also has a positive impact on the market [47].

In this Section, a few examples of Hall magnetic sensors are presented such as biosensors, contactless current sensors, angular position sensor, linear position sensor, contactless joystick sensor, electronic compass, speed and timing sensors and specific sensors. More information on the most important application can be found in the literature of the providers of Hall magnetic sensors. Practically all manufacturers of Hall sensors (Asahi Kasei Microsystems of Japan, Massachusetts-based Allegro Microsystems, Infineon Technologies of Germany, Micronas of Switzerland, and Belgium-based Melexis) offer a large variety of applications [42–46].

Biosensors

Magnetic Hall sensors are suitable for integration and scaling in CMOS technology, and hence, enable very compact and low cost systems. Magnetically labeled bioassays are therefore a promising approach for addressing the requirements and growing need of point-of-care diagnosis [17]. Fig. 2.11 shows the cross section of a magnetic bead sensor plate which is used for detecting the magnetic labels.

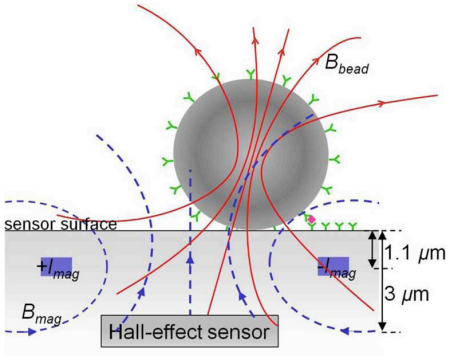

Fig. 2.11 Cross section of a label detector using CMOS magnetic Hall sensor (reprinted from [17]).

For measuring magnetic field produced by electro- and permanent magnets, in the range of $10^{-4}\mu$T to a few tens of tesla, Hall sensors are typically used [2]. For example they are used to test the electro-magnets applied in particle accelerators, nuclear magnetic resonance (NMR) imaging systems and NMR spectroscopy systems.

Contactless Current Sensors

Measuring and sensing electrical current can be done indirectly, by measuring the magnetic field associated with the current flow. The main advantage of magnetic current sensing is that it doesn't interfere with the circuit in which the current is being sensed [39].

A basic configuration of a contactless current Hall effect sensor has been shown in Fig. 2.12. The three Hall effect based technologies have been used for AC and DC current measurement. First, open-loop Hall effect transducers use a Hall sensing plate placed into the air gap of a magnetic circuit. The second technology is based on the close-loop current sensing. The difference between the open-loop and the closed-loop current transducers is that the latter has a built-in compensation circuit which improves performance. Finally, Hall effect ETA transducers employ a combination of open-loop and closed-loop technologies. At low frequencies (2-10 KHz) they

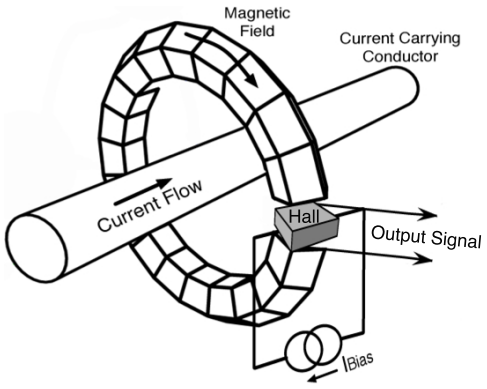

Fig. 2.12 Basic configuration of a contactless current Hall effect sensor.

work as open-loop transducers, thus the Hall plate is providing a signal proportional to the primary current to be measured. At high frequencies they work as current transformers. These signals are electronically added in order to form a common output signal [4].

Contactless Angular, Linear and Joystick Position Sensors

Fig. 2.13(a) shows an angular position sensor (also referred to as a rotary sensor) that measures the relation by which any position with respect to any other position is established. It calculates the orientation of an object with respect to a specified reference position as expressed by the amount of rotation necessary to change from one orientation to the other about a specified axis. The magnetization of the magnet is perpendicular to the axis and parallel with the sensor plane. With a rotation of the axis the flux density vector rotates in the sensor plane and the output signal of the two sensor axes X and Y yields a sine and consine signals with the rotation [1].

For linear position measurement, the two-axis Hall sensor is combined with a magnet which is now magnetized orthogonally to the sensor plane Fig. 2.13(b). The magnet is now shifted parallel to one axis at a certain distance above and sideways of the sensor. This again leads to a sine a co-sine reading of the direction of the field angle. The ratio of both values is directly proportional to the magnet position [1].

By using all three magnetic field sensitive axes, a contactless magnetic joystick can be implemented, as shown in Fig. 2.13(c). The two tilt angles in the XZ and YZ planes can be computed very accurately by using all three mangnetic field components. Here again, the position information is derived from the ratio of magnetic field components, so that temperature and ageing drift of magnet and sensor are cancelled out [1].

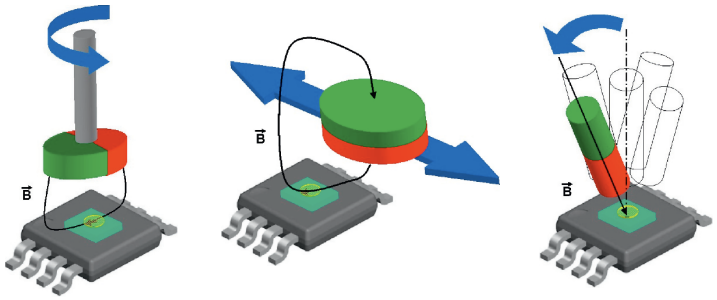

Fig. 2.13 (a) Magnetic contactless angle sensor, (b) magnetic contactless linear position sensor and (c) contactless magnetic joystick (reprinted from [1]).

Electronic Compass

The Earth's magnetic field intensity is about 50 μT and has a component parallel to the Earth's surface that always points towards the magnetic north Earth's. This is the basis for all magnetic compasses.

Nowadays, various types of technologies are applied to electronic compasses, and they are based on the magneto-resistive [e.g., anisotropic magnetoresistance (AMR) or giant magnetoresistance (GMR)] effect, the fluxgate effect, or on the magneto-impedance (MI) effect in zero-magneto-strictive amorphous wires. Although these sensors are more sensitive and temperature-stable with higher bandwidth, they either require a lot of power or a very delicate post-processing of the ferromagnetic core. In [36] a Hall-IMC compass is presented that combines the advantages of simple post-processing and low-power consumption, as shown in Fig. 2.14. For realizing this compass, four Hall plates have been used simultaneously and their outputs are added in an amplifier.

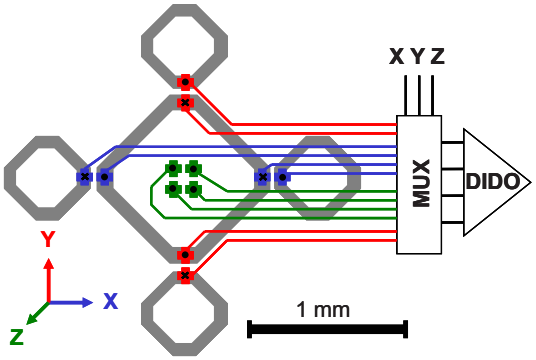

Fig. 2.14 Entire IMC structure and Hall plates (reprinted from [41]).

Speed and Timing Sensors

The ability to measure the speed or position of a rotating shaft is necessary for the proper function of many types of machinery. Hall sensors are commonly used to time the speed of wheels and shafts, such as for internal combustion engine ignition timing, tachometers and anti-lock braking systems (ABS) [39].

Specific Sensors

Some of the Hall sensors are used as application-specific sensors. For example, Melexis designed a Hall IC to provide control and power-driver functions for a small brushless DC motor. This type of motor is commonly used in the cooling fans found in virtually all personal computers. Fig. 2.15 shows a typical DC brushless fan which is disassembled to expose the motor, Hall sensor and drive electronics [39]. The Hall sensor is also used in the brushless DC motor to sense the position of the rotor and to switch the transistor in the right sequence.

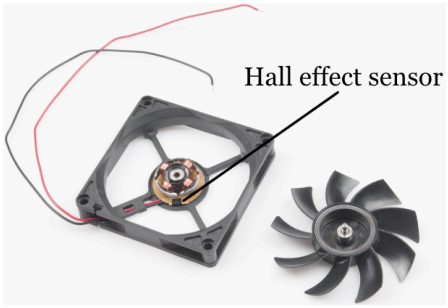

Fig. 2.15 DC brushless fan using Hall effect sensor.

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Chapter 3
Current-Mode Horizontal Hall Magnetic Sensors

Abstract In this chapter a horizontal magnetic Hall sensor working in current-mode is presented. The proposed sensing device is composed by two Hall plates able to provide a differential current at the output nodes, as shown in the first part. The purpose of the second part is an implementation of the twin horizontal sensor device, sensor biasing circuit and proper common-mode feedback (CMFB). The current spinning technique and carrying out of the related switches are then described. The chapter ends with the simulation and measurement results of the fabricated sensor in a standard 0.18 μm CMOS technology.

3.1 Proposed Architecture

The magnetic Hall sensor system includes the Hall plates, as well as the digital and analog electronics parts which are needed for generating selected useful information from the applied magnetic field. In other words, the Hall plates sense the magnetic field and produce an electrical signal.

In most of Hall sensors, the output electrical signal is voltage. As mentioned in 2.4, this kind of Hall sensors is called voltage-mode. This means that the magnetic field to be measured is converted into an output voltage. This output voltage is typically in the order of microvolts to millivolts and must be amplified before being transmitted to the outside world. Typical amplification of a factor of 1000 is performed by a chain of amplifiers which are directly integrated on the same silicon surface with the Hall plates [1]. All circuitry for magnetic field sensing, amplification, analog and digital control unit are implemented in the same chip. More information about conventional voltage-mode Hall sensors is presented in [2–6].

As an alternative solution, an Hall sensor can work in current-mode. The output is current and not voltage. In the current-mode Hall sensors, there is no variation between the terminal potentials and so any influence of the parasitic capacitances. Also as already mentioned in chapter 2, it is possible to use a smaller number of terminals, therefore the ultimate miniaturization of the device is easier [2].

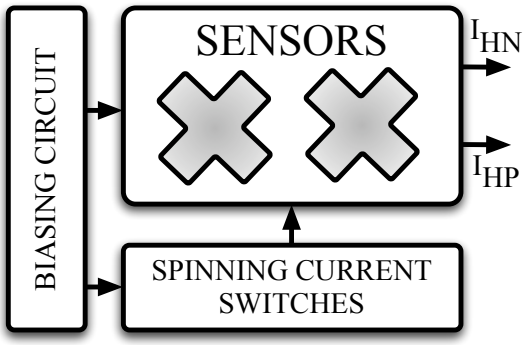

Fig. 3.1 Block diagram of the proposed magnetic current-mode Hall sensor.

This chapter presents a low power current-mode Hall sensor microsystem with differential output current, as shown in Fig. 5.2. The system comprises a twin horizontal Hall sensor biased by a current I_{Bias}. The switch box implements the current spinning technique. The differential output current level is typically within nanoamper to milliamper range, depending on the bias current. The physical structure of the proposed current-mode Hall sensor is the same of existing devices, with the same possibility of compensating for the offset caused by mismatch (current spinning, see 2.5.2). The difference is in the way the bias is provided and the output signal is extracted. Extensive and accurate physical simulations and behavioral models of the current-mode Hall sensors allowed to optimize its size, shape and performance for the chosen technology, a standard 0.18-μm CMOS technology. The offset at the output terminals of the sensors is reduced to less than 50 μT by spinning current technique and measurement results show good sensitivity better than 2 $\%T^{-1}$ for magnetic fields in the range from 0 to 10 mT, as shown in Section 3.3. The circuit operates properly with a bias current as low as 12 μA. The benefit of having current at the output is that the current integration over a defined time period determines an output voltage with a gain proportional to the integration time.

As the signal level at the output of the sensor is very low, it requires additional amplification and signal processing circuitry. The Hall system is integrated with a readout circuit on a single chip to increase the magnetic sensitivity. The readout interface for magnetic sensors are described in detail later in Chapter 5.

3.2 Implementation

The main implemented blocks of proposed Hall microsystem are explained in this Section. Starting from key features of the twin cross-shaped Hall plate, the transistor-level design of the biasing circuit and common mode feedback (CMFB) are indicated and further current spinning switches are presented.

3.2.1 Horizontal Current-Mode Hall Sensor Devices

Several current-mode Hall structures have been modeled and evaluated with respect to noise, offset and sensitivity using COMSOL Multiphysics™ and Verilog-A [7]. The cross-shaped model is the optimum plate structure to fit the lowest noise and residual offset and the best sensitivity. In addition, the symmetrical cross-shaped Hall plate grants high sensitivity and immunity to alignment tolerances resulting from the fabrication process. The use of the symmetrical cross-shaped Hall plate and the proposed current-mode approach enables to easily apply the current spinning as already discussed in 2.5.2.1. Fig. 3.2 shows the four states of input and outputs for each 90° rotation. From the bottom figure it can be also observed the output offset of Hall plate during the four states. After the fourth phase, it is expected that the average of the offset will be zero.

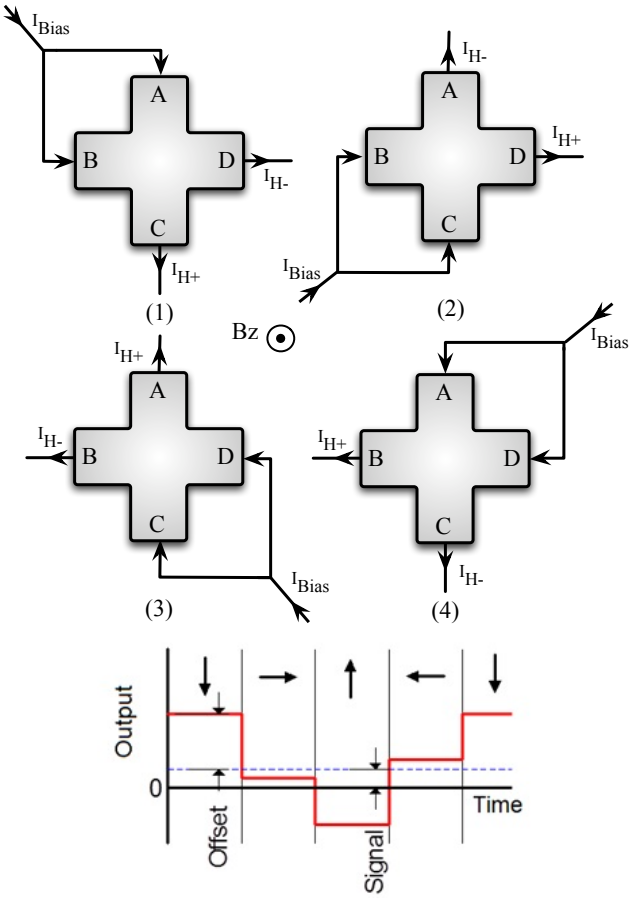

Fig. 3.2 Spinning current technique and output offset of a single cross-shaped Hall plate during four states.

Table 3.1 summarizes the four phases of the current spinning operation. At the beginning, the bias current is injected into terminals A and B (phase 1). During phase 2, after 90° rotation, the bias current is injected into B and C terminals and so on for other phases.

Table 3.1 Four phases for spinning current method.

Current	Phase1	Phase2	Phase3	Phase4
I_B	A,B	B,C	C,D	D,A
I_{H-}	D	A	B	C
I_{H+}	C	D	A	B

A low doped N-well makes the Hall plates. In order to reduce the flicker noise and surface carrier losses, a shallow highly doped P^+ conductive top layer covers the surface of the active area. The four contact regions in the N-well diffusion are N^+ highly doped. Fig. 3.3 shows the model geometry of the cross section view and top view of the Hall plate in a CMOS technology.

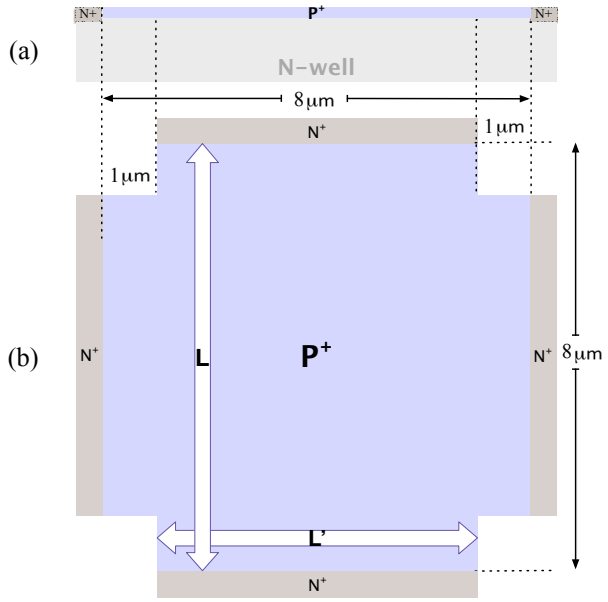

Fig. 3.3 Model geometry of a cross-shaped Hall plate in a CMOS technology: (a) cross view and (b) top view.

According to Fig. 3.3 top view: the maximum width and length of each plate is 8 µm. The cross section figure shows the depth of the N-well is 1.4 µm while N^+ thickness is just 0.25 µm. This CMOS technology uses the doping concentration of

$> 10^{18} cm^{-3}$ for the P^+ layer, $5 \times 10^{17} cm^{-3}$ and $> 10^{20} cm^{-3}$ for N-well and N^+ layers respectively. The metal-1 to N-well via is carried out as contact.

The horizontal device of Fig. 3.3 operating in the current-mode has been studied in [7]. The obtained sensitivity for doping and carrier mobility fitting a conventional 180 nm CMOS technology is $S_I = 3.5\% T^{-1}$, 24% larger than its voltage-mode counterpart. This improvement depends on the different boundary conditions established by the output terminal voltage. Other physical configurations and mode of operation can further increase the sensitivity. Several different solutions have been studied in order to increase the sensitivity. Among them, the most promising is based on a twin cross-shaped Hall sensor. The solution of Fig. 3.4 depicts a twin cross-shaped sensor: the current enters into two shorted terminals of a cross shaped sensor and exits from two shorted terminals of the second sensor. This solution is suitable for the current spinning technique, normally used for compensating the static mismatched of the device.

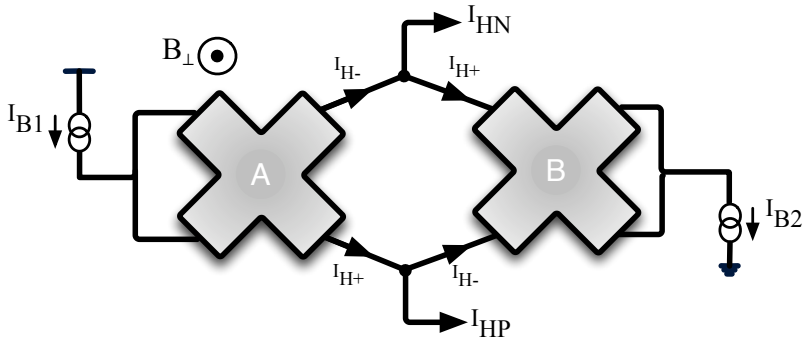

Fig. 3.4 Proposed twin current-mode Hall sensor structure.

In this condition, with zero magnetic field, the sensor structure is balanced, thus making null the output currents, I_{HN} and I_{HP}. An external magnetic field unbalances the sensor, providing two Hall currents, I_{Hall}, at the output nodes. The Hall current, for a cross-shaped Hall plate in presence of an external perpendicular magnetic field $B_\perp$, can be expressed as

$$I_{Hall} = \frac{\beta B_\perp I_{bias}}{1 - (\beta B_\perp)^2} \tag{3.1}$$

where β is the magnetic resistance coefficient in presence of a magnetic field. It is defined as

$$\beta = \frac{R_{(B)} - R_{(B=0)}}{R_{(B=0)} B_\perp} \tag{3.2}$$

where $R_{(B=0)}$ and $R_{(B)}$ define the Hall plate resistance in absence and presence of an external magnetic field, respectively.

The output currents of each Hall plate, I_{H+} and I_{H-} in Fig. 3.4, are

$$I_{H+} = \frac{I_{bias}}{2} + \frac{I_{Hall}}{2} \tag{3.3}$$

$$I_{H-} = \frac{I_{bias}}{2} - \frac{I_{Hall}}{2} \tag{3.4}$$

In the proposed configuration, the use of a couple of Hall plates makes the sensor output currents, I_{HP} and I_{HN}, which are the difference of the output currents of each Hall plate. Using equations (3.3) and (3.4), the sensor output currents are given by

$$I_{HP} = I_{H+} - I_{H-} = I_{Hall} \tag{3.5}$$

$$I_{HN} = I_{H-} - I_{H+} = -I_{Hall} \tag{3.6}$$

For the used configuration, the difference of the output currents is twice the Hall current ($2 \times I_{Hall}$), thus doubling the sensor sensitivity with respect to conventional implementations.

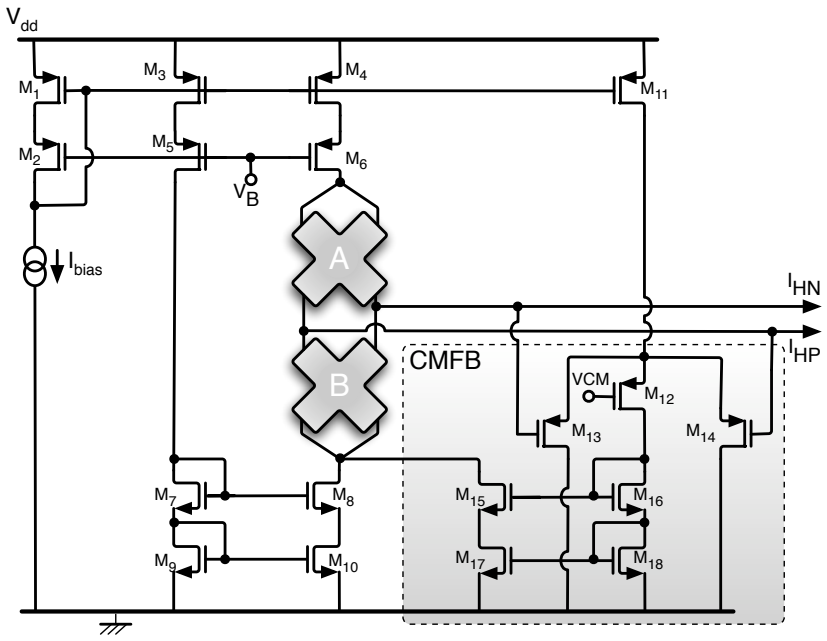

Fig. 3.5 Schematic diagram of Hall plates with biasing and common mode feedback circuit.

3.2.2 Sensor Biasing Circuit

The sensor structure of Fig. 3.4 for bias uses two current generators which are nominally equal. A possible mismatch brings the current generator with the larger value to the triode region. This forces the use of a feedback control to make the two current generators equal. Fig. 3.5 shows the used circuit. The P-channel cascode current mirror replicates the bias current, I_{bias}. A second N-channel cascode mirror gives rise to the sink current. Its value is systematically less than the required current to leave some room for the common mode control. This current is regulated by means of the common mode feedback (CMFB) realized with the P-channel differential pair M_{13} - M_{14}. The current flowing in M_{12} (mirrored by $M_{15} \sim M_{18}$) makes the common mode voltage at the output of the sensor equal to VCM, thus ensuring that the drain and sink bias currents are equal.

3.2.3 Current Spinning Switches

Since the output offset strongly limits the DC resolution of the sensors, the use of the crossed-shaped Hall plate enables the current spinning technique, [8], to reduce offset and $1/f$ noise.

The output and supply terminals of each Hall plate are periodically interchanged so that the input bias current polarity is rotated in each position whereas the offset appears at the output terminals. The plates are clocked with four phases. At the end of a complete spinning operation, the average of offset becomes zero.

Fig. 3.6 shows the sensor and switches configuration driven by the four phases whose time diagram is given in Fig. 3.7. During each phase, Φ_1, Φ_2, Φ_3, and Φ_4, for each plate two terminals are connected to I_{bias} while the remaining two are the outputs. The implementation uses 32 switches, each of them being a complementary CMOS pair.

3.3 Simulation and Measurement Results

Single Horizontal Cross-Shaped Hall Plate

The current-mode technique has been applied to a two-dimensional model of the Hall plate simulated in COMSOL Multiphysics, with parameters summarized in Table 3.2. Fig. 3.8 shows the model geometry of the single Hall plate: the maximum width and length is 8 μm. The figure also shows the surface electrical distribution when a magnetic field of 20 mT is applied. The simulation uses the nominal bias current of 12 μA injected in terminals A and B, which show a higher value of surface electrical potential in red colour. The model geometry of the Hall plate has been

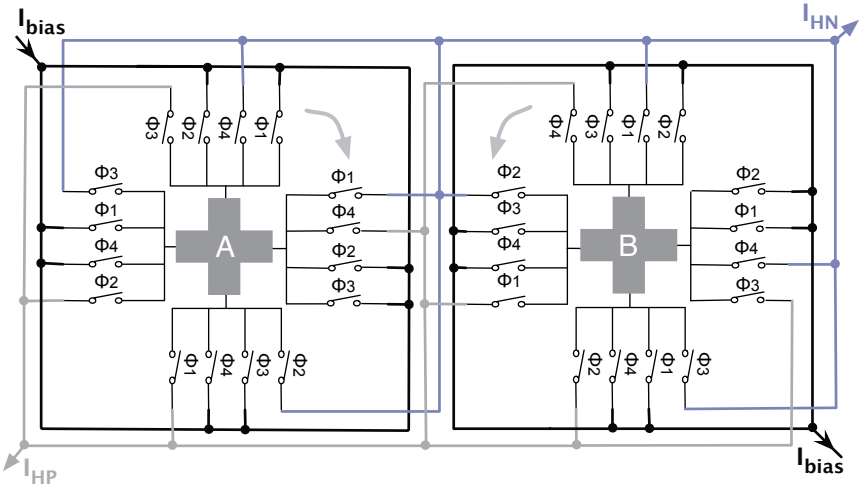

Fig. 3.6 Hall plates with switches configuration for current spinning.

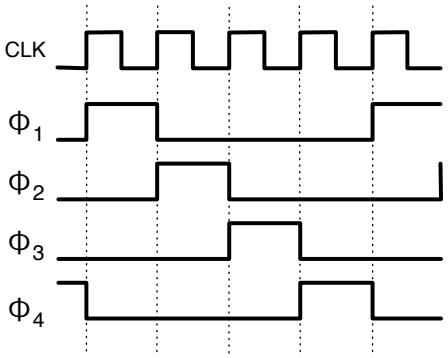

Fig. 3.7 Phases timing diagram for current spinning operation.

simulated both without any mismatch and with mismatch. Simulation results are summarized in the following.

First consider the cross-shaped Hall plate without any mismatch. Fig. 3.9 shows the simulated input and output currents of the Hall plate. The solid line shows the input currents of terminals A and B (equal to 6 μA) while the dash-dotted and the dotted lines represent the output currents at terminals C and D. These output currents increase and decrease, respectively, by changing the magnetic field within the 0 to 20 mT range. Since there is no mismatch in the Hall plate, the output currents are completely symmetric.

Table 3.2 Model Parameters

Symbol	Value	Parameter
q [C]	$-1.602e-19$	Electron Charge
n [cm^{-3}]	$-2.6e16$	Doping
μ [cm^2/Vsec]	1200	Mobility
sigma0 [S/m]	-q*n*μ	Silicon Conductivity
R_h [m^3/C]	$-1/(q*n)$	Hall Coefficient
B_z [mT]	$0-20$	Magnetic Field
V_0 [V]	0.02	Applied Voltage
t_si [m]	$0.3e-6$	Silicon Tickness
I_0 [μA]	12	Input Current

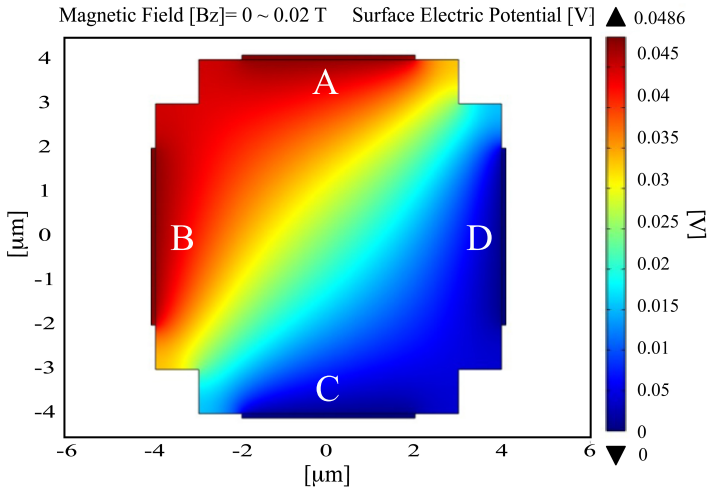

Fig. 3.8 COMSOL simulation results of a single current-mode cross-shaped Hall sensor.

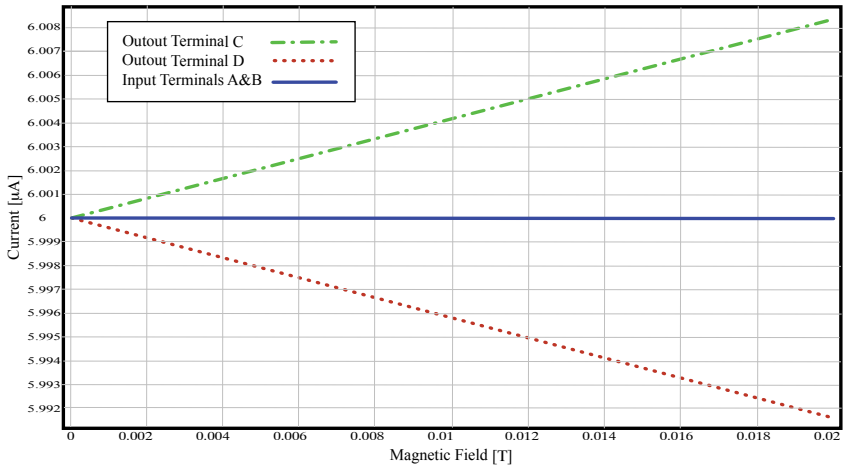

Fig. 3.9 Simulated input and output currents of the current-mode Hall plate without any mismatch.

Table 3.3 summarizes the simulation results plotted in Fig. 3.9. The maximum differential output current is 13.3 nA for a magnetic field equal to 20 mT. These current levels are pretty small, but the output signal can be increased by integrating the current signal over a given period of time.

Table 3.3 Simulation results of the current-mode Hall plate without mismatch.

Magnetic Field	**Current**		
B_z [T]	$I_A + I_B$ [μA]	I_C [μA]	I_D [μA]
0	12	6	6
0.001	12	6.00033	5.99967
0.002	12	6.00067	5.99933
0.003	12	6.001	5.999
0.004	12	6.00133	5.99867
0.005	12	6.00166	5.99834
0.006	12	6.002	5.998
0.007	12	6.00233	5.99767
0.008	12	6.00266	5.99734
0.009	12	6.00299	5.99701
0.01	12	6.00333	5.99667
0.011	12	6.00366	5.99634
0.012	12	6.00399	5.99601
0.013	12	6.00432	5.99568
0.014	12	6.00466	5.99534
0.015	12	6.00499	5.99501
0.016	12	6.00532	5.99468
0.017	12	6.00565	5.99435
0.018	12	6.00599	5.99401
0.019	12	6.00632	5.99368
0.02	12	6.00665	5.99335

Mismatch in Hall plate dimensions due to possible mask misalignment during fabrication limits accuracy and causes offset in the output signal. Fig. 3.10 shows the average of output currents of the Hall plate after current spinning as simulated in COMSOL. Simulations include a 0.01-μm mismatch in the C terminal of the Hall plate.

From Fig. 3.10 it can be noted that, at the end of complete spinning and averaging of four phases (as shown with the green solid line), the offset for a zero magnetic

field is eliminated. When increasing the magnetic field from 0 to 20 mT, the positive output (I_{H+}) rises and the negative output (I_{H-}) decreases.

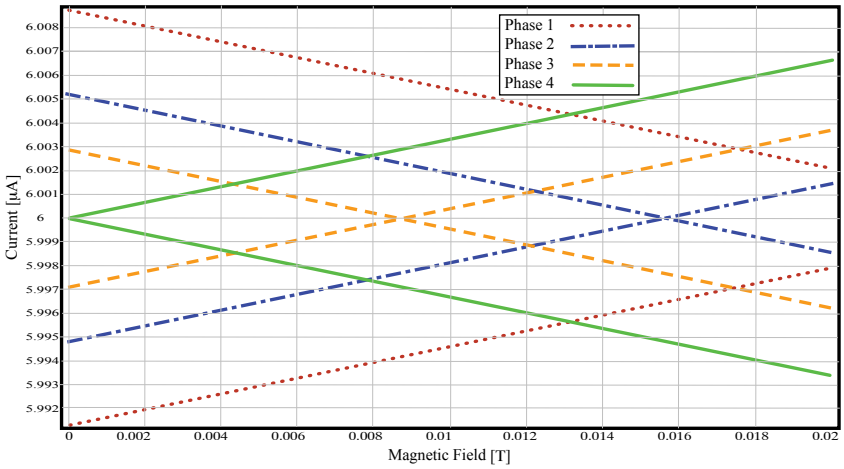

Fig. 3.10 Simulated average output currents (I_{H+} and I_{H-}) of current-mode Hall sensor plate with mismatch after the current spinning method.

The Hall plate has been modeled and described using Verilog-A language so that it can be simulated in the Cadence environment, as well [9].

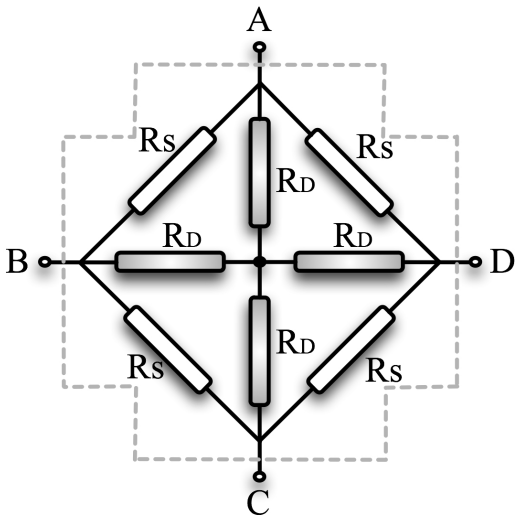

Fig. 3.11 The 8-resistors model implemented in Verilog-A using eight resistors.

Fig. 3.11 shows the 8-resistors Hall plate model. It includes four electrical terminals (A, B, C and D) and eight resistors (four side resistors, R_S, and four diagonal resistors, R_D). The values of these resistors are controlled by three parameters: the external magnetic field, the initial value of resistors, R_0, and the magnetic resistance coefficient, β. The extraction of parameters from device simulations is as follows. The initial value of resistors, R_0, is obtained in two steps. The first step consists of grounding terminals C and D and applying 12 μA to terminals A and B. In the second step, terminals B and D are grounded and the current is applied to terminals A and C. The magnetic resistance coefficient, β, is defined as the average of the initial values of resistors, R_0, in presence and absence of the magnetic field.

Table 3.4 Comparison between the simulations of the Hall plate in COMSOL and Verilog-A

Magnetic Field	**COMSOL**		**VERILOG-A**	
B_z[mT]	I_D[μA]	I_C[μA]	I_D[μA]	I_C[μA]
0	6	6	6	6
10	6.0033	5.99667	6.003373	5.996627
20	6.00665	5.99335	6.006746	5.993254

In order to show the correctness and accuracy of this model, the simulation results have been compared with the ones achieved with the COMSOL model, as summarized in Table 3.4. I_C and I_D stand for currents of C and D terminals, respectively. The results are in excellent agreement with each other and the difference is less than 0.1%.

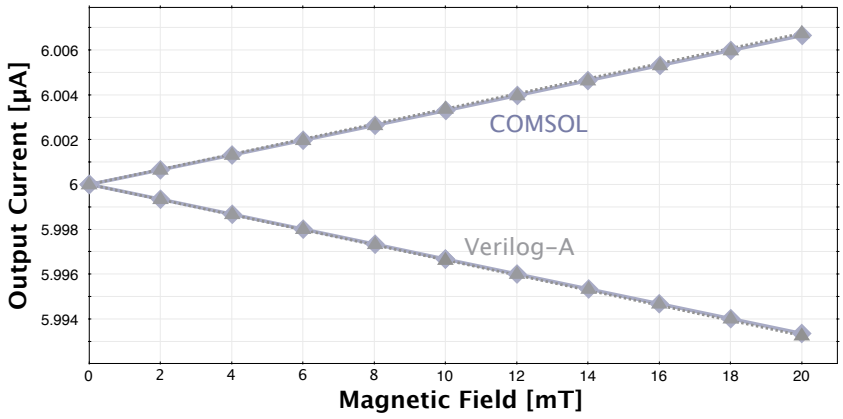

Fig. 3.12 Simulated output currents of the Hall plate in COMSOL and Verilog-A as a function of magnetic field.

Fig. 3.12 draws the simulated output currents of the Table 3.4. The simulations have been performed with 12 μA input bias current (injected in terminals A and B) while the magnetic field has been considered from 0 to 20 mT. The graph obtained from Verilog-A simulation is equal to the one achieved with COMSOL.

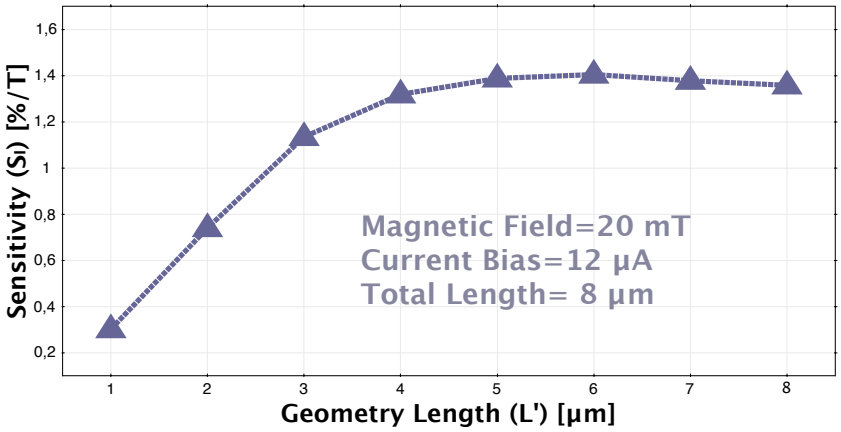

Fig. 3.13 Simulated sensitivity as a function of the Hall plate width.

The Hall current and, hence, the sensitivity depends on the geometry of the device and on physical parameters. It is given by

$$S_I = G\frac{r_H}{qnt} \tag{3.7}$$

where G is the geometry parameter, r_H the Hall factor, t the thickness of the sensor, and n the carrier concentration, [2].

COMSOL Multiphysics™simulations determine the optimal dimensions of the cross-shaped sensor. This study uses a total length of 8 µm and the inner square varying from 1 to 8 µm. Fig. 3.13 shows the results for a constant bias current of 12 µA and 20- mT magnetic field. The sensitivity goes from a minimum of 0.37%T^{-1} to an optimum value (1.42 %T^{-1}) for L' = 6 µm.

The sensitivity depends on temperature because the Hall factor r_H depends on temperature. This because of the variation of carriers concentration, n, and carriers mobility, μ, [10]. COMSOL Multiphysics™simulations verify the expected behavior, as Fig. 3.14 shows. The figure considers the relatively low temperature range, from −40 °C to +85 °C. Even for this simulation the bias current is 12 µA and the applied magnetic field is 20 mT. Since the sensitivity significantly changes above the room temperature, as it happens for all the Hall sensors, suitable correcting methods will be necessary.

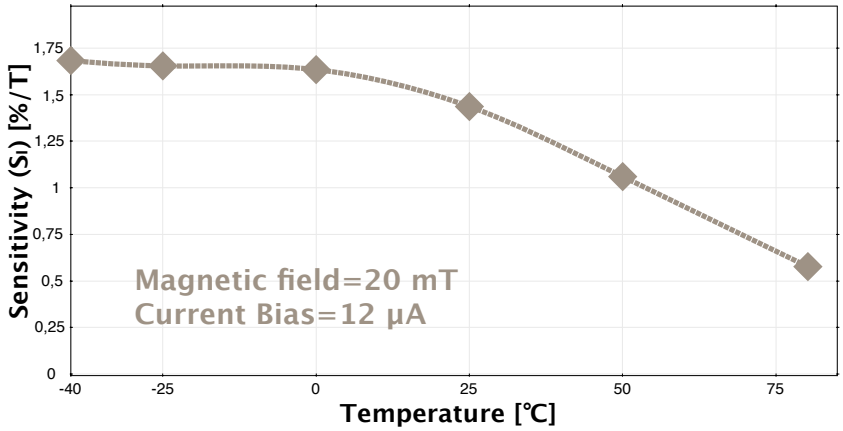

Fig. 3.14 Simulated sensitivity as a function of the temperature.

Twin Horizontal Cross-Shaped Hall Plate

As already presented in Fig. 3.4, the solution of Fig. 3.15 depicts a twin cross-shaped sensor in CMOS technology.

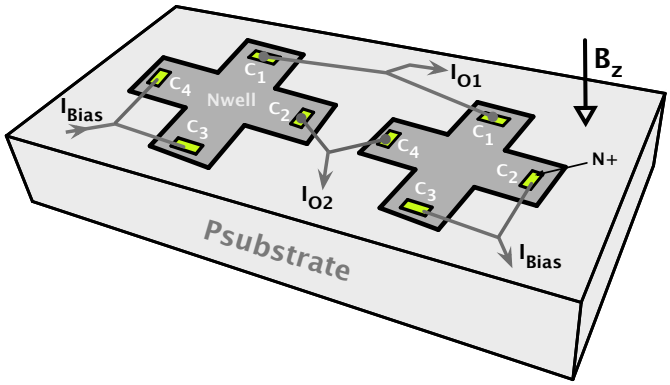

Fig. 3.15 Twin horizontal current-mode Hall device in CMOS technology.

The current enters into two shorted terminal of a cross shaped sensor and exits from two shorted terminals of the second sensor. The solution is suitable for the current spinning technique, normally used in order to compensate for the static mismatched of the device.

Fig. 3.16 shows the model geometry of the two Hall plates used in a COMSOL Multiphysics™ simulation: the maximum width and length of each plate is 8 µm. The figure shows the simulated surface electrical distribution and the current distribution when a perpendicular magnetic field of 20 mT is applied. The plot is for a

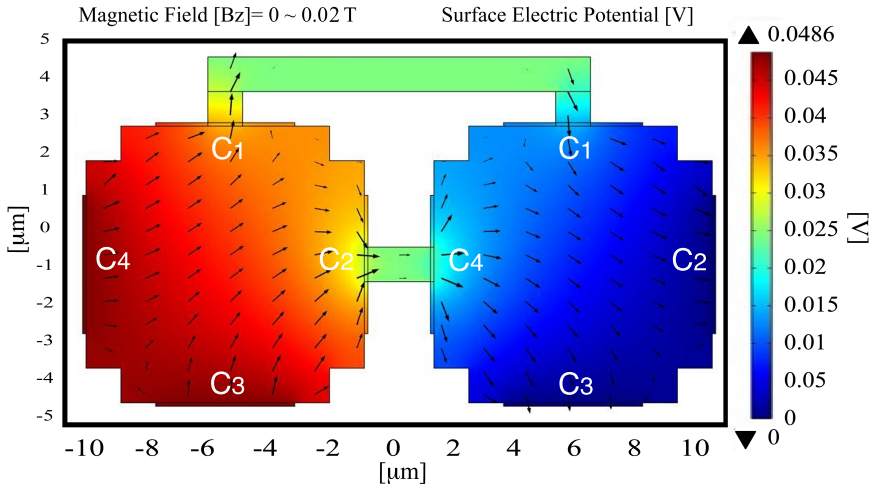

Fig. 3.16 COMSOL simulation results of a twin current-mode cross-shaped Hall sensor.

bias current of 12 µA injected in terminals C_3 and C_4 of the first plate and drained from terminals C_2 and C_3 of second plate.

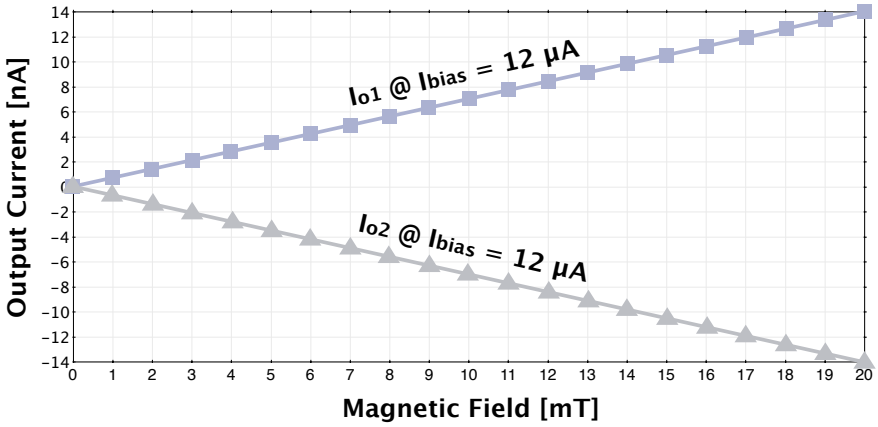

Fig. 3.17 Simulated output currents (I_{O1} and I_{O2}) of a cross-shaped current-mode horizontal Hall sensor as a function of the magnetic field at 12 µA bias current.

Fig. 3.17 gives the output currents, I_{O1} and I_{O2}, as a function of magnetic field at 12 µA. According to $I_{Hall} = I_{O1} - I_{O2}$ and Table (2.2) the sensitivity can be calculated as 11 $\%T^{-1}$. The result is 3.1 times higher than the single cross-shaped sensor operating in the current-mode.

Experimental Results

This part describes the experimental results of the proposed twin current-mode Hall sensor. The design of the testing board and the measurement setup are presented at the beginning, whereafter the measurement results are in detail discussed.

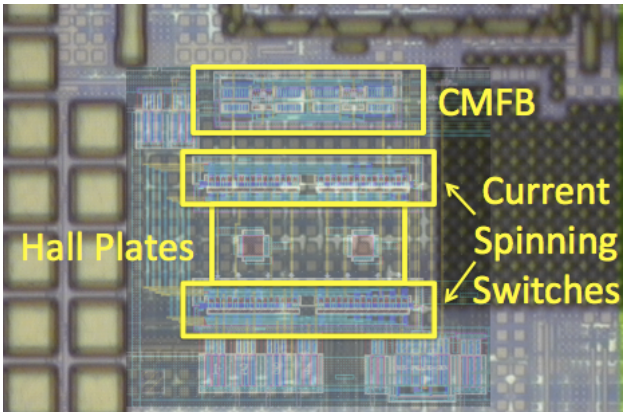

Fig. 3.18 Chip microphotograph of the most relevant blocks.

A sensor prototype has been fabricated in a standard 0.18-μm CMOS process with 6 metal and 2 poly layers. Its microphotograph with its layout back-annotated is shown in Fig. 3.18. The figure highlights main circuital blocks. The sensor plates and relevant switches occupy an active area of 80×50 μm^2. The whole chip area is 300×200 μm^2. The rest of the area is dedicated to the readout circuit, which will be discussed in chapter 5. The nominal supply voltage and the nominal bias current are 1.8 V and 12 μA, respectively. The current spinning frequency is 1 MHz.

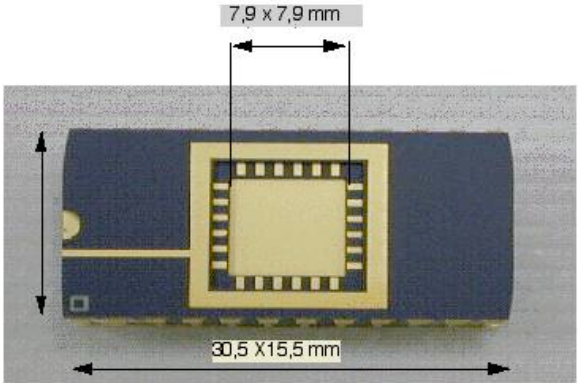

Fig. 3.19 Dual in-line 24-pins package of fabricated chip.

The chip was packaged in a 24-pins Dual in-line (DIL), as shown in Fig. 3.19. Custom 2-layers printed circuit board (PCB) was designed to measure the 24-pins DIL prototype.

Fig. 3.20 shows the 3D of the mother board designed in Altium software, while Fig. 3.21 illustrates the fabricated board with soldered components. In order to minimize disturbances between analog and digital parts, the motherboard contains two power supplies VDDA (1.8 V for analog circuits) and VDDD (1.8 V for digital clock generator circuits).

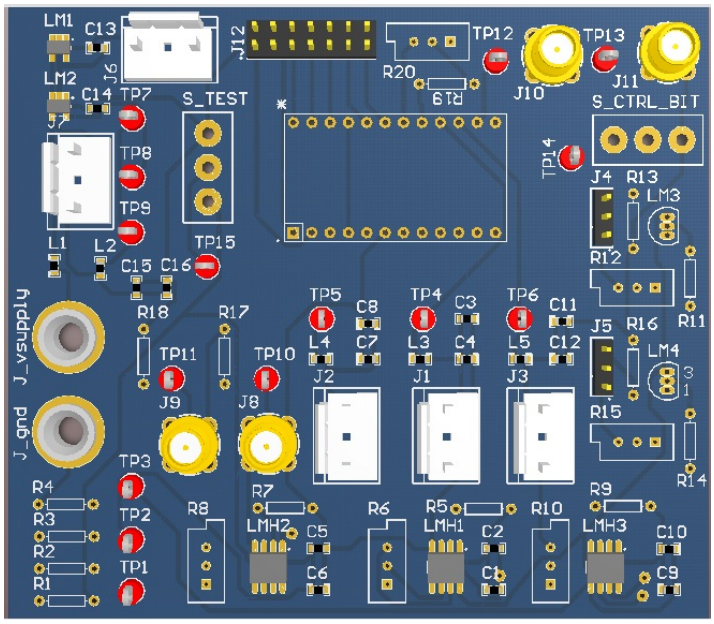

Fig. 3.20 3D Top layer of the BCB board test in Altium.

The measurement setup is shown in Fig. 3.22. The PCB together with the chip are powered by a 5 V power supply, which is used by the components on the mother board to generate two 1.8 V analog and digital power supply and a 0.9 V common-mode voltage.

A digital signal generator/analyzer (NI PXI-6552) provides the four phases $\Phi_1 \sim \Phi_4$ of Fig. 3.7 for spinning current. The PXI system is a National Instruments PC-based platform for test, measurement, and control. The graphical programming tool used is LabVIEW. A Helmholtz coil is used for generating the necessary magnetic field. A set of Helmholtz coils consists of two circular coils of equal diameter and equal number of turns parallel to each other along an axis through the center of the coils, separated by a distance equal to the common radius of the coils. The two coils are connected in series in order to produce a nearly uniform magnetic field in a region surrounding the center point of the axis between the two coils [11]. The PCB

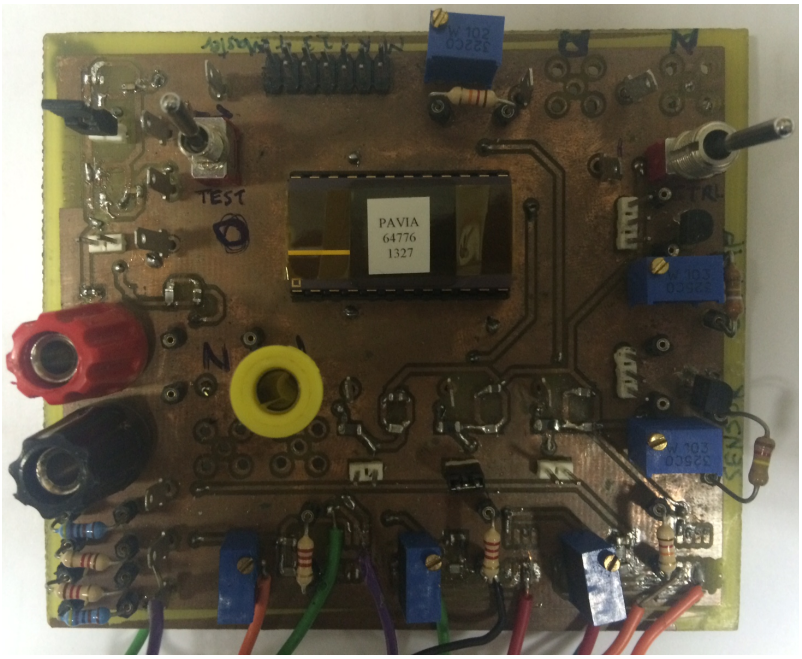

Fig. 3.21 Fabricated 2-layers test board with soldered components.

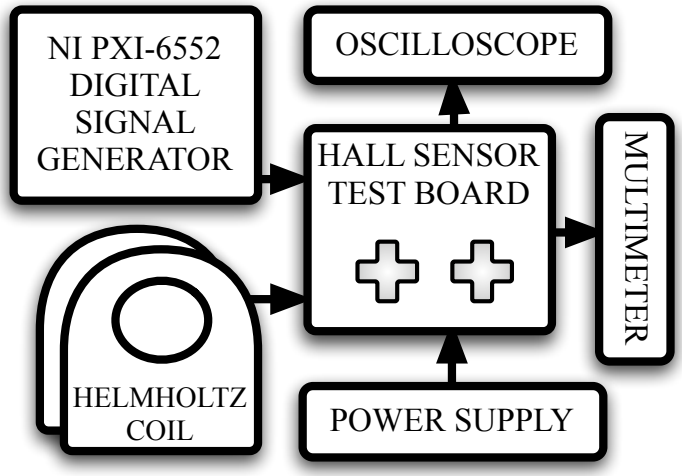

Fig. 3.22 Used measurement setup.

together whit the Hall sensor chip is placed at the center of the Helmholtz coils in order to apply a magnetic field ranging from 0 to 10 mT.

Fig. 3.23 plots the measured differential sensor output current, I_{Hall}, as a function of the sensor bias current for two different magnetic field, 5 mT and 7 mT. I_{bias} is ranging from 0 to 48 μA. The figure shows that the sensor has good linearity with respect to the applied magnetic field.

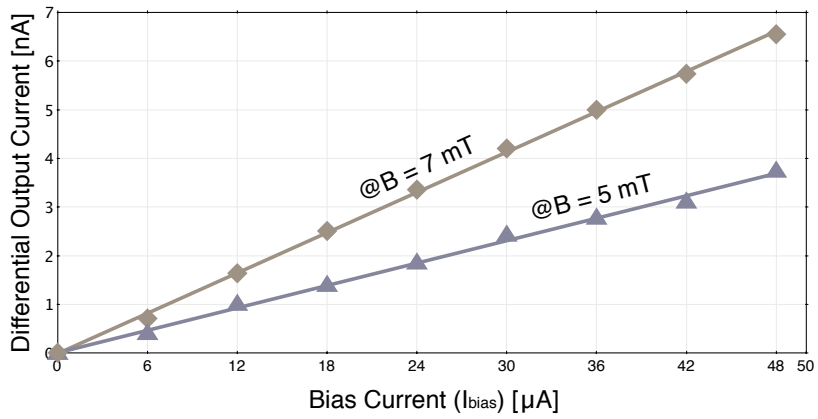

Fig. 3.23 Measured sensor output current as a function of the biasing current at different magnetic fields.

Fig. 3.24 gives the sensitivity, S_I, as a function of the sensor bias current (ranging from 6 to 48 μA) for the above external magnetic fields. The measured sensor sensitivity is within the $1.3 \sim 2\ \%T^{-1}$ range.

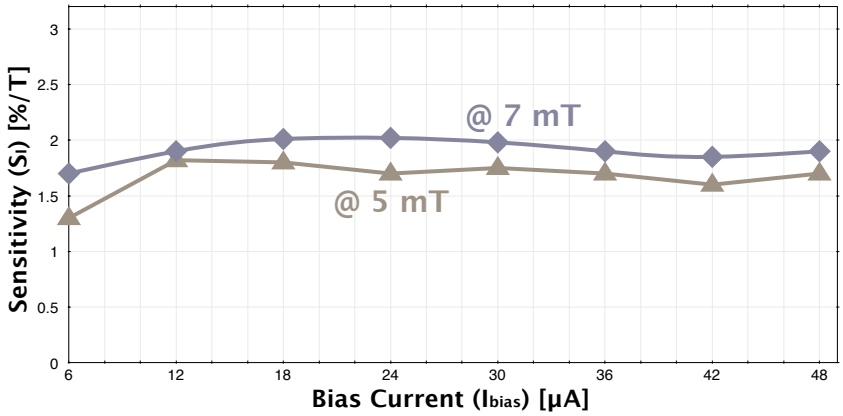

Fig. 3.24 Measured sensor sensitivity as a function of the biasing current at different magnetic fields.

Table 3.5 summarizes the magnetic and electrical microsystem performance for a biasing current of 12 μA. As can be noticed, the overall sensors area is 80×50 μm^2, in which every sensor occupy 8×8 μm^2. The sensor and the relevant switches for current spinning measured power consumption is 65 μW.

Table 3.5 Performance Summary

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Technology	0.18 μm CMOS
Sensor Area	$80 \times 50\ \mu m^2$
Plate Area	$8 \times 8\ \mu m^2$
Number of Sensors	2
Current Spinning Frequency	1 MHz
Supply Voltage	1.8 V
Sensitivity	$1.3 \sim 2\ \%T^{-1}$
Measurement Range	0 ~ 7 mT
Power Consumption	65 μW

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Chapter 4
Current-Mode Vertical Hall Magnetic Sensors

Abstract In this chapter a four-folded current-mode vertical Hall sensor (VHS) is presented. The current spinning technique is applied to a vertical Hall sensor driven in current mode to eliminate the offset and to increase the sensitivity. Different geometries have been studied and simulated by using a simulator based on finite element method. A four-folded three-contacts vertical Hall device model displayed the lowest residual offset and the best sensitivity. Simulations results, obtained in two different environments, are compared and discussed. COMSOL results are validated with respect to the electrical behavior of an 8-resistor Verilog-A model implemented in Cadence environment. The implementation of the four different geometries of 4-folded 3-contact vertical Hall sensor device, sensor biasing circuit and proper digital control unit are expressed next. Current spinning technique and carrying out of the related switches are described in following. The chapter ends with the simulation and measurement results of the fabricated sensor in a standard 0.18 μm CMOS technology.

4.1 Proposed Architecture

Vertical Hall sensors have already been compared to Horizontal Hall sensors in Section 2.3. The horizontal Hall effect device, also referred to as Hall device, has an horizontal device toward the semiconductor substrate and measures the magnetic field, B_Z, perpendicular to the sensor device surface. Whereas, the vertical Hall sensors (VHS) are sensitive to the in-plane component of the magnetic field, B_Y, and detect the magnetic field in the plane of the sensor device. Several geometries have been studied in [1], [2], [3] and [4]. Among them, a four-folded geometric structure that uses the current-spinning technique, provides high resolution and low offset performance [5].

This chapter presents a high sensitive current-mode vertical Hall sensor microsystem with differential output current. Thef system comprises four different geometries vertical Hall sensor (Basic, Small-Distance, Small-Width and Deep-Nwell

devices as summarizes in Table 4.1). A multiplexer has been used for select the optional sensor device and connect the terminals to outputs terminals of chip. The differential output current level is typically within micro-amper to milli-amper range, depend on the bias current. The physical structure of each Hall sensor device is a 4-folded 3-contact vertical device, with the possibility of compensating for the offset caused by mismatch. Extensive and accurate physical simulations and behavioral models of the current-mode Hall sensors allowed optimizing its size, shape and performance for the chosen technology, a standard 0.18-μm CMOS technology. The offset at the output terminals of the sensors is reduced by spinning current technique. The chip operates properly with a bias current of 100 μA. The benefit of having current at output is that its integration over a defined time period determines an output voltage with a gain proportional to the integration time.

The proposed scheme shows that the use of current as output quantity instead of voltage increases the sensitivity. Furthermore, integrating a current into a capacitor for a given time slot provides relatively large signals and averages the noise. The readout interface for magnetic sensors are in details described later in chapter 5.

4.2 Implementation

The main implemented blocks of proposed Hall microsystem are explained in this Section. Starting from key features of the 4-folded 3-contact vertical device, and further the design of the multiplexer and relevant switches are indicated.

Several types and shapes of vertical Hall devices including four-contact (4C), five-contact (5C), six contact (6C) and 4-folded 3-contact Hall sensor have been presented and analyzed in the past to their sensitivities and offsets [5] and [6]. Among them, 4-folded 3-contact Hall sensor has recognized for simplicity to reach high sensitivity and low offset. Fig. 4.1 shows a 3-contact vertical Hall sensor, which we series four of it to make a 4-folded 3-contact Hall sensor. The geometry of 3-contact device is fitted to a 0.18 μm CMOS technology, where cross-section shown in Fig. 4.1(a). The device has been modeled on a silicon p-substrate with a deep n-well active region. Three n+ diffusions serve as contacts to which the drive bias currents are applied and at which the output Hall current are measured. The three contacts in Fig. 4.1(b) are denoted C (center contact) and two S (side contact). The n+ diffusions are separated by p+ diffusions. Since the Hall current (I_{Hall}) and therefore sensitivity are inversely proportional to the n-well doping concentration, a n-well with small width (W) is normally used in the fabrication process, as shown in the top view of the device in Fig. 4.1(b).

The geometry and size of n-well, n+ and p+ diffusion are influenced on the performances of the sensor. Furthermore, the distance between the contacts and also distance between the contacts and edge of the device are most critical points, which the designer should consider them for getting optimum results.

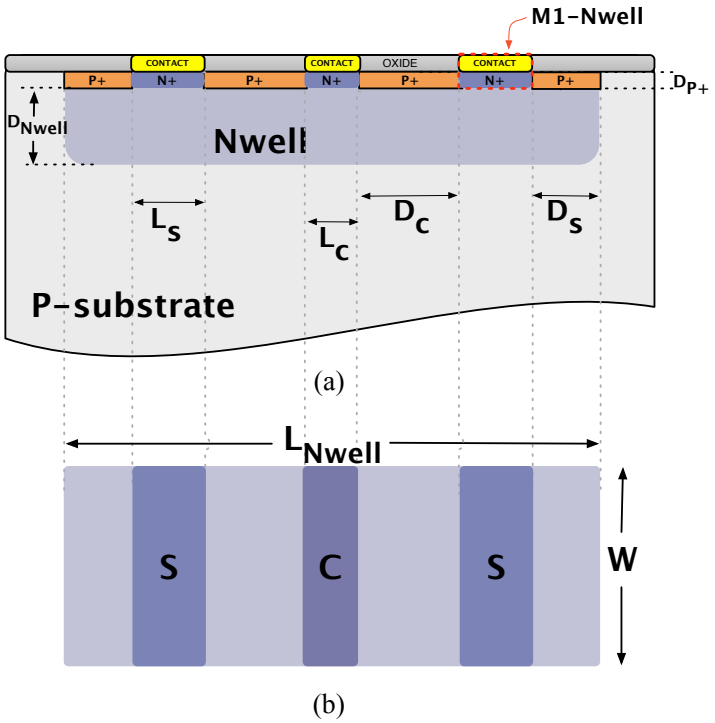


Fig. 4.1 The 3-contact vertical Hall sensor in semiconductor substrate of a CMOS technology: (a) cross section view and (b) top view.

4.2.1 Four-Folded Vertical Sensor Device

Since different structures have been proposed in the literature, this study preliminarily compares them, when used in the current-mode using 2D COMSOL. The architectures with five contacts, [2] and [3], and eight symmetrical contacts, [1], demonstrate limitations for offset performance and complexity of readout. The current-mode four-folded vertical Hall device model turned out to be the optimum selection. Fig. 4.2(a) shows its cross-section. Four lined up N-wells with three n-plus contacts each make the device. Metal connections create a ring of external contacts. The device has four terminals, C_1, C_2, C_3 and C_4. If a current enters one of the terminals, say C_1, and exits from terminal C_3, supposing to have equal structures, the current through C_2 and C_4 is zero with zero magnetic field. A magnetic field parallel to the surface in Y-direction alters the current flow, as shown in Fig. 2. The solid-lines represent the current trajectory in the zero magnetic field case and the dashed-lines show the current trajectory at nonzero magnetic field and under the influence of Lorenz force. A differential current, I_{Hall}, at the two output terminals results. The sensitivity of the device is

$$S_I = \left| \frac{I_{Hall}}{I_{bias} \times B_Y} \right| \tag{4.1}$$

In order to compare the operation of the vertical Hall sensor in voltage-mode and current-mode let draw it as shown in Fig. 4.2(b) and Fig. 4.2(c), respectively. The effect of the magnetic field in the four sections of the sensor is depicted in the figures. For the voltage-mode operation, the current path is shortened in S_4 and lengthened in S_2. However, because of the symmetry, the voltage of the output terminal is in the middle for both S_2 and S_4 (V_{O1} and V_{O2}). Thus, they are ineffective for the magnetic sensitivity. As shown shortly, we can use equivalent resistances from pairs of the four terminals. They, as shown in the figure, are (R-ΔR_V), (R+ΔR_V) on the top section, and (R+ΔR_V), (R-ΔR_V) in the bottom section. V_{O1} and V_{O2} can be expressed as

$$V_{O1} = \frac{V_{bias}}{2R}(R - \Delta R_V) \tag{4.2}$$

$$V_{O2} = \frac{V_{bias}}{2R}(R + \Delta R_V) \tag{4.3}$$

The differential Hall voltage is given by

$$V_{HV} = V_{bias}\frac{\Delta R_V}{R} \tag{4.4}$$

The operation in the current-mode, shown in Fig. 4.2(c), connects the output terminals to ground. The equations describing the equivalent model are

$$I_1 = \frac{V_x}{(R - \Delta R_I)} \tag{4.5}$$

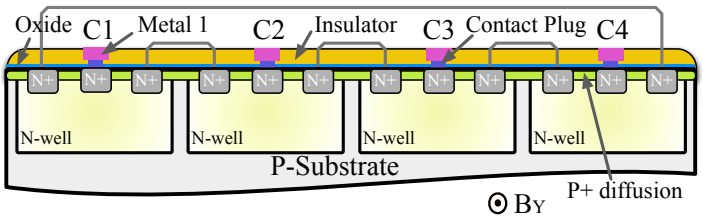
$$I_2 = \frac{V_x}{(R + \Delta R_I)} \tag{4.6}$$

that yield the differential Hall current as

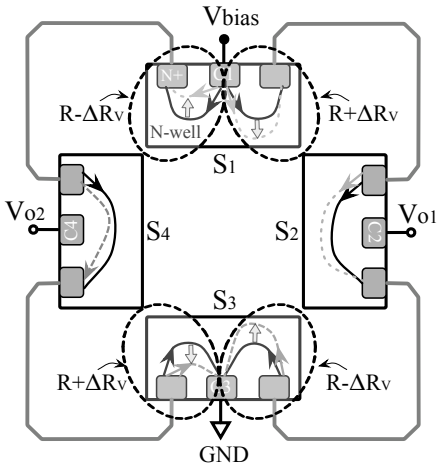
$$I_{HI} = I_{bias} \cdot 2 \cdot \frac{\Delta R_I}{R} \tag{4.7}$$

The last expression gives a sensitivity two times bigger than the one obtained in the voltage-mode, supposing $\Delta R_V = \Delta R_I$. However, since in the current mode even S_2 and S_4 are active, we have $\Delta R_V < \Delta R_I$.

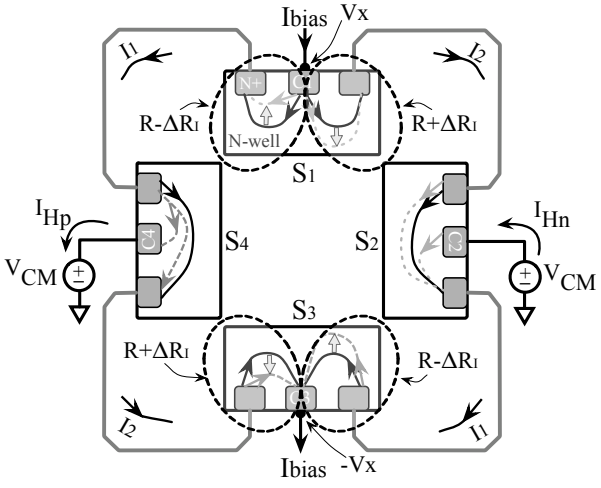
This chapter analyzes the influence of current injection and current output signals on vertical Hall effect sensors performances, including noise and offset, with the aid of COMSOL simulations. Moreover, an accurate 8-resistor network model for the four-folded vertical Hall device is described in Verilog-A and tested in a Cadence environment. Simulation results obtained in COMSOL and in Cadence show excellent matching and system potentiality.



(a)



(b)



(c)

Fig. 4.2 (a) Three contacts four-folded vertical Hall device cross-section, (b) vertical Hall device in voltage-mode, (c) vertical Hall device in current-mode configuration: biasing conditions and currents flows.

4.2.2 Offset Reduction

The offset can be reduced by current spinning technique, as already discussed in 2.5.2.1. Moreover, a well chosen geometry of the Hall device can greatly improve the results.

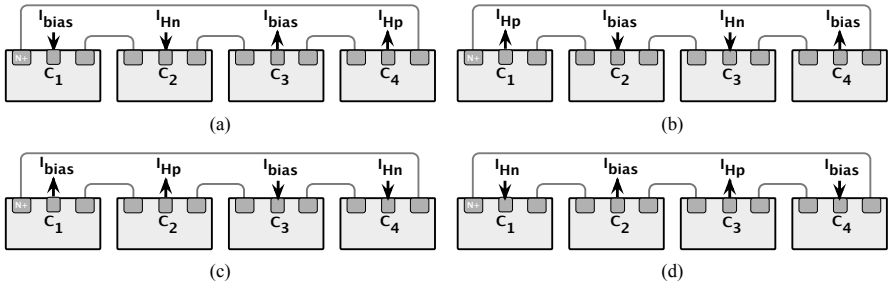


Fig. 4.3 The four modes current spinning configuration: (a) Mode 1, (b) Mode 2, (c) Mode 3 and (d) Mode 4 for a 4-folded 3-contact vertical Hall sensor.

For implement the current spinning technique, four different modes are commonly used to operate a 4-folded 3-contact vertical Hall sensor, as shown in Fig. 4.3. They change by the input contacts to which the input bias current are injected and which the same bias current are drained. The differential of current outputs gives the Hall Current, $I_{Hall} = I_{Hp} - I_{Hn}$. For example consider mode 1 in Fig. 4.3(a): the bias current (I_{bias}) injects into a contact terminal C_1 and the same bias current (I_{bias}) is drawn from another non-adjacent contact terminal C_3. In presence of the magnetic field, two differential output currents are available at the remaining two terminals, C_2 and C_4. When a nonzero magnetic field, B_Y, is applied in Y direction, the inject current into C_1 is divided to unbalance currents, which they are entered to second and fourth folds of the device. Indeed, the Lorentz force shortens the trajectory of the injected I_{bias} on the left side of the C_1, where the current enters to fourth fold. On the other side, the Lorentz force lengthens the trajectory on the right hand, where the current enters to second fold of the Hall device. This phenomenon leads to unequal currents at the input and outputs of the second and fourth folds. Therefore, the output differential currents can be derived as:

$$I_{Hp} = [\frac{I_{bias}}{2} + \frac{I_{Hall}}{2}] - [\frac{I_{bias}}{2} - \frac{I_{Hall}}{2}] = I_{Hall} \tag{4.8}$$

$$I_{Hn} = [\frac{I_{bias}}{2} - \frac{I_{Hall}}{2}] - [\frac{I_{bias}}{2} + \frac{I_{Hall}}{2}] = -I_{Hall} \tag{4.9}$$

The difference of the output currents is $2 \times I_{Hall}$.

The current spinning interchanges periodically the output and supply terminals of the Hall device so that the input bias current injecting point is rotated in each

state while the offset appears at the output terminals. The device after clocked with four phases has been eliminated the output offset.

4.2.3 System Implementation

The geometry plays an important role on the Hall sensors performance. Four different vertical current-mode Hall sensors have been designed and integrated in a 0.18 µm CMOS technology and evaluated for Hall current (I_{Hall}), sensitivity, offset and etc. The four integrated Hall devices are presented in Table 4.1. Furthermore the used dimension and size are depicted on the cross section and top view of the vertical Hal device in Fig. 4.4. The design parameters include L_C, L_S, D_C, D_S, W and d, which stand for center contact length, side contact length, distance between center and side contact, distance side contact from border of sensor, width and distance between the folds, respectively. The center contacts are used for biasing and measurements purpose, whereas the side contacts dedicated as connection between the four folds of the device.

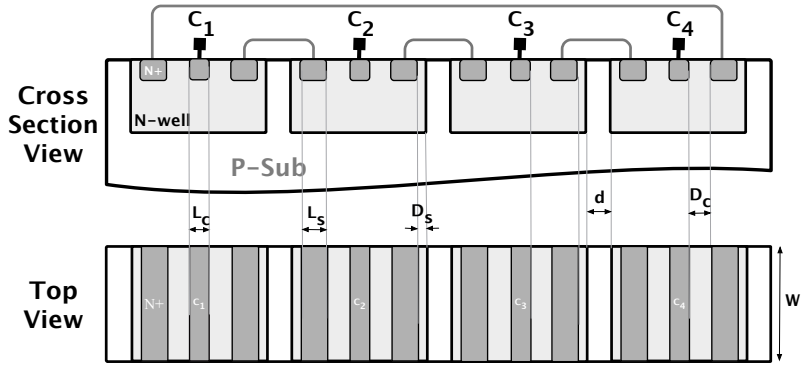


Fig. 4.4 The 4-folded 3-contact vertical Hall sensor in cross section view and top view.

Table 4.1 Geometry variations of four different integrated 4-folded 3-contact vertical Hall sensors

Hall Device	L_C [µm]	L_S [µm]	D_C [µm]	D_S [µm]	W [µm]	d [µm]
Basic	1.71	2.65	9	5	7.44	2
Small-Distance	1.71	2.65	**6**	5	7.44	2
Small-Width	1.71	2.65	9	5	**6.2**	2
Deep N-well	1.71	2.65	9	5	**11.6**	2

The *Basic* device integrated as a reference shape. The *Small-Distance* and *Small-Width* device are scaled version of the *Basic* device, which have changing in the distance center contact from side contact and sensor width, respectively. For the *Deep N-well* device has been replaced n-well active region by a deep n-well layer.

The four devices were fabricated on a same chip in a 0.18 μm CMOS technology. The positioning and placement of sensor devices are presented in Fig. 4.5. The chip uses a multiplexer digital unit (MUX) to control and connect each sensor device to the output pads. $C_1 \sim C_4$ are connected to each sensor device by selective inputs, S_1 and S_2. The relevant switches SW0~SW3 realized the connections.

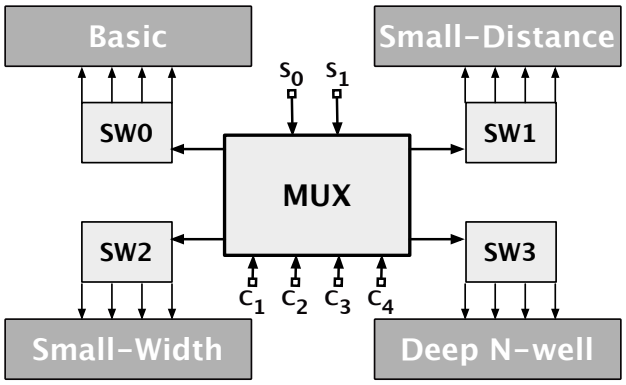


Fig. 4.5 Placement of four analyzed Hall devices on a tested chip.

4.3 Simulation and Modeling

This Section presents the symmetrical models of the current-mode vertical Hall device. First, the COMSOL model is illustrated and simulation results are presented. Later on, the 8-resistor model described in Verilog-A and Cadence-based simulation results follow.

COMSOL Simulation

A two-dimensional model of the current-mode vertical Hall device has been implemented and simulated in COMSOL with the model parameters summarized in Table 4.2. Fig. 4.6 shows the four configurations of the model geometry and the surface electrical distribution of the three contacts four-folded vertical Hall device when a magnetic field of 0.5 T is applied. The simulation uses a nominal bias current of 100 μA.

Table 4.2 Model Parameters of a 2D VHS Model in COMSOL.

Symbol	Value	Parameter
N_D [cm^{-3}]	$7.78 \cdot 10^{16}$	Doping
$R_\square$ [Ω/sq]	1028	N-well Sheet Resistance
σ_n [S/m]	1040	N-well Conductivity
σ_p [S/m]	10	P-Sub Conductivity
B_Y [T]	$0 \sim 0.5$	Magnetic Field
t [m]	$6 \cdot 10^{-6}$	Silicon Thickness
I_0 [μA]	100	Bias Current

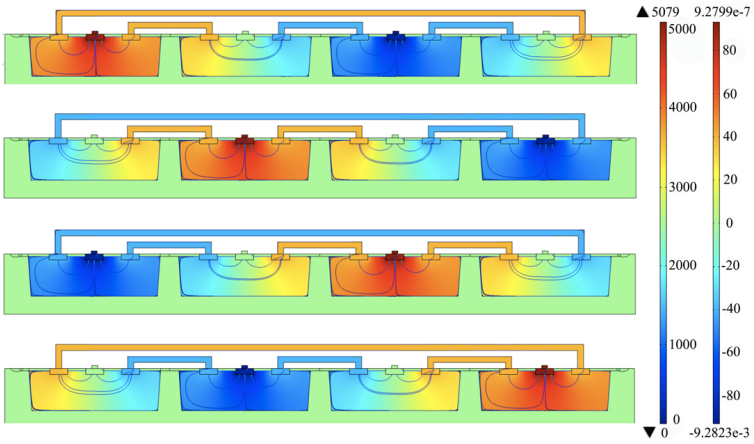
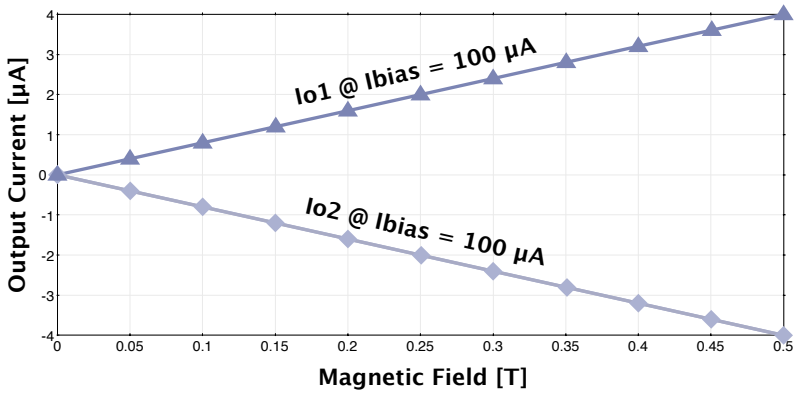


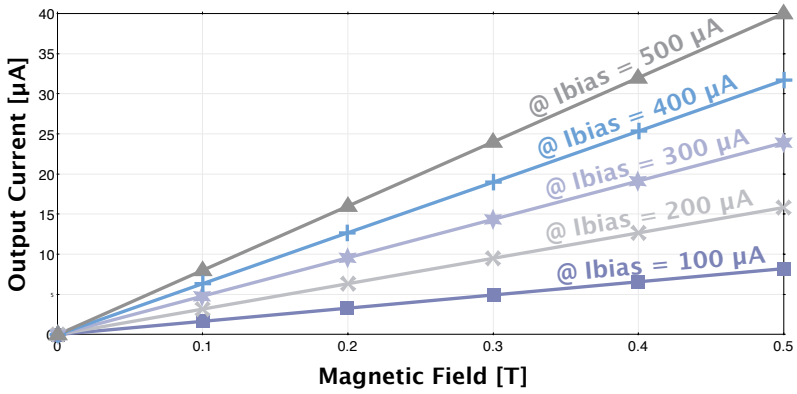
Fig. 4.6 Simulation of three contact vertical Hall device in COMSOL environment and current streamline of four modes of operating in the current-mode.

In order to compensate for the mismatches due to possible masks misalignment during fabrication, e.g. non-equal distance between contacts, the sensor uses the current spinning method. Simulations include a mismatch in the terminal C_4 of the sensor. Fig. 4.7(a) shows the simulated average output currents of the vertical Hall device, when changing the magnetic field within the 0 to 0.5 T range after the four current spinning phases. The offset is zero and the maximum differential output current (Hall current) is almost 8 µA for a magnetic field equal to 0.5 T. These current levels can be transformed into suitable voltages by integrating the current signal over a given period of time.

Fig. 4.7(b) draws the simulated Hall currents when the bias current (I_{bias}) is ranging from 100 µA to 500 µA with a step of 100 µA and the magnetic field ranges from 0 to 0.5 T with steps of 0.1 T.



(a)



(b)

Fig. 4.7 (a) Simulated sensor output currents as a function of the magnetic field at 100 µA bias current after four phases, and (b) Simulated sensor Hall current as a function of the different biasing current at different magnetic field.

Verilog-A Model

Models to simulate magnetic sensors taking into account physics, geometry and technological constraints are implemented in a first phase of this project using COMSOL tool and they turned out to be very helpful in system design. It is however not straightforward to include in COMSOL simulations secondary effects such as the presence of noise effects, parasitic capacitances, electronics non-idealities, etc [7].

In order to better analyse the overall performance from a system point of view and to prepare a custom tool for analog circuit design, alternative solutions for sensor modelling are analysed with an eye on languages compatible with integrated cir-

cuits simulators. Sensor modelling in Cadence environment allows to optimize electronic front-end considering non-idealities and sensor versus electronics interference. Verilog-AMS is a derivative of Verilog hardware description language which includes analog and mixed signal extensions to describe behaviour of devices. In order to this specific case, Verilog-A, a continuous time subset of Verilog-AMS, is used.

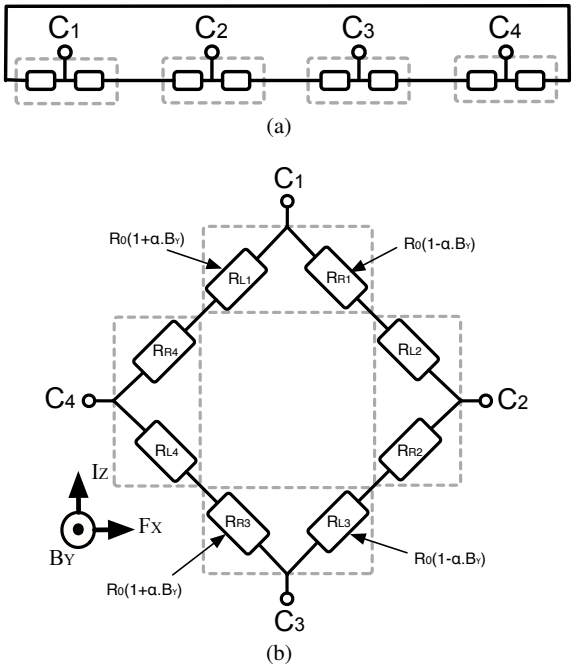


Fig. 4.8 (a) The equivalent model implemented in Verilog-A using eight resistors, (b) A same model in a Wheatstone bridge depiction.

The vertical Hall sensor is simplified into a series of eight resistors, as schematically shown in Fig. 4.8(a). Each contact terminal has two resistors, one on the left (R_L) and one on the right (R_R). The initial values of all resistors at zero magnetic field are equal (R_0). Fig. 4.8(b) shows the same model arranged in a Wheatstone bridge, which has been modeled and described using Verilog-A language so that it can be simulated in the Cadence environment. It includes four electrical terminals (C_1, C_2, C_3 and C_4) and eight resistors (four R_L and four R_R). The values of these resistors are controlled by three parameters: the external magnetic field, the initial value of resistors, R_0, and a magnetic resistance coefficient, α:

$$R_L = R_R = R_0(1 \pm \alpha.B_Y) \tag{4.10}$$

The magnetic resistance coefficient, α, is defined as the average of the initial values of resistors, R_0, in the presence and absence of the magnetic field.

Simulations have been performed in Cadence using 100 μA input bias current and considering the magnetic field in the range from 0 to 0.5 T. Results are summarized and compared with COMSOL simulations in the following.

Verilog-A and COMSOL Comparison

In order to show the accuracy of the Verilog-A model, the simulation results have been compared with the ones achieved with the COMSOL model, as summarized in Table 4.3. For example in present of 0.5 T magnetic field COMSOL shows a current difference (I_{Hall}) of 7.80084 μA, while Verilog-A presents 7.80036 μA for Hall current. The results are in excellent agreement and the difference is less than 0.1%.

Table 4.3 Numerical comparison between the simulations of the vertical Hall device in COMSOL and Verilog-A

Magnetic Field	**COMSOL**		**VERILOG-A**	
B_Y[T]	I_{Hp} [μA]	I_{Hn} [μA]	I_{Hp} [μA]	I_{Hn} [μA]
0	0	0	0	0
0.1	0.59772	-0.59772	0.59798	-0.59798
0.2	1.43061	-1.43061	1.43021	-1.43021
0.3	2.26121	-2.26121	2.26102	-2.26102
0.4	3.08317	-3.08317	3.08351	-3.08351
0.5	3.90042	-3.90042	3.90018	-3.90018

As can be seen from the resulting simulation, the Hall current obtains from differential current outputs at 0.5 T;

$$I_{Hall} = I_{Hp} - I_{Hn} = 3.90042 - (-3.90042) = 7.80084 \ \ [\mu A] \tag{4.11}$$

From Eq. 2.11, the absolute sensor sensitivity is calculated as:

$$S_{A_I} = \frac{I_{Hall}}{B} = \frac{7.80084\ [\mu A]}{0.5\ [T]} = 15.60168 \quad [\mu A\, T^{-1}] \tag{4.12}$$

According to Table 2.2 and a bias current of 100 μA, the sensor sensitivity is defined as:

$$S_I = \frac{S_{A_I}}{I_{bias}} = \frac{15.60168\ [\mu A\, T^{-1}]}{100\ [\mu A]} \simeq 15.6 \quad [\%T^{-1}] \tag{4.13}$$

This value of sensor sensitivity is promising compare to current vertical Hall sensors, which they have reported a sensitivity in range of $1.5 \sim 4.3\ \%T^{-1}$ [3], [4], [5] and [6].

This study shows the effectiveness of a current-mode Hall sensor. Simulation and modeling results show that the vertical Hall sensor obtains a sensitivity better than $15.6\ \%T^{-1}$, which reveals that the proposed technique enables superior performance of magnetic field sensitivity, in terms of signal to noise ratio compared to sensitivity performance of voltage-mode Hall sensors.

The analysis and the design of a complete Hall sensor microsystem and peripheral readout circuits will be continued in the next chapter, all using a conventional CMOS technology.

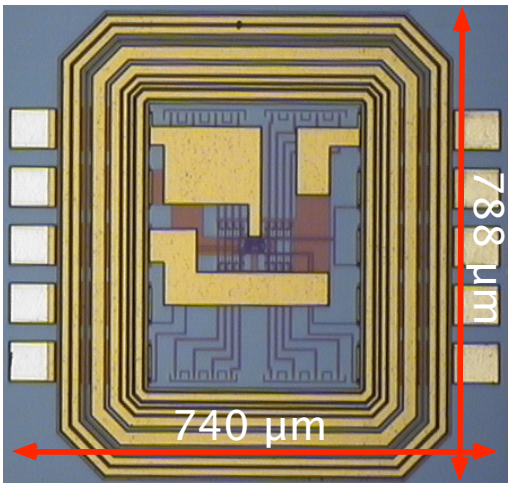
4.4 Measurement Results

The experimental results of the four different proposed vertical Hall sensors have been discussed in this section. First the design of testing board and measurement setup are explained. Whereafter the measurement results are described.

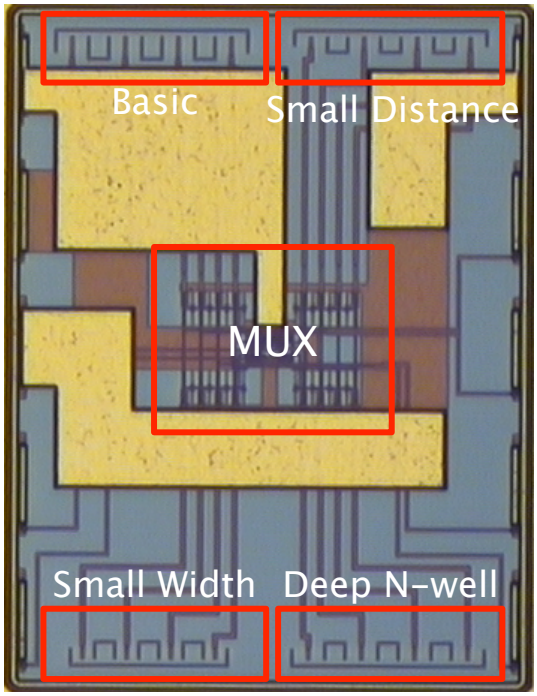
The experimental prototype of the multi 4-folded 3-contact Hall sensor is fabricated in a standard 0.18 μm CMOS technology. Fig. 4.9 shows the chip microphotograph, where the four sensors (Basic, Small-Distance, Small-Width and Deep N-well) and multiplexer block highlighted in Fig. 4.9(b). The whole chip occupies an area of $788 \times 740\ \mu m$.

The prototype has 10-pins, which all connected directly to PCB. Custom printed circuit boards (PCBs) were designed to measure prototype, which includes a motherboard and a baby board. Fig. 4.10(a) shows the top layer of the motherboard designed in Altium Designer software, where Fig. 4.10 illustrates the fabricated board with component soldered. In order to avoid any interferences between the digital and analog parts, the motherboard uses two different power supply VDD and DVDD. These reference voltages are regulated by two voltage regulators (LM4120) on PCB. The top layer plane is connected to VDD, where the bottom layer plane is GND. Both inject and drain bias current sources were provided by two current generators (LM234) on the motherboard. Two toggle switches used as selectors. The main parts of designed board includes current generators, voltage regulators and selectors have been highlighted in the figure. The baby board uses a 80-pin socket (10 pins are connected to chip) to hold the chip, allowing to fast replacement of other samples during measurement. In order to generating a wide range of an external magnetic field, an Helmholtz coil with dimensions of $20 \times 36 \times 38$ cm has been used.

The measurement has been performed in two different voltage and current modes, as shown in Fig. 4.11. In order to test of the sensor in voltage-mode, it is biased by a current generator while the opposite terminal is connected to ground. The changing of voltages at other two terminals, V_{O1} and V_{O2} in Fig. 4.11(a), in presence of an external magnetic field generates an Hall voltage ($V_{Hall} = V_{O2} - V_{O1}$).

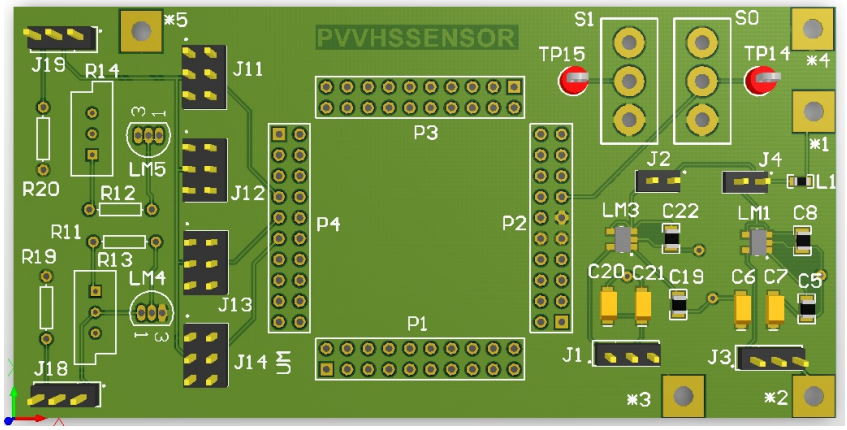


(a)

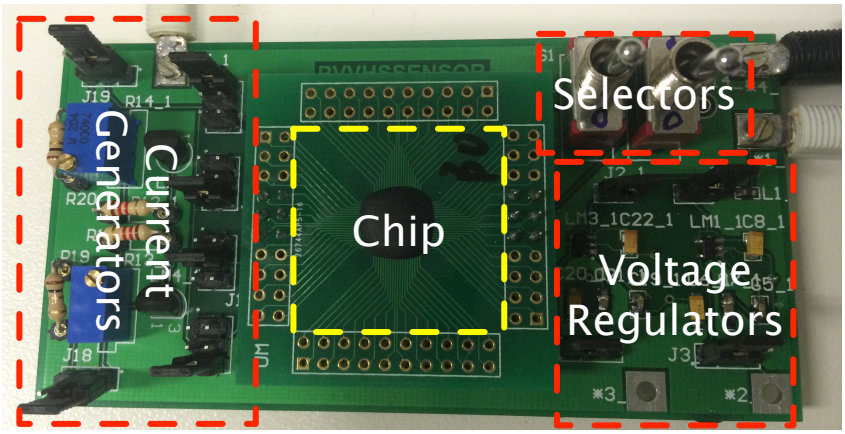


(b)

Fig. 4.9 (a) PVVHSSENSOR chip microphotograph, (b) placement of the multi-sensors on the same chip.



(a)



(b)

Fig. 4.10 (a) 3D Top layer of the BCB board test in Altium, (b) fabricated test board with components soldered.

Fig. 4.11(b) shows the configuration bias of the sensor in current-mode. In order to ascertain of this measurement, two current generators, LM234, generates bias currents. Whereafter, for fixing an constant voltages of V_{CM}, at the output terminals two off-chip low offset opamp, LF412, have been used.

Fig. 4.12(a)~Fig. 4.12(d) show the current-mode sensitivity and voltage-mode sensitivity versus bias current for different Hall sensor devices. The magnetic field of 5 mT was used, while the bias current is changing from 10 μA to 50 μA in step of 10 μA. The diamond line (blue) illustrates the sensitivity measurement results of the current-mode configuration, where the triangle line (brown) shows sensitivity results of the voltage-mode configuration.

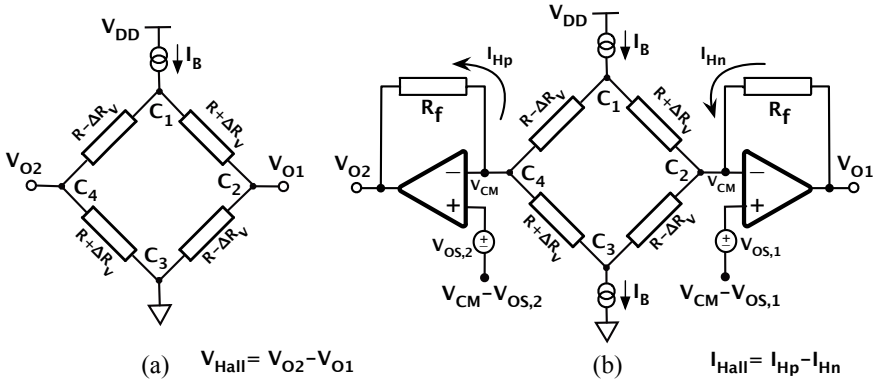


Fig. 4.11 Configuration of the fabricated chip in (a) Voltage-mode and (b) Current-mode.

Table 4.4 reports the measured characterization of four different vertical Hall sensors. From the measurement results, the offset and sensitivity varied with geometry. The information for the current-mode and voltage-mode sensitivities are altered by changing of distance between contact terminals (D_C) and N-well width (W). In order to get a better voltage-mode sensitivity, the sensor width can be decreased. The `Small-Width` sensor device has best voltage-mode sensitivity. On the part of current-mode by decreasing of the contacts distances can be improved the sensitivity, while with deeper N-well diffusion this value will be meliorated. The `Deep N-well` and `Small-Distance` sensor devices prove to have the best performance in terms of the current-mode sensitivity.

In terms of offset, according to current spinning technique as mentioned in 4.2.2, the residual offset can be calculated as

$$V_{OS,T} = \frac{V_{OS,\Phi_1} + V_{OS,\Phi_2} + V_{OS,\Phi_3} + V_{OS,\Phi_4}}{4} \tag{4.14}$$

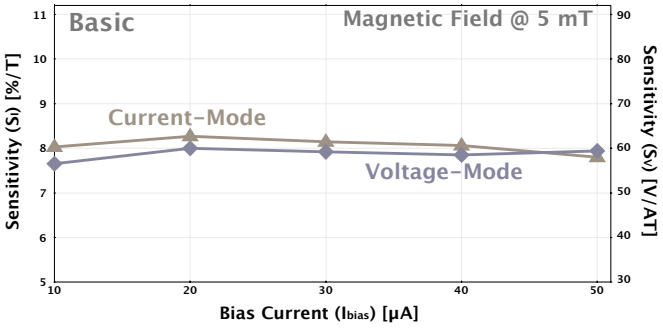
where $V_{OS,\Phi_{1,2,3,4}}$ are the voltage offset of each four current spinning phases.

The magnetic field equivalent offset is defined as

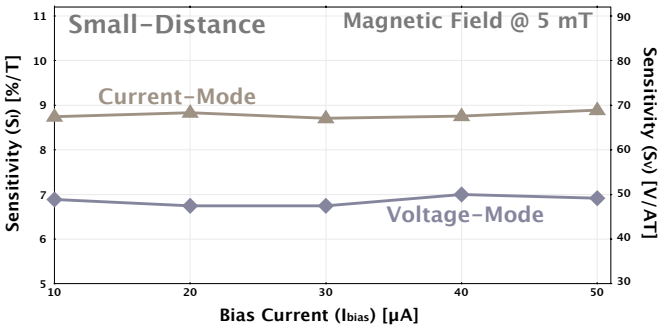
$$B_{OS} = \frac{V_{OS,T}}{S_A} \tag{4.15}$$

where S_A is the absolute sensor sensitivity which, obtained by dividing Hall voltage over the magnetic filed in V/T (See Eq. 2.10).

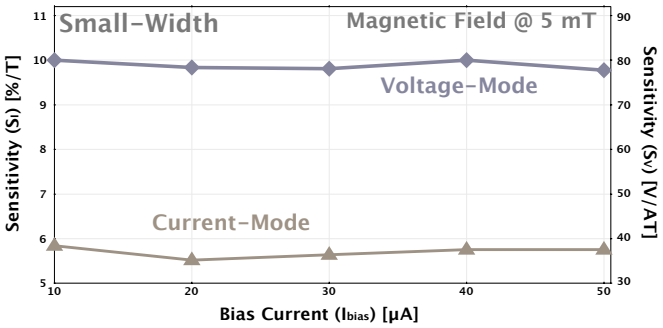
The offset measurements were performed in the absence of magnetic field after four phases of current spinning technique and was evaluated at room temperature. The magnetic field for calculation of Hall voltage and absolute sensitivity is considered 5 mT. The `Basic` device presented lower offset in compared to other sensor devices, which measured $41.66 \pm 8\ \mu T$ magnetic field equivalent offset. The highest offset is related to the `Deep N-well` device with more than $500\ \mu T$.



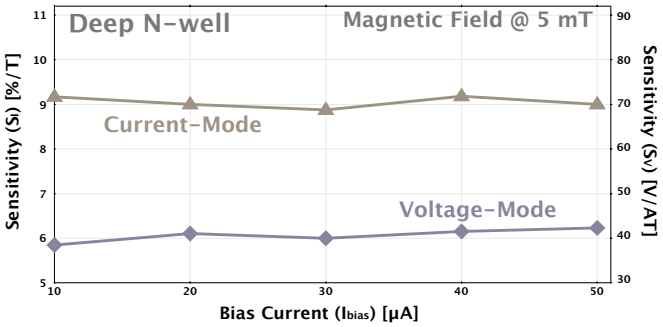
(a) Basic sensor device



(b) Small-Distance sensor device



(c) Small-Width sensor device



(d) Deep N-well sensor device

Fig. 4.12 Measured sensitivity of each vertical Hall sensor as a function of bias current in both current and voltage modes.

Table 4.4 Integrated four different vertical Hall sensors characterization

Hall Device	S_I [%/T]	S_V [V/AT]	$V_{OS,T}$ [μV]	B_{OS} [μT]
Basic	8±0.1	59±1	0.05±0.01	41.66±8
Small-Distance	8.7±0.2	50±1	0.075±0.015	83.33±17
Small-Width	5.6±0.4	78±2	0.65±0.01	406±6
Deep N-well	9±0.1	43±1	0.425±0.02	531±15

Fig. 4.13 shows the situation of each Hall sensor device in related to values of current-mode sensitivity, voltage-mode sensitivity and magnetic equivalent offset after analysing and extracting the experimental results.

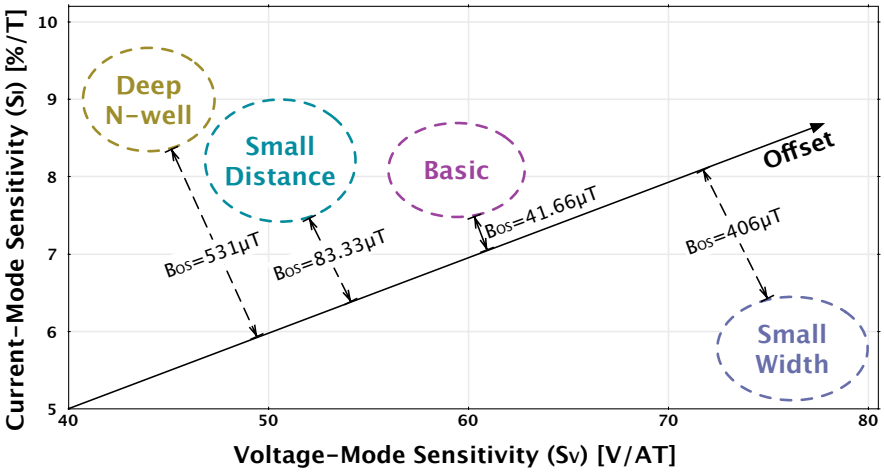


Fig. 4.13 Comparison of four different geometries of vertical Hall sensors in terms of current-mode sensitivity, voltage-mode sensitivity and magnetic field equivalent offset.

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Chapter 5
Magnetic Sensor Interface

Abstract Sensor design for both horizontal and vertical magnetic Hall sensors was addressed in Chapter 3 and Chapter 4, respectively. This Chapter presents a continuation design process of the system and gives detailed design procedures for all the integrated blocks needed in a high-performance sensor microsystem. A design procedure is discussed for each block of the microsystem starting from analog front-end including a chopped I/V converter, switched-capacitor filter and digital control unit. First, the analog front-end of the horizontal prototype is explained, while subsequently, the readout circuit of the vertical prototype is described.

5.1 Analog Front-End

The magnetic Hall sensor system includes the Hall plates, as well as the digital and analog electronics parts which are needed for generating selected useful information from the applied magnetic field. In other words, the Hall plates sense the magnetic field and produce an electrical signal. Several different Hall sensors in horizontal and vertical classes have been studied in [1], [2], [3], [4], [5], [6] and [7].

The differential output current level is typically within the range of nano-ampere to milli-ampere, depending on the bias current. In CMOS technology, there are three ways of detecting current using non-sampled techniques: common gate detection, resistive detection and integrating detection, as shown in Fig. 5.1.

For the common gate detection, Fig. 5.1(a), the output current of sensor, $\pm I_{Hall}$, flows into the sources of a common-gate stage (N-channel input). In this case, assuming the transistors are in saturation, the current noise introduced by the MOS directly depends on the transconductance (g_m) of the transistor:

$$\bar{i}_n{}^2 = 4kT(\frac{2}{3}g_m) \tag{5.1}$$

where ${i_n}^2$ is the equivalent current on the sense node [8]. Therefore, in order to have a good SNR, a relatively large bias current, I_B is required.

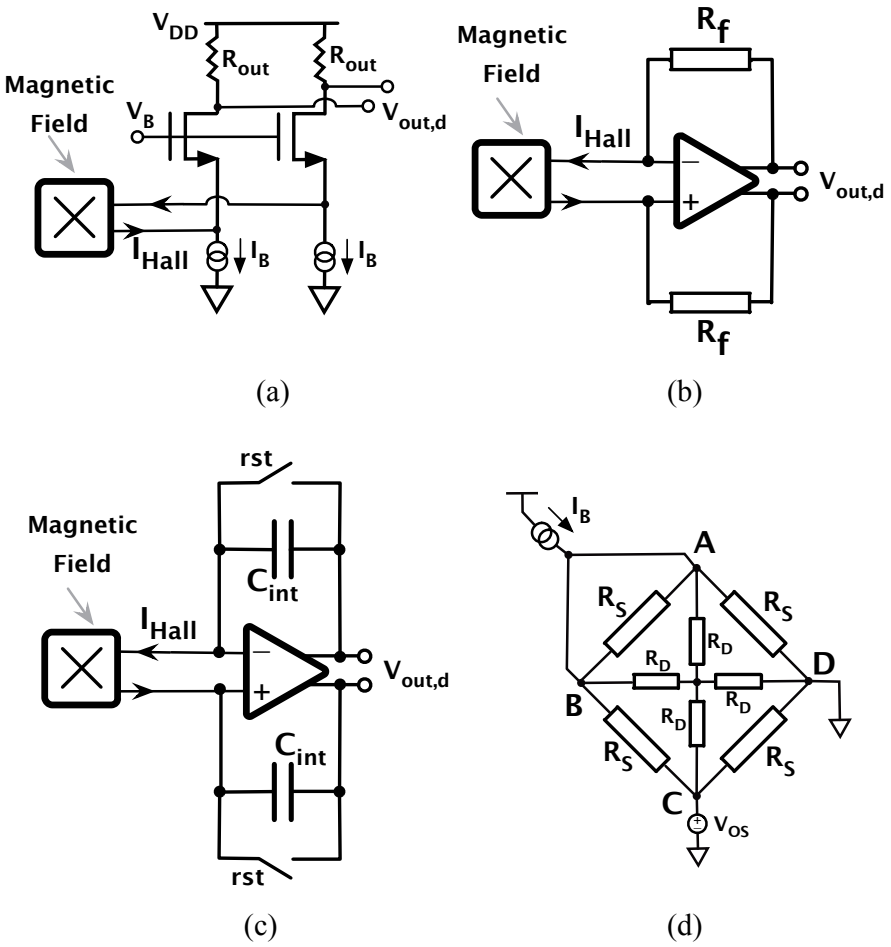


Fig. 5.1 Three I/V configurations: (a) common-gate detection, (b) resistive detection and (c) integrator capacitive detection. (d) 8-resistors Hall plate equivalent model.

In the resistive detection, Fig. 5.1(b), the output current of the sensor is sensed by a resistance, R_f. In this way the current is converted into a voltage that can be further amplified. In this case, the resistance R_f itself is the main noise source. This limits the maximum transresistance gain of the sensor interface.

The third method, shown in Fig. 5.1(c), integrates the currents $\pm I_{Hall}$ over the capacitor C_{int} for a given period of time after a reset. The method grants better noise performance, [8], [9], and provides a transresistance gain proportional to the integration time.

An integrating detection topology has been chosen in order to detect, amplify and convert the Hall current into an analog voltage. In addition to benefiting from

less input current noise in this topology, the use of a low noise operational amplifier enables the integration of the signal current over a period of time with very low residual offset and ensures superior voltage sensitivity.

The first scheme is pseudo-differential, while the other fully differential. For all of them, the equivalent offset of the measure circuit causes an offset in the differential current. If the offset is significant value, it is necessary to compensate for the limit. In order to quantify the consequence of the offset, we can use the equivalent circuit of the sensor depicted in Fig. 5.1(d), [10]. Simple calculations show that an offset V_{os} unbalancing nodes C and D causes a current difference, ΔI, equal to

$$\Delta I = V_{os} \frac{R_S + 3R_D}{R_S R_D} \tag{5.2}$$

ΔI is proportional to the offset voltage and is independent from the bias current. A fitting of the designed Hall sensor with the electrical model of Fig. 5.1(d) provides R_S = 18 kΩ and R_D = 8 kΩ. With these values, an offset of 4 mV causes a current imbalance ΔI = 1.67 µA. If the current sensitivity is 3%/T, it is required to use I_B = 55.67 mA for generating equal signal current with a 1-mT magnetic field.

5.2 Horizontal Prototype

Fig. 5.2 shows the top-level architecture block diagram of the proposed current-mode Hall sensor microsystem. The system comprises of a twin horizontal Hall sensor biased by a current I_{bias}, a switch box which implements the current spinning technique, a digital control unit and an analog front-end circuit to amplify and measure the output currents of the sensor.

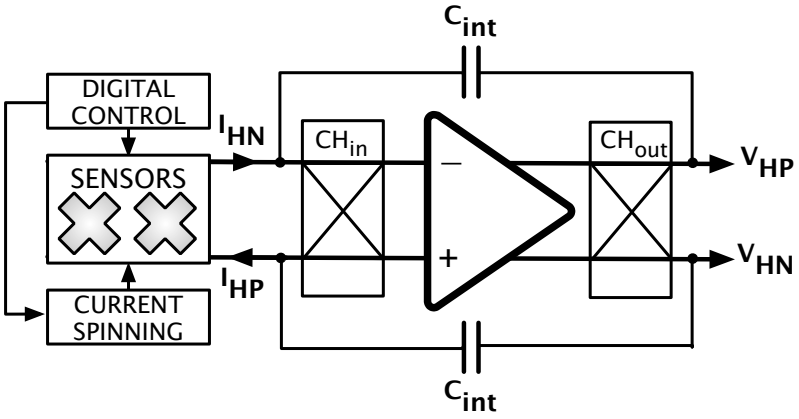


Fig. 5.2 Block diagram of the proposed horizontal magnetic current-mode Hall sensor microsystem.

This project avoids the offset limit by using a chopper stabilized op-amp, [11]. It uses two current-driven Hall plates to form a twin horizontal Hall sensor. The sensor plates provide two differential output currents, I_{HN} and I_{HP}, which are integrated for a given time-slot. The digital unit controls the circuit and generates the phases necessary for the chopper and current spinning operations.

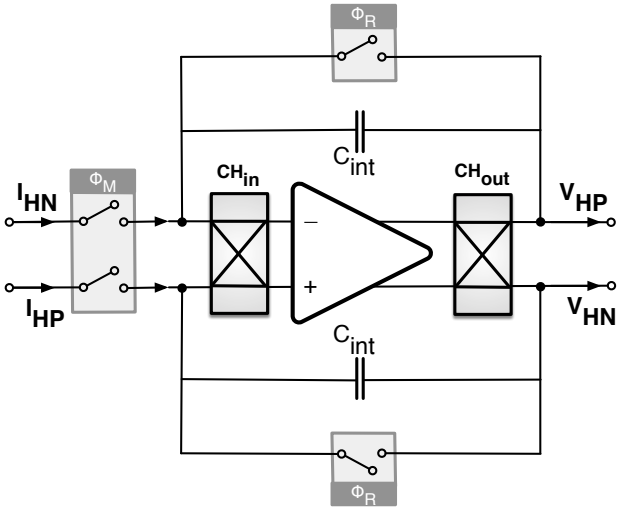
5.2.1 Readout Circuit

The analog front-end comprises of a current to voltage converter, which is directly connected to the sensor output, as the signal levels can be very low at this stage. In other words, the differential output currents of the sensors are fed to the read-out circuit, which shall guarantee low noise and offset.

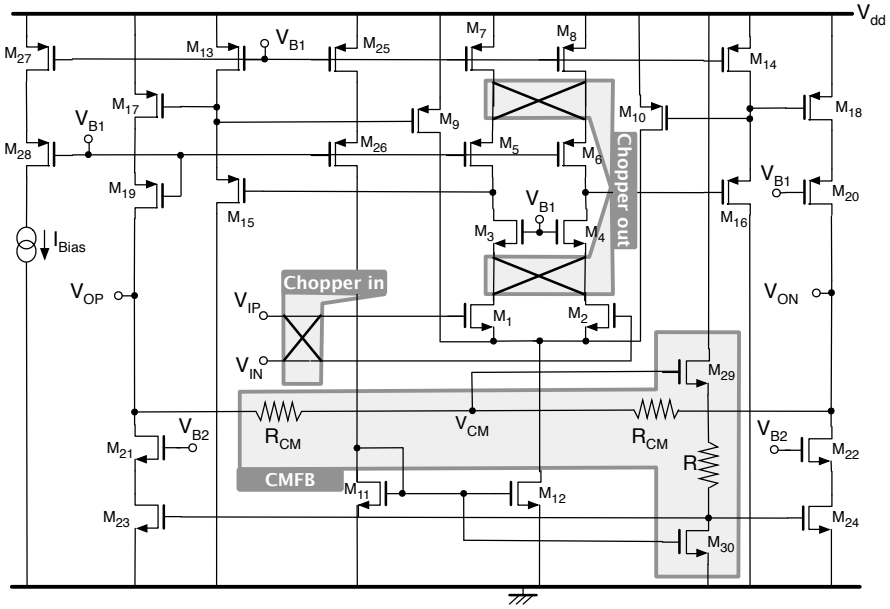
An op-amp featuring 109-dB DC gain and chopper stabilization realizes the current integration. The block diagram of current to voltage converter is shown in Fig. 5.3(a). Fig. 5.3(b) shows the low power two stages fully differential telescopic amplifier and the common mode feedback circuit. The blocks are designed using the same 0.18 μm CMOS technology. The telescopic amplifier is used because it achieves enough gain, while ensuring low-power and low-noise. The input devices of the telescopic amplifier are chosen to be NMOS because the f_T of NMOS devices is approximately three times that of PMOS devices.

The two stage fully differential amplifier uses chopping to eliminate the input offset and low frequency noise by means of chopper switches which enable a modulation-demodulation technique. In practice, the chopper switches modulate the input signal, amplify the modulated signal, and demodulate the (modulated and amplified) signal. As a result the signal is modulated, amplified and then demodulated back to the base band; on the contrary, the input offset and 1/f noise voltages of the amplifier are only amplified and modulated and, therefore, may be removed by low pass filtering [11]. As shown in Fig. 5.3, the input chopper in a NMOS input differential pair is modulated up to the chopping frequency and then the second chopper again transposes the signal at low impedance nodes and demodulates back the signal cancelling out the offset.

The integration of the current signal over the capacitances C_{int} gives rise to complementary voltage ramps at the output. However, its finite gain, A_0, affects the accuracy of the measurement because of the voltage at the input terminals ($-V_{out}/A_0$) which unbalances the magnetic sensors. If the maximum swing of the complementary ramps is ±0.4 V, a DC gain higher than 100 dB unbalances the input by ∓4 μV. This high gain is obtained with the fully differential scheme of Fig. 5.3, which is a two stages amplifier. Each stage is a cascode. The coupling between the two stages uses source followers to accommodate the voltage room necessary for the current chopping of the first stage. The common mode feedback uses a resistors averaging network. The value of R_{CM} is large (1 MΩ) and does not affect the gain of the second stage. The simulated DC gain is 109 dB and the GBW is 11 MHz.



(a)



(b)

Fig. 5.3 Analog front-end; (a) top-level architecture of current-to-voltage converter and (b) its two stage fully differential amplifier.

The measure starts with a reset of the integrating capacitors and lasts for an integer number, K, of current spinning cycles, which is digitally controlled. The differ-

ential output voltages become

$$V_{out,\pm} = \pm \frac{|I_{HP}|8K}{C_{int} f_{clk}} \tag{5.3}$$

At the end of the integration period, the currents I_{HP} and I_{HN} are disconnected from the readout circuit and the output voltages V_{HP} and V_{HN} are available for further processing or for output sampling.

5.2.2 Digital Control Unit and Output Switched-Capacitor (SC) Filter

A digital control unit generates all the signals necessary for current spinning, reset, integration cycles, chopper and output switched-capacitor filter. Fig. 5.4 shows the all driving phases timing diagram. It uses an external master clock of 1 MHz.

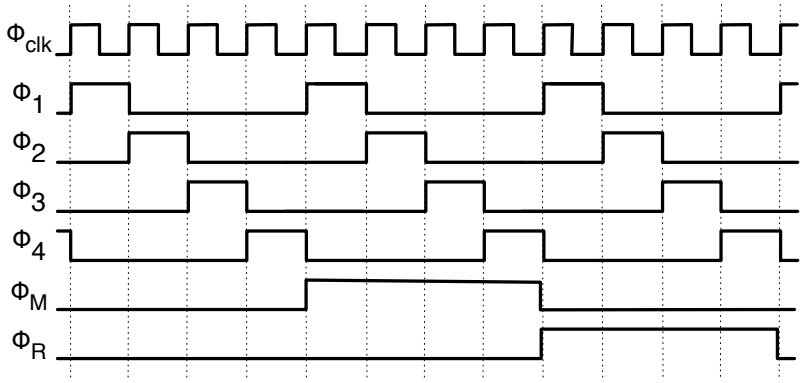
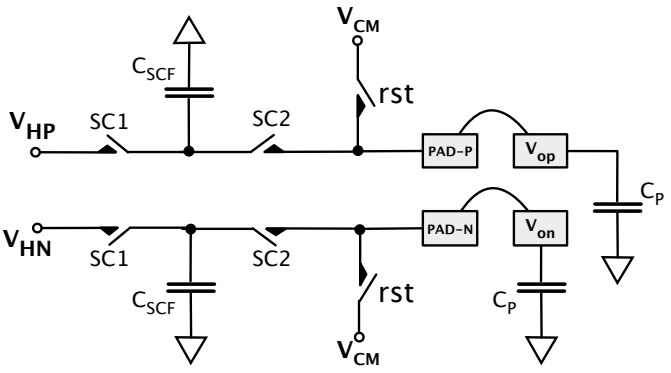


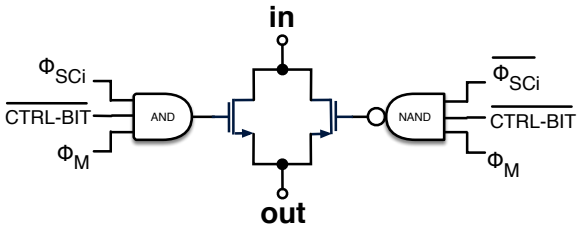
Fig. 5.4 Phases timing diagram for current spinning, reset and measure operation.

Since the outputs are the analog voltages generated at the end of the current integration, it would be necessary to drive the output pins with power hungry buffers. Instead, this design uses simple switched-capacitor RC filters to drive the large pins capacitances, as shown in Fig. 5.5(a). During the integration phase, the op-amp is load-free and the output pins are pre-charged to the common mode voltage. At the end of the integration phase, the small switched capacitors C_{SCF} exponentially charge the output pins. The charging period is about 16 exponential time constants of the RC filter.

Fig. 5.5(b) presents in detail the complementary switches, which are used in the switched-capacitor filter.



(a)



(b)

Fig. 5.5 Output stage of the sensor system; (a) Switched-capacitor filter and (b) phase control of its complementary CMOS switches.

Moreover, digital control unit includes a non-overlapping phase generator. Fig. 5.6 shows a possible circuit to generate two non-overlapping clocks, which are used as chopping clock phases [12].

5.2.3 Measurement Results

This Section describes the experimental results of the proposed twin current-mode Hall sensor. The measurement setup are presented at the beginning, whereafter, the measurement results are discussed in detail.

A sensor prototype has been fabricated in a standard 0.18 μm CMOS process with 6 metal and 2 poly layers. Its whole chip microphotograph including the 24 pins is shown in Fig. 5.7(a). The chip area is 1.08×1.08 mm^2. The sensor plates and relevant switches occupy an active area of 80×50 μm^2, as illustrated in Fig. 5.7(b). The figure presents the rest of the active area with back-annotated layout, which is dedi-

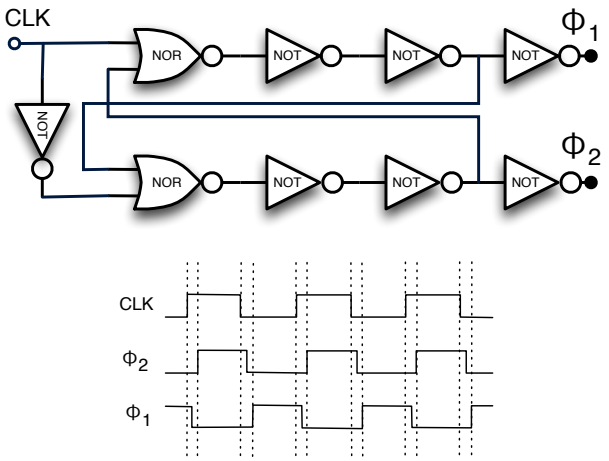


Fig. 5.6 Implemented non-overlapping phase generator.

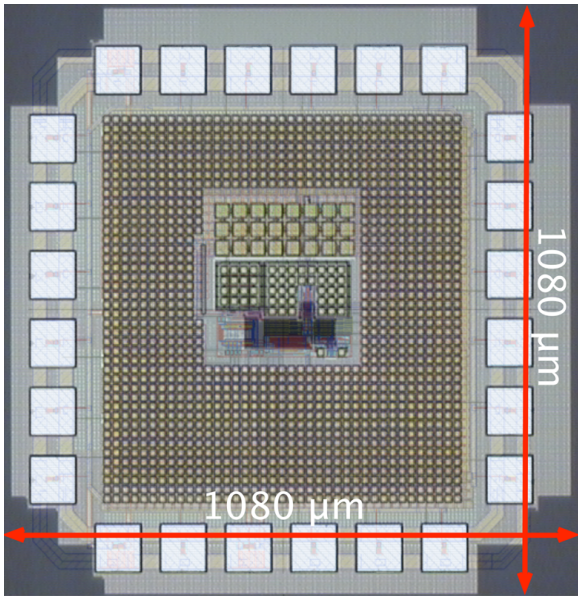
cated to the integrator readout circuit and digital control unit. Furthermore, the figure highlights main circuital blocks, where all the system blocks occupy $300 \times 200\ \mu m^2$. The nominal supply voltage and the nominal bias current are 1.8 V and 12 μA, respectively. The master clock frequency is 1 MHz, where current spinning frequency is defined as 250 kHz.

The measurement setup is the same as the setup of the horizontal sensor which was shown in Chapter 3. Custom 2-layers printed circuit board (PCB) was designed to measure the 24-pins DIL prototype. The PCB together with the chip are powered by a 5 V power supply, which is used by the components on the mother board to generate two 1.8 V analog and digital power supply and a 0.9 V common-mode voltage.

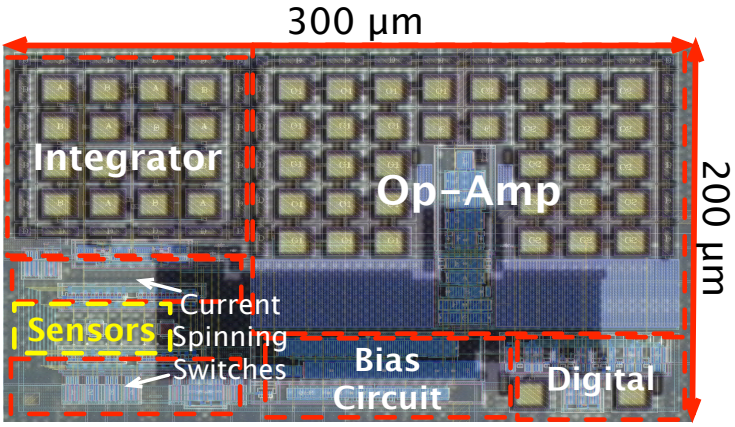
A digital signal generator/analyzer (NI PXI-6552) provides the four phases Φ_{clk}, $\Phi_1 \sim \Phi_4$, Φ_R and Φ_M of Fig. 5.4 for spinning current. The graphical programming tool used is LabVIEW. A Helmholtz coil is used for generating the necessary magnetic field. The two coils are connected in series in order to produce a nearly uniform magnetic field in a region surrounding the centre point of the axis between the two coils [13]. The PCB together with the Hall sensor chip is placed at the centre of the Helmholtz coils in order to apply a magnetic field ranging from 0 to 7 mT.

Table 5.1 summarizes the magnetic and electrical microsystem performance for a biasing current of 12 μA. As can be noticed, the overall sensors area is 80×50 μm^2, in which every sensor occupies 8×8 μm^2. The overall measured power consumption is about 120 μW. The read-out section consumes 54 μW. The sensor and the relevant switches for current spinning measured power consumption is 65 μW.

Measurements have been performed on the available 10 samples. Fig. 5.8 shows the differential output voltage for sample #6 as a function of the applied magnetic field. It ranges from 0 to 7 mT. The bias current is 12 μA. The sensors offset is less



(a)



(b)

Fig. 5.7 Hall sensor microphotograph: (a) whole chip including pads with (b) its back-annotated layout of main circuital blocks.

Table 5.1 Hall Microsystem Performance Summary

Specification	Value	Unit
Technology	0.18	[μm]
Sensor Plate Size	8×8	[μm^2]
Number of Sensors	2	Plate
Active Area	300×200	[μm^2]
Power supply	1.8	[Volt]
Sensitivity	1660	[V/A/mT]
Nonlinearity	$< \pm 0.2$	[$\%_{FS}$]
Measurement Range (B_z)	$0 \sim 7$	[mT]
Power Consumption	120	[μW]
Offset	50	[μT]

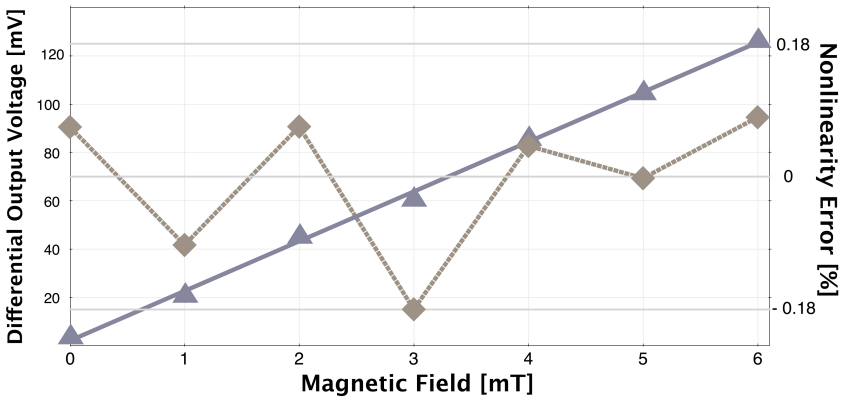


Fig. 5.8 Measured sensor differential output voltages as function of the magnetic field and its nonlinearity error.

than 50 μT and the differential signal has a slope of 20 mV/mT. The nonlinearity error, as Fig. 5.8 shows, is always lower than $\pm 0.2\%_{FS}$ (± 12 μT). Fig. 5.9 shows the measured transient response of the microsystem output voltages in presence of a 6-mT magnetic field. As it can be noticed, during Φ_M, the output voltages take about 30 μs to settle to ±60 mV around the common mode value. At 25 kS/s, the achieved voltage sensor sensitivity after the sensor interface is 1660 V/A/mT.

Finally, the system is compared to state-of-the-art. Table 5.2 summarised the performance of the tested prototype chip and compare it to other horizontal CMOS Hall sensors, which published in literatures. As can be noted, this work as a current-mode approach has high sensitivity and the offset is in good agreement with pervious works. The work used current-mode solution for the first time and described better performances in linearity, area and power consumption.

Table 5.2 Comparison table of this work with other state-of-the-art horizontal CMOS Hall sensors

Refrence	JSCC2005 [14]	JSCC2007 [15]	JSCC2013 [16]	SENSORS2013 [17]	JSCC2014 [18]	This Work
Technology	0.6 µm BiCMOS	0.35 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Supply Voltage	3.3 - 24 V	2.2 - 3.6 V	2 V	3.3 V	5 V	1.8 V
Area	4.9 mm^2	6.44 mm^2	0.6 mm^2	11.25 mm^2	N/A	1.08 mm^2
Hall Sensor Device	4×Cross-Shaped	12×Cross-Shaped	10k Array Pixel	4×Square-Shaped	4×Cross-Shaped	2×Cross-Shaped
Principal Mode	Voltage	Voltage	Voltage	Voltage	Voltage	Current
Spinning Frequency	220 kHz	50 kHz	None	20 kHz	1 kHz	250 kHz
Sensitivity	90 $\mu V/mT$	250 V/AT	50 mV/T	50 mA/T	50 mV/T	1660 V/A/mT
Offset	< 200 µT	10 µT	120 mT	40 µT	25 µT	< 50 µT
Current/Voltage Bias	N/A	350 µA	88 mA	1 mA	350 µA	12 µA
Power Consumption	5.7 mA	30 mW	300 mW	2 mA×3.3 V	N/A	120 µW
Nonlinearity	N/A	< 0.5%	N/A	< 0.08%	N/A	< 0.02%

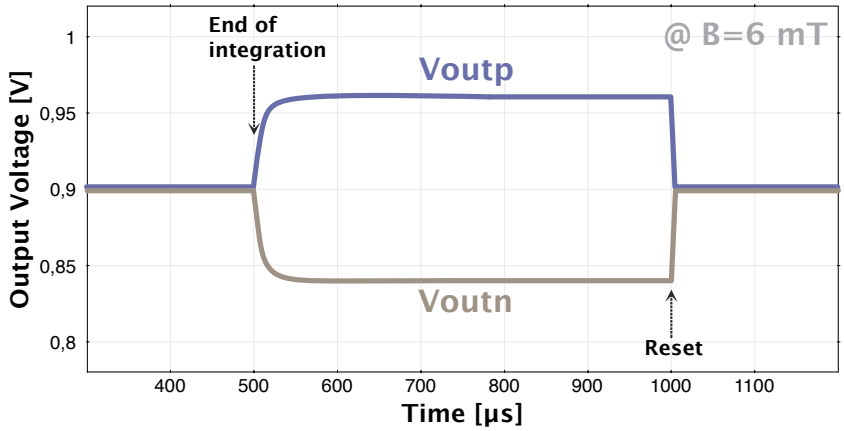


Fig. 5.9 Measured transient response of output voltages.

5.3 Vertical Prototype

This section describes a possible interface circuit to detect and amplify the output currents of the vertical Hall sensor (VHS) which is discussed in Chapter 4. A standard system architecture of a fully integrated vertical current-mode Hall sensor microsystem is shown in Fig. 5.10. It consists of a vertical four-folded three-contact Hall device and a chain of dedicated electronics functions. The main function of the front-end is to improve the sensitivity and decrease the residual offset. The sensor device, bias circuit and switch box to provide the current-spinning are studied in the previous Chapter. The front-end is made up of a chopper integrator amplifier which acts as an I/V converter and a switched-capacitor filter acting as a low pass filter. In the following, these blocks are explained.

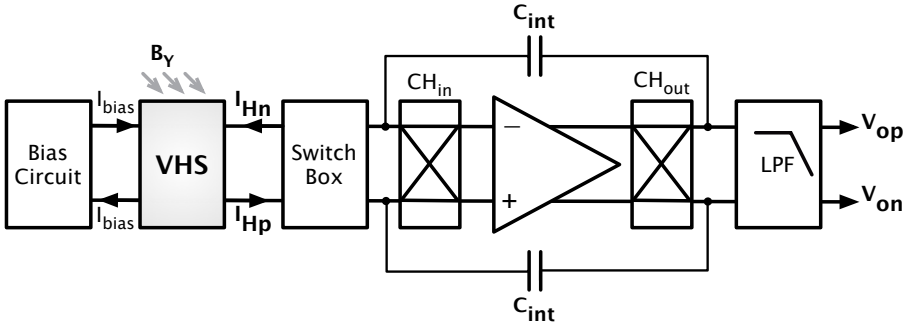


Fig. 5.10 Block diagram of proposed vertical current-mode Hall microsystem.

5.3.1 Readout Circuit

As discussed in Chapter 2, the current spinning technique is used to attenuate sensor offset. An offset cancellation scheme realised by current spinning switches, $\Phi_{CS,i}$, as shown in Fig. 5.11. The current spinning switches, $\Phi_{CS,i}$, are changing periodically from i=1 to i=4. They are connected to an integrating I/V converter in order to amplify the output currents of the sensor and have a desired analog output voltage. The integrator uses a chopping technique to reduce 1/f noise, offset and thermal effects.

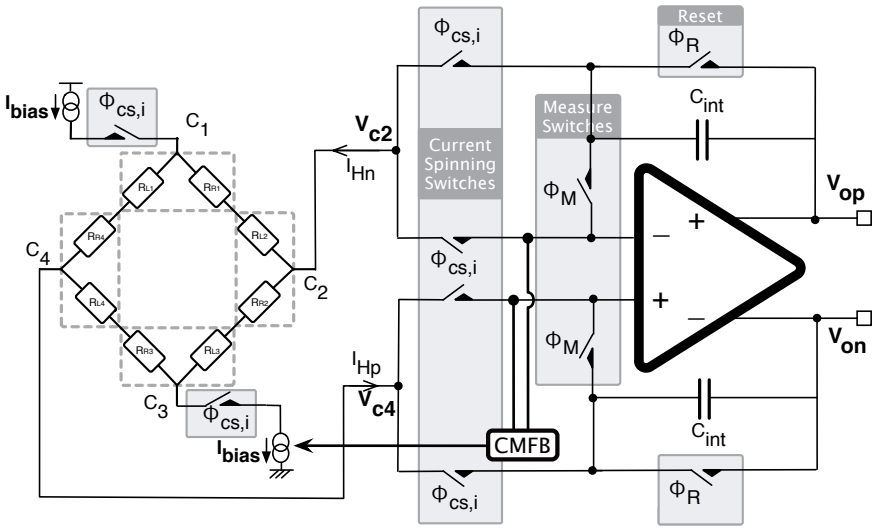


Fig. 5.11 Overall scheme of vertical Hall microsystem configuration.

On the side of enable the current spinning, four phases non-overlapping clocks are used. Four clock phases are defined as Φ_1, Φ_2, Φ_3 and Φ_4. Other clocks used in the readout circuit include a clock used to reset the integrator (Φ_R) and a measure clock (Φ_M) to disconnect the readout circuit from the sensor and hold the output voltage to measure before reset phase, Φ_R. In order to realize of measure phase it is feasible to place measure switch between sensor device and interface, as shown in Fig. 5.12(a). In the current-mode scheme in order to have stability on the sensor device without magnetic field, the outputs must be at same voltage. Accordingly, the request is to have the outputs of the bridge equal:

$$\boxed{\mathbf{V_{c2} = V_{c4}}}$$

If Q is the charge on C_{int} at time t and the voltage across it changes from common-mode voltage (V_{CM}) to positive output voltage (V_{op}), then:

$$Q = (V_{op} - V_{in})C_{int} = I_{Hn}\,t$$
$$V_{op} = V_{in} + \frac{I_{Hn}\,t}{C_{int}} = V_{in} + \frac{1}{C_{int}}\int I_{Hn}\,dt \tag{5.4}$$

The same result for negative output voltage (V_{on}) can obtain as:

$$V_{on} = V_{ip} - \frac{I_{Hp}\,t}{C_{int}} = V_{ip} - \frac{1}{C_{int}}\int I_{Hp}\,dt \tag{5.5}$$

But, if the voltage drop on the measure switches (ΔV) isn't negligible, then:

$$\begin{aligned} V_{c2} &= V_{in} + \Delta V \\ V_{c4} &= V_{ip} - \Delta V \\ since \quad V_{in} = V_{ip} \implies V_{c2} &\neq V_{c4} \end{aligned} \tag{5.6}$$

The problem is V_{c2} and V_{c4} are not equal, which causes an unbalancement at outputs of bridge sensor when there is no magnetic field. Accordingly, this solution isn't applicable for placing of the measure switches between sensor device and readout interface.

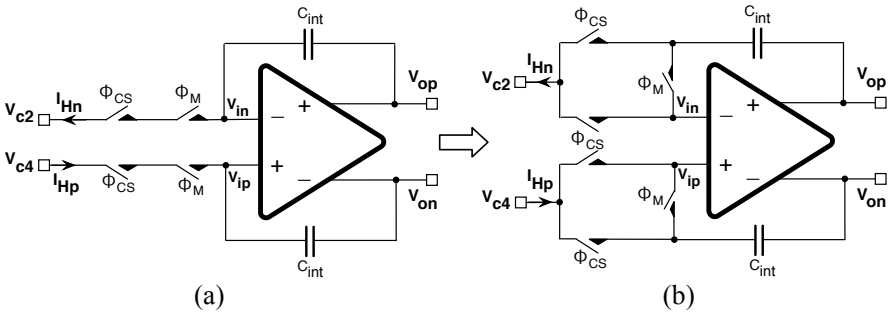


Fig. 5.12 Proposed placement of measure switches, Φ_M, for cancelling of voltage drop across it.

However, in order to cancelling the problem of stability and get proper equal voltage at outputs (V_{c2} and V_{c4}), the scheme of presented in Fig. 5.12(b) is proposed and implemented. Assuming that none of the currents I_{Hn} and I_{Hp} enter the op-amp inputs, then all of the currents flows through integrator capacitors (C_{int}) and charge them up and down, respectively. Therefore, since V_{in} and V_{ip} are virtually shorted, then:

$$\begin{aligned} V_{c2} &= V_{in} \\ V_{c4} &= V_{ip} \\ since \quad V_{in} = V_{ip} \implies V_{c2} &= V_{c4} \end{aligned} \tag{5.7}$$

Consequently, this solution is suitable for placing of the measure switches in the readout interface. In this state, the outputs of integrator during integration can be defined as:

$$V_{op} = V_{in} + R_{on} I_{Hn} + \frac{1}{C_{int}} \int I_{Hn}\, dt \tag{5.8}$$

$$V_{on} = V_{ip} - R_{on} I_{Hp} - \frac{1}{C_{int}} \int I_{Hp}\, dt \tag{5.9}$$

where R_{on} is the on-state resistor of the current spinning switch.

However, at the measure time, Φ_M, when current spinning switches are open and measure switches are close, the outputs can be achieved by:

$$V_{op} = V_{in} + \frac{1}{C_{int}} \int I_{Hn}\, dt \tag{5.10}$$

$$V_{on} = V_{ip} - \frac{1}{C_{int}} \int I_{Hp}\, dt \tag{5.11}$$

The operation of the readout circuit proceeds as following shown in Fig. 5.13. During phase Φ_1, a current bias is injected into terminal C_1 and a same bias current is drawn from the non-adjacent terminal of C_3. At the same time, a current of I_{Hn} enters into terminal C_2 and the same current of I_{Hp} exits from C_4 because of unbalancement of an external magnetic field. As a matter of fact, the Hall sensor produces a differential output current (I_{Hall}), which is the input of I/V converter. During this period, the I/V converter is connected to a sensor and I_{Hall} is integrated over a capacitor (C_{int}). In this phase, Φ_M and Φ_R are disconnected.

At the same time as phase Φ_2, the connections of terminal contacts are changed with 90° clockwise rotation. Concurrently, terminals C_2 and C_4 are linked to current biases, while, current outputs terminals I_{Hp} and I_{Hn} are generated at terminals C_1 and C_3, respectively. The I/V converter is connected to the same sensor as Φ_1. The Hall current, I_{Hall}, is still integrated and Φ_M and Φ_R are disconnected. The subsequent current spinning technique to offset suppression is achieved by repeating the exchange bias in Φ_3 and Φ_4.

In the time of phase Φ_M, the readout electronics is disconnected from sensor, completely. At this time, the last value of integration holds for measure.

For the time being reset phase, Φ_R, the interface still is disconnected from the sensor and the integrator resets after Φ_M.

The two stage fully differential telescopic op-amp scheme used in analog front-end of vertical Hall sensor microsystem is shown in Fig. 5.14.

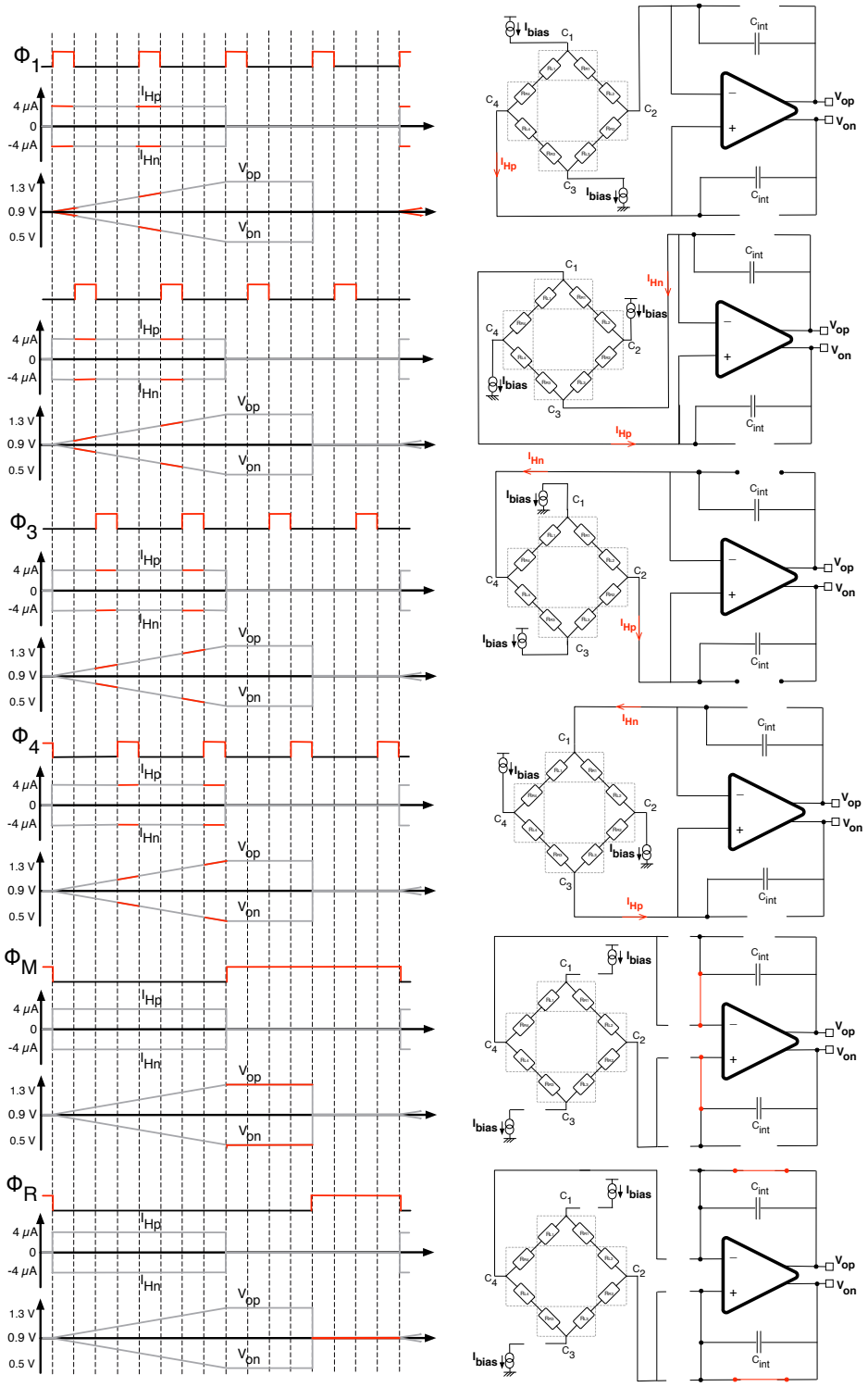


Fig. 5.13 Vertical Hall microsystem operations of driving phases Φ_1, Φ_2, Φ_3, Φ_4, Φ_M and Φ_R.

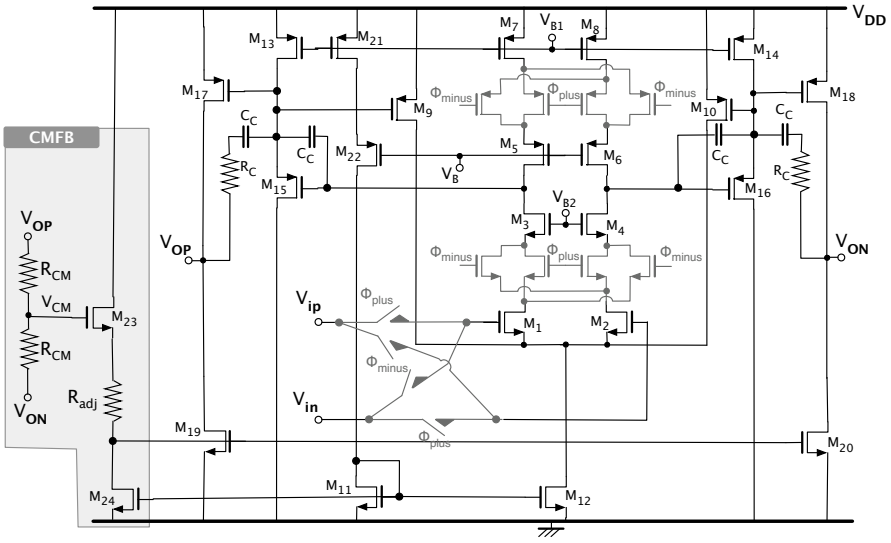


Fig. 5.14 Circuit schematic of used op-amp in analog interface of vertical Hall sensor.

A discrete-time resistance common-mode feedback (CMFB) is used because of more linearity compare to continuos-time. The M_9 and M_{10} transistors are part of this CMFB, where adjusting resistor (R_{adj}) is a off-chip resistor. The biasing voltages V_B, V_{B1} and V_{B2} are generated by a bias voltages (not shown in the figure) while V_{CM} is the common-mode voltage.

In order to have a good stability and phase margin C_C and R_C are used as a Miller compensation between first stage output, level shifter and second stage output. Their values are 1.5 pF and 5 kΩ, respectively. The obtained phase margin value is 60° degree. A source follower P-channel level shifter (M_{15} and M_{16}) used between first and second stages to providing required upward voltages of output stage transistors (M_{17} and M_{18}).

In the interest of cancel offset a chopped technique is used. This part of op-amp shown by grey colour in Fig. 5.14, which are derived by two Φ_{plus} and Φ_{minus}. These phases are generated by a no-overlapping phase generator in digital unit.

The simulated DC gain and gain bandwidth product (GBW) under typical conditions are 110 dB and 11 MHz with 2 pF capacitive load.

5.3.2 Switches and Digital Control Unit

The functionality of the design architecture is provided by closing or opening corresponding signal paths. The digital control defines four phases of current spinning, reset, integration cycles, and non-overlap clocks for chopper and switched-capacitor

filter. All signal paths are routed by employing CMOS complementary switches. The implementation of the 24 switches in order to realise current spinning technique is shown in Fig. 5.15.

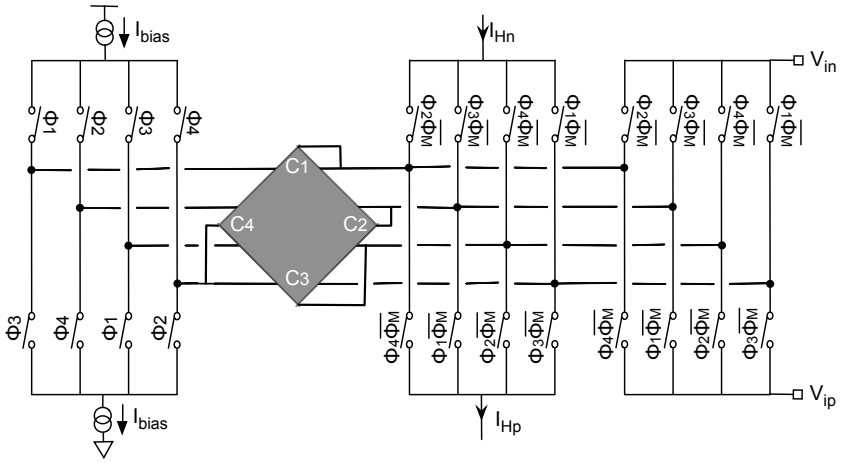


Fig. 5.15 Implementation of the four-phase current spinning technique for the vertical Hall sensor.

The switches are driven by six different control signals which are shown in Fig. 5.16. The non-overlapping clock signals from Φ_1 to Φ_4 are used for driving the current spinning switches during the integration time. Φ_R performs the reset after the integration, while the signals are held for measuring before the reset by Φ_M.

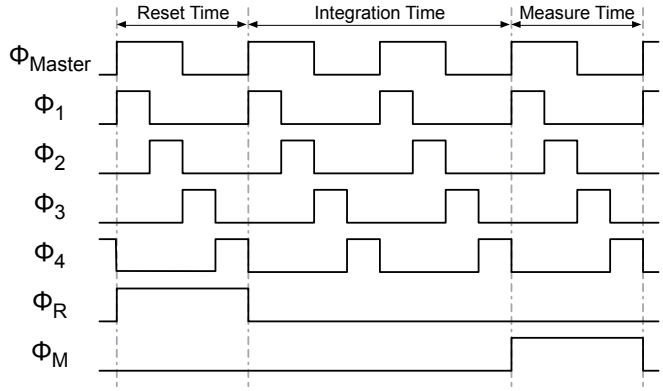


Fig. 5.16 Diagram and timing sequence of the six-phases for controlling of the current spinning during integration, reset and measure time.

5.3.3 Switched-Capacitor Filter

The output voltages of the integrator can be directly connected to output pads. The drawback of this topology is that there is no load capacitor compensation and a big capacitance loads the opamp output, thus slowering the operation and introducing the risk of instability. Another method is to employ a switched-capacitor filter in its signal path to filter the ripple out and to isolate the internal operation from external reading. The circuit acts like a switched-capacitor network whose function is equivalent to an RC low pass filter.

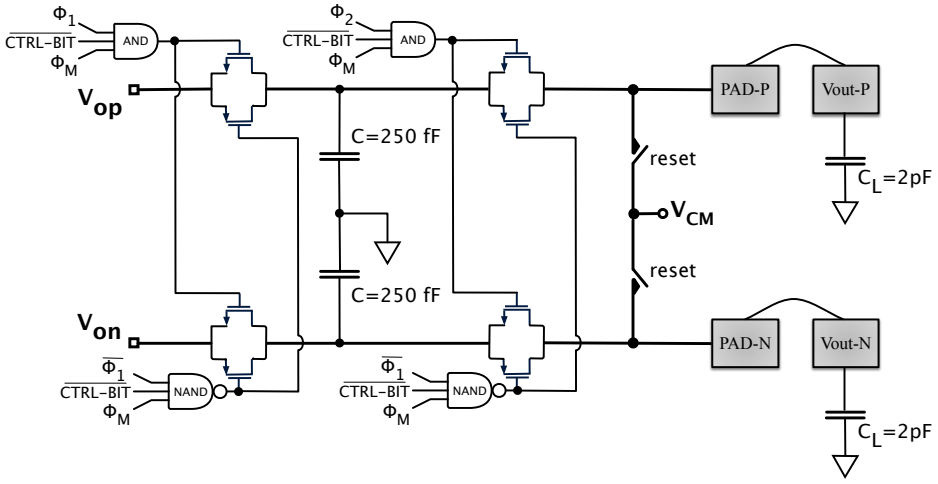


Fig. 5.17 Proposed switched-capacitor filter as a output circuit of magnetic Hall microsystem.

Fig. 5.17 shows the proposed switched-capacitor filter as a output circuit of vertical magnetic Hall microsystem. In order to realise that, four complementary switches are used. The switches are controlled by Φ_1 and Φ_2 phases, which are applying to a AND gate for NMOS and a NAND gate for PMOS transistors during the measure clock phase, Φ_M. At reset time, the outputs go back to common-mode voltage. The values of SC and load capacitors are 250 fF and 2 pF, respectively.

5.3.4 Measurement Results

This section describes the experimental results of the proposed VHS with related analog front-end. First the design of the testing board and measurement setup is explained. After that, the measurement results are discussed.

An experimental prototype of the VHS and its readout is fabricated in a standard 0.18 μm CMOS technology.

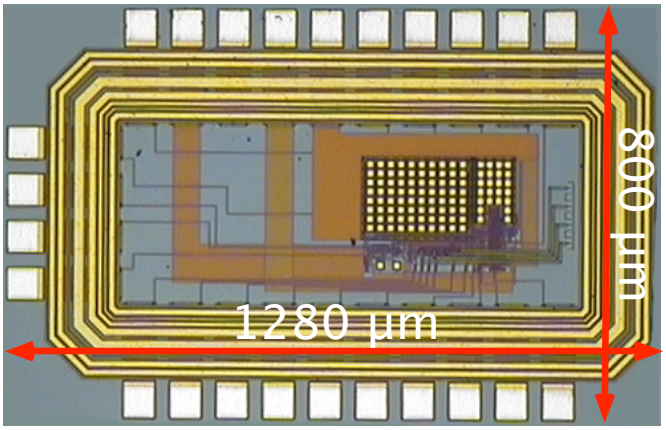


Fig. 5.18 PVVHSREADOUT chip microphotograph.

Fig. 5.18 shows the chip microphotograph, whose main circuital blocks are highlighted in Fig. 5.19. The chip occupies an area of 1280×800 μm^2, whereas the active area of core chip is 300×230 μm^2.

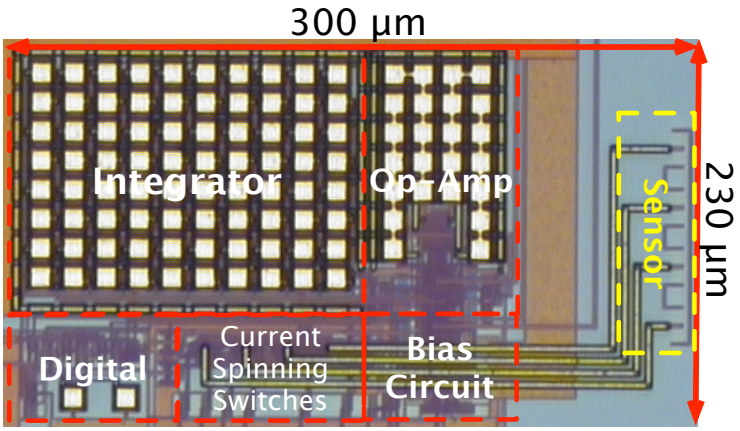


Fig. 5.19 Main circuital blocks of the vertical Hall sensor with integrated interface.

The 24-pins of the chip are connected directly to PCB. Custom printed circuit boards (PCBs) were designed to measure the prototype, which includes a mother-board and a baby board. Fig. 5.20 shows the top layer of the motherboard designed in Altium Designer software, where Fig. 5.21 illustrates the fabricated board with soldered components.

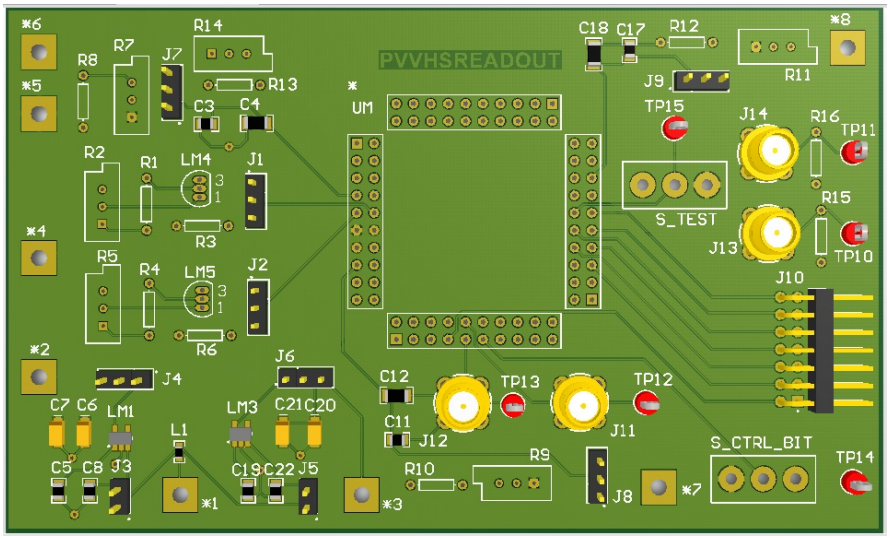


Fig. 5.20 3D Top layer of the BCB board test in Altium.

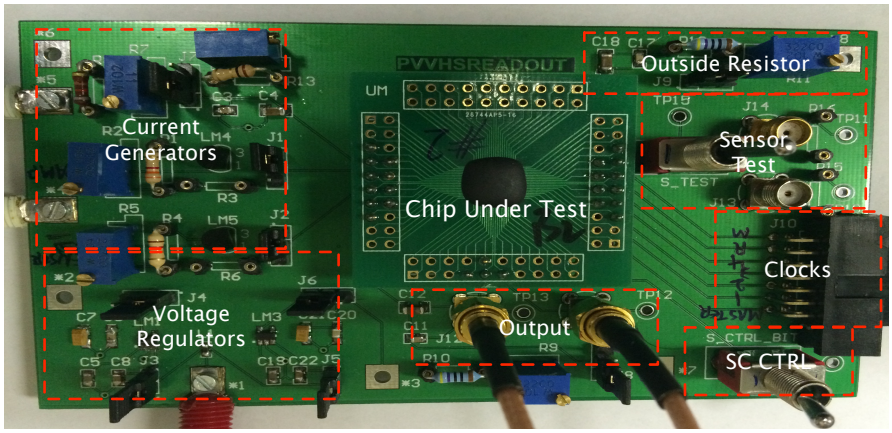


Fig. 5.21 Fabricated test board with components soldered.

In order to avoid any interferences between the digital and analog parts, the motherboard uses two different power supply VDD and DVDD. These reference voltages are regulated by two voltage regulators (LM4120) on PCB. The top layer plane is connected to VDD, where the bottom layer plane is GND. The common-mode and bias voltage of the test signal going into the chip is set through 6 matching resistors connected to a voltage reference on the PCB. This common-mode voltage can be adjusted using a variable resistor (trimmer) but is nominally at half the voltage supply (0.9 V). Both bias currents for the op-amp and the sensor were provided by two current generators (LM234) on the motherboard. The main parts of the designed board include the current generators, the voltage regulators, the clocks header and the output SMA connectors have been highlighted in the figure. The baby board uses a 80-pin socket (24 pins are connected to the chip) to hold the chip, allowing the replacement of other samples during measurement.

Fig. 5.22 shows the block diagram of the measurement setup. An Helmholtz coil with dimensions of $20 \times 36 \times 38\ cm^3$ was used in order to produce an external magnetic field up to 10 mT. Furthermore, a Digital Teslameter shows the exact value of magnetic fields inside of the Helmholtz coil.

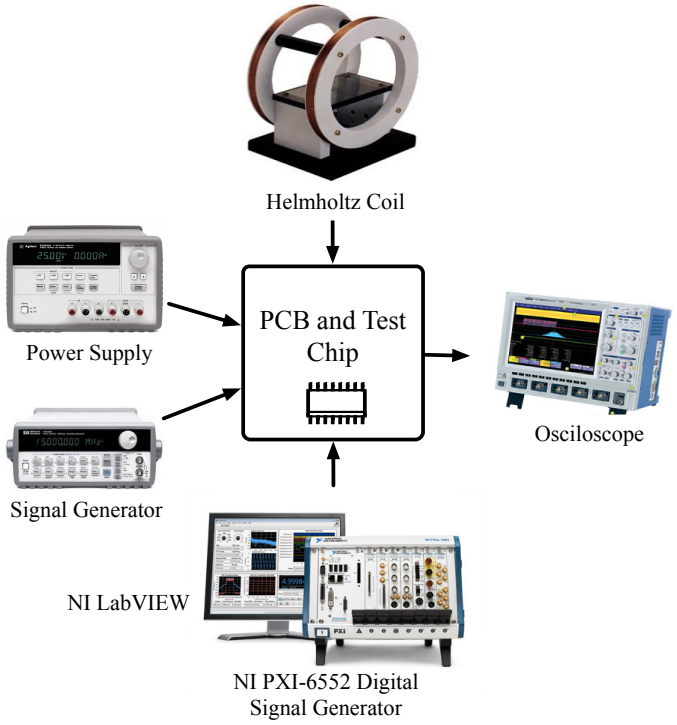


Fig. 5.22 Used measurement setup.

In order to enable measurements automation, data are collected using Data Acquisition Board NI PXI 6552 by National Instruments and a data acquisition software is implemented using LabVIEW.

Table 5.3 summarizes the magnetic and electrical microsystem performance. The measured sensitivity after interface is 2400 V/A/mT where the magnetic equivalent offset is about 40 μT. The overall measured power consumption is 900 μW. The readout section consumes 360 μW. The Sensor and relevant switches for current spinning measured power consumption is 540 μW.

Table 5.3 PVVHSREADOUT Microsystem Performance Summary

Specification	Value	Unit
Technology	CMOS 0.18	[μm]
Sensor Plate Size	150×7.44	[μm^2]
Chip Area	1280×800	[μm^2]
Active Area	300×230	[μm^2]
Power supply	1.8	[Volt]
Measurement Range (B_z)	0 ~ 10	[mT]
Sensitivity	2400	[V/A/mT]
Offset	40	[μT]
Spinning Frequency	10	[kHz]
Chopper Frequency	5	[kHz]
Power Consumption	900	[μW]

Fig. 5.23 shows the integrator output voltages measured with low capacitive active probes. The chopper frequency has been chosen to 5 kHz for a 10 kHz spinning frequency to emphasize the integration of the offset each spinning period. It results spur signals as large as few hundreds of milli-Volt cancelled out at the end of the spinning cycle. For a bias current equal to 50 μA and an applied magnetic field of 2.5 mT, the final differential output voltage is the expected 300 mV after three current spinning periods (300 μs).

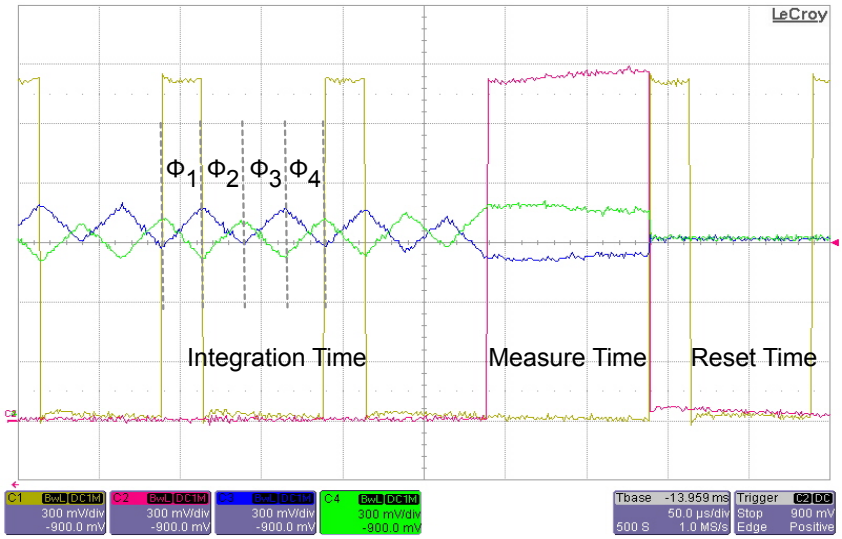


Fig. 5.23 Output Voltage transient response measured with active microprobe.

References

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Chapter 6
Conclusions

This thesis has focused on two classes of magnetic Hall sensor structures in current domain. First, a twin horizontal Hall sensor operating in current-mode and able to provide differential currents at the output nodes has been fabricated in a standard 0.18-μm CMOS process. After that, a four-folded vertical Hall sensor has been implemented and fabricated in the same CMOS technology. Afterwards, these Hall sensors have been integrated with a readout circuit in a single chip to increase the magnetic sensitivity.

In another point of view, the sensors have been optimized on two structural levels: device level and device-interface electronics level. On device level, a horizontal and a vertical Hall sensors have been explained in Chapter 3 and Chapter 4, respectively. On device-interface electronics level, it has been shown that both the design of a Hall device and the interface electronics are crucial to increase the sensitivity, as discussed in Chapter 5.

Measurement results show that both types of Hall sensor achieve a high sensitivity when an external magnetic field is applied. The use of symmetric Hall plates and a current-mode approach enables current spinning technique for offset cancellation. The power consumption in both horizontal and vertical microsystems is in the range of tens of μW.

6.1 Highlights

The following list summarizes the highlights of the system design and performance:

- A new current-mode approach has been proposed and applied to both horizontal and vertical Hall magnetic sensors. The benefit of the work in current domain is having an output current instead of an output voltage used in conventional Hall sensors. The current output can be easily integrated with an integrator and converted to an analog voltage reference needed for an analog to digital converter (ADC). The higher resolution in the low magnetic fields is one of the benefits of the current-mode Hall sensors using high mobility plate. In order to integrate Hall sensors using current-mode approach, the number of terminals can be reduced. Therefore, the ultimate miniaturization of the system will be easier. Due to the general trend in microelectronics towards scaling and thanks to these advantages, the current-mode Hall sensor is bound to become more popular in the future.

- The current spinning technique has been discussed for current-mode Hall sensors. The spinning current technique allows to strongly reduce the offset of Hall sensors. The use of the symmetric Hall plate enables to apply the current spinning technique. Using this technique, the Hall plate offset can be reduced to about 50 ~100 μT.

- A system level behavioural model has been developed using FEM simulation. The proposed scheme applies to a two-dimensional model of the Hall plate simulated in COMSOL Multiphysics. Furthermore, the geometry and temperature influence of the proposed sensors have been studied.

- The models for horizontal and vertical sensor have been described in behavioral Verilog-A language and tested on a Cadence Spectre simulator tool using technological parameters of a 0.18 μm CMOS technology. Modelling of the sensors in Cadence environment allows to optimize readout circuit considering non-idealities and sensor versus electronics interference.

- An I/V converter has been designed and integrated as analog front-end. It consists of a chain of dedicated electronics functions. The main function of the front-end is to improve sensitivity and decrease the residual offset. The front-end is made up of a chopper integrator amplifier which acts as an I/V converter and a switched-capacitor filter as a low pass filter. The use of a low-noise chopper stabilized operational amplifier enables the cancelation of offset, whereafter integration of the signal current and ensures superior voltage sensitivity.

- An experimental setup for magnetic field measurements has been developed. The three PCB boards have been designed by Altium Designer and fabricated for every chip. The three prototypes have been measured and tested. The results proved the feasibility of building a magnetic Hall sensor based on current-mode for horizontal and vertical structures.

6.2 Outlook

This study allows to critically analize aspects of magnetic Hall sensor microsystems. The main goals of this project were the implementation of sensor device in the CMOS technology and the reduction of related residual offset. To that end, several different symmetric horizontal and vertical Hall sensors have been implemented and measured. The CMOS Hall sensors designed and verified during the thesis were proof of concepts. The magnetic sensors can be further optimized for low fields in both horizontal and vertical classes. A next step is the integration of the entire microsystem with internal clock generator and an ADC for a digital output. As future perspective in biomedical application, a Hall sensor can be integrated in the same CMOS IC together with the transceiver of the NMR system to deal with temperature and position variation of the sample.

Appendix A
Layout Description

The additional material presented in this appendix, aims to show the layout description of the main blocks used to implement the Hall magnetic sensor prototypes of Chapter 3, Chapter 4 and chapter 5. The first layout corresponds to the design of the Horizontal Hall-Effect Current-Mode Magnetic Sensor (PVHALLREADOUT). The second layout describes the design of the Four Vertical Four-Folded Magnetic sensor devices (PVVHSSENSORS) and the last layout explains the Vertical Hall Magnetic Sensor with High Sensitive Readout (PVVHSREADOUT). The layout of the sensor devices, integrator, switched-capacitor (SC) implementation of the filters as well as the different analog and digital blocks involved in the design of the three prototypes are shown in detail.

A.1 First Chip Layout Description (PVHALLREADOUT)

The following figures show the layout of the horizontal Hall sensor with analog front-end (PVHALLREADOUT):

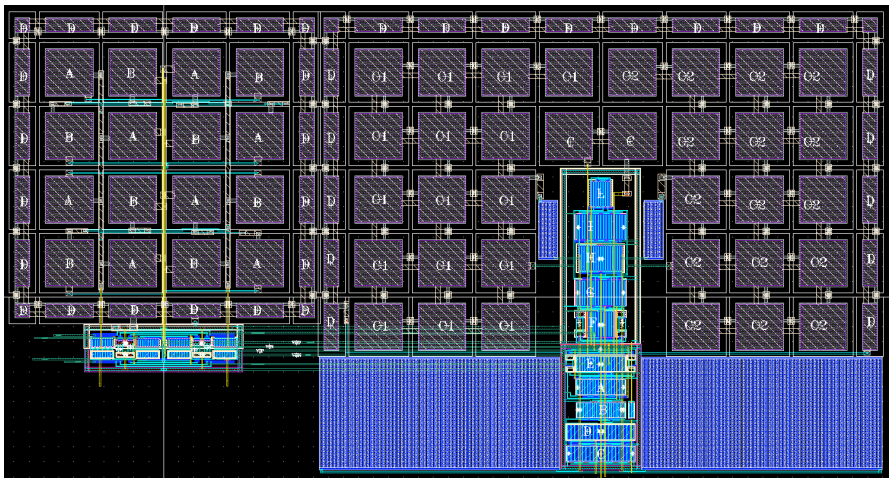

Fig. A.1 Layout of the integrator readout interface including a fully differential telescopic Op-Amp with discrete-time CMFB.

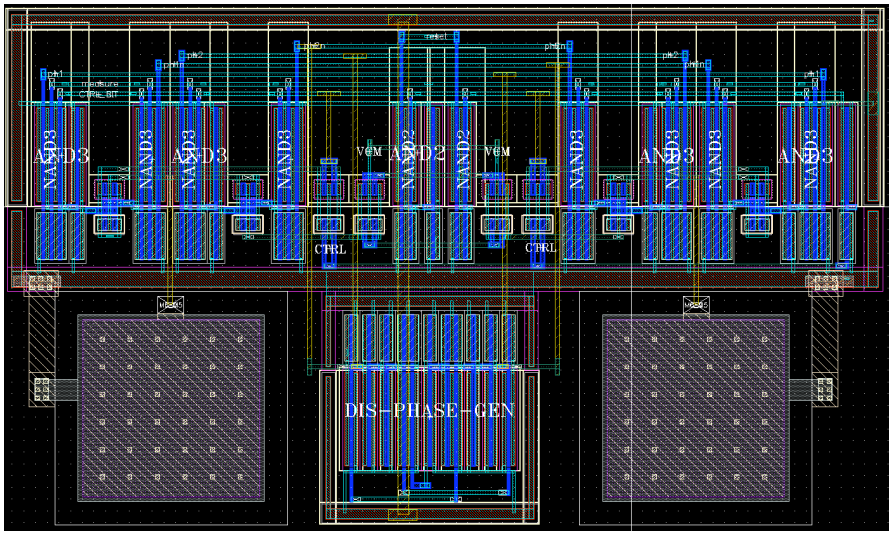

Fig. A.2 Switched-capacitor filter layout including a non-overlapping phase generator for chopper phases and other digital parts.

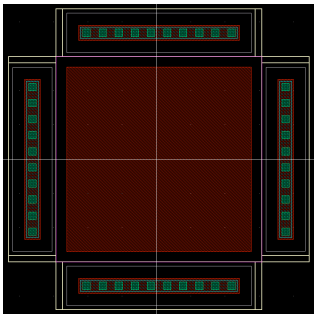

Fig. A.3 Sensor plate layout including four metal1 to N^+ high doped contacts and a low doped N-well, which is covered by a shallow highly doped P^+.

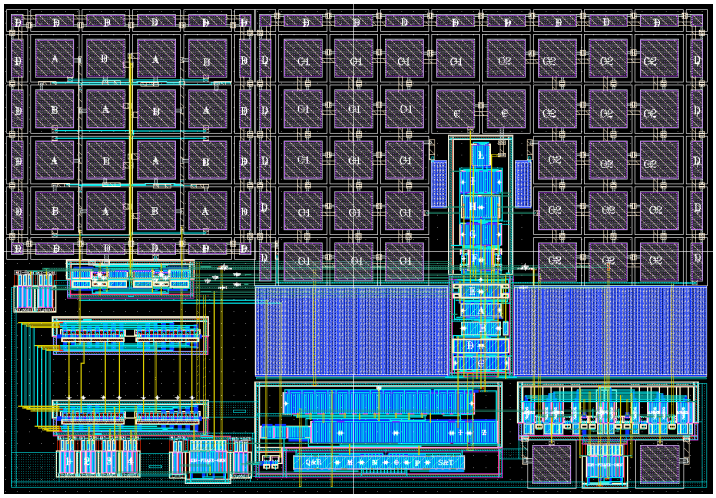

Fig. A.4 Full view of the layout chip core including the op-amp, the digital control unit, the bias and the current spinning switches.

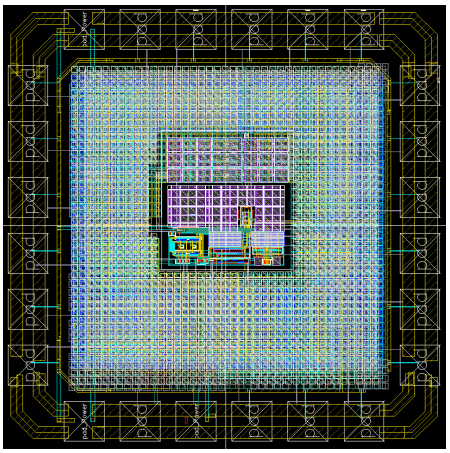

Fig. A.5 Top view layout of whole horizontal Hall sensor including pad-ring and density filled.

A.2 Second Chip Layout Description (PVVHSSENSORS)

The following figures present the layout of the multi-sensor Hall system (PVVHSSENSORS):

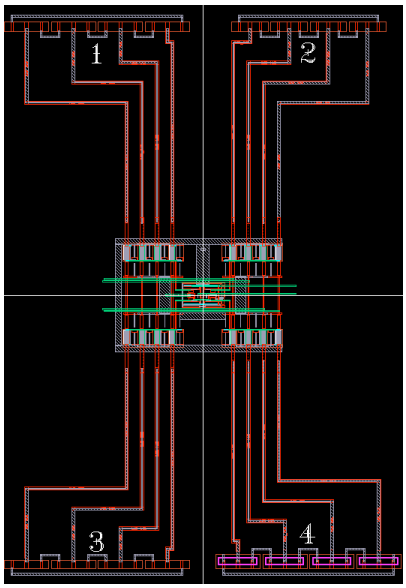

Fig. A.6 Layout of chip core including a multiplexer with four different vertical Hall sensor.

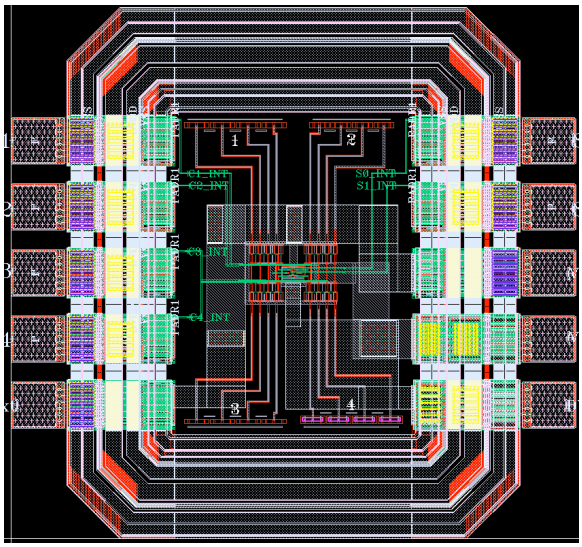

Fig. A.7 Top view layout of vertical Hall sensor including the pad-ring.

A.3 Third Chip Layout Description (PVVHSREADOUT)

The following figures show the layout of the vertical Hall sensor with analog front-end (PVVHSREADOUT):

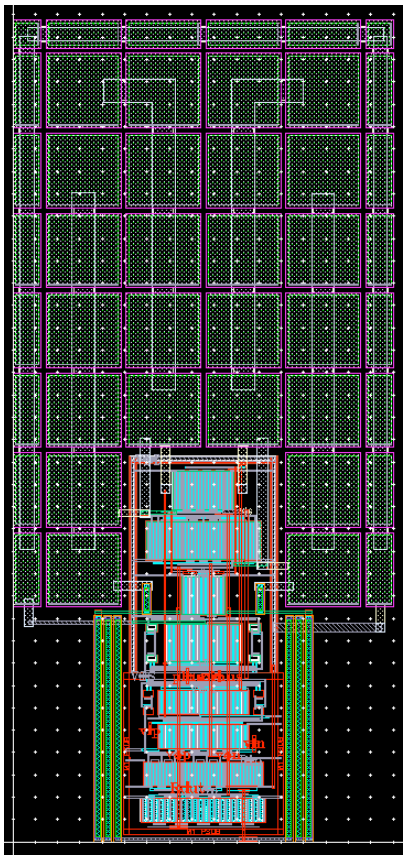

Fig. A.8 Layout of the fully differential telescopic Op-Amp with discrete-time CMFB.

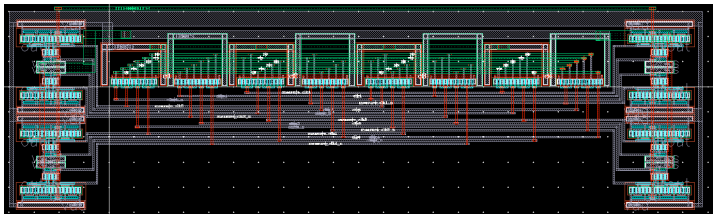

Fig. A.9 Switch box includes 32 switches for the implementation of the current spinning technique.

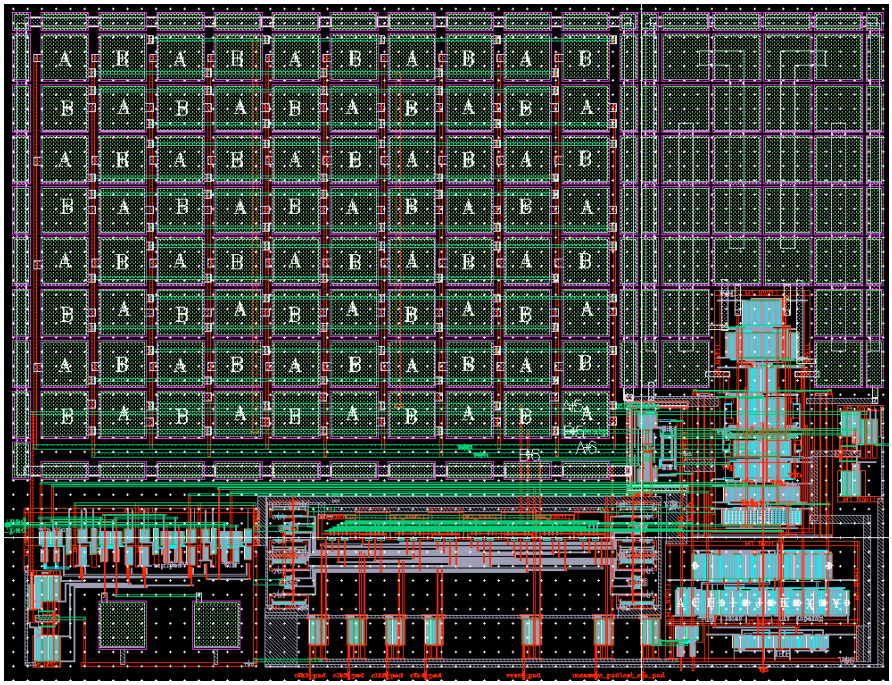

Fig. A.10 Core layout of vertical Hall sensor including switched-capacitor filter, analog readout circuit, digital parts and current spinning switches without pad-ring.

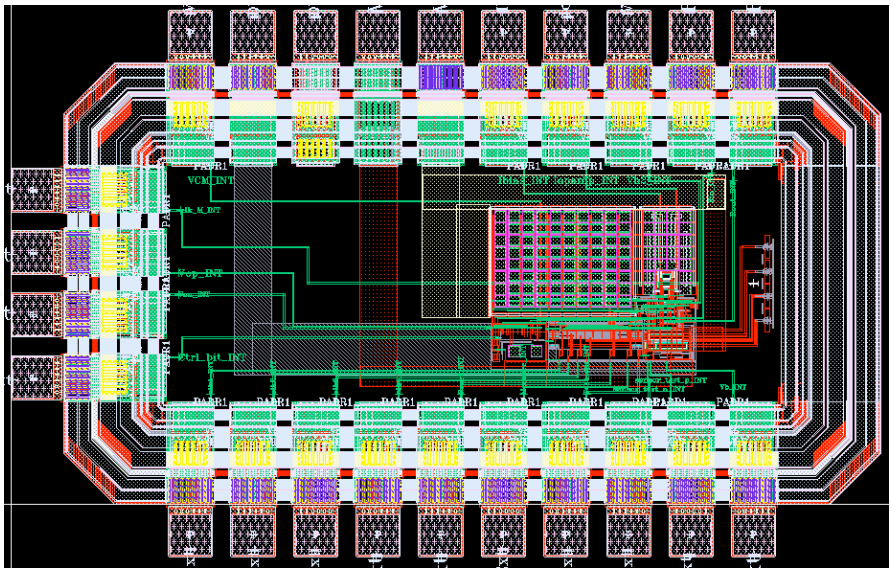

Fig. A.11 Top view layout of vertical Hall sensor with analog front-end and its padring.

Appendix B
Hall Effect Model Considerations in COMSOL Multiphysics

This Chapter is dedicated to 2D model simulation of an horizontal Hall sensor in COMSOL. Simulation modelling of Hall devices allows designers to avoid repeated building of multiple chip prototypes to analyze designs for new or existing parts. Before creating the chip prototype, users can virtually investigate many digital prototypes and can optimize some performance such as geometry, sensitivity and offset.

The basics of the Hall effect have been described in detail in Chapter 2. In fact, the Hall plate simulated in COMSOL environment is subject to a magnetic field. The magnetic field is introduced into the current flow region of the solid of Hall effect measurements, effectively. It adds an anisotropic term into the conductivity of a nominally homogenous, isotropic solid material. The anisotropic conductivity is caused by the magnetic field through the Lorentz force. The Lorentz force produces a proportional, differential voltage/charge/current accumulation between two output terminals [1].

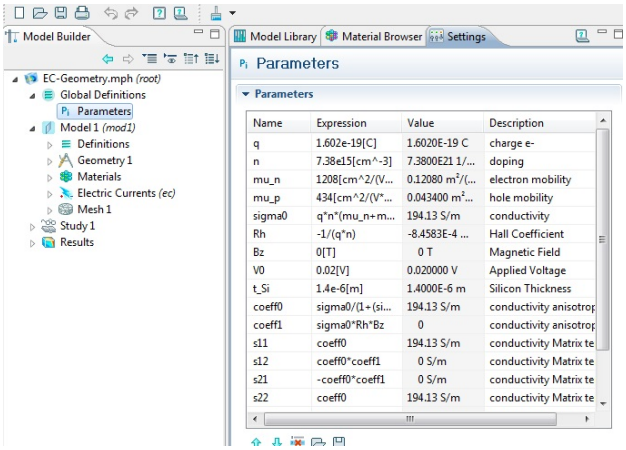

Fig. B.1 Model Parameters.

To start building Hall-Effect model, after activating of the COMSOL software, in model navigator the ”2D Model” has been selected. The parameters are first imported in the ”Parameters” edit window, as shown in Fig. B.1. These parameter values are taken from a standard 0.18 μm CMOS technology.

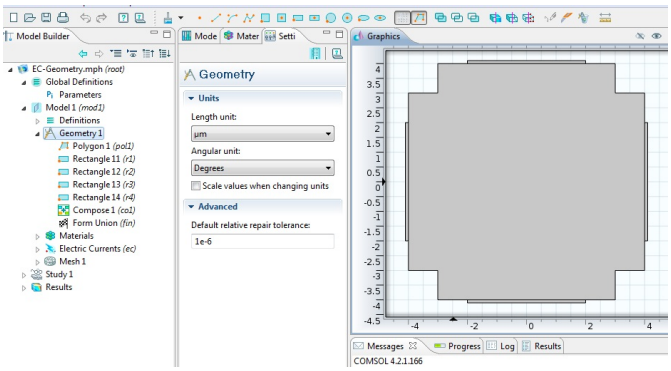

Fig. B.2 Model Geometry.

Using the menu bar in ”Model 1”, the proper shapes have been drawn. As can be noted in Fig. B.2 a polygon is used for cross-shaped plate and four rectangle are employed as four contact terminals.

After drawing the geometry, it is possible to add materials to designed model from ”Materials” icon below Geometry, as shown in Fig. B.3. Here, for Hall plate a ”Silicon (single-cristal)” material was used, where the contact terminals were made up by ”Copper”. The materials are chosen from ”Material Browser”.

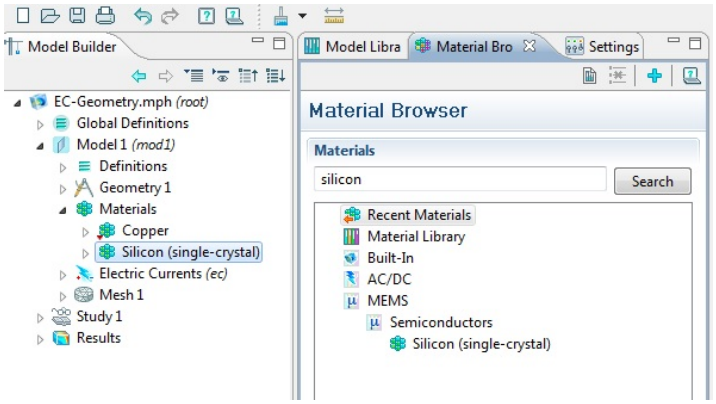

Fig. B.3 Model Materials.

In order to add a physics area, by right clicking on Model icon, it is possible to choose ”Electric Currents (ec)” as proper physics for modelling the magnetic field application. Fig. B.4 shows the selected physics and its content to introduce an anisotropic region in Hall plate.

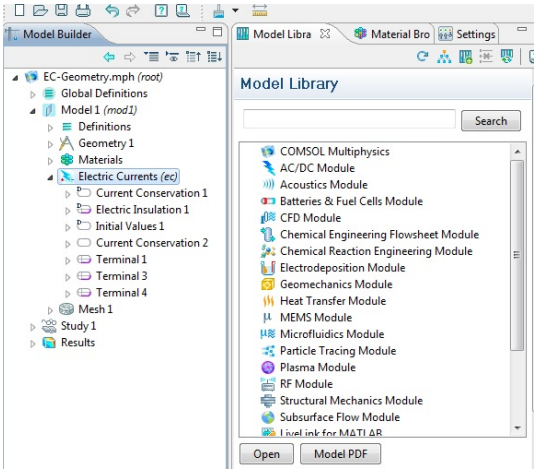

Fig. B.4 Model physics.

According to ”Current Conversation”, it can be defined the electrical conductivity of the plate in anisotropic and contact terminals in isotropic, as shown in Fig. B.5.

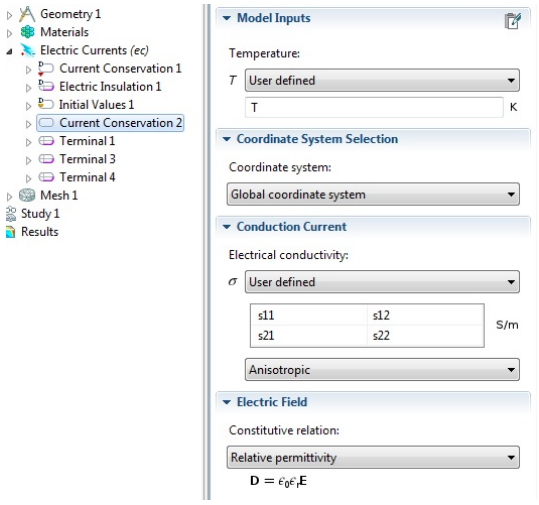

Fig. B.5 Model physics.

In ”Electric Currents (ec)” physics also the input and output terminals must be specified. As Fig. B.6 shows, a 12 µA current is injected to ”Terminal 1”, while the ”Terminal 3” and ”Terminal 4” are grounded. Using ”Mesh” icon in bottom of physics, a proper ”Mesh” is generated for the model.

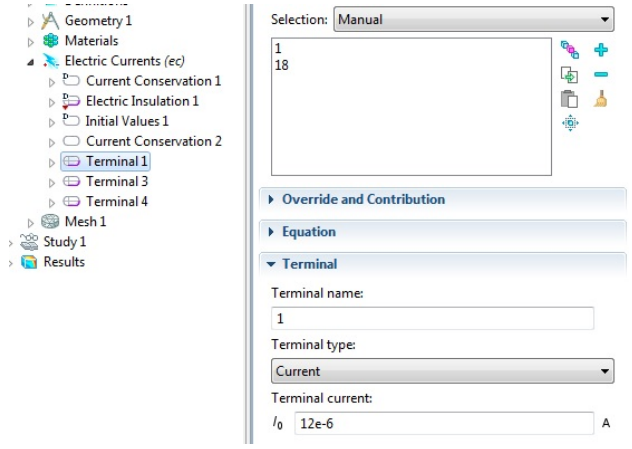

Fig. B.6 Model physics.

In order to apply the magnetic field, a ”Parametric Sweep” is chosen in the ”Study” section, as shown in Fig. B.7. This allows the modeller to see solutions for a wide range of magnetic field values. Here, the range of magnetic field is from 0 to 20 mT. Furthermore, a ”Step 1: Stationary” is picked, so that the modeller can solve the Model over a range of B_Z, as defined in ”Parametric Sweep”.

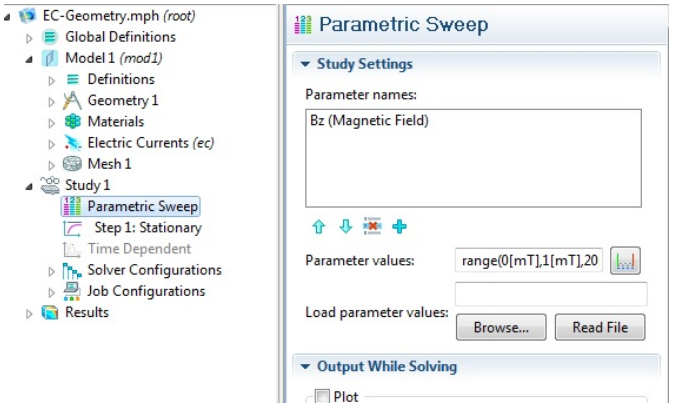

Fig. B.7 Model Study.

The default plot is a 2D surface plot of the voltage distribution at the highest value of the magnetic field (B_Z=20 mT), which appears after the numerical solving the Model, as shown in Fig. B.8.

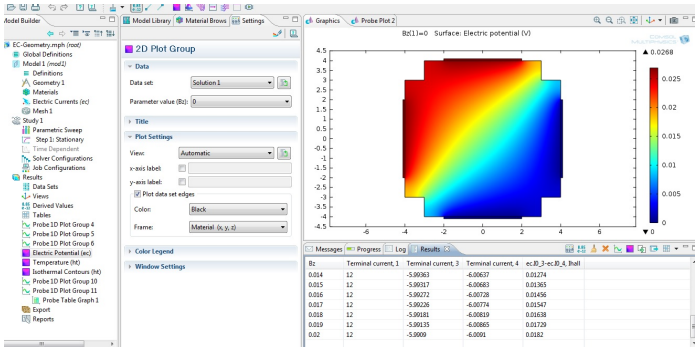

Fig. B.8 2D plot electric potential result.

More detailed information are displayed by adding contour lines. Using the ”Definitions” icon, above the Geometry, the outputs can be selected which are presented by an 1D plot graph. Fig. B.9 shows the output terminals 3 and 4 as a function of magnetic field.

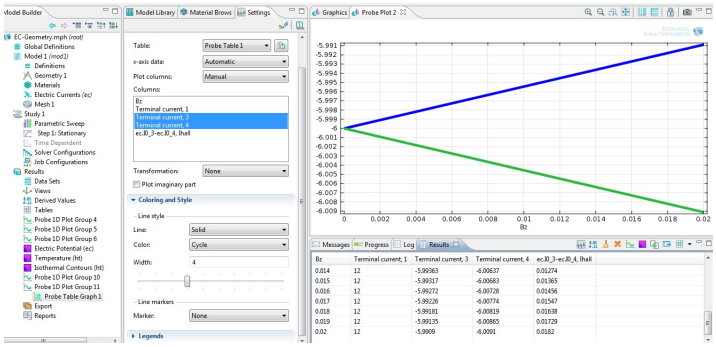

Fig. B.9 1D plot graph result.

References

1. R. W. Pryor, *Multiphysics Modeling Using COMSOL: A First Principles Approach*. Jones and Bartlett Publishers, 2009.

Appendix C
List of Publication

Publications related to this PhD research:

1. **H. Heidari**, E. Bonizzoni, U. Gatti and F. Maloberti, "A CMOS Current-Mode Magnetic Hall Sensor", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 11, No. 4, May 2015. (Under Review)

2. **H. Heidari**, E. Bonizzoni, U. Gatti and F. Maloberti, "A 0.18-μm CMOS Current-Mode Hall Magnetic Sensor with Very Low Bias Current and High Sensitive Front-End", *Proc. of IEEE Sensors*, pp. 1467–1470, November 2014, Valencia, Spain.

3. **H. Heidari**, E. Bonizzoni, U. Gatti and F. Maloberti, "Analysis and Modeling of Four-Folded Vertical Hall Devices in Current Domain", *Proc. of IEEE Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 1–4, July 2014, Grenoble, France. (Gold leaf award)

4. **H. Heidari**, E. Bonizzoni, U. Gatti and F. Maloberti, "A Current-Mode CMOS Integrated Microsystem for Spinning-Current Hall Magnetic Sensors", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 678–681, June 2014, Melbourne, Australia. (ISCAS honorary mention for best paper award)

5. **H. Heidari**, U. Gatti, E. Bonizzoni and F. Maloberti, "Low-Noise Low-Offset Current-Mode Hall Sensors", *9th IEEE Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 325–328, June 2013, Villach, Austria.