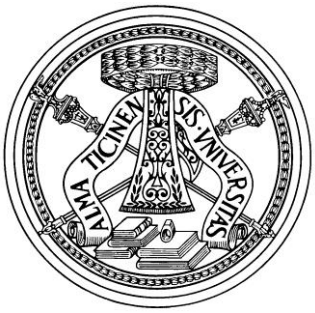

UNIVERSITA' DEGLI STUDI DI PAVIA

FACOLTA' DI INGEGNERIA

Dottorato di Ricerca in Microelettronica, XXVI CICLO

High Speed Analog CMOS Equalizer for Optical Fiber Dispersion in Next Generation Data Center Networking

Tutor:

Prof. Andrea Mazzanti

Ph.D Dissertation of

Enrico Mammei

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Publications

- E. Mammei, F. Loi, F. Radice, A. Dati, M. Bruccoleri, M. Bassi, A. Mazzanti, "A Power-Scalable 7-Tap FIR Equalizer with Tunable Active Delay Line for 10-to-25Gb/s Multi-Mode Fiber EDC in 28nm LP-CMOS," *in IEEE ISSCC Dig. Tech. Papers*, 2014, pp.142-143.

- E. Mammei, F. Loi, F. Radice, A. Dati, M. Bruccoleri, M. Bassi, A. Mazzanti, "Analysis and Design of a Power-Scalable Continuous-Time FIR Equalizer for 10-Gb/s to 25-Gb/s Multi-Mode Fiber EDC in 28-nm LP CMOS," in *IEEE J. of Solid State Circuits*, vol. 49, no. 12, Dec. 2014.
- E. Mammei, E. Monaco, A. Mazzanti, F. Svelto, "A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz Minimum Noise FOM Using Inductor Splitting for Tuning Extension," *in IEEE ISSCC Dig. Tech. Papers*, 2013, pp.350-351.
- F. Svelto, A. Ghilioni, E. Monaco, E. Mammei, A. Mazzanti, "The Impact of CMOS scaling on the Design of Circuits for MM-Wave Frequency Synthesizers," in High-performance AD and DA Converters, IC Design in Scaled Technologies, and Time-Domain SignalProcessing, Springer 2014.

Abstract of the Dissertation

Analysis and Design of a Power-Scalable Continuous-Time FIR Equalizer for 10Gb/s to 25Gb/s Multi-Mode Fiber EDC in 28nm LP-CMOS

by

Enrico Mammei

Doctor of Philosophy in Microelectronics

University of Pavia, Pavia, 2014

Professor Andrea Mazzanti, Chair

The ever increasing demand for higher communication bandwidth is pressuring the industry to produce links with much faster data rates. For example, the current optical links with data rates of 10Gbps need to be upgraded to data rates of 25Gbps and over. However, such a data rate increase will cause severe optical dispersion which will in turn reduce the usable channel length. To regain this channel length loss, the dispersion needs to be compensated for. Dispersion can be handled in various ways, one of which being an electronic dispersion compensator (EDC). Because EDCs can be easily integrated in the receiver with minimum additional cost, they are becoming the prime tool for dispersion compensation. In this dissertation, a continuous-time 7-tap FIR equalizer tailored to dispersion compensation in multi-mode fiber links is presented. By using a novel active delay line, the ultra-compact

equalizer is very flexible, maintaining optimal performances and power scalability over a wide range of input data-rates. Particular care is taken to address critical issues of continuous-time realizations, such as noise, linearity and dynamic range.

Extensive experimental results, carried out on test chips realized in 28nm LP-CMOS technology, are presented. The equalizer demonstrates successful operation with variable data-rates ranging from 10Gb/s to 25Gb/s and power dissipation scalable from 55mW to 90mW. Compared to previously reported high-speed FIR equalizers, the proposed solution accepts the largest variation of the input data-rate with state-of-the-art power efficiency and core silicon area of only 0.085 mm^2, meeting the demand of emerging 400Gbps standards.

Chapter 1

Introduction

Total Internet traffic has experienced dramatic growth the past two decades. More than twenty years ago, in 1992, global Internet networks carried approximately 100 GB of traffic per day. Ten years later, in 2002, global Internet traffic amounted to 100 gigabytes per second (GB/s). In 2013, global Internet traffic reached 30TB/s and is expected to growth to 50TB/s in 2018 (Fig. 1.1) with a 21 percent compound annual growth rate (CAGR).

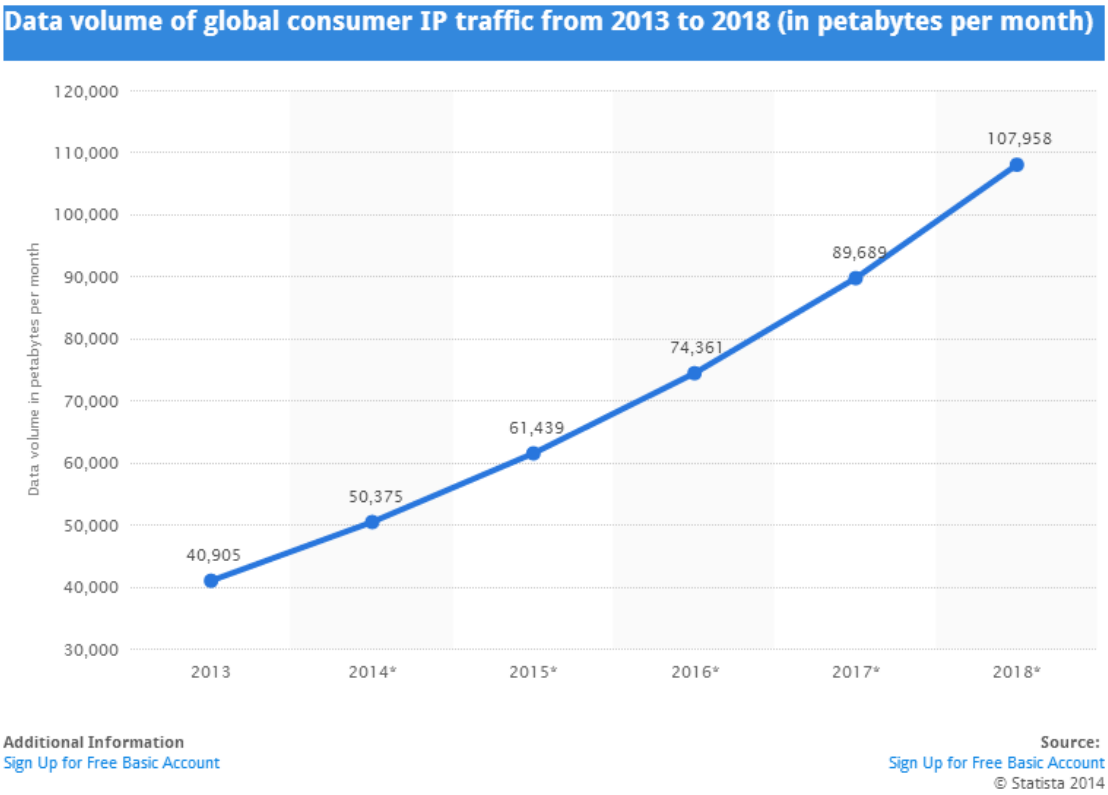


Figure 1.1: Global consumer IP traffic from 2013 to 2018 [1].

This growth is driven since the advent on the market of new mobile devices and applications. For example tablets are the fastest-growing device category with 29 percent CAGR over the forecast period, followed by machine-to-machine (M2M) connections with 26 percent CAGR. Device categories such as non-smartphones are actually going to start seeing a decline over the forecast period, increasingly being replaced by smartphones, which will more than double at 18 percent CAGR over the forecast period. Connected TVs, which includes flat-panel TVs, set-top boxes, digital media adapters, Blu-ray disc players, and gaming consoles will double to 2.6 billion by 2018. In addition to new devices, bandwidth-hungry applications will lead to a strong increase in IP traffic. For example (Fig. 1.2), all forms of IP video, which includes Internet video, IP VoD, video files exchanged through file sharing, video-streamed gaming, and videoconferencing, will continue to be in the range of 80 to 90 percent of total IP traffic with 21% CAGR. Globally, IP video traffic will account for 79 percent of traffic by 2018[2].

In this scenario it is important to recognize that most of the Internet traffic is originated, passes or terminates in Data Centers. Data center traffic (Fig. 1.3) will continue to dominate Internet traffic for the foreseeable future and by 2017 will triple to reach 7.7 zettabytes (10^{21}) per year with a 25 percent CAGR. This impressive growth, associated with data-intensive applications that are hosted in the data center servers (e.g. cloud computing applications, search engines, etc.) requires high interaction between the servers. This rises significant challenges to the networking of the data centers demanding more dense and efficient interconnections with high bandwidth and reduced latency.

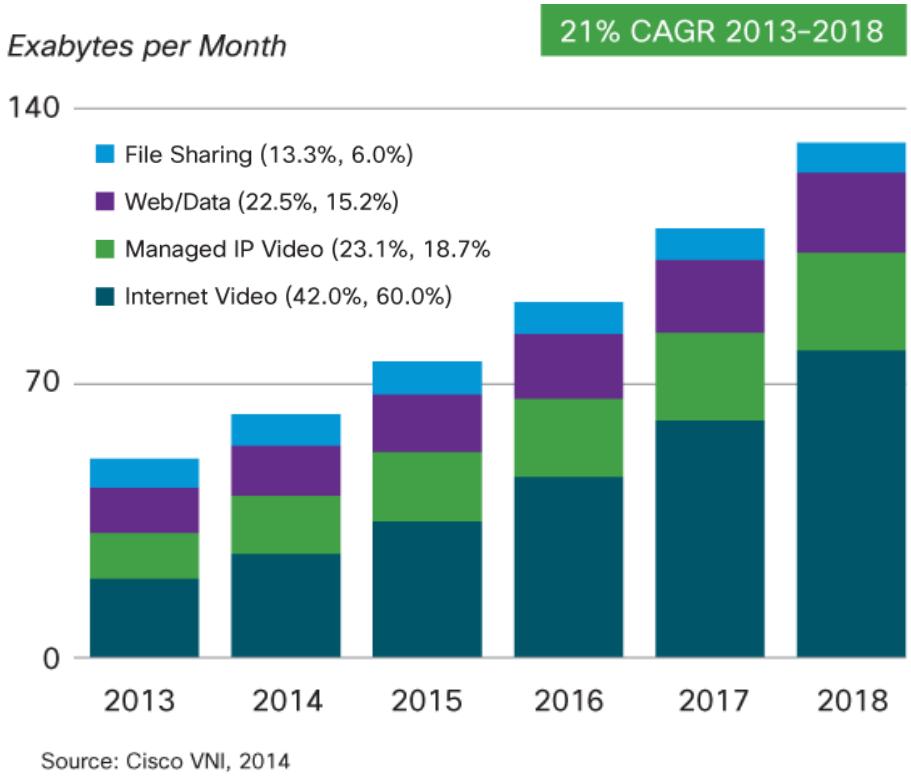


Figure 1.2: Global consumer IP traffic distribution.

Figure 1.3: Global Data center IP traffic.

1.1 Data Centers

Data centers are buildings of million Sq.Ft. (Fig1.4) based on thousands of high performance servers interconnected with high performance switches (Fig. 1.5). Applications that are hosted in the servers (e.g. cloud computing, search engines, etc.) are data-intensive and require high interaction between different servers [3]. The throughput and latency in future data center networks must be improved significantly to sustain the increased network traffic, but at the same time the power consumption inside the racks must remain almost constant due to thermal constraints [4].

Figure 1.4: Microsoft Data Center in Dublin.

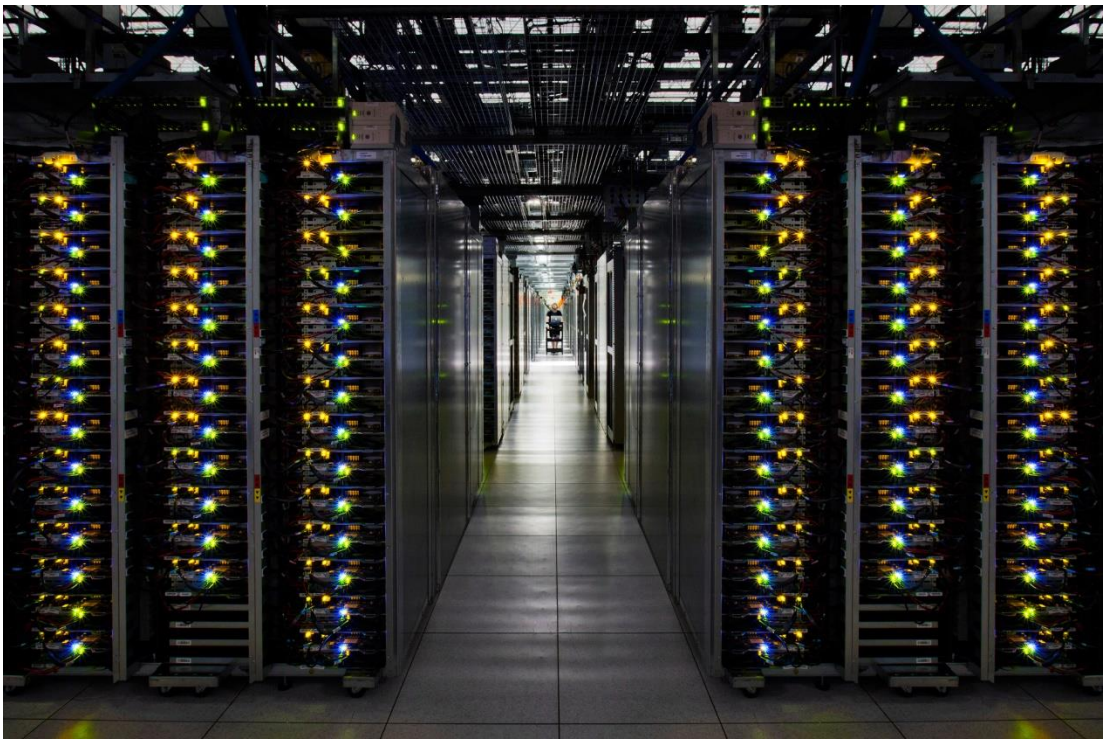


Figure 1.5: Inside Data Center.

Furthermore, as more and more processing cores are integrated into a single chip, the communication requirements between racks will keep increasing significantly [5]. Table I shows the projections for performance, bandwidth and power consumption for future high performance systems [6]. Note that while the peak performance will continue to increase rapidly, the budget for the total allowable power consumption that can be afforded by the data center is increasing in a much slower rate (2x every 4 years) due to thermal dissipation issues.

One of the most challenging issues in the design and deployment of a data center is therefore the power consumption. Greenpeace's Make IT Green report [7], estimates that the global demand for electricity from data centers was around 330 billion kWh in 2007 and a 3x increase is expected by 2020. The servers in the data centers

consume around 40% of the total IT power, storage up to 37% and the network devices consume around 23% of the total [8].

Year	Peak performance [PF]	Bandwidth requirements [PB/s]	Power consumption bound [MW]
2012	10	1	5
2016	100	20	10
2020	1000	400	20

Table I: Performance, BW. requirements and Power consumption for future systems

To keep steady the temperature of the building site, additional power is required to supply the HVAC equipment (Heating-Ventilation and Air-Conditioning). In this scenario, improving the energy efficiency of the network devices has a significant impact on the overall power consumption.

To follow the bandwidth requirements while keeping sustainable the development of future data centers, energy efficiency of links have to be reduced from 25mW/Gb/s to almost 1mW/Gb/s by 2020. This requirement opens one of the most challenging low-medium-term goals of new century IT engineers.

1.2 Fiber optic interconnections

Figure 1.6 shows the high level block diagram of a typical data center. As mentioned, the data center consists of multiple racks hosting the servers connected through an interconnection network.

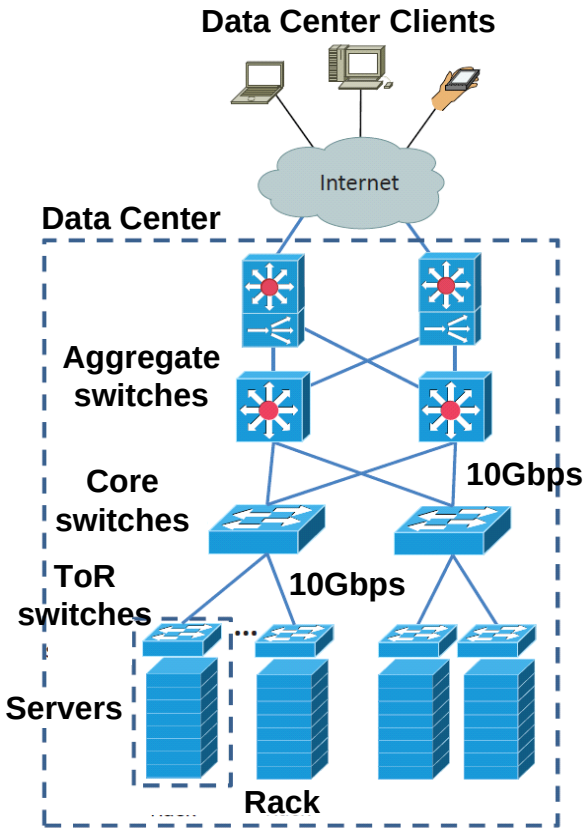


Figure 1.6: Architecture of current data center network.

When a request is issued by a user, then a packet is forwarded through the Internet to the front end of the data center. In the front end, the content switches and the load balance devices are used to route the request to the appropriate server. A request may require the communication of this server with many other servers. At present, the servers are connected through a Top-of-the-Rack Switch (ToR) using 1 Gb/s links.

These ToR switches are further inter-connected through *aggregate* switches using 10 Gb/s links in a tree topology. Currently, the optical technology is utilized in data centers only for point-to-point links based on low cost multimode fibers (MMF) for short-reach communication. These MMF links are used for the connections of the switches using fiber-based Small Form-factor Pluggable transceivers (SFP for 1 Gb/s and SFP+ for 10 Gb/s) displacing the copper-based cables [9]. In the near future higher bandwidth transceivers are going to be adopted for 40Gb/s and 100Gb/s Ethernet. As the traffic requirements in data centers are increasing to Tb/s, all-optical interconnects could provide a viable solution to these systems that will meet the high traffic requirements while decreasing significantly the power consumption [10],[11],[12]. Figure 1.7 shows the bandwidth requirements for next generation data center interconnections. Electrical medium, today preferred in very-short reach links, will be soon replaced by optical media.

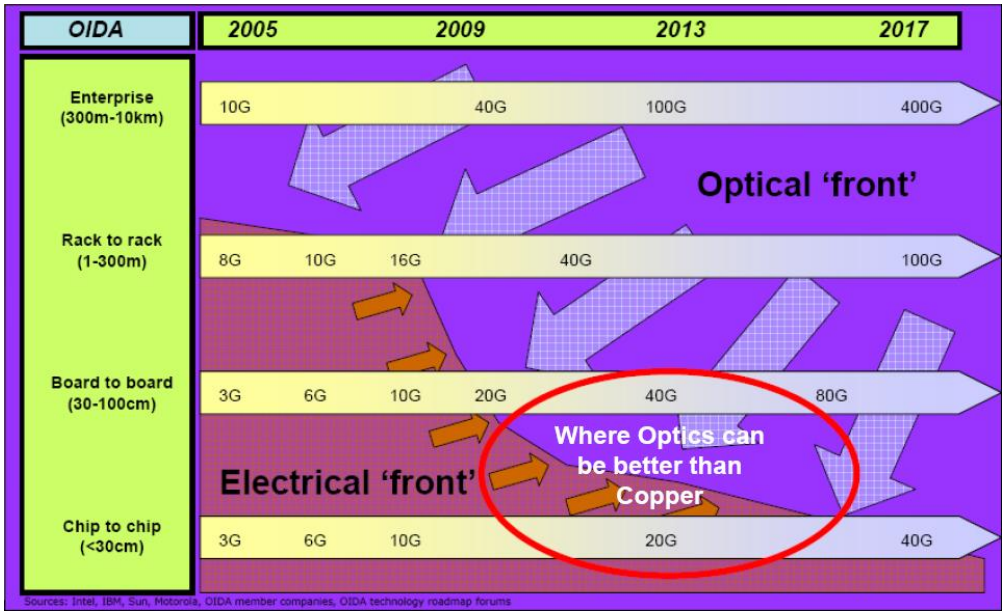


Figure 1.7: Optical Fiber Roadmap in Data Center.

1.2.1 Multi-Mode Fibers

Optical fibers can be categorized as single mode fiber (SMF) or multimode fiber (MMF) based upon the light propagation mechanism through the fiber. In single-mode fiber all the light propagates along the same path. This is accomplished by reducing the diameter of the core to such a degree that all the light is constrained to follow the same path (the core diameter is approximately 9um). In multimode fiber the core diameter is much larger (approximately 50um) resulting in multiple propagation modes, or paths, that the light can follow, as shown in Figure 1.8. This results in an unwanted phenomena called modal dispersion. Modal dispersion leads to optical energy spreading over several symbol times and severe ISI limiting maximum communication distance and data-rate.

Because of the large core and also the possibility of large numerical aperture (range of angles over which the system can accept or emit light), multi-mode fiber has higher "light-gathering" capacity than single-mode fiber. In practical terms, the larger core size simplifies connections and also allows the use of lower-cost optical sources such as light-emitting diodes (LEDs) and vertical-cavity surface-emitting lasers (VCSELs) which operate at the 850 nm and 1300 nm wavelength (single-mode fibers used in telecommunications operate at 1310 or 1550 nm and require more expensive laser sources).

Multi-mode fibers are classified according to the ISO 11801 standard — OM1, OM2, OM3 and OM4 — which is based on the modal bandwidth of the fiber. The modal bandwidth is determined from the optical output power frequency spectrum.

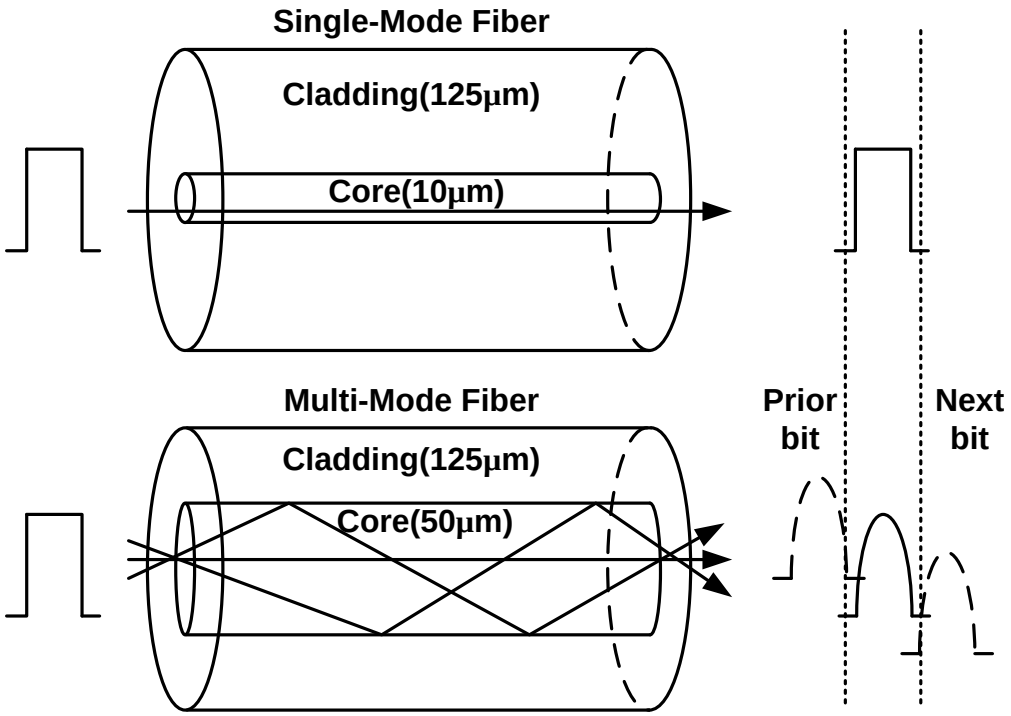


Figure 1.8: Single-mode and Multi-mode Fiber propagation.

The frequency at which the amplitude drops three decibels (dB) relative to the zero frequency component of the fiber is defined as the −3 dB bandwidth (or modal bandwidth).

OM4 fiber is the next generation 50-micron laser-optimized multimode fiber with extended bandwidth. It is designed to enhance the system cost benefits enabled by 850 nm VCSELs for existing 1 and 10 Gb/s applications as well as future 40 and 100 Gb/s systems. Supporting Ethernet, Fibre Channel, and OIF applications, OM4 fiber allows extended reach upwards of 550 meters at 10 Gb/s for building backbones and medium length campus backbones. It is also well suited for shorter reach data center and high performance computing applications, where optical loss budgets are tight at 10 Gb/s and are expected to get even tighter when pushing speed at 40 Gb/s and 100 Gb/s.

IEEE continues to work on standards for next-generation speeds. The IEEE 802.3bm Task Force has defined a Physical Medium Dependent (PMD) solution involving already-proven parallel optics technology. These systems will transmit one 10Gb/s or 25Gb/s signal on each of 4 fibers to reach 40Gb/s and 100Gb/s, respectively. To address market demands for efficient support of the exponential bandwidth growth the IEEE 802.3 400G Ethernet Study Group, approved in March 2013, was formed to explore development of a 400Gb/s Ethernet standard .

1.2.2 Modal Dispersion

Multi-mode fibers are the preferred media in data center because of the less expensive equipment compared to single-mode fiber. However MMF suffer from modal dispersion, a mechanism whereby different components of a signal travel through the transmission medium at different speeds. This causes pulse spreading at the fiber output and substantial inter symbol interference (ISI) that limits drastically maximum data-rate or distance. As an example OM3 MMF supports 1Gb/s transmission up to 2km and only 100m at 10Gb/s. Analysis of ISI introduced by MMFs is a complex task because fibers have nondeterministic dispersion characteristics. The set of modes dominating the transmission can vary depending on the particular fiber type used, the laser alignment (i.e. the precise launch method into the fiber), and even environmental factors such as vibration and temperature. Additionally, even fibers of the same type can have dramatically different dispersion profiles. In general it is therefore more instructive to analyze dispersive effects in MMF in terms of a population of fibers. An accurate analysis would then implies the use statistical

models. A simplified approach, more useful for circuits and systems design was proposed in the IEEE802.3aq standard. Called pre-cursor, post-cursor and symmetric stressors, the standard introduces the three pulses shown in Fig. 1.9 as representative for most of the multi-mode fiber pulse responses [13]. Although introduced for 10Gb/s speed on legacy fibers (OM1-2), it is reasonable to assume they could be valid to model also the dispersion of improved fibers when used at higher data rate [14],[15].

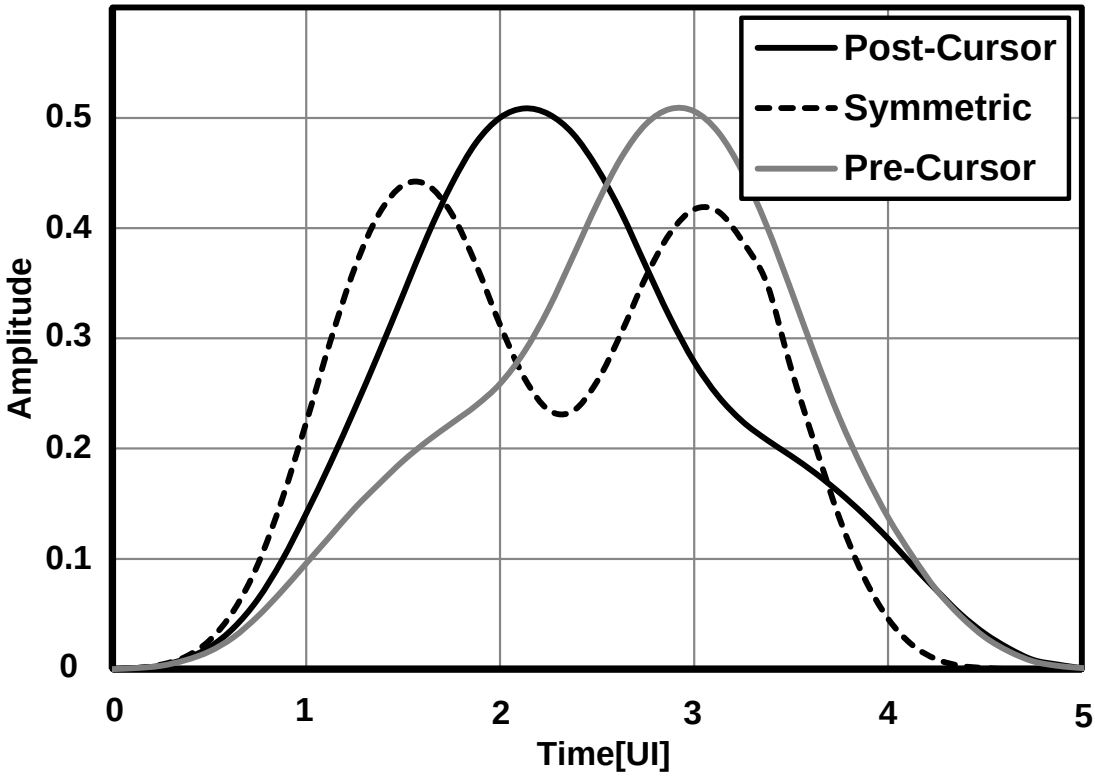


Fig. 1.9. IEEE802.3aq stressors representative of MMF channels.

Dispersion mitigation techniques are necessary to enable cost-effective support of high speed communication over MMF LANs and ignite the rapid and widespread

adoption of this networking technology. Transmitting at a lower data rate but employing multilevel modulation (to achieve the same effective data rate) or optical mode filtering techniques are expensive approaches to solve the problem. The technology showing the greatest potential to enable a cost-effective solution is electronic dispersion compensation (EDC) at the receiver.

Several EDC implementations , consisting of a linear FIR filter cascaded with a non-linear equalizer such as DFE, shown in Fig. 1.10, have been proposed at 10Gb/s to extend the communication distance from tens of meters up to 300m on legacy fibers, according to the 10GBASE-LRM standard. At this data-rate DSP-based EDCs are preferable [16-18] thanks to the high flexibility, robustness and ease of portability between different technology nodes. On the other hand, power dissipation for a digital architecture running at 25Gb/s would still be excessively high in current technology nodes, pushing the investigation of analog techniques for signal processing.

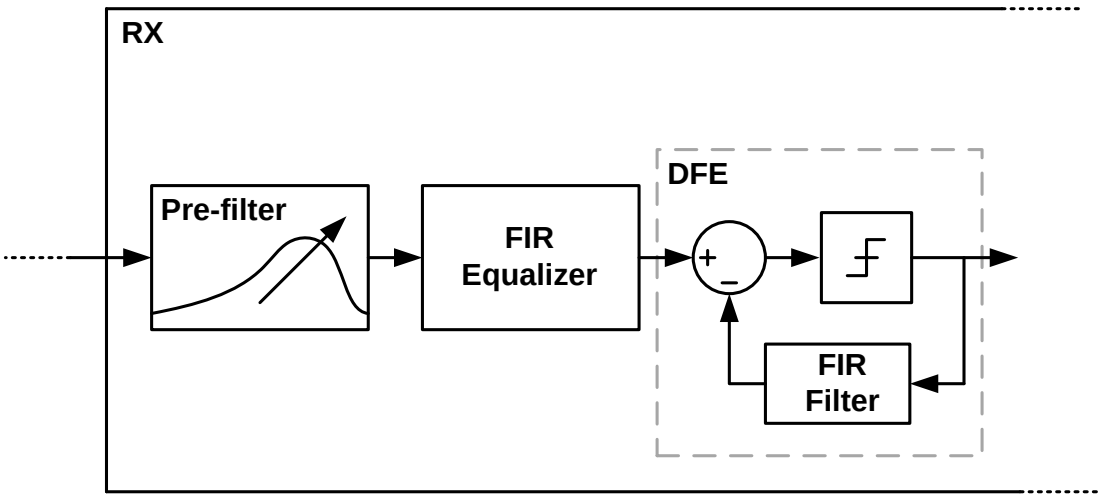


Fig. 1.10. Block diagram of EDC.

1.3 Purpose of this work and Thesis organization

This work will focus on the realization of a FIR equalizer for 25Gb/s EDCs. This is expected to be a key component for the deployment of next generation Ethernet standards supporting 400 Gb/s over optical fibers.

At this speed, an analog signal processing approach is commonly preferred to achieve better power efficiency. This is confirmed by several works, presented in the literature, addressing the design of analog integrated circuits for wireline communications at 25Gb/s or more. Many published backplane transceivers include high performance pre-emphasis analog filters and complex DFE equalizers that can be easily adapted for use in the EDC of Fig. 1.10 [19],[20]. On the other hand, design of the front-end FIR equalizer is much more challenging. This is a fundamental component for the EDC which has not been widely investigated so far. Both discrete- and continuous-time design approaches are possible. A discrete-time four-taps FIR equalizer has been recently proven to work up to 19Gb/s in 40-nm CMOS [21]. Analog delays are realized by sampling the input signal with multiple clock phases featuring 25% duty cycle. The main draw-back of this approach is the need for a co-design of the FIR equalizer with the clock recovery circuits. In addition, while a four-taps filter implementation fits well with popular wireline receivers working with a quarter-rate clock, increasing the number of taps, as required in MMF EDCs, sets undesirable constraints to the clock generation and distribution of the complete receiver. Continuous time CMOS analog FIR equalizers have been reported with good performances in terms of power dissipation. To meet the bandwidth requirements for data-rates in excess of 10Gb/s, passive or hybrid (i.e. passive and

active) delay lines have been exploited [22-26]. On the other hand integrated inductors featuring high-quality factor, used in delay lines, occupy large silicon area, making them impractical if high delay is required or if multiple parallel I/Os are stepped on the same chip to reach 400Gb/s. Furthermore, being the delay proportional to passive components value (capacitance and inductance), wide tuning range (fundamental to have compatibility with different communications standards and data-rates) needs a large change in component values, trading with quality factor, impedance magnitude and hence power dissipation. As a result, reported FIR equalizers beyond 10Gb/s have very limited or no delay variation and power scalability.

The dissertation describes the design and fabrication of a 10-25Gb/s 7-tap analog FIR equalizer for multimode-fiber EDCs. Through different architectural and circuit design techniques, many implementation challenges are overcome and a low-power high-performance equalizer is proposed. A delay line based on the cascade of all-pass CMOS filter sections is proposed. This solution allows high tuning range, thus accommodating a wide data-rate range with scalable power dissipation and very low area, key parameters for industrial applications. Realized in 28-nm LP CMOS technology, chip core silicon area is only 0.086 mm^2 and measurements prove successful equalization from 10Gb/s to 25Gb/s with power dissipation ranging from 55mW to 90mW. Compared with others 7-tap equalizers, this is the first FIR equalizer operating at 25Gb/s with a compact active delay line. Core area is ~10x smaller than state of the art. With these features, the equalizer accommodates the demand of variable transfer rates, back-compatibility, and energy efficiency

requirements of emerging 400Gb/s standards.

The thesis is organized as follow:

Chapter 2 provides an overview and comparison of different architectures and circuit techniques for equalizers for high speed random binary signals. Equalizers can be divided into linear and nonlinear. The differences, operation principles and performances are briefly discussed.

In Chapter 3 detailed MATLAB system level analysis is proposed to derive the FIR equalizer specifications (number of taps, delay, noise.). From this analysis, a 7-tap *3*/4-spaced filter is proposed as an optimal solution for 25Gb/s MMF-based equalization. The chapter ends with a discussion related to the challenges expected from circuit design.

Chapter 4 presents in detail the circuit topologies and design for each block of the FIR equalizer. The key component is the analog delay line. A new topology for the implementation of active all-pass filter sections are proposed allowing very low core area and high flexibility. In addition the design of a Trans-Impedance-Amplifier is proposed as a solution to add the signal currents provided by each tap of the filter with the high bandwidth requirement for 25Gb/s data rate.

The measurement results of the fabricated chip are presented in Chapter 5. First, small-signal AC measurements are performed to verify the operation of the building blocks. The equalization capability has been verified at different data rate (from 10 to 25Gb/s) by emulating a MMF channel. Furthermore the FIR is tested at 10Gb/s together with a serdes receiver provided by STMicroelectronics to implement a complete EDC.

Chapter 7 concludes the thesis with a summary of the FIR equalizer performances and comparison with state of the art.

The Appendix describes an additional activity carried out during the PhD activity. It is proposed the design of a Millimeter Wave VCO operating at 40GHz with 31.6% tuning range, low power consumption and a state-of-the art Phase Noise Figure of Merit. The large tuning range is achieved with a new circuit technique to implement a dual band resonator.

Chapter 2

Equalization Techniques for High Speed Links

In the previous chapter, dispersion introduced by MMF links have been introduced. In the frequency domain, the channel exhibits a distorted transfer function which is responsible for ISI and eye closure on the received data. The purpose of the EDC is compensating the channel distortion in order to restore the signal integrity. The EDC combines different equalization techniques and architecture which are presented in this chapter.

In general, equalizers can be divided into linear and nonlinear types, discussed in Sections 2.1 and 2.2, respectively. The EDC must be very flexible and able to track the time-variant frequency response of the fiber. Adaptation algorithms are discussed in Section 2.3.

2.1 Linear Equalizers

Two types of linear equalizers are commonly used in multi-Gb/s applications: simple analog filters with a peaking response and FIR filters. Peaking equalizers have been extensively covered in the literature [27-30] and they have been utilized for many decades. The frequency response of these filters resembles a low pass filter with some peaking.

The amount of peaking, as well as its location in frequency can be adjusted in order to provide different transfer functions. This flexibility enables the equalizer to compensate the loss of different transmission channels.

The transfer function and a typical CMOS implementation of one such equalizer is shown in Fig. 2.1. The circuit is a differential amplifier degenerated by a parallel RC network. Here, the high frequency boost is achieved by reducing the gain of the amplifier at DC with the degeneration resistor. The gain roll-off at high frequency is due to the pole set by the load resistors and capacitors. The position in frequency of the peak gain can be tuned by changing the degeneration capacitor. Although the transfer function can be adjusted, the shape of the equalizer transfer function is unchanged. This lack of flexibility severely limits the use of these very simple equalizers for optical channels.

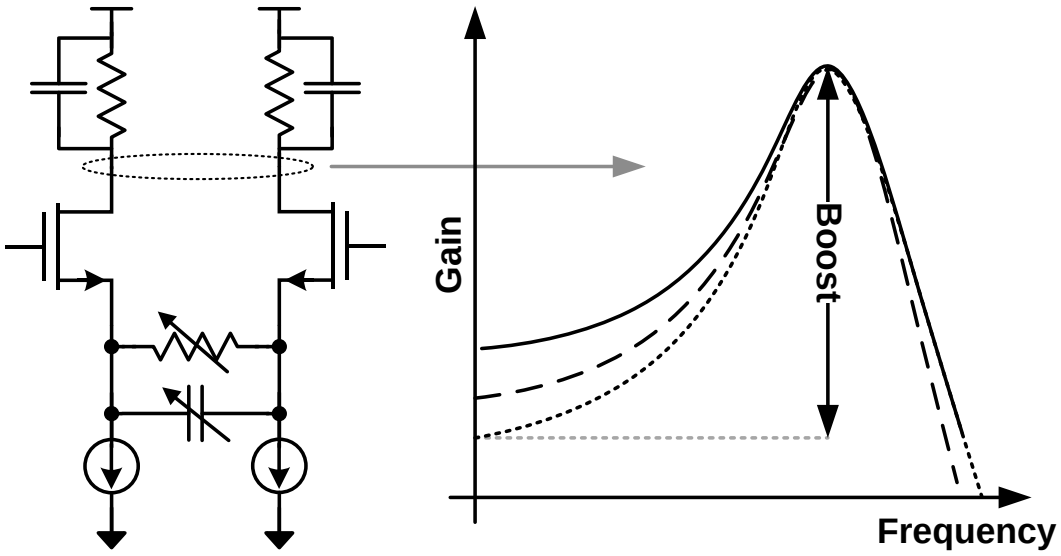


Figure 2.1: Typical CMOS implementation and transfer function of a Peaking Filter.

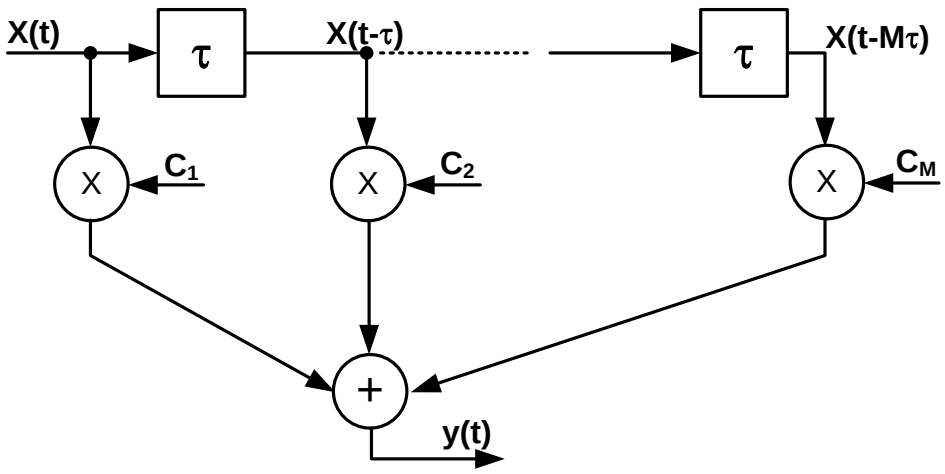


Figure 2.2: *M*-tap FIR block diagram.

A finite impulse response (FIR) filter, often called Feed-Forward Equalizer (FFE), is the most practical architecture for channels with a highly distorted transfer function because it is highly flexible and can generate complex transfer functions [31-34]. The block diagram of a FFE is shown in Fig. 2.2. The input signal, $x(t)$, propagates along a delay line composed of M elements each one introducing a delay of τ. The delayed signals are then multiplied by adjustable coefficients and finally summed together. A tap in the middle is commonly referred to as the main tap. The taps that follow the main tap are called post-cursor taps while the taps before the main tap are called pre-cursor taps The output signal, *y(n)* is given by:

$$y(t) = \sum_{i=0}^{M} (C_i \cdot x(t - i\tau)) \tag{2.1}$$

where C_i is the coefficient value which multiplies the signal at the i^{th} tap of the delay line.

The input-output relationship shows that the equalizer performances depend from the coefficients value but also from the delay between consecutive taps, τ.

The delay value can be equal or less than the bit-period. In the first case the FFE is called Symbol Spaced Equalizer (SSE) while with lower delay we talk about Fractionally Spaced Equalizer (FSE). In the frequency domain, given the tap-to-tap delay different filter transfer functions can be achieved selecting different tap values. On the other hand, to gain insight into the operation of the FFE it is more intuitive to look at the waveforms in the time domain. Figure 2.3 shows a 4-tap equalizer and the waveforms at the output of each tap.

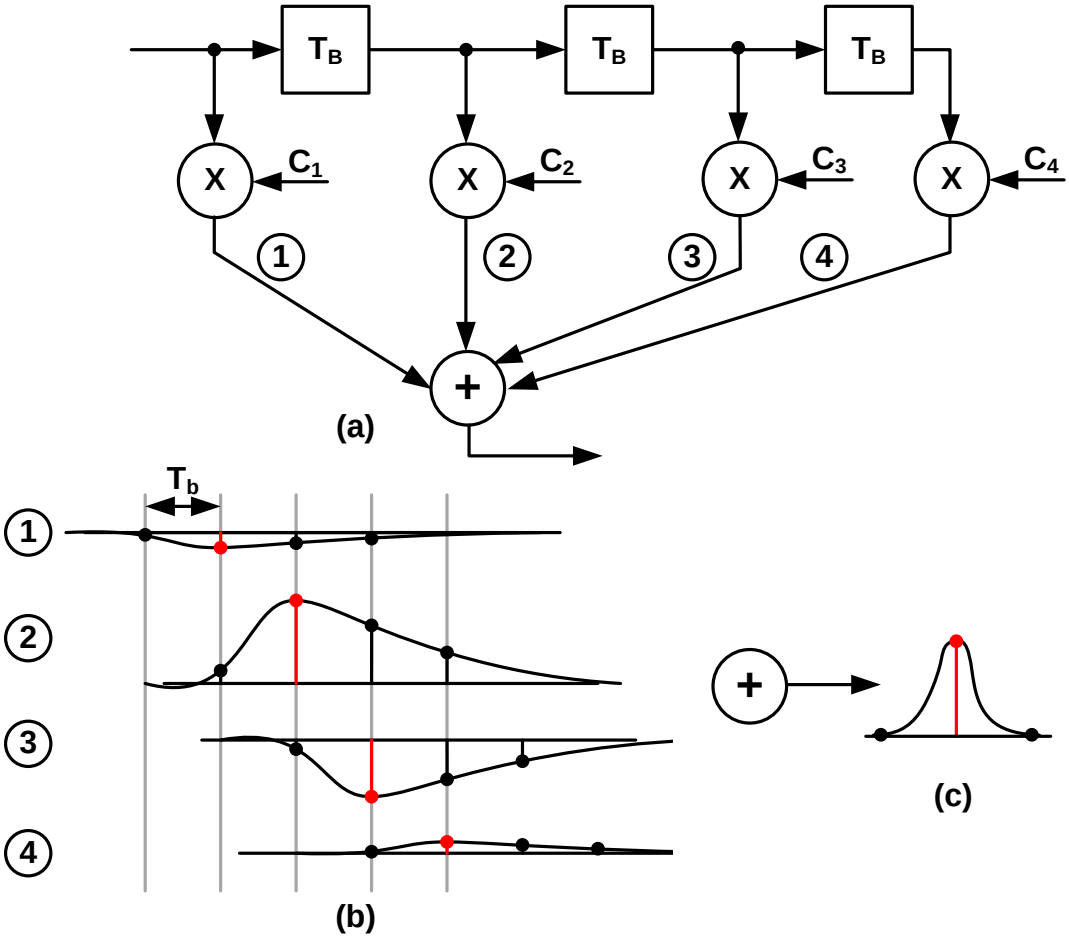


Figure 2.3: Time-domain operation of a 4-tap FFE; (a) block diagram, (b) signals at each taps output, (c) Equalized signal by subtracting the post/pre cursor from the present symbol.

Let's suppose the input, x(t), is the channel pulse response, corresponding to the response when an isolated bit is transmitted. The second tap is the main tap and, as a reference, let's assume C_2=1. The output at node (2) is therefore the channel pulse response delayed by T_B. The energy located over adjacent time slots is responsible for inter symbol interference and have to be removed by the equalizer. As shown in the picture, this can be done by adding delayed and versions of the input, available at nodes (1), (3) and (4), appropriately scaled by selecting the pre- and post-cursor tap gains, C_1, C_3 and C_4.

2. 2 Nonlinear Equalizers

The most popular architecture to implement a non-linear equalizer is the Decision Feedback Equalizer (DFE) [35]. The principle of operation is based on the fact that if we know the channel pulse response, we can cancel the ISI by looking at the received bit and subtracting its interference to the following bits. The DFE structure, shown in Fig. 2.4. is composed of an *N*-tap filter closing the feedback around the slicer.

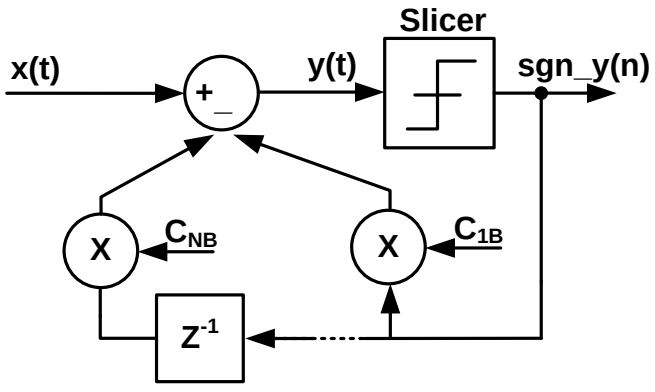


Figure 2.4: N-tap DFE block diagram.

After the slicer, the signal may have only two logic levels: +/-1. The signal at the slicer input y(t) is given by :

$$y(t) = x(t) - \sum_{i=1}^{N} (C_{iB} \cdot \text{sgn\_}\, y(n-i)) \tag{2.2}$$

where C_{iB} is the coefficient value which multiplies the signal at the i^{th} tap of the feedback delay line. Having a digital signal after the slicer, the delay line can be easily implemented by cascading flip-flops. In addition, compared to linear equalizers, the DFE does not introduce noise amplification because after the hard decision performed by the slicer, the signal propagating through the delay line is noiseless [36-37]. Despite these advantages, DFE alone is never used. A linear equalizer such as the FIR is always required, in front of the DFE, because the latter can correct only post-cursors ISI. In addition, DFEs can also suffer from error propagation in their feedback loop.

Another example of nonlinear equalizer is the Maximum Likelihood Sequence Equalizer (MLSE). In this type of equalizer ISI is removed from the received data by looking on a sequence of bits as opposed to a single bit [38-39]. MLSE does not suffer from error propagation and provides the best performance among topologies discussed here. However, this kind of equalizer is rarely used in high speed communications because of the high complexity leading to high power consumption and die area.

2.3 Equalizers Adaptation

Multi-Mode fiber channels exhibit different and time-varying responses requiring the use of adaptive equalizers. To this end, many adaptation algorithms have been proposed over the last few decades [40]. The Least Mean Square (LMS) algorithm is the most commonly used. This algorithm is based on minimizing the Mean Square Error (MSE) between the received and ideal data sequence. The block diagram of the adaptation algorithm applied to a FIR filter is shown in fig. 2.5. The error signal, $e(n)$, is first estimated by subtracting the equalizer output, $y(n)$, from the target signal, $d(n)$:

$$e(n) = y(n) - d(n) \tag{2.3}$$

Then the MSE value can be written:

$$MSE = E[e^2(n)] \tag{2.4}$$

where $E[\ ]$ denotes the expectation operation. To find the optimum value of the FFE coefficient C_i, the partial derivative of the MSE with respect to C_i needs to be driven to zero.

$$\frac{\partial MSE}{\partial C_i} = \frac{\partial (E[e^2(n)])}{\partial C_i} = 2 \cdot E[e(n) \cdot \frac{\partial e(n)}{\partial C_i}] \tag{2.5}$$

Since $d(n)$ is a binary signal with either +1 or -1 value, and it is independent of coefficient C_i, (2.7) can be simplified to:

$$\frac{\partial MSE}{\partial C_i} = 2 \cdot E[e(n) \cdot \frac{\partial y(n)}{\partial C_i}] \tag{2.6}$$

Finally, combining (2.1) and (2.6) leads to:

$$\frac{\partial MSE}{\partial C_i} = 2 \cdot E[e(n) \cdot x(n-i+1)] \tag{2.7}$$

Equation (2.7) indicates that in order to find the optimum value of C_i, the average value of $e(n) \cdot x(n-i+1)$ needs to be driven to zero. The following well-known iterative equation [41] performs this task:

$$C_i(n+1) = C_i(n) + \mu \cdot e(n) \cdot x(n-i+1) \tag{2.8}$$

where the step size μ determines the adaptation rate.

The blocks related to the adaptation loop in Fig. 2.5 are shaded. The use of multipliers would lead to a significant increase in power consumption. A less power-consuming approach is shown in Fig. 2.6 which is based on the sign-sign LMS algorithm [42] where the error, $e(n)$ and the data signals along the delay line are replaced with their signs. As shown in Fig. 2.6, high-speed multipliers can now be replaced with simple multiplexers that provide positive or negative value of $x(n\text{-}i+1)$ to the integrator based on the sign of the error signal.

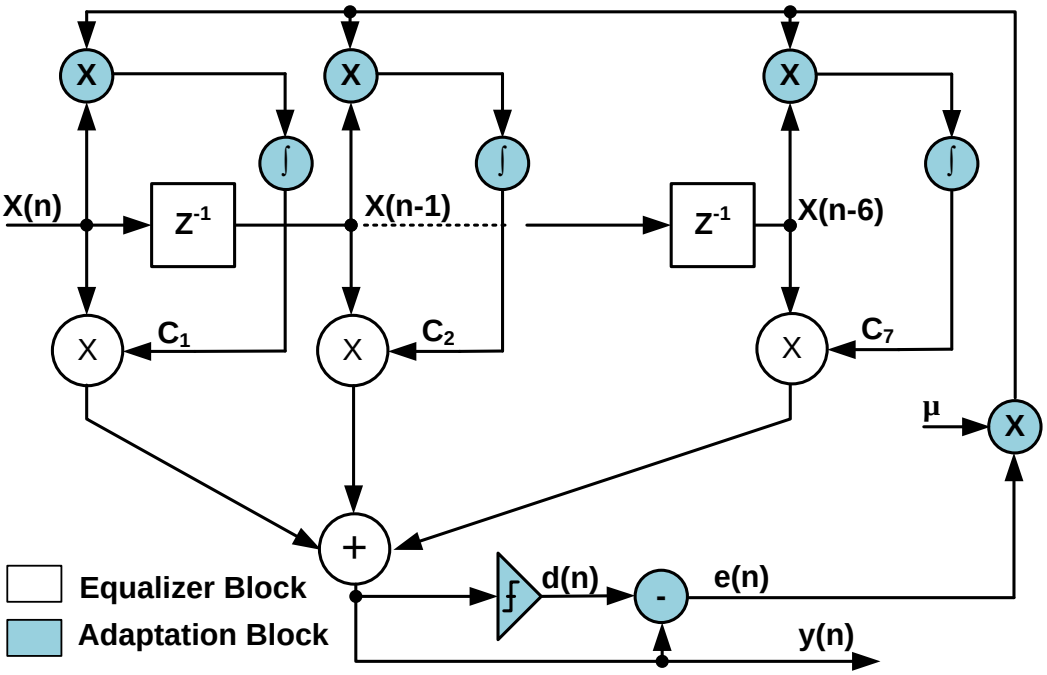


Figure 2.5: 7-tap FFE with LMS adaptation.

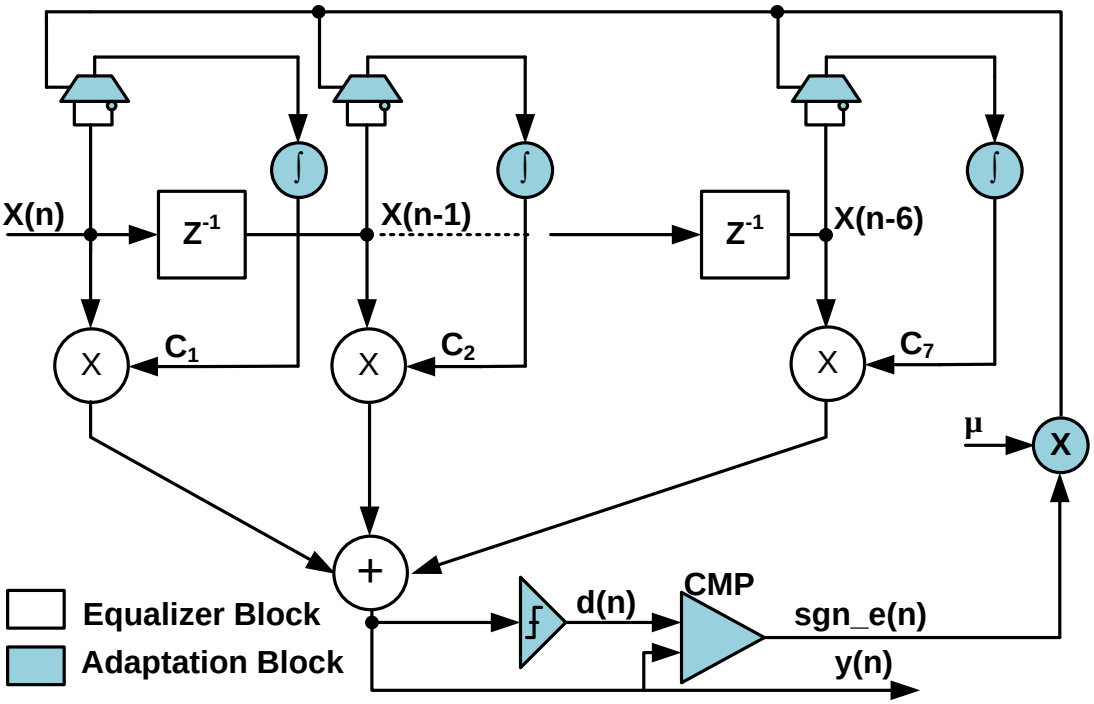


Figure 2.6: 7-tap FFE with sign-error LMS adaptation.

Chapter 3

System Level Simulations

In this chapter a detailed system level analysis of the MMF EDC is proposed to derive FIR filter specifications. A behavioral model of the EDC is implemented and simulated with MATLAB. Section 3.1 introduces the block diagram of the analog FIR equalizer and the key design parameters. Section 3.2 describes the system level simulation results for the complete EDC. Once the FIR equalizer specification are derived, circuit implementation challenges are briefly discussed in Section 3.3.

3.1 Analog FIR Filter and Design Parameters

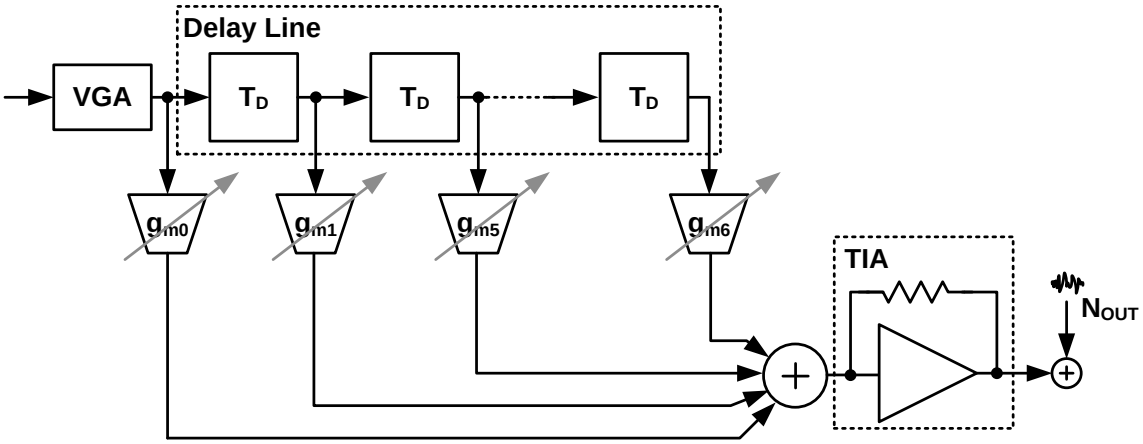


Figure 3.1: FFE block diagram.

The block diagram of the FIR filter developed in this work is shown in Fig. 3.1. The active delay line is realized with cascaded elements providing a tap-to-tap time delay T_d, while the tap amplifiers are trans-conductors with digitally programmable gain g_m.

A trans-impedance amplifier (TIA) with gain R_T is used to sum the output currents and a variable gain amplifier (VGA) at the input of the filter is employed to have a precise control on the input voltage swing.

When considering fully digital implementations, it is well known that fractionally spaced FIR equalizers (having a tap-to-tap delay which is a fraction of the bit duration) offer several advantages over symbol spaced equalizers. Thanks to the higher sampling rate, they do not suffer from aliasing, may provide boost well beyond Nyquist frequency ($f_N=1/2T_S$), are less sensitive to the clock sampling phase and allow simultaneous equalization and matched filtering [43],[44]. On the other hand, the shorter is the tap-to-tap delay, the larger is the number of taps to cover the same time window.

When targeting an analog continuous-time realization, minimizing the number of taps is highly desirable to limit power dissipation. Moreover, differently from digital implementations, a primary issue that must be carefully considered is the impact of the equalizer noise to the output signal SNR. In fact, an analog FFE impairs the SNR not only because of the enhancement of the high frequency noise superimposed to the input signal, but also and most importantly because of the noise introduced by the equalizer building blocks themselves, represented in Fig.3.1 by the noise N_{out} added to the output signal.

To simplify the analysis let's assume a negligible noise contributed by the delay line. If N_{out} is due only to the noise introduced by the tap amplifiers and TIA, it is independent from the specific set of filter coefficients i.e. the equalizer transfer function. Given the input signal swing, the amplitude and SNR of the output signal

are set by the DC gain of the FIR equalizer which is determined, according to Eq. 2.1, by the sum of the filter coefficients. Maximum amplitude and SNR are then achieved with all the coefficients having the same sign. However, to provide boost at high frequency, the filter needs alternating positive and negative values. Being the coefficients bounded by the maximum gain of the tap trans-conductors and TIA of Fig.3.1, the DC gain and output signal SNR are penalized when the filter is configured to equalize channels introducing high frequency attenuation. In conclusion, with a fixed number of taps and for a given channel loss, the lower is the tap-to-tap delay, the higher is the penalty. To gain insight, Fig. 3.2 shows the transfer functions of two-tap FIR equalizers with different T_d providing 15dB boost at Nyquist Frequency. The coefficients are bounded within ±1, reasonable value consider a 25Gb/s operating circuit.

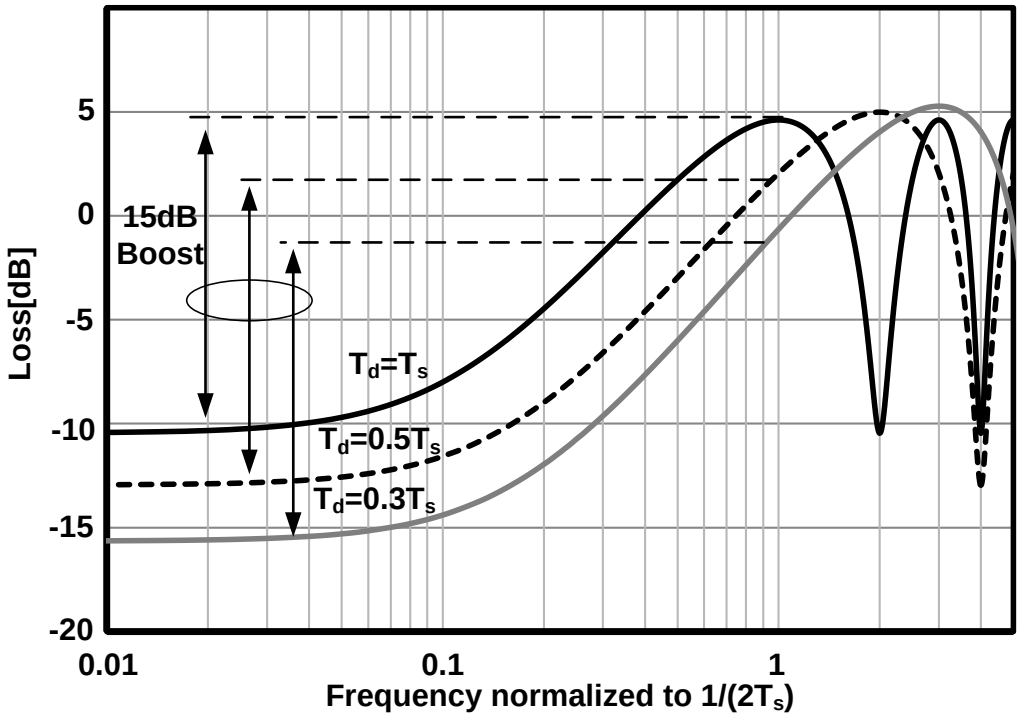


Fig. 3.2. Transfer functions of two-tap FIR equalizers providing 15dB boost at Nyquist frequency with coefficients bounded within ±1 and different *Td*.

The DC gain loss with $T_d=T_S$ is 10dB. $T_d=T_S/2$ and $T_d=T_S/3$ yield respectively 3dB and 6dB more DC loss leading to the same SNR penalty when considering the filter noise. Increasing the number of taps when reducing T_d may restore the DC loss but needs more power dissipation and leads also to an increase of N_{out}. Therefore, best SNR is achieved by selecting T_d equal to T_S. Calibrations of the delay line have not been implemented because the impact of limited T_d drifts on the equalizer transfer function is counteracted by the adaptation algorithms used to set optimal filter coefficient values.

System level simulations of the complete EDC have been performed with MATLAB to determine the optimal number of taps of the FFE, the delay of each tap, the quantization levels for the filter coefficients and the maximum tolerated output noise.

3.2 EDC System Level Simulations

A model of a complete EDC, shown in block diagram of Fig. 3.3 has been implemented in MATLAB to perform system level simulations and derive the FIR filter specifications listed above.

The EDC comprises a pre-filter, the FIR filter and DFE. The pre-filter is a programmable peaking filter used to recover high frequency loss of the channel in a coarse way. FIR and DFE perform fine equalization of the signal after the peaking filter to minimize ISI and recover correctly the transmitted sequence.

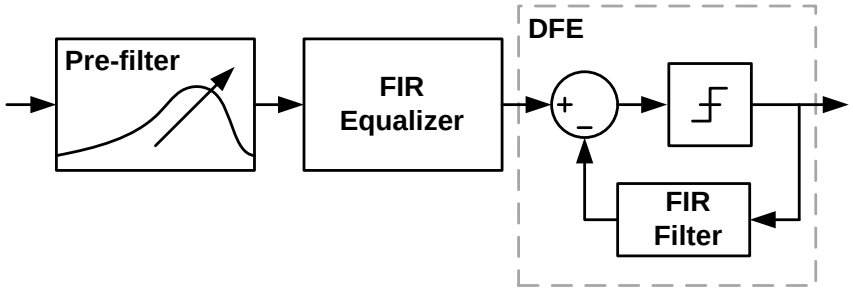


Fig. 3.3. Block diagram of EDC

Channels featuring the pulse responses shown in Fig. 1.6 have been considered. The magnitudes of the frequency response for the three channels are shown in Fig. 3.4. The pre-cursor and post-cursor channels exhibit a low-pass transfer function while the channel with the symmetric pulse response features a deep in-band notch.

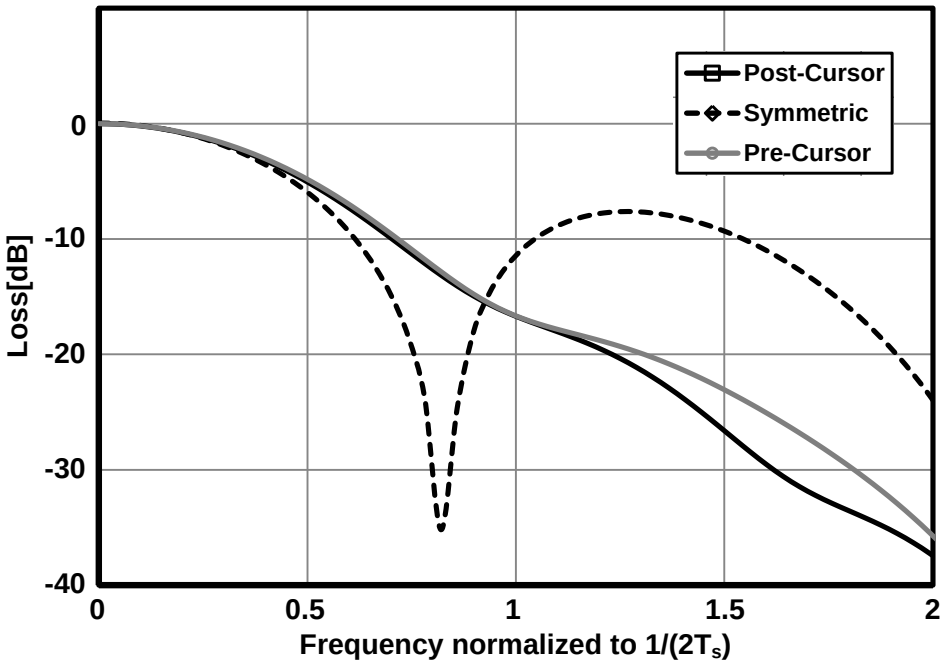


Fig. 3.4. IEEE802.3aq stressors magnitude of transfer functions.

In the three cases, attenuation at Nyquist ranges from a minimum of 7dB for the symmetric pulse to more than 15dB for the pre-cursor and post-cursor pulses. To limit

the high frequency boost required to the FIR equalizer and hence the SNR penalty, a fixed emphasis of 10dB is assumed to be introduced by the pre-filter shown in Fig. 3.3. Five symbol-spaced taps are considered for the DFE, as proposed in [45].

The first evaluated parameter of the FIR is the tap-to-tap delay, Td. As previously discussed, a delay near T_S is preferable to avoid SNR degradation with a limited number of taps. On the other hand, it is important to have T_d not beyond T_S otherwise the equalization performance degrades quickly. To satisfy this condition within PVT variations we selected a nominal T_d of $3/4T_S$.

Figure 3.5 shows the simulated Vertical Aperture of the eye at the input of the slicer in Fig. 3.3 for the three channels with increasing number of taps of the FFE. The vertical aperture, used as figure of merit, is defined as the ratio between minim signal level due to residual ISI and mean signal level.

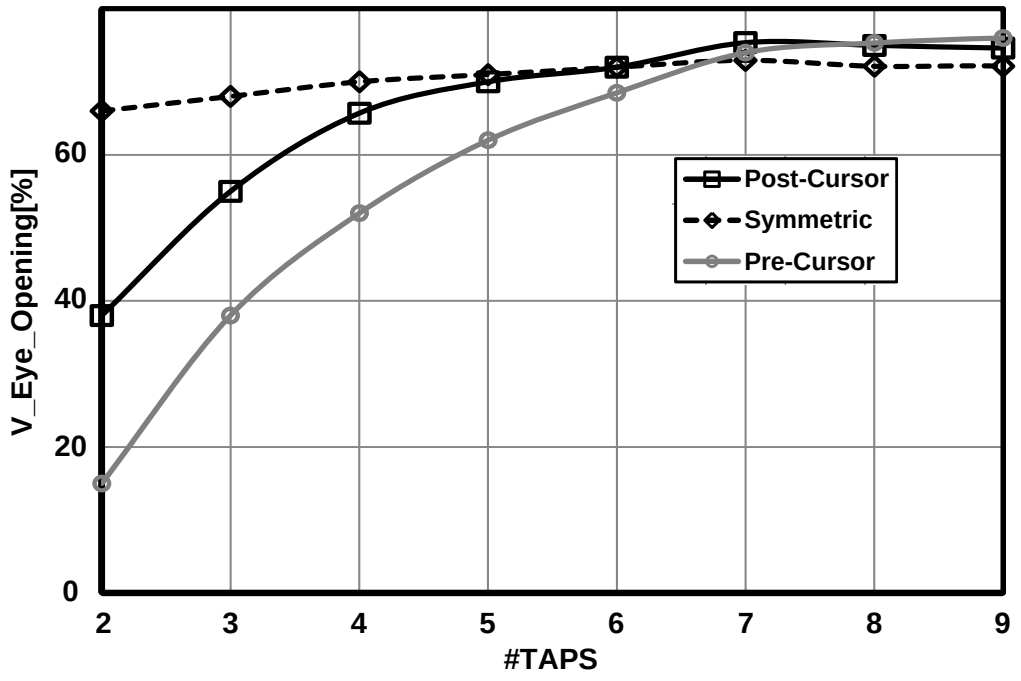


Fig. 3.5. Eye Vertical Aperture at the output of the EDC with increasing number of taps of the FFE. Five taps DFE is considered.

Eye opening saturates to ~72% and there is almost no advantage from using a filter with more than seven taps. It is interesting to note that the equalization performance is more sensitive to the number of taps when the channel suffers from an increasing amount of pre-cursor ISI. In fact, while the channel modeled by the symmetric stressor is mostly equalized by the DFE alone (due to the high distortion introduced by notch, as shown in Fig. 3.4), the channel showing the pre-cursor pulse response needs seven taps to reach the optimal performance.

Simulations with quantized filter coefficients have been also performed suggesting 6-bits are sufficient to have negligible performance penalty (Fig. 3.6).

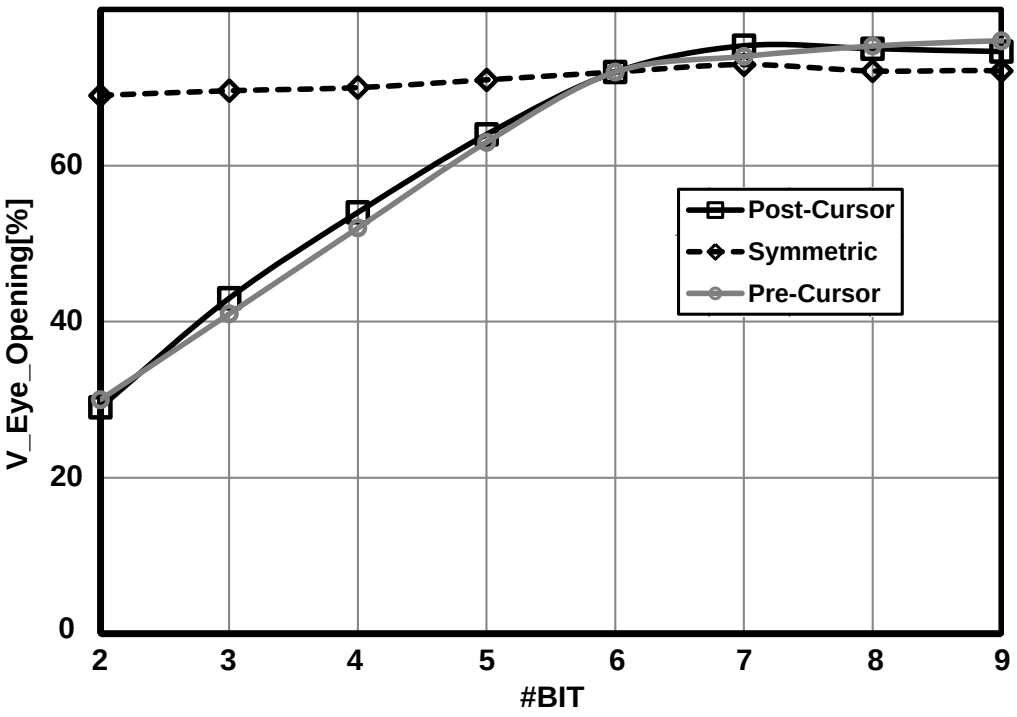
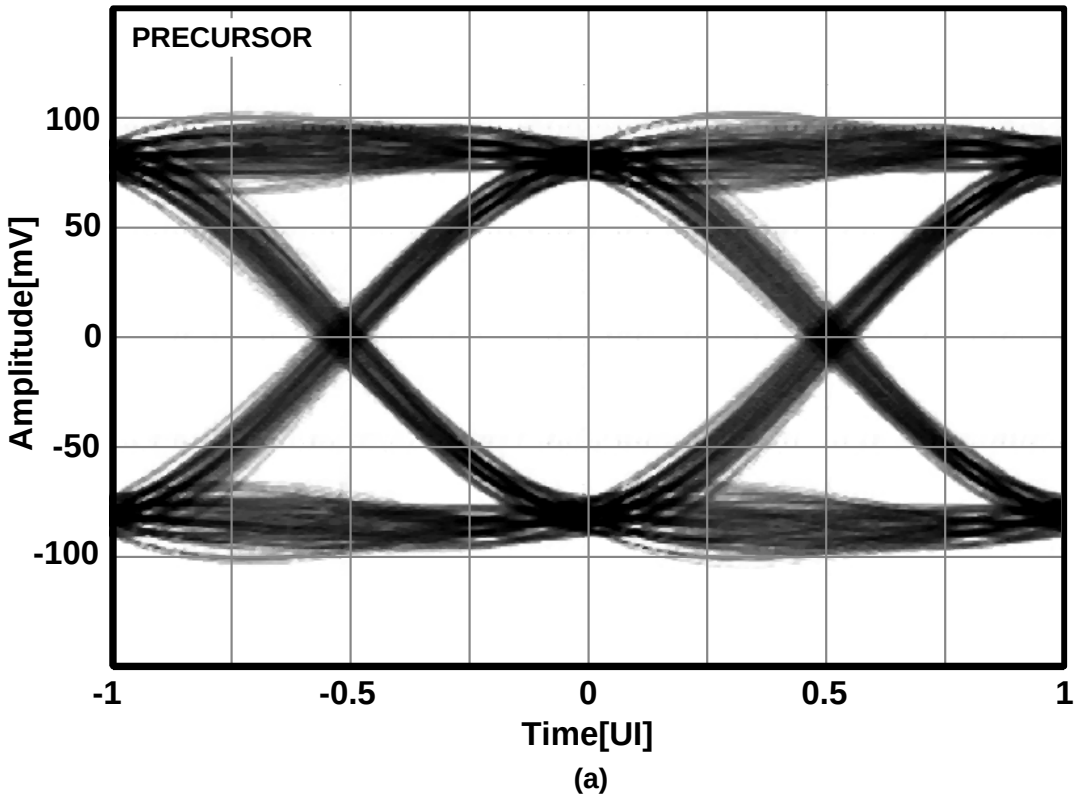


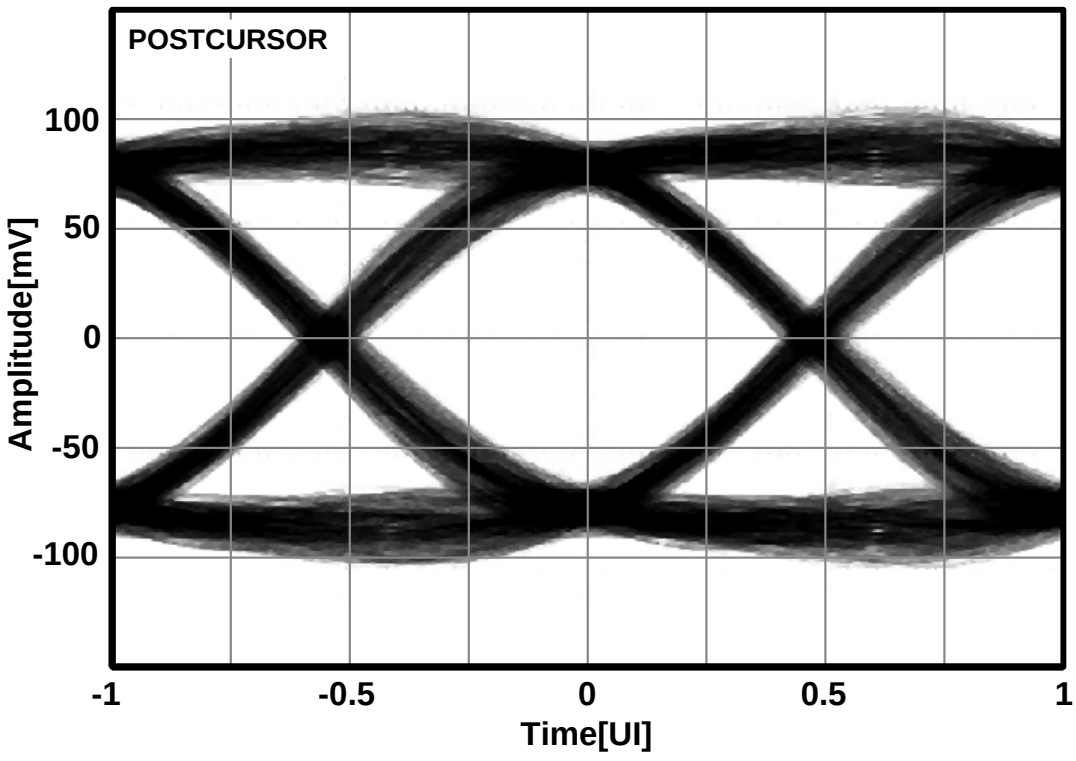
Fig. 3.6. Eye Vertical Aperture at the output of the EDC with increasing number of bits for the tap amplifiers.

Finally, to gain insight on the complete EDC performances, Fig. 3.7 shows the output eye diagrams for the three channels. Signal amplitude at the input of the FFE is

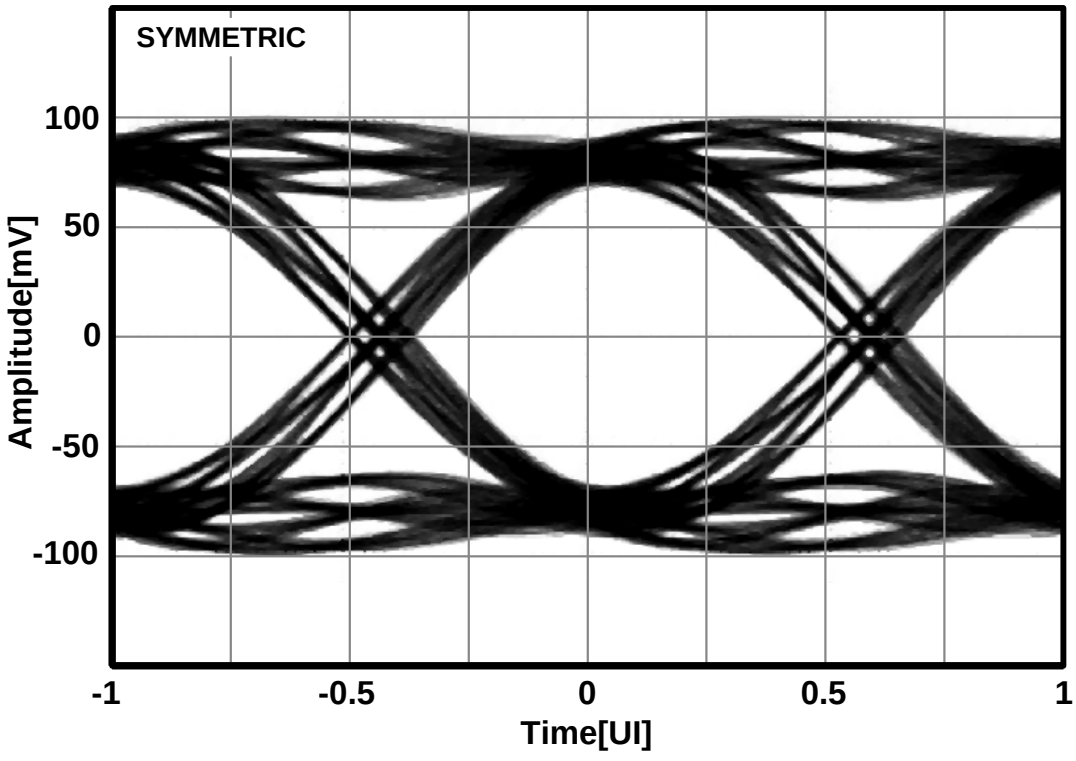
assumed constant at $200mV_{pk\text{-}to\text{-}pk}$ (a realistic value considering 1V supply) while the filter coefficients are bounded within ±1. The pk-to-pk vertical openings are 170mV, 145mV, 160mV and pk-to-pk horizontal openings are 0.65UI, 0.63UI, 0.64UI for the pre-cursor, post-cursor and symmetric stressors, respectively. To assess the impact of the noise introduced by the analog FFE, Fig. 3.7 shows also the bathtub plots calculated by convolving the simulated data-dependent jitter histograms, extracted from the eye diagrams, with the random jitter due to N_{out}. Targeting $6mV_{rms}$ maximum noise, the horizontal eye openings at 10^{-12} Bit-Error-Rate (BER) are 0.54UI, 0.44UI and 0.53UI for pre-cursor, post-cursor and symmetric stressors, respectively.



(a)


POSTCURSOR
100
50
0
-50
-100
Amplitude[mV]
-1
-0.5
0
0.5
1
Time[UI]

(b)


SYMMETRIC
100
50
0
-50
-100
Amplitude[mV]
-1
-0.5
0
0.5
1
Time[UI]

(c)

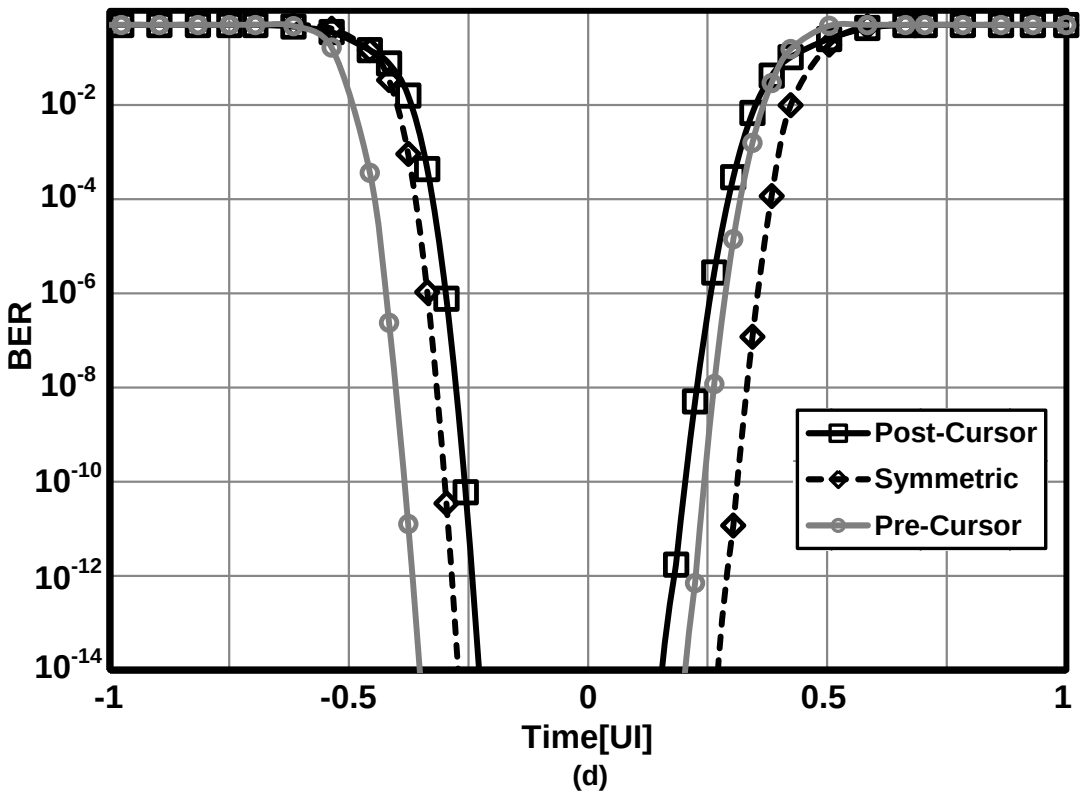


Fig. 3.7. Simulated eye diagrams and bathtubs at the output of the EDC for channels with pre-cursor, post-cursor and symmetric pulse response.

Table II summarizes the FFE requirements. For compatibility with legacy channel, the equalizer needs to accommodate a variable data rate ranging from 10 to 25Gb/s with a tap-to-tap delay set to $3/4T_s$. Seven taps with 6-bits quantized coefficients are necessary to successfully address all the three pulse responses typical of MMF channels. Assuming a signal level greater than $200\text{mV}_{\text{pk-pk}}$ and coefficients bounded within ±1, N_{out} of 6mV_{rms} can be tolerated, still leaving margin for other source of noise such as the input photodiode and interface electronics. In principle, increasing the input signal swing may improve the output SNR. On the other hand attention must be paid to avoid distortion introduced by the limited linear region of the filter building blocks which would significantly impair the equalization performances.

Data rate	10-25 Gb/s
Tap-to-tap delay T_d	$3/4T_s$
Number of taps	7
Coefficients range	±1
Coefficients	6 bits
Input signal	$> 200mV_{pk\text{-}to\text{-}pk}$
Output noise	$< 6mV_{rms}$

Table II. FFE specifications

3.3 Circuit implementation Challenges

Ultra-high speed optical transceivers design were commonly designed by using compound semiconductor technologies such as III-V SiGe. However, from a systems point of view, CMOS is the preferred the technology because of several advantages. First, the use of a standard CMOS process allows substantially lower power dissipation due to low supply voltage (1V for 28nm technology) and negligible static power dissipation in circuits implemented by digital logic. Second, CMOS design enables a very high level of integration, which eliminates the often power-hungry and error-prone chip-to-chip interfaces, thereby increasing the port density. Lastly, the enormous investment from industry and academia in fabrication, modeling, and design automation makes CMOS technology the most economical and reliable semiconductor process. The aggressive scaling of silicon technology also guarantees that that transistor speeds are improving faster than in other types of technologies. Thus, chip performance at high frequencies can be readily enhanced with each new generation of scaling. The utilization of CMOS technology thus results in significant space, power, and cost savings for the system.

Although the CMOS process speed is the major limitation for designing individual high speed blocks such as buffers, implementation of the 7-tap FFE with the architecture shown in fig. 3.1 faces additional challenges. First, since a cascade of multiple blocks is required, especially in the delay line, the bandwidth of each block to support 25Gb/s data rate needs to exceed 25GHz. Otherwise, the equalizer itself will generate excessive ISI, thus diminishing its capability to compensate for the link dispersion. To have back-compatibility with 10Gb/s standards the delay of the delay line needs to be changed by a factor 2.5 and power consumption needs to be scaled according with data rate to maintain the maximum power efficiency. The gain variation of the delay elements also needs to be controlled across the PVT range to avoid performance penalty. Finally, the large number of tap amplifiers and their relatively long interconnections result in high output parasitic capacitance at adder input introducing a severe gain-bandwidth trade-off that limits equalization performances.

In the next chapter, the design of a 7-tap 3/4T-spaced analog FFE is covered in detail. Various architectural and circuit design techniques are used to overcome the above challenges.

Chapter 4

FIR Equalizer Circuit Design

In the previous chapters, the general theory of feed-forward equalization and detailed analysis of multimode-fiber link receiver was discussed. The block diagram of the implemented FIR equalizer is shown in Fig 4.1. Specification of equalizer derived from system level simulations have been summarized in table II.

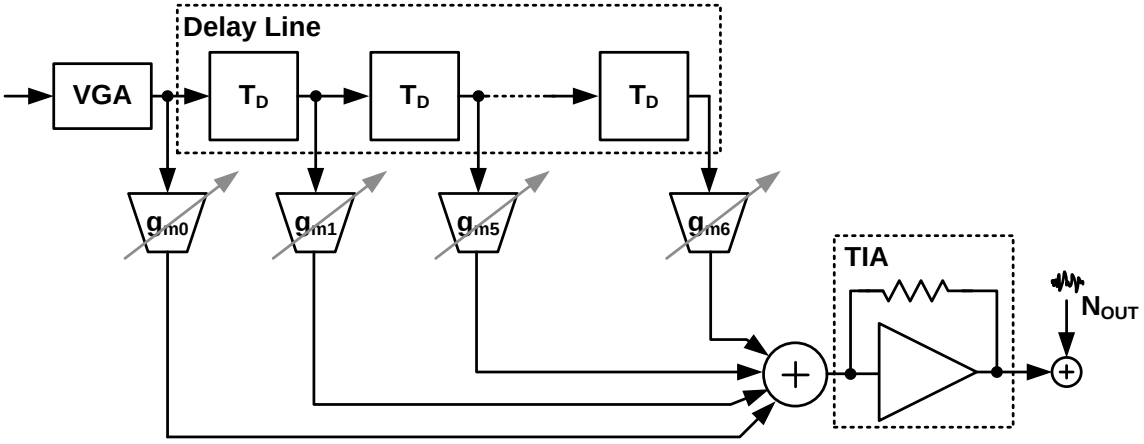


Figure 4.1: FFE block diagram.

This chapter presents the circuit design and is organized as follow:

Sections from 4.1 to 4.3 describe the delay elements, multipliers and TIA. The design of input and output interfaces for testing is presented in Section 4.4 while Section 4.5 provides an overview of the chip at top level.

4.1 Delay line element

Continuous time FIR equalizers operating at more than 10Gb/s usually exploit lumped-elements delay lines realized with cascaded LC-ladder sections to simultaneously meet the requirements for high delay and wide bandwidth. However LC sections suffer from narrow tuning range and require excessive silicon area due to the need for high Q inductors.

To achieve wide delay tuning range and small size, continuous time active delay lines are potentially attractive. Several solutions have been proposed by cascading low-pass filter sections. Unfortunately, delay trades with bandwidth and to achieve a sufficiently wide bandwidth, reported FIR equalizers have a too limited number of taps and small tap-to-tap delay [46],[47].

A CMOS all-pass stage has been investigated to implement the active delay line. The block diagram is shown in Fig. 4.2.

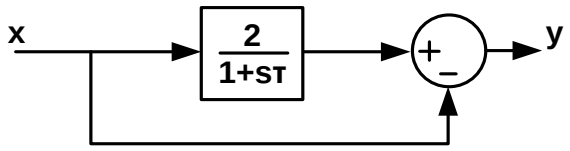


Fig. 4.2. Block diagram of the all-pass stage.

It is realized with a one-pole low-pass filter with time constant τ, and a unity-gain path. The transfer function *H(f)* and group delay $\tau_g(f)$ are:

$$H(f) = \frac{1 - j2\pi f\tau}{1 + j2\pi f\tau} \qquad (4.1)$$

$$\tau_g(f) = \frac{2\tau}{1+(2\pi f\tau)^2} \qquad (4.2)$$

The frequency response is ideally flat, thus exempting the all-pass stage from the trade-off between group delay and bandwidth typical of low-pass filters.

The in-band group delay is 2τ and decreases with frequency. Since a higher τ results in a larger high-frequency roll-off, a more constant tap-to-tap group delay T_d could be achieved, if required, by cascading several all-pass sections each one featuring a smaller τ. As an example, Fig. 4.3 plots T_d versus frequency assuming a tap-to-tap delay element realized with n = 1, 2 and 3 cascaded all-pass stages (Fig 4.4 shows the corresponding responses to a Gaussian pulse). It is also assumed T_d=3/4T_S and the frequency axis is normalized to Nyquist frequency, 1/(2T_S). Increasing n from 1 to 3 limits the T_d roll-off at Nyquist from 60% to 15%. On the other hand, a 7-tap FIR equalizer would require 18 all-pass sections, leading to prohibitively large power dissipation.

To minimize power consumption, the tap-to-tap delays have been realized with only a single all-pass stage. Meanwhile, for a targeted transfer function, the impact of the group delay roll-off over frequency can be partly compensated by properly adjusting the filter coefficients. To gain insight on this behavior, let's first consider the simplified case of a two-taps FIR equalizer providing 15 dB boost at Nyquist. Fig. 4.5 compares the transfer functions achieved with a flat tap-to-tap delay and with an all-pass stage.

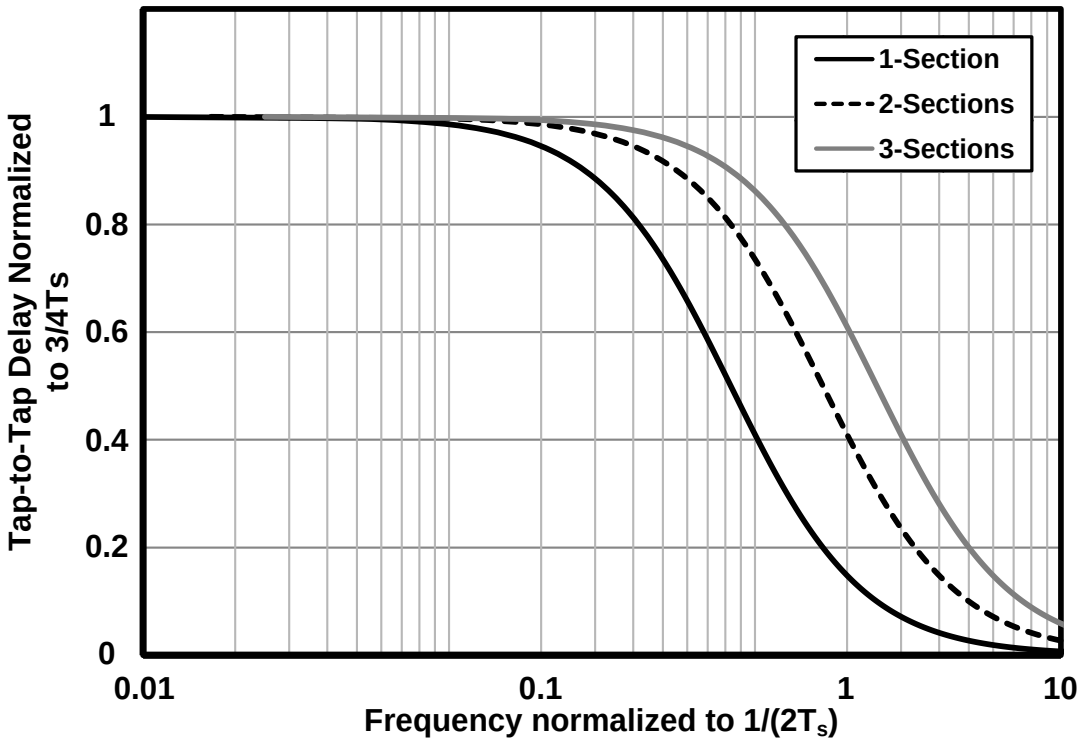


Fig. 4.3. Tap-to-tap delay realized with a different number of all-pass sections.

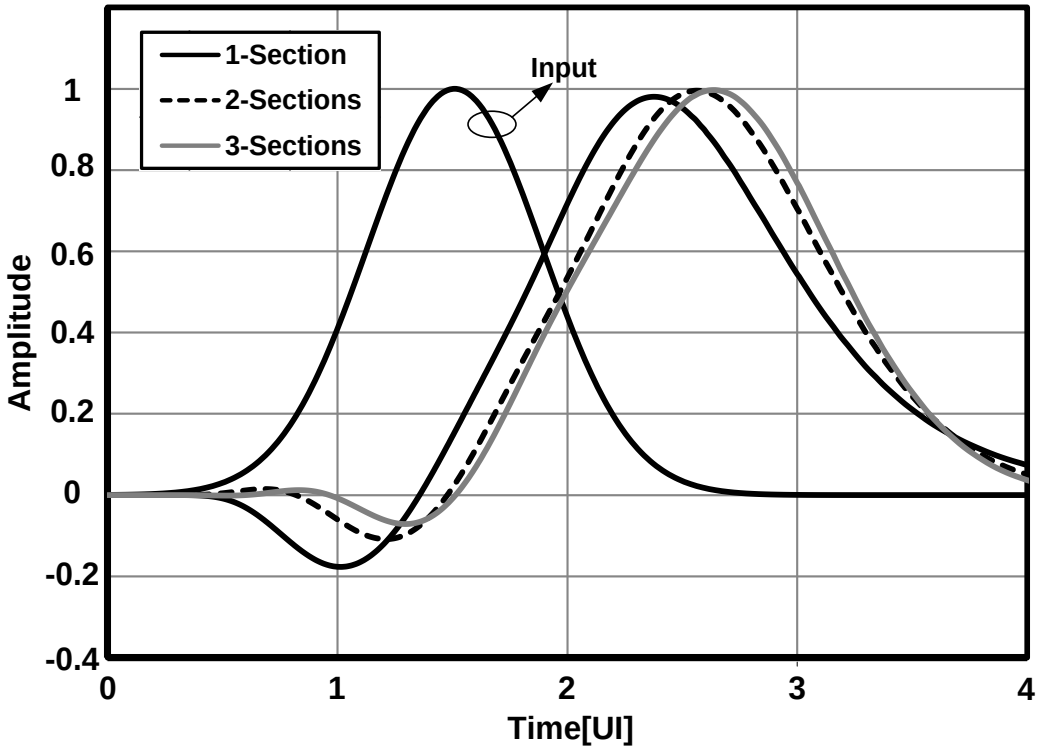


Fig. 4.4 Gaussian pulse responses to all-pass delay realized with a different number of all-pass sections.

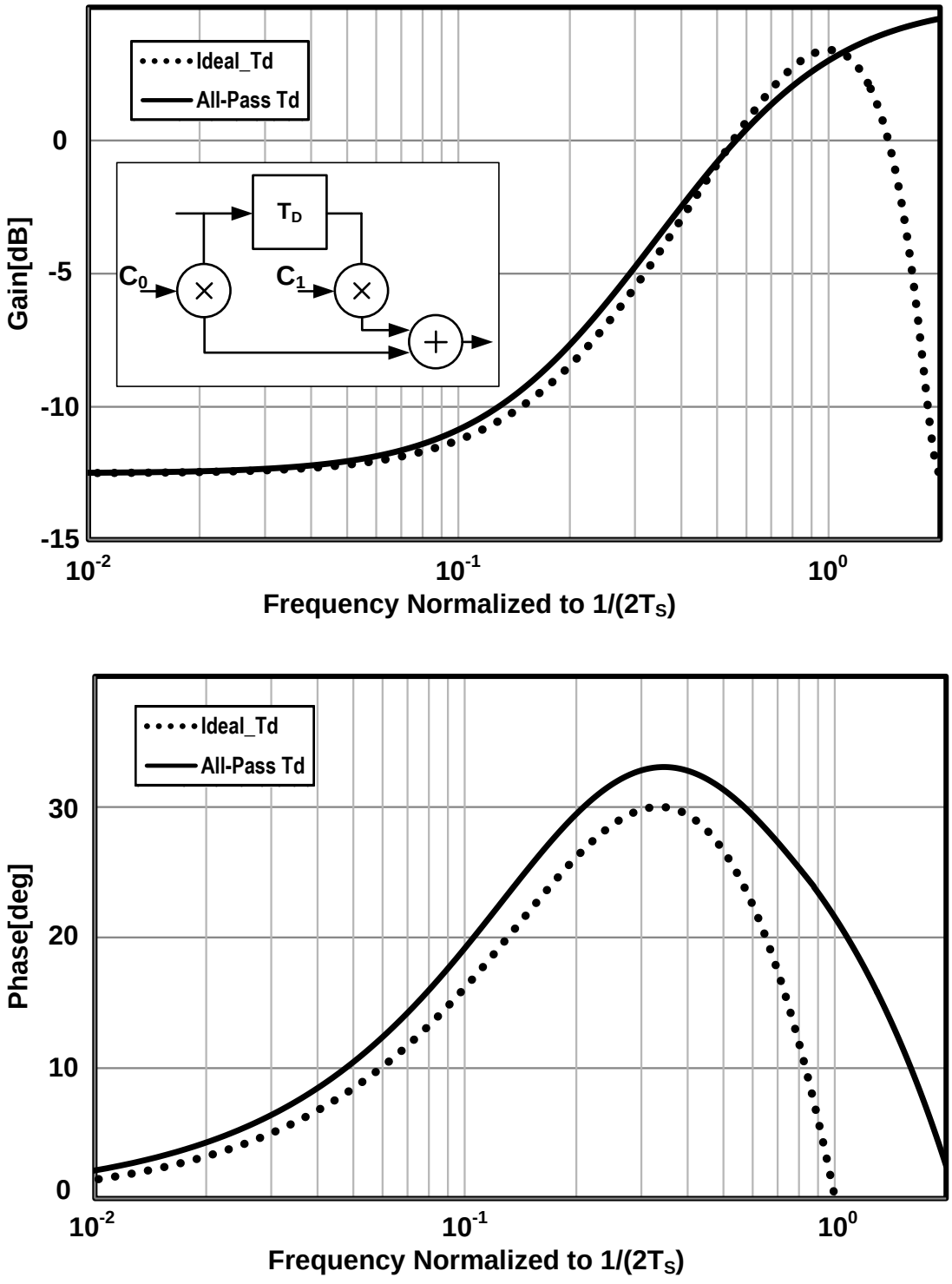


Fig. 4.5. Transfer functions of a two-taps FIR equalizer providing 15 dB boost at Nyquist Frequency with the tap-to-tap delay realized with an all-pass section and with an ideal flat delay.

In the ideal case the filter coefficients are (C_0, C_1) = (0.87, -0.6) while with the all-pass delay stage they are slightly changed to (C_0, C_1) = (1, -0.74). The in-band transfer functions are very similar, with less than 1 dB maximum deviation. Additionally, the T_d roll-off introduced by the all-pass section enables gain boost well beyond the Nyquist, as ideally provided by a fractionally-spaced equalizer with small tap-to-tap delay. Phase response deviates from the ideal case around Nyquist frequency, but this effect is negligible in equalization performances. In the more complex case of the 7-tap FIR equalizer, simulations including the coefficients adaptation algorithm confirm that the group delay roll-off does not compromise the equalization capability. This is further confirmed by the experimental results presented in the next chapter.

Fig. 4.6 shows two possible CMOS differential circuits implementing the all-pass stage block diagram of Fig. 4.1. g_{m1} and the R-C load form the low pass filter with gain $g_{m1}R=2$ and time constant $\tau=RC$. In the circuit of Fig. 4.6(a) the input and the filtered signals are subtracted by combining the output currents of g_{m2} and g_{m3}, while in the circuit of Fig. 4.6(b) the two voltage signals are subtracted at the input of the transconductors g_{m2} and g_{m3}.

The latter solution has been selected because it provides a remarkable dynamic range improvement. In fact, the maximum voltage swing at the input of g_{m2} is reduced from $2V_{in}$ to $V_{in}/2$. The maximum swing, equal to V_{in}, is at the input of g_{m1} and compared to the circuit in Fig. 4.6(a) the topology in Fig. 4.6(b) improves 1 dB compression point by ~6 dB.

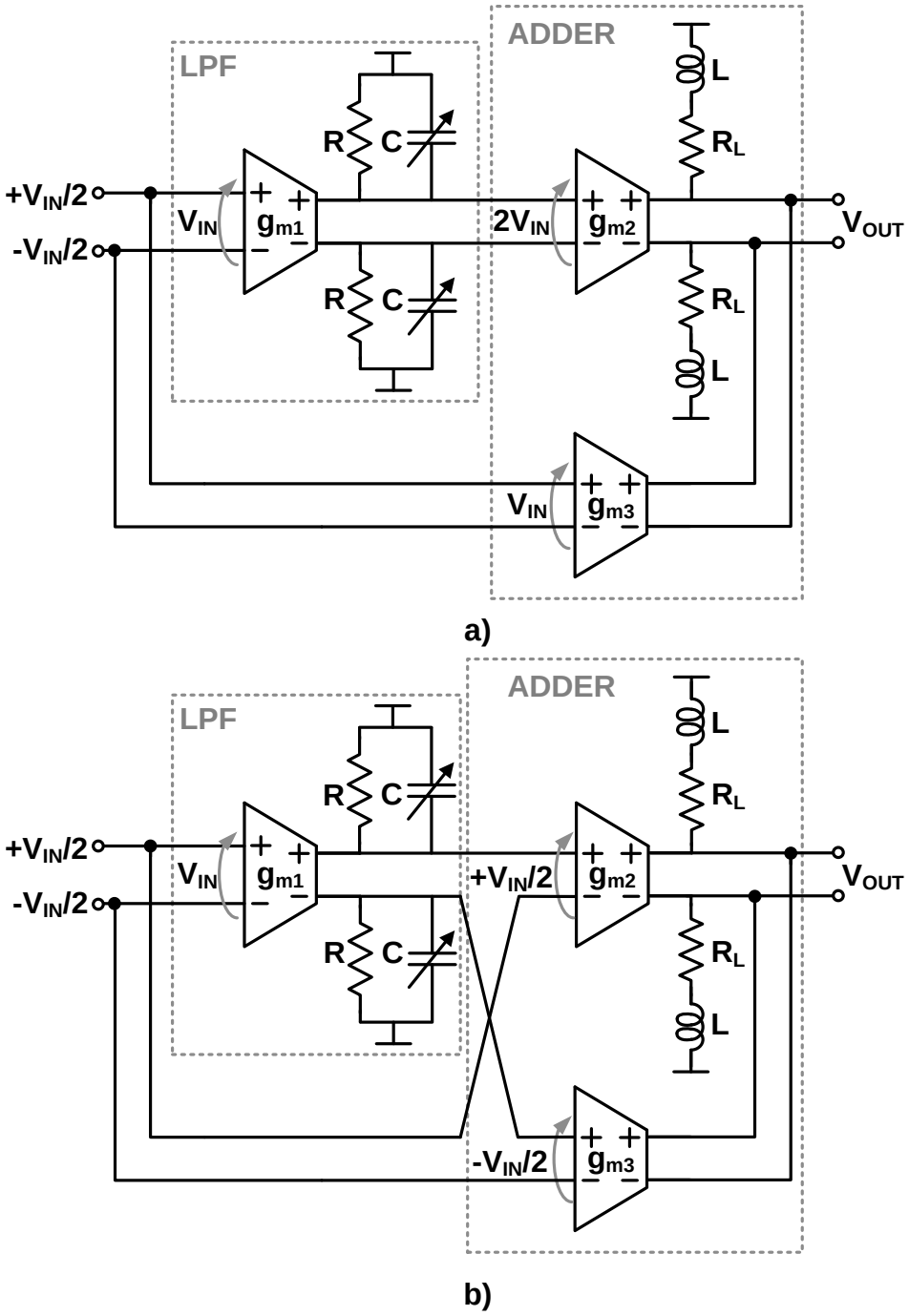


Fig. 4.6. Possible CMOS realizations of the all-pass stage.

The circuit has been designed with all the transconductors sharing the same transistors size of 20μm/28 nm. The overdrive of g_{m1} determines the linearity of the stage and nominal bias current was set to 3mA leading to 1dB compression point of

220mV$_{0\text{-}pk}$, high enough to meet the minimum 200mV$_{pk\text{-}pk}$ input signal swing requirement of Table-II with negligible distortion. Load resistors are digitally programmable (with 3-bit logic) to correct processing spreads and typical values are R_L=100Ω and R=200Ω. Furthermore tail currents of the differential pairs are set with a replica bias circuit which keeps the gain of the stages constant. From simulations, the gain drift due to supply and temperature variations is within 1dB.

The in-band group delay can be tuned from 75ps to 30ps by digitally programming the capacitive load of g_{m1}, thus covering the 10Gb/s - 25Gb/s data-rate interval (Fig. 4.7a). Low-Q peaking inductors L of 500pH are introduced in series with the load resistors R_L to extend the bandwidth, limited by the capacitance loading of the tap amplifier and the cascaded stage. Bandwidth and power dissipation of the all-pass stage can be scaled from 14GHz with 5.5mW to 25GHz with 9mW by programming the load resistors and biasing currents (Fig.4.7b).

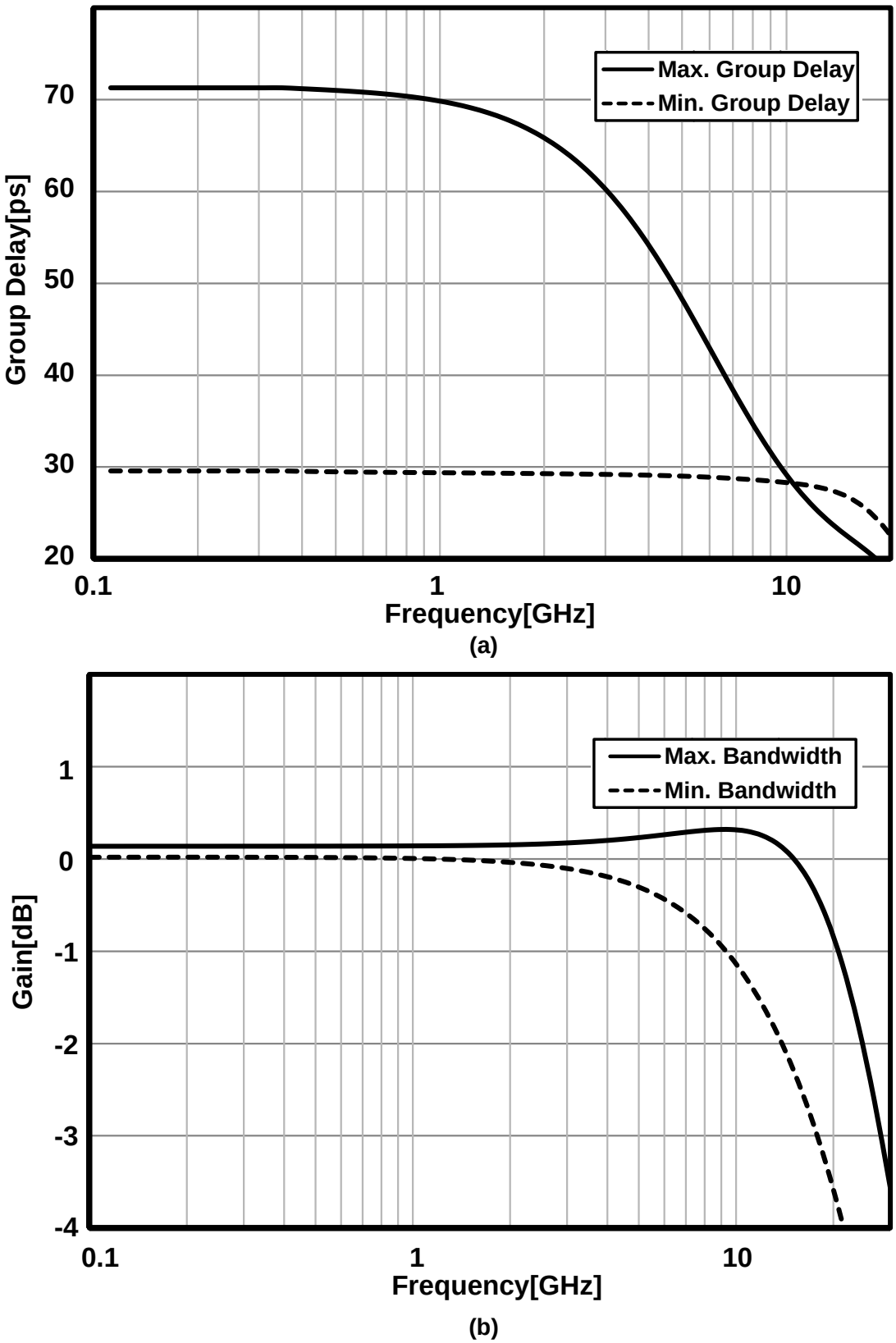


Fig. 4.7. All-pass delay cell response: (a) group delay, (b) magnitude response.

4.2 Taps amplifier

Another key block of a FIR equalizer is the programmable tap amplifier. It is commonly realized with Gilbert cells [48] [49]. This technique suffers from a few shortcomings. Fig. 4.8 represents one such multiplier, which works in four quadrants. The input signal is fed to two high-speed differential pairs whose outputs are connected with opposite polarity. This connection leads to subtraction of the output current of one differential pair from the other. By adjusting the relative current of the differential pairs, the output signal swing can be changed. More specifically, the tap coefficient is controlled through digital control bits that are fed to a DAC. The output analog voltage steers the multiplier current from one high speed differential pair to the other, and hence adjusts the magnitude of the output swing.

In addition, Gilbert cell multiplier gain steps are non-linear [50]. Although degeneration resistors can be added to increase the linear region of the multiplier, the multiplication step size still exhibits non-uniformity, especially when the current of one side is much larger than the other.

In addition, when the Gilbert cell is close to its gain limit, one of the high-speed differential pairs receives only a small amount of current which creates significant total harmonic distortion (THD) at the output. Since an FFE is a linear filter, it is incapable of compensating nonlinearity, and therefore, multiplier THD greatly degrades the equalizer performance.

The adopted solution, similar to the topology proposed in [50] is shown in Fig. 4.9.

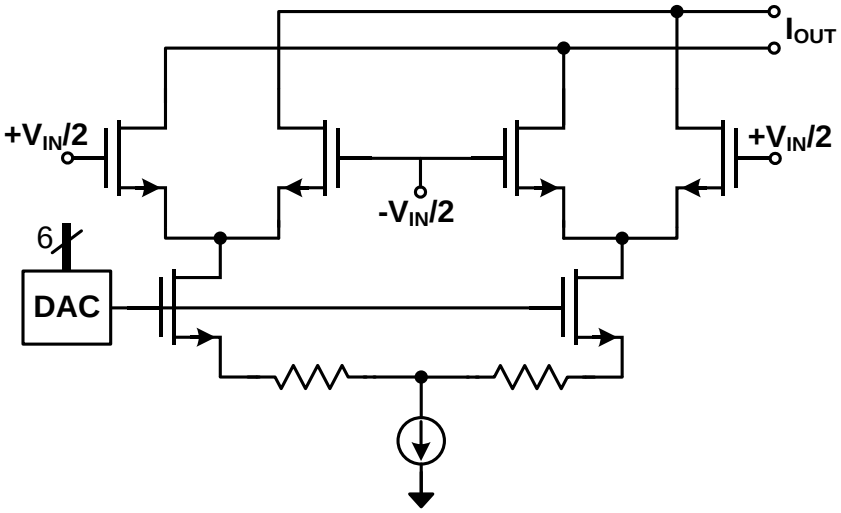


Figure 4.8: Conventional Gilbert cell multiplier.

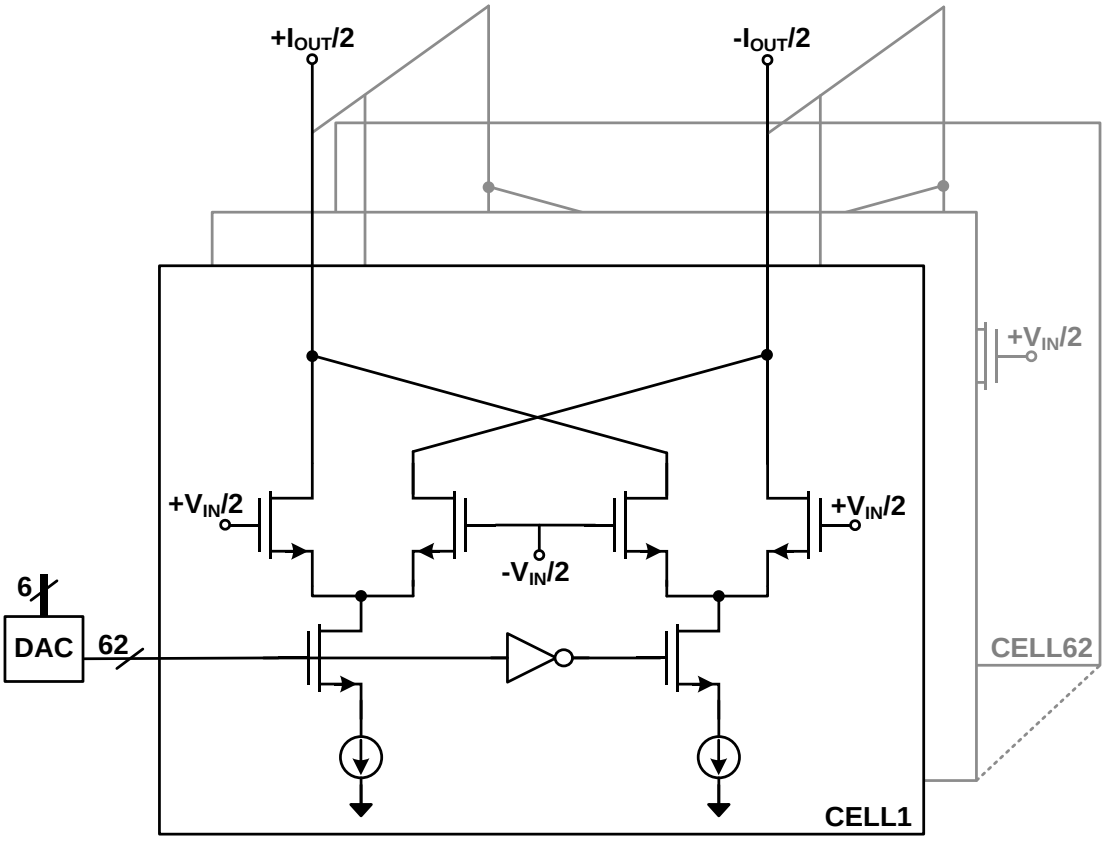


Fig. 4.9. Schematic of a digitally-programmable tap transconductance amplifier. Each amplifier comprises 62 elements in parallel.

To achieve positive and negative gains, each unit element includes two digitally controlled differential pairs, driven by the same input signal but delivering output currents with opposite sign. Only one pair is active at a time. If $\bar{g}_m$ is the transconductance of a single differential pair and *N* is the number of slices configured with a positive gain, the overall transconductance is $g_m = \bar{g}_m(2N - 62)$. A logic decoder is implemented to control the 62 slices with a 6-bit programming code. Since the gain is actually controlled in a thermometric fashion, monotonicity with the programming code, fundamental for the equalizer adaptation, is ensured.

Fig. 4.10 shows the simulated multiplier behavior as the value of *N* is varied from 0 to 62. The uniformity of the multiplier gain step is evident in this simulation result.

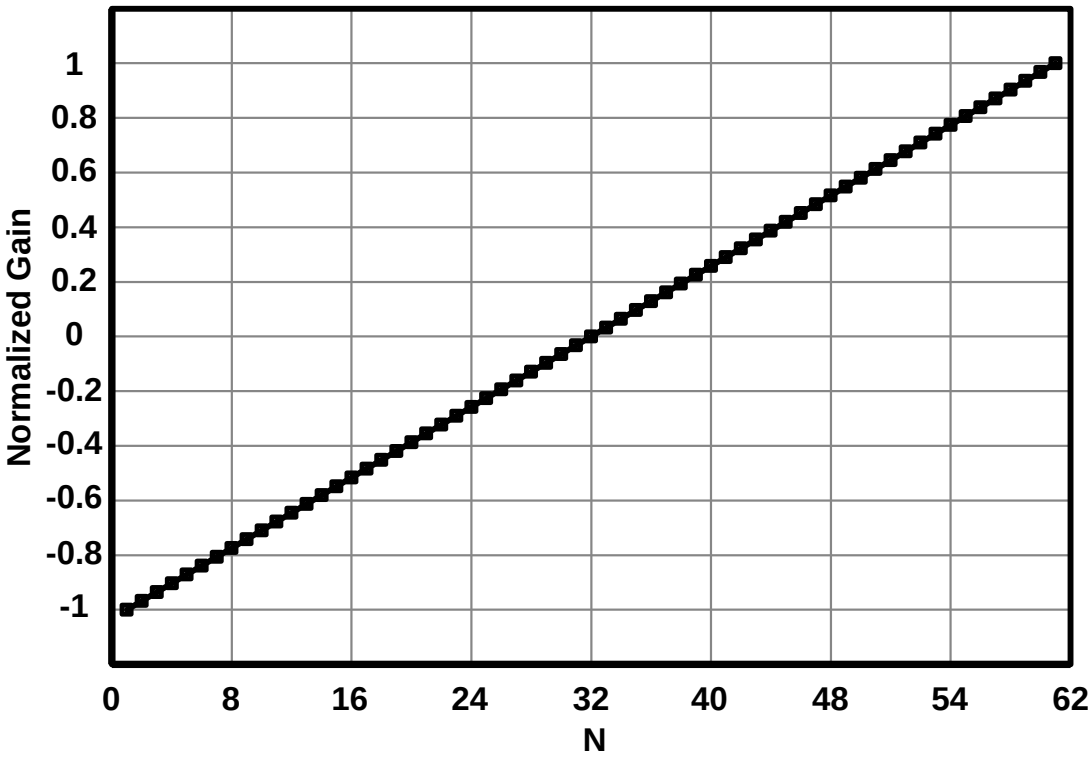


Figure 4.10: Multiplier normalized gain as a function of *N*

Compared to analog multipliers this topology features a linearity independent from the gain because the latter is varied without changing the transistors overdrive voltage. Moreover, the DC output current is constant, thus simplifying the regulation of the common-mode at the nodes where all the taps signal currents are summed.

Each tap amplifier is biased at 1.5 mA and transistors have been sized with an overdrive voltage providing the same input 1dB compression point of the delay elements ($220mV_{0\text{-}pk}$). The transconductance gain is programmable within ±6.5 mS.

4.3 Trans-Impedance Amplifier

In a 7-tap FFE summation of the signal currents is challenging. The tap amplifiers and their relatively long interconnections result in high output parasitic capacitance (~250fF in this design) introducing a severe gain-bandwidth trade-off if the current are summed with a simple resistive load. As an example, with a 200-Ω resistor and 250fF parasitic capacitance the pole frequency would be ~3.2GHz only. As proposed in [51], a feedback TIA is adopted providing better noise performances than small resistors followed by an open-loop amplifier [52][53].

The TIA has been designed to achieve a gain up to 46 dBΩ, allowing maximum filter coefficients in excess of ±1 when the tap transconductors are programmed at the maximum gain (6.5mS). The schematic is shown in Fig. 4.11. M_1, biased by M_3, form the core amplifier while R_T is the feedback resistor. M_2 provide the biasing current to the taps. To meet the bandwidth required by a 25Gb/s data-rate, peaking inductors of 1nH are used at the output and M_1 is sized to provide up to 70mS transconductance.

Only minimum channel length transistors, featuring a very low intrinsic gain (g_m/g_{ds}=4-6), have been used in the design.

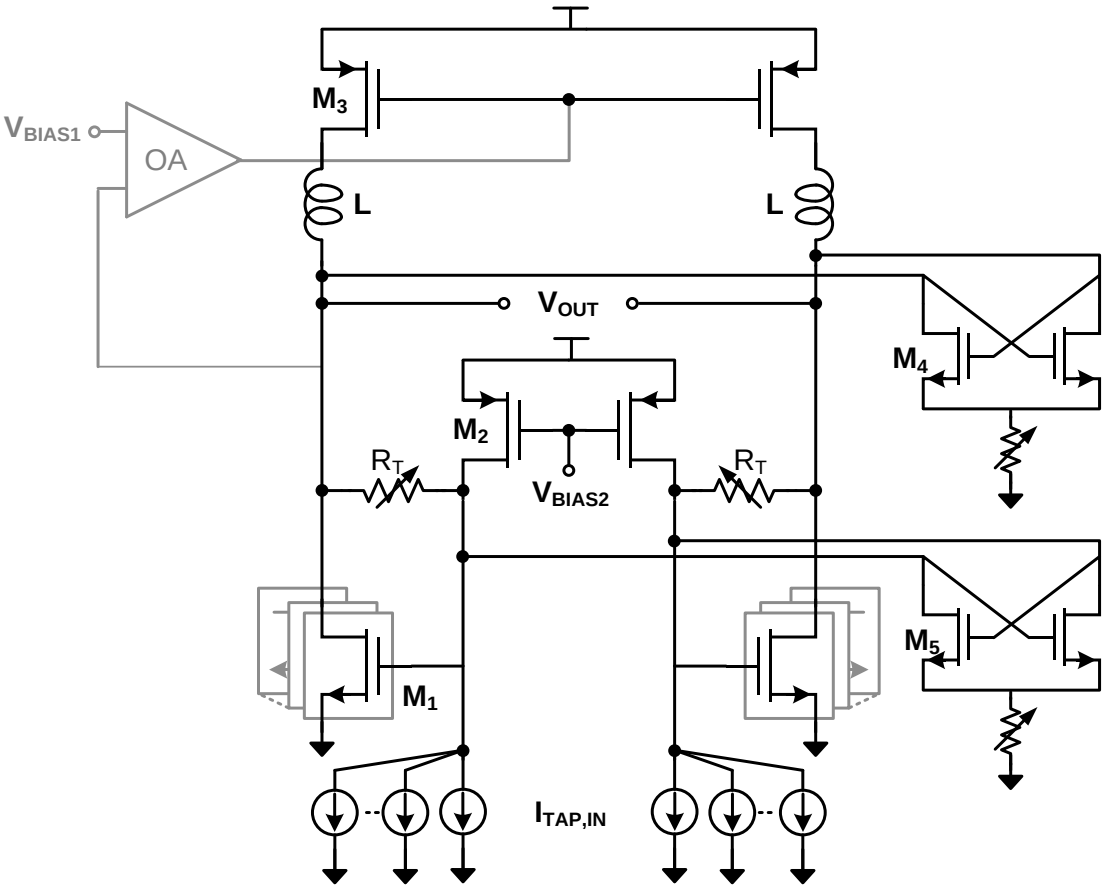


Fig. 4.11. Schematic of the TIA.

The high output conductance of the devices impairs the TIA performances. Instead of using cascode stages, which would introduce parasitic poles and limit signal swing, negative resistors, realized with the cross-coupled pairs M_4 and M_5, are introduced in parallel to the input and output ports of the TIA to partially cancel the devices output conductance. Figure 4.12 compares the simulated trans-impedance gain with and

without the cross-coupled pairs. The negative resistors allow more than 7 dB gain improvement at negligible power dissipation.

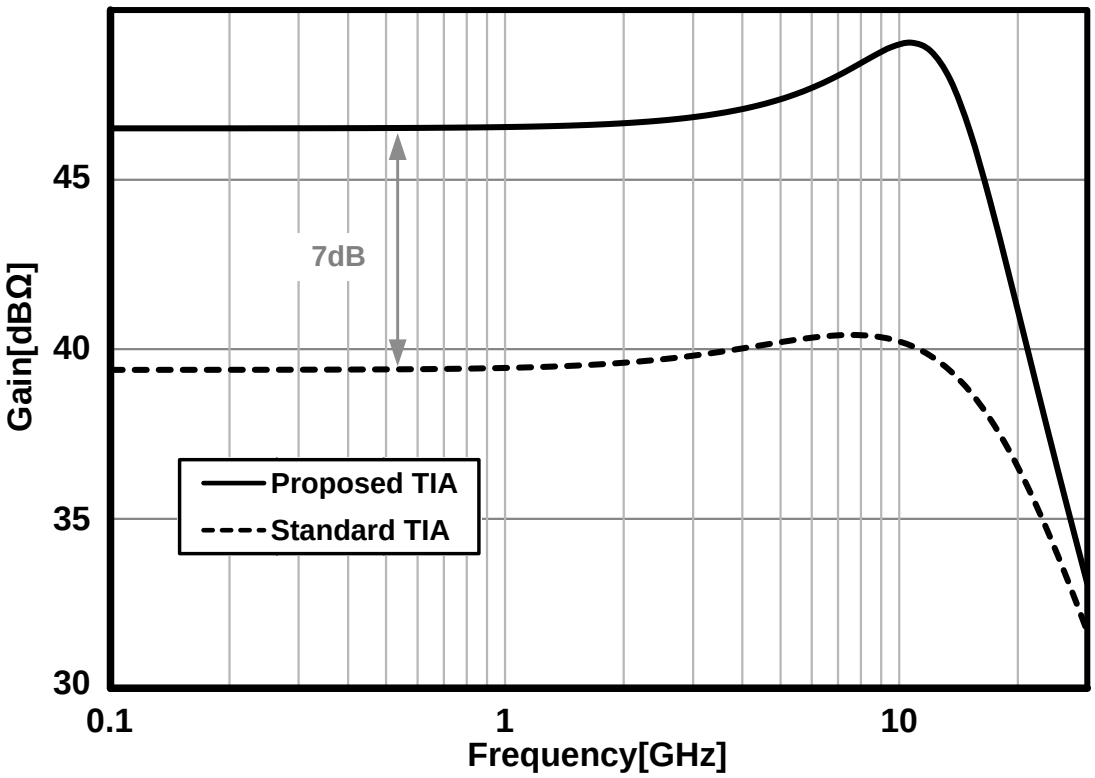


Fig. 4.12. Comparison of TIA trans-impedance with and without negative resistors.

At maximum gain TIA -3dB bandwidth is 17 GHz, enough for a 25Gb/s equalizer, with a power consumption of 25mW. To have maximum flexibility and keep high power efficiency, gain, bandwidth and power dissipation can be reconfigured by changing the feedback resistor and switching ON and OFF parallel unit elements of $M_{n1,2}$. The transimpedance gain is programmable from 33 to 46dBΩ while the -3dB bandwidth can be reduced down to 9 GHz with 10mW dissipation at 10Gb/s (Fig. 4.13).

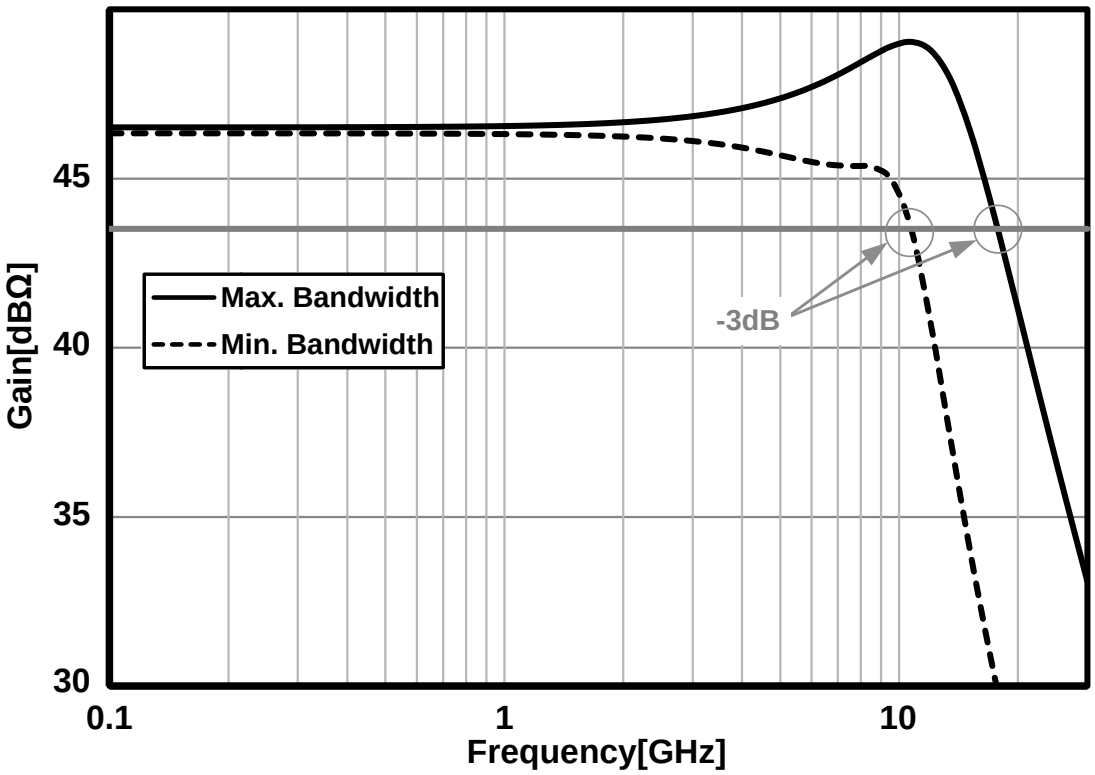


Fig. 4.13. Comparison of the TIA -3dB bandwidth for 10-25Gb/s operation mode.

The noise performance of the complete FIR equalizer has been evaluated with simulations. Total output noise changes with the multipliers coefficients because of the non-negligible contribution from the active stages of the delay line. With all the coefficients set to zero (i.e. with the tap amplifiers programmed for an equivalent transconductance of 0mS) noise of the delay line stages does not reach the output. In this case, with the TIA at maximum bandwidth, the simulated N_{out} is 1.8mV$_{rms}$, determined only by the tap amplifiers and TIA. With all the tap amplifiers at maximum gain, which should represent a worst-case situation, N_{out} rises to 4.2 mV$_{rms}$, still meeting with margin the target requirement of table II.

4.4 Input and output interfaces

The chip is packaged in a flip-chip Ball Grid Array (BGA) where on-die bumps are used to transfer data between the die and the package. The required spacing between the bumps is dictated by the package which leads to 150µm-long interconnect between the bump and the chip 25Gbps I/O.

The bumps are connected to on-chip 100Ω differential terminations through a transmission line. The input dc voltage is set using a resistor, R_T, and current source, I_T, as shown in Fig. 4.14. The value of R_T and I_T is chosen so that the resultant dc voltage is equal to FFE stages common mode voltage.

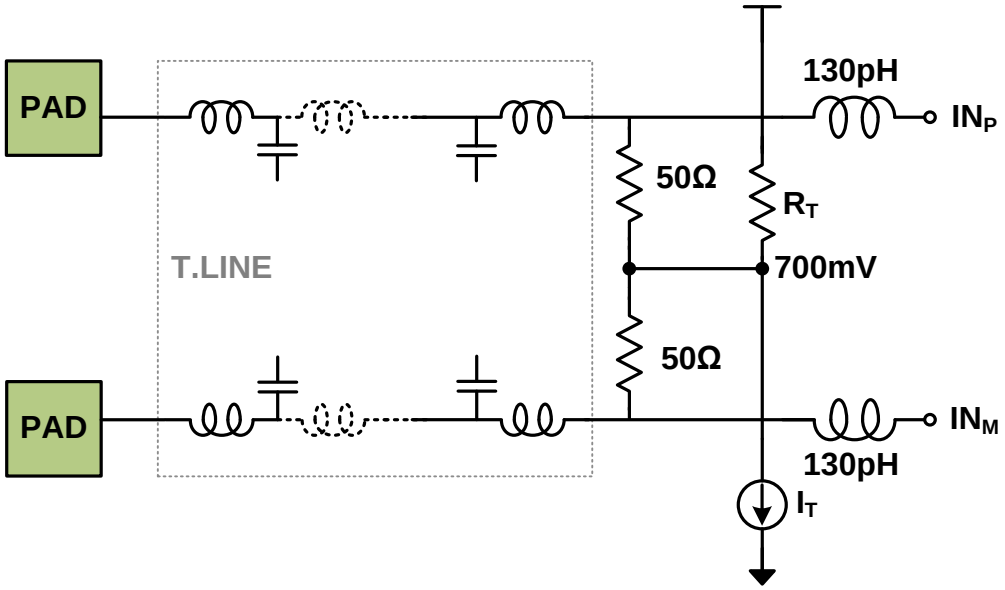


Figure 4.14: 100Ω differential input termination.

In addition, to compensate for the first stage input gate capacitance, a pair of inductors is added to the input lines.

The simulated ac response of the input path, that includes 4-port S-parameter model of the package, on-chip micro strip lines and the 100Ω termination show a -3dB bandwidth of 22GHz, enough for a 25Gb/s signal.

The input network is connected to a Variable Gain Amplifier (VGA) introduced in front of the FIR equalizer, as shown in Fig. 4.1. The VGA is used to control the signal amplitude on the delay line. It is realized with a circuit topology similar to the tap amplifiers. The gain is controlled within -6 to + 6 dB with 5 bits resolution (Fig. 4.15).

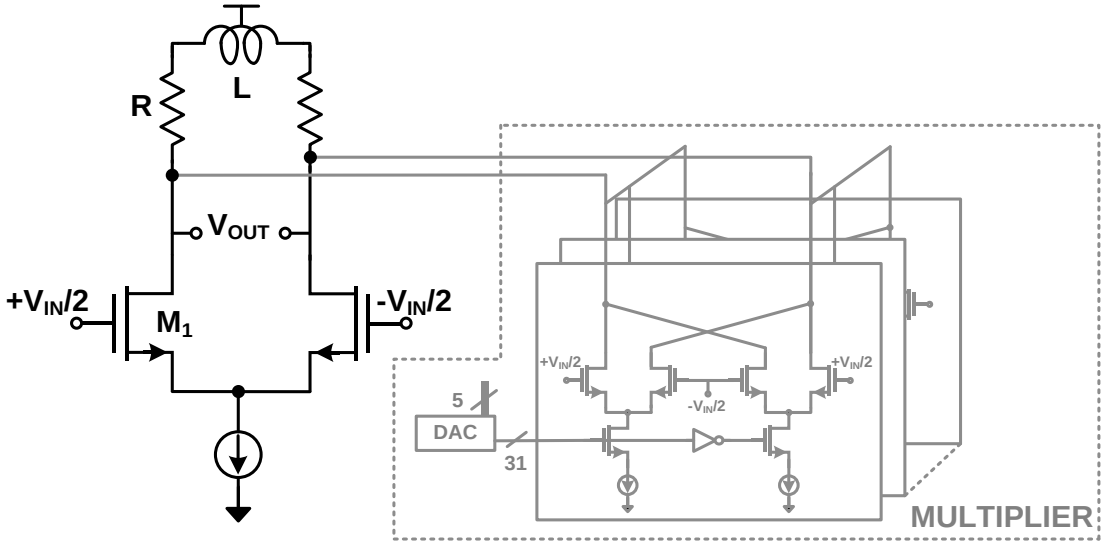


Fig. 4.15. Schematic of the Variable Gain Amplifier.

The FIR filter is followed by a three-stage output buffer. Each stage, realized with a shunt-peaked CML stage with resistive degeneration, provides a 0-3.3dB programmable gain for a total gain from 0 to 10dB.

4.5 Chip top level

Fig. 4.16 shows the chip top-level block diagram where the digital and the analog blocks are differentiated by their shade.

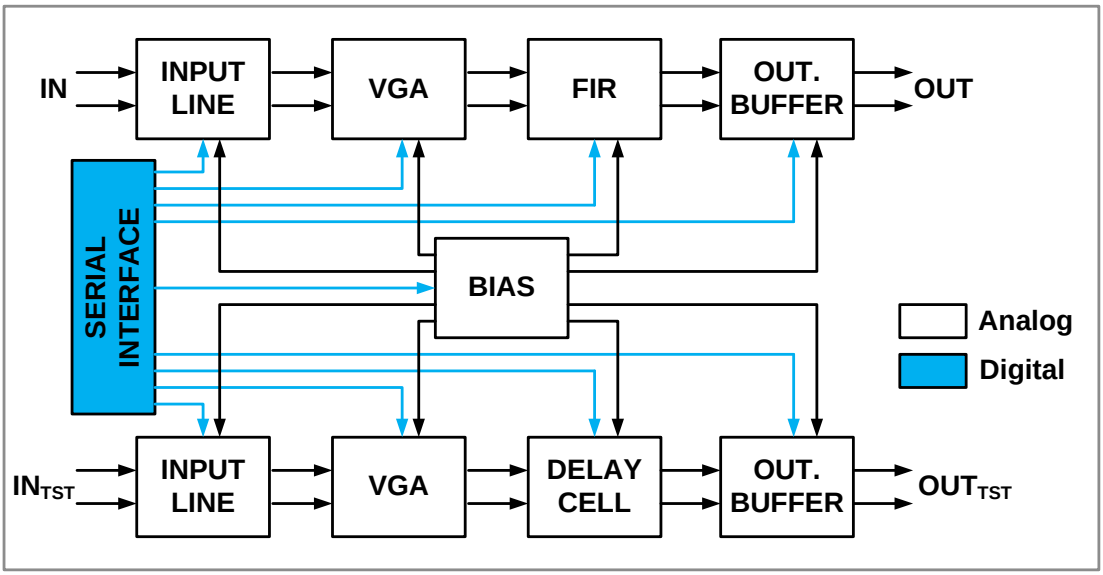


Figure 4.16: Chip block diagram.

The incoming 25Gb/s data is fed into the input termination block discussed in Section 4.4. The FIR core equalizes the received signal with ISI and output is then transmitted out of the chip though the output buffer. The biasing-block (Band-Gap) generates the required currents for the input termination, FIR and the output driver. The digital control signal for the FIR and the bias blocks are provided by a serial interface. A second path is used to test the VGA and a single-stage delay. As mentioned, the chip was manufactured using a 28nm standard CMOS process and the FIR core, shown in Fig. 4.17, has an area of 0.085mm^2.

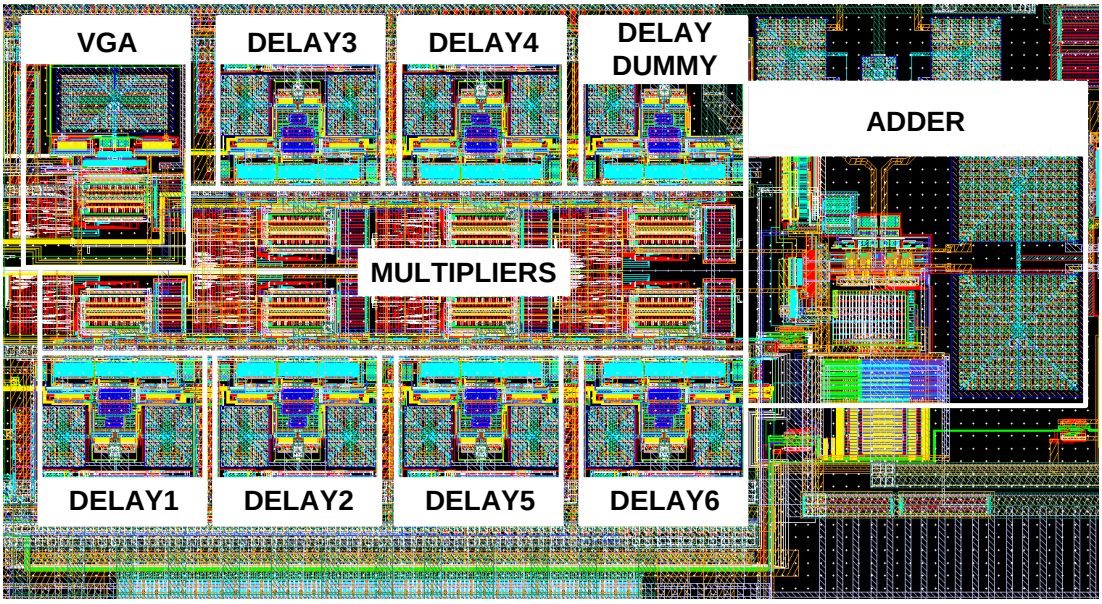


Fig. 4.17. Layout of the FFE core.

The chip expected performance is summarized in table III and the photomicrograph of the realized prototype is showed in Fig.4.18 where each sub-blocks are highlighted.

Functionality		7 tap 3/4T spaced FIR equalizer
Data Rate		10-25Gb/s
Technology		28nm CMOS
VDD		1V
-3dB Bandwidth	Delay cell	≈ 25 GHz
	Multiplier+Adder	≈ 17 GHz
	Driver	≈ 20 GHz
Maximum Output Noise		$4.8mV_{RMS}$
Power Consumption		55-90mW
Package		Flip chip plastic BGA

Table III: Chip performance summary.

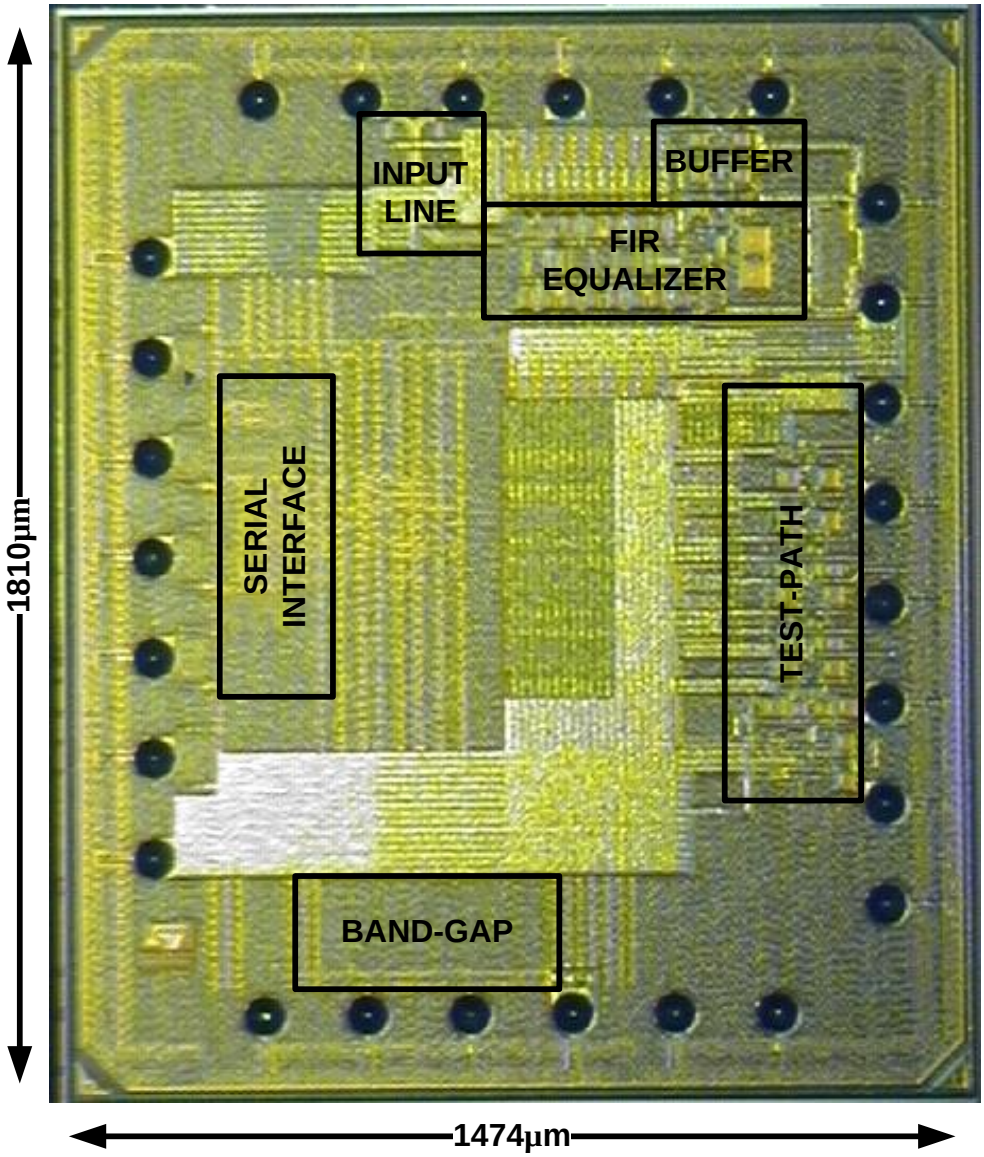


Figure 4.18: Photomicrograph of the realized test-chip.

Chapter 5

FIR Equalizer Measurements

Experimental results on the realized test chip are presented in this chapter. Small-signal AC measurements, maximum input amplitude and taps gain are shown in Section 5.1. Section 5.2 is dedicated to time-domain measurements. In particular, eye diagrams quality is used to highlight the chip equalization capability from 10 to 25Gb/s. Measurement setup, PC-assisted equalization, and optical-channel emulation are also described in this section. Finally, in Section 5.3, measurements of the FIR equalizer cascaded with a Ser-Des provided by STMicrolectronics to implement a complete EDC are presented.

5.1 Gain, Frequency Response and Compression

Small-signal AC measurements have been performed with a four-port Vector-Network-Analyzer, Agilent PNA-X N5245S, to assess the functionality of the prototype. The performance of the package and on-chip termination is characterized by the return loss parameter S_{11} shown in Fig. 5.1. Measurements are in good agreement with the expected shape from simulations. S_{11} is lower than -10dB up to 20GHz. To verify DUT bandwidth, in particular VGA, TIA and output buffer blocks, some measurements have been carried out by activating only the first tap in the FIR equalizer (Fig. 5.2). The results are shown in Fig.5.3 where VGA is modified from minimum to maximum gain. Gain can be changed from -4 to 8dB and total bandwidth

is limited to 13GHz by package parasitics.

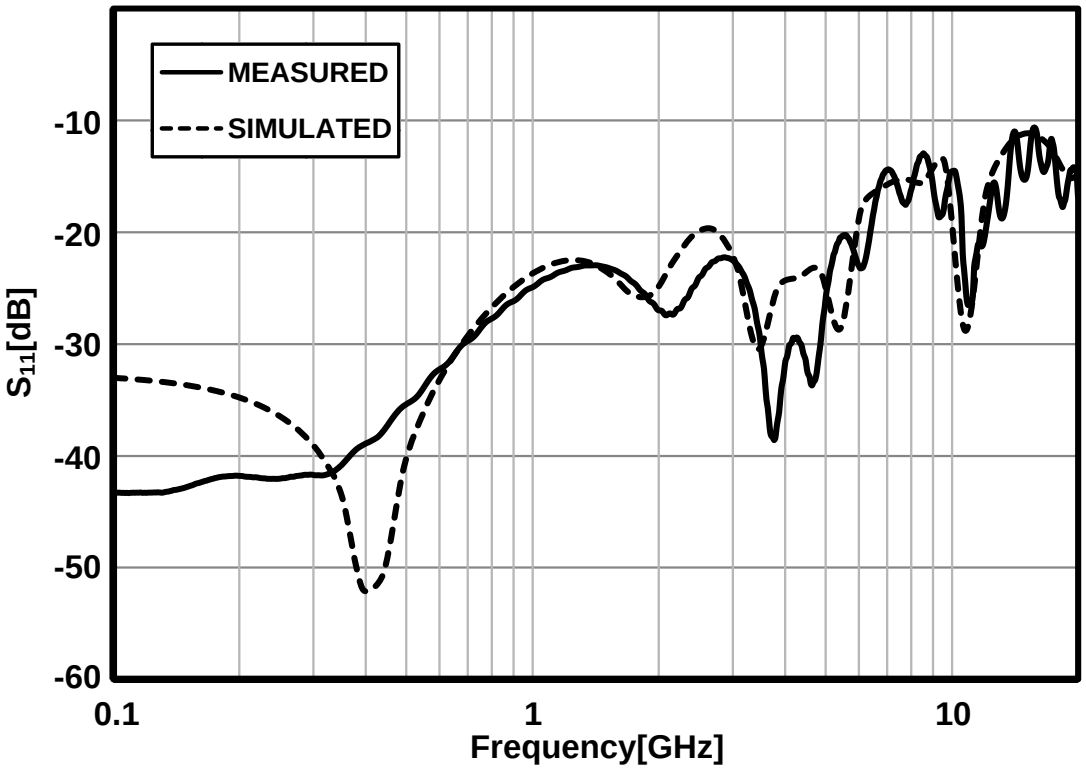


Figure 5.1: Input return loss of measured chip and board.

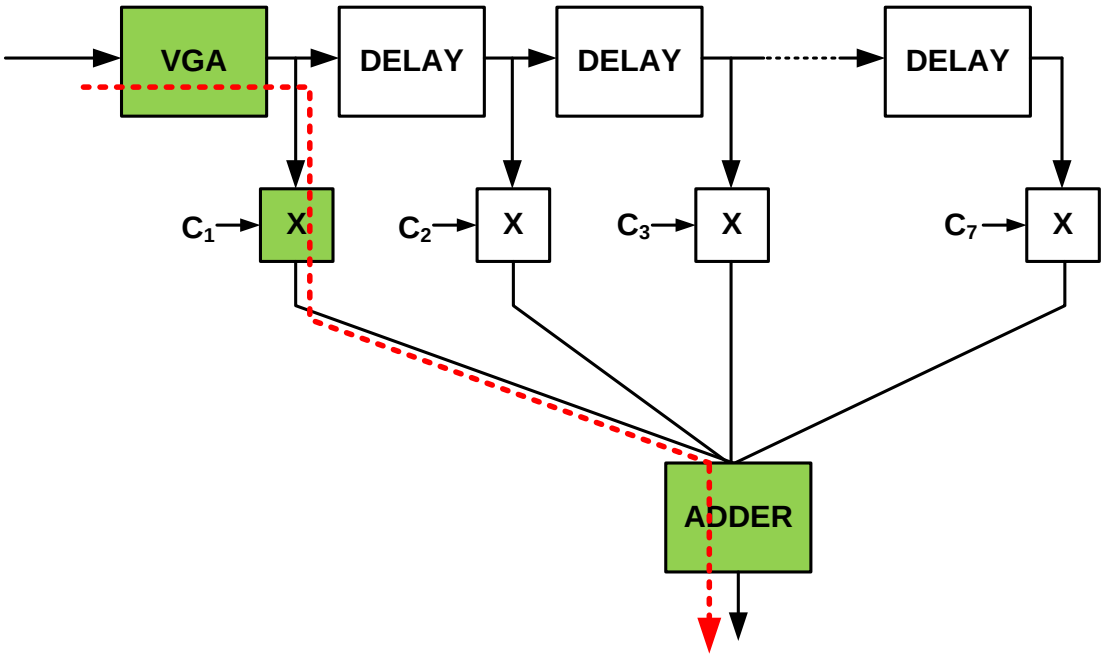


Figure 5.2: Path used to measure VGA, TIA and output buffer transfer function.

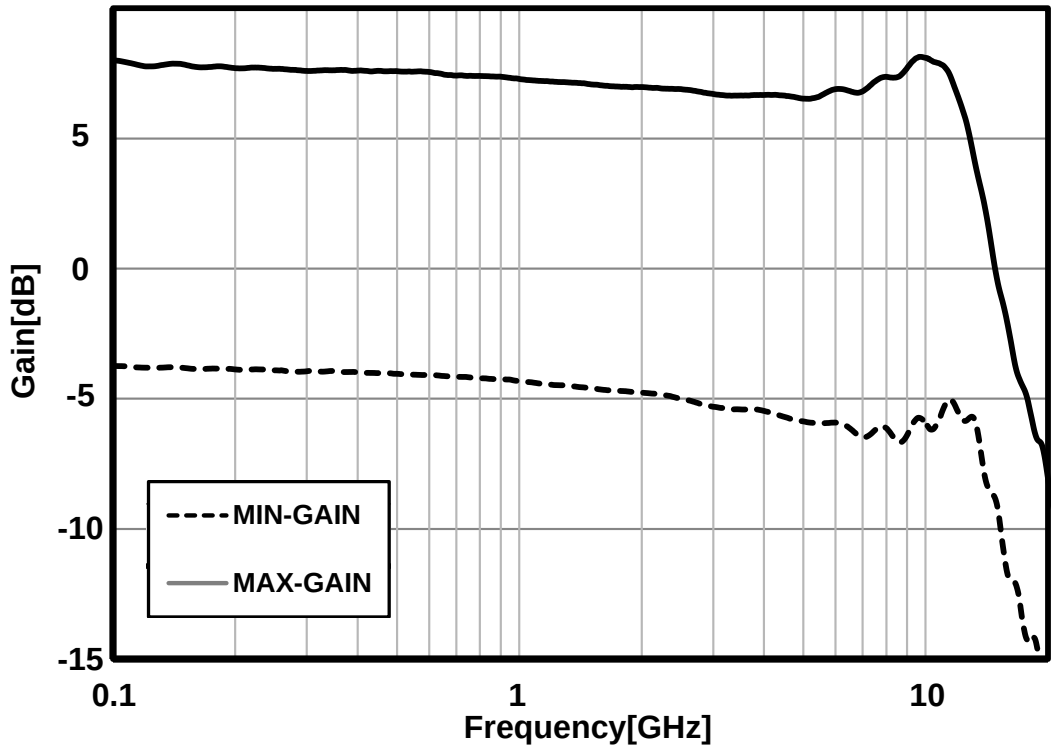


Figure 5.3: Input-output transfer function of FFE with only first tap active.

With the same setup, transient measurements have been performed to verify the correct operation of the taps and test the linearity of the filter. A sinusoidal signal was fed to the differential input through a SMA balun while the differential outputs were connected to a sampling scope. Fig. 5.4 shows the output signal when a single tap is active and the gain programmed from the minimum negative value to the maximum positive value. Monotonicity, key feature for the correct operation of adaptation algorithms, is verified for all the taps and among different samples

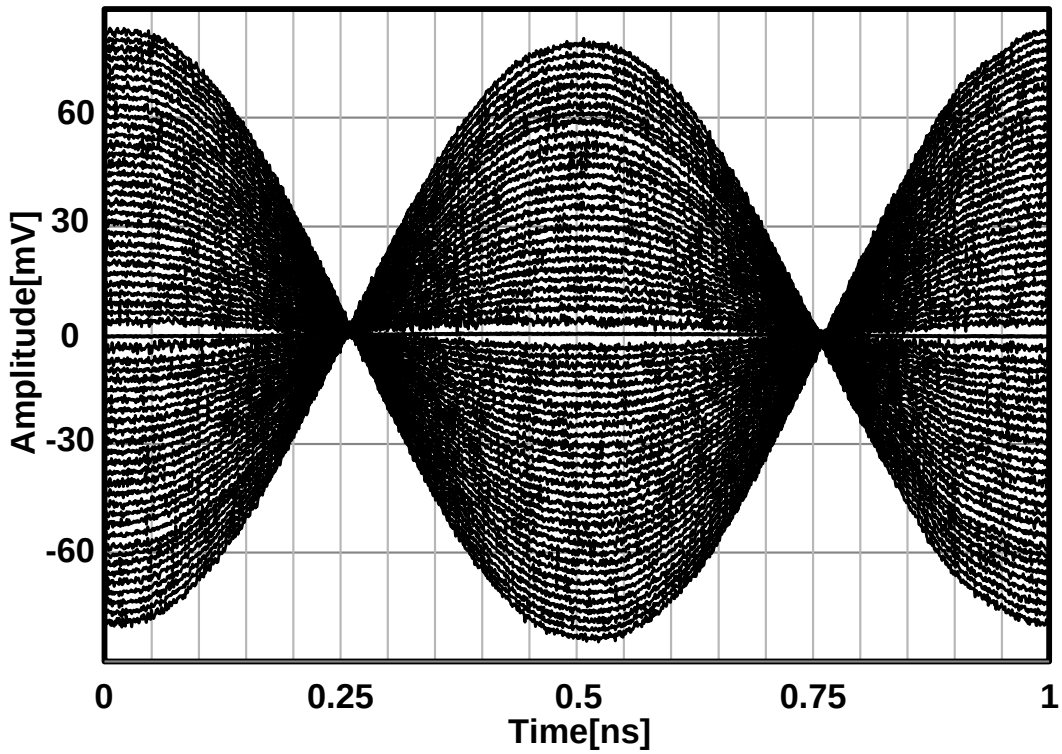


Figure 5.4: Measured output sinusoids with a single tap active and gain sweep from min to max.

Compression measurements, fundamental to evaluate the distortion introduced by equalizer, are reported in Fig. 5.5 showing the normalized gain as a function of the input voltage swing with the first and the last tap active at maximum gain. The input 1dB compression point when the signal flows only through the first tap is -14.5dBV ($380mV_{pk-pk}$) while it is reduces to -16.4dBV ($300mV_{pk-pk}$) when it flows through all the delay line. This value is in line with minimum input signal defined by system level simulations ($200mV_{pk-pk}$).

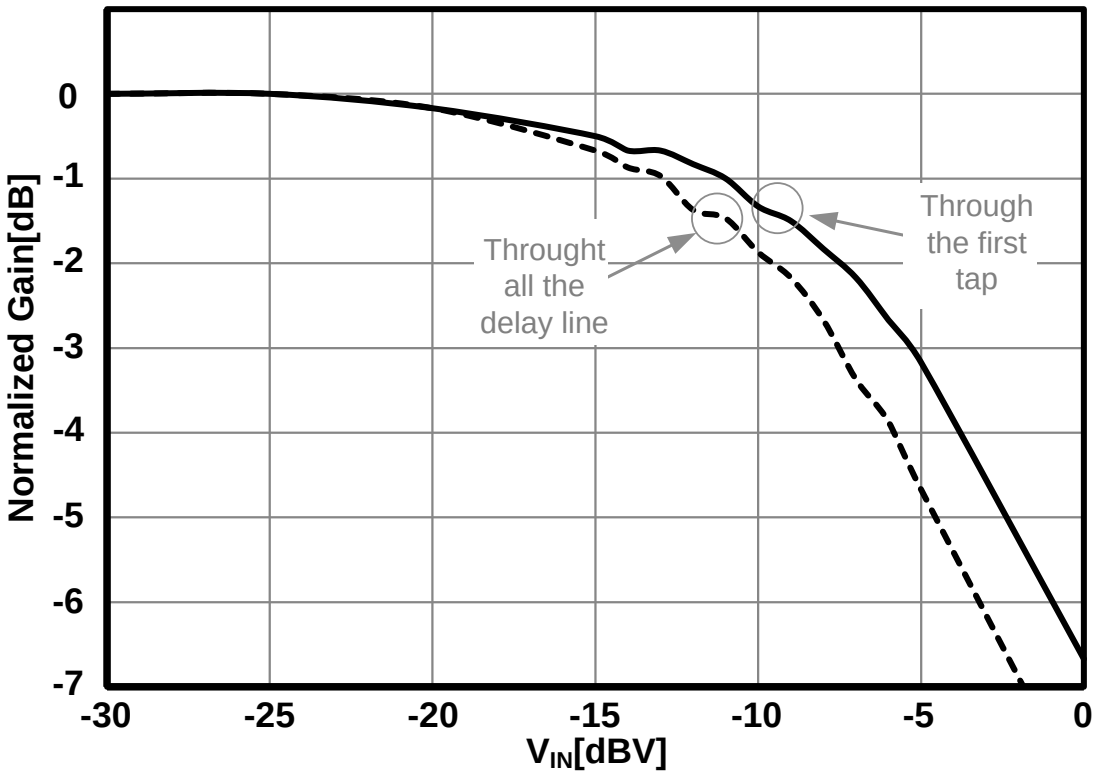


Figure 5.5: Normalized gain as a function of the input amplitude.

Delay line is one of the most important block in FIR. The delay and bandwidth determine the equalization performances. To test the response of a single delay cell, the transfer functions measured by activating one tap at a time have been recorded and then, to isolate the frequency response of the delay line from the response of the PCB, package, TIA and output buffer, the transfer function with the first tap active is subtracted from all the measurements (as showed in Fig. 5.6). The results are reported in Fig. 5.7 and Fig. 5.8, where the FIR equalizer is programmed for 25Gb/s and 10 Gb/s operation. Top and bottom plots are the magnitude and group delay of the transfer functions, respectively.

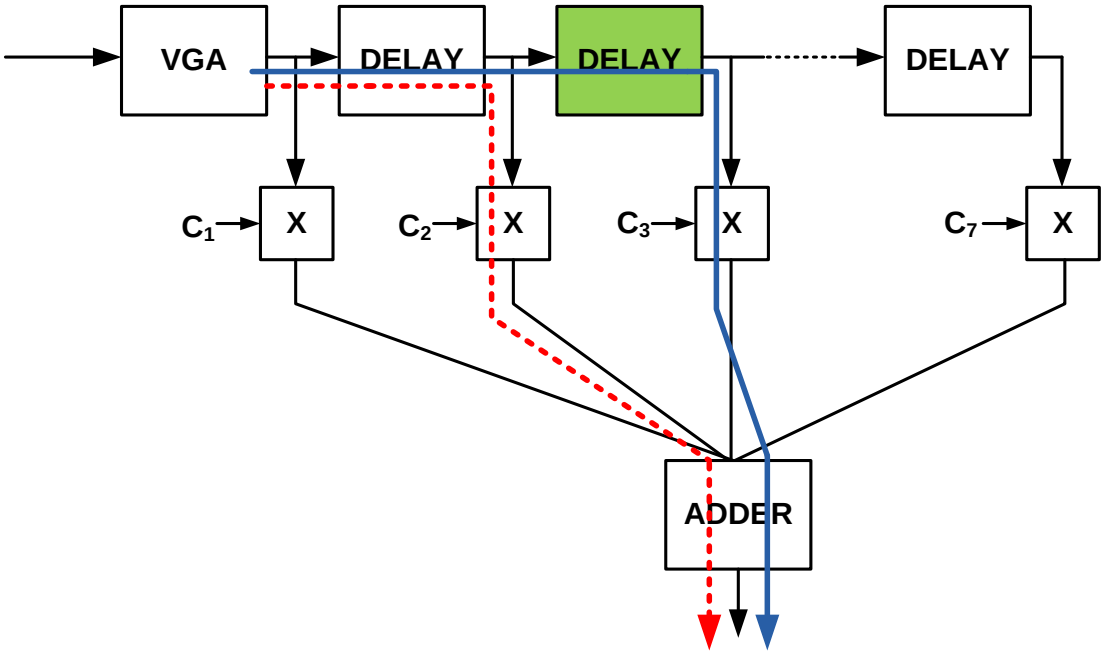


Figure 5.6: Methodology used to measure delay cell transfer function: difference between blue and red path.

The bandwidth of the tap-to-tap delay stage is 24.4GHz for 25Gb/s and 13.5GHz for 10Gb/s. As expected, bandwidth decreases by advancing through the delay elements, and for the complete delay line it is 13.2GHz at 25Gb/s, with 55mW power dissipation, and 5.5GHz at 10 Gb/s with power scaled to 35mW. Good matching is observed between the delay elements and tap amplifiers, being gain variation among all the curves within ±1.1dB. Also the tap-to-tap delays are well matched both for high and low data-rate, with low-frequency deviation within 10 % from the ideal spacing of 30ps and 75ps for 25Gb/s and 10Gb/s operation, respectively.

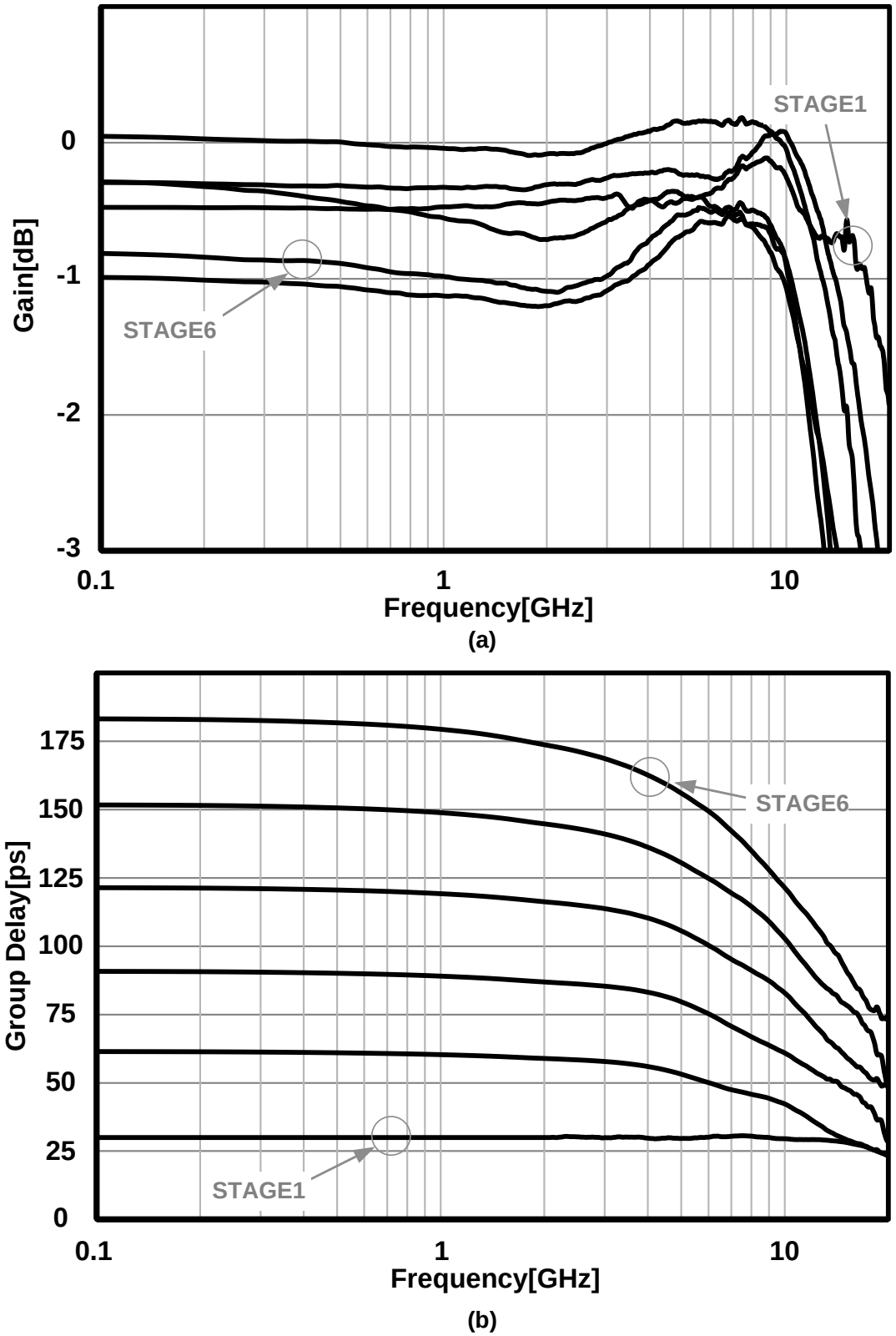


Figure 5.7: Magnitude and group delay of the transfer function from the input of the delay line to the output of each tap with the FIR equalizer programmed for 25Gb/s.

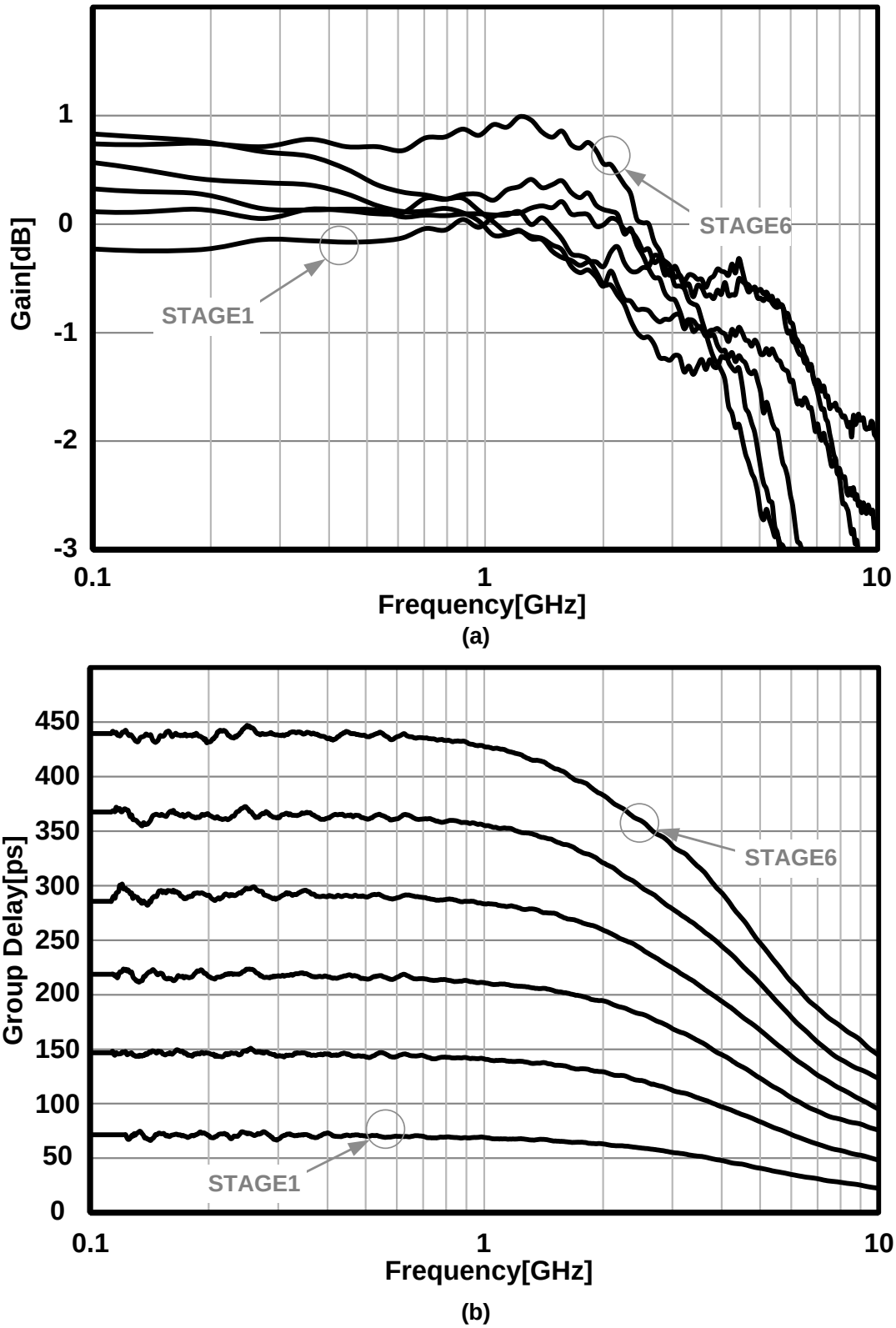


Figure 5.8: Magnitude and group delay of the transfer function from the input of the delay line to the output of each tap with the FIR equalizer programmed for 10Gb/s.

5.2 Eye diagrams

The equalization capability has been verified by using two FIR filters connected as depicted in the experimental setup shown in Fig. 5.9.

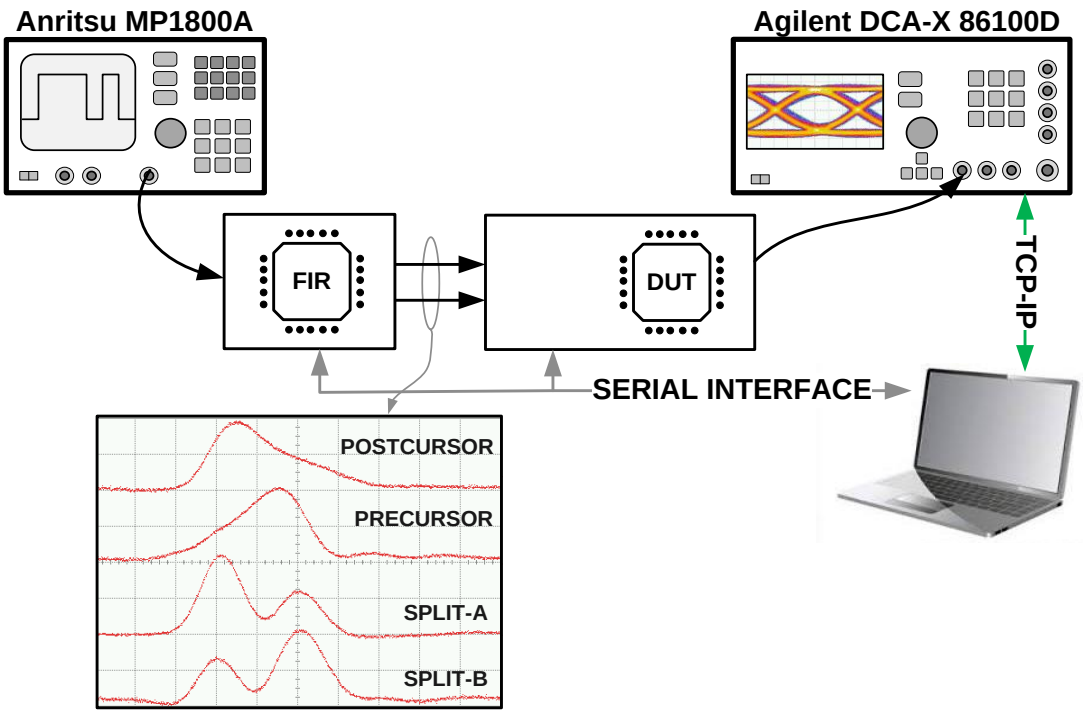


Figure 5.9: Measurement setup and emulated channel pulse responses for testing of the MMF link equalization capability.

A first FIR filter driven by a pattern generator is used to mimic the channel dispersion introduced by a multi-mode fiber. Examples of pulse responses are shown in the figure. A second chip (DUT) performs equalization.

Tests have been performed with pulses spread over 4-5 symbols, slightly more aggressive than the IEEE802.3aq pulses already showed in the first chapter. We considered also pulses having the energy concentrated on two different peaks, namely Split-A and Split-B, but the fully symmetric pulse is disregarded, being the DFE

fundamental for good eye opening. Fig. 5.10 shows measured eye diagrams at the input and output of the FIR equalizer at 25Gb/s. The amplitude of the input signal is $250mV_{pk-pk}$. The tap-to-tap delay is set to 30ps and core power dissipation is 90mW from 1V supply. Output eyes amplitude is ~100mV with pk-to-pk vertical and horizontal openings better than 43% and 57% respectively.

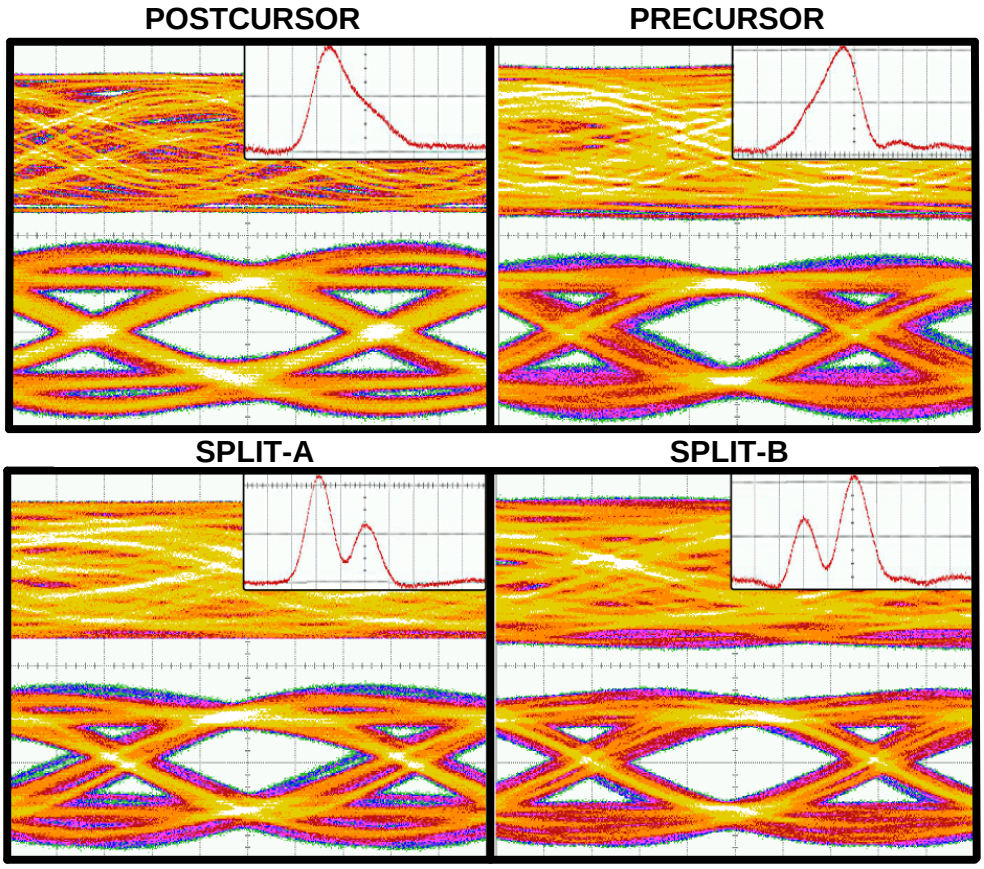


Figure 5.10: Eye diagrams at the output of the FIR equalizer with the channel pulse responses shown in Fig. 5.16, at 25 Gb/s (V. scale 40mV/div, H. scale 6.64ps/div).

The same tests have been performed at 10Gb/s with the power consumption of the filter scaled down to 55mW. As an example, equalization of channels with the "Postcursor" and "Split-A" pulse response are shown in Fig.5.11. Measurements with

T_d = 30ps and T_d raised to 75ps are compared. To keep the same eye amplitude on the scope, the gain of the output buffer is raised to 4-5dB when the smaller T_d is used. The higher T_d is therefore preferable, as expected from the discussion in Chapter 3, to limit the DC attenuation and SNR penalty introduced by the filter.

Interestingly, looking at the quality of the eye diagrams in Fig. 5.11, changing T_d has a different impact on the two channels. With the "Postcursor" channel, equalization performance is quite independent from T_d. But in "Split-A" case, raising T_d to the optimal value yields a remarkable benefit to the eye quality. The peak-to-peak horizontal eye opening increases from 48% to 69%, significantly improving the timing margin. The different impact of Td on the two channels can be qualitatively explained by looking at the channel FFTs, shown on the right plots in Fig.5.11. Despite the large attenuation at Nyquist, the "Postcursor" channel has a regular low-pass shape. This channel can be equalized with a simple high-pass response, easily implemented also without adjusting T_d. On the contrary, the "Split-A" channel has an in-band notch. Frequencies at which each tap of the FIR introduces boost or attenuation are inversely proportional to T_d, and setting a larger T_d shifts the full FIR equalizing capability to lower frequency allowing better inversion of channels with significant in-band distortion.

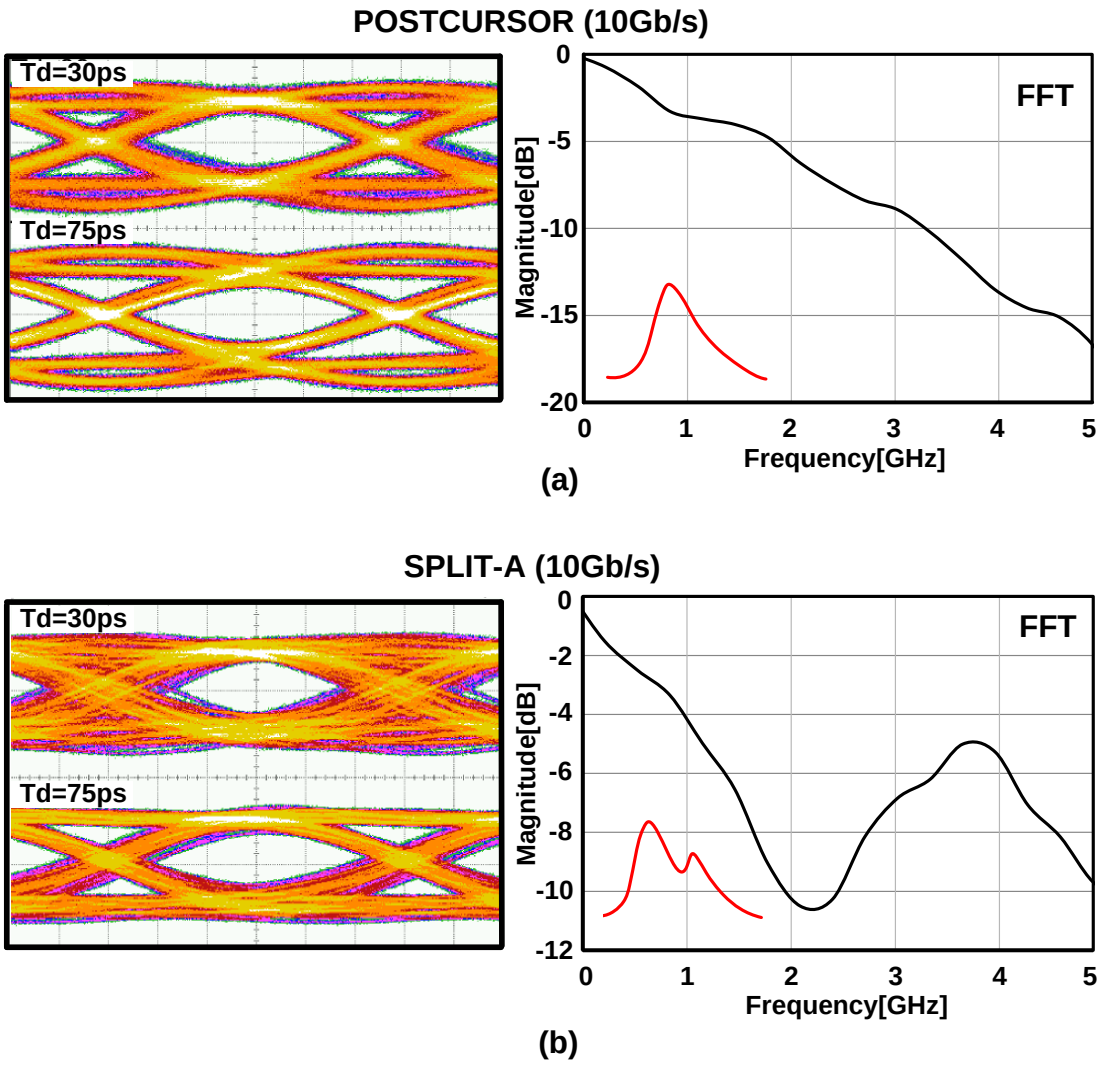


Figure 5.11: Equalization of two different channel responses at 10 Gb/s with Td=30ps and Td=75ps (V.scale 40mV/div, H.scale 16.6ps/div).

5.3 Measurements of the FIR cascaded with a Ser-Des

To evaluate the performances of FIR in a complete EDC system, some measurements are performed with a complete Ser-Des in cascade. Fig. 5.12 shows the experimental setup. The output of the FIR equalizer feeds a wireline receiver, realized by STMicroelectronics, which comprises a pre-emphasis filter, 3-tap DFE, CDR and on-chip eye monitor [54].

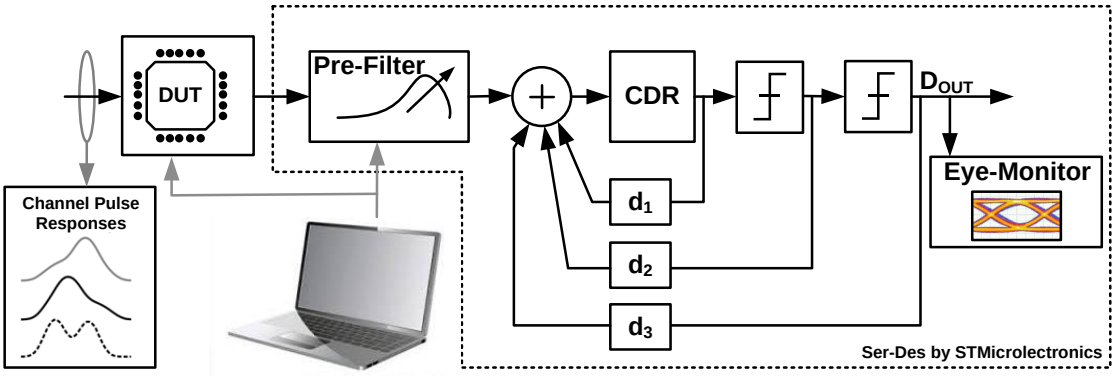


Figure 5.12: Measurement setup and emulated channel pulse responses for testing FFE with a complete Ser-Des.

Measurements were limited to a data-rate of 10Gb/s by the speed of the receiver. Channels with the pulse responses of Fig. 5.12 (the same provided by 802.3aq standard) have been tested and the plot in Fig.5.13 reports the measured bathtubs with PRBS7 sequences. The channel featuring a symmetric pulse response is mostly equalized by the DFE and the modest horizontal opening of 0.25 UI at BER=10^{-12} is attributed to the availability of a DFE with 3-taps only. On the contrary, in the cases of dispersion compensation of the pre- and post-cursor channels, the FIR equalizer plays a primary role and horizontal openings are improved to 0.45 UI and 0.44 UI respectively.

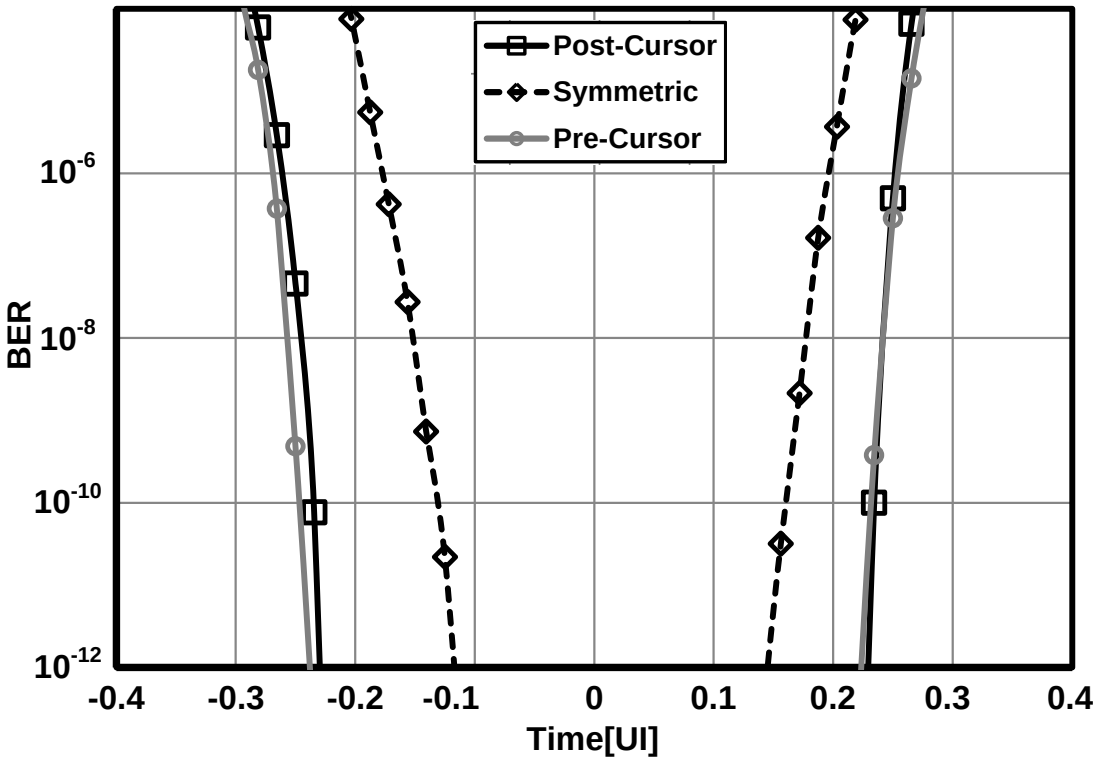


Figure 5.13: Measured bathtubs at 10Gb/s for channels with the pulse responses of standard 802.3aq.

Chapter6

Conclusions

An ultra-compact CMOS continuous-time 7-tap FIR equalizer for multi-mode fiber dispersion compensation up to 25 Gb/s has been presented. A system level analysis to derive equalizer specifications has been proposed with emphasis on the discussion of issues specifically related to continuous-time FIR filter implementations. The design of a test chip has been described with a detailed analysis of the delay line and gain stages. Realized in 28 nm LP CMOS technology, core silicon area is only 0.085 mm and comprehensive experimental results proved successful equalization from 10 Gb/s to 25 Gb/s with power dissipation ranging from 55 mW to 90 mW.

Measurements are summarized and compared with published FIR equalizers in Table II. The presented equalizer features a state-of-the-art power dissipation normalized to data-rate and total delay. The tunable active delay line leads to maximum flexibility allowing successful operation over the largest variation of the input data-rate with scalable dissipation. Compared with others 7-tap equalizers, core area is reduced. These features are particularly effective to accommodate the demand of variable transfer rates, back-compatibility and energy efficiency of emerging 400 Gb/s standards.

Ref	Tech.	Data Rate [Gb/s]	#Taps	Total Delay [ps]	Power [mW]	Power/(DataRate*Total Delay) [mW]	Core Area [mm^2]
[22]	180n SiGe	10	7	300	40	13.3	1.9
[25]	130n CMOS	10	7	450	325	72.2	3.8
[23]	90n CMOS	24-30	3	70	25	14.8-11.9	0.3
[24]	180n CMOS	30-40	3	50	70	46.6-35	0.45
[26]	65n CMOS	40	7	75	65	21.6	0.75
This work	**28n CMOS**	**10-25**	**7**	**450-180**	**55-90**	**12.2-20**	**0.085**

Table IV: FIR equalizer performance summary and comparison with the state of the art.

References

[1] www.statista.com

[2] www.cisco.com

[3] S. Sakr, A. Liu, D. Batista, and M. Alomari, "A Survey of Large Scale Data Management Approaches in Cloud Environments," *IEEE Commun.Surveys & Tutorials*, vol. 13, no. 3, pp. 311–336, Jul. 2011

[4] G. Schulz, *The Green and Virtual Data Center*, 1st ed. Boston, MA, USA: Auerbach Publications, 2009.

[5] L. Schares, D. M. Kuchta, and A. F. Benner, "Optics in future data center networks," in Symposium on High-Performance Interconnects, 2010, pp.104–108.

[6] P. Pepeljugoski, J. Kash, F. Doany, D. Kuchta, L. Schares, C. Schow, M. Taubenblatt, B. J. Offrein, and A. Benner, "Low Power and High Density Optical Interconnects for Future Supercomputers," in Optical Fiber Communication Conference and Exhibit, OthX2, 2010.

[7] *Make IT Green: Cloud Computing and its Contribution to Climate Change*. Greenpeace International, 2010.

[8] http://www.greendataproject.org

[9] C. F. Lam, H. Liu, B. Koley, X. Zhao, V. Kamalov, and V. Gill, "Fiber optic communication technologies: what's needed for datacenter network operations," IEEE Commun. Mag., vol. 48, pp. 32–39, July 2010.

[10] M. Glick, “Optical interconnects in next generation data centers: An end to end view,” in Proc. 2008 16th IEEE Symposium on High Performance Interconnects, 2008, pp. 178–181.

[11] C. Minkenberg, “The rise of the interconnects,” in *HiPEAC Interconnects cluster meeting, Barcelona*, 2010.

[12] A. Davis, “Photonics and Future Datacenter Networks,” in *HOT Chips, A Symposium on High Performance Chips, Stanford*, 2010.

[13] IEEE Std 802.3aq-2006. “Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications”

[14] R. E. Freund, C.-A. Bunge, N. N. Ledentsov, D. Molin, Ch. Caspar, “High-Speed Transmission in Multimode Fibers,” *IEEE J. of Lightwave Technology*, vol. 28, no. 4, pp.569-586, Feb 2010.

[15] http://www.ieee802.org/3/aq/public/upload/OM1and22IPRMeasurements1-5-05.pdf

[16] O. E. Agazzi, M. R. Hueda, D. E. Crivelli, H. S. Carrer, A. Nazemi, G. Luna, F. Ramos, R. López, C. Grace, B. Kobeissy, C. Abidin, M. Kazemi, M. Kargar, C. Marquez, S. Ramprasad, F. Bollo, V. Posse, S. Wang, G. Asmanis, G. Eaton, N. Swenson, T. Lindsay, P. Voois, “A 90-nm CMOS DSP MLSD transceiver with integrated AFE for electronic dispersion compensation of multimode optical fibers at 10 Gb/s,” *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 2939–2957, Apr. 2008.

[17] J. Cao, B. Zhang, U. Singh, D. Cui, A. Vasani, A. Garg, W. Zhang, N. Kocaman, D. Pi, B. Raghavan, H. Pan, I. Fujimori, A. Momtaz, "500 mW ADC-Based CMOS AFE With Digital Calibration for 10 Gb/s Serial Links Over KR-Backplane and Multimode Fiber," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1172–1185, June 2010.

[18] B. Zhang, A. Nazemi, A. Garg, N. Kocaman, M. R. Ahmadi, M. Khanpour, H. Zhang, J. Cao, A. Momtaz, "A 195mW / 55mW Dual-Path Receiver AFE for Multistandard 8.5-to-11.5 Gb/s Serial Links in 40-nm CMOS," *in IEEE ISSCC Dig. Tech. Papers*, 2013, pp. 34-35.

[19] J. F. Bulzacchelli, C. Menolfi, T. J. Beukema, D. W. Storaska, J. Hertle, D. R. Hanson, P.-H. Hsieh, S. V. Rylov, D. Furrer, D. Gardellini, A. Prati, T. Morf, V. Sharma, R. Kelkar, H. A. Ainspan, W. R. Kelly, L. R. Chieco, G. A. Ritter, J. A. Sorice, J. D. Garlett, R. Callan, M. Brändli, P. Buchmann, M. Kossel, T. Toifl, D. J. Friedman, "A 28-Gb/s 4-Tap FFE/15-Tap DFE Serial Link Transceiver in 32-nm SOI CMOS Technology," *IEEE J. of Solid State Circuits*, vol. 47, no. 12, pp. 3232-3248, Dec. 2012.

[20] H. Kimura, P. Aziz, T. Jing, A. Sinha, R. Narayan, H. Gao, P. Jing, G. Hom, A. Liang, E. Zhang, A. Kadkol, R. Kothari, G. Chan, Y. Sun, B. Ge, J. Zeng, K. Ling, M. Wang, A. Malipatil, S. Kotagiri, L. Li, C. Abel, F. Zhong, "28Gb/s 560mW Multi-Standard SerDes with Single-Stage Analog Front-End and 14-Tap Decision-Feedback Equalizer in 28nm CMOS", *in IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 38-39.

[21] A. Agrawal, J. F. Bulzacchelli, T. O. Dickson, Y. Liu, J. A. Tierno, D. J. Friedman, "A 19-Gb/s Serial Link Receiver With Both 4-Tap FFE and 5-Tap DFE Functions in 45-nm SOI CMOS", *IEEE J. of Solid State Circuits*, vol. 47, no. 12, pp. 3220-3231, Dec. 2012.

[22] H. Wu, J. A. Tierno, P. Pepeljugoski, J. Schaub, S. Gowda, J. A. Kash, A.Hajimiri, "Integrated transversal equalizers in high-speed fiber-optic systems," *IEEE J. of Solid State Circuits*, vol. 38, no. 12, pp. 2131-2137, Dec. 2003.

[23] J. Sewter and A. C. Carusone, "A CMOS Finite Impulse Response Filter With a Crossover Traveling Wave Topology for Equalization up to 30 Gb/s," *IEEE J. of Solid State Circuits*, vol. 41, no. 4, pp. 909-917, April 2006.

[24] J. Sewter and A. C. Carusone, "A 3-Tap FIR Filter With Cascaded Distributed Tap Amplifiers for Equalization Up to 40Gb/s in 0.18μm CMOS," *IEEE J. of Solid State Circuits*, vol. 41, no. 8, pp. 1919-1929, August 2006.

[25] S. Reynolds, P. Pepeljugoski, J. Schaub, J. Tiemo, and D. Beisser, "A 7-Tap Transverse Analog-FIR Filter in 0.13μm CMOS for Equalization of 10Gb/s Fiber-Optic Data Systems," *in IEEE ISSCC Dig. Tech. Papers*, 2005, pp. 330-331.

[26] A. Momtaz and M. M. Green, "An 80 mW 40 Gb/s 7-Tap T/2-Spaced Feed-Forward Equalizer in 65 nm CMOS," *IEEE J. of Solid State Circuits*, vol. 45, no. 3, pp. 629-639, March 2010.

[27] A.J. Baker, "An adaptive cable equalizer for serial digital video rates to 400Mb/s," *Int. Solid-State Circuits Conference, Digest of Technical Papers*, pp. 174-175, Feb. 1996.

[28] J. N. Babanezhad, "A 3.3V analog adaptive line-equalizer for fast Ethernet data communication," *Proc. Custom Integrated Circuits Conference*, pp. 343-346, May 1998.

[29] G. Zhang, *et al.*, "A 10Gb/s BiCMOS adaptive equalizer," *Int. Solid-State Circuits Conference, Digest of Technical Papers*, pp. 748-749, Feb. 2004.

[30] S. Gondi, *et al.*, "A 10Gb/s CMOS adaptive equalizer for backplane applications," *Int. Solid-State Circuits Conference, Digest of Technical Papers*, pp. 328-329, Feb. 2005.

[31] P. P. Monteiro, *et al.*, "40Gb/s GaAs MMIC signal processor for optical communication systems," *GaAs Applications Symp.*, Sept. 2001.

[32] M. Nakamura, *et al.*, "Electrical PMD equalizer ICs for a 40Gb/s transmission," *Optical Fiber Communication Conference, Technical Digest OFC/NFOEC*, TuG4, Apr. 2004.

[33] H. Wu, *et al.*, "Integrated transversal equalizers in high-speed fiber-optic systems," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2131-2137, Dec. 2003.

[34] H. Jiang, *et al.*, "SiGe equalizer IC for PMD mitigation and signal optimization of 40Gbits/s transmission," *Optical Fiber Communication Conference, Technical Digest OFC/NFOEC,* OWO2, Apr. 2005.

[35] J. Proakis, *Digital Communications*. New York: McGraw-Hill, 1995.

[36] L. Moller, *et al*., "ISI mitigation using decision feedback loop demonstrated with PMD distorted 10 Gbit/s signals," *Electron. Letters,* vol. 35, no. 24, 25, pp. 2092-2093, Nov. 1999.

[37] A. Momtaz, *et al*., "Fully Integrated 10Gb/s Receiver with Adaptive Optical Dispersion Equalizer in 0.13μm CMOS," *IEEE J. Solid-State Circuits,* vol. 42, no. 4, pp. 872-880, April 2007.

[38] G.D. Forney Jr., "Maximum-likelihood sequence estimation of digital sequences in the presence of intersymbol interference," *IEEE Trans. Inform. Theory,* vol. IT-18, no. 3, pp. 363-378, May 1972.

[39] A. Weiss, "On the performance of electrical equalization in optical fiber transmission systems," *IEEE Photonics Technology Letters,* vol. 15, no. 9, pp. 1225-1227, Sept. 2003.

[40] H. Bae, *et al*., "An MLSE receiver for electronic dispersion compensation of OC-192 fiber links," *IEEE J. Solid-State Circuits,* vol. 41, no. 11, pp. 2541-2554, Nov. 2006.

[41] E. A. Lee and D. G. Messerchmitt, *Digital Communications*, 2nd edition, pp. 532-543, Norwell, MA: Kluwer, 1993.

[42] E. Eweda, "Analysis and design of a signed regressor LMS algorithm for stationary and nonstationary adaptive filtering with correlated Gaussian data," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 1367-1374, Nov. 1990.

[43] R. Gitlin and S. Weinstein, "Fractionally-spaced equalization: An improved digital transversal equalizer," *Bell Syst. Tech. J.*, vol. 60, no. 2, pp. 275–296, Feb. 1981.

[44] S. Qureshi, "Adaptive equalization," *Proc. IEEE*, vol. 73, no. 9, pp. 1349–1387, Sep. 1985.

[45] Q. Yu, and A. Shanbhag, "Electronic Data Processing for Error and Dispersion Compensation," *IEEE J. of Lightwave Technology*, vol.24 no.12, pp. 4514-4525, Dec 2006.

[46] H. Liu, J. Liu, R. Payne, C. Cantrell, M. Morgan, "A 18mW 10Gbps Continuous-Time FIR Equalizer for Wired Line Data Communications in 0.12μm CMOS," in *Proc. IEEE CICC*, 2009, pp. 113-116.

[47] M. Maeng, F. Bien, Y. Hur, H. Kim, S. Chandramouli, E. Gebara, J. Laskar, "0.18-□m CMOS Equalization Techniques for 10-Gb/s Fiber Optical Communication Links," *IEEE Trans. On Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3509-3519, Nov. 2005.

[48] S. Reynolds, *et al*., "A 7-Tap transverse analog-FIR filter in 0.13µm CMOS for equalization of 10Gb/s fiber-optic data systems," *IEEE Int. Solid-State Circuits Conference, Digest of Technical Papers*, pp. 330-331, 2005.

[49] J. Sewter, *et al.*, "A 3-tap FIR filter with cascaded distributed tap amplifiers for equalization up to 40Gb/s in 0.18um CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1919-1929, Aug. 2006.

[50] A. Momtaz and M. M. Green, "An 80 mW 40 Gb/s 7-Tap T/2-Spaced Feed-Forward Equalizer in 65 nm CMOS," *IEEE J. of Solid State Circuits*, vol. 45, no. 3, pp. 629-639, March 2010.

[51] D. H. Garduno, J. S. Martinez, "A CMOS 1Gb/s 5-Tap Transversal Equalizer Based on lnductorless 3rd-Order Delay Cells", *in IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 232-233.

[52] D.Li, G. Minoia, M. Repossi, D. Baldi, E. Temporiti, A.Mazzanti, and F. Svelto, "A Low-Noise Design Technique for High-Speed CMOS Optical Receivers", *IEEE J. of Solid State Circuits*, vol. 49, no. 6, pp. 1437-1447, June 2014.

[53] E. Sackinger "Broadband Circuits for Optical Fiber Communications", Chapter 5, Wiley, 2005.

[54] M. Pozzoni, S. Erba, P. Viola, M. Pisati, E. Depaoli, D. Sanzogni, R. Brama, D. Baldi, M. Repossi, F. Svelto, "A Multi-Standard 1.5 to 10 Gb/s Latch-Based 3-Tap DFE Receiver With a SSC Tolerant CDR for Serial Backplane Communication," *IEEE J. of Solid State Circuits*, vol. 44, no. 4, pp. 1306-1315, Apr. 2009.

Appendix

Low Phase Noise MM-Wave VCO with Inductor Splitting for Tuning-Range Extensions

As 40 Gb/s optical communication systems enter the commercial stage, the transceiver chipset requires lower power dissipation, lower costs, and a wide frequency range to meet the requirements of several standards, such as OC-768/STM-256 (39.8 Gb/s), OTU-3 (43.0 Gb/s), and LANPHY (44.6 Gb/s). Generation of the clock signals requires high spectral purity oscillators with a center frequency near 40GHz and wide tuning range to cover different standards and compensate processing variation [1]. VCOs based on LC resonators are commonly adopted. The LC tank Q is limited by capacitors, at mm-waves, preventing better performances just due to scaling. Design of VCOs in this band is further penalized by trade-off between phase noise and frequency tuning range, as confirmed by experimental results reported in the literature, and summarized in figure A.1. Tuning range encompasses a rapid degradation, as frequency increases.

A new topology of LC VCO, based on inductor splitting, is proposed in this chapter [2]. The proposed circuit technique enables low noise over a very wide tuning range. Realized prototypes prove the following performances: an oscillation frequency tunable between 33.6 and 46.2GHz corresponding to a 31.6% total tuning range, a power dissipation of 9.8mW, phase noise at 10MHz offset ranging between -

115 and -118dBc/Hz with a $1/f^3$ corner of 800 kHz, and a resulting Figure Of Merit (FoM) between 175 and 180dBc/Hz meeting the requirements for 40Gb/s optical standards.

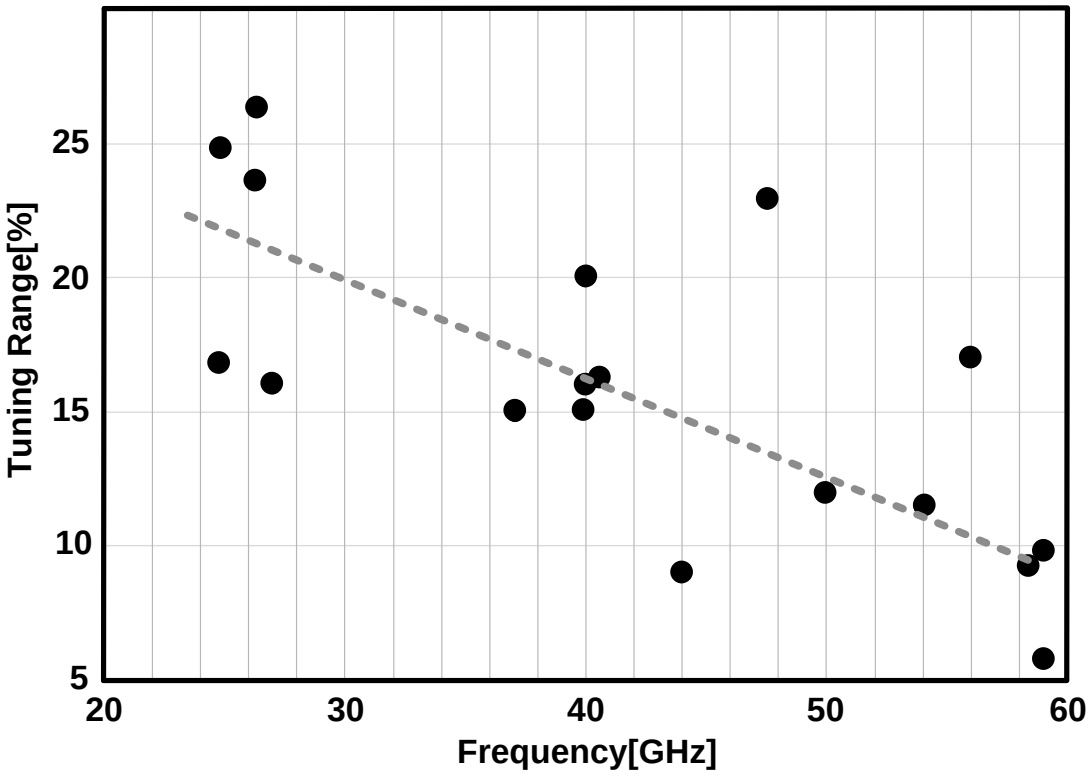


Figure A.1: Tuning range vs. center frequency of recently reported mmWave CMOS oscillators.

A.1 Switched LC-resonator with wide tuning range

Figure A.2 shows a simplified equivalent circuit of an oscillator with the traditional tank with switched capacitor C_T and the proposed alternative made of a switch in series with inductor L_T.

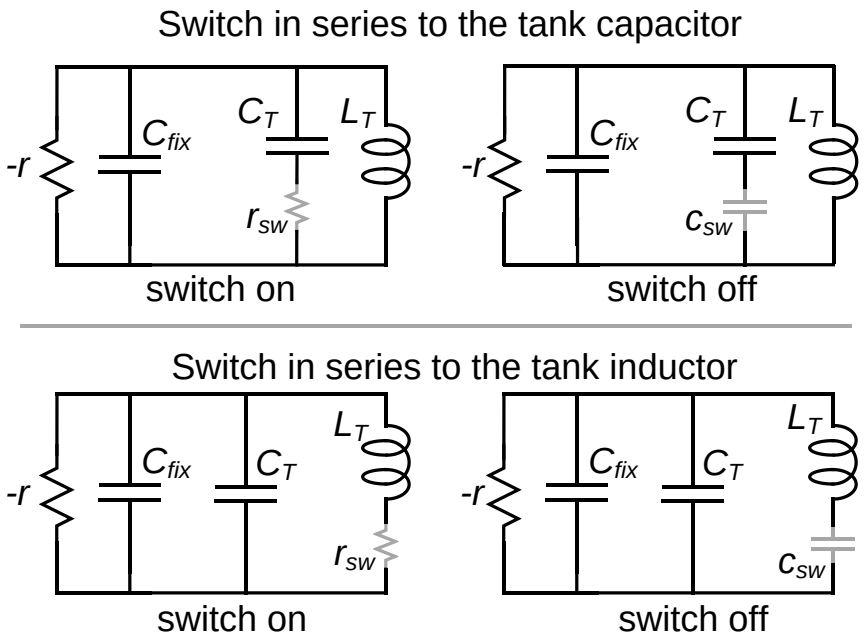


Figure A.2: Simplified equivalent circuit of an LC-tank oscillator with a switch in series to the capacitor and inductor.

The negative resistance models the active devices while C_{FIX}, comparable or even larger than C_T at mm-Waves, represents the fixed capacitance loading the tank, introduced primarily by parasitics of the negative resistance and buffer. When the switch is on, the two tanks have the same resonance frequency equal to $1/(2\pi(L_T(C_{FIX}+C_T))1/2)$ but when the switch is off, the behavior of the two circuits is

remarkably different. The oscillation frequency f_0 for the top-right circuit in figure A.2 is:

$$f_0 = \frac{1}{2\pi\sqrt{L_T\left(C_{FIX} + \frac{C_T C_{OFF}}{C_T + C_{OFF}}\right)}} \qquad \text{(A.1)}$$

If the parasitic capacitance of the switch is negligible compared with C_T and C_{FIX}, (i.e. $C_{OFF} << C_T, C_{FIX}$) the oscillation frequency simplifies to $f_0 \approx \frac{1}{2\pi\sqrt{L_T C_{fix}}}$, i.e. C_{FIX} sets an upper bound to the maximum frequency step.

In the bottom-right circuit of Figure 6.2, C_{OFF} appears in series with C_T+C_{FIX} instead of C_T only, determining a larger variation of the equivalent tank capacitance and removing the limitation introduced by C_{FIX} on the maximum oscillation frequency, given by:

$$f_0 = \frac{1}{2\pi\sqrt{L_T\left(\frac{(C_T + C_{FIX})C_{OFF}}{C_T + C_{FIX} + C_{OFF}}\right)}} \qquad \text{(A.2)}$$

which, in the limit case of C_{OFF} much lower than C_{FIX} and C_T, simplifies to $f_0 \approx \frac{1}{2\pi\sqrt{L_T C_{off}}}$.. Looked at in an alternative way, for the same relative frequency step, the switch in series with L_T can assume a much higher C_{OFF}. It can be therefore realized with a larger transistor leading to a lower R_{ON} and less penalty to the tank quality factor. As a numerical example, assuming typical values of L_T = 100pH, C_T ~ C_{FIX} = 100fF, the resonance frequency with the switches closed is 35.6GHz. A fractional frequency step of 20% sets C_{OFF} = 50fF in the switched capacitor while

allowing C_{OFF} = 400fF when the switch is in series with the inductor. With C_{OFF} = 1.27fF/μm and R_{ON} = 432Ω·μm measured for the 32nm CMOS technology, the on resistance of the switch comes out to be 11Ω and 1.37Ω for the switched capacitor and inductor, respectively. With lossless reactive components, the tank quality factor would be 8.1 and 16.3 respectively, thus showing a remarkable advantage. Simulation results taking into account losses of the tank components are shown in Figure A.3. The plot compares the minimum Q of the traditional tank and the proposed solution at different tuning steps for a center frequency of 40GHz. For f_{MAX}/f_{MIN} = 1.2, connection of the switch in series with the inductor improves the tank Q by 50%, from 3 to 4.5. Simulations reveal advantage increases further when targeting a larger tuning step.

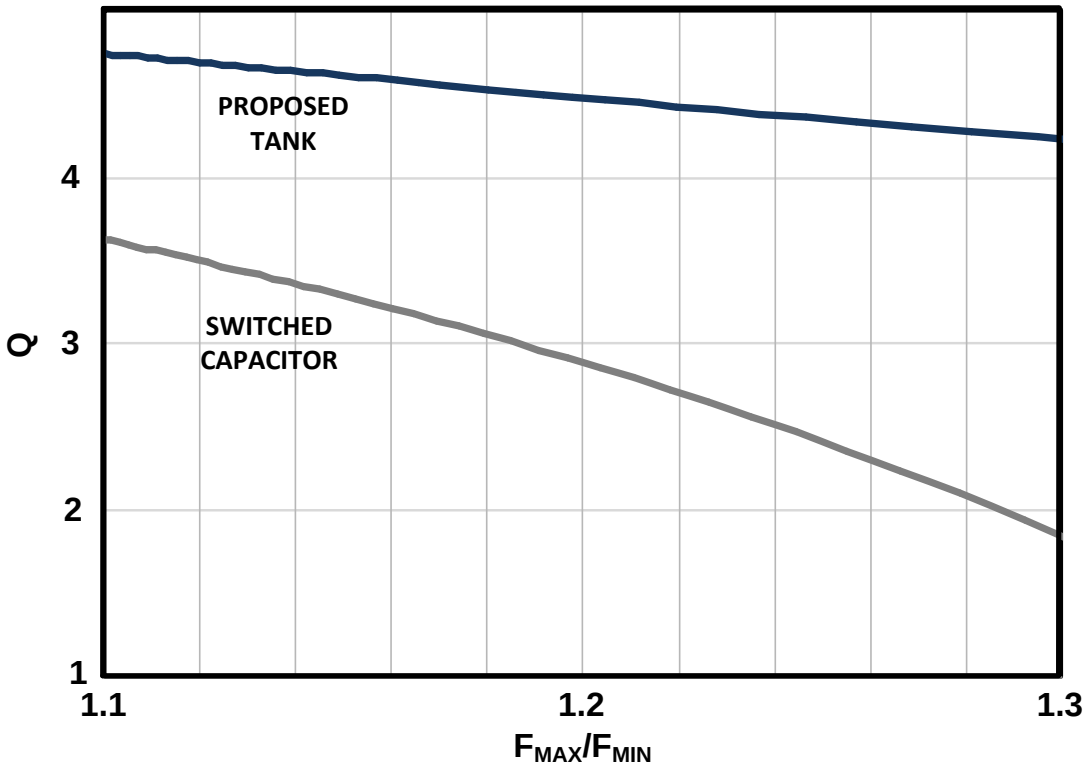


Figure A.3: Simulated minimum Q at 40GHz versus the tuning step for the traditional and proposed tank.

A.2 Circuit design

A wide tuning range VCO based on the proposed LC-tank has been designed in 32nm CMOS technology. The center frequency is 40GHz targeting high-speed Gb/s wireless communications at V-band with a sliding-IF receiver architecture [3]. Tuning range in excess of 20% is required to cover 57GHz to 66GHz bandwidth with margin against process variations and poor device and parasitic modeling. The schematic of the VCO is shown in figure A.4.

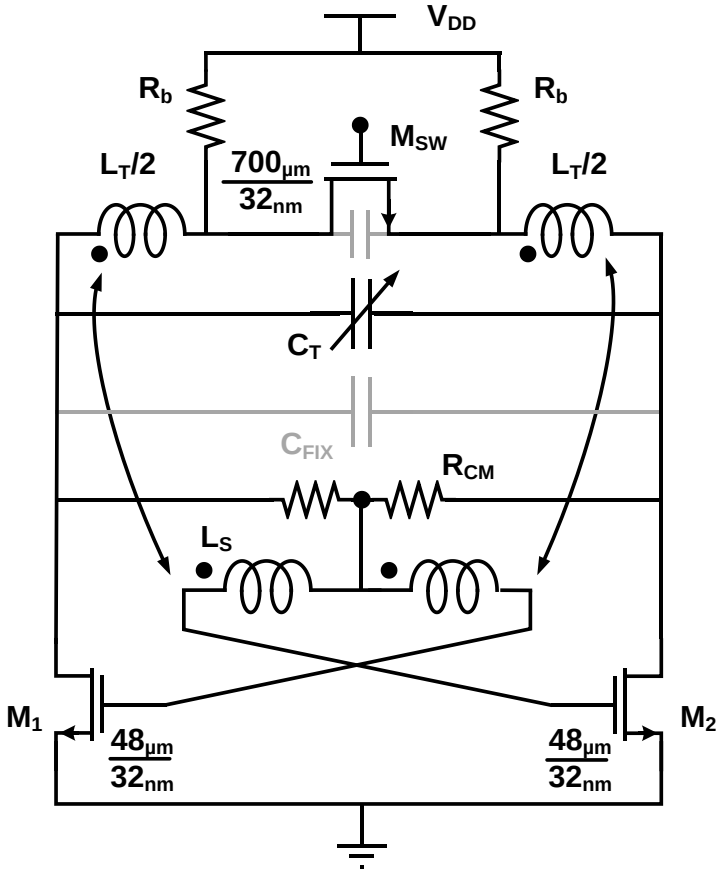


Figure A.4: Schematic of the proposed VCO.

Inductor L_T with capacitors C_T and C_{FIX} realizes the resonator. Transistor M_{SW} splits the inductor and, by exploiting its parasitic capacitance in off-state, allows a coarse

tuning-step dividing the total oscillator tuning range in two main sub-bands. Finer tuning is implemented by realizing C_T with a bank of three binary-sized switched MOM capacitors and a small varactor. Being M_{SW} very large, the on resistance has a negligible impact on the overall tank quality factor which varies from 4 to 5.5 in the tuning range. Transistors M_1-M_2, with a current consumption regulated by the two top biasing resistors R_b, compensate resonator losses. The feedback from the tank to the gate terminals of M_1-M_2 is implemented through the secondary coil of a transformer L_S, and the gate biasing is provided by resistors R_{CM} connected to the center tap of L_S. Feedback via the transformer is required to prevent the circuit from latching when M_{sw} is off. It also leads to larger loop gain. To gain insight, figure A.5 shows the simplified equivalent circuit of the oscillator with M_{SW} on and off.

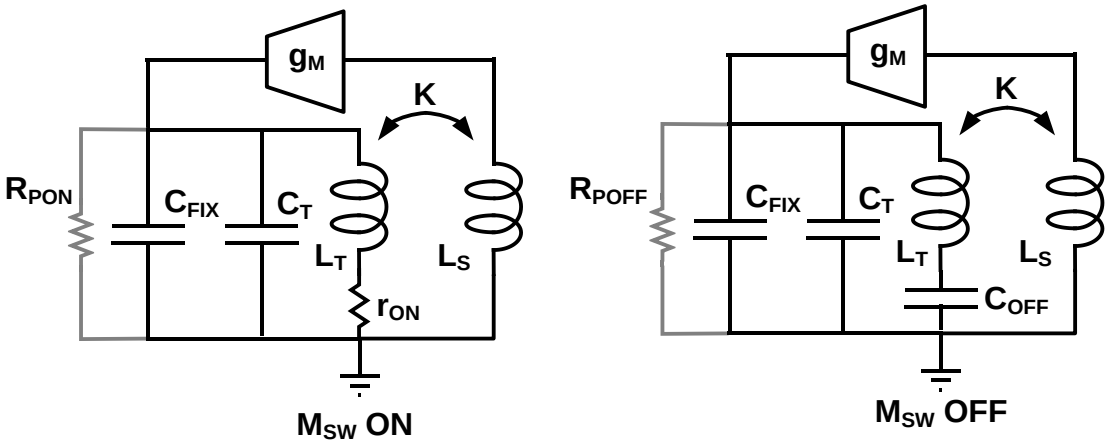


Figure A.5: Equivalent circuits of the oscillator in the two main sub-bands.

In the lower sub-band, with M_{SW} on, the tank impedance at resonance frequency f_{low} is $R_{PON} = 2\pi f_{low} L_T Q$ and the loop gain is :

$$G_{LOOP} = k\sqrt{\frac{L_S}{L_T}} g_m 2\pi f_0 L_T Q \qquad \text{(A.3)}$$

Looking now at the right circuit in figure A.5, which represents the oscillator with M_{SW} off, the tank impedance is infinite at DC. The transformer suppresses the loop gain at DC and avoids the circuit from latching. At resonance frequency f_{hi}, the tank impedance is given by:

$$R_{POFF} = 2\pi f_{HI} L_T Q \alpha^2 \quad \text{with} \quad \alpha = \frac{C_{OFF}}{C_T + C_{FIX} + C_{OFF}} \tag{A.4}$$

The capacitive divider drastically limits the impedance at the drain of the transistors (α^2 = 0.35 – 0.45). The transformer thus helps raising the loop gain, otherwise requiring a prohibitively high g_m. By inspection of the right circuit in fig. A.5 the loop gain is given by:

$$G_{LOOP} = k\sqrt{\frac{L_S}{L_T}}\alpha g_m 2\pi f_0 L_T Q \tag{A.5}$$

In the realized VCO the estimated impedance magnitude of the tank ranges from 80Ω to 105Ω. The transformer has been designed with a primary inductor L_T of 100pH and secondary L_S of 120pH. Magnetic coupling k is 0.75. Core active devices M_1-M_2 in figure 16 are 48μm wide over minimum channel leading to a transconductance of 25mS which ensures a loop gain larger than 1.7.

A.3 Measurements

Test chips have been realized by STMicroelectronics in CMOS32nm-LP technology. For characterization the VCO drives a buffer, realized with an open-drain differential pair, and a frequency divider-by-four [4](Fig.A.6). Both the signal at mm-Waves and a replica scaled in frequency are thus available. A micrograph of the test chip is shown in Fig.A.7.

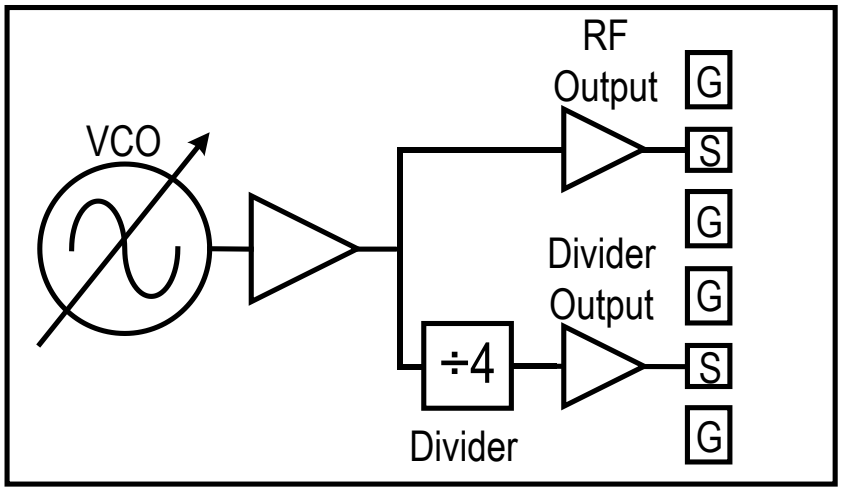


Figure A.6: Setup measurement of VCO.

The oscillation frequency is tunable from 33.6GHz to 40.8GHz with M_{SW} on and from 38.8GHz to 46.2GHz with M_{SW} off, corresponding to 31.6% total tuning range. The wide overlapping of 2GHz between the two bands is more than expected. An accurate redesign reducing overlap to a minimum would allow a tuning range of 35%. The power dissipation is 9.8mW from a 1V supply. The phase noise has been measured after the frequency divider and reported to the carrier frequency assuming negligible noise introduced by the divider. Figure A.8 shows a typical plot, for a

carrier frequency of 40GHz. The phase noise at 10MHz offset is -118dBc/Hz with a $1/f^3$ corner frequency of ~800kHz. Phase noise at 10MHz offset and the FOM versus the oscillation frequency are shown in Figure A.9. The phase noise ranges from -115.2dBc/Hz to -118dBc/Hz with a corresponding FOM from 177.5 to 180dBc/Hz.

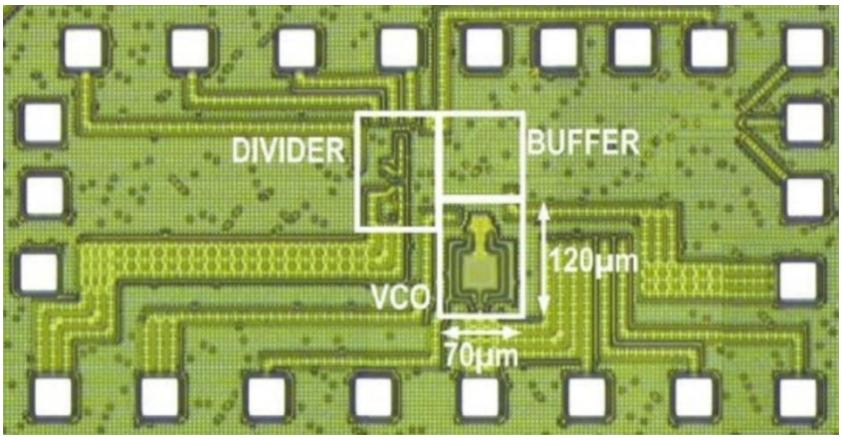


Figure A.7: Die microphotograph of the realized VCO.

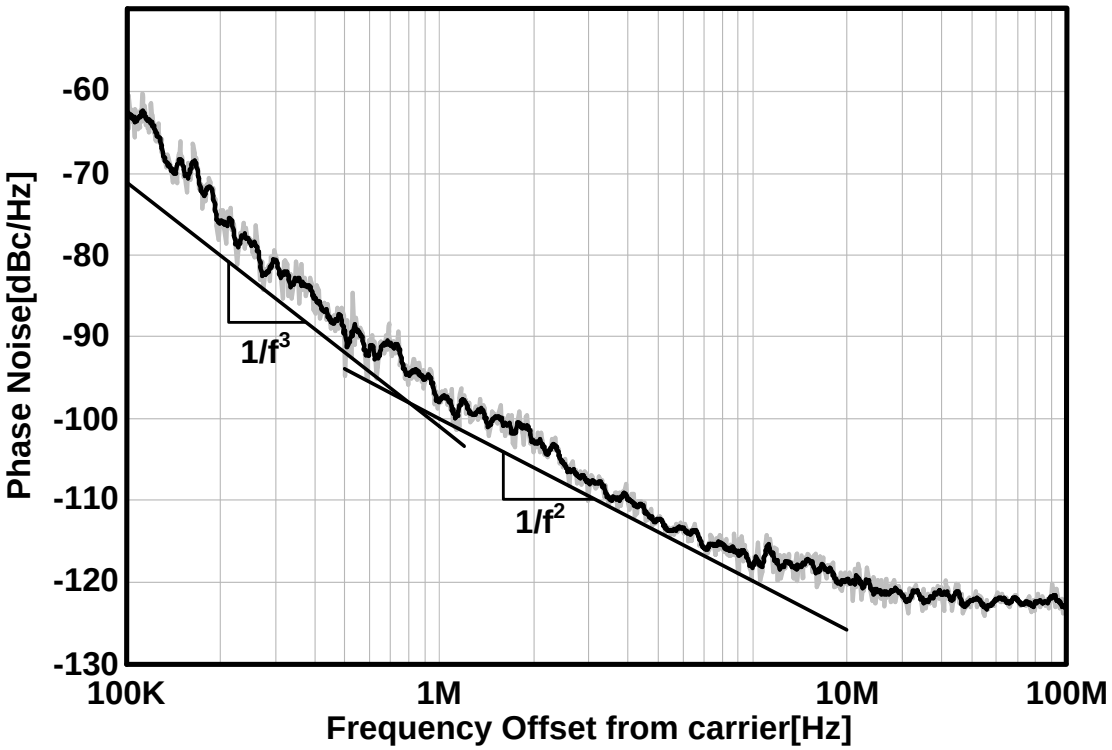


Figure A.8: Measured phase noise for the VCO oscillating at 40GHz.

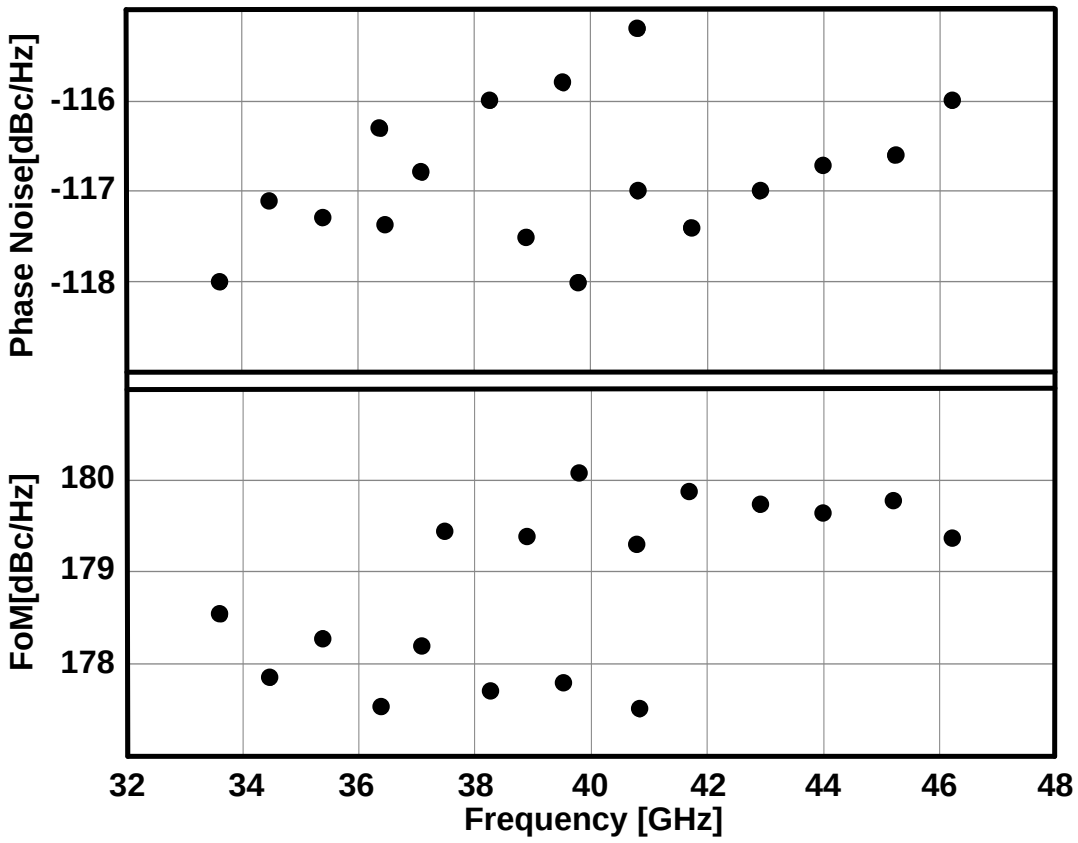


Figure A.9: Phase noise and FoM of the VCO versus frequency.

Experimental results are summarized and compared to recently reported mm-Wave VCOs in Table V. VCOs exploiting transformer tuning [58,59] achieve record tuning ranges, much more than typically required, at the cost of a severe in-band phase noise penalty, as evidenced by the very low minimum FOM. The proposed VCO has a state-of-the-art FOM, despite being realized in an ultra-scaled 32nm node, comparable with traditional switched capacitors or varactor solutions [60,61].

Ref	Freq (GHz)	T.R. (%)	P_{diss} (mW)	PN@10MHz (dBm/Hz)	FoM (dBc/Hz)	Tech CMOS
[5]	57.5 / 90.1	44.2	8.4 / 10.8	-104.6 / -112.2	172 / 180	65nm
[6]	11.5 / 22	59	20 / 29	-107 / -127	158.6 / 177	130nm
[7]	34.3 / 39.9	15.0	14.4	-118 / -121	178.4 / 180	65nm
[8]	43.2 / 51.8	22.9	16.0	-117 / -119	179 / 180	65nm
[9]	21.7 / 27.8	24.8	12.2	-121	177.5	45nm
This work	**33.6 / 46.2**	**31.6**	**9.8**	**-115.2 / -118.0**	**177.5 / 180**	**32nm**

Table V: VCO performance summary and comparison with the state of the art.

References

[1] K.Watanabe, *et al.*, “A Low-Jitter 16:1 MUX and a High- Sensitivity 1:16 DEMUX with Integrated 39.8 to 43 GHz VCO forOC-768 communication systems,” in Proc. IEEE Solid-State Circuit Conf. Dig. Tech. Papers, Feb. 2004, pp. 166–167.

[2] Mammei, E.; Monaco, E.; Mazzanti, A.; Svelto, F., "A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz minimum noise FOM using inductor splitting for tuning extension," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International , vol., no., pp.350,351, 17-21 Feb. 2013.

[3] Vecchi, F.; Bozzola, S.; Temporiti, E.; Guermandi, D.; Pozzoni, M.; Repossi, M.; Cusmai, M.; Decanis, U.; Mazzanti, A.; Svelto, F., "A Wideband Receiver for Multi-Gbit/s Communications in 65 nm CMOS," Solid-State Circuits, IEEE Journal of , vol.46, no.3, pp.551,561, March 2011.

[4] Ghilioni, A.; Mazzanti, A.; Svelto, F., "Analysis and Design of mm-Wave Frequency Dividers Based on Dynamic Latches With Load Modulation," Solid-State Circuits, IEEE Journal of , vol.48, no.8, pp.1842,1850, Aug. 2013

[5] Jun Yin; Luong, H.C., "A 57.5-to-90.1GHz magnetically-tuned multi-mode CMOS VCO," Custom Integrated Circuits Conference (CICC), 2012 IEEE , vol., no., pp.1,4, 9-12 Sept. 2012.

[6] S.Saberi,J.Paramesh:“A 11.5-22GHz Dual-Resonance Transformer-coupled quadrature VCO,” in Proc. RFIC Conf. 2011, June 5–6,2011, pp. 1–4.

[7] Nariman, M.; Rofougaran, R.; De Flaviis, F., "A switched-capacitor mm-wave VCO in 65 nm digital CMOS," Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE , vol., no., pp.157,160, 23-25 May 2010.

[8] Murphy, D.; Gu, Q.J.; Yi-Cheng Wu; Heng-Yu Jian; Xu, Z.; Tang, A.; Wang, F.; Chang, M.-C.F., "A Low Phase Noise, Wideband and Compact CMOS PLL for Use in a Heterodyne 802.15.3c Transceiver," Solid-State Circuits, IEEE Journal of , vol.46, no.7, pp.1606,1617, July 2011.

[9] Osorio, *et al.*, "A 21.7-to-27.8GHz 2.6-degrees-rms 40Mw frequency synthesizer in 45nm CMOS for mm-Wave communication applications," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International , vol., no., pp.278,280, 20-24 Feb. 2011.