Universitá degli Studi di Pavia

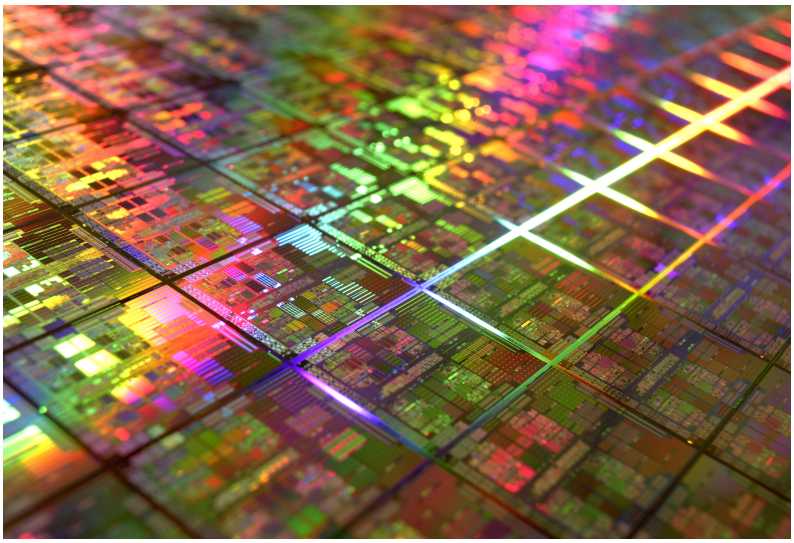
Facoltá di Ingegneria

Dottorato di Ricerca in Microelettronica

XXV ciclo

Building Blocks for mm-wave Phased-Array Receivers in CMOS Technology

Anna Moroni



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dissertation submitted by

Anna Moroni

to obtain the degree of

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Your work is going to fill
a large part of your life,
and the only way to be
truly satisfied is to do
what you believe is great work.
And the only way to do great work
is to love what you do.
If you haven't found it yet,
keep looking.
Don't settle.
As with all matters of the heart,
you'll know when you find it.
And like any great relationship,
it just gets better and better
as the years roll on.
So keep looking until you find it.
Don't settle.

Steve Jobs

Contents

Introduction

Millimeter wave technology for the 60 GHz band is one of the most exciting opportunities for circuit, antenna and communication system engineers over the next decade. 60 GHz is, in fact, the beginning of a trend of escalating carrier frequencies that will deliver unprecedented data rates, several tens of gigabits per second, allowing uncompressed high-definition media transfers, sensing and radar applications, and virtually instantaneous access to massive libraries of information [1]. In 2001 the Federal Communication Commission (FCC) has made available a 7 GHz "unlicensed" band between 57 and 64 GHz for wireless communications and many research institutions and companies have begun to study new mm-wave wireless systems. 60 GHz wireless communications allow high data rates (up to 6 Gbps), higher integration levels, strong levels of frequency reuse and enhanced safety due to the strong amount of atmosphere's absorption at these frequencies. These features make this band suitable for a variety of applications such as high speed WLANs, wireless short-range systems for inter-vehicle and roadside to vehicle communications (IVC and RVC), broadband services distribution (ITS's), optical fiber extension and LAN bridges.

The present thesis in particular addresses multi-Giga data-rates WLAN applications, that is high-speed internet access, wireless high speed file transfers, uncompressed exchange of information between TV, cameras, DVD and other appliances. The design of mm-wave systems for high speed WLAN presents many design challenges, mainly related to the high operative frequencies, close to the cut-off frequency of the last technologies' transistors. A design approach based on different levels is

fundamentally: device, building blocks circuital topology and transceiver architecture have to be studied in parallel. Moreover, in order to fully account for the behavior of active and passive devices up to 60 GHz, it is necessary to design, model and characterize these devices (mos, varactors, inductors, capacitors and transmission lines). A careful optimization of the layout is also of primary importance to achieve good performances and represents an important part of the project. Around 60 GHz the design of any building block in the RF receiving chain pose many design challenges. The poor quality factors of passive elements limit the performances of the active devices and the difficulty in accurately modeling all the physical phenomena that affect their behavior, such as substrate coupling and skin effect, makes it extremely hard to predict the actual circuit performances. Millimeter-wave passive models for CMOS components are not readily available; therefore, extensive electromagnetic simulations must be performed on each single device. It should be emphasized that accurate electromagnetic simulations on complex structures often require too high computational tasks necessitating some layout simplifications to be completed. Also distributed effect must be taken into account: any interconnection within the circuit which is an appreciable size of a wavelength should be treated as a transmission line and accurately modeled. Transmission lines, therefore, become very important elements in the entire millimeter-wave portion of the radio, as they are widely used as both interconnects and to realize passive components, as an alternative to lumped inductors. Electromagnetic simulations and direct on-chip characterizations of active and passive devices have been carried out to accurately model all devices.

Some of the mm-wave issues, such as limited achievable gain, high noise figure and the strong sensitivity to device modeling, could be partly relaxed adopting a phased array based approach. Integration of a complete phased array system in silicon results in substantial improvements in cost, size and reliability providing opportunities to perform on-chip signal processing and conditioning. At the circuits level, the division of the signal into multiple parallel paths relaxes the power handling and noise requirements for each individual active device. In all phased array architectures, except the RF recombination one, LO distribution represents a difficult task, and, if a direct-conversion topology is chosen, also the I/Q LO generation becomes challenging. Quadrature LO generation typically degrades the generation

system performances considerably if classical coupled-oscillators are exploited and the I/Q outputs of the coupled-VCOs must travel large distances to reach every single mixer in the array, which gives significant losses and mismatches. In my research activity, these issues have been overcome by combining the LO generation and distribution tasks through the use of a spatially distributed oscillator. I/Q LO signals have to be generated and be directly available at the spatially separated I/O LO ports of each direct down-conversion mixer without the need for a lossy distribution network.

As concerning the RF signal path, the antenna interface of receivers remains very hard to tune. Ideally, the antenna interface of an RF receiver should match the impedance of the antenna so as to extract the maximum possible wanted (in-band) signal power from the antenna and prevent reflections, amplify the wanted signal with low noise, and reject unwanted (out-of-band) interferers. However, in the current literature, achieving these goals over wide mm-wave tuning range has proven challenging. A solutions for receivers capable of capturing several widely spaced bands can be a wideband receiver with only moderate rejection of interference at many bands. To this purpose, in my research activity a broadband matching down-conversion mixer will be presented. Furthermore, in principle, a homodyne (direct conversion) receiver does not require any RF components but a mixer and local oscillator in order to work, and indeed early receivers included only these components [2]. This simple approach has recently garnered more attention, as recent works suggest that connecting the antenna directly to a CMOS passive mixer without an RF LNA can provide significant benefits, such as extremely low power [3]or greatly increased tuning range and linearity [4], [5].

In this thesis a phased-array direct-conversion distributed receiver prototype in a standard 65nm CMOS technology, adopting the baseband recombination approach, is presented. It is composed by four coupled distributed wave oscillators connected to broadband passive down-conversion mixers. This architecture aims at minimizing the power consumptions due to LO signal distribution, given a wide matching bandwidth at the RF input signal.

Chapter I reviews the main characteristics of millimeter-waves propagation, the main application fields and the emerging standards for mm-wave wireless communications. The motivation and the architecture of the phased-array receiver prototype

structure are discussed.

Chapter II deals with the broadband passive down-conversion mixer design. In the first part the input wideband matching network implementation is discussed and in the second part the mixer performances, as input impedance,gain and noise factor, are evaluated. Then the mixer core design will be presented and the experimental results will be reported, showing a broad matching bandwidth from 51 to over 67 GHz.

In **Chapter III** the phased-array concept and the advantages and drawbacks of the various phased-array architectural approaches are presented and the LO distribution problem is then discussed. The second part of the chapter focuses on the description of the proposed LO generation and distribution system. The implemented oscillator is presented, which is defined "hybrid" wave oscillator (HWO), because it is composed coupling a rotary and two standing wave oscillators (RWO and SWO). The method to couple two standalone HWOs will be explained and the 4-coupled HWOs array structure will be shown. Then a phase noise analysis of SWO, RWO, HWO and 4-coupled HWOs array will be discussed. Finally the HWOs array design will be presented and the experimental results will be reported, conforming the phase noise theory analysis.

The conclusions summarize the major contributions of this thesis and suggest topics which deserve further work.

Chapter 1

Millimeter Wave Receivers

The constant scaling of CMOS technology has resulted in CMOS devices becoming fast enough for millimeter wave operations and enabling the realization of low cost 60 GHz transceivers. Despite the large number of CMOS circuits and solutions that have been published over the past few years, some issues still hamper the optimal design of a complete mm-wave CMOS transceiver. The principal design issues are low transmission power and high noise figure; another one is given by the limited RF bandwidth. Furthermore, the high free-space path loss and the poor quality of CMOS technology at high frequencie results in the need for directional communication, which can be implemented using programmable phased-array multiple-antenna systems. [28]

In section I the characteristics of 60 GHz wireless transmissions will be presented: in particular, the emerging standards and regulations in different countries will be discussed and section II will describe the most important challenges of millimeter wave design, given by limitations of the CMOS technologies. In section III the possible alternative phased array architectures for the realization of a 60 GHz front-end will be shown with their advantages and limitations. Also a possible solution to avoid the local oscillator distribution issue in phased array configuration will be proposed. In particular a broadband distributed mm-wave receiver will be presented, composed by a distributed coupled oscillators array connected to broadband matched passive mixers, which will be described in detail in the next two chapters.

1.1 60 GHz standards

Already in 2001 [10], the Federal Communication Commission (FCC) has made available a 7GHz "unlicensed" band between 57 and 64 GHz for wireless communications, and many research institutions and companies have begun to study new mm-wave wireless systems. The mm-wave PHY operating frequency is within the 57-66 GHz range as allocated by the regulatory agencies in Europe, Japan, Canada, and the United States. This band will also be available in other areas where allocated by the regulatory bodies. The regulatory 60 GHz bands vary slightly from country to country, but have a large overlap as shown in Fig. 1.1 [11].

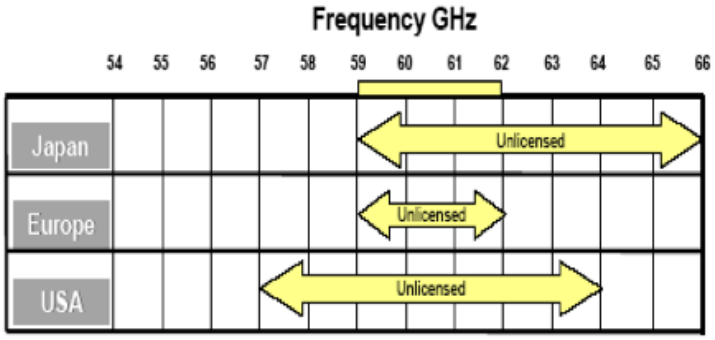

Figure 1.1: Worldwide unlicensed 60 GHz bands.

The new WLAN based on the mm-wave transmission [12] offer these and other services (HDTV, home theater etc. ..) at even higher data transfer rates up to 2Gb/s; they also allow high coexistence with all other microwave systems included in 802.15 family.

There are many standardization and commercialization efforts currently underway by the engineering community for 60-GHz WPAN. Current technical standards activities include IEEE 802.15.3c, WirelessHD, IEEE 802.11ad, the WiGig standard, and ECMA 387 [1]. All of these standards target short range 60-GHz networks and they are shown in Table 1.1

WirelessHD is an industry-led effort to define a next generation wireless high-definition interface specification for consumer electronics products. The consortium has completed the WirelessHD specification version in May 2010.

Ecma International TC48 is also developing a standard for 60 GHz technology for very high data-rate short range unlicensed communications to support bulk data

Name	**Forum Type**	**Status**	**Maximum Data Rate** (Gbps)	**Applications**
Wireless HD	Industry Consortium	Spec. 1.0, Jan 2008	4 (OFDM)	Uncompressed HD video
ECMA 387	International Standard	Draft 1.0, Dec 2008	4.032 (OFDM) 6.35 (SC)	Bulk data transfer and HD streaming
802.15.3c	International Standard	Released October 2009	5.7 (OFDM) 5.2 (SC)	Portable point-to-point file transfer and streaming
802.15.3ad	International Standard	Target completion Dec. 2012	>1	Rapid up-download, wireless display, distribution of HDTV
WiGig	Industry Consortium	Released May 2010	7	File transfer, wireless display and docking, streaming high definition

Table 1.1: Comparison of major 60 GHz standards that are under development.

transfer such as downloading data from a kiosk and high definition multimedia streaming. It has completed ECMA-387 specification in December 2008. ECMA-387 uses distributed MAC based on MBOA-MAC from WiMedia.

Wireless Gigabit Alliance (WiGig) is yet another effort to standardize 60 GHz technology. The goal is to provide a single technology that can support instantaneous file transfers, wireless display and docking, and streaming high definition media on a variety of devices.

In addition, the IEEE 802.11 Very High Throughput (VHT) Study Group is actively studying 60 GHz solution for future WPAN standards. In December 2008, Task Group TGad is approved as a result of the work pursued by VHT Study Group. TGad will define enhancement to the IEEE 802.11 standard for 60 GHz band. While **IEEE 802.15.3c** is targeting WPAN, one of the distinct goals of IEEE 802.11 TGad is to maintain WLAN experience such as a larger coverage and backward compatibility to 802.11.

1.2 Millimeter wave circuit design challenges

The 60 GHz band, extending over several gigahertz of unlicensed bandwidth, is attractive for short range high speed communications all over the world. However, the design of mm-wave wireless transceivers presents many design challenges, mainly because of the high operative frequencies, close to the cut-off frequency f_t of the transistors, and because of the low analog qualities of over-scaled MOS transistors. A design approach based on different levels is of primary importance: devices, building blocks circuital topology and transceiver architectures have to be studied in parallel. The devices and the interconnects tying them to one another entail issues that become only more serious as the frequency of operation enters the mm-wave range and also the devices models provided by the technology have been evaluated until 20 GHz. In order to fully account for the behavior of active and passive devices up to 60 GHz we have properly designed and modeled MOS transistors, varactors, inductors, capacitors and transmission lines, using electromagnetic simulations (EM) with the software *Agilent Momentum* (*ads*).

- **Inductors**

  The inductors have been realized as planar spirals, as reported in Fig. 1.2, where the "ring" number can be changed, depending on the layout area which can be occupied and on the inductance value. For example, in 65 nm TSMC

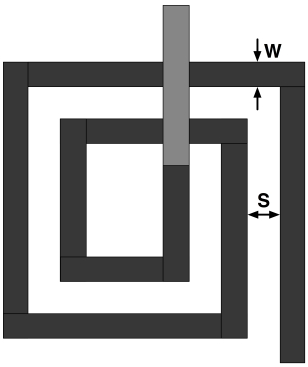

Figure 1.2: Example of planar spiral inductors.

CMOS technology, the quality factor Q of a spiral inductor with 2 loops, designed using the top metal, can vary from 8 to 13. In Fig. 1.3 the quality factor is reported as a function of inductance value, thus as a function of the loop length, where the W and S remained constant: in particular $W = 4\mu m$ and $S = 2\mu m$.

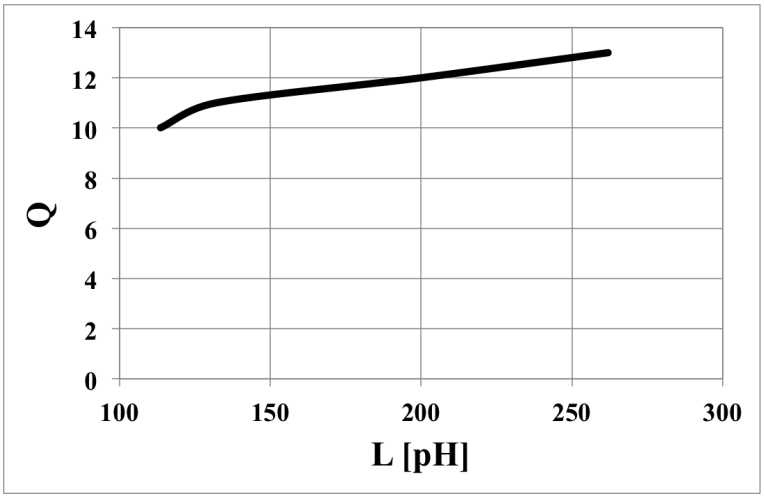

Figure 1.3: Quality factor as a function of the inductance value.

- **Transmission Lines**

  Transmission lines play many roles: they transport signals between structures, perform impedance matching, and are at times the best means of creating inductive or capacitive elements, especially when lumped components are impractical or too lossy to fabricate in the semiconductor process due to parasitic lead inductances or poorly defined current return paths [19]. An ideal T-line is inherently scalable in length and it is fully characterized by characteristic impedance Z_0 and the electric length e°.

  The two primary forms of transmission lines used for 60 GHz structures include microstrip transmission lines and coplanar waveguide transmission lines [20]. Microstrip designs offer higher capacitive quality factors (defined as the ratio of electric energy stored to energy lost per cycle) than coplanar lines due to the placement of their ground shield above the substrate [20]. Coplanar designs offer higher inductive quality factors (defined as the ratio of magnetic energy stored to energy lost per cycle) than microstrip designs [20], [21]. In millimeter wave often, as in our design, the importance of inductive components makes coplanar transmission lines preferable to microstrip ones. The primary challenge of passive component design is selecting the correct topology and dimensions for each component to avoid excessive losses. For a differential

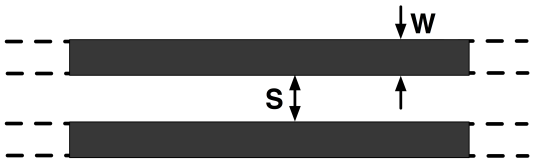

Figure 1.4: Overhead view of an integrated coplanar line.

T-line (Fig. 1.4), the line parameters can be extracted from the simulated S-parameters as obtained by the EM solver *Agilent Momentum*. By recalling that the ABCD representation of a transmission line with propagation constant γ and characteristic impedance Z_0 is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh\gamma\, l & Z_0 \sinh\gamma\, l \\ \dfrac{Z_0 \sinh\gamma\, l}{Z_0} & \cosh\gamma\, l \end{bmatrix}, \tag{1.1}$$

the parameters of interest (i.e. odd mode propagation constant, differential impedance and multi-section differential RLGC parameters per unit-length) can be calculated as [14]:

$$
\begin{aligned}
e^{\circ} &= \beta\, l, && (1.2)\\
\gamma &= \frac{1}{l}\ln\left(A+\sqrt{A^2-1}\right), && (1.3)\\
Z_0 &= \sqrt{\frac{B}{C}}, \qquad [\Omega] && (1.4)\\
\alpha &= \mathrm{Re}[\gamma], \qquad [Neper/m] && (1.5)\\
\beta &= \mathrm{Im}[\gamma], \qquad [Radian/m] && (1.6)\\
R &= \mathrm{Re}[\gamma\, Z], \qquad [\Omega/m] && (1.7)\\
L &= \frac{\mathrm{Im}[\gamma\, Z]}{2\pi\, f}, \qquad [H/m] && (1.8)\\
G &= \mathrm{Re}[\gamma/Z], \qquad [S/m] && (1.9)\\
C &= \frac{Im[\gamma\, Z]}{2\pi\, f}. \qquad [F/m] && (1.10)
\end{aligned}
$$

The transformation from S to ABCD parameters has been done using standard textbook formulas. The R,L,G and C values extracted can be used to build the familiar multi-sectional equivalent model, in order to use the line even in time domain circuit simulations (Fig. 1.5). The quality factor of the CPS

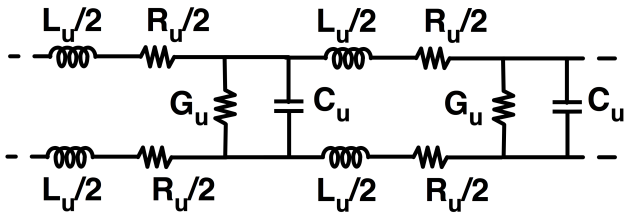

Figure 1.5: Differential RLCG model of the coplanar strip-line.

has been improved by shielding the transmission line by means of floating metal strips located underneath the guiding structure realized on the lowest metal layer M1 [15] (Fig. 1.6). The distance between two consecutive bars has been set to 1 μm in order to minimize the field penetration. Shielding the resonator from the underlying substrate has two beneficial effects. Primarily, the shunt losses are virtually eliminated, thus enhancing the quality factor

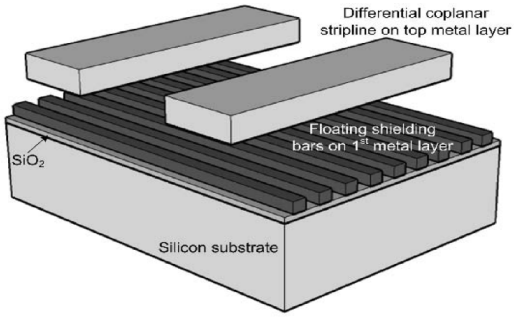

Figure 1.6: Shielded CPS principle.

of the transmission line. Secondly, the effective zero potential plane causes the separation of the electric and magnetic energies that results in slow-wave propagation [16]. This is because, while the magnetic fields permeate the entire substrate, the electric fields are virtually stopped at the floating bars boundary, therefore the transmission line inherits a capacitance in accordance with the small distance between the trace and the bar. The complete penetration of magnetic fields implies that the inductance is not expected to change while the shunt capacitance is increased resulting in a reduced velocity of signal propagation. The reduction of the signal velocity makes it possible to achieve the same phase shift of an unshielded structure but with a reduced line length.

To find the optimal topology for the CPS, the metal width (W) and separation (S) are swept between 2 μm and 32 μm and 4 μm and 38 μm, respectively. The line length is kept constant and equal to 100 μm. The results of Momentum simulations are given in Fig. 1.7 and Fig. 1.8. The highest quality factor ($\approx$30) is achieved with a line width of 24 μm and a conductors spacing of 34 μm. Q improves with a shielded structure and this can be explained by inspecting the values of the RLGC lumped model, in particular the shunt loss element G_p. In an unshielded structure, the presence of the semi-conductive substrate makes large stripes correspond to large values of G_p. For those structure, the electric quality factor is much lower than the magnetic one so that the overall Q is low.

The models shown in this section are only the starting point to the design of the chip layout, because the parasitics elements due to the interconnections play a

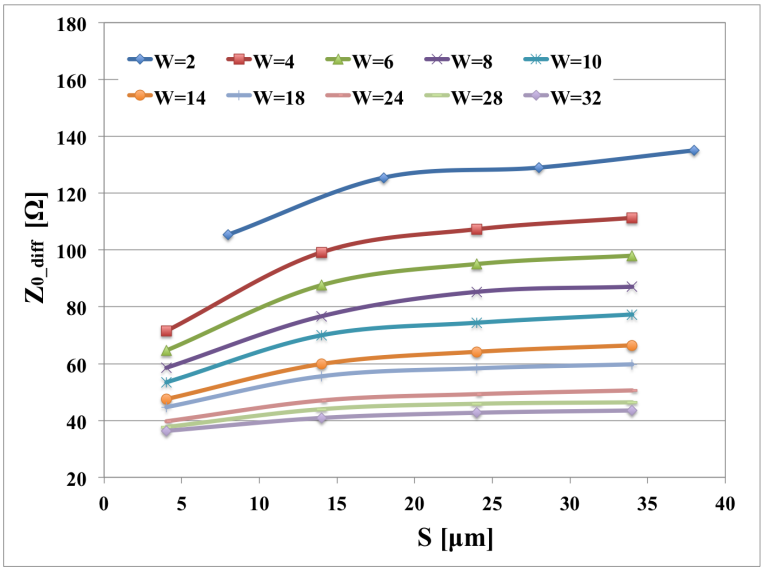

Figure 1.7: Differential characteristic impedance of a transmission line.

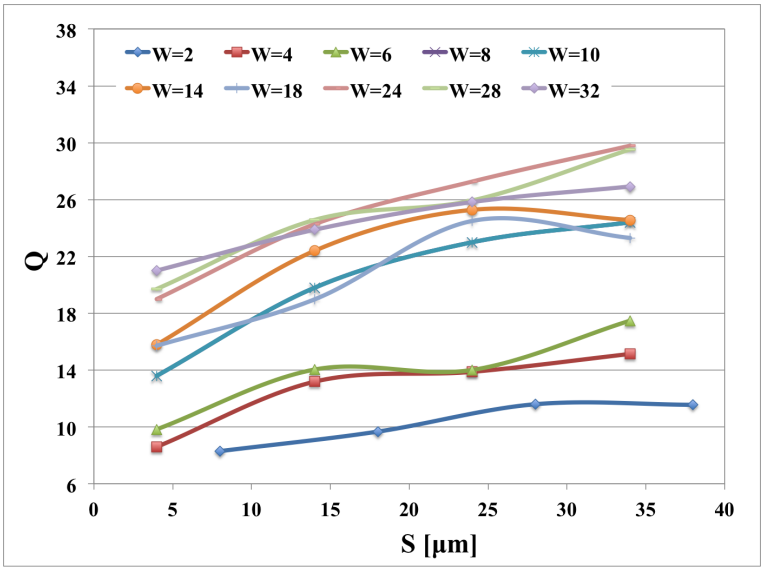

Figure 1.8: Quality factor of a transmission line.

fundamentally role. Each part of the designed layout must be modeled with EM simulation, to evaluate the parasitics elements and their impact on the circuit design and, if it is necessary, the layout must be re-designed to reduce the losses. The chip area surrounding inductors and t-lines has been properly prefilled with dummies to reach the local density requirements and dummies effect has been verified through EM simulations (Fig. 1.9). Some simplifications on complex layout structures and on the actual metal prefillers pattern have proven necessary. A careful optimization of the layout has been carried out both for the passive mixer and HWO implementations, particularly aimed at minimizing the parasitics losses due to the layout design, as interconnections.

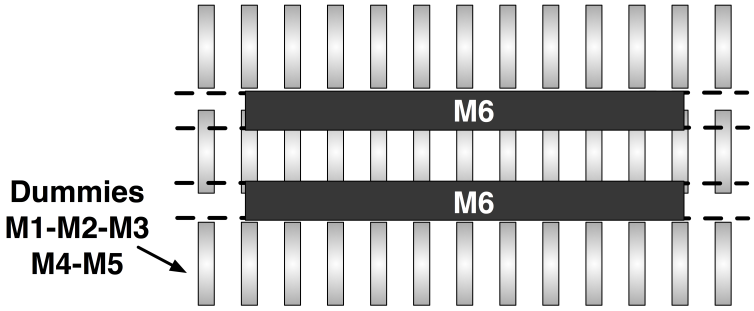

Figure 1.9: Example of a T-line design with dummies used to EM simulations.

1.2.1 Front-end technology

Complementary metal-oxide semiconductor (CMOS) is the dominating technology for most wireless products below 10 GHz. This dominance has been achieved by reliability, low cost, and high device count advantages of CMOS compared to the other semiconductor technologies such as SiGe and GaAs. Therefore in this technology, the performances, in particular the maximum frequency f_{max}, are lower than in the other semiconductor technologies, but they have a continuous improvement thanks the scaling-down. In Fig.1.10 and Fig. 1.11 the cut-off and maximum frequencies (f_T, f_{max}) are shown as functions of channel length of NMOS devices for different technologies. We notice that f_T and f_{max} increase as the scaling-down and it is encouraging for the next RF applications with CMOS technology.

Today, with the aggressive scaling of gate length, CMOS technology is pushing

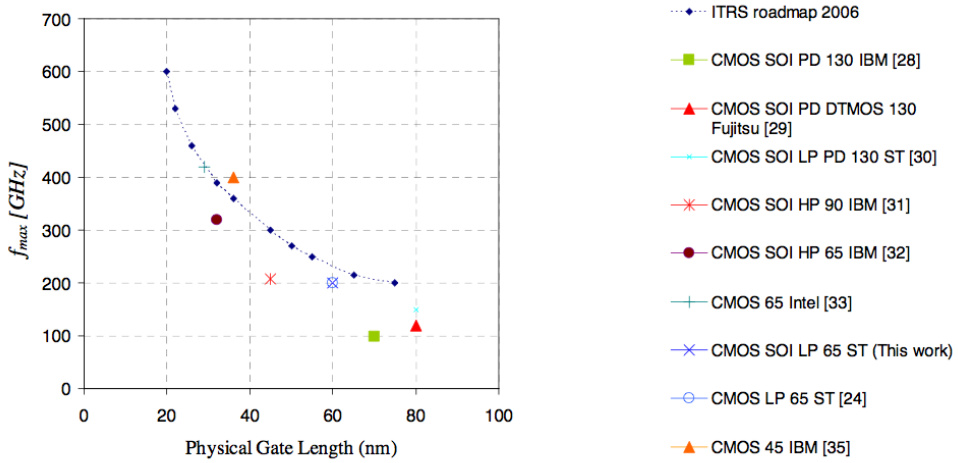

Figure 1.10: Maximum frequency as a function of channel length of NMOS devices for different technologies.

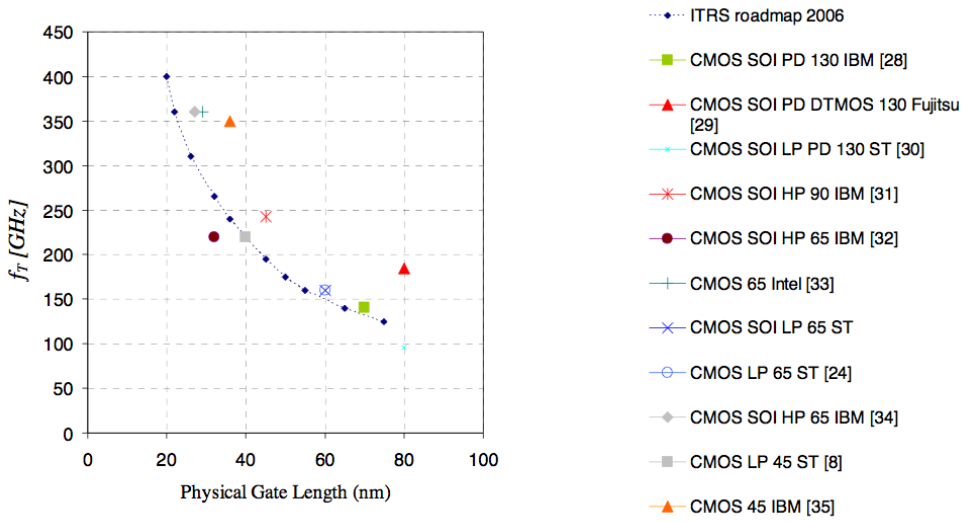

Figure 1.11: Cut-off frequency as a function of channel length of NMOS devices for different technologies.

further into the mm-wave region. Moreover, CMOS is the most promising technology for system-on-chip design, because it enables integration of the analog RF circuits as well as the digital signal processing and baseband circuits in the lowest possible area, which leads to a lower cost and compact solution. Therefore, the nano-scale CMOS technology, such as 65nm, offers commercial mm-wave solutions for short range and high data rate applications. In my research activity, the 65nm CMOS technology was used to implement the designed chips.

The 65nm TSMC process offers cost-effective benefits superior to the 90nm node, for example it features two times the 90nm gate density and boasts a speed improvement of between 30 to 50 percent. TSMC's 65nm logic family includes general purpose (GP), low power (LP) and LPG options. Furthermore, each process supports low, standard and high V_t options, with operating voltages range from 0.9 V to 1.26 V and I/O voltages include 1.8 V, 2.5 V and 3.3 V (5V tolerant). Raw gate density is around $854 Kgate/mm^2$, based on TSMC's standard cell library. The 65nm process provides a combination of general purpose (G) and low power (LP) core transistors together with a 2.5 V I/O transistor as a Triple Gate Oxide (LPG) process for optimizing speed, power, and leakage for wireless/consumer applications

- **MOS model**

  Now we focus our attention on 65 nm CMOS technology MOS model. Firstly, models are extracted from very sensitive high frequency S-parameter measurement suffering also from the de-embedding techniques that are not much optimized for these frequencies [22]. Moreover, intrinsic device effects negligible at lower frequencies must now be considered: the substrate effects are significant on the device performances; also effects such as short channel, tunneling leakage, STI (shallow trench isolation) stress induced and well proximity effects must be captured by the model [23]. Another reason for the 60 GHz modeling complexity is due to the important role of the device layout, which is more difficult to address. The device interconnections introduce parasitics inductors, resistors and capacitors, which dominate the performances of the device as the frequency increase. Each small finger of the device can be represented with an intrinsic transistor model based on the quasi-static-equations whereas the interconnections between the fingers are captured by electromagnetic sim-

ulations and experimental techniques. Since the layout details (connections to the gate, drain, source, and bulk, locations of the substrate contacts, etc..) have a major impact on the performances, models should be extracted only for fixed layouts and the transistors used in the circuit should be exactly the same previously characterized and modeled.

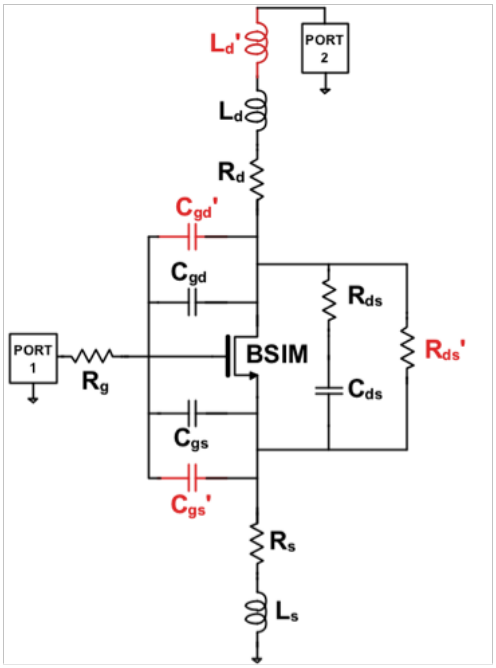

Figure 1.12: NMOS model.

A test chip with a collection of different size PMOS and NMOS devices has been integrated in the 65nm TSMC CMOS technology. The S-parameter of each device has been extracted using a 3-step de-embedding technique and has been compared to a custom 60 GHz NMOS model. For example, Fig. 1.12 shows the NMOS model: BSIM model is the MOS model provided by TSMC technology valid until 20 GHz, the layout parasitic capacitors and inductors have been extracted using EM Agilent Momentum simulations. The model includes also the gate resistance R_g, due to non-quasi-static effects and the capacitors C'_{gs} and C'_{ds} , the drain inductance L'_d and the resistance C'_{ds} added to take into account both the intrinsic parasitics elements, which are not evaluated by the low frequency BSIM model, and the parasitic elements due to the interconnections, which are closely tied to the de-embedding structures

used to extract the DUT S-parameters from the raw measurements data. The comparison between the measured and de-embedded device S-parameter and those extracted from our model shows a good fitting, regarding S_{12}, S_{21} and the imaginary parts of $Y_{11}, Y_{22}, Y_{12}, Y_{21}$. There are instead some discrepancies, which increase with frequency, in the real parts of Y_{22} and Y_{21}. These differences are probably due to the de-embedding technique issues at 60 GHz, where an accurate valuation of parasitics elements would be fundamental, but at the same time at these frequencies is very difficult to evaluate the very parasitics elements.

1.3 Millimeter wave phased arrays

The mm-scale wavelength of 60 GHz allows unprecedented levels of integration of analog and microwave components such as transmission lines and disparate monolithic microwave integrated circuits (MMICs) onto a single chip or package [1]. Millimeter wave wireless will find applications both indoor and outdoor for short-range WPANs and longer range uses such as mm-wave backhaul between base stations. The maximum range envisioned for 60 GHz systems for WPANs is several meters, whereas outdoor systems will likely be used for links up to 1 km. A more nuanced view of WPAN distinguishes two classes of devices that will occupy the 60 GHz WPAN product space. The first class is high performance devices capable of operating in non-line-of sight (NLOS) conditions such as around corners and past obstacles, and a range up to 10 m. The second class will be occupied by lower performance devices that only operate in line-of-sight (LOS) conditions with a range of a few meters (e.g. 3 m maximum), and will offer consumers a lower price entry point into the 60 GHz product space. The short wavelength of millimeter wave frequencies makes it possible to integrate receive and transmit antenna(s) on the chip. Integrated antennas offer significant benefits: 1) they obviate the need for expensive and lossy millimeter wave packaging; 2) they lend themselves to differential operation, transmitting a greater power for a given voltage swing; 3) the receive and transmit paths can incorporate separate antennas to avoid the use of lossy transmit/receive switches; 4) the transmitter need not be ac-coupled to the antenna; 5) they eliminate the need for high-frequency electrostatic discharge (ESD) protection devices; 6) the

antennas can serve in a beamforming array, raising the output power [17]. However, in millimeter-wave transceivers, several system and circuit level challenges must be met, such as the lack of efficient and low cost antennas and packaging solutions, the severe path losses, the low output power and nonlinearity of power amplifiers and the limited achievable gain and high noise figure of low noise amplifiers at 60 GHz.

The high free-space path loss, the poor quality of CMOS technology and the intrinsic link budget limitations at mm-wave frequencies are addressed using programmable phased-array multiple-antenna systems [24] [25]. Indeed, integration of a complete phased array system in silicon results in substantial improvements in cost, size and reliability. At the same time, it provides numerous opportunities to perform on-chip signal processing and conditioning, without having to go off-chip, leading to additional saving in cost and power.

At the circuits level, the division of the signal into multiple parallel paths relaxes the power handling and noise requirements for individual active devices used in the array, as will be discussed later; this also makes the system more robust to the failure of individual components. Multiple antenna phased arrays imitate the behavior of a single directional antenna whose beam-steering capability can be controlled electronically; this electronic steering makes it possible to emulate antenna properties such as gain and directionality, while eliminating the need for continuous mechanical reorientation of a directive antenna. A phased array receiver consists of several sig-

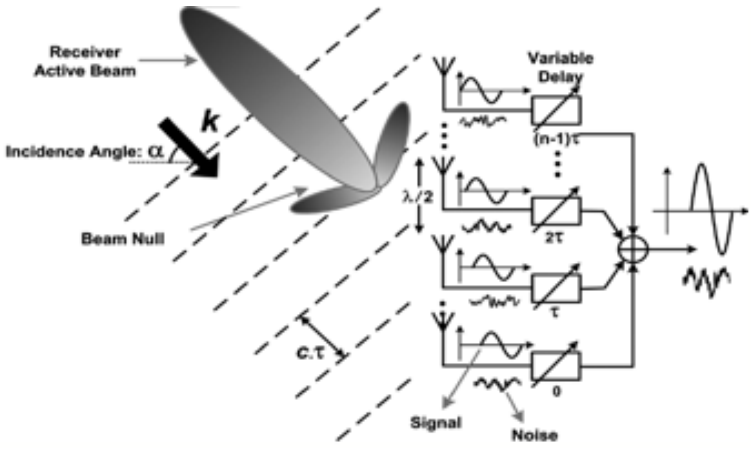

Figure 1.13: Phased array receiver.

nal paths, each connected to a separate antenna. The antenna elements of the array

can be arranged in different spatial configurations [26]: the array can be formed in one, two, or even three dimensions, with one- or two-dimensional arrays being more common. As shown in Fig. 1.13, an ideal phased array receiver compensates for the time delay difference between the signals from different antennas and combines the signals coherently to enhance the reception from the desired direction(s), while rejecting emissions from other unwanted directions. Thus the receiver is capable of canceling out interferers as long as they do not originate from the same direction as the signal [10].

1.3.1 Local oscillator distribution

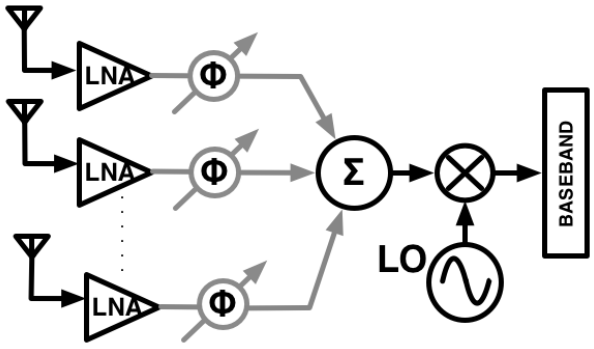

Figure 1.14: Radio frequency phase shifting architecture.

At millimeter-wave the direct down-conversion architecture is preferred over the heterodyne one, because it eliminates the image frequency challenge of superheterodyne receivers and can be implemented in less area and more cheaply. As mentioned, for narrow-band application, controllable phase shifters are needed to compensate for the phase shift between the input signals, in order to add them coherently. The basic possibilities to perform beamforming depended mainly on where the phase adjustment is performed. Phased-array architectures can be divided into three main categories: RF phase-shifting [27], local oscillator (LO) phase shifting [28] and baseband phase rotation [29].

In RF phase-shifting arrays (Fig. 1.14), the signals received from the array antennas are scaled, delayed and combined prior to down-conversion. This configuration requires a minimal amount of hardware, but low-noise broadband variable phase

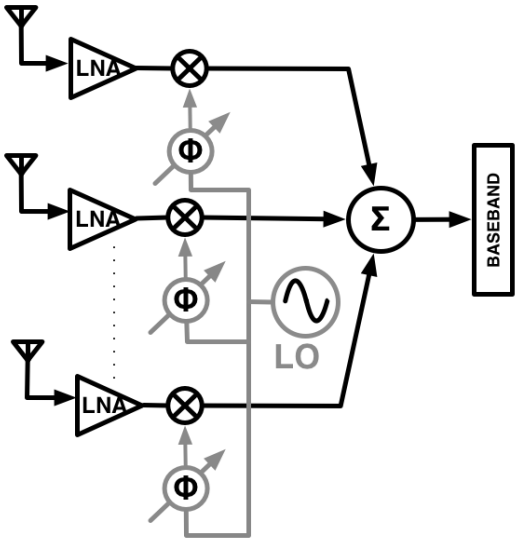

Figure 1.15: Local oscillator phase shifting architecture.

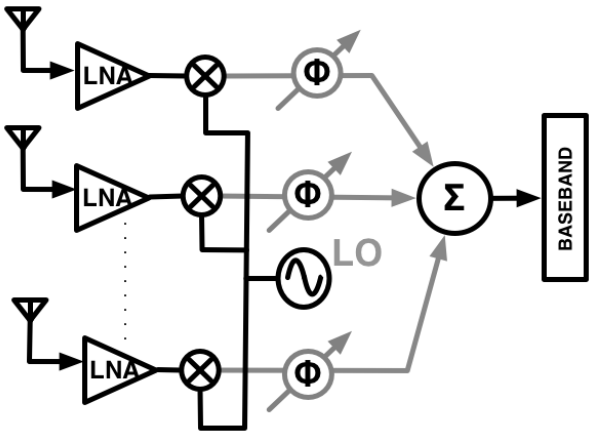

Figure 1.16: Baseband phase shifting architecture.

shifters and variable gain amplifiers pose great design challenges. Any additional noise and distortion in the RF path degrades the signal-to-noise ratio (SNR) and, to compensate for it, larger arrays are needed, leading to higher system costs. This motivates the use of IF and baseband recombination architectures.

LO path phase shifting (Fig. 1.15) alleviates the design issues in the RF path, in fact it is less sensitive to amplitude variations and noise addition can be obtained, but requires considerable power consumption for variable LO phase generation and distribution. Moreover, reciprocal mixing is a more serious issue than in RF combining architectures, where unwanted interferers are rejected prior to mixing; hence, higher LO spectral purity is needed [30].

To save power, phase rotation can be carried out directly at baseband (Fig. 1.16) using digitally-controlled variable-gain baseband amplifiers [29] provided that a quadrature LO is available. This approach also comes with the challenge of the LO distribution, and requires baseband hardware for the implementation of the phase shifting and signal combination.

In the latter two cases, although the RF losses are minimized, however the power overhead due to LO distribution is still significant. In fact the issue of these architectures is given by the LO distribution: for example, as shown in Fig. 1.17a, in a classic LO phase-shifting configuration the signal that generates from the single VCO must be carried out at each mixers of the N single receiver of the array. LO signals must travel large distances experiencing significant losses and mismatches; this means that most of power is wasted in the LO distribution: for example, in [28], a two-path 52 GHz phased-array receiver, based on LO phase-shifting, the 35% of the total power consumption is used to generate the LO signal and even the 38% of the total power consumption is used in the LO distribution. To address this issue, we proposed an array of coupled distributed oscillators, which can be used to carry out LO generation and distribution at the same time (Fig. 1.17b). Our aim is to design a phased-array composed by distributed oscillators, where each oscillator can be connected directly to each mixer of the single receivers. Thus the receiver, which composed the array, will have an oscillator and, thanks the oscillator distributed configuration, each VCO will be coupled to each other to create a distributed configuration. This fits well with the distributed nature of the phased array architecture and allows to take advantage of the power needed for LO distribution to improve

phase noise. As a result a more efficient and potentially lower power design can be achieved.

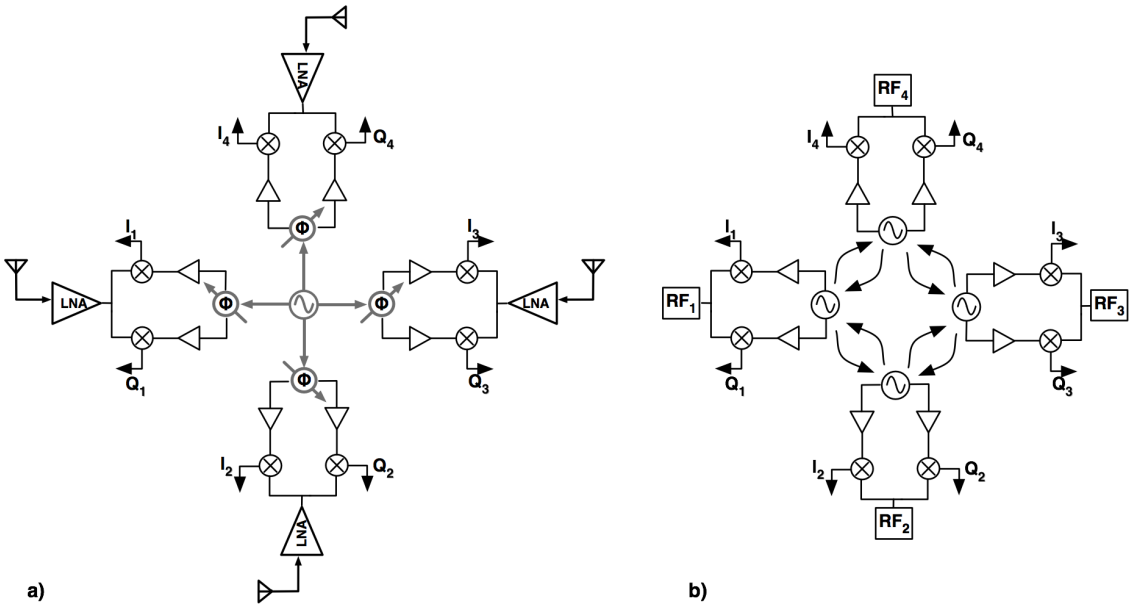

Figure 1.17: a)Block diagram of a 4 element phased array receiver using LO phase-shifting, b)Block diagram of a 4 elements phased array direct-conversion receiver with coupled oscillators array for LO generation and distribution.

This idea has been implemented, in my research activity, in a mm-wave 4-paths phased array receiver prototype. The designed distributed oscillator is a "Hybrid" Wave Oscillator (HWO), which will presented in chapter 3 [34]. Each HWO is connected to the quadrature passive down-conversion mixer using a LO buffer.

The passive mixer is characterized by a broad matching bandwidth; in fact, depending on the market, the product aims at frequency regulations to allow slightly different frequency ranges to be used. The mixer is a key circuit block in communications systems and in order to use the maximum available bandwidth in every region, needs to cover the entire frequency range from 57 to 66 GHz. However, to achieve such a wide matching bandwidth is a challenge of integrated millimeter-wave CMOS design: not only a high RF bandwidth is crucial, but also the IF bandwidth has to be sufficiently large for high throughput. The RF bandwidth is an important parameter for a mixer as it determines the spectral coverage of the RF band with a proper adjustment of the LO frequency for a fixed IF. The broadband passive mixer design will be discussed in chapter 2 [18].

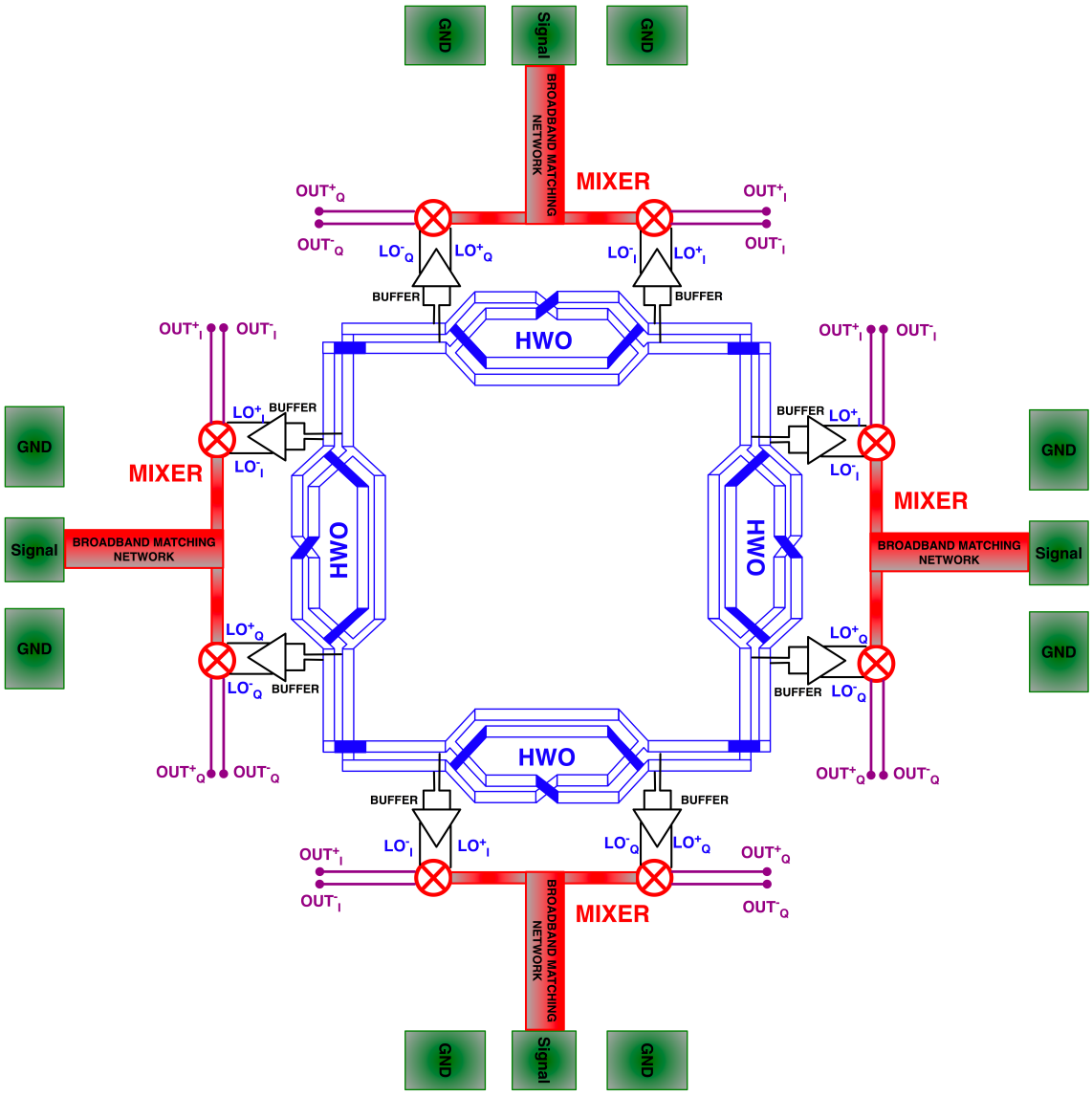

Figure 1.18: Complete broadband distributed mm-wave receiver architecture.

The complete architecture, which we have implemented, is shown in Fig. 1.18.

1.4 Conclusions

The recent release of a license-free 7 GHz band around 60 GHz has triggered a world-wide research effort on mm-wave circuit and system design for this frequency band. The constant scaling of CMOS technology has resulted in CMOS devices

becoming fast enough for mm-wave operation and enabling the realization of low-cost 60 GHz transceivers. Despite the large number of CMOS circuits and solutions that were published over the past few years, some issues still hamper the optimal realization of a complete 60 GHz CMOS transceiver. The high free-space path loss and the poor quality of CMOS technology at mm-wave frequencies result in the need for directional communication, which can be implemented using programmable phased-array multiple-antenna systems. A direct conversion architecture offers three basic possibilities to implement beamforming: in the signal path, either at RF, at baseband or in the digital domain, or in the LO path. The RF phase shifting is characterized by high RF losses, instead in both LO and BB phase-shifting cases the complexity of the LO distribution subsystems is increased, as each signal path needs to be supplied with a strong LO signal. In large systems, using a central 60 GHz LO, source this leads to high power consumption due to the 60 GHz LO buffering. This problem is solved here by using a 4-coupled distributed phased-array receiver, where each distributed oscillator carries out the LO signal directly to the quadrature mixer.

Chapter 2

Broadband Millimeter Wave Passive Mixer

For the receiver circuitry the choice of the mixers architecture is very important, because it influences the entire down-conversion chain. Heterodyne systems employ two consecutive stages of down-conversion, while the homodyne system requires only one mixer, thus the complexity of the system is lower [36]. In CMOS technology, [37] the two mixer topologies that are popular and most commonly used are: the active double-balanced mixer (Gilbert mixer) [38]; and the passive double-balanced mixer [39]. Operationally, active mixers modulate transconductance while passive mixers modulate a switch resistance [19]. Active mixers provide a conversion gain through switches that serve as amplifying elements, while in passive mixers the conversion gain is attained using a trans-impedance stage after the down-conversion [1].

The direct down-conversion architecture presents several design issues and the typical ones are the DC voltage offset and strong flicker noise. These phenomena are particularly remarkable on a classical active architecture: the Gilbert cell mixer. Another problem of the active mixer configuration is the linearity and this aspect is accentuated by the low voltage supply for sub-micrometer devices [40]. An alternative approach can rely upon the use of a passive mixer. Passive mixers are easier to implement at subterahertz frequencies compared to active mixers [41], [42]. Passive mixers consume very little power, can achieve high linearity performance [41], and lower flicker noise and shot noise [42] than active designs. Large LO power is difficult

to achieve at 60 GHz, since transistors operate closer to the transit frequency and maximum frequency of oscillation in CMOS [19] and this greatly complicates mixer design (especially switch-based passive mixers, which often require higher LO power levels in order to switch firmly). Conversion gain falls off quickly and conversion loss rises quickly with reduced LO power [19]. Thus, 60 GHz mixer designs must consider lower LO power levels if passive mixers are used and also gain and linearity must be balanced.

Moreover, the "transparency" of passive mixers should be exploited to achieve high selectivity at RF and, eventually, recognizing the capability of passive mixers to provide low-noise impedance matching, mixer-first receiver architectures have started to emerge. The non unilaterality of passive mixers has made classic analysis and optimization techniques obsolete. Several simplified models have been proposed through the years to enable a more in-depth understanding of passive mixers operation. Nonetheless, still today, clear design guidelines for low-noise passive mixers design are lacking. Several questions remain without a clear answer, unless possibly restrictive assumptions are made. In a classic receiver front-end the signal is first low-noise amplified and converted to current by the LNA and then frequency translated by a current commutating switching stage. Alternatively, in mixer-first receivers, the mixer core provides low-noise impedance matching and frequency down-conversion. When the operating frequency is close to the device f_T (e.g. in mm-wave applications) it is not uncommon to use power-matching between blocks. Therefore, even when a low-noise amplifier proceeds the mixer, it is interesting to analyze the performances of the mixer under power matching condition.

In this chapter, a passive mixer is presented where the antenna directly interfaces to the passive mixer and provides wideband input matching without significant degradation of performance (especially noise figure and linearity) [18]. In the first section the entire passive down-conversion mixer architecture will be presented, explaining the reasons behind the broadband mixer design; the second section will show how the broadband matching network of 28 GHz at the mixer input can be designed and implemented and in the third section the mixer performances (input impedance, gain and noise figure) of the passive mixer will be analyzed. Finally, in the fourth section the mixer core design will be presented, in particular the choice of the mixer parameters values (switches dimensions, baseband stage dimensions,...)

will be explained, driven by the goal to achieve a good trade-off between wideband matching, noise figure and power consumption. In the last section the experimental results will be shown.

2.1 Power Matched Mixer Architecture

After the matching network, traditional receivers have an LNA that must be low noise, provide power gain, and exhibit good linearity, while providing an input impedance that is matched [43]. This is not entirely straightforward: a simple resistive matching network always results in a noise figure above 3 dB. In fact, a reasonable definition for an LNA is an amplifier which provides a real impedance match while maintaining a sub-3 dB noise figure. For applications requiring low noise figure and a good impedance match, a resonant antenna impedance matching network is typically used. To make matters worse, the impedance of the antenna and matching network is strongly frequency dependent, severely limiting channel tuning range for high performance receivers. Because performance tradeoffs tend to fall so heavily on the receiver front end, and involve relatively inflexible components, many multiband systems that receive a range of frequencies use multiple, parallel front-ends, tuned to different frequencies, using distinct matching networks and LNAs [46], [47]. Alternatively, an LNA with wideband impedance matching and good noise figure can be achieved using either a wideband amplifier with resistive feedback [48], [49], or with a noise-canceled LNA [50]. Such designs intrinsically require large amounts of power to operate at RF frequencies while maintaining a constant antenna impedance, and still generally provide a relatively fixed input impedance. At the other extreme, applications requiring low power consumption and cost can simply forgo the matching network and LNA completely, connecting directly to a passive mixer [51] [4].

Both in case the mixer is connected to the antenna and to a LNA, it is useful to implement a matching network as wide as possible to work at the entire mm-wave frequency range. In my research activity, we address the design of the passive mixer, and the main goal is to demonstrate the feasibility of a quadrature down-converter in CMOS technology with a simple input matching network capable of covering a broad frequency range with good performances and low power dissipation. The

mixer selected for this design is a power-matched passive mixer (Fig. 2.1), whose input broadband matching network design will be discussed in the next section and the baseband stage is a a differential resistive feedback amplifier (section 2.3.3). This

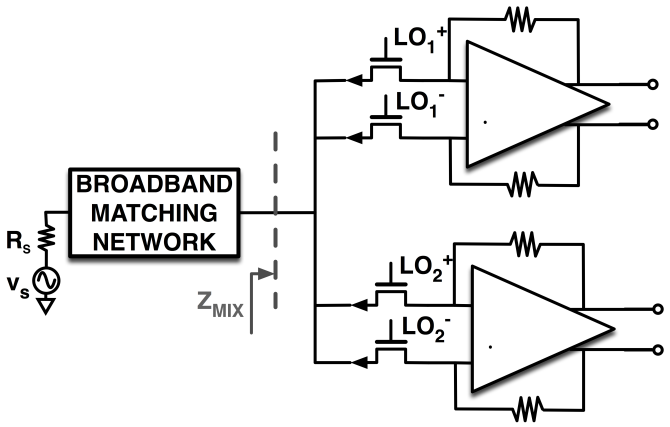

Figure 2.1: Broadband passive mixer architecture.

type of mixer offers several advantages: first, it can be power matched to the driving stage over a broad frequency range because it provides a resistive input impedance; second, compared to Gilbert-cell like designs (e.g. [53]) passive mixers feature lower flicker noise (an important feature in scaled CMOS technologies); third, thanks to the baseband trans-impedance stage, they provide higher gain, reducing the noise contribution of the following stages.

2.2 Broadband Matching Network

In the designed mixer a wide band matching network is needed; however, at millimeter wave, the matching bandwidth is limited by the devices f_T but the parasitics capacitances, which, for example in 65nm CMOS technology, can weight over 20% of the total load capacitance value. Indeed, the mixer input impedance Z_{MIX} represents a bottleneck to achieve a broadband match: the R_{MIX} is given in first approximation by the single switch resistance, but C_{MIX} weights four times C_{gs} ($C_{MIX} = 4 * (C_{gs} + C_{par})$), which limits the matching bandwidth (Fig. 2.1). To simplify the matching issue, the mixer has been modeled as a RC load, which usually requires only a narrow matching network, where the load impedance is equivalent to the mixer input impedance (Fig. 2.2).

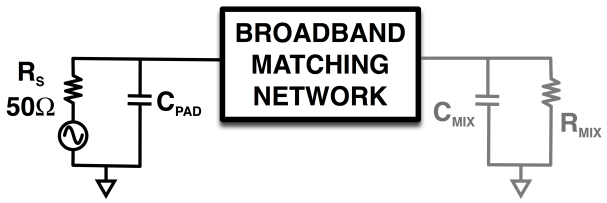

Figure 2.2: RC model of passive mixer.

To achieve input matching, many choices are available and there are many factors that may be important in the selection of a particular matching network, as the network complexity: a simpler matching network is usually cheaper, more reliable and less lossy than a more complex design. To establish the trade-off between maximum allowable reflection in the pass-band and the bandwidth, Bode-Fano criterion can be used: this criterion gives, for a certain canonical types of a load impedances, a theoretical limit on the minimum reflection coefficient magnitude that can be obtained with an arbitrary matching network and it provides a benchmark against which a practical design can be compared.

Fig. 2.2 shows a lossless network used to match parallel RC load impedance, and the Bode-Fano criterion can be expressed as:

$$\int_0^\infty \ln \frac{1}{|\Gamma|}\, \mathrm{d}\omega \leq \frac{\pi}{RC}, \tag{2.1}$$

where Γ is the reflection coefficient seen looking into the arbitrary lossless matching network.

In conclusion, for a given load (fixed RC product), a broader bandwidth ($\Delta\omega$) can be achieved only at the expense of a higher reflection coefficient in the pass-band (Γ_m). For example in 65nm CMOS technology, for a RC equal to 6ps, a 40 GHz bandwidth can be obtained with a -17 dB return loss. To obtain a wideband matching network, we started considering the classic lumped narrow matching networks to extract a method to design a matching network with a large bandwidth, and then we used this method to realize our broadband T-line network, more suitable at mm-wave.

First of all, we consider the classic narrow lumped matching networks used when the load is only resistive.

- **L-Match Network**

  The simplest type of lumped matching network is the L-section, which uses two reactive elements to match arbitrary load impedance to a transmission line. There are two possible configurations for this network: high pass configuration and low pass configuration (Fig. 2.3).

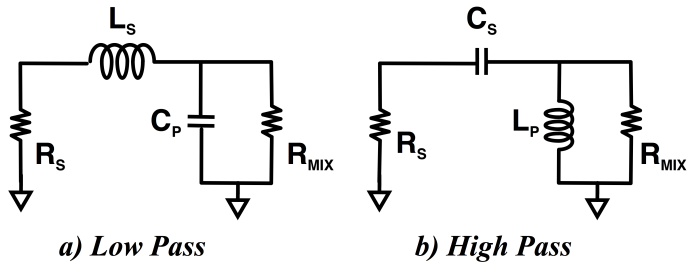

Figure 2.3: L-match network circuit: a) Low pass, b) High pass.

This network topology has only two degrees of freedom (L and C values), hence once the impedance transformation ratio and the frequency have been specified, the quality factor, which influences the bandwidth, is automatically determined and is given by:

$$Q_{LowPass} = \sqrt{\frac{R_{MIX}}{R_S} - 1}, \tag{2.2}$$

$$Q_{HighPass} = \frac{R_{MIX}}{R_S} \frac{1}{\sqrt{\frac{R_{MIX}}{R_S} - 1}}. \tag{2.3}$$

- **$\Pi-$Match Network**

  One limitation of L-match network is that it has only two degrees of freedom, impedance transformation ratio and quality factor. To acquire a third degree of freedom, a π-match network (for example, we consider the low-pass $\pi-$match network, shown in Fig. 2.4) can be used: this matching network can be considered as two L-match connected in cascade, one that transforms down and one that transforms up.

  The load resistance R_P in transformed down to a lower intermediate resistance R_{mid} at the junction of the two inductors and then R_{mid} is transformed up to

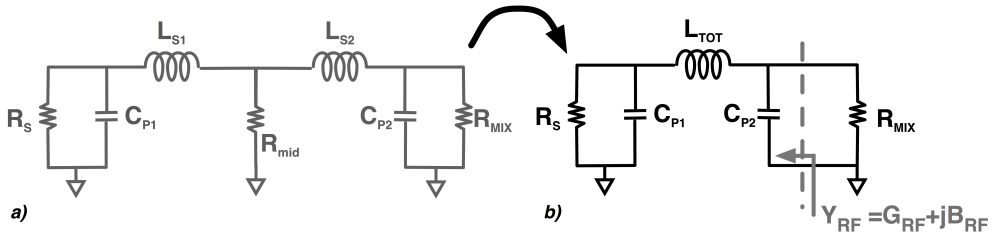

Figure 2.4: π-match network circuit: a) two L-match networks connected in cascade, b) π-match network.

a value R_S by a second L-match section. Typically, the Q of an L-match is not particularly high, because huge transformation factors are infrequently required, instead the π-match decouples Q from the transformation ratio and this allows to achieve much higher Q than generally available from L-match: in particular the quality factor of a low-pass $\pi-$match network is given by:

$$Q_{LowPass} = Q_1 + Q_2 = \sqrt{\frac{R_{MIX}}{R_{mid}} - 1} + \sqrt{\frac{R_S}{R_{mid}} - 1}. \tag{2.4}$$

Now center frequency, quality factor (or bandwidth) and overall impedance transformation ratio can be independently defined; furthermore the parasitic capacitances, which cannot be neglected in a real matching network, can be absorbed into the network design.

At millimeter-wave the load is not only resistive, because the parasitic capacitances cannot be neglected. Achieving a broadband match with a complex load (Fig. 2.2) is more difficult, particularly as one seeks to approach the Bode-Fano criterion limit. The imaginary part of the load can be absorbed in matching network, leaving a real impedance matching problem, and if the imaginary part value is too high to the matching network, the excess imaginary part can be resonated at the frequency of interest.

In order to maximize the bandwidth, a design approach based on doubly-terminated passive ladder filters could be used. In this case, considering that both load and source are impaired by parallel capacitors, at least three inductors or T-lines would be needed (Fig. 2.5a). However, to reduce the complexity and the area of the matching network, it is important to achieve the widest possible bandwidth with a minimum number of inductive elements. A wideband match can be also realized

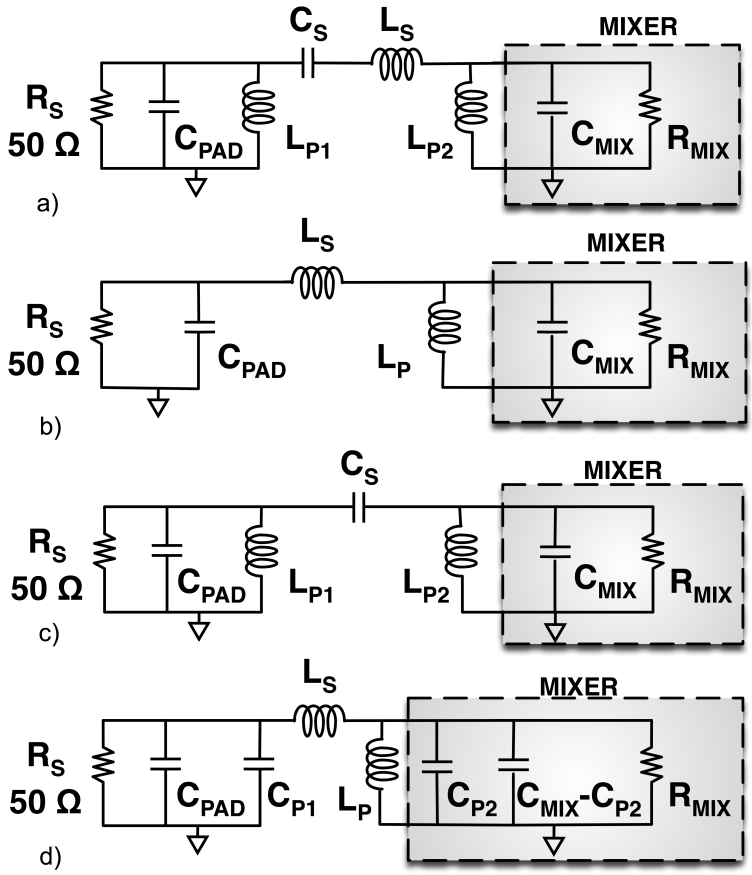

Figure 2.5: Broadband matching networks: a) 3° order band pass network, b) low-pass L-match network, c) doubly-resonated high pass π-match network, d) low pass π-match network.

with the classic lumped matching topologies, previously described, which use only two inductors. In Fig. 2.5, the schematics of the considered design approaches are reported, all using at most two inductors. In the resonated low-pass L-match design (Fig. 2.5b), the load capacitance is resonated by a parallel inductor, while the pad capacitance is absorbed in a low-pass L-match. In the doubly-resonated high-pass π-match design (Fig. 2.5c), the load and pad capacitances are resonated by parallel inductors. The load resistance is matched to the 50 Ω source by the high-pass π-network that absorbs the source and load resonating inductors. In the resonated low-pass π-match design (Fig. 2.5d), the load capacitance is partially resonated by a parallel inductor and partially incorporated in the low-pass π-network that fully absorbs the pad capacitance.

The simulated $|s_{11}|$ of the four topologies are reported in Fig.2.6: the widest bandwidth is achieved using the low-pass π-network with partially resonated load (Fig.2.5d). The design procedure to obtain a wide matching bandwidth for this

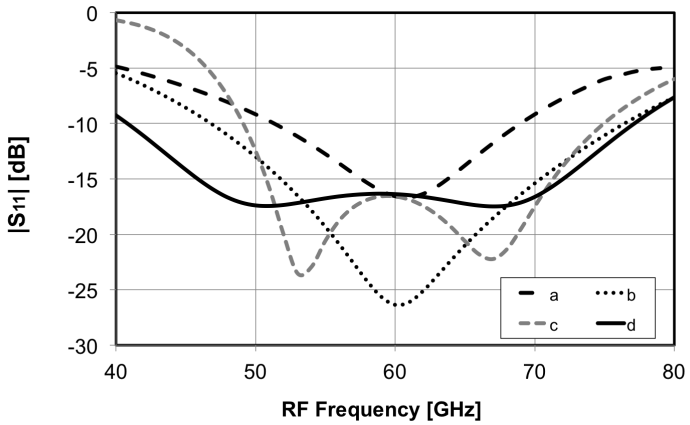

Figure 2.6: Simulated $|s_{11}|$ of the broadband matching networks reported in Fig.2.5 a to d.

topology is as follows: initially consider a classic low-pass π-network, reported in Fig. 2.4, in which $C_{P1} = C_{PAD} + C_{P1'}$ and $C_{P2} = C_{MIX} - C_{P2'}$ and assume that the circuit parameters, except for R_S, can be chosen freely. An illustration of the real (G_{RF}) and imaginary part (B_{RF}) of the admittance Y_{RF} seen looking back toward the source is shown in Fig. 2.7.

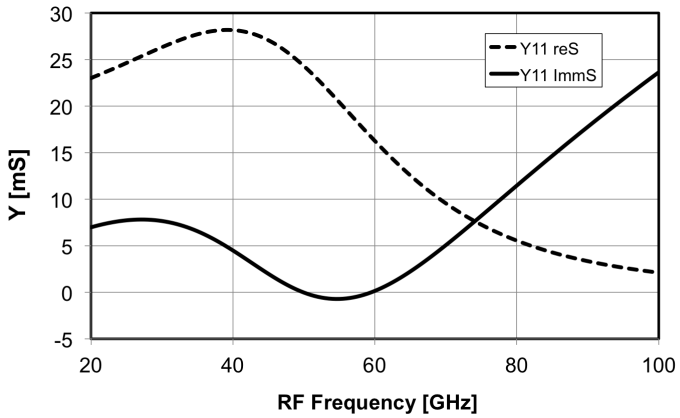

Figure 2.7: Simulated admittance seen from the mixer input toward the source: real and imaginary part.

The imaginary part goes to zero at the chosen center frequency (ω_0 =60 GHz in the example), while the real part shows a maximum at a generally different frequency (ω_{MAX}) and it corresponds to:

$$\omega_{MAX} = \sqrt{\frac{1}{L_{TOT}C_1} - \frac{1}{2R_S^2C_1^2}}. \tag{2.5}$$

By imposing:

$$\omega_{MAX} = \omega_0, \tag{2.6}$$

the impedance flatness and hence the matching bandwidth are maximized. The resulting design equation is:

$$Q_2 = \frac{Q_1}{1 + 2Q_1^2}, \tag{2.7}$$

where $Q_1 = \omega_0 R_S\, C_{P1}$ and $Q_2 = \omega_0 R_{MIX} C_{P2}$. The matching bandwidth increases as Q_1 and Q_2 are decreased; on the other hand, the pad capacitance sets a lower limit to the value of Q_1, ultimately C_{PAD} sets an upper bound to the mixer core impedance R_{MIX}, as shown in Fig. 2.8. The remaining capacitance $C'_{P2} = C_{MIX} - C_{P2}$ is then

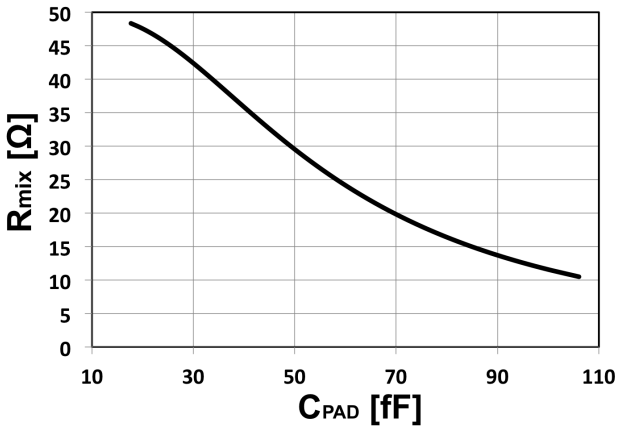

Figure 2.8: Equivalent mixer resistance as a function of the pad capacitance

resonated out by a parallel inductance L_P. The final value of R_{MIX} will be chosen slightly larger than the value given by (2.7), as a compromise between in-band return loss and bandwidth. The designed lumped matching network is reported in Fig. 2.9. At millimeter wave, transmission lines are preferred respect to inductors, to reduce area and losses. The analysis to evaluate a T-line broadband matching network is

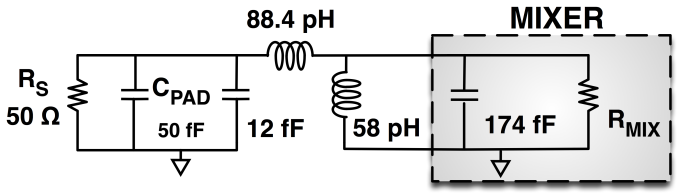

Figure 2.9: Lumped broadband matching network.

similar to the previous procedure, but in this case we have an additional degree of freedom with respect to lumped matching networks: for a T-line both characteristic impedance (Z_0) and electric length (e°) have to be imposed.

Replacing the two inductors of the lumped matching network in Fig. 2.9 with coplanar transmission lines, the equations, which describe real and imaginary part of the admittance seen looking back toward the source, can be solved in numerical way. The same bandwidth can be obtained for different values of Z_0, as shown in Fig. 2.10.

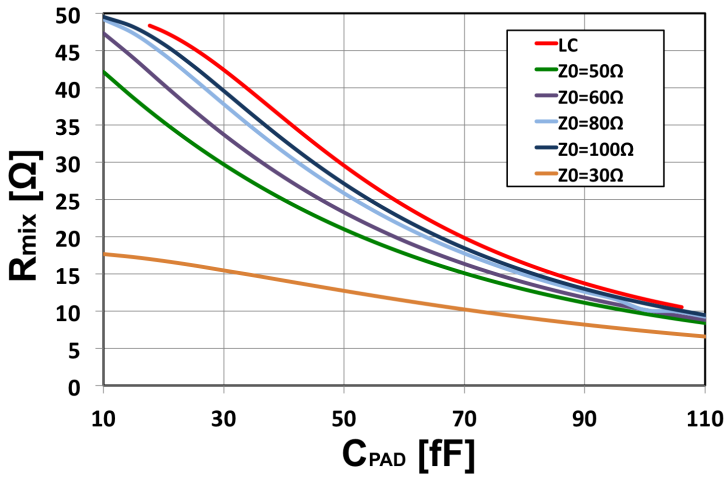

Figure 2.10: Equivalent mixer resistance R_{mix} as a function of pad capacitance for different characteristic impedance Z_0 values.

The equivalent T-line broadband matching network of the lumped network, is shown in Fig. 2.11. In Fig. 2.12 we noticed that the two networks are characterized by near the same bandwidth of 40 GHz with a $s_{11} = -10dB$.

However the matching network must be modified, because the mixer has to be connected to the distributed oscillator presented in chapter 3, as shown in Fig. 2.13; therefore the T-line network is split in two, to connect to the two separate mixer

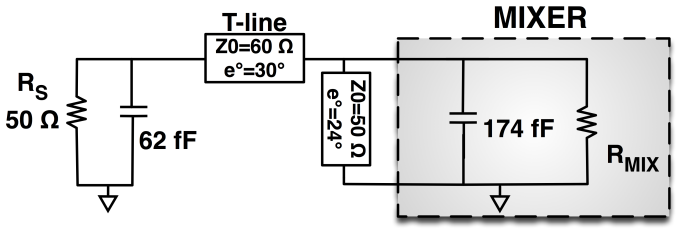

Figure 2.11: Transmission line broadband matching network.

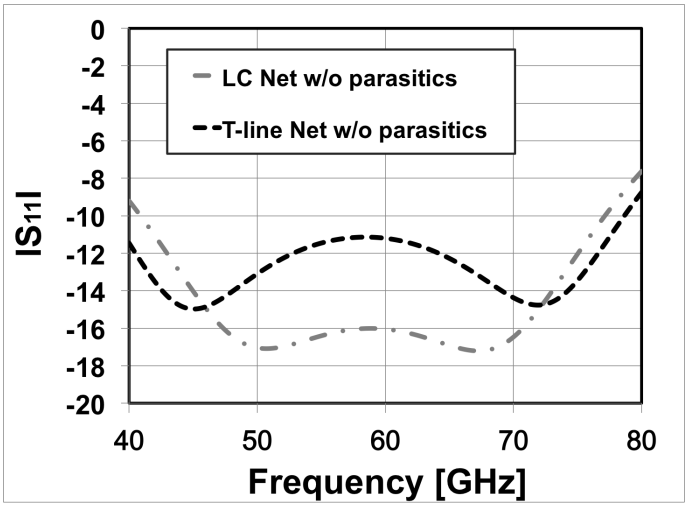

Figure 2.12: s_{11} of lumped broadband matching network and of T-line broadband matching network.

cores. In this case the C_{MIX} value is half than before, therefore ideally the match bandwidth should be larger than the previous case, but now also the layout parasitics capacitances due to the interconnections must be taken into account and they weight on the matching, reducing the bandwidth; however, the implemented split matching network achieves a 28 GHz bandwidth, at $|s_{11}| < -10dB$ (Fig. 2.14).

2.3 Mixer Performances Analysis

The non unilaterality of passive mixers has made classic analysis and optimization techniques obsolete. Several simplified models have been proposed through the years to enable a more in-depth understanding of passive mixers operation. Nonetheless, still today, clear design guidelines for low-noise passive mixers design are lacking. Several questions remain without a clear answer, unless possibly restrictive assump-

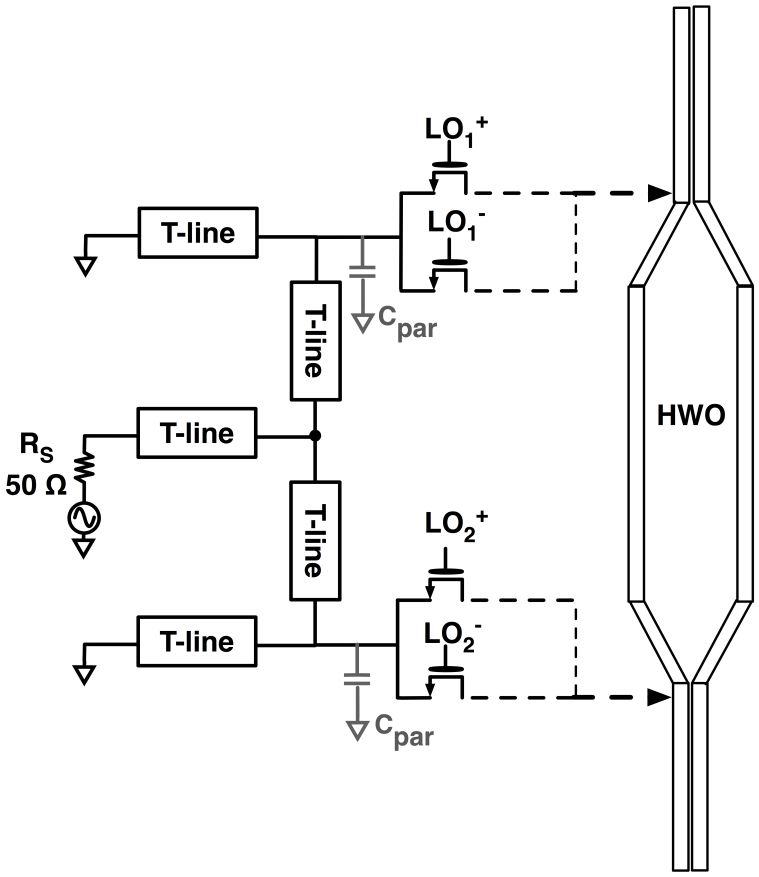

Figure 2.13: Implemented architecture of the split broadband matching network used in the passive mixer design.

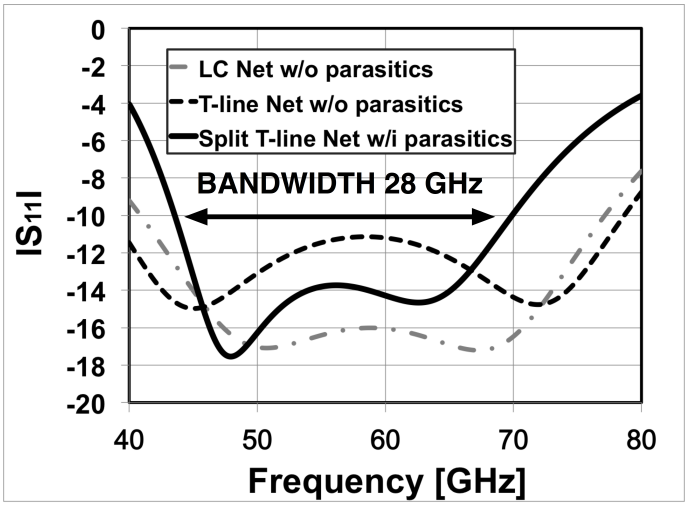

Figure 2.14: $s_{11}$of split broadband matching network.

tions are made. In a classic receiver front-end the signal is first low-noise amplified and converted to current by the LNA and then frequency translated by a current commutating switching stage. Alternatively, in mixer-first receivers, the mixer core provides low-noise impedance matching and frequency down-conversion. When the operating frequency is close to the device f_T (e.g. in mm-wave applications) it is not uncommon to use power-matching between blocks. Therefore, even when a low-noise amplifier proceeds the mixer, it is interesting to analyze the performances of the mixer under power matching condition. The down-conversion mixer core may be driven by an LNA (directly or through a transconductor stage), and in this case the driver can be represented as a current generator (current-driven mixer), or the mixer can be driven directly by the antenna, and in this case the driver can be represented by a voltage generator with a series resistance equal to the mixer input impedance (power matching). Parasitic capacitors (from the driving circuit and from the switches) also load the input node. Especially at high frequencies, a resonant input network may be used to resonate with the parasitic capacitors at the input frequency. The purpose of this section is to introduce a power-matched passive mixer core model that predicts input impedance, gain and noise, and to discuss the limits for the NF of the mixer. The baseband stage will be represented here as a simple passive (resistive) load. Then, focusing on mixer design guidelines, practical baseband stage implementations will be considered. Following Molnar's work [43], the passive mixer is modeled with four switches resistances R_{SW} (Fig. 2.15), which are successively turned on in four non-overlapping, 25% duty-cycle phases over the course of one local oscillator (LO) period [4]. These non-overlapping pulses are necessary for preventing the performances degradation described in [54]. The input port of the mixer is connected directly to the antenna port, with the source resistance R_S. The switches sample the RF voltage onto four capacitors C_L loaded by the baseband resistors R_{BB}. The phase-split nature of the LO, the mixer, and hence the amplifiers produce differential baseband signals with both I (from the 0° and 180° switches) and Q (from 90° and 270°) components.

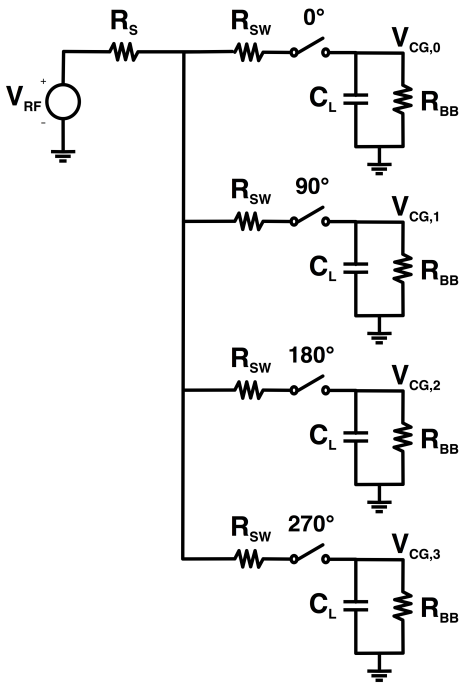

Figure 2.15: Simplified circuit model of 4-phase passive mixer.

2.3.1 Impedance and gain analysis

The model, shown in the Fig. 2.15, treats the switches as a small series resistance, R_{SW}, which represents the on-resistance of the switching MOSFET. Since the LO pulses are completely non-overlapping, only one is active at a time, so the series resistance of all of the switches can be lumped together and treated as a single resistor of the same value, as shown in Fig. 2.16. If we treat the antenna impedance as a resistor (neglecting its reactive components for the moment), then the entire RF portion of the circuit can be modeled as a single lumped series combination of R_S and R_{SW} and in series with a parallel array of four ideal switches. We can define an effective antenna resistance as:

$$R'_S = R_S + R_{SW}. \tag{2.8}$$

We now define a virtual voltage V_x at the node in between R_{SW} and the ideal switches. The baseband port of the switches is loaded by the parallel combination of a filtering capacitor C_L and the amplifier input resistance R_{BB}. If the time constants

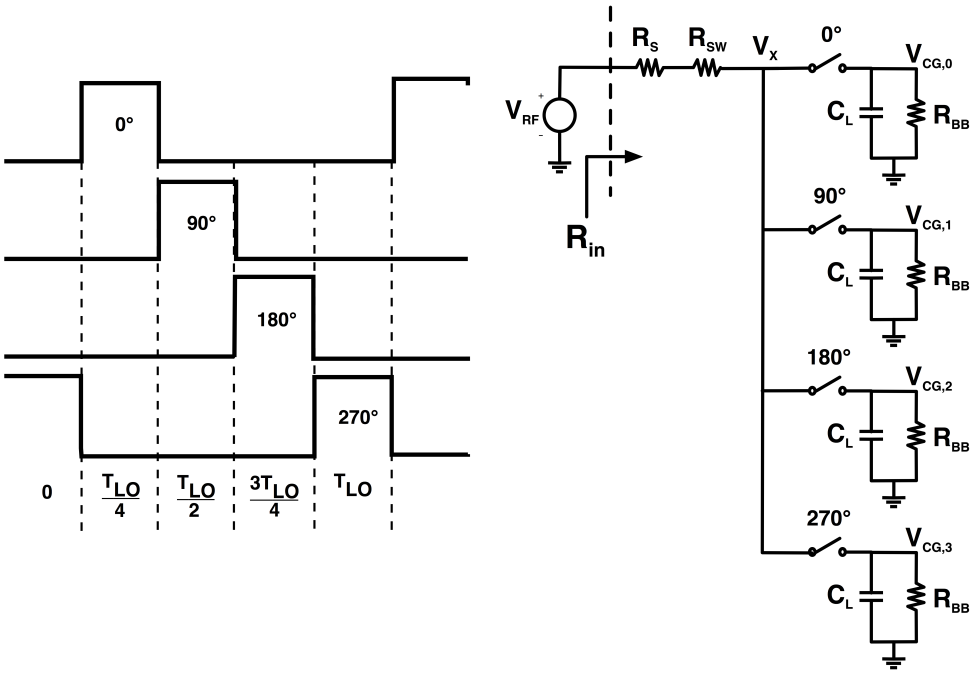

Figure 2.16: Equivalent model to 2.15, with R_{SW} lumped with R_S, based on non overlapping nature of the LO waveform.

$R_{BB}C_L$ and R'_SC_L are significantly larger than the LO period T_{LO}, then we can approximate these capacitors as holding their voltage constant over a given LO cycle. For in-band signals, the input signal from the antenna can be approximated as a sinusoid with fundamental frequency $\omega_{LO} = \frac{2\pi}{T_{LO}}$ and time varying phase $\phi(t)$ and amplitude $A(t)$, which capture both modulation and offset frequency of the received signal. If the amplitude and phase offset change slowly relative to T_{LO} they can be approximated as constant over a given LO period, and the input voltage V_{RF} can be expressed as:

$$V_{RF}(t) = A\cos\omega_{LO}t + \phi. \tag{2.9}$$

To compute the input impedance presented by the mixer to the antenna and the voltage gain ($V_{CG,m}$), where $m = 0, 1, 2, 3$ indicates the C_L capacitors, we can use the conservation of charge in node V_x between the RF side of the mixer and the baseband side. The voltage gain is equal to:

$$V_{CG,m} = \frac{4\sqrt{2}}{\pi}\frac{R_{BB}}{R_{BB} + 4R'_S}, \tag{2.10}$$

as explained in details in [43].

The mixer input impedance can be expressed as:

$$Z_{in} = R'_S \frac{R_{BB} + 4R'_S}{\left(1 - \frac{8}{\pi^2}\right) R_{BB} + 4R'_S}. \tag{2.11}$$

We can notice that, when $R_{BB} \to 0$, then $Z_{IN} \to R'_S$, that is R'_S is in parallel with R_{BB}. When $R_{BB} \to \infty$, then $Z_{IN} \to \frac{R'_S}{\left(1-\frac{8}{\pi^2}\right)}$, instead of tending to infinity, because the harmonics at input node dissipate power.

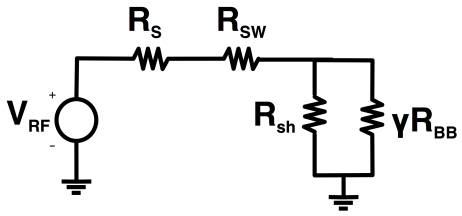

Figure 2.17: LTI equivalent circuit for quadrature passive mixer with R_{sh}, due to harmonics and impedance-transformed R_{BB}.

According to (2.11), the passive quadrature mixer can be modeled using a time invariant circuit model shown in Fig. 2.17, as described in [43]. This circuit accounts for the linear time-varying (LTV) effects of the switches with an impedance transform term γ acting on R_{BB}, and an additional resistance R_{sh}, in shunt with the baseband resistance R_{BB}. R_{sh} is extracted from the charge balance and represents the power lost due to up-conversion by harmonics of the LO through the switches to the antenna and is given by:

$$R_{sh} = R'_S \frac{4\gamma}{1 - 4\gamma} \approx 4.3R'_S, \tag{2.12}$$

where

$$\gamma = 2/\pi^2. \tag{2.13}$$

Note that while R_{sh} is proportional to R'_S in (2.12), this only holds as long as R_S is constant across all frequencies.

In the previous discussion, we defined the up-converted voltage only at the fundamental of LO, or ω_{LO}. However, its stairstep nature seen in Fig. 2.18 indicates

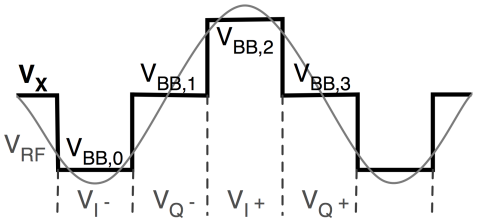

Figure 2.18: Approximation of waveform V_x from Fig.2.15.

that it contains odd harmonics of the LO as well as its fundamental. Therefore the effect of these harmonics on matching has to be analyzed starting by describing V_x in terms of its Fourier series, as explained in Molnar's analysis. We can balance charge flow into and out of each baseband capacitors for each LO cycle. In this case the voltage gain expression is more complex than the previous case and can be extracted by:

$$V_{CG,m} = \frac{R_{BB}}{T_{LO}} \int_{m\,T_{LO}/4-T_{LO}/8}^{(m+1)T_{LO}/4-T_{LO}/8} \left(\frac{V_{RF}}{R'_S\left(\omega_{LO}\right)} - \sum_{n=1,3,5,\ldots}^{\infty} \frac{V_{x,n}}{R'_S\left(n\omega_{LO}\right)} \right) \mathrm{d}t\,. \quad (2.14)$$

In this case the resistance R_{sh} can be expressed as:

$$R_{sh} = \left(\sum_{n=3,5,\ldots}^{\infty} \frac{1}{n^2} \frac{1}{R_S\left(n\omega_{LO}\right) + R_{SW}} \right)^{-1}. \quad (2.15)$$

Thus, we see that in the general case R_{sh} depends upon the antenna impedance at each of the odd harmonics of the LO frequency, and represents the dissipation and/or re-radiation of power due to these harmonics. If we remove the frequency dependence of R_S and perform the summation we find that this impedance is actually equal to the R_{sh} found in (2.12), using the charge balance method. This confirms that the virtual resistance which is used in the LTI model (Fig. 2.17) actually represents the loss due to harmonic re-upconversion and dissipation:

$$R_{sh} = \left(\sum_{n=3,5,\ldots}^{\infty} \frac{1}{n^2} \frac{1}{R_S + R_{SW}} \right)^{-1} = R'_S \frac{4\gamma}{1-4\gamma}. \quad (2.16)$$

This model (Fig. 2.17) for the passive mixer shows that the impedance seen by

the antenna, through a quadrature passive mixer, consists of the parallel combination of R_{sh} and γR_{BB}, in series with the switch resistance R_{SW}; in particular, this impedance becomes:

$$R_{in} = R_{SW} + \gamma R_{BB} || R_{sh}. \tag{2.17}$$

This result indicates that the impedance seen at the antenna interface can be modified by changing R_{BB}. In particular, (2.17) shows that changing baseband resistance can be used to tune the input resistance over a range that is limited by the properties of the mixer: $R_{SW} < R_{in} < R_{SW} + R_{sh}$.

Equation (2.17) implies also that, when antenna impedance R_S is treated as constant and real, and $R_{sh} > R'_S$, an impedance match can always be achieved by choosing R_{BB} such that:

$$R_{BB} = \frac{1}{\gamma} \frac{R_{sh}\, R_S - R_{sh}\, R_{SW}}{R_{SW} + R_{sh} - R_S}. \tag{2.18}$$

So far, we assumed that the source impedance R_S is real; however at input node, especially at frequencies, such as at 60 GHz, there are parasitics capacitances mainly due to the mixer switches and pads and also parasitics inductances due to bonding wires (Fig. 2.19). Therefore, an analysis with complex source impedance $Z_S(\omega)$, instead of R_S, must be taken into account. In this case the passive mixer is modeled using the equivalent circuit, shown in Fig. 2.19, and (2.8) becomes:

$$Z'_S = Z_S(\omega_0) + R_{SW}. \tag{2.19}$$

It is possible to obtain the passive mixer LTI model also in this case, substituting the parameter R_S in the previous expressions with Z_S. The impedance Z_{sh}, which represents the higher harmonics behavior, becomes complex and, following Molnar's analysis, can be expressed as:

$$Z_{sh} = \left(\sum_{n=3,7,11,\ldots}^{\infty} \frac{1}{n^2\, Z'^{*}_S(n\omega_{LO})} + \sum_{n=5,9,13,\ldots}^{\infty} \frac{1}{n^2\, Z'_S(n\omega_{LO})} \right)^{-1}. \tag{2.20}$$

Using the (2.20), the Z_{in} expression extracted by the model in Fig. 2.20 is similar

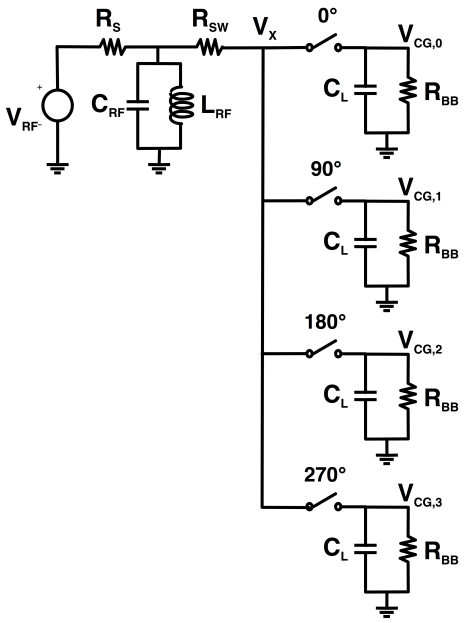

Figure 2.19: Simplified circuit model of 4-phase passive mixer, with RF filter to model the parasitics capacitance.

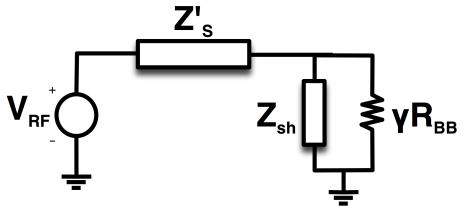

Figure 2.20: LTI equivalent circuit for passive mixer with Z_{sh}, due to RF parasitics capacitance.

to the one in (2.17) and is given by:

$$Z_{in} = R_{SW} + \gamma R_{BB} || Z_{sh}. \tag{2.21}$$

At millimeter wave frequencies, the parasitics capacitances effects can be neglected only at principal harmonic, using a shunt inductance L_{RF} (Fig. 2.20), which resonates with the parasitics capacitance C_{RF} at ω_0. However the parasitics effects are not cancelled at odd harmonics, degrading the mixer performances. In particular, this parasitics capacitances at RF reduce the mixer input impedance, as shown in Fig. 2.21, where the input mixer impedance is plotted when the parasitics capaci-

tances are neglected at RF frequencies or correspond to 10 pF or 100 pF. The same behavior can be noticed for the conversion gain, shown in Fig. 2.22. At 60 GHz,

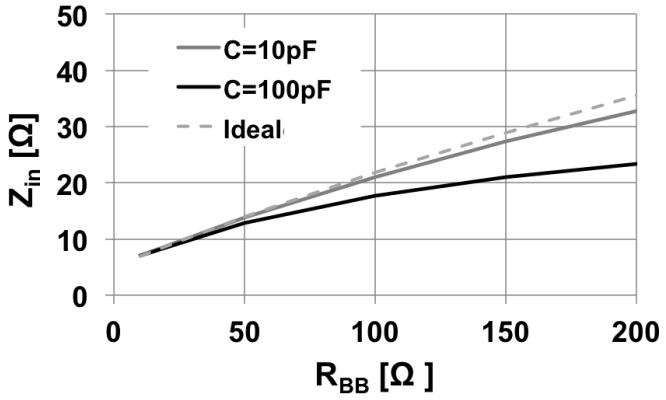

Figure 2.21: Input resonating filter effect on input passive mixer resistance.

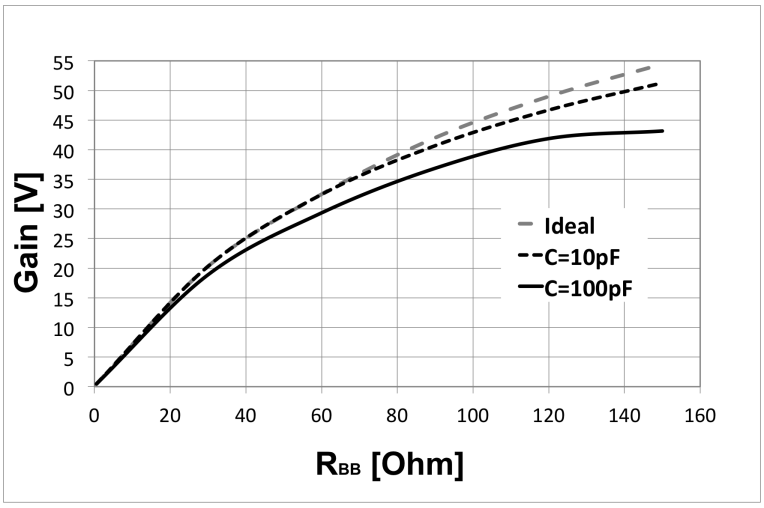

Figure 2.22: Input resonating filter effect on input passive mixer voltage gain.

since C_{RF} is characterized by high values, the approximation $\omega_{LO} C_{RF} R_{SW} \ll 1$ can be introduced in (2.20), obtaining:

$$R_{sh} \approx \frac{4\gamma}{1-4\gamma} R_{SW}, \tag{2.22}$$

$$B_{sh} \approx 0. \tag{2.23}$$

Thanks to this approximation, the impedance Z_{sh} is real and does not depend on

source impedance Z_S, and the mixer matching analysis can be deepened; in fact, exploiting (2.22) and (2.18), the baseband resistance equation can be expressed as:

$$R_{BB} = \frac{4\,R_{SW}\,(R_S - R_{SW})}{R_{SW} - (1 - 8/\pi^2)\,R_S}. \tag{2.24}$$

This result is important, because it means that switch resistance has a lower bound to achieve the mixer matching; in particular:

$$R_{SW} > \left(1 - 8/\pi^2\right) R_S. \tag{2.25}$$

So far a quadrature mixer was analyzed; if a 50% duty-cycle in-phase mixer is considered, the same analysis, shown previous, can be followed, but in this case the voltage V_{RF} has two frequencies components at fundamental harmonic [54]: one at main RF frequency $(\omega_{LO} + \Delta\omega)$ and one at its image frequency $(\omega_{LO} - \Delta\omega)$; this behavior can be modeled adding a shunt resistance R_{imm}, as shown in Fig. 2.23. Following the same analysis used for the quadrature mixer and under the

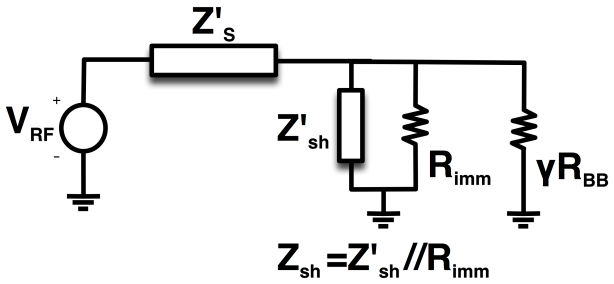

Figure 2.23: Equivalent model to 50% duty-cycle passive mixer.

same assumptions, the Z_{sh} values ($Z_{sh} = Z'_{sh}||R_{imm}$) for this case can be calculated. In particular, when the RF capacitances are neglected, the Z_{sh} impedance can be approximated as:

$$R_{sh} = R'_{sh}||R_{imm} \approx \frac{1}{2}\frac{4\gamma}{1-4\gamma}R'_S||\left(R_{SW} + R'_S\right). \tag{2.26}$$

When the RF capacitances are considered, the Z_{sh} impedance can be approximated as:

$$R_{sh} \approx \frac{1}{2}\frac{4\gamma}{1-4\gamma}R_{SW}||\left(R_{SW} + R'_S\right), \tag{2.27}$$

In Table 2.1 the approximated R_{sh} values are summarized:

R_{sh}	**w/o** C_{RF}	**w/i** C_{RF}
only I	$\frac{1}{2}\frac{4\gamma}{1-4\gamma}R'_S \| \| (R_{SW}+R'_S)$	$\frac{1}{2}\frac{4\gamma}{1-4\gamma}R_{SW} \| \| (R_{SW}+R'_S)$
I/Q	$\frac{4\gamma}{1-4\gamma}R'_S$	$\frac{4\gamma}{1-4\gamma}R_{SW}$

Table 2.1: Approximated R_{sh} values for in-phase and quadrature mixer.

2.3.2 Noise figure analysis

The equivalent band-pass LTI mixer model, given in Fig. 2.17, allows to easily calculate the quadrature mixer NF and Molnar's model can be directly applied [43]. To see this, we first need to look at the various sources of noise in the circuit shown in Fig. 2.15. There are three fundamental sources of noise: the baseband resistance R_{BB}, the switch resistance R_{SW}, and the thermal noise from the antenna itself R_S. As before, we can safely merge the antenna and switch resistance into a single resistor R'_S. To find the total noise, we compute the total noise current injected into the RF and baseband node, and multiply these with the total impedance at those nodes. Thus the corresponding noise currents will be defined as:

$$i^{*2}_{n,BB} = \frac{4k\,T}{\gamma\,R_{BB}}, \tag{2.28}$$

and

$$i^{*2}_{n,S'} = \frac{4k\,T}{R'_S}. \tag{2.29}$$

However the noise down-converted by the mixer at odd harmonics of the LO must be included in the noise calculation and it is given by:

$$i^{*2}_{n,S'} = \frac{4k\,T}{R'_S}. \tag{2.30}$$

The mixer noise schematic can be modeled as shown in Fig. 2.24.

We note that the sum of the antenna noise currents $i^{*2}_{n,S'}\,(n\omega_{LO})$ for $n = 3, 5, 7, \ldots$,

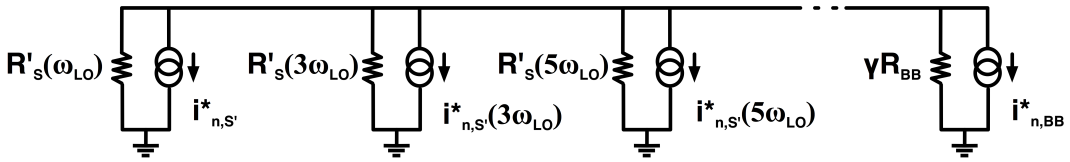

Figure 2.24: Equivalent current noise model to quadrature passive mixer.

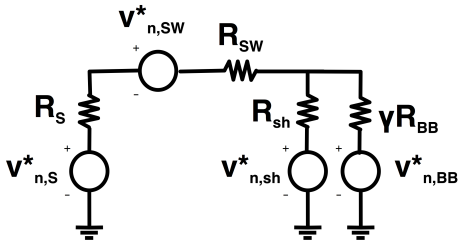

Figure 2.25: Equivalent voltage noise model to quadrature passive mixer.

is exactly the noise that would be generated by R_{sh}, if it was a real resistor. Therefore, we can use also the noise model shown in Fig 2.25 interchangeably. The total noise voltage is the sum of the thermal voltage sources corresponding to each resistor in the circuit. The noise factor for this circuit is found by dividing the total output noise by the portion of that noise caused by the source input noise of R_S:

$$F = 1 + \frac{v_{n,SW}^{*2}}{v_{n,S}^{*2}} + \frac{v_{n,sh}^{*2}}{v_{n,S}^{*2}} \left(\frac{R_S + R_{SW}}{R_{sh}} \right)^2 + \frac{v_{n,BB}^{*2}}{v_{n,S}^{*2}} \left(\frac{R_S + R_{SW}}{\gamma Z_{BB}} \right)^2 . \tag{2.31}$$

The noise factor can be expressed also as:

$$F = 1 + \frac{R_{SW}}{R_S} + \frac{R_{sh}}{R_S} \left(\frac{R_S + R_{SW}}{R_{sh}} \right)^2 + \frac{\gamma R_{BB}}{R_S} \left(\frac{R_S + R_{SW}}{\gamma Z_{BB}} \right)^2 . \tag{2.32}$$

where the second term is given by the switches resistance R_{SW}, the third by the higher harmonics terms represented by the resistance R_{sh} and the last term is given by the baseband resistance R_{BB}.

Replancing (2.12) in (2.32), the noise factor is expressed only as a function of the mixer physical resistances:

$$F = \frac{\pi}{8} \left(1 + \frac{R_{SW}}{R_S} \right) + \frac{(R_S + R_{SW})^2}{\gamma \, R_S \, R_{BB}}. \tag{2.33}$$

Thanks to this expression, it simple to see that if the observation variable is the voltage across the mixer, the noise factor of a power-matched mixer improves decreasing the switches resistance R_{SW} and increasing the baseband resistance R_{BB}.

The minimum noise figure achieved for a quadrature power-matched passive mixer, neglecting the parasitics capacitances, can be calculated imposing the matching condition: the baseband resistance R_{BB} must be equal to

$$R_{BB} = \frac{4\left(R_S^2 - R_{SW}^2\right)}{R_{SW} + \left(16/\pi^2 - 1\right) R_S} \tag{2.34}$$

To obtain the minimum noise factor value, the switches resistance R_{SW} must tend to zero and R_{BB} corresponds to:

$$R_{BB}\Big|_{R_{SW}\to 0} = \frac{4R_S}{\left(16/\pi^2 - 1\right)} \tag{2.35}$$

Introducing (2.35) in (2.32), the minimum NF in voltage mode is equal to 3 dB.

This model neglects the parasitics capacitances, therefore it is valid for low frequencies. If we want to evaluate the NF at millimeter wave, the model with parasitics capacitances must be taken into account (Fig. 2.19), as shown before in the input impedance analysis.

The noise model is the same used in the previous analysis (Fig. 2.25), because obviously the capacitances do not introduce noise, but now the impedances Z_S and Z_{sh} become complex and the voltage noise generator associated with this two impedance can be written as:

$$v_S^{*2} = 4kT\,\mathrm{Re}\left(Z_S\right), \tag{2.36}$$

$$v_{sh}^{*2} = 4kT\,\mathrm{Re}\left(Z_{sh}\right). \tag{2.37}$$

The mixer noise factor can be calculated following the same discussion and under the same assumptions shown in the previous case, using the new noise generator given in (2.36), so that the noise factor can be expressed as:

$$F = 1 + \frac{R_{SW}}{\mathrm{Re}\left(Z_S\right)} + \frac{\mathrm{Re}\left(Z_{sh}\right)}{\mathrm{Re}\left(Z_S\right)}\left|\frac{Z_S + R_{SW}}{Z_{sh}}\right|^2 + \frac{\gamma R_{BB}}{\mathrm{Re}\left(Z_S\right)}\left|\frac{Z_S + R_{SW}}{\gamma Z_{BB}}\right|^2. \tag{2.38}$$

At resonance frequency f_0, the input LC filter allows to have a real source impedance, which corresponds to R_S, and the noise factor can be written as:

$$F = 1 + \frac{R_{SW}}{R_S} + \frac{\mathrm{Re}\,(Z_{sh})}{R_S}\left|\frac{R_S + R_{SW}}{Z_{sh}}\right|^2 + \frac{\gamma R_{BB}}{R_S}\left|\frac{R_S + R_{SW}}{\gamma Z_{BB}}\right|^2. \tag{2.39}$$

If we use the approximation expressed in (2.22), the noise factor is given by:

$$F = 1 + \frac{(R_S + R_{SW})^2}{R_S}\left(\frac{1 - 4\gamma}{4\gamma}\frac{1}{R_{SW}} + \frac{1}{\gamma\, R_{BB}}\right). \tag{2.40}$$

In order to add gain to the receiver and to improve its noise figure, while maintaining the impedance matching functionality through the passive mixer, we have proposed the receiver architecture shown in Fig. 2.26. This receiver consists of a

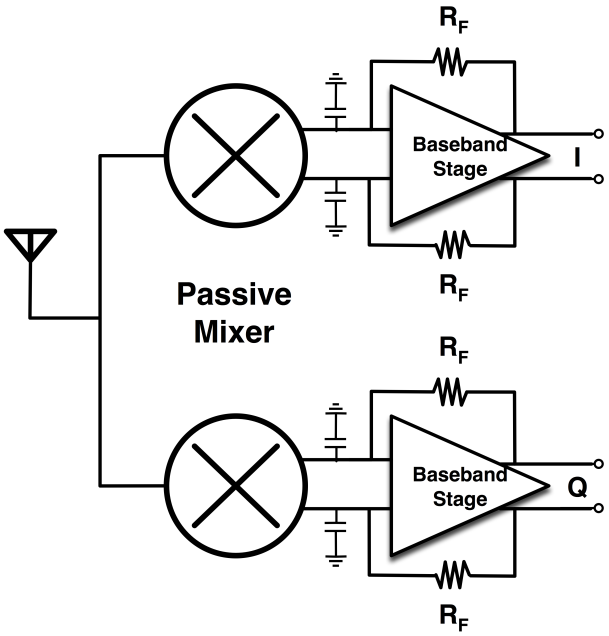

Figure 2.26: Quadrature passive mixer with baseband stage.

passive quadrature mixer, followed by baseband amplifiers in resistive feedback. We find the new effective baseband resistance present on each branch by applying the Miller effect to the feedback resistor R_F:

$$R_{BB} = \frac{R_F}{1 + A} \tag{2.41}$$

Substituting the new R_{BB} expression into the impedance matching, LTI model shows that we can perform impedance matching using the amplifier feedback resistors. Once we have added the feedback amplifiers to implement R_{BB}, the noise performance changes as well. Whereas most of the noise sources in (2.31) can be treated

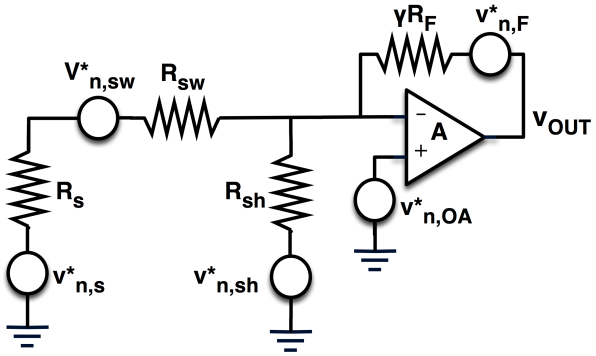

Figure 2.27: Equivalent noise quadrature passive mixer model.

as standard resistive thermal noise, the baseband noise is now due to the feedback resistor and the input referred noise of the amplifier itself. The new noise model, used to calculate the noise factor, is shown in Fig. 2.27: the noise generators taken into account are the source resistance R_S, the switches resistance R_{SW}, the higher harmonics contribution modeled with R_{sh} and the baseband stage. The baseband stage noise is composed by the noise given by the feedback resistance R_F and by the amplifier blocks A. The noise factor, extracted by this model, is given by:

$$F = \frac{4kT\left[(R_S+R_{SW})\left(\frac{V_{out}}{V_{n,S}}\right)^2 + R_{sh}\left(\frac{V_{out}}{V_{n,sh}}\right)^2 + \gamma R_F\left(\frac{V_{out}}{V_{n,F}}\right)^2\right] + \gamma V_{n,OA}\left(\frac{V_{out}}{V_{n,S}}\right)^2}{4kT R_S\left(\frac{V_{out}}{V_{n,S}}\right)^2}. \tag{2.42}$$

In particular:

$$\begin{aligned} F &= 1 + \frac{R_{SW}}{R_S} + \frac{R_{sh}}{R_S}\left(\frac{R_S+R_{SW}}{R_{sh}}\right)^2 + \frac{\gamma R_F}{R_S}\left(\frac{R_S+R_{SW}}{\gamma R_F}\right)^2 \\ &\quad + \frac{\gamma R_{n,OA}}{R_S}\left(\frac{R_S+R_{SW}}{\gamma R_F} + \frac{R_S+R_{SW}+R_{sh}}{R_{sh}}\right)^2. \end{aligned} \tag{2.43}$$

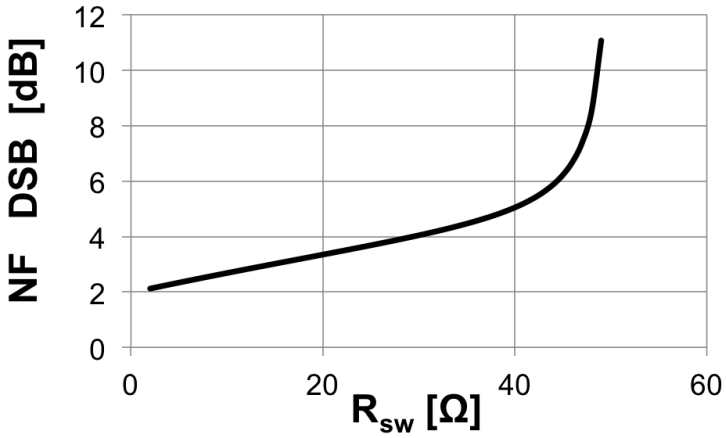

Figure 2.28: NF DSB as a function of switches resistance at low frequencies.

We can note that the γ factor is taken into account both in R_F noise and in the amplifiers noise, because the baseband noise is translated in frequency when it is reflected at the input. Further increasing the R_F value, the noise contributions of the feedback resistance and the amplifier decrease. In Fig. 2.28, the noise figure of a ideal mixer is plotted as a function of switches resistance in matching condition, that is:

$$R_F = \frac{4\left(R_S^2 - R_{SW}^2\right)}{R_{SW} + \left(\frac{16}{\pi^2} - 1\right) R_S} \left(1 + A\right), \tag{2.44}$$

with a $f_{RF} = 100MHz$ (at these frequencies there are not parasitics) and A=30. The minimum NF value in this case corresponds to 2 dB and we can note that the NF increases more quickly when R_{SW} values becomes too high, and that the smaller is the resistance R_{SW}, the better is NF value; therefore there is a upper bound for the switches resistance value.

If we consider also the parasitics capacitances, as shown in Fig. 2.29, the source impedance Z_S and Z_{sh} become complex and the noise voltage generators can be

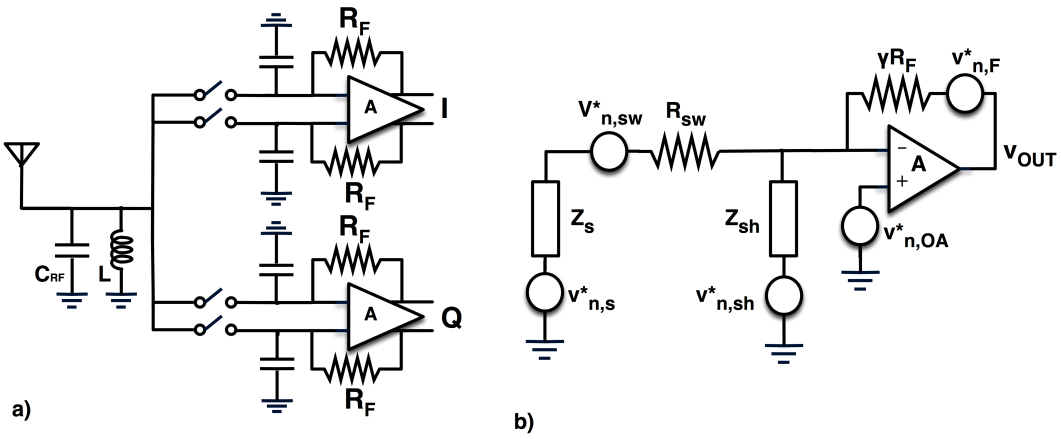

Figure 2.29: a) Quadrature passive mixer with baseband stage with RF parasitics capacitances, b) Equivalent noise quadrature passive mixer model with baseband stage with RF parasitics capacitances.

written as:

$$V*^2_{n,S'} = 4kT\left(\mathrm{Re}\left(Z_S\right)+R_{SW}\right), \tag{2.45}$$

$$V*^2_{n,sh} = 4kT\,\mathrm{Re}\left(Z_S\right), \tag{2.46}$$

$$V*^2_{n,F} = 4kT\,\gamma\,R_F, \tag{2.47}$$

$$V*^2_{n,OA} = 4kT\,\gamma\,R_{n,OA}. \tag{2.48}$$

$$\tag{2.49}$$

Following the same approach explained in the previous case and introducing a resonance filter at fundamental harmonic, the noise factor is given by:

$$\begin{aligned} F &= 1+\frac{R_{SW}}{R_S}+\frac{Re\left(Z_{sh}\right)}{R_S}\left|\frac{Z_S+R_{SW}}{Z_{sh}}\right|^2+\frac{\gamma R_F}{R_S}\left|\frac{Z_S+R_{SW}}{\gamma R_F}\right|^2 \\ &\quad+\frac{\gamma R_{n,OA}}{R_S}\left|\frac{Z_S+R_{SW}}{\gamma R_F}+\frac{Z_S+R_{SW}+Z_{sh}}{Z_{sh}}\right|^2. \end{aligned} \tag{2.50}$$

If the approximation in (2.22) is adopted, the noise factor can be written as:

$$F = 1 + \frac{R_{SW}}{R_S} + \frac{(R_S + R_{SW})^2}{R_S\, R_{SW}} \frac{1-4\gamma}{4\gamma} + \frac{\gamma R_F}{R_S}\left(\frac{R_S + R_{SW}}{\gamma R_F}\right)^2 + \frac{\gamma R_{n,OA}}{R_S}\left(\frac{R_S + R_{SW}}{\gamma R_F} + \frac{R_S}{R_{SW}}\frac{1-4\gamma}{4\gamma} + \frac{1}{4\gamma}\right)^2 . \tag{2.51}$$

In Fig. 2.30, the noise figure of a millimeter-wave mixer is plotted as a function of

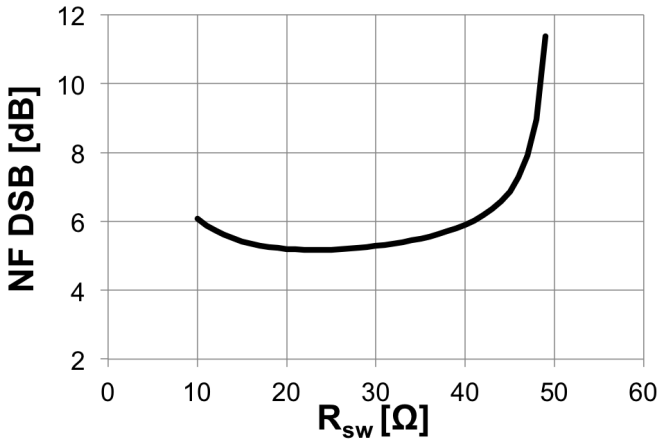

Figure 2.30: NF DSB as a function of switches resistance at millimeter wave.

switches resistance in matching condition, that is:

$$R_F = \frac{4R_{SW}\,(R_S - R_{SW})}{R_{SW} - \left(1 - \frac{8}{\pi^2}\right) R_S}\,(1 + A)\,, \tag{2.52}$$

with a $f_{RF} = 60GHz\,(\omega_{LO} C_{RF}\, R_{SW} \gg 1)$ and A=30. We can notice that the NF is near constant in a range of switches resistance values and increases more quickly when R_{SW} value increases or decreases: therefore there is a R_{SW} optimum to minimize the NF value of a power matched mixer at millimeter wave.

If a 50% duty-cycle in-phase mixer is considered, the previous NF analysis is still valid and the noise factor expressions (2.32) and (2.39) can be still used, substituting the R_{sh} definition given in (2.26) and (2.27) respectively.

2.3.3 Baseband analysis

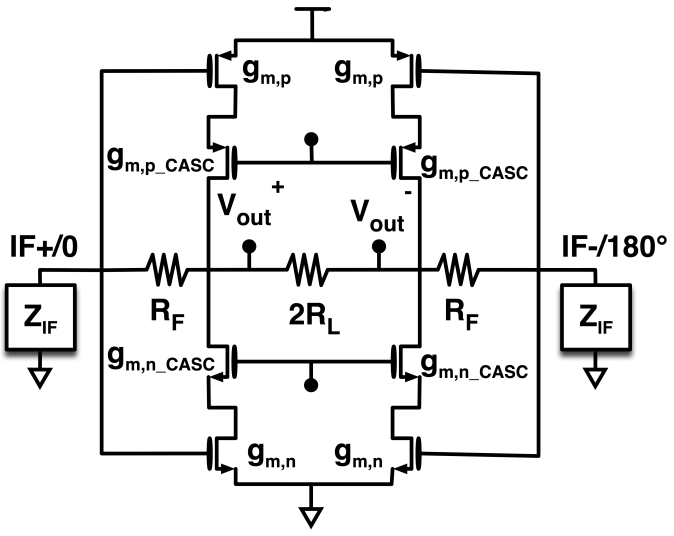

Figure 2.31: Baseband stage schematic.

Now we analyze the baseband noise in detail: the implemented baseband stage is composed by a differential resistive feedback cascode amplifier, which takes advantage of current reuse between the NMOS and PMOS input devices and it was optimized both to provide a low impedance and to have as low output noise as possible (Fig.2.31). To evaluate the baseband voltage gain, an equivalent load impedance R'_L was defined as:

$$R'_L = R_L || \frac{g_{m,p_{CASC}}}{g_{ds,p}\, g_{ds,p_{CASC}}} || \frac{g_{m,n_{CASC}}}{g_{ds,n} g_{ds,n_{CASC}}}. \tag{2.53}$$

The baseband voltage gain (Fig.2.32) can be expressed as:

$$A_{BB} = \frac{R'_L}{R_F + R'_L} \left(1 - g_m\, R_F\right), \tag{2.54}$$

and, using (2.41), the equivalent baseband resistance R_{BB} can be expressed as:

$$R_{BB} = \frac{R_F}{1 + \dfrac{R'_L}{R_F + R'_L} \left(1 - g_m\, R_F\right)}, \tag{2.55}$$

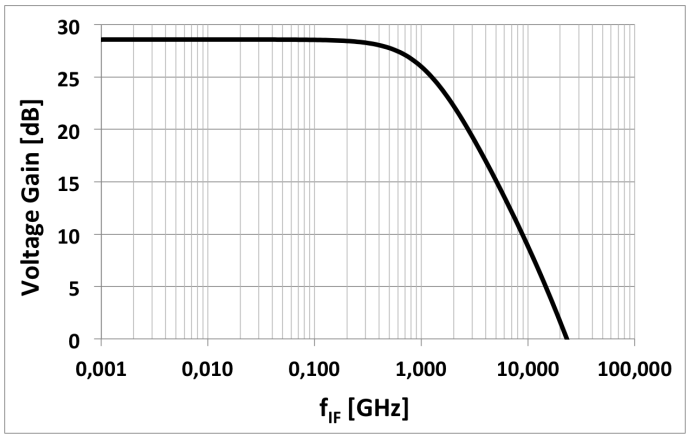

Figure 2.32: Baseband output voltage gain.

Concerning the noise analysis, there are three main noise contributors: the MOS transistors, the feedback resistance R_F and the load resistance R_L. If we consider the voltage noise generators of these elements, the output noises can be calculated as:

$$n_{p-n,MOS} = 4k\,T\,\gamma_{p/n}\,g_{m,p/n}R_{OUT}^2, \tag{2.56}$$

$$n_{R_F} = \frac{4k\,T}{R_F}\left[1+\frac{Z_{IF}}{R_F+Z_{IF}}\left(g_{m,TOT}R_F-1\right)\right]^2 R_{OUT}^2, \tag{2.57}$$

$$n_{R_L} = \frac{4k\,T}{R_L}R_{OUT}^2, \tag{2.58}$$

where Z_{IF} is the impedance seen from the input baseband stage to the RF input and is given by:

$$Z_{IF} = \frac{4\pi^2}{\pi^2-2}R_S \approx 5R_S. \tag{2.59}$$

and

$$g_{m,TOT} = g_{m,p}+g_{m,n}, \tag{2.60}$$

$$R_{OUT} = \frac{R_F}{1+\dfrac{R_F}{R_L'}+g_{m,TOT}\dfrac{Z_{IF}\,R_F}{Z_{IF}+R_F}-\dfrac{Z_{IF}}{Z_{IF}+R_F}}. \tag{2.61}$$

In Table 2.2 the baseband output noise values are reported:

As shown in Fig. 2.33, the main noise contributor is represented by the feedback

$n_{n,MOS}\,[V^2/Hz]$	$n_{n,MOS}\,[V^2/Hz]$	$n_{R_F}\,[V^2/Hz]$	$n_{R_L}\,[V^2/Hz]$
3.9×10^{-18}	3.74×10^{-18}	1.49×10^{-17}	1.035×10^{-19}

Table 2.2: Baseband output noise values.

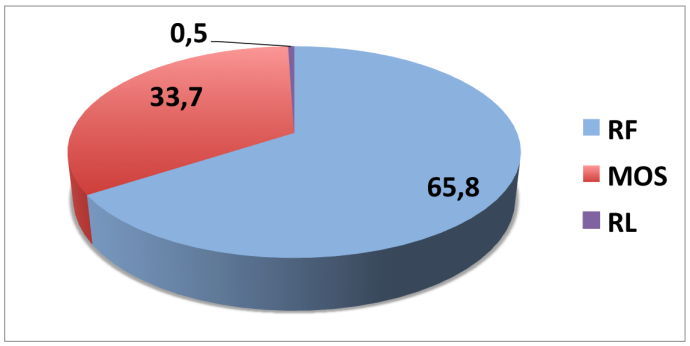

Figure 2.33: Baseband output noise percentage.

resistance R_F, while the load resistance R_L noise can be neglected.

In conclusion, impedance matching imposes an additional constraint for the design of the mixer: the source impedance gives an upper and a lower bound to the possible values of the switches on-resistance. For a given source impedance and switch on-resistance, the baseband impedance is set according to (2.17). This leads to a different trade-off between switch size and NF. In the broadband case with small RF input capacitance, the harmonic shunt impedance is proportional to the total source impedance (R'_S); the NF is still a decreasing function of the baseband trans-resistance/impedance, but, as the baseband impedance is increased, the switch on-resistance must be reduced correspondingly. Furthermore, the finite source impedance/resistance lowers the baseband driving impedance, further increasing the baseband noise transfer function. Still, for small switch resistance a quite good NF is achievable: e.g. for 50 Ω source impedance and 10 Ω switch on-resistance (corresponding to a baseband resistance of about 233 Ω) and a baseband OPAMP equivalent noise resistance of 50 Ω, a NF of 2.7 dB is achievable. On the other hand, as the input capacitance and/or the operating frequency are increased, the NF rises sharply. The resonated solution becomes (eventually) more advantageous. In this case, the switch on-resistance cannot be too low. In fact, the shunt

impedance is proportional to the switches on-resistance and therefore, the lower the switches on-resistance, the higher the baseband noise transfer function. Still, as the switch on-resistance is increased and the baseband impedance reduced correspondingly, the NF tends to degrade due to the lower down-conversion gain. As a result an optimum switch resistance, from 20 to 30 Ω, is found that allows to minimize the NF as a function of the source impedance and of the OPAMP noise resistance (hence of power dissipation).

2.4 Mixer Core Design

The quadrature power-matched mixer has been implemented in the phased-array receiver prototype, as shown in the chapter 3, but also a standalone prototype was implemented to test it (Fig. 2.34). In this last case, the LO signal is generated off-chip and is supplied in phase to the two mixer cores using an on-chip single-ended driven differential coplanar T-line balun (Fig. 2.34).

The mixer parameters were optimized for the case when the mixer is driven in quadrature, indeed when driven by in-phase instead of quadrature LO signals, mixer performances are only slightly degraded: the gain remains within 1 dB and the NF within 0.5 dB. Hence this prototype provides a good estimate of the performances that will be achieved in the integrated receiver.

The choice of the switch dimensions depends on the trade-off between the RF input impedance, needed to realize a wideband matching network, low switch gate capacitance values, to improve the LO tuning range, a low noise figure and the power consumption. Therefore the matching condition imposes (2.52) and to further obtain a wideband, following the (2.7), with $C_{PAD} \approx 50fF$, as in our case, the input mixer impedance corresponds to:

$$R_{in,MIX} < 30\Omega. \tag{2.62}$$

Concerning the NF, observing Fig. 2.28, if R_{SW} decreases again, the NF also increases, but, if R_{SW} decreases, to satisfy the matching condition, the equivalent baseband resistance decreases as the mixer gain and the NF worsens.

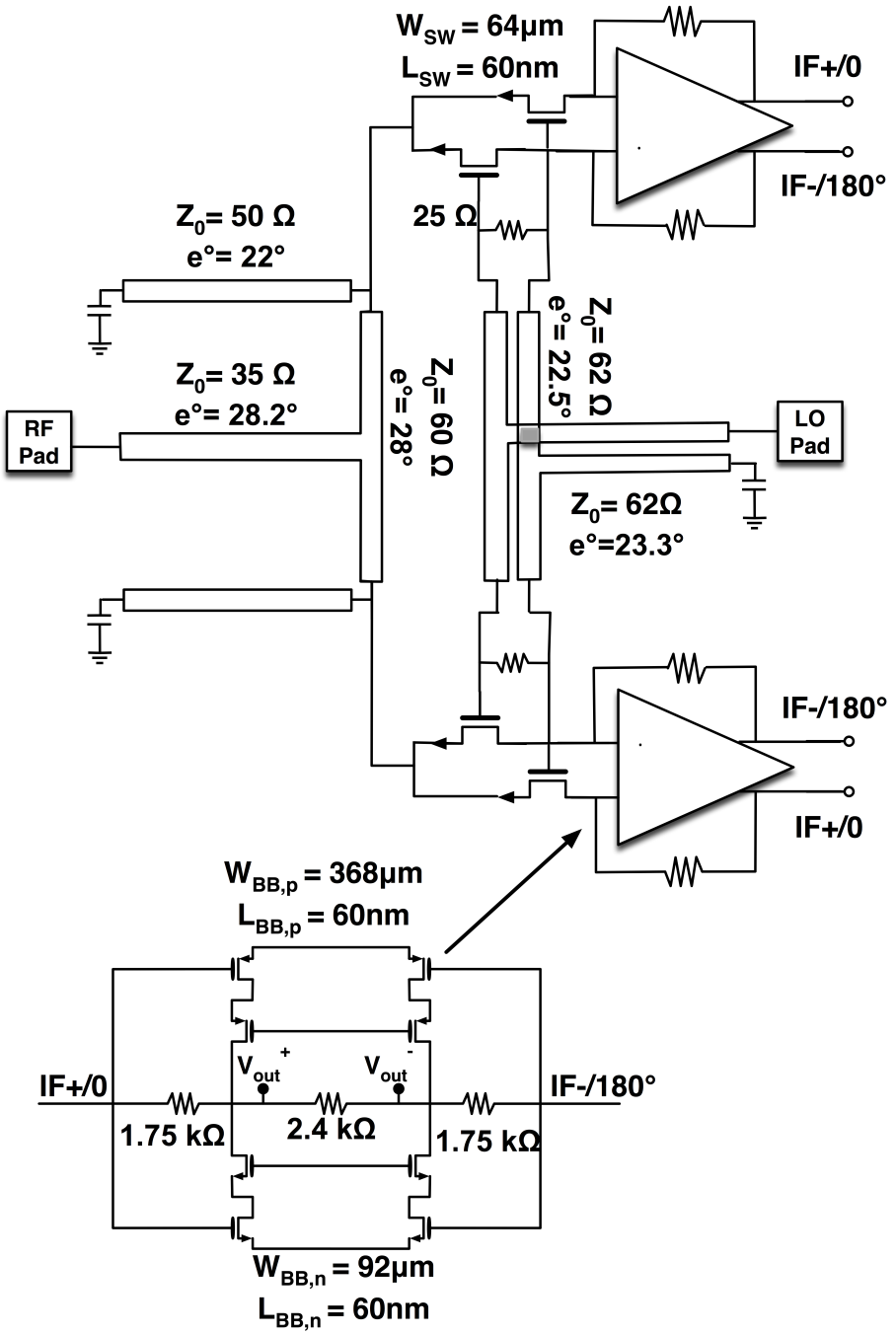

Figure 2.34: Complete mixer schematic.

The minimum noise is obtained when

$$15\Omega \leq R_{SW} < 30\Omega, \tag{2.63}$$

with a $A_{BB} = 30$, which corresponds to the voltage gain of the implemented baseband stage. The R_{SW} and R_F values must be set taking into account these restrictions.

The baseband power consumption depends on the MOS transconductances g_m. Therefore, to reduce the power consumption, the g_m must be reduced, and using the (2.55), we observed that if the g_m value decreases, the R_{BB} value increases. As a consequence, to satisfy the matching condition, the switches resistance must be decreased, but R_{SW} value cannot be lower than 15 Ω, as descents from (2.63). Following these motivations, the R_{SW} value is chosen equal to 20 Ω.

The input matching network replicates the topology in Fig. 2.11 using slow-wave coplanar T-lines, with 3 μm thick Cu top metal and metal level 1 patterned ground shield, which reduces substrate losses with a quality factor near 12. The balun was implemented following the same philosophy used to design the input matching network, with a differential T-line, metal level 1 patterned ground shield, split in two to connect to the two separate coupled switches located about 200 μm apart and with two differential resistances on the switches gate equal to 25 Ω. The differential T-line input is used as single-ended, therefore the input single-ended LO signal is split in two differential LO signals, which drive the switches gates. Both input matching network and balun are characterized by large structures, which increase the parasitics elements; in particular these architectures gives moderate losses of near 3 dB. The balun losses can be embedded when we evaluate the mixer performances, because the mixer is integrated in a direct-conversion receiver and the balun is integrated only in this prototype to test the mixer. The matching network losses instead must be taken into account in the mixer performances; therefore there is a trade-off between the large matching bandwidth and the losses due to achieve it. However, as shown in the next section in the measurements, in spite of the matching network losses the measured gain and noise performances are comparable to the other narrow-band implementations presented in literature.

Each baseband stage (Fig. 2.31 and Fig. 2.34) has a bias voltage of 600 mV on

the IF node and the bias voltage of the PMOS and NMOS cascode are respectively 900 mV and 300 mV. The baseband amplifier is dimensioned to obtain a low output noise, as shown in section 2.3.3, achieving a power consumption of each mixer cores equal to 14 mW.

2.5 Experimental Results

The tested mixer was integrated in a 65nm CMOS technology having 6 metal layers and a 3 μm ultra-thick top metal, occupying a total area of 600×650 μm including pads (Fig. 2.35). The measurement band, from 50 GHz to 67 GHz, is limited on

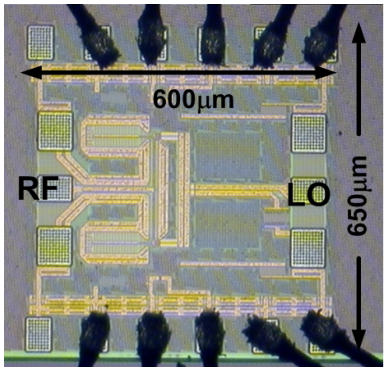

Figure 2.35: Chip microphotograph.

the lower side by the LO amplifier bandwidth and on the upper side by the signal source. The chip was bonded on a printed-circuit board and the principal issue of this test setup (Fig. 2.36) was to generate a good external LO signal, to drive the switches with the proper power level. A power amplifier was used to generate the LO signal; however its bandwidth starts from 50 GHz, therefore the mixer cannot be tested at lower frequencies. Moreover, the power amplifier losses, the coaxial cable and interconnections losses change with the frequency, so the real LO power, which drives the mixer, is not easy to evaluate with precision. At the baseband output two low noise differential amplifiers in cascade were implemented on the board to increase the output gain, in order to evaluate better the noise parameters. The RF input tone was provided to the mixer input using a microprobe and the S-parameters were extracted using a probe station, which works until 67 GHz. Experimental and simulated results are reported in Fig. 2.37 - 2.40, showing good agreement.

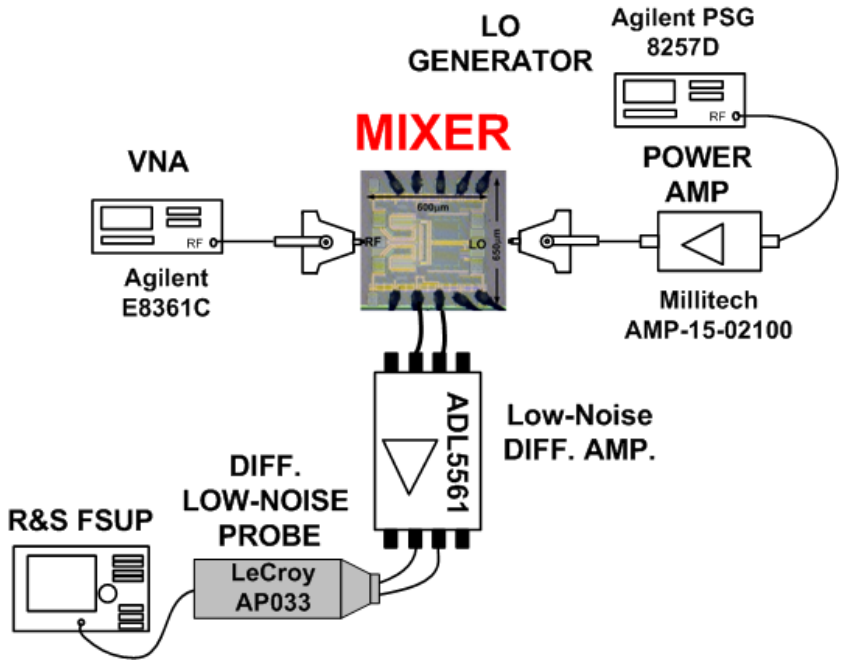

Figure 2.36: Measurement setup to test the in-phase passive mixer.

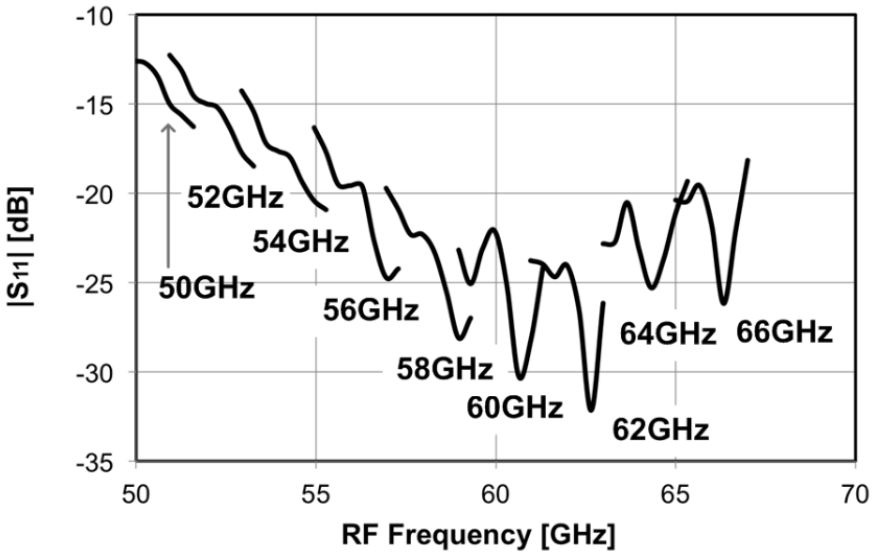

Figure 2.37: Impedance matching: measured s_{11} for different LO frequencies.

Fig. 2.37 reports the measured in-band $|s_{11}|$ as a function of the RF input frequency for different LO frequencies, from 50 GHz up to 67 GHz. The passive mixer must be matched in a narrow band for each LO frequency from 50 to 67 GHz. The $|s_{11}|$ measurements show that, for the LO signal range from 51 to 67 GHz, the RF input in-band $|s_{11}|$ is lower than -12 dB throughout the measured band.

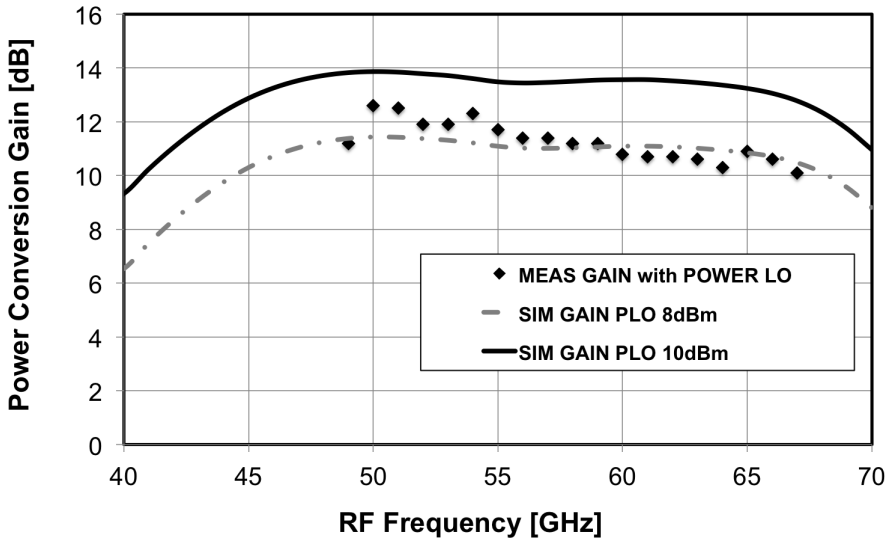

Figure 2.38: Measured and simulated down-conversion gain as a function of LO frequency.

In Fig. 2.38 the down-conversion gain is reported: measured down-conversion gain varies between 10 and 13 dB in the measurement band, because the external LO power decreases, when frequency increases due to the losses of the test bench. This is consistent with a simulated 3-dB RF bandwidth of 28 GHz, with a estimated LO power of 8-10 dBm. Measured and simulated IF bandwidths, including loading from the differential probe used for testing, are about 320 MHz. This is consistent with an unloaded bandwidth above 1.5 GHz. When passive mixer is driven by quadrature instead of in-phase LO signals, gain will improve by 1 dB. The double-sideband (DSB) NF is reported in Fig. 2.39, where NF was measured with the Y-factor method using a 50-75 GHz noise source. The NF varies between 12 and 14 dB in the measurement band, indeed when the LO power decreased due to the losses, the noise increases. We have reported the NF measurement with an estimated LO power between 10 and 12 dBm. When passive mixer is driven by quadrature instead of

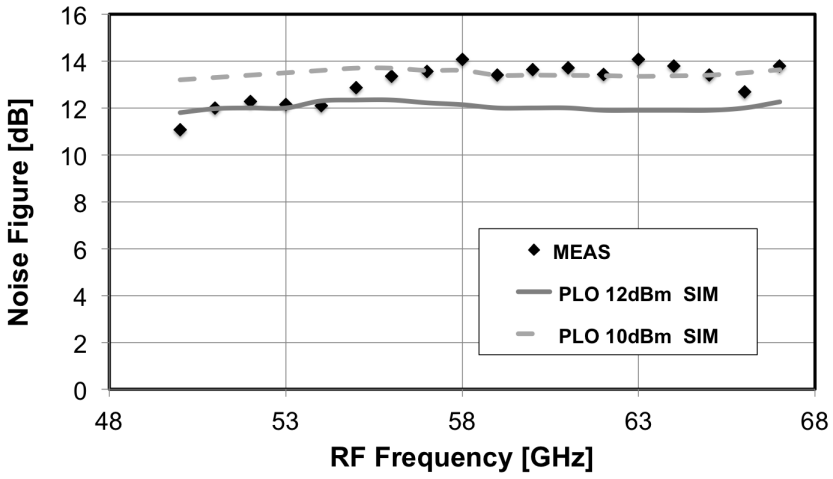

Figure 2.39: Measured and simulated DSB NF as a function of LO frequency for 20 MHz IF.

in-phase LO signals, noise factor will improve by 0.5 dB. Fig. 2.40 reports the NF as a function of the intermediate frequency, where the flicker corner frequency is 5.5 MHz.

Table 2.3 compares the performances of this prototype with other CMOS implementations. Thanks to the wideband matching stage, this design features a remarkably wide RF bandwidth. Power consumption is higher compared with implementations without an active baseband stage (e.g. [55]). This is explained by the fact that the baseband stage consumes considerable power and adds significant noise but it also provides the necessary gain to reduce the impact of noise from the following stages. Thermal noise is comparable to other designs featuring an active topology with the added benefit that this design has higher gain and a reduced flicker noise corner.

2.6 Conclusions

In this chapter a millimeter-wave power-matched passive mixer designed in a standard 65nm CMOS technology has been introduced. Different broadband matching networks have been shown in connection with the design procedure to achieve a

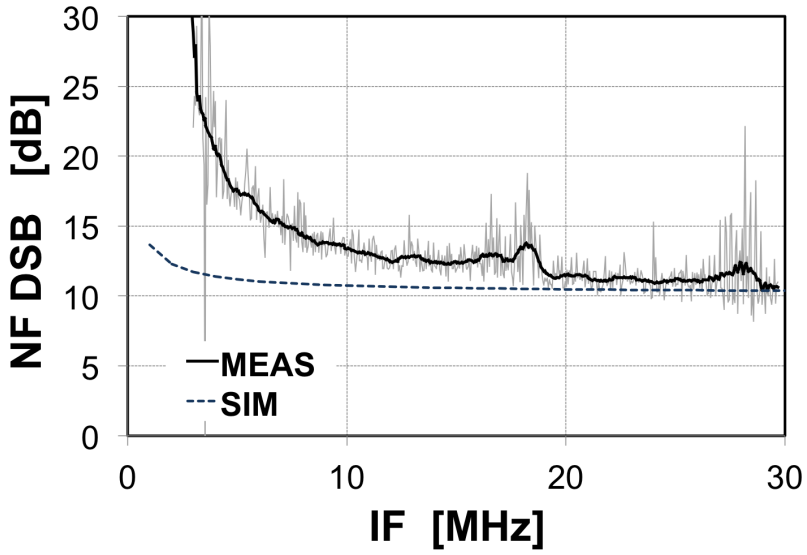

Figure 2.40: NF as a function of the intermediate frequency: experimental data and simulated results.

	This Work	**[53]**	**[55]**
3dB RF BW [GHz]	> 49-67	74-92	55-61
Max Gain [dB]	13	6	-2
NF DSB [dB]	11-14 @ 20 MHz IF	8-10 @ 1 GHz IF	10.8 @ 2 GHz IF
P_{-1dB} **[dBm]**	-12	-	-3.5
Power [mW]	14	45	2.4

Table 2.3: Performance summary and comparison.

broadband matching network with only two inductors. Thanks to this analysis a T-line matching network has been implemented, obtaining a matching bandwidth from 51 to beyond 67 GHz. To design the implemented matching network, the layout parasitics elements had to be estimated with accurate electromagnetic simulations, because they can reduce appreciably the bandwidth. The down-conversion mixer core may be driven by an LNA (directly or through a transconductor stage), or directly by the antenna.

The analyses of the input impedance, gain and noise reported here reveal important features of passive mixer-first receivers. The first is that for quadrature passive mixers using non-overlapping clocks, the input impedance at the RF port of the device is strongly sensitive to the impedance presented to the baseband ports of the mixer, and increasing the baseband resistance acts to increase the apparent RF resistance, allowing for baseband-controlled impedance matching. This method can be expanded with baseband feedback between in-phase and quadrature paths to implement a complex conjugate impedance match at the RF port. A third important point is that the degree to which the baseband impedance can influence the RF impedance depends on re-radiation back through the mixer at higher harmonic frequencies. What holds for impedance also holds for noise, with noise figure depending on both the antenna and baseband impedance, and with increased harmonic shunting degrading this NF.

Finally, the mixer core design has been shown: in particular the mixer has been designed to be driven in quadrature and it was integrated in a direct conversion receiver, driven by a distributed oscillator (chapter 3), but the mixer has been tested standalone and it was driven by an external LO signal given by an integrated differential T-line balun. When driven by in-phase instead of quadrature LO signals, mixer performances are only slightly degraded: the gain remains within 1 dB and the NF within 0.5 dB. Hence this prototype provides a good estimate of the performances that will be achieved in the integrated receiver.

The experimental results show a good agreement with the simulation and the prototype mixer features competitive and stable performances over a broad frequency range from 50 GHz up to 67 GHz.

Chapter 3

Distributed "Hybrid" Wave Oscillator Array

As shown in the first chapter, in millimeter-wave transceivers intrinsic link budget limitations are addressed using phased-array architectures. One of the issues in receiver and transmitter arrays is how to distribute the local oscillator (LO) signal without wasting excessive power. In this chapter we propose an array of coupled distributed oscillators as an efficient way to generate and distribute the LO, as shown conceptually in Fig. 3.1. The idea is that, if oscillators coupling is carried out properly, phase noise can be greatly improved, especially in large arrays [56], and part of the improvement could be traded-off to lower the power dissipation. To support this view, we study the phase noise in distributed oscillators starting from standing-wave and traveling-wave oscillators and then extend the analysis to hybrid-wave and arrays of hybrid-wave oscillators. The analysis is based on the direct calculation of the local impulse sensitivity function (ISF) of noise generators in distributed oscillators. This approach is in our opinion beneficial compared with other approaches previously proposed for the phase noise analysis of distributed oscillators. In [57] the phase noise in rotary traveling wave oscillators (RWO) is analyzed as a superposition of standing-wave oscillators. This approach, based on a linear time-invariant analysis, suffers from limited accuracy and cannot be directly extended to other distributed oscillator topologies (such as the one we have used). In [58] an ISF-based phase noise analysis is presented but the ISF is determined

purely from numerical simulations of a specific oscillator implementation. In order to determine the closed form expression for the ISF we follow the approach based on the system state variables, as reported in [59]. Andreani proposed a state variable normalization method that gives accurate results in sinusoidal multiphase oscillators [60]. As such the technique is limited to arrays of identical oscillators. We observe that this normalization corresponds to an energy-based normalization, i.e. it allows to compute the overall energy as the sum of the square of the state variables. Based on this observation, this normalization technique can be extended to any coupled oscillators and to non-sinusoidal waveforms. In section I a distributed "Hybrid" wave

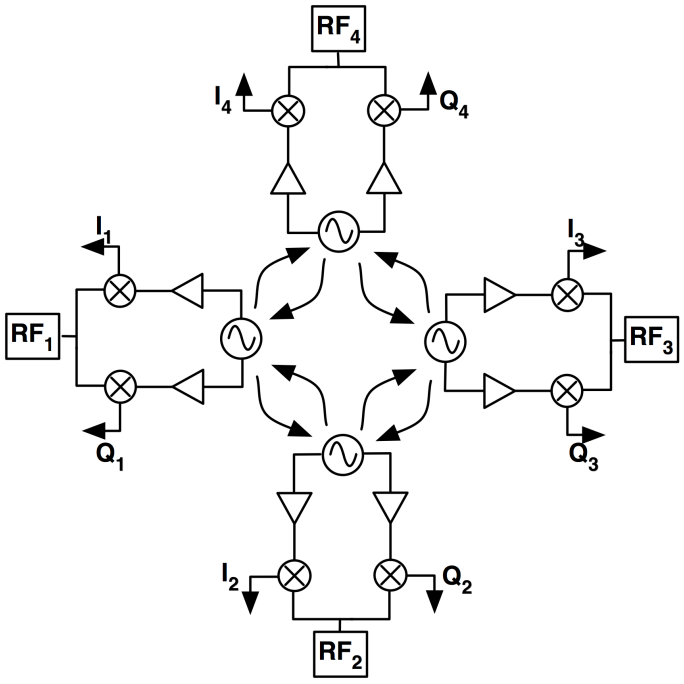

Figure 3.1: Block diagram of a 4 elements phased array direct-conversion receiver with coupled oscillators array for LO generation and distribution.

oscillator array architecture, proposed in [34], and the oscillators coupling technique will be proposed. Section II analyzes the phase noise in distributed oscillators and arrays of distributed oscillators. In section III the design of standing and rotary wave oscillators, which compose the standalone HWO, will be described. The last section deals with the experimental results of the standalone HWO and the HWOs array compared to the simulation.

3.1 Distributed oscillators

A promising approach to distribute the LO signal, originally developed for microprocessor gigahertz-rate clock generation and distribution, makes use of a scalable array of rotary wave oscillators (RWO). In a standalone RWO, a traveling wave distributes the clock around the loop and multiple LO phases are produced by wave propagation delay. As shown in Fig. 3.2, a twisted differential T-line forms a closed loop for the required feedback. Distributed cross-coupled inverters compensate for the loss of the transmission line in order to give a loop gain higher than unity and varactors can be inserted to adjust the frequency of operation. A single RWO is also not suitable since, in a typical phased array, the receiver and transmitter elements are located far away from each other and a single $\lambda/2$ loop is simply not long enough.

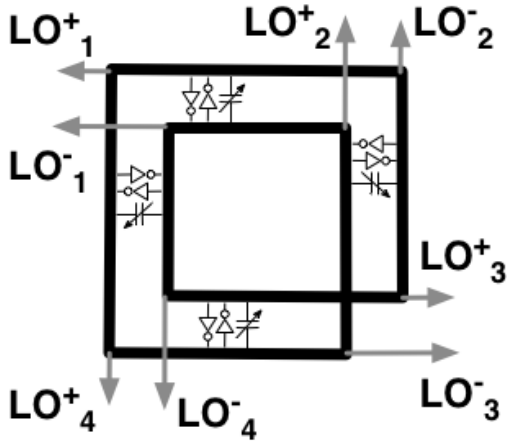

Figure 3.2: Example of a single loop RWO architecture.

A RWO large loop can be used (Fig. 3.3), with a single twisted loop $(2N + 1)\ \lambda/2$ long: 'long' rotary wave oscillator could in principle be made to work at a frequency higher than its fundamental but in practice forcing a millimeter-wave oscillator to work around the desired n-th harmonic is not a trivial task.

More recently, standalone RWOs working at millimeter-wave frequencies have also been reported [65],[66]; however, as shown by this design (Fig. 3.4), an array of millimeter-wave RWOs with the architecture proposed in [33] would result in a rather dense structure, leaving little space for the layout of the other blocks.

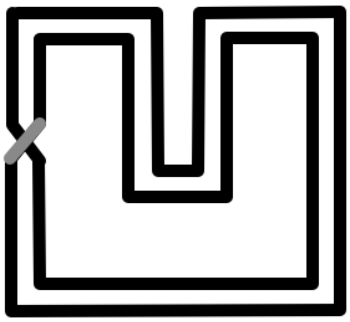

Figure 3.3: Example of a multiple loop RWO architecture.

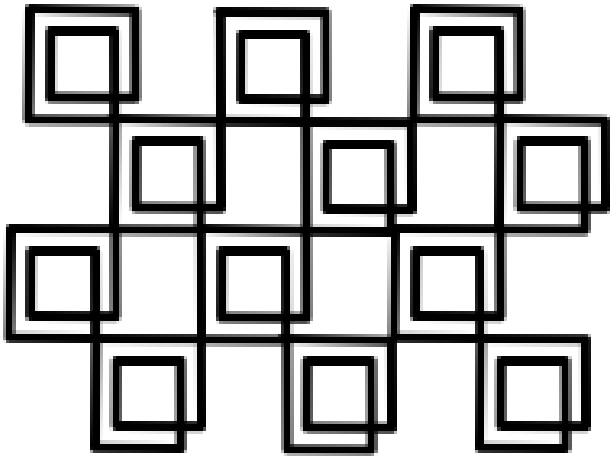

Figure 3.4: Example of a RWO grid architecture.

The starting point for the array architecture proposed in my research activity is the distributed oscillator, similar to the one proposed in [67](Fig. 3.5), and was termed "hybrid" wave oscillator (HWO) since it combines traveling and standing waves, using both rotary and standing wave oscillators. In this design, the core is composed by RWO loop, $\lambda/2$ long, terminated by four standing wave oscillators (SWO), each $\lambda/4$ long.

In our design, we have implemented an oscillator, which not only provides good performances, in terms of phase noise and power consumption, but which also exploits a structure that helps the LO distribution.

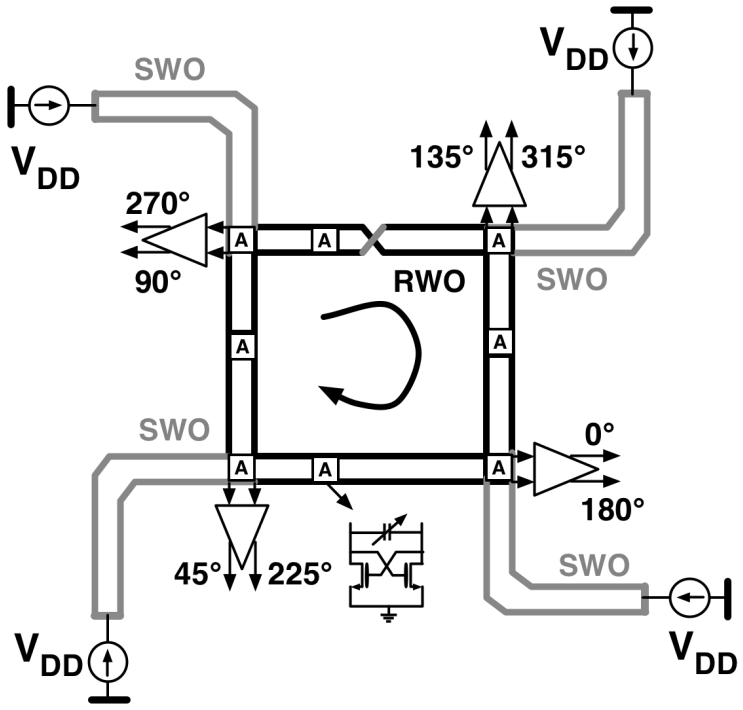

Figure 3.5: Example of a standalone HWO proposed in [67].

The "Hybrid" Wave Oscillator (HWO), which has been designed is shown in Fig. 3.6: the core is composed by RWO loop $\lambda/2$ long and it is terminated by two SWOs, each $\lambda/4$ long, terminated by short circuits. In the RWO a traveling wave distributes the clock around the loop, while the cross-coupled connection provides additional 180° phase shift. At millimeter wave frequencies the use of PMOS transistors for loss compensation along the transmission line (T-line) is discouraged due to the lower cut off frequency and inherent higher capacitive loading. Hence the active elements are only NMOS transistors and the current is supplied through two $\lambda/4$ transmission lines connected on opposite sides of the loop (point A and A' in Fig. 3.6). Distributed cross-coupled inverters compensate for the loss of the transmission line in order to give a loop gain higher than unity and varactors are inserted to adjust the frequency of operation. The quadrature LO signals can be extracted where the RWO and SWO are connected together.

To obtain a large LO distribution architecture, the proposed solution in this work is to couple two or more HWOs to design a N-coupled HWOs phased-array.

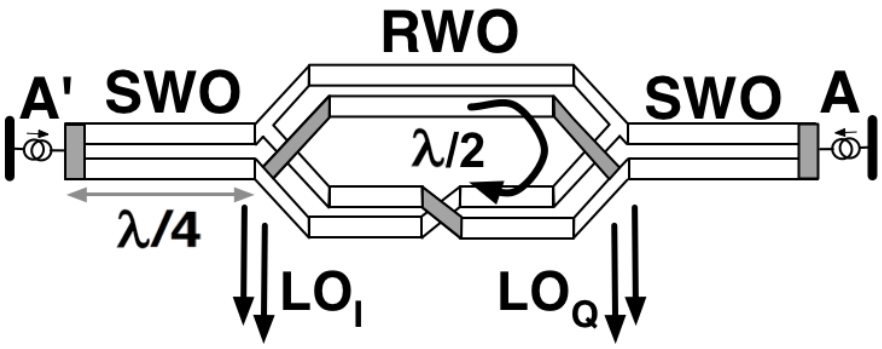

Figure 3.6: Standalone Hybrid Wave Oscillators design.

3.1.1 Oscillator coupling technique

In our work we have combined 4 HWOs to form an array to distribute the LO signal. In a HWO, the forward wave is reflected by the short circuit in B and a backward wave goes from B to A (Fig. 3.7), therefore the standing wave is given by the sum of two waves traveling in opposite directions. The current in the SWO branch is maximum when the voltage is minimum. If two or more identical such oscillators are drawn side by side, they can be strongly coupled without perturbing the resonance frequency by connecting the ends of the $\lambda/4$ T-lines and removing the short circuit termination, as shown in Fig. 3.8. When such a connection is made, a virtual short circuit is formed at the middle points between the two T-lines (B in Fig. 3.8), the forward wave is not reflected anymore and goes from A to A' and it will superimpose with the wave traveling in the opposite direction, forming again a standing wave. Also in this case, the virtual short circuit is formed in point B and the current in the SWO branch is maximum when the voltage is minimum, in particular the voltage is minimum in the virtual short circuit point B. Therefore the SWO T-lines will sustain a standing-wave much in the same way as the standalone HWO.

In the proposed HWO array, each oscillator unit consists of a RWO loop $\lambda/2$ long and two SWO $\lambda/4$ long connected on opposite sides of the loop, as reported in Fig. 3.9. PMOS supply the bias current and the quadrature LO signals can be taken where the RWO and SWO are connected together. Using a coupled oscillator array, there is another advantage, in fact the phase noise improves, as it will be shown in the next section.

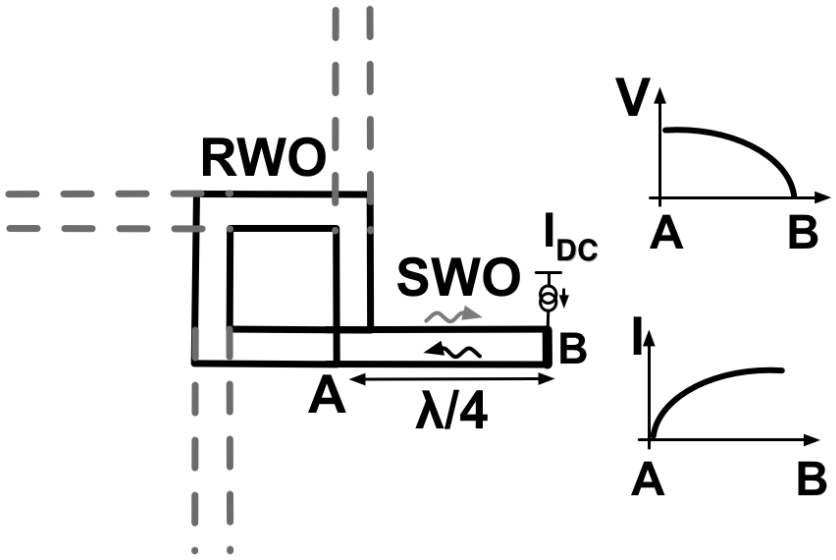

Figure 3.7: Example of a standalone HWO structure.

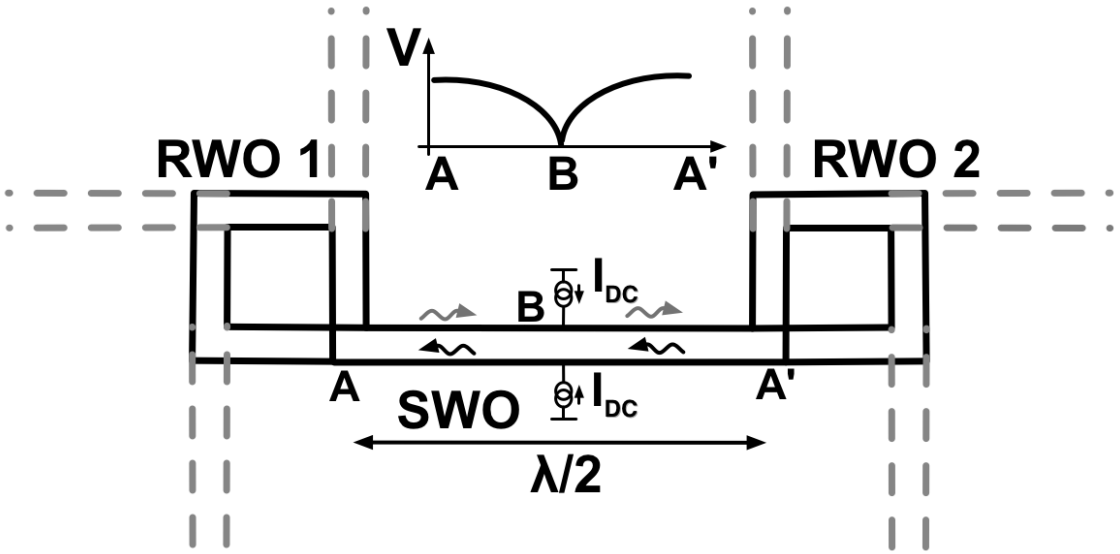

Figure 3.8: Example of two HWOs coupled.

3.2 Distributed oscillators phase noise theory

In this section, oscillators phase noise analysis is presented using the usual definitions of PN and noise contribution. We will first analyze phase noise in standing-wave and the rotary-wave oscillators and then determine the phase noise of the compound

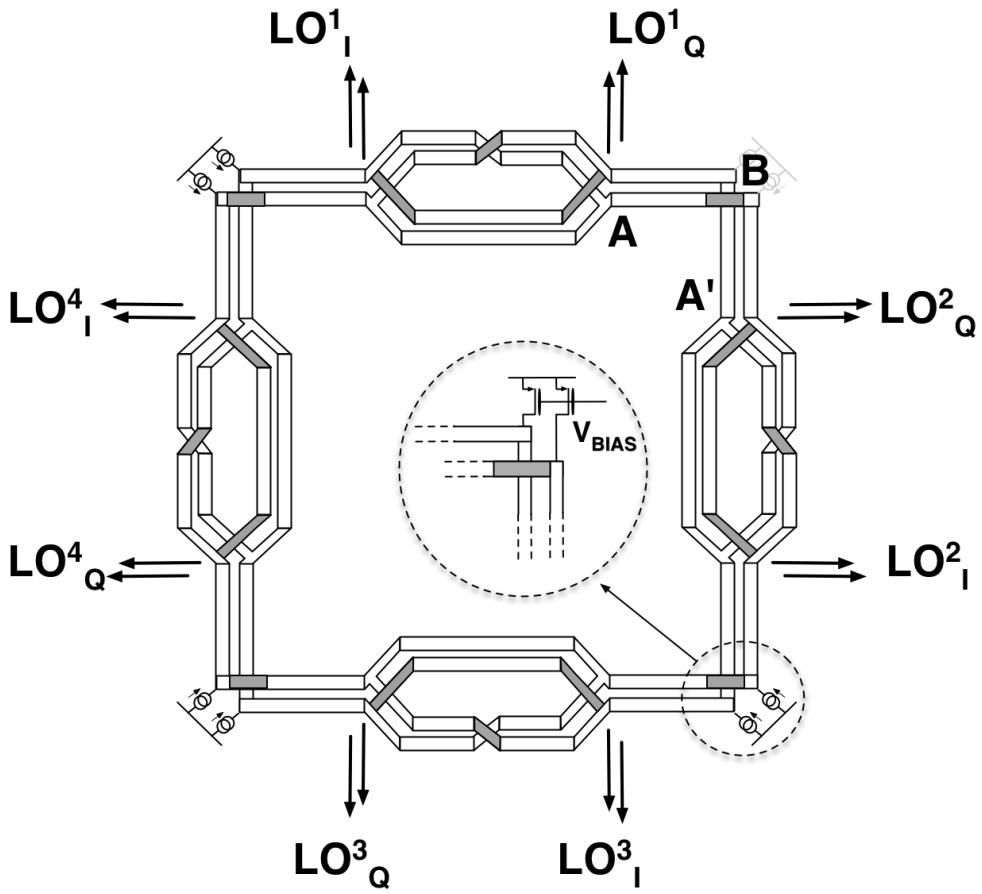

Figure 3.9: Four coupled Hybrid Wave Oscillators array design.

HWO oscillator.

Even though, due to high frequency losses, the phase noise benefit compared with classic LC oscillators is limited, thanks to the distributed nature, quadrature outputs can be easily and efficiently generated. In fact, since RWO exhibit resonance not only at the fundamental but also at its odd harmonics, sharper edges can be obtained with a potential benefit in terms of phase noise for a given power and frequency [57].

3.2.1 Sinusoidal Standing Wave Oscillators

In a standing wave oscillator the oscillation frequency is set by the total delay of the shorted T-line, corresponding to 1/4 of the oscillation period. Theoretically a $\lambda/4$

shorted T-line shows harmonic resonances at the odd harmonics of the fundamental, leading to near square-wave oscillations. However, at millimeter-wave frequencies the impedance at harmonic resonance frequencies is much smaller than the impedance at the oscillation frequency, resulting in a near sinusoidal oscillation. In fact due to the active devices load and to the losses, which increase with frequency since Q is dominated by varactors, achieved waveform can be considered sinusoidal and higher harmonics can be neglected. This aspect is evident looking at Fig. 3.10: the differential input impedance has only a peak at 60 GHz and there are not higher harmonics peaks.

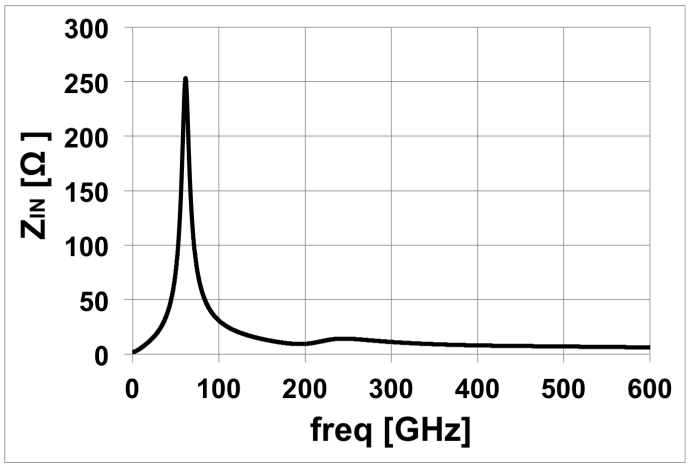

Figure 3.10: T-line input differential impedance.

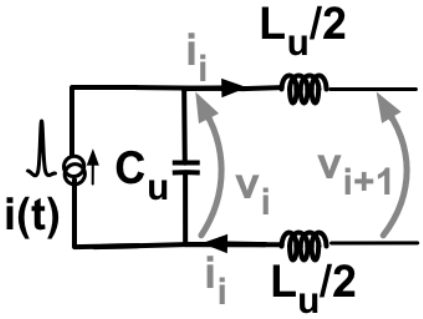

Figure 3.11: T-line cell model.

Each T-line section of the SWO is modeled as a series of N cells, each providing a delay of $\sqrt{LC}$. Using the LC model reported in Fig. 3.11 and neglecting the

NMOS cross-coupled pair capacitance, the system can be described using 2N state variables, representing inductors currents and capacitors voltages. The state vectors are all voltages and are related to the circuit voltages and currents as follows:

$$\begin{cases} x_{2i+1} = v_i, \\ x_{2i} = Z_0\, i_i. \end{cases} \tag{3.1}$$

and the oscillation frequency is given by:

$$\omega_0 = \frac{\pi}{2} \frac{1}{N\sqrt{L_u C_u}}. \tag{3.2}$$

Notice that the total stored energy can be calculated as:

$$E_{tot} = \frac{1}{2} C_u \sum_{i=1}^{N} x_i^2. \tag{3.3}$$

The excess phase due to a charge pulse Δq at node v_i is related to the variation in the state variables as:

$$\Delta\varphi = \omega_0 \Delta x_i \frac{\partial x_i/\partial t}{\left|\partial \boldsymbol{X}/\partial t\right|^2}. \tag{3.4}$$

The step variation in the state variable x_i (Δx_i), when it refers to a node voltage v_i, is equal to $\Delta q/C_u$, where C_u is the node capacitance[63]. We will use this approximation for the sake of simplicity and we will come back to include the effects of the input capacitance later.

Phase noise is generated by the losses in each T-line cell, represented by the parallel conductance G_u, and by the NMOS transistors. According to the time-variant phase noise theory of Lee-Hajimiri [59] the phase noise can be calculated as:

$$\mathcal{L}\left(\Delta\omega\right) = 10 \log\left(\frac{\sum_{i=1}^{N} N_i}{A_0^2/2}\right), \tag{3.5}$$

where A_0 is the input amplitude and N_i is the phase noise contribution of the i-th noise generator in Fig. 3.12 as given by:

$$\mathcal{N}_i = \frac{1}{\left(2C_{TOT}\Delta\omega\right)^2 T_0} \int_0^{T_0} \Gamma_i^2\, \bar{i}_{n,i}^2\, \mathrm{d}t, \tag{3.6}$$

where C_{TOT} is the total T-line capacitance.

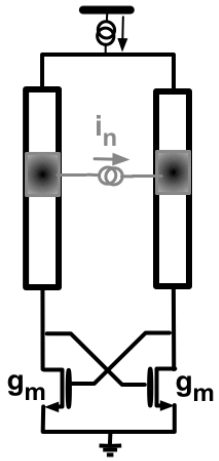

Figure 3.12: Standing wave oscillator model.

The impulse sensitivity function (ISF) Γ_i provides a measure of the phase shift caused by a noise charge impulse Δq applied to the i-th node according to:

$$\Delta\varphi = \frac{\Delta q}{C_{TOT} A_0}\Gamma_i. \tag{3.7}$$

According to (3.7), the ISF is then calculated as:

$$\Gamma_i = N A_0\, \omega_0 \frac{\partial x_i/\partial t}{|\partial \boldsymbol{X}/\partial t|^2}. \tag{3.8}$$

Due to high frequency losses the voltage at the input of the T-line is nearly sinusoidal. The same is not true for all internal nodes since the harmonic terms vary quickly along the T-line, showing nulls and peaks, while the fundamental is monotonically decreasing. Nonetheless, since in absolute terms higher harmonics are relatively small, we approximate the state variables as sinusoidal:

$$\begin{cases} x_{2i+1} \approx A_0 \cos\left(\dfrac{i\pi}{2N}\right)\cos\left(\omega_0 t\right), \\ x_{2i} \approx A_0 \sin\left(\dfrac{i\pi}{2N}\right)\sin\left(\omega_0 t\right). \end{cases} \tag{3.9}$$

The denominator of (3.8) is then given by:

$$|\partial \boldsymbol{X}/\partial t|^2 = \frac{N}{2}\left(A_0\,\omega_0\right)^2. \tag{3.10}$$

Notice that a simple expression results since, with the chosen normalization, the denominator of (3.8) is constant with time. In theory this approach may be inaccurate since it neglects the phase variations caused by noise sources orthogonal to the limit cycle. However, as was shown analytically by Andreani [60] for the case of a single oscillator, with the proper normalization of the state variables the excess phase caused by orthogonal noise sources can be made negligible. The proposed energy-based normalization approach provides accurate results also for the SWO. The closed form expression of the ISF can be derived using the state space vector X. If the state variables are normalized such that the T-line total stored energy is proportional to the sum of the state variables squared (3.3), the resulting ISF expression is

$$\Gamma_i = -2\sin\left(\omega_0 t\right)\cos\left(\frac{i\pi}{2N}\right). \tag{3.11}$$

Notice that this expression is an extension of the result found by Lee-Hajimiri [59] for the sinusoidal LC-tank oscillator ($\Gamma = \sin(\omega_0 t)$) and later extended by Andreani [60] to the case of multiphase LC oscillators ($\Gamma = \sin(\omega_0/N)$). The multiplying factor by 2 is due to the use of C_{TOT} in the definition of Γ, that was adopted here for simplicity in the definition.

The total phase noise contributed by the T-line losses can be calculated as:

$$\mathcal{N}_{T-line} = \frac{4kT/R_{pu}}{\left(2C_{TOT}\Delta\omega\right)^2}\sum_{i=1}^{N}\Gamma_{i,rms}^2 = \frac{2kT/R_{pu}}{\left(C_{TOT}\Delta\omega\right)^2}\sum_{i=1}^{N}\cos^2\left(\frac{i\pi}{2N}\right) \tag{3.12}$$

$$\mathcal{N}_{T-line} = \frac{2kT}{\left(C_{TOT}\Delta\omega\right)^2}\frac{1}{R_T}, \tag{3.13}$$

where $R_T = 2R_{pu}/N$ is the equivalent tank input resistance, accounting for all losses. In fact, the power dissipated by the T-line losses is given by:

$$P_{diss} = \sum_{i=1}^{N}\frac{v_i^2}{2R_{pu}} = \frac{A_0^2}{2R_{pu}}\sum_{i=1}^{N}\cos^2\left(\frac{i\pi}{2N}\right) = \frac{A_0^2}{2R_T}. \tag{3.14}$$

Hence the phase noise due to the T-line losses can be calculated as using the lumped parallel loss resistance $R_T = 2Q/\left(\omega_0 C_{TOT}\right)$ and the associated ISF as given by (3.11) with $i = 0$. The result in (3.13) is similar to what is obtained in an LC-tank oscillator having a parallel loss resistance R_T and a tank capacitance equal to $C_{TOT}/2$.

The phase noise contribution given by the cross-coupled NMOS pair can be calculated reusing the above results and following a similar derivation as reported by Andreani-Mazzanti in [61]. Under the same assumptions as in [61], essentially transistors working in off or saturation region, thermal noise current spectral density given by $4kT\gamma_{NMOS}g_m(t)$ and sinusoidal oscillation voltage, and using the ISF as derived above ($\Gamma_{NMOS} = \Gamma_0$) it can be shown that:

$$\mathcal{N}_{T-line} = \frac{2kT}{\left(C_{TOT}\Delta\omega\right)^2}\frac{\gamma_{NMOS}}{R_T}. \tag{3.15}$$

In order to derive a more convenient phase noise expression, we recall that, using (3.3), the stored energy is $E_{TOT} = C_{TOT}A_0^2/4$ and we can express the quality factor Q as a function of energy stored and power dissipation ($Q = \omega_0 E_{TOT}/P_{diss}$). It may also be convenient to express the power dissipated by the tank with respect to the power drawn from the supply:

$$P_{DC} = \frac{P_{diss}}{\eta_P}, \tag{3.16}$$

where η_P is the oscillator DC to RF power conversion efficiency from the supply to the resonator.

Now the total phase noise can be expressed as a function of the dissipated power and the quality factor and it is given by:

$$\mathcal{L}_{SWO}\left(\Delta\omega\right) = 10\log\left[\frac{2kT}{P_{DC}}\frac{1+\gamma_{NMOS}}{\eta_P}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]. \tag{3.17}$$

The expression is exactly identical to that of an LC-tank oscillator. In Fig. 3.13 the phase noise T-line and total SWO, as a function of supply current, is simulated and calculated. We can observe that there is a good agreement between the PN calculations and simulations concerning T-line phase noise. As regards SWO phase noise, the calculated phase noise for high current values has a slight mismatch respect to simulated phase noise, because the MOS for high supply current work in

voltage limited region, but the assumptions for the MOS phase noise calculation are valid in current limited region. In the NMOS cross-coupled pair the differential

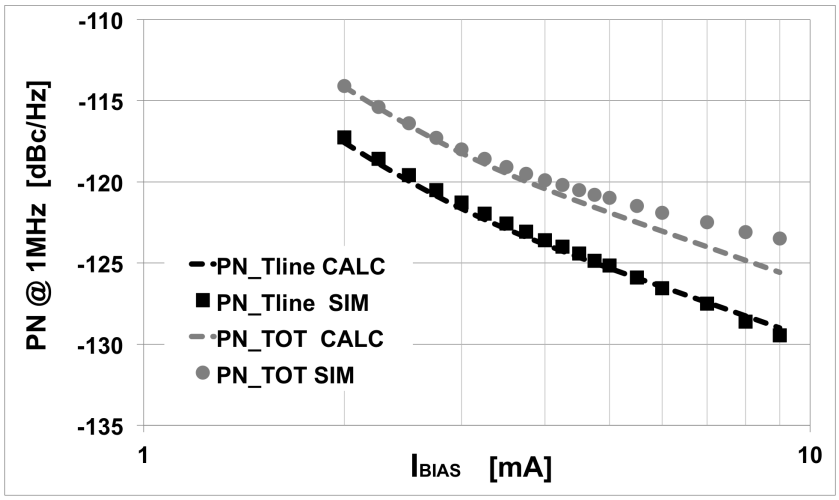

Figure 3.13: Simulations and calculations of T-line SWO and total SWO phase noise.

output current is well approximated as a square wave with 50% duty-cycle and the resulting DC to RF current conversion efficiency is $4/\pi$. The power efficiency is then essentially a function of the oscillation amplitude. (3.17) then explains why in a standing-wave oscillator it is advantageous to concentrate the negative resistance at the input of the T-line instead of distributing it along the line as in a RWO. In fact, the oscillation amplitude is maximum in that point, which translates into a maximum power efficiency η_P and therefore into a better phase noise for a given power dissipation. As the oscillation amplitude increases and the transistors enter, for a fraction of the period, into the triode region, the current conversion efficiency decreases and the NMOS contribute more noise than predicted by (3.15), eventually determining an optimum in the phase noise.

At millimeter-wave frequencies capacitive loading results in significant 'line shortening' and cannot be neglected. As will be shown, the effect of line shortening is to change the oscillation frequency for a given T-line length. However, the phase noise as expressed in (3.17) remains valid. In fact, using the T-line model shown before with N delay cells and describing the oscillator as a system whose state vector X consists of $2N + 1$ state variables (3.1), the first state variable x_0 is given by the voltage across the parasitic capacitor multiplied by the square root of the ratio

C_{PAR}/C_u, while the remaining 2N variables represent the T-line capacitor voltages and inductors currents, multiplied by the characteristic impedance Z_0. Approximating the input voltage as a sinusoid of amplitude A_0, the resulting state vector is given by:

$$\begin{cases} x_0 \approx \sqrt{N}_0 A_0 \cos(\omega_0 t), \\ x_{2i} \approx A_0' \cos\left[\dfrac{\pi(N_0+i)}{2(N+N_0)}\right] \cos(\omega_0 t), \\ x_{2i+1} \approx A_0' \sin\left[\dfrac{\pi(N_0+i)}{2(N+N_0)}\right] \sin(\omega_0 t), \end{cases} \tag{3.18}$$

$$A_0' = \frac{A_0}{cos\left(\dfrac{N_0\pi}{2N}\right)}, \tag{3.19}$$

with $N_0 = C_{PAR}/C_u$. We can use again (3.3) and (3.8) to calculate energy and ISF associated with noise generators in parallel with capacitors. Notice that, when calculating Γ_0, the state variable step Δx_0 is $\sqrt{N}_0 \Delta v_0$ and that the local capacitance is C_{PAR}, or N_0 times C_u. If the parasitic capacitance is small ($N_0 << N$), we have that $A_0' \approx A_0$ and the denominator of (3.4) is well approximated as:

$$|\partial \boldsymbol{X}/\partial t|^2 = \frac{N+N_0}{2}(A_0\omega_0)^2 \tag{3.20}$$

and the ISF associated with the noise generators in parallel with each capacitor is given by:

$$\Gamma_i = -\frac{2N}{N+N_0}\sin(\omega_0 t)\cos\left[\frac{\pi(N_0+i)}{2(N+N_0)}\right]. \tag{3.21}$$

The total phase noise contribution due to the T-line is then calculated as:

$$\begin{aligned} \mathcal{N}_{T-line} =& \frac{4kTN_0/R_{pu}}{(2NC_u\Delta\omega)^2}\Gamma_{0,rms}^2 + \frac{4kT/R_{pu}}{(2NC_u\Delta\omega)^2}\sum_{i=1}^{N}\Gamma_{i,rms}^2 \\ =& \frac{2kT/R_{pu}}{((N+N_0)C_u\Delta\omega)^2}\left[N_0 + \sum_{i=1}^{N}\cos^2\left[\frac{(N_0+i)\pi}{2(N+N_0)^2}\right]\right], \end{aligned} \tag{3.22}$$

$$\mathcal{N}_{T-line} = \frac{2kT}{((N+N_0)C_u\Delta\omega)^2}\frac{1}{R_T'}, \tag{3.23}$$

with

$$R'_T = \frac{2R_{pu}}{(N+N_0)}. \tag{3.24}$$

Hence (3.13) and (3.14) still apply provided that we substitute C_{TOT} with $C_{PAR} + NC_u$ and R_T with R'_T.

If the SWO is designed to operate at lower frequencies, a non-sinusoidal oscillation amplitude is expected. Our approach can be easily extended to the case of non-sinusoidal oscillations by modifying the waveform expressions used in the derivation of the ISF. Given that the stored energy remains constant over time, a constant factor in the denominator of the ISF will be found also when higher harmonics are accounted. However the ISF also becomes non-sinusoidal, leading to phase noise conversion from the higher harmonics of the noise generators [59]. The resonator noise contribution should be calculated to account for the fact that in general the quality factor is frequency dependent. This is also very important to consider when deriving an expression for phase noise as a function of power since the expression of Q as a function of energy and power dissipation should be used instead of the definition based on narrow-band impedance.

3.2.2 Sinusoidal Rotary Wave Oscillators

In the Rotary Wave Oscillator, a traveling wave propagates around the $\lambda/2$ loop. Assuming that there is only one wave propagating in one direction (methods to ensure this condition will be discussed in the next section), the voltage (current) at the input of each cell is equal to the voltage (current) at the input of the previous cell delayed by $\sqrt{(L_u C_u)}$. In a millimeter-wave RWO, with losses strongly increasing with frequency, the traveling wave is well approximated by a sinusoid:

$$\begin{cases} v_i \approx A_0 \cos\left(\omega_0 t - \dfrac{i\pi}{N}\right), \\ i_i \approx \dfrac{A_0}{Z_0} \cos\left(\omega_0 t - \dfrac{i\pi}{N}\right), \end{cases} \tag{3.25}$$

with the oscillation frequency given by:

$$\omega_0 = \frac{\pi}{N\sqrt{L_u C_u}}. \tag{3.26}$$

Using the same notations as in (3.5) and (3.7), we can describe the system using a state vector with 2N variables where again the state variables are normalized such that the T-line total stored energy is proportional to the sum of the state variables squared ($E = k\sum_i x_i^2$).

Modeling each T-line section of the RWO using the LC model reported in Fig. 3.11, as for the SWO, the system can be described using 2N state variables, representing inductors currents and capacitors voltages as given by (3.25). The state vectors are all voltages and are related to the circuit voltages and currents using (3.1) and the total stored energy can be calculated again using (3.3). Thanks to the expression in (3.4), (3.8), the ISF can be calculated as:

$$|\partial \boldsymbol{X}/\partial t|^2 = N\left(A_0\omega_0\right)^2, \tag{3.27}$$

and the ISF associated with the noise generators in parallel with each capacitor is given by the simple sinusoid in quadrature with the capacitor voltage:

$$\Gamma_i = -\sin\left(\omega_0 t - \frac{i\pi}{N}\right). \tag{3.28}$$

As expected from the symmetry and differently from the SWO, all the cells contribute equally to the overall phase noise.

The total phase noise contributed by the T-line losses can be calculated as:

$$\mathcal{N}_{T-line} = N\Gamma_{rms}^2 \frac{4kT/R_{pu}}{\left(2C_{TOT}\Delta\omega\right)^2} = \frac{kT}{\left(C_{TOT}\Delta\omega\right)^2}\frac{1}{2R_p}, \tag{3.29}$$

where $R_P = R_{pu}/N$ is the equivalent parallel loss resistance, accounting for the losses along the whole T-line. In fact, the power dissipated by the T-line losses is given by:

$$P_{diss} = \sum_{i=1}^{N} \frac{v_i^2}{2R_{pu}} = \frac{A_0^2}{2R_p}. \tag{3.30}$$

Hence the phase noise due to the T-line losses can be calculated as using the lumped parallel loss resistance $R_P = Q/\left(\omega_0 C_{TOT}\right)$ and the associated ISF as given by (3.28) with i=0. Following the same discussion in the previous sub-section and under the same assumptions, the phase noise contribution of the MOS transistors

can be calculated also in this case as:

$$\mathcal{N}_{NMOS} = \frac{kT}{\left(C_{TOT}\Delta\omega\right)^2}\frac{\gamma_{NMOS}}{2R_p}. \tag{3.31}$$

In order to derive a more convenient phase noise expression, we recall that, based on (3.28), the stored energy is $E_{TOT} = C_{TOT}A_0^2/2$ and we express the quality factor Q as a function of energy stored and power dissipation ($Q = \omega_0 E_{TOT}/P_{diss}$). Now using (3.29), (3.31) and (3.16) the total phase noise of the RWO can be calculated as:

$$\mathcal{L}_{RWO}\left(\Delta\omega\right) = 10\log\left[\frac{2kT}{P_{DC}}\frac{1+\gamma_{NOMS}}{\eta_P}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]. \tag{3.32}$$

3.2.3 Hybrid Wave Oscillator

As shown in the two previous subsections, from a theoretical point of view, the achievable phase noise in RWOs and SWOs, for given oscillation frequency, power dissipation and loaded quality factor of the T-lines, is essentially the same and corresponds to the same FoM of an LC oscillator having the same tank quality factor. When one RWO and two SWO are connected we can still use the same approach as before to derive the ISF and calculate the overall phase noise. Notice that, since the two oscillators have the same FoM, we expect the HWO to also retain the same FoM. For the same T-line design parameters, the SWO has 1/4 the power dissipation and 6 dB higher phase noise than the RWO. Based on coupled oscillators theory, when a RWO and two SWO are coupled, as in the proposed HWO, thanks to the synchronization, close-in phase noise is expected to be $10\log 6$ or 7.8 dB better than in a single SWO [56]. Following the same approach used to study the phase noise of SWO and RWO, we describe the system using a state vector. It is convenient to segment the vector as follows:

$$X_{HWO} = \begin{bmatrix} X_{SWO1} \\ X_{RWO} \\ X_{SWO2} \end{bmatrix}, \tag{3.33}$$

where $X_{SWO1,2}$ and X_{RWO} are defined as specified in (3.1) referring respectively to SWO1, SWO2 and RWO. Since the T-line unitary cells in SWO1, 2 and RWO are

assumed all equal here, no further normalization is necessary. If this was not the case we should have scaled each variable x_i proportionally with the square root of the associated cell capacitance. We compute the overall phase noise as a sum of the contribution of SWOs and RWO:

$$\mathcal{L}_{RWO}\left(\Delta\omega\right) = 10\log\left[\frac{N_{SWO1} + N_{RWO} + N_{SWO2}}{A_0^2/2}\right], \tag{3.34}$$

where A_0 is the oscillation amplitude at the input of SWO1, 2 and along the RWO.

The phase noise contribution associated with the i-th noise generator of the SWO can be calculated as:

$$\mathcal{N}_{L-SWO,i} = \frac{1}{\left(2C_{SWO}\Delta\omega\right)^2 T_0}\int_0^{T_0}\Gamma_{SWO,i}^2\,\overline{i^2}_{n-SWO,i}\,\mathrm{d}t, \tag{3.35}$$

where the ISF is defined by the following relations:

$$\Delta\varphi = \frac{\Delta q}{C_{SWO}A_0}\Gamma_{SWO,i}, \tag{3.36}$$

$$\Delta\varphi = \omega_0\frac{\Delta q}{C_u}\frac{\partial x_i/\partial t}{\left|\partial \boldsymbol{X}_{HWO}/\partial t\right|^2}. \tag{3.37}$$

From the above definition it follows that:

$$\Gamma_{SWO,i} = \mathcal{N}_{SWO}A_0^2\,\omega_0\frac{\Delta q}{C_u}\frac{\partial x_i/\partial t}{\left|\partial \boldsymbol{X}_{HWO}/\partial t\right|^2}, \tag{3.38}$$

where $N_{SWO}\,(= C_{SWO}/C_u)$ is the number of cells in the RWO. Similarly, the phase noise contributions of the RWO can be calculated using:

$$\mathcal{N}_{L-RWO,i} = \frac{1}{\left(2C_{RWO}\Delta\omega\right)^2 T_0}\int_0^{T_0}\Gamma_{RWO,i}^2\overline{i^2}_{n-RWO,i}\,dt, \tag{3.39}$$

where the ISF is defined by the following relations:

$$\Delta\varphi = \frac{\Delta q}{C_{RWO}A_0}\Gamma_{RWO,i} \tag{3.40}$$

where φ is still defined by (3.37). From the above definition it follows that:

$$\Gamma_{RWO,i} = \mathcal{N}_{RWO} A_0^2 \omega_0 \frac{\Delta q}{C_u} \frac{\partial x_i/\partial t}{\left|\partial \boldsymbol{X}_{HWO}/\partial t\right|^2}, \tag{3.41}$$

where $N_{RWO}\,(= C_{RWO}/C_u)$ is the number of cells in the RWO. It is easy to show that the denominator in (3.38) and (3.41) is given by:

$$\left|\partial \boldsymbol{X}_{HWO}/\partial t\right|^2 = 2\left[\frac{\mathcal{N}_{SWO}}{2}\left(A_0\omega_0\right)^2\right] + \mathcal{N}_{RWO}\left(A_0\omega_0\right)^2. \tag{3.42}$$

Having assumed all the cells to be equal to $N_{RWO} = 2N_{SWO}$, hence

$$\left|\partial \boldsymbol{X}_{HWO}/\partial t\right|^2 = \frac{3}{2}\mathcal{N}_{RWO}\left(A_0\omega_0\right)^2. \tag{3.43}$$

From (3.38) and (3.43) and using the wave solution in (3.9), it is immediate to calculate the SWO ISFs:

$$\Gamma_{SWO,i} = -\frac{1}{3}\sin\left(\omega_0 t\right)\cos\left(\frac{i\pi}{2\mathcal{N}_{SWO}}\right). \tag{3.44}$$

Plugging (3.44) into (3.35) and considering both NMOS and T-line loss noise generators it is immediate to show that:

$$\mathcal{N}_{L-SWO} = \frac{kT}{\left(C_{SWO}\Delta\omega\right)^2}\frac{1+\gamma_{NMOS}}{18R_T}, \tag{3.45}$$

with $R_T = 2Q/\left(\omega_0 C_{SWO}\right)$. From (3.41) and (3.43) we compute the ISF for the RWO:

$$\Gamma_{RWO,i} = -\frac{2}{3}\sin\left(\omega_0 t - \frac{i\pi}{2\mathcal{N}_{RWO}}\right). \tag{3.46}$$

Plugging (3.46) into (3.35) and considering both NMOS and T-line loss noise generators it is immediate to show that:

$$\mathcal{N}_{L-RWO} = \frac{2}{9}\frac{kT}{\left(C_{RWO}\Delta\omega\right)^2}\frac{1+\gamma_{NMOS}}{R_P}, \tag{3.47}$$

with $R_P = Q/\left(\omega_0 C_{RWO}\right)$. Using (3.45) and (3.47), the phase noise in (3.34) can be

calculated as:

$$\mathcal{L}_{HWO}(\Delta\omega) = 10\log\left(\frac{kT\omega_0^2(1+\gamma_{NMOS})}{(2Q\Delta\omega)^2}\frac{4/3R_P}{A_0^2/2}\right) \tag{3.48}$$

The total power dissipated by the resonator can be calculated as:

$$P_{diss,HWO} = 2\frac{A_0^2}{2R_T} + \frac{A_0^2}{2R_P} = \frac{3}{4}\frac{A_0^2}{R_P}. \tag{3.49}$$

Using (3.49) into (3.48) and introducing the HWO power efficiency as done previously for the RWO and SWO, we have:

$$\mathcal{L}_{HWO}(\Delta\omega) = 10\log\left[\frac{2kT}{P_{DC,HWO}}\frac{1+\gamma_{NMOS}}{\eta_{P,HWO}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]. \tag{3.50}$$

3.2.4 Hybrid Wave Oscillators Array

As shown before, if two or more identical such oscillators are drawn side by side, they can be strongly coupled without perturbing the resonance frequency. The phase of the array can be analyzed as done exploiting the analysis carried out in the previous sub-sections. If the array consists of M coupled oscillators, it can be described using a state vector as follows:

$$X_{Arrey} = \begin{bmatrix} X_{HWO1} \\ X_{HWO2} \\ \cdots \\ \cdots \\ X_{HWO,M} \end{bmatrix}, \tag{3.51}$$

where each vector $X_{HWO,k}$ describes the k-th hybrid-wave oscillator. The array phase noise can be calculated as:

$$\mathcal{L}_{Array}(\Delta\omega) = 10\log\left(\frac{\sum_{k=1}^{M}\mathcal{N}_{HWO,k}}{A_0^2/2}\right) \tag{3.52}$$

where the noise $\mathcal{N}_{HWO,k}$ relates to the k-th HWO and is defined as in (3.6). Now, since the node voltages of each oscillator in the array is well approximated by the node voltage of the individual oscillator, it is easy to show that the contributions of

all oscillators in the array are equal and that the ISF of each noise contributor will be divided by M^2. As a result the array phase noise is simply given by the phase noise of the individual HWO divided by M:

$$\mathcal{L}_{Array}(\Delta\omega) = \mathcal{L}_{HWO}(\Delta\omega) - 10\log M, \tag{3.53}$$

where $\mathcal{L}_{HWO}$ is given by (3.48).

To compare the designs it is convenient to use the classic oscillator Figure of Merit (FoM), defined as:

$$FoM = PN(\Delta\omega)\, P_{mW} \left(\frac{\Delta\omega}{\omega_0}\right)^2. \tag{3.54}$$

The FoM is a function of Q and power efficiency η_P and it shows essentially the same expression for SWO, RWO, HWO and HWOs array, valid also for LC-tank oscillators:

$$FoM = 10\log\left[\frac{kT(1+\gamma_{NMOS})}{2Q^2\eta_P}\right]. \tag{3.55}$$

3.3 Oscillator design

The standing and the rotary wave oscillators were designed using differential T-lines, which are implemented as slow-wave differential coplanar waveguide structures, using the 3 μm thick copper top metal and metal level 3 patterned ground shield. The ground shield reduces substrate losses and provides an additional degree of freedom that allows to optimize the overall oscillator length based on chip floorplan considerations. The T-Line can be modeled as a series of delay cells and each one includes varactors for frequency tuning, as shown in Fig. 3.14.

- **Standing Wave Oscillator design**

  The SWO consists of a shorted differential T-line with NMOS cross coupled pair (Fig. 3.15). The supply current is provided by the PMOS transistors. Notice that, due to the standing wave, the points where the DC current is injected show essentially no voltage swing and loading by the PMOS transistors is negligible. The differential T-line has an unloaded characteristic impedance

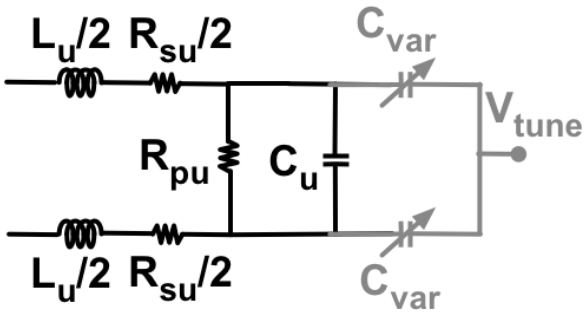

Figure 3.14: T-line cell lumped model, with varactors capacitances.

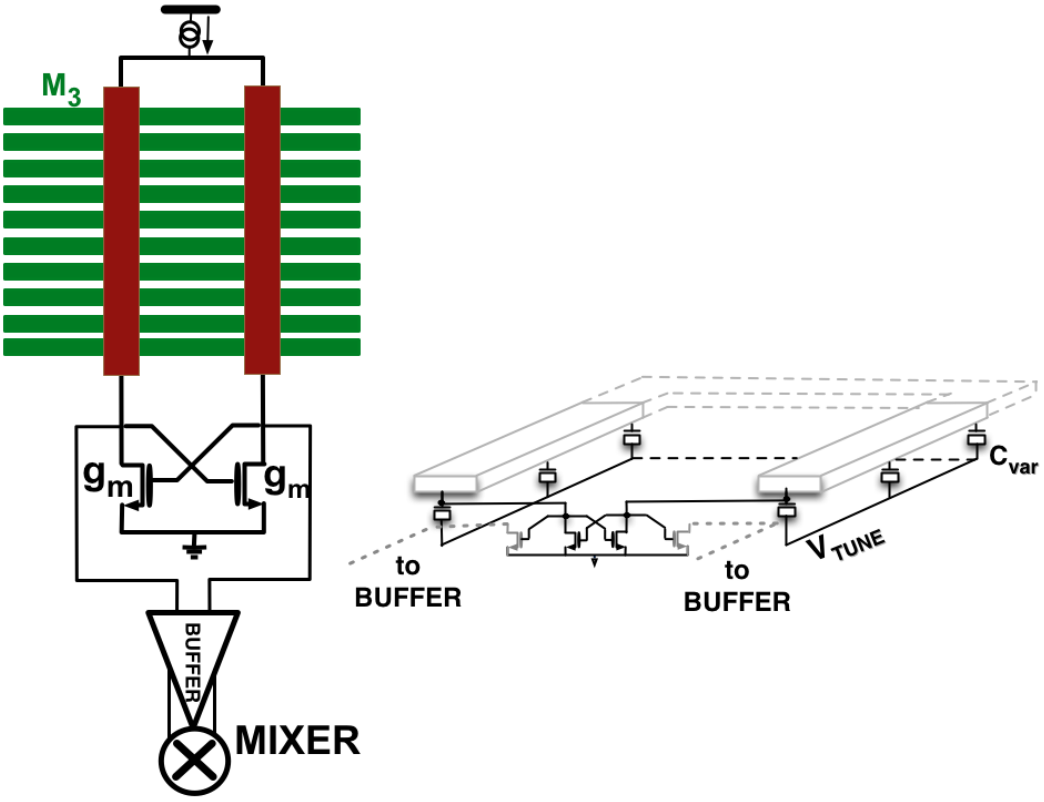

Figure 3.15: SWO design.

Z_0 equal to 62 Ω and a quality factor Q of 12.

It is well known that a transmission line terminated with a short circuit or with an open circuit behaves like a resonator. For instance, a parallel type of resonance can be achieved using a short-circuited transmission line that has

an electrical length of $\lambda/4$ at the desired oscillation frequency. At resonance, the line behaves as a parallel LC tank with:

$$R_{tank} = \frac{Z_0}{\alpha\, l} = \frac{4Q\, Z_0}{\pi}, \tag{3.56}$$

$$C_{tank} = \frac{\pi}{4\omega_0\, Z_0}, \tag{3.57}$$

$$R_{tank} = \frac{1}{\omega_0^2\, C_{tank}}. \tag{3.58}$$

The quality factor (Q) is a function of the propagation coefficient (β) and of the attenuation per unit-length (α):

$$Q = \omega_0\, R_{tank}\, C_{tank} = \frac{\pi}{4\alpha\, l}. \tag{3.59}$$

At resonance frequency, it is $l = \pi/2\beta$, and thus the previous expression becomes

$$Q = \frac{\beta}{2\alpha}. \tag{3.60}$$

The line parameters can be extracted from the simulated S-parameters, as shown before in section(1.5), and observing the equivalent circuit of a unit-cell of CPS shown in Fig. 3.14, the relation between resonance frequency and the loading capacitance, for N-cell cascaded unit-cells, is given by:

$$f_{osc} = \frac{v_p}{4l} = \frac{1}{4N_{cell}\, d\, \sqrt{L_u\,(C_u + C_{par})}}, \tag{3.61}$$

while the phase shift of a unit cell is given by:

$$\delta = 2\pi\, f \sqrt{L_u \left(C_u + \frac{C_{var}}{d}\right) d}, \tag{3.62}$$

where L_u and C_u are the inductance and capacitance per unit-length of the unloaded CPS, $l = N\, d$ is the total line length and d is the size of each cell. For a varactor-loaded transmission line it is possible to define two useful parameters, namely the capacitance loading factor (x_C) and the capacitance

ratio (y), which are defined as:

$$x_C = \frac{C_{var}^{max}}{d}, \tag{3.63}$$

$$y = \frac{C_{var}^{min}}{C_{var}^{max}}. \tag{3.64}$$

where C_{var}^{min} and C_{var}^{max} are the minimum and maximum variable capacitance in each cell. By equating the phase shift of the unit section at the minimum and maximum resonance frequencies, it is possible to express the frequency ratio f (f_{max}/f_{min}) as a function of the capacitance ratio and loading factor:

$$f \approx \sqrt{\frac{1+x_C}{1+x_C\,y}}. \tag{3.65}$$

Once x_C is calculated from (3.65), the length of the line can be calculated as:

$$l = N_{cell}\,d, \tag{3.66}$$

where N_{cell} is the number of unit cells that are required for a phase shift of $\pi/2$:

$$N_{cell} = \frac{\pi}{2\delta_{min}}. \tag{3.67}$$

The derived calculation can capture the phase-shifting nature of a generic loaded T-line as:

$$\delta_{min} = 2\pi\, f_{min}\, d\sqrt{L_{min}C_{min}}\sqrt{1+x_C}. \tag{3.68}$$

This expression does not take into account the parasitics capacitances due to the MOS and the terminations and also in the phase noise analysis section we have assumed the SWOs and RWOS to be made of a $\lambda/4$ T-line. However, the main effect of the parasitic capacitance, for example, at the input of the SWO is to decrease the oscillation frequency and to shift higher order resonance frequencies away from the harmonics of the fundamental. Notice that, the oscillation frequency in the absence of parasitic capacitance can be calculated using (3.2) only if the number of delay cells is really large. In practice the actual

number of cells is cannot be increased indefinitely due to layout constraints. For a finite number of equal delay elements the resonance frequency can be calculated exactly finding the zeros of the recursively defined admittance:

$$Y_N = sC_u + 1, \tag{3.69}$$

with $1/Y_0 = 0$.

We have obtained that a very good approximation of this exact solution is found by artificially increasing the number of cells N by 1/2 in (3.2). The error with this improved approximation is less than 1% already with 3 cells, while using (3.2) the error would be 15%. With more than 10 cells the error is below 0.1%, while it would be 4.8% using (3.2). Notice moreover that in general the higher order series and parallel resonance frequencies will not be exactly aligned with the harmonics of the fundamental frequency but they will approach these values, at least for the lower harmonics, as the number of cells increases. When a parasitic capacitance is added the exact calculation becomes more involved. Again, we have found that, for a relatively small number of delay cells, a much better approximation than (3.70) and (3.71) is found by artificially increasing the value of N by 1/2. In our calculations on phase noise we will use the actual oscillation frequency as obtained from simulations instead of the approximated one.

In practice, due to the capacitance of the cross coupled MOS transistors as well as any parasitic capacitance in these nodes (e.g. from an output buffer) the T-line must be significantly shorter than 1/4. Oscillation frequency with parasitic capacitance C_{PAR} is determined equating the imaginary part of the capacitance and of the T-line, resulting in the following equation:

$$\omega_0 C_{PAR} = \frac{1}{Z_0 \tan\left(N\omega_0\sqrt{L_u C_u}\right)}. \tag{3.70}$$

For small C_{PAR}, the oscillation frequency is well approximated as:

$$\omega_0 \approx \frac{\pi/2}{N\sqrt{L_u C_u}} \frac{1}{1 + C_{PAR}/\left(NC_u\right)} \tag{3.71}$$

- **Rotary Wave Oscillator design**

  As shown before, in a distributed oscillator, NMOS cross-coupled pairs must be distributed along the loop to the higher possible degree to compensate for line losses. The RWO consists of N active delay cells, where the passive circuit is essentially the T-line model shown in Fig. 3.14 and the phase velocity v_p of the wave traveling along the loop is given by:

$$v_p = \frac{1}{\sqrt{C_U\, L_U}} \tag{3.72}$$

  The wave after one lap is inverted due to the twist, therefore two laps are needed to complete one cycle. The oscillation frequency then can be expressed as:

$$f_0 = \frac{v_p}{2l} = \frac{1}{2N\sqrt{C_U\, L_U}}. \tag{3.73}$$

  From (3.73), the loop oscillation frequency is proportional to the phase velocity of the sustained travelling wave, thus the most straightforward way of performing oscillation frequency tuning is to change the wave phase velocity by periodically loading the T-line with varactors: the maximum and minimum oscillation frequency are analytically given by:

$$f_{min} = \frac{1}{2N\sqrt{L_U\,(C_U + C_{MOS} + C_{MAX})}}, \tag{3.74}$$

$$f_{MAX} = \frac{1}{2N\sqrt{L_U\,(C_U + C_{MOS} + C_{min})}}, \tag{3.75}$$

  where C_{MOS} is the fixed capacitance value given by active devices, while C_{min} and C_{MAX} are respectively the total minimum and maximum differential varactor capacitance.

  Since the design kit of the used 65 nm TSMC CMOS technology does not provide scalable MOS varactor models for the accumulation MOS varactor, a custom scalable $Verilog - A$ model has been developed on the bases of experimental data. The varactor characterization has been carried out from S-parameter measurement on a dedicated on-wafer test-structures, using three steps de-embedding procedures. Device capacitance has been expressed as a

function of the voltage between the gate electrode and n-well and it has been derived carrying out measures on 60 fingers devices with different finger sizes. The measured capacitive curve of a 1-finger a-MOS varactor device, with finger length $L_f = 60nm$ and finger width $W_f = 0.5\mu m$ is shown in Fig.3.16. The

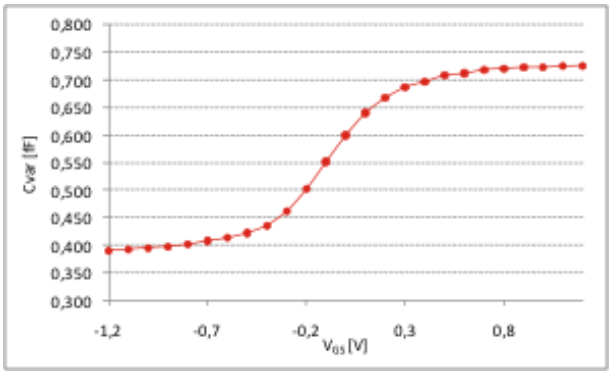

Figure 3.16: Measured varactor capacitive curve.

device performs a small-signal C_{MAX}/C_{min} of nearly 1.8. Exploiting the hyperbolic tangent function an analytical curve which perfectly fits the measured data samples has been found:

$$C_{var} = 0.558[fF] + 0.168[fF] \tanh\left[\left(V_{gs} + 0.1\right)/0.4\right] \tag{3.76}$$

and a $Verilog-A$ model for the 1-finger varactor lossless capacitance has been created on the basis of this fitting function. A fixed value resistance has been added in series to the capacitance $Verilog-A$ model supposing a conservative minimum varactor quality factor Q of nearly 10.

The issue in a RWO is to set a preferred propagation direction, because a RWO loop can sustain waves propagating in both directions producing a standing wave mode. To avoid that, we introduced a delay between the gate and the drain, which is essentially the T-line delay: the cross-coupled NMOS transistors are connected as shown in Fig. 3.17. The time delay, between the places where the gate and the drain of the same NMOS are connected (Fig. 3.18), leads to an equivalent reactive impedance, that depends on the wave propagation direction, leading to two different resonance frequencies for the two directions of propagation. If the forward wave is considered, the delay

generates an inductive impedance, while if the backward wave is considered, the delay generates a capacitive impedance.

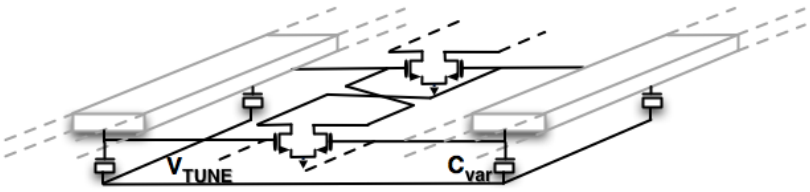

Figure 3.17: Simplified layout view of a RWO section.
Shielding bars below the top metal conductors are not shown for better clarity.

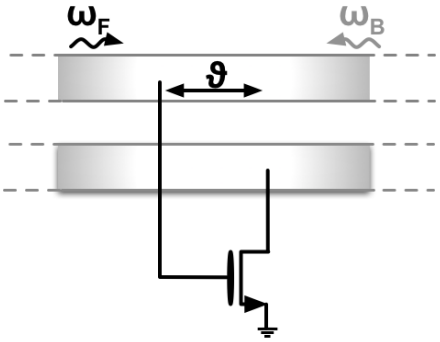

Figure 3.18: Simplified model of the RWO time delay between the gate and the drain of the cross-coupled NMOS transistors.

The direction resulting in the lower loss (corresponding to the lower frequency in our case) is automatically selected. In order to evaluate the effect of this solution on the RWO loop delay, in Fig. 3.19 a number of RWO active delay cells are connected in series. The array is driven by a voltage source and loaded by a resistor equal to the T-Line characteristic impedance. In the actual implementation turns and T-line cross coupling add significant delay and they are not sensitive to the propagation direction, however a good insight of the actual oscillator behavior can be gained from this simulation. The phase shift of a signal traveling from A to B (forward wave) or from B to A (backward wave) is reported in Fig. 3.20 for two extreme settings of the varactors control voltage. If the array in Fig. 3.19 were closed, connecting point A to point B, to form a loop, it would oscillate at the frequency corresponding to the 180° phase shift. It can be seen that this condition is met at a slightly higher frequency for

the backward wave compared with the forward wave. This simply means that we cannot have oscillation consisting of two waves having the same frequency and propagating in opposite directions.

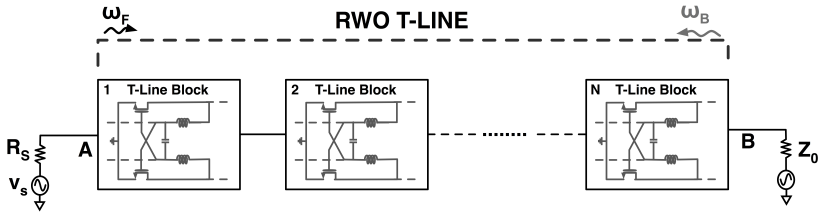

Figure 3.19: RWO T-line forward and backward waves phase shifting as a function of LO frequency .

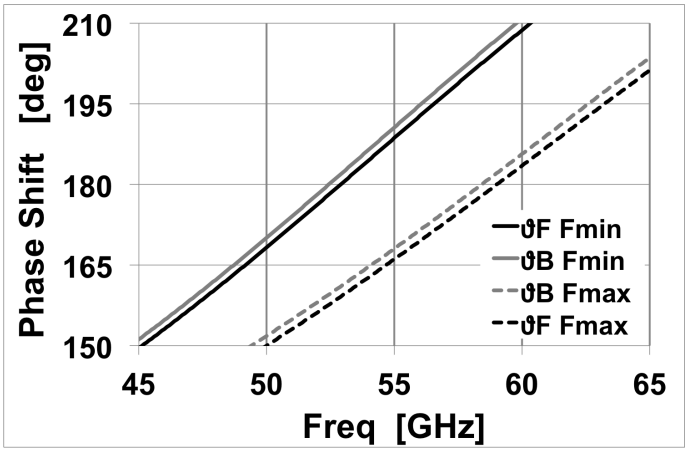

Figure 3.20: T-line forward and backward waves phase shifting as a function of LO frequency.

For the purpose of phase noise analysis we assume that the load capacitance has the same quality factor of the transmission-line. This is justified by the fact that, in our design, a varactor is added in parallel to any fixed capacitance to achieve good tuning range. As shown in the previous section, theoretically, when a RWO and two SWO using the same T-Line are coupled to form a HWO, close-in phase noise is expected to be 6 dB better than in the SWO alone, while preserving the same FoM [56]. In practice, loading from the NMOS transistors leads to a SWO that is shorter than $\lambda/4$ and to a RWO with lower T-lines characteristic impedance. These effects are more pronounced when accumulation-mode MOS varactors are added for frequency tuning since, in order to achieve the same tuning range, varactors must scale

proportionally with the total capacitance. These design constraints lead to some inevitable difference in the quality factor and hence also in the phase noise. Simulated

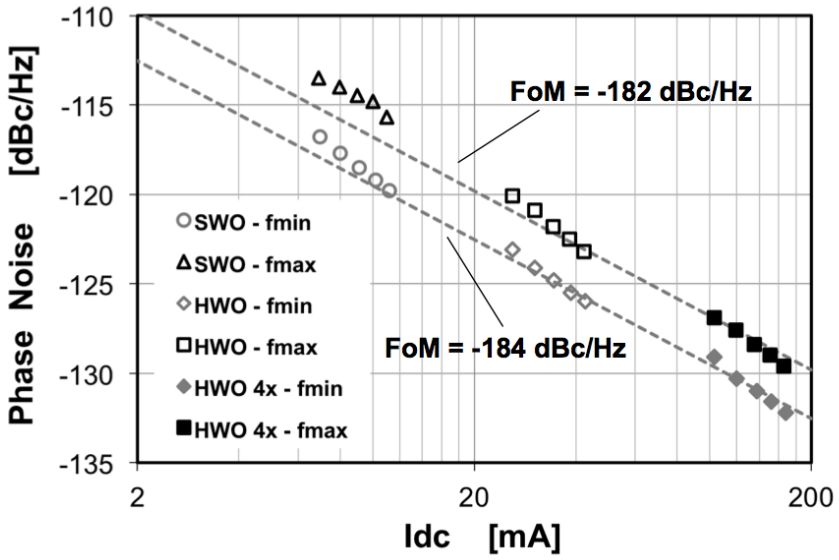

Figure 3.21: Phase noise simulation as a function of current consumption and oscillation frequency for the SWO, HWO and 4xHWOs array.

phase noise at 10 MHz offset as a function of current consumption is reported in Fig. 3.21 for the HWO and for the SWO alone at the two extremes of the tuning range (58 and 63 GHz respectively, for both oscillators). At the lower end of the tuning range, where AM-PM is negligible, the FoM of the HWO is approximately the same as for the SWO, while at the higher end it is slightly better. The same simulations were then carried out on the array of four HWOs. The HWO units are bilaterally coupled through the standing-wave oscillators in a nearest neighbor configuration. The proposed coupling arrangement ensures strong coupling between neighboring oscillators, while at the same time the operation of each oscillator in terms of oscillation frequency and voltage swings in each node is essentially unaffected. Neglecting AM-PM, the theory of coupled oscillators presented in [56] predicts, for an array of N bilaterally coupled oscillators, a close-in phase noise that is $1/N$ the phase noise of a single oscillator, provided that the coupling phase is chosen properly. As shown in Fig. 3.21, the simulation results on four coupled HWOs confirm the additional 6 dB phase noise improvement and the same FoM of the single HWO.

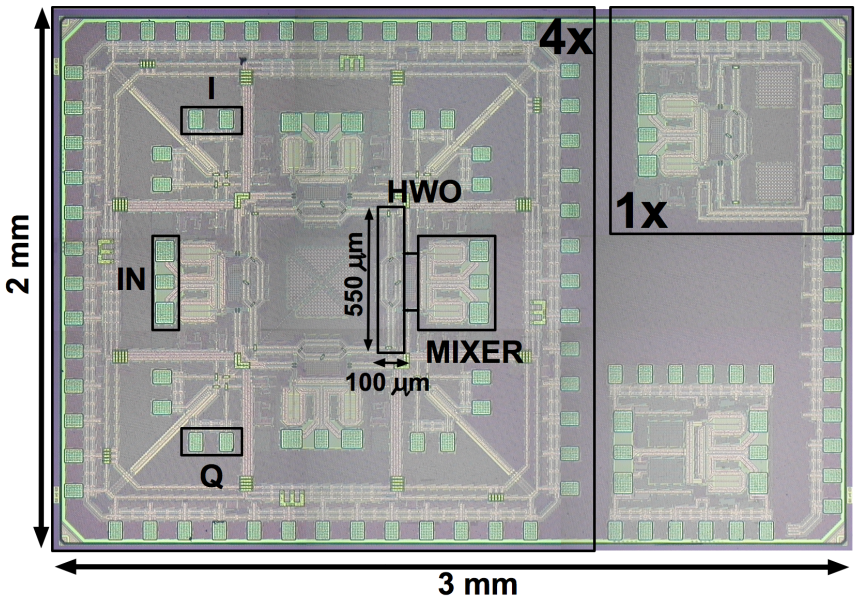

Figure 3.22: Chip microphotograph.

3.4 Experimental results

The test chip was implemented in a 65nm CMOS technology from TSMC and the die photo is shown in Fig. 3.22. It includes a four-oscillators array and a single quadrature oscillator. Each HWO occupies an area of $550 \times 100\mu m$ and is connected to a LO buffer and to quadrature down-conversion mixer, shown in the previous chapter, that allows to simplify testing. The LO buffer was designed as $\lambda/4$ transmission line, terminated to V_{DD}, driven by a small differential common-source stage that loads the oscillator with an equivalent differential capacitance of about 10 fF. This capacitance can be easily embedded in the RWO by designing the Y-shaped T-line connection with higher unloaded characteristic impedance. The chip was bonded on a printed-circuit board and the RF input tone was provided to the mixer input using a microprobe (Fig. 3.23).

Down-converted quadrature waveforms, sampled by a digital oscilloscope, are shown in Fig. 3.24. The oscillator operates nominally at 1.2 V and each HWO has a current consumption of 30 mA. When tuned to 52 GHz, the measured phase noise at 10 MHz frequency offset is -125 dBc/Hz for the single oscillator and -131 dBc/Hz for the four-oscillators array, as reported in Fig. 3.25. There is a good

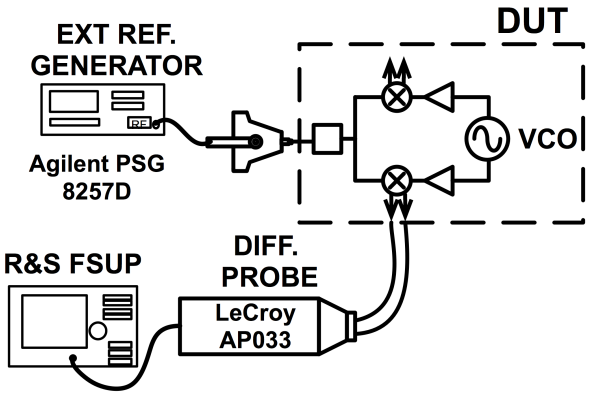

Figure 3.23: Measurement setup to test the HWOs.

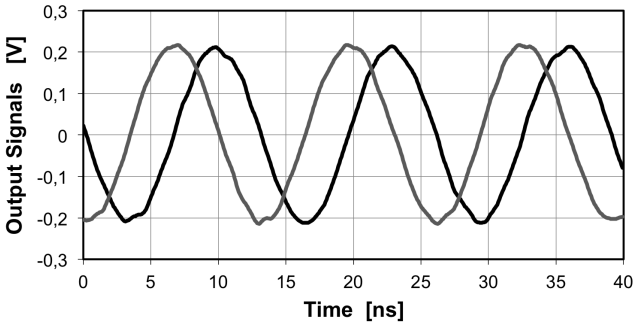

Figure 3.24: Phase noise simulation as a function of current consumption and oscillation frequency for the SWO, HWO and 4xHWOs array.

agreement between the simulations and measurements and the four HWOs array phase noise improves by 6 dB as estimated theoretically. A 3.4 dB phase noise variation is observed in Fig. 3.26, when the oscillator is tuned to higher frequencies. This is consistent with simulations and can be mostly attributed to increased AM-PM conversion by the accumulation-mode MOS varactors. A significant reduction of this spread is expected by adopting a switched-tuning arrangement, as is common practice.

The performances of the proposed HWO are compared with state-of-the-art quadrature and multiple output oscillators in Table 3.1.

It can be seen that the HWO achieves the best phase noise and FoM reported so far. Notice that LO distribution power consumption is already included in the HWO, while it would significantly worsen the overall FoM of other single-oscillator implementations.

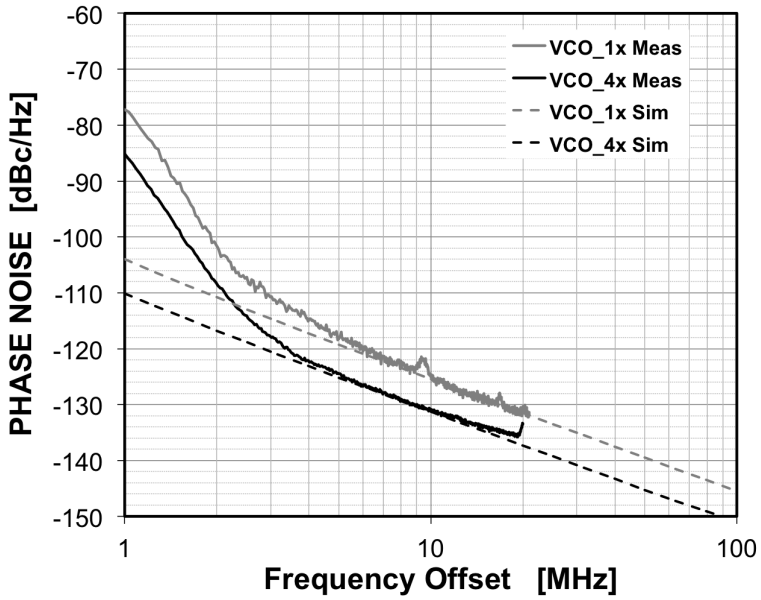

Figure 3.25: Measured Phase Noise at 10 MHz offset as a function of oscillation frequency for the 4 elements oscillators array.

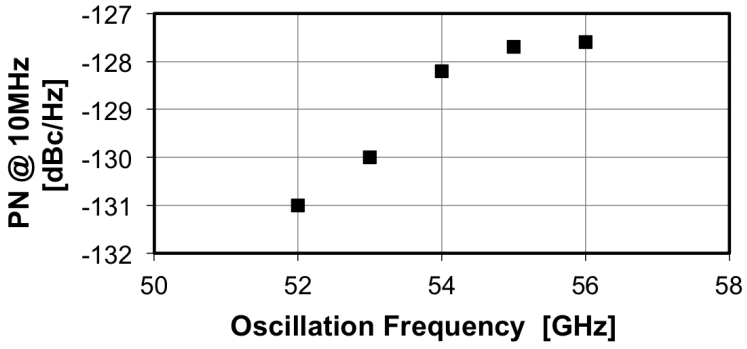

Figure 3.26: Phase noise simulation as a function of current consumption and oscillation frequency for the SWO, HWO and 4xHWOs array.

Ref	**Arch.**	**Tech.**	$f_0/\Delta f$ $[GHz]$	**PN** $[dBc/Hz]$	**FoM** $[dBc/Hz]$	**Power** $[mW]$
[62]	QVCO	65 nm CMOS	58.2/4.3	-95/-97 @ 1MHz	-177/ -179	22
[64]	QVCO	65 nm CMOS	93.1/4	-90 @ 1MHz	-172.7	43.2
[28]	QVCO	90 nm CMOS	48/8	-85 @ 1MHz	-165	22.7
[65]	RWO	180 nm CMOS	30/0.5	-104 @ 1MHz	-175	52
[66]	RWO	120 nm SiGe	45/2.9	-112 @ 1MHz	-173	13.8
[67]	RWO	180 nm CMOS	32/0.9	-108 @ 1MHz	-180	54
This Work single VCO	HWO	65 nm CMOS	54.2/4.6	-125 @ 10MHz	-183.7/ -180.9	36
This Work Array	HWO	65 nm CMOS	54.2/4.6	-131 @ 10MHz	-183.7/ -180.9	144

Table 3.1: Performance comparison of multiple outputs VCOs.

3.5 Conclusions

In this chapter a hybrid rotary/standing-wave oscillator with quadrature outputs has been introduced. It has been shown how two or more hybrid wave oscillators can be coupled without perturbing the resonance frequency to obtain an array which has the same behavior of a standalone HWO. The hybrid wave oscillator designed has been used as a building block for an array of coupled oscillators, conceived for on-chip phased arrays.

A noise analysis based on the impulse sensitivity function and noise contributors has been proposed for standing, rotary and hybrid wave oscillators. For all the three cases the same expression of phase noise has been obtained and it is equal to

the phase noise expression used for the classic LC-tank oscillators. Thanks to this analysis, we have demonstrated that the phase noise for an HWOs array improves by $10 \log N$, where N is the number of oscillators which were used in the array: in our case, the standalone HWO has a low phase noise compared to the state of art VCO, and moreover the 4 coupled HWOs array phase noise improves in theory by 6 dB with respect to the standalone HWO, as the phase noise measurements confirm. The proposed architecture, demonstrated in a 4-element array, features a high FoM and is scalable to large arrays, with increasing benefits in terms of phase noise.

This design can be considered as a proof of concept and, in future implementations, the improvement in phase noise may be traded off to reduce the power dissipation. It was shown that the energy-based normalization of the state variables provides accurate closed form expressions for the ISF of standing-wave and traveling-wave oscillators and, in general, we believe that it can be applied to all oscillators based on high order resonators.

Conclusions

Millimeter-wave wireless communications allow high data rates (up to 6 Gbps), higher integration levels, strong levels of frequency reuse and enhanced safety due to the strong amount of atmosphere's absorption at these frequencies. The main application field of 60 GHz wireless transmissions is nowadays represented by high speed WLAN, but they are also exploited for intelligent transportation systems (ITS's), radars and other applications.

Millimeter wave the design requires different levels of analysis: device, building blocks, circuital topology and transceiver architecture have been studied in parallel. Electromagnetic simulations and direct characterizations on dedicated test chips of active and passive devices has been carried out to try modeling devices as accurately as possible. Moreover, around 60 GHz the design of any building block in the RF receiving chain poses many design challenges, therefore in millimeter-wave transceivers intrinsic link budget limitations are addressed using phased-array architectures. The principal phased-array configurations have been discussed and this analyses has shown that the LO distribution represents a difficult task in all phased array architectures, except for the RF recombination one. To address this issue, in this work, a phased-array direct-conversion receiver prototype adopting the IF recombination approach has been designed and implemented in a standard 65nm CMOS technology; in particular, it is shown how the power consumptions due to LO signal distribution has been minimized, using four coupled distributed wave oscillators (HWO) connected directly to broadband passive down-conversion mixers. This receiver has been designed to work on entire mm-wave frequency range, therefore

at the input of each mixer, a broadband matching network has been implemented. This matching network allows to connect the mixer directly to antenna providing significant benefits, such as extremely low power, or greatly increased tuning range and linearity.

In the second chapter, the passive mixer design has been described: in particular a simple broadband matching network and the associated design procedure has been presented and the principal performance as input impedance, gain and noise have been analyzed. The prototype mixer features competitive and stable performances over a broad frequency range from 50 GHz up to 67 GHz.

The last chapter deals with the four coupled HWOs array: a hybrid rotary/standing-wave oscillator with quadrature outputs has been introduced and it has been used as a building block for the array of coupled oscillators. The proposed architecture, demonstrated in a 4-element array, features a high FoM (-183.7 dBc/Hz) and is scalable to large arrays, with increasing benefits in terms of phase noise. We have demonstrated that the HWOs array phase noise improves by a factor $10 \log N$, if N represents the number of coupled oscillators, and the figure of merit of the array remains constant as the number of coupled oscillators. This architecture provides a proof of concept and, in future designs, the improvement in phase noise may be traded off to reduce the power dissipation.

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