A Study of Successive Approximation Register ADC Architectures

A Ph.D. Thesis by
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To
Claudia

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Introduction

1.1 Motivation and Structure of the Thesis

In the era of all-mobile devices and the Internet of Things, power efficient solutions are required by new applications. Wearables and battery supplied systems are in high demand, asking designers to come up with new ideas for ultra low-power high-performances data converters. Among all the possible architectures, SAR ADCs stand out because of their high efficiency. Besides, the quasi all-digital nature of this topology greatly adapts to the technological scaling and the simple structure better suits to more complex system-level designs. Apart from being an excellent choice as a stand-alone or time-interleaved architecture, SAR ADCs are particularly suited for hybrid solutions that further pushes away the limits of other types of converters, such pipeline or oversampled ADCs.

The goal of this thesis is to study the versatility and adaptability of the SAR algorithm for different applications. In order to do so, 3 different projects carried out during the Ph.D. activity are presented. These are

1. An 8-b 700 MS/s Flash-SAR ADC with 86.7 fJ/conversion-step in 65-nm CMOS.
2. A 14-b 33.6 V DR Extended Range ADC for Battery Monitoring.
3. A 200 μW 12-b 8 MS/s SAR ADC for Ultrasound Systems.

The presented ADCs highly differ from the performances point of view, but they all share the fact that they use the SAR algorithm to meet the requirements of the given application. The first two projects were fabricated and tested, while the third has been simulated at post-layout level.

Project # 1 is a high-speed single-channel ADC for wireline communications. The architecture uses a sub-ranging approach with a flash converter and a multi-bit per cycle SAR ADC. Redundancy is applied to relax the accuracy requirements of the first stages, and a shift-register free logic is implemented. Thresholds in the multi-bit per cycle SAR converter are produced by a special preamplifier that uses an interpolation-like technique. A novel comparator speeds up the overall operation

of the converter, by using a built-in preamplifier that initially unbalances the output of the latch.

Project # 2 implements an extended-range ADC for monitoring the voltages of a stack of 8 Li-Ion batteries. The system uses an 8-channel TI-incremental ADC for the coarse conversion of the battery cell voltages, and a single SAR ADC for the fine conversion. The high-voltage section is limited to 8 switches and a high-voltage capacitor reducing the cost of the converter. The remaining part of the circuit operates at a nominal 5-V supply. The time-interleaved structure obtains an almost-simultaneous sampling of the battery cells, and the single fine converter limits the mismatch between channels.

Project # 3 is a very compact SAR ADC for ultrasound pixel-arrayed systems. The ADC is intended to be used in the acquisition channel of a wearable transcranial doppler ultrasound system (TCD) to measure cerebral blood flow velocity (CBFV) at the middle cerebral artery (MCA). There are 64 such channels, so area and power constraints are the most stringent specifications. An hybrid resistive-capacitive structure is used to reduce the area of the DAC, while an asynchronous logic optimises the timing of the converter and the power consumption.

This chapter introduces to the reader the most common data converter architectures and provides a discussion on the evolution of data converter during the past years. Finally, a research on the state-of-the-art in SAR ADCs is provided. Chapters 2, 3 and 4 present the three different projects (# 1, # 2 and # 3), while conclusions are drawn in Chapter 5. The bibliography is dedicated for each chapter in order to provide a more direct access to the reader.

1.2 Data Converter Architectures

The first specification which defines a data converter is its type. The conversion algorithm normally provides this kind of information. The types of converters are classified in two main categories: Nyquist rate and oversampling. This distinguishes between the following design strategies: using an input that occupies a large fraction of the available bandwidth or using an input-band that only occupies a small part of the Nyquist range[1]. The ratio between the Nyquist limit and the signal band, $f_s/2(f_B)$, is called oversampling ratio (OSR). Converters with a large OSR are called oversampling converter, whereas Nyquist-rate converters have a small OSR, typically less than 8.

The main architecture's way of operation are described below. For a more accurate analysis on ADC specifications and topologies the reader can refer to [1–3].

[1] The Nyquist-Shannon sampling theorem states that *"A band limited signal, x(t), whose Fourier spectrum, X(jω), vanishes for angular frequencies* $|\omega| > \omega_s/2$ *is fully described by an uniform sampling x(nT), where* $T = 2\pi/\omega_s$*." The Nyquist range becomes [0 - f_s], where f_s is the sampling frequency.*

1.2.1 Nyquist Rate

1.2.1.1 Flash ADCs

The flash architecture uses a parallel conversion algorithm. An n-bit quantizer identifies 2^n bins with 2^n - 1 transition points; therefore, the converter requires 2^n - 1 reference voltages and 2^n - 1 comparators. The output of the comparators will be logic 1 up to the input level and logic 0 above. A decoder can then translate this thermometric representation into an n-bit digital output.

Fig. 1.1 shows the basic block diagram of a full-flash ADC, where the reference voltages are generated by a resistive divider. The input is sampled by a sample & hold circuit (S&H) into the positive input of the comparator, while the reference voltage is applied at the negative input. Only one clock cycle is required for the conversion, as all comparators work at the same time.

Full-flash converters are the optimum for very high-speed, but the resolution cannot be very high as a number of limits make the implementation unpractical. A first issue concerns the availability of a reference voltage divider that can operate at very high-speed and high-resolution. Another practical limit that determines the maxi-

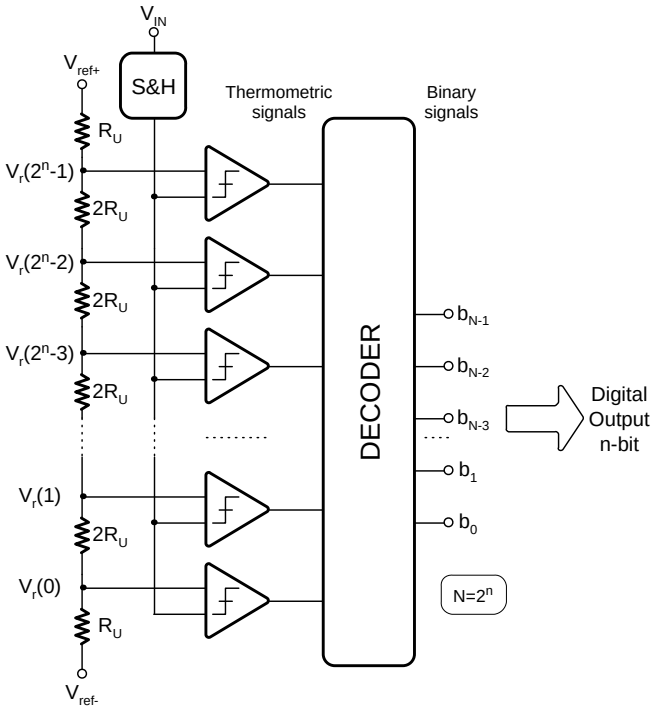

Fig. 1.1 Basic block diagram of the full-flash converter.

mum resolution is the exponential increase of the circuit complexity with the number of bits: every additional bit doubles both the silicon area and, more importantly, the power consumption. Furthermore, a larger resolution increases the capacitance load at the output of the S&H caused by the parasitic capacitance of the comparators. Usually, passive S&H are used in order to reduce power consumption. But, increasing the input capacitance to the sampler circuit increases linearly the power consumption consumed by the S&H and limits its speed operation.

The limits discussed above are such that with present technologies it is impractical to design an 8-bit full flash with conversion speeds higher than 2 GS/s or a 6-bit flash operating at more than 8 GS/s.

1.2.1.2 SAR ADCs

The successive approximation algorithm performs the A/D conversion over multiple clock periods by exploiting the knowledge of previously determined bits to find the next significant bit. The method aims to reduce the circuit complexity and power consumption using a serial approach and solving one bit per clock period.

For a given dynamic range 0 - V_{FS}, where V_{FS} is the full-scale voltage, the most significant bit (MSB) distinguishes between input signals that are below or above the limit $V_{FS}/2$. Therefore, comparing the sampled input with $V_{FS}/2$ obtains the first bit as illustrated by the timing scheme of Fig. 1.2 (a). The knowledge of the MSB restricts the search for the next bit to either the upper or the lower half of the 0 - V_{FS} interval. After this, a new threshold is chosen (either $V_{FS}/4$ or $3V_{FS}/4$) and the next bit can be estimated. The voltages used for the comparisons are generated by a DAC under the control of a logic system known as the successive approximation register (SAR) as shown in Fig. 1.2 (b).

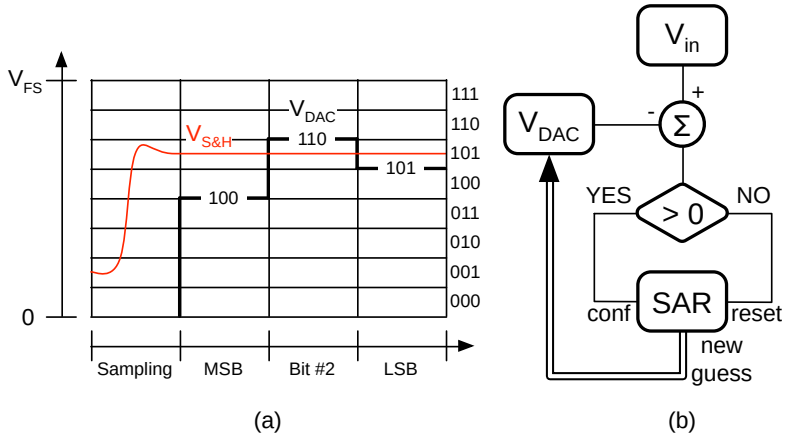

Fig. 1.2 Timing (a) and flow diagram (b) of the successive approximation technique.

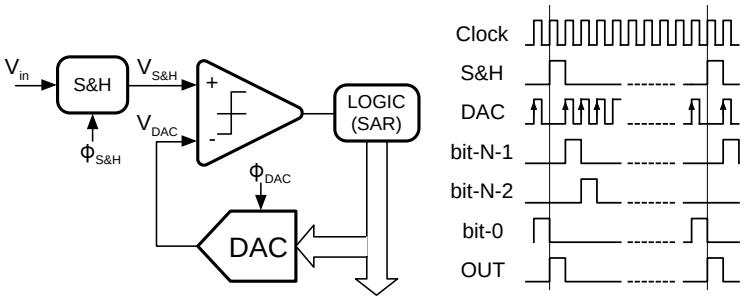

Fig. 1.3 Basic block diagram of the SAR converter.

The method uses one clock period for the S&H and one clock period for the determination of every bit thus requiring (n+1) clock intervals for an n-bit conversion. Fig. 1.3 shows a typical block diagram of a SAR converter. The S&H samples the input during the first clock period and holds it for N successive clock intervals. The digital logic controls the DAC according to the successive approximation algorithm. The SAR predicts the next bit, that is then either confirmed or not by the output of the comparator. At the end of the N comparisons, the output is ready as a binary code so no decoder is needed.

Fig. 1.4 shows the most common implementation of the successive approximation algorithm, the charge redistribution method. It uses an array of binary weighted capacitances and just one comparator as an active element. The sampling phase, ϕ_S, pre-charges the entire array to the input signal by connecting the bottom plates of the array to the input and the top plates to the analog ground. After sampling, the SAR begins the conversion by first connecting the bottom plate of the largest capacitance ($2^{n-1}C_U$) to the reference voltage, V_{ref}, and the remaining part of the array to ground. The superposition principle determines the voltage on the top plate, applied to the comparator, to be equal to

$$V_{comp}(1) = \frac{V_{ref}}{2} - V_{in} \tag{1.1}$$

Since this voltage is the difference between the MSB voltage and the input, it is only necessary to compare it to ground. The comparator result determines the MSB and enables the SAR to establish the conditions for the next bit calculation. If the MSB is 1, the connection of ($2^{n-1}C_U$) to V_{ref} is confirmed and the capacitance ($2^{n-2}C_U$) is tentatively connected to V_{ref} for the second comparison. Depending on the value of the already determined MSB, the new top plate voltage becomes

$$V_{comp}(2) = \frac{3V_{ref}}{4} - V_{in} \quad or \quad V_{comp}(2) = \frac{V_{ref}}{4} - V_{in} \tag{1.2}$$

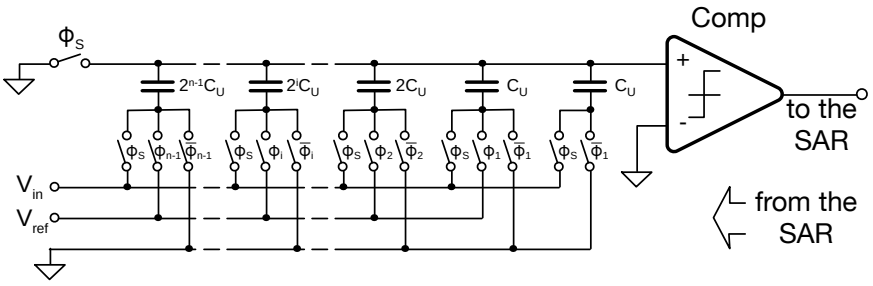

Fig. 1.4 Charge redistribution implementation.

for MSB = 1 or MSB = 0, respectively. This voltage is then used to determine the next bit and the algorithm continues until all the n-bit are generated.

Variations of the scheme of Fig. 1.4 and different applications of the SAR converter will be discussed in Section 1.4.

1.2.1.3 Pipeline ADCs

Pipeline ADCs, similar to pipeline logic blocks, achieve a high throughput by unwinding over space what should be done over time by a sequential scheme. They use several stages that process different inputs simultaneously, like in Fig. 1.5. While the first stage is processing V_{in}(t), the second stage is processing V_{in}(t-1), the third stage V_{in}(t-2), and so on. Each stage produces two outputs, the digital representation of the input, N_i, and the residual voltage, R_i. The residual represents the difference between the input to the stage and the analog version of the output N_i (usually provided by a DAC) amplified in order to match the next stage input range. It is usually generated and transferred to the next stage by means of an operational amplifier. The amplification of the residual relaxes the accuracy requirements of the successive stages. Ideally, if the input range of the all the stages is the same, the multiplying factor for the residual voltage is 2^{n_i}, where n_i is the number of bits solved in the stage. The total resolution of the pipeline architecture is given by the sum of the bits solved at each stage.

The generation of the residual voltage in modern technologies has become a major issue, as low-voltage supply makes operational amplifiers an unsuitable solution. Another limiting factor is the poor improvement of the bandwidth of op-amp in modern scaled technologies, if compared to the high-speed performances in digital circuits. Several techniques have been proposed to overcome this problem. However, the delay introduced by the residue generator is usually the main limitation to the speed operation of the converter.

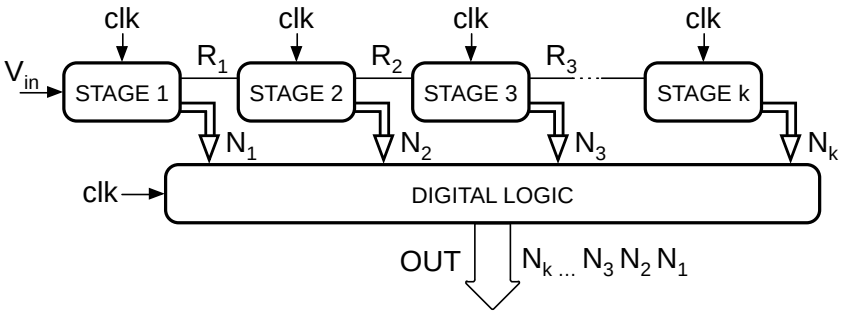

Fig. 1.5 Basic block diagram of the pipeline converter.

A difference with other Nyquist rate converters, is the larger latency introduced by pipeline ADCs. This might become a problem when using the converter in a feedback loop.

1.2.2 Oversampled ADCs

The key advantage of oversampling is that the signal band occupies a small fraction of the Nyquist interval making it possible to use digital cancellation on the relatively large fraction of the quantisation noise that is outside the band of interest. The result is a lower quantisation noise power in the band of interest and a higher equivalent number of bits. The use of an ideal digital filter after the A/D conversion removes the noise from f_B to $f_s/2$ and significantly reduces the quantisation noise power by a factor of $f_s/(2f_B)$, leading to

$$V_{n,B}^2 = \frac{\Delta^2}{12} \cdot \frac{2f_B}{f_s} = \frac{V_{ref}^2}{12 \cdot 2^{2n}} \cdot \frac{2f_B}{f_s} \tag{1.3}$$

where V_{ref} is the reference voltage, Δ is the LSB voltage and n is the number of bits of the quantizer.

The definition of the effective number of bits (ENOB) shows that oversampling by a factor OSR = $f_s/(2f_B)$ potentially improves the number of bits from n to

$$ENOB = n + 0.5 \cdot log_2(OSR) \tag{1.4}$$

where OSR is the *oversampling ratio*.

1.2.2.1 ΣΔ ADCs

The sigma-delta (ΣΔ) ADC is the converter of choice for modern voiceband, audio, and high-resolution precision industrial measurement applications. A ΣΔ ADC contains very simple analog electronics (a comparator, voltage reference, switches, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This digital circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low pass filter).

If simply oversampling is used to improve resolution, an oversampling factor of 2^{2N} is required to obtain an N-bit increase in resolution. The ΣΔ converter does not need such a high oversampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband. Fig. 1.6 shows the noise shaping principle. An input signal with a bandwidth equal to f_B is oversampled by a noise-shaping A/D with sampling frequency equal to $f_N = OSR \cdot f_B$. The output of the A/D represents the quantised signal, with a quantisation noise that has been noise-shaped. This noise is high-pass filtered, so to move its spectral density to the upper part of the Nyquist range, i.e. out-of-band. A digital filter then filters out the quantised signal in order to reject all the quantisation noise in the high-frequency zone. Finally, a decimator reduces the output data rate to the one required by the Nyquist theorem, f'_N.

Incorporating the quantizer in a feedback loop as shown in Fig. 1.7 gives rise to the desired noise shaping. The scheme has a sampled data input that, after the processing data block A(z), is converted into digital. For closing the loop it is necessary to generate the analog representation of the converted signal by means of a DAC. A second processing block, B(z), is used before the subtracting element. The linear model of Fig. 1.7 (b) represents the quantization error with the additive noise ϵ_Q that is a second input to the circuit.

The goal of the system is to have different transfer functions for the input signal X and the noise signal ϵ_Q. These are namely *Signal Transfer Function* (STF) and *Noise Transfer Function* (NTF). By inspection of the scheme it results

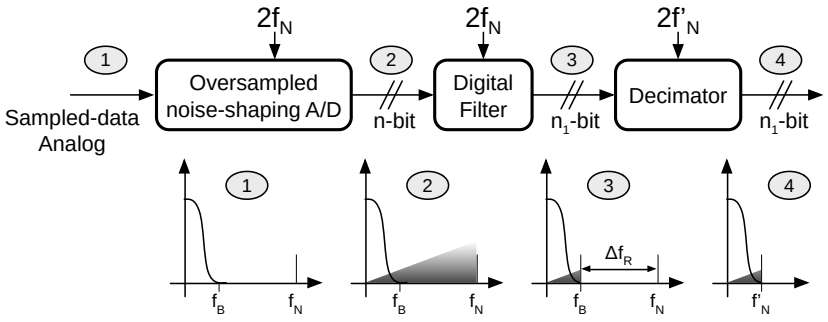

Fig. 1.6 Out-of-band noise rejection and decimation of a noise shaped signal.

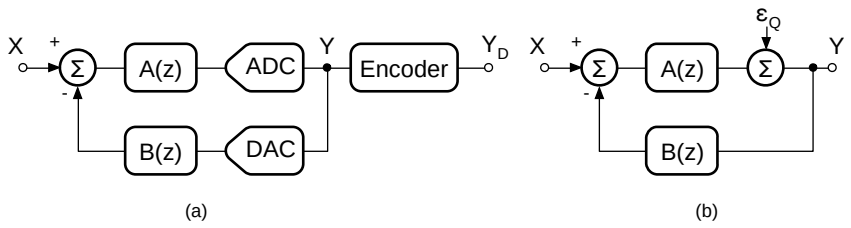

Fig. 1.7 Incorporating the quantizer in a feedback loop obtains noise shaping.

$$[X - Y \cdot B(z)]\, A(z) + \epsilon_Q = Y \tag{1.5}$$

whose solution yields

$$Y = \frac{X \cdot A(z)}{1 + A(z)B(z)} + \frac{\epsilon_Q}{1 + A(z)B(z)} \tag{1.6}$$

The idea is to provide a low-pass filter function to STF and a high-pass filter function to NTF, in order to ensure the required noise-shaping. Often, the processing block B(z) is not used (B(z) = 1), and A(z) is an integrator. This solution is called a first order ΣΔ modulator.

The input of the modulator can be already in the discrete-time or a S&H is necessary for the data conversion. The former case is called a sampled-data ΣΔ, the latter case corresponds to a continuos-time ΣΔ modulator.

Fig. 1.8 shows the block diagram of a sampled-data ΣΔ that uses

$$A(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{1.7}$$

leading to

$$Y(z) = X(z)\, z^{-1} + \epsilon_Q(z)\, (1 - z^{-1}) \tag{1.8}$$

The effect of the modulator is to introduce a simple delay to the input signal, while it can be proven that the noise signal is high-pass filtered. Besides, in [1] the maximum SNR of the first order ΣΔ modulator, in the case of an ideal filter that removes the out-of-band noise, is given and it is

$$SNR_{\Sigma\Delta,1|dB} = 6.02n' + 1.78 - 5.17 + 9.03 log_2(OSR) \tag{1.9}$$

where n' = $\log_2$k, and k is the number of thresholds used in the quantiser. This leads to an effective number of bits equal to

$$ENOB = n' - 0.86 + 1.5 log_2(OSR) \tag{1.10}$$

where the first term accounts for the SNR improvement due to a multi-level quantiser, and the second term is a fixed cost required to secure an improvement of

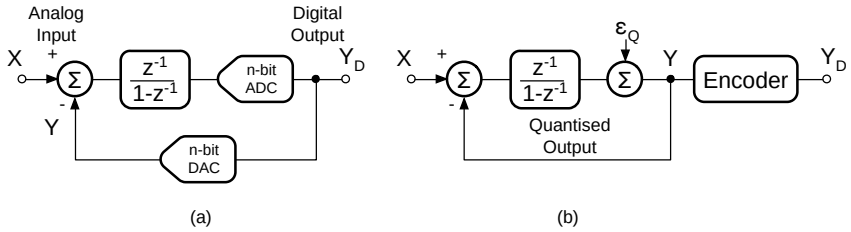

Fig. 1.8 (a) Sampled-data first order sigma delta modulator and (b) its linear model.

1.5 bits every doubling of the sampling frequency. If compared to (1.4), for every doubling of the OSR one extra bit is gained. More complex architectures implement higher order modulators and achieve better enhancement in the SNR. The reader can refer to [1, 2] for a deeper insight on the $\Sigma\Delta$ modulator.

Notice that the noise shaping function implemented by the $\Sigma\Delta$ modulator does not get rid of the quantisation noise, but it only moves its spectral density to the high frequency part of the Nyquist range. Actually, the effect of the noise shaping results in a global amplification of the quantisation error power by 2. A digital filter does need to filter out the high-frequency noise produced by the modulator in order to achieve the required A/D conversion. In this case, a large OSR relaxes the filter requirements as it distances the bandwidth from the high-frequency part of the Nyquist range.

Another remark concerns the linearity and noise specifications of the ADC and the DAC. The digital signal generated by the ADC is such that any limit affecting it is relaxed by the feedback loop gain. Indeed, the ADC error must be referred to the input of the modulator by dividing it by the transfer function of the integrator. Since at low frequency (which is the region of interest) the integrator has a very large gain, the error is greatly attenuated in the signal band. The same benefit does not apply to the DAC as its error is injected directly at the input of the modulator together with the input.

The benefits provided by oversampling and noise shaping enable the use of a small number of quantisation levels. However, the noise shaping technique is based on the white nature of the quantisation noise. This condition applies under a given set of circumstances:

1. all the quantisation levels are exercised with equal probability;
2. a large number of quantisation levels are used;
3. the quantisation steps are uniform;
4. the quantisation error is not correlated with the input.

Thus, the use of a small number of quantisation levels does not comply with the conditions necessary for considering ϵ_Q as white noise. If the signal contains a dominant DC component, the quantisation noise becomes a repetitive pattern that produces spectrum tones, and also the 4th condition mentioned above is not longer observed. A possible solution to this problem, apart from using multi-bit quantisers,

is to implement the dithering technique. Basically, an auxiliary input that eliminates the correlation between ϵ_Q and the signal is added. Obviously, the dither must be effective against the tones and should not alter the signal. For this there are two possibilities: the first is to inject a sine wave whose frequency is out of the signal band. The digital filter used to cancel the out-of-band noise then removes the effect of the dither. The second method utilises a noise-like signal whose contribution does not degrade the SNR, which can either be thermal noise of the electronics in role or an external random signal.

It is important to notice that, even with dithering, $\Sigma\Delta$ ADCs cannot provide a deterministic measurement of a DC signal, as some information of the past signals will always be present at the output of the decimator due to the nature of the converter.

1.2.2.2 Incremental ADCs

Instrumentation and measurement applications, such as the readout of bridge transducers, battery monitoring and biomedical acquisition systems require monotonic analog-to-digital converters with high resolution, good linearity, low offset and, typically, low power. Incremental converters, directly derived from $\Sigma\Delta$ schemes, are particularly suitable for those needs. Although they share the same structure as a $\Sigma\Delta$ ADC, in an incremental ADC the integrators are reset at the start of each conversion.

As a result, only the samples of the used set determine the output and no information about previous samples is used, and so there is no need to describe the quantisation error as noise and even to talk about noise shaping. Thus an incremental ADC does not suffer from the limitations of small number of quantisation levels and does not need dithering to operate with DC input signals. Instead, the input should be constant or change slowly during the entire conversion, otherwise the digital result becomes a weighed average of the analog input, in a manner similar to that of a FIR filter.

The equivalent number of bits of an incremental converter depends on the order of the scheme, the number of clock cycles per sample, the resolution of the quantiser and the digital post processing. Generally, to obtain a given resolution, higher order modulators are more efficient since the required number of clock periods is reduced. However, when the order of the scheme is higher than two, stability requirements can limit the effectiveness of the architecture.

Fig. 1.9 shows the block diagram of a first-order incremental ADC. It consists of a delayed-integrator, a comparator and a 2-level DAC. The operation principle is as follows: when a new conversion cycle starts, the output of the integrator, V_{res}, is reset. Since the frequency of the input signal of incremental ADCs is usually low, V_{in} can be regarded as a constant signal. In each clock period, V_{in} subtracts V_{out} (the analog version of D_{out}) and the difference is accumulated by the delayed integrator. At the end of N clock cycles, the residue voltage at the output of the integrator is given by

$$V_{res} = \sum_{i=1}^{N-1} V_{in}(i) - \sum_{i=1}^{N-1} D_{out}(i) V_{ref} \tag{1.11}$$

Due to the stability of the feedback loop, the voltage of V_{res} is limited, namely $-V_{ref} < V_{res} < V_{ref}$, where $\pm V_{ref}$ are the reference voltages. The input signal V_{in} can be, hence, represented as

$$V_{in} = \frac{\sum_{i=1}^{N-1} D_{out}(i) V_{ref}}{N-1} + \frac{V_{res}}{N-1} \tag{1.12}$$

and the resolution of a first-order incremental ADC can be expressed as

$$R_{1-ord} = log_2(N-1) \tag{1.13}$$

Unfortunately, the conversion efficiency of a first-order incremental ADC is low. Methods for increasing the resolution are by increasing the number of clock periods

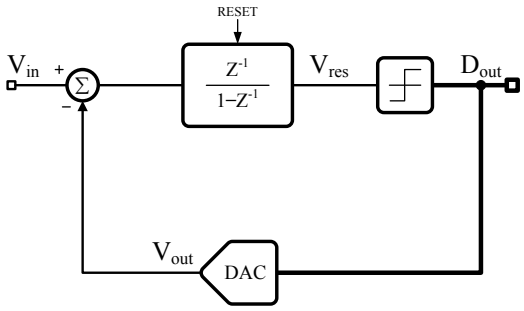

Fig. 1.9 First-order incremental ADC block diagram.

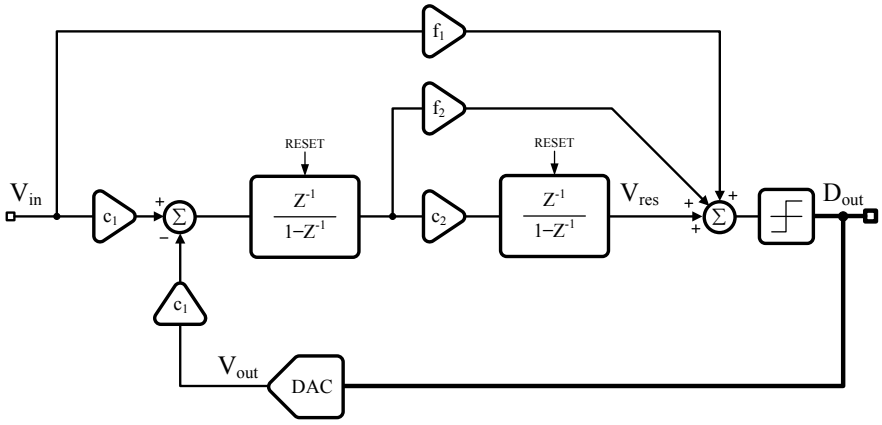

Fig. 1.10 Second-order incremental ADC block diagram.

N and using more effective schemes with cascaded integrators. High-order incremental ADCs, therefore, contain multiple integrators with reset at the beginning of the conversion cycle. The key points are to increase the accumulation efficiency, while maintaining the stability of the structure and keeping $V_{res}(N)$ minimized.

A conventional second-order incremental ADC is discussed here to illustrate how the conversion efficiency changes compared with the first-order architecture. As seen in Fig. 1.10, this structure contains two integrators with delay. In the signal path there are two coefficients c_1 and c_2. In order to keep the loop stable, two feed-forward paths are included with coefficients f_1 and f_2. This scheme also employs a comparator and a 2-level DAC. Using the same mathematical approach employed for the first order scheme, $V_{res}(N)$ for this second-order structure can be expressed as

$$V_{res}(N) = c_1 c_2 \sum_{i=1}^{N-1} \sum_{j=1}^{i-1} V_{in}(i) - c_1 c_2 \sum_{i=1}^{N-1} \sum_{j=1}^{i-1} D_{out}(j) V_{ref} \tag{1.14}$$

Similarly, the resolution of the second-order structure is described as

$$R_{2-ord} = log_2 \frac{c_1 c_2 (N-1)(N-2)}{2!} \tag{1.15}$$

To compare the conversion efficiency of first-order and second-order incremental ADCs, parameters N = 1024, $c_{1,2} = 1$, $f_1 = 1$ and $f_2 = 2$ are chosen. According to (1.13) and (1.15), the first-order scheme can provide 10-bit resolution while the second-order structure achieves 19 bit. [4]

1.3 Data Converter Evolution

Once upon a time the area of application for different converter types was a well defined space in the speed/resolution graph as shown in Fig. 1.11 in [5]. The designer's architectural choice was a simple trade-off between some factors such as latency, speed, accuracy and area that could all be summarised in a table like in Table 1.1. In this particular classification, SAR ADCs were an effective solution for medium-high resolution converters working at low-medium conversion rate and occupy the centre of the speed/resolution space. Pipeline ADCs could improve both resolution and speed, if compared to SAR ADCs, at the cost of extra power and area consumption and longer latencies. For very high-speed operations folding ADCs and flash ADCs were the only choice, but the achieved resolution was not too high. Finally, $\Sigma\Delta$ ADCs occupy the high-resolution low-speed application area.

However, as stated in [6], *an interesting consequence of the relentless optimisation and improvements seen* [...] *is the increasing competition among ADC architectures.* [...] *Today's ADC designer is confronted with an overlapping design space offering multiple solutions that are difficult to differentiate in their suitability.*

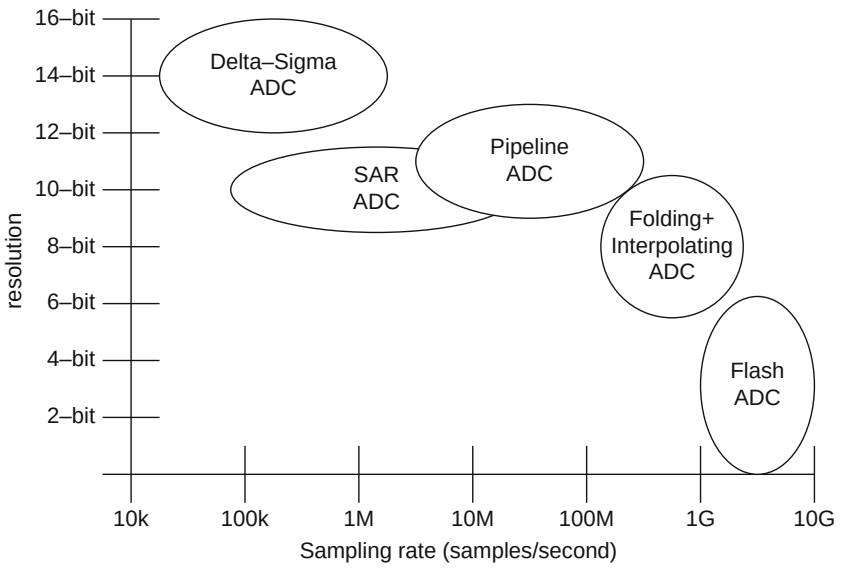

Fig. 1.11 ADC architecture comparison, [5].

Table 1.1 Comparison of ADC architectures, [5].

Architecture	Latency	Speed	Accuracy	Area
Flash	Low	High	Low	High
SAR	Low	Low-medium	Medium-high	Low
Folding + interpolating	Low	Medium-high	Medium	High
Delta-sigma	High	Low	High	Medium
Pipeline	High	Medium-high	Medium-high	Medium

The technological evolution, along with the research activity, is the driven factor for this new trend. As new technologies improve the switching speed of modern transistors, the same is not true for their intrinsic gain. This trend favours more digital based architectures over analog solutions, and requires *op-amp free* analog-to-digital converters. As a result, SAR ADCs have played a significant role in advancing the state of the art over the past years and have been a versatile solution for ultra low-power to ultra high-speed applications, [7–11].

The impressive scaling adaptability of SAR ADC has pushed its limits outside the low-power, medium-resolution and medium-speed space, becoming a competitive solution in applications previously dominated by other architectures. This is the case for pipeline ADCs and high-speed medium-resolution applications. The research in pipeline ADCs has focused in new techniques for op-amp-less residue amplification and a push for low stage count [12], leading to significant reductions in power and complexity. Passive residue transfer techniques [13] are an interesting idea, but the

advantage of the interstage gain that relaxes the accuracy of successive stages is lost. Other techniques, like the zero-crossing [14], pulse bucket brigade [15], and ring amplifiers [16] and fully-dynamic amplification [17] are power efficient alternatives to op-amps in generating residue. Pipeline ADCs remain the only topology that can meet the stringent application requirements in high-speed conversion for wireless infrastructures,reaching astonishing performances like the ones in [18].

For ultra high-resolution oversampling and noise shaping remain the way to go. The CMOS technology shrinking has enabled larger bandwidth in oversampled ADCs, extending its operating bandwidth up to a few hundreds of MHz with sampling frequencies as large as 6 GS/s, as proven by [19–22].

Flash ADCs maintain their application target of high-speed low-resolution applications. As stated in [23], *flash ADCs have regained some interest due to the imminent shift from 2-level to 4-level pulse-amplitude modulation (PAM) signaling in high-speed data links.* The state of the art for flash ADCs exceeds the 1 GS/s sampling rate, [24, 25].

In order to boost the performances of data converters, two main approaches have been used: hybrid architectures and time-interleaving solutions. The former aims to merge different architectures in order to take advantage of main benefits from each topology. Most common results are flash-SAR Subranging ADCs, [26], SAR-assisted pipelined ADCs, [27], and extended-range ADCs, [28, 29]. The possible alternatives in merging different architectures are countless and can involve all different approaches. Anyhow, SAR ADC, because of its simple structure, is the most suitable topology for such structures. A flash-SAR Subranging ADC is presented in Chapter 2.

Time-interleaved (TI) architectures increase the conversion rate of a data converter by using a number of converters working in parallel for a simultaneous quantisation of input samples. A suitable combination of the results makes the operation equivalent to a single converter whose speed has been increased by a factor equal to the number of parallel elements. Again, SAR ADC appears to be the most suitable architecture for time-interleaving techniques, as it can reach medium resolution and speed with low power and low area consumption. Some remarkable results have been achieved with TI-SAR architectures, like the ones in [30–32]. However, also other converters lend themselves to time-interleaved solutions, like pipeline ADCs in [33, 34], or flash ADCs in [35, 36]. A TI-extended-range ADC is presented in Chapter 3.

1.4 The State of the Art in SAR ADCs

The basic block diagram of the SAR ADC is descrbed in Fig. 1.2. The main blocks are the S&H, the comparator, the DAC and the SAR logic. This architecture has been known for decades, [37, 38], but interest in such topology only increased in recent years. As a result, countless innovative techniques and approaches have been presented to push the limits of SAR ADCs from the standard low-power medium

resolution and speed operation. To list all of them would be an impossible work, and it is outside of the intent of this thesis. Instead, some of the most recent and renowned ideas will be present here, in order to give the lecturer a rough understanding on the state-of-the-art on SAR ADCs research activity.

The main limitation on the charge redistribution method proposed by McCreary and Gray, [37, 38], is the way the DAC is implemented. The capacitive array area doubles for every extra bit of resolution, limiting the maximum achievable bandwidth and increasing the power consumption. To overcome this problem, several techniques in reducing the capacitive array have been presented, like the C-2C structure, [39, 40], the split-DAC array, [41, 42], or the resistive-capacitive hybrid DAC, [43, 44]. All these solutions aim to reduce the array area to the minimum required by the kT/C noise, independently from the resolution of the ADC. A smaller array reduces the total capacitance to be switched at each step of the searching algorithm, reducing both the power consumption and the DAC settling time. Moving the DAC structure from plain-binary to more complex topologies often degrades the overall linearity of the ADC. The solution in [10] provides a compact and linear solution for DACs operating at high-speed. Another solution, for reducing the area of the array in SAR ADCs operating at medium speeds, is to apply noise-shaping to the DAC in order to improve its resolution, [45].

Another key factor, apart from the DAC structure, is the switching algorithm that performs the successive approximation. In fact, the standard binary approach is not very efficient and consumes most of the power in the very first steps. The solution in [46] improves the efficiency of the switching activity by solving the LSB first, while the Set-and-Down technique samples the voltages directly onto the top plates of the DAC performing the first comparison without switching capacitors, saving time and energy, [47]. Redundant switching sequences are an efficient way of relaxing the settling constraints of the DAC, [48, 49]. The time saved by relaxing the DAC settling is generally much larger than the extra cycles needed to resolve all bits. Some designs use multi-bit per cycle architectures to speed up the searching algorithm in high-speed applications, [50–52].

Asynchronous clocking, [11, 53, 54], has often been used in recent designs to shorten the overall conversion time by removing waiting times during SAR operation. In addition, only one external clock pulse of nominally 12.5% duty cycle is required to define the sampling window and start the conversion, thus saving power in the clock distribution.

Recently, more system-oriented designs are being presented, [55]. This is the case of the study in [56] that uses a loop-embedded input source follower for shielding the large sampling capacitor from the input, making it easier to drive the ADC linearly up to Nyquist.

Fig. 1.12 shows the achieved Walden figure of merit[2] at Nyquist ($\mathrm{FoM}_{W,hf}$) as a function of the conversion rate (f_{snyq}) for ADCs presented in the IEEE International Solid-State Circuits Conference (ISSCC) from 1997 to 2016 (data extrapolated from [58]). SAR and TI-SAR ADCs have been highlighted to better under-

[2] The Walden figure of merit is defined as $\mathrm{FoM}_{W,hf} = \frac{P}{2^{ENOB} 2 f_B}$ in [57]

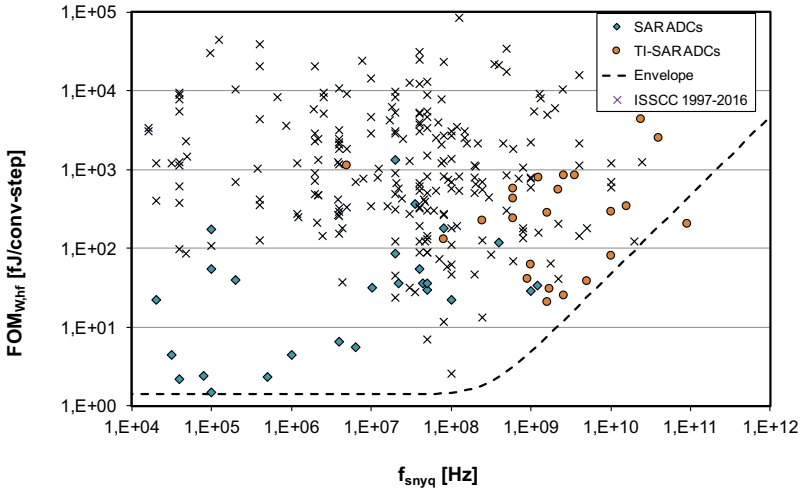

Fig. 1.12 Walden figure of merit at Nyquist ($FoM_{W,hf}$) as a function of the conversion rate (f_{snyq}) for ADCs presented in the IEEE International Solid-State Circuits Conference (ISSCC) from 1997 to 2016. Data extrapolated from [58].

stand the impact of this architecture in the present state-of-the-art. The resulting graph shows how successive approximation data converters are the most efficient solution for low-speed applications from tens of kHz up to tens of MHz, [7, 59]. They are also a very suitable topology for ultra high-speed operation in time-interleaved ADCs, [30, 31]. Even, the cutting edge solution in [60] achieving a figure of merit of 2.6 fJ/conversion-step with a sampling frequency equal to 100 MS/s takes advantage of the SAR algorithm to implement an hybrid architecture.

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Chapter 2
An 8-b 700 MS/s Flash-SAR ADC with 86.7 fJ/conversion-step in 65-nm CMOS

Abstract This project, in collaboration with the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau, foresees the design of a high-speed medium-resolution ADC. In order to achieve higher bandwidth, a 3 stage multi-bit per cycle structure was implemented. The studied solution uses a searching algorithm that allows for relaxed accuracy requirements in the early stages of conversion, and a preamplifier with embedded threshold generation for the multi-bit per cycle architecture. The achieved measured conversion rate is 700 MS/s, with an ENOB as high as 7.4 bits and 5.96 mW of power consumption with a nominal supply voltage of 1.2 V. The measured Walden figure of merit at Nyquist is 86.7 fJ/conversion-step. The ADC was fabricated in a 65-nm CMOS process and the active area of the chip is 150 x 220 μm^2

2.1 Introduction

The telecommunication industry has experienced a rapid growth in the last few decades. The wireless mobile communication standards are the major contributors. This growth has seen many generations from 1G, 2G, 3G, 4G, and even 5G. Each of these generations drives continuous improvement of wireless technologies, higher data rates, larger capacities and richer features compare to the previous ones. However, the capacity requirements and spectrum shortage are increasingly prominent, with the explosive growth of mobile traffic demand. Thus, the bottleneck of wireless bandwidth becomes a key problem of the future wireless mobile communication networks.

While 5G is still in the process of standardization, the industry agrees that access to new, high-band spectrum, as well as millimeter wave (mm-Wave) beamforming and steering, will be fundamental aspects of ultra-dense, high-capacity, low-latency next-generation network. A new 5G mobile network is expected to operate in a range of frequency bands between 6 and 100 GHz, including mm-Wave frequencies, which enables very high (up to 10 Gbps) data rates, and in some scenarios, also

very low end-to-end latencies (less than 5 ms). Therefore, the 5G mobile broadband system [1] can provide multi-gigabit communication services such as high definition television (HDTV) and ultra-high definition video (UHDV). Broadband wireless standards, i.e., IEEE 802.11ad, or WiGig, using RF frequencies around 60 GHz require low-to-medium resolution analog-to-digital converters (ADCs) with a sampling rate in the GS/s range.

Ultra high-speed data converters operating at tens of GS/s use time-interleaved structures for pushing forward the single channel bandwidth limits, [2], [3]. Flash architectures for the core ADCs are an unsuitable solution for resolutions above 6 bits. Instead, the SAR architecture is a convenient choice because of its simple structure and low power consumption. Moreover, modern technologies allow relatively high conversion rates.

The speed of an N-channel time-interleaved structure is N times the conversion-rate of a single channel. A possible strategy is to choose a large interleaving factor. However, integrating many channels turns problematic the clock distribution with unavoidable clock skew that limits the resolution and generates spurious tones. The clock skew causes a non-periodic input sampling and, in order to compensate for the resulting errors, complex calibration methods must be used, [4]. A more effective strategy implies the choice of relatively low values of N and pushes the conversion rate of the single channel to the upper limit allowed by the technology. With 28-nm and 32-nm CMOS technologies, it is possible to exceed 0.7 GS/s, [9, 10]. The use of less advanced technology, like the 65-nm CMOS, enables lower conversion rates (400 MS/s with a two bit/step SAR architecture [11]).

This 65-nm ADC uses a flash-SAR architecture achieving a conversion speed of 700 MS/s with a peak signal to noise and distortion ratio (SNDR) of 47.5 dB. The result, comparable with the one obtained with smaller line-widths, benefits from an architecture composed by the cascade of a 4-bit flash and a two-step SAR converter. Both steps determine 3-bit. The 4+3+3 bits produce the 8-bit output; the applied redundancy avoids calibration in the flash and in the first step of the SAR. The active area of the chip is 150 x 220 μm^2 and the measured total power consumption is 5.96 mW.

2.2 Architecture

The converter is composed by the cascade of a 4-bit flash and a two-step SAR converter. Both steps of the SAR determine 3-bit. The 4+3+3 bits produce the 8-bit output. The conversion steps are called coarse, intermediate and fine stages; the applied redundancy avoids calibration in the flash and in the first step of the SAR. A special preamplifier generates the thresholds required for the SAR ADC to implement the multi-bit per cycle conversion.

The coarse stage uses 14 comparators. The thresholds are nominally set at voltages corresponding to the bins $(24 + n \cdot 16)$, with $n = 0, \cdots, 13$. A thermometric zero at the output identifies the bin interval $0, \cdots, 32$, the thermometric one iden-

tifies 16, ⋯, 48 and so forth, as Fig. 2.1 shows. The comparator accuracy must be ±8 LSBs, i.e. ±37.5 mV for 1.2-V_{pp} reference voltage. The margin is large enough for a properly designed comparator and reasonable clock skew. Therefore, the stage does not need calibration.

The intermediate stage explores the interval chosen by the coarse conversion, using 6 thresholds placed at ±10, ±6 and ±2 LSBs from the central point, as Fig. 2.1 shows. The used redundancy allows a ± 2 LSB accuracy. A thermometric code gives the next interval to explore. Finally, the fine stage uses 7 thresholds placed at ±3, ±2, ±1 and 0 LSBs and requires a full accuracy of ±0.5 LSBs. A logic block combines the outputs from all the three stages and generates the 8-bit word.

Since the full scale voltage is 1.2 V_{pp} and, consequently, the LSB is about 4.7 mV, a careful design and layout require a foreground calibration only for the thresholds used in the fine stage.

Fig. 2.2 illustrates the block diagram of the architecture. A fully differential capacitive array and a single ended flash simultaneously perform the input sampling. The coarse conversion is carried out by the flash, whose output set the MSBs of the capacitive array. The generated residual is the input of a special preamplifier that provides 8+8 differential outputs. Half of these are the input of six fully differential latches whose outputs determine the three Intermediate Significant Bits (ISBs) of the first SAR cycle. The ISBs set the LSBs section of the capacitive array. The new generated residual is fed into the preamplifier and, by using the other outputs, the remaining 3 bits are obtained.

The capacitive array has two sections, one formed by 14 capacitors of value $4C_U$, the other formed by 8 capacitors of value C_U for a total array of $64C_U$. The structure implements a 5-bit DAC suitable for the flash and for the first SAR cycle steps. Since the second SAR cycle determines three bits without using the array, the used approach reduces the capacitive array from $256C_U$ to $64C_U$ (−75%). The nominal value of C_U to satisfy the kT/C noise requirement is 9 fF (C_{TOT} = 576 fF).

Fig. 2.2 also shows the timing of each stage for a complete conversion cycle. After sampling, the flash section carries out the first conversion step. Two subsequent phases (DAC+SAR) complete the remaining conversion steps. Finally, one time slot

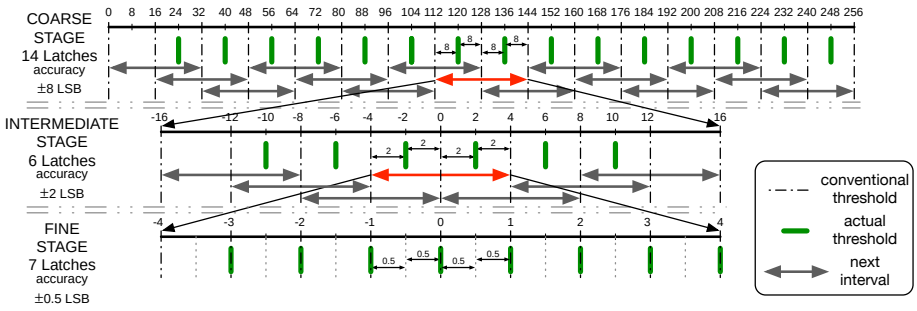

Fig. 2.1 Searching algorithm with redundancy.

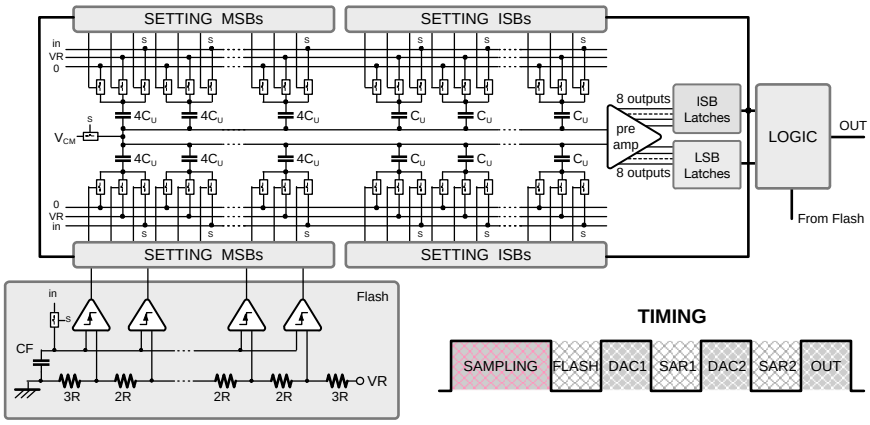

Fig. 2.2 Architecture of the proposed Flash-SAR ADC.

is allocated for the data out. In order to generate all the required phases, the converter needs an input clock and an internal phases generator with frequency twice the sampling frequency.

2.3 Circuit Blocks Design

In this section, the circuital design of the main blocks of the converter is described. They are the the digital logic, the bootstrap circuit, the flash ADC, the comparator and the preamplifier.

2.3.1 Digital Logic

The digital logic provides the phases needed for the converter and the switch driving registers that control the DAC accordingly to the converter stages output.

Thanks to the reduced number of steps of the ADC, granted by the multi-bit per cycle approach, a shift register free timing logic can be implemented. The circuit is based on a frequency divider, as Fig. 2.3 shows. An external clock, *CLK_EXT*, at twice the sampling frequency is divided into two clock signals running at the sampling frequency and shifted by 90°. A combinatory circuit provides all the phases required for the converter to work properly, while internal feedbacks ensure non-overlapping conditions in the generation of the signals. An external signal, *RES_EXT*, can reset the timing logic.

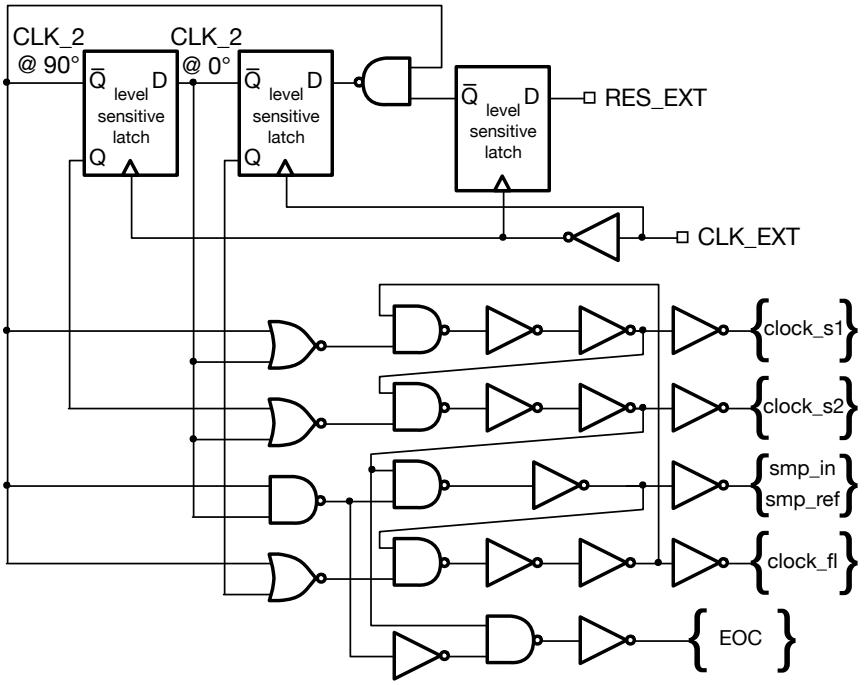

Fig. 2.3 Divider-assisted timing logic.

Apart from the sampling signals, *smp_in* and *smp_ref*, which sample both the input and the reference for the flash ADC, three clock signals are required for start each step of the converter. These are *clock_ fl*, *clock_ s1* and *clock_ s2*. Finally, an end of conversion signal concludes the conversion cycle, i.e. *EOC*. Fig. 2.4 shows the timing diagram of the clock phases.

The switch driving registers introduce a delay in the feedback path of the SAR converter that is added to the DAC settling time. For this reason, it is required to keep this delay as small as possible. The implemented logic, in Fig. 2.5 and Fig. 2.6, introduces a 3-gate delay from when the output of the comparator is ready to when the actual switch at the bottom plate of the DAC is driven.

In the flash section in Fig. 2.5, the clock signal $\overline{smp\_in}$ first sets the outputs such that the switches at the bottom plates of the DAC are all open. In fact, FL_p and FL_n drive the pMOS switches tight to the positive reference, while $\overline{FL_p}$ and $\overline{FL_n}$ drive the NMOS switches tight to the negative reference. After the sampling, the logic is ready to sample the output of the flash comparators OP and ON. Based on the latch decision, either one side or the other is reset choosing which side of the DAC is set to '1' and which is set to '0'. There are 14 such structures connected between each comparator of the flash ADC and each capacitor of the flash section in the capacitive DAC.

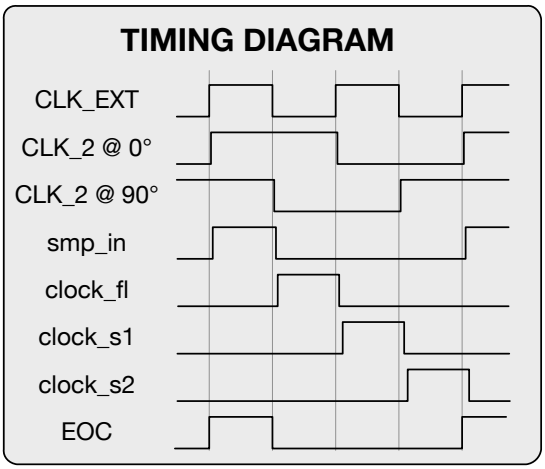

Fig. 2.4 Timing diagram of the phases generated by the logic of Fig.2.3.

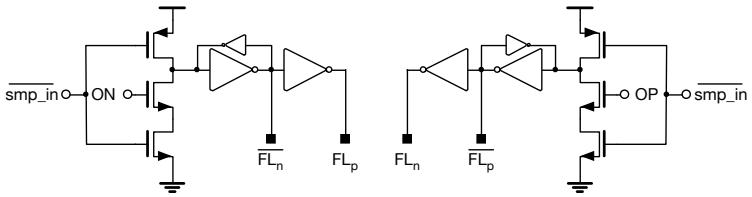

Fig. 2.5 Switch driving registers for the flash section of the capacitive DAC.

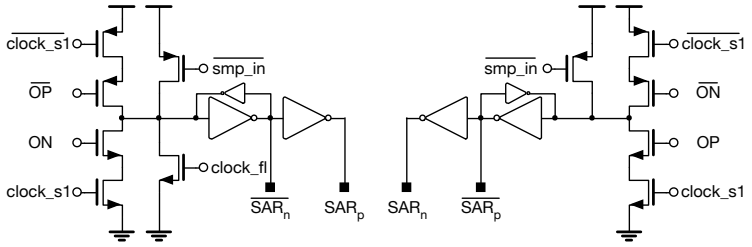

Fig. 2.6 Switch driving registers for the SAR section of the capacitive DAC.

In a similar way, the SAR section is controlled by the circuit in Fig. 2.6. $\overline{smp\_in}$ reset to an open condition the switch drivers. Next, the signal *clock_fl* sets the positive DAC section to '1' and the negative one to '0' for the 'test' step of the SAR algorithm. Finally, the output of the SAR comparators OP and ON are read. The nomenclature used is the same as the one used for the flash section. There are 6 such structures connected between each comparator of the first SAR step and each

capacitor of the SAR section in the capacitive DAC. The remaining two unit capacitances in the SAR section are connected one to the positive reference and the other to the negativa one, following the searching algorithm requirements.

The digital logic is completed by a bank of registers that sample the output synchronous to the rising edge of the end of conversion signal, and a decoder that provides a binary output to the logic analyzer during testing.

2.3.2 Bootstraped sampling switch

Sampling switches in ADCs introduce two main errors, due to charge injection and non-linearities of the ON resistance of the switch. The first effect mainly results from the generation and the dissolution of the conductive channel sitting under the gate when the transistor is in the ON state. The channel charge in a MOS transistor working in a triode region is equal to

$$\Delta Q = WL_{eff}C_{OX}(V_{GS} - V_{th}) \tag{2.1}$$

where W and L_{eff} are the effective width and length of the transistor, C_{OX} is the oxide capacitance per unit area, and (V_{GS} - V_{th}) is the overdrive voltage.

When the switch is turned off, the charge of the channel needs to disappear. The only nodes where the charges can go are the two terminals of the switch itself. A fraction of the total charge will affect one terminal, the remaining will influence the other. The charge going to the sampling capacitance will generate a voltage offset that depends on many factors: the technology, the sizing of transistors used, the input voltage, and the clock timing. Most importantly, the offset is input dependant, which leads to harmonic distortion in the sampling operation.

The second error derives from the dependance from the input signal of the ON resistance of the switch. In fact, the ON resistance of a MOS switch is equal to

$$R_{on} = \frac{1}{\mu \frac{W}{L} C_{OX}(V_{GS} - V_{th})} \tag{2.2}$$

where μ is the mobility of the charges (either electrons or holes).

In both cases, the overdrive voltage (V_{GS} - V_{th}) is a function of the input signal, being $V_S = V_{IN}$. Bootstrapping is a technique, which ideally removes the signal dependency of both issues, by ensuring a constant overdrive voltage to the switch. Fig. 2.7 describes the technique, which is divided into to phases. First, the bootstrap capacitance C_B is pre-charged to V_{DD} and the sampling switch gate is tight to ground. During the sampling phase, C_B is connected between gate and source of the switch, ensuring a constant overdrive voltage equal to (V_{DD} - V_{th}) that is independent from the input signal. This ensures a constant ON resistance of the MOS working in the triode region, and, if the conditions at the node V_O does not change, a constant charge injection of the switch when it opens. Besides, the nMOS sam-

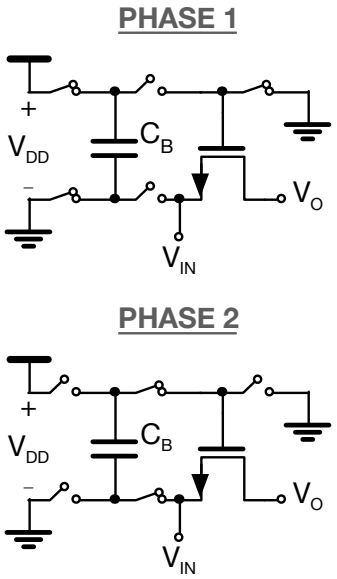

Fig. 2.7 Description of the bootstrapping technique.

pling switch can close also for input signals that are larger than (V_{DD} - V_{th}) and no pass-transistor logic is required.

The bootstrap clock is generated by the circuit in Fig. 2.8, using the structure presented in [5]. During $\overline{CLK}$, the capacitor C_B is pre-charged to V_{DD} by M_1 and M_2. M_3 and M_4 tight to ground the output clock CLK_{OUT} and turn off M_8 and M_{10}, while M_5 turns off M_7. When CLK goes high, M_6 turns on M_7 which turns on M_8. M_8, together with M_9, samples V_{IN} at the bottom plate of C_B. This boosts the top plate of C_B to $V_{DD} + V_{IN}$. M_7 provides to the output CLK_{OUT} this value attenuated by the parasitic capacitance C_P. The main contribution to this parasitic is the one of the bulk parasitic of M_7. Therefore, there is a tradeoff between the effectiveness of the bootstrap logic and the maximum sampling speed achievable by the circuit. M_4 reduces the V_{DS} and V_{GS} applied to M_3 during the CLK phase, while M_{10} ensures that the V_{SG} of M_7 never exceeds V_{DD}. M_4 and M_3 are made large enough not to introduce excessive jitter noise in the falling edge of the sampling clock.

The bootstrapped clock is then distributed both to the flash ADC and the capacitive DAC in the SAR section. Since the flash ADC is single-ended, there is imbalance between the logic that is connected to the positive and the negative polarities of the input signal. Dummy switches are placed for the negative one, in order to balance the load seen at CLK_{OUT} and ensure symmetry.

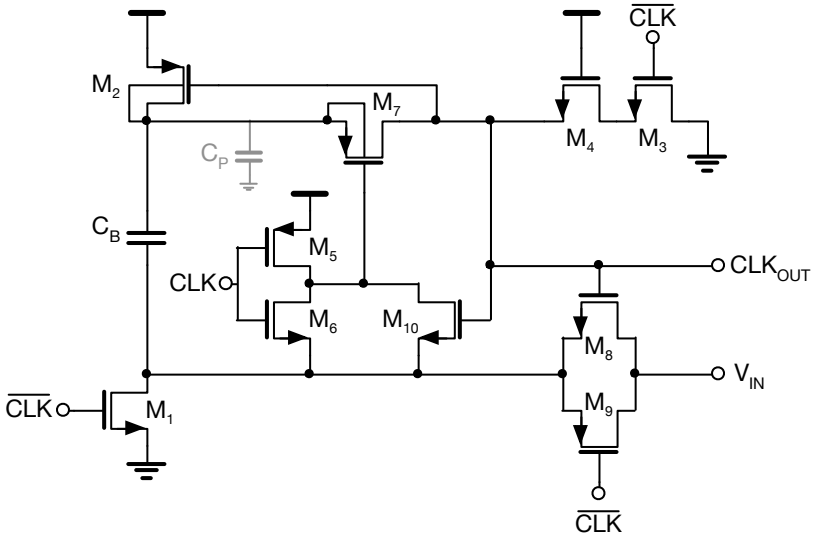

Fig. 2.8 Schematic view of the bootstrap logic.

2.3.3 Flash ADC

The flash ADC implements the coarse conversion step in the search algorithm. Thus, it is required to design a 14-threshold converter, with an accuracy for the thresholds of ±8 LSBs. A careful design should not ask for calibration, as the resolution requirements are relaxed by a digital correction technique.

The last stages of the converter are implemented by a SAR ADC, which has a fully-differential rail-to-rail input range. If a similar structure is implemented in the flash ADC, a fully differential comparator should be designed. This not only complicates the circuit implementation, but it also increases the power consumption of the converter. Instead, a single-ended rail-to-rail ADC is used and the input stage of the comparators are either pMOS or nMOS accordingly to the common-mode voltage that they are analyzing. This is possible, as the coarse stage does not need to produce a residual voltage, but only a digital word for the MSBs to be used in the next stages. Then, moving from a single ended output to a differential one only requires a logic inverter.

The reduced mobility of holes makes pMOS input-stage comparators slower, requiring larger transistors to meet the speed constraints of the converter. This translates into larger power consumption, compared to the nMOS counterpart. For this reason, pMOS comparators are only used for the low input common-mode region. The presented architecture uses only five pMOS comparators, and nine nMOS ones.

The thresholds are generated with a thermometric resistive ladder. Unsilicided n+ polysilicon resistors are used for achieving high matching accuracy in the resistive

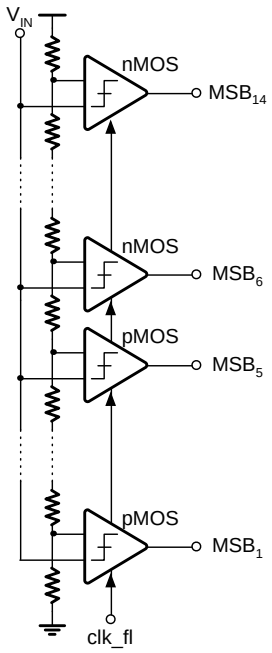

Fig. 2.9 Flash converter architecture.

string, [6]. These resistors present a lower sheet resistance compared to the silicided version. In this way, minimum width resistors can achieve the required unit value for the resistive string, reducing the area occupied by the flash references. The final string is composed by 16 unit resistors of 60 Ω.

The resulted architecture is the one in Fig. 2.9. The applied redundancy in the searching algorithm allows using a very simple structure. Besides, the thermometric DAC used in the cascaded SAR does not call for a decoder, so that the output of the comparators are fed directly into the next stage.

Errors in the flash come from three main factors: relative offset between the comparators, mismatch errors in the threshold generation, and sampling switch charge injection imbalance. While the first two can be overcome by a careful design, the last one might not present a straightforward solution. In fact, in a single-ended solution, the sampling switch is present only in one input of the comparator, while the other one is directly connected to the resistive string, like in Fig. 2.10 (a) for an pMOS case. This generates asymmetry in the clock feedthrough seen by the two inputs of the comparators. The charge injection from the sampling switch gives rise to a voltage drop at the input node, that can generate an error at the output code. The error is not negligible as the sampling switches are relatively large, the sampling clock (*smp_in*) is bootstrapped and the sampling capacitance is kept as small as possible. Normally, this error is treated as an offset of the converter as the charge

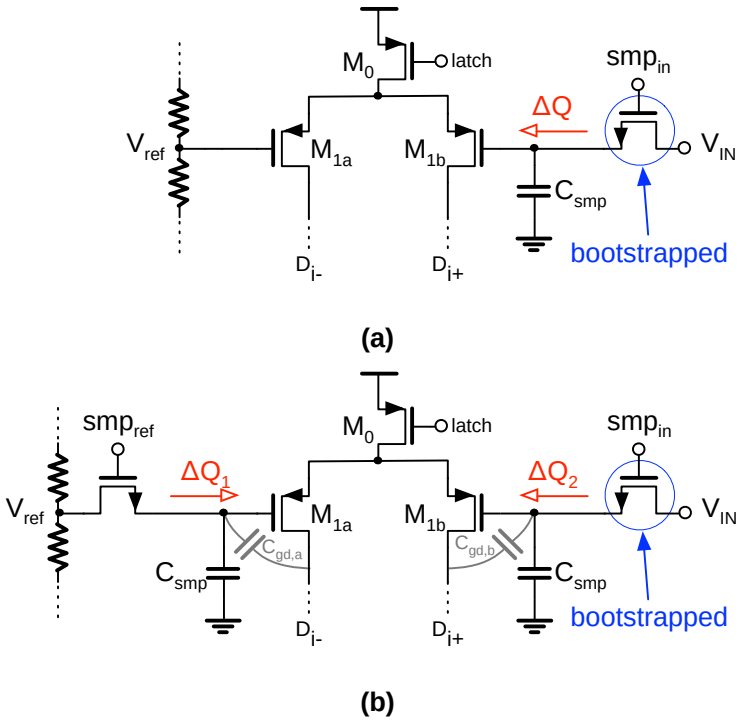

Fig. 2.10 Comparator input stage in flash ADC for pMOS part. (a) Standard approach. (b) Proposed solution.

injection is similar in all the comparators, apart from the sampling switches random mismatches. Anyway, in order to avoid calibration in the coarse stage, a solution addressing this problem has been implemented. Symmetry in the proposed structure was made possible by sampling also the reference voltage, as Fig. 2.10 (b) shows. The idea is to equalize the charge injection from both sides in order to generate a common-mode error that is rejected by the differential input pair of the comparator. In order to do so, also the sampling clock for the reference (*smp_ref*) should be bootstrapped. This would require a bootstrap circuit for each reference voltage, which is not affordable due to area and power constraints. Instead, a different sizing of the sampling switches is done in order to compensate for the overdrive voltage mismatch.

The charge injection of an nMOS switch opening can be derived from (2.1). The overdrive voltage in the input sampling switch is constant and, in first approximation, equal to V_{DD} thanks to the bootstrap circuit, so also the charge injection is constant and it does not depend from the input signal. Also the charge injection in the reference sampling switch is constant, but in this case the overdrive voltage is

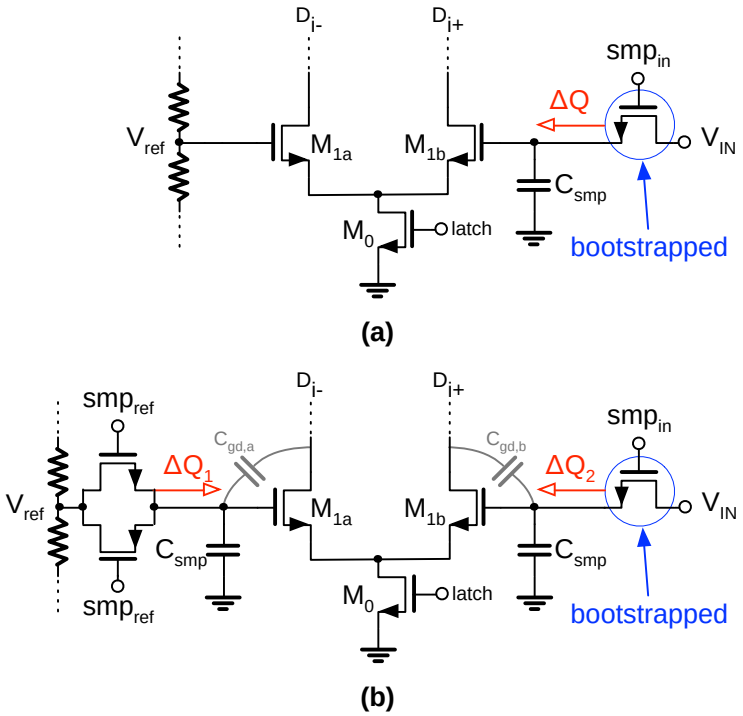

Fig. 2.11 Comparator input stage in flash ADC for nMOS part. (a) Standard approach. (b) Proposed solution.

not equal to V_{DD}. Thus, a fine-tuning of the sampling switches can equalize the charge injection ΔQ_1 and ΔQ_2 in Fig. 2.10 (b).

In the upper part of the flash ADC, pMOS switches are required for sampling the reference. Hence, the charge injection is different in polarity as the channel in pMOS is formed by holes and not by electrons. In this case, pass-transistor gates are used for equalizing the charge injection, Fig. 2.11. The pMOS switch is used to properly sample the reference, while the nMOS switch provides the required ΔQ_1 for the fine-tuning technique. It is known that this technique works correctly when the input common mode voltage is around $V_{DD}/2$, which is not the case here. Thanks to the low accuracy requirements of the flash ADC, the technique is also effective at higher common mode voltages.

2.3.4 Comparator with built-in preamplification

The delay of a comparator depends significantly of the differential input amplitude. For this reason, it might seem beneficial to place a preamplifier driving the latch. But, the delay introduced by the preamplifier needs to be accounted for, making the actual benefit in speed negligible. Besides, a preamplifier would increase area and power consumption of the comaparator. Instead, the idea is to incorporate the amplification feature into the latch itself, [7].

A comparison of the input stage of a static preamp and the input of the sense amplifier dynamic latch shows that the circuit are equal, Fig.2.12. The difference is in the role of the transistor connected to the common sources. In one case it is a current source, in the other is a switch. This suggest to merge the two functions to obtain the circuits of Fig. 2.13. The dynamic latch integrates the preamplification function into the latch itself. The circuit, in the latch phase, works in the same way as the conventional sense amplifier latch. In the reset phase, the current I_{SS} flows into the input pair, while the regenerative loop transistors are diode connected by the reset. The result is a static amplification of the input signal equal to the square root of the aspect ratios of input transistors and diode connected load. The parasitic capacitance at the output of the preamplifier is significantly reduced, compared to the one seen by an extra preamplifier in front of the latch, because it is only due to the one at nodes D_i+ and D_i-. This increases the speed of the comparator with respect to an equivalent latch with a preamplifier in front.

The solution was compared to a sense amplifier latch, [8], and the same sense amplifier latch driven by a preamplifier. The tail current used for the preamplifier and the proposed solution is the same. Figure 2.14 shows the results. An effective advantage in terms of speed is achieved by the proposed solution. This is due to two main reasons. First, the preamplifier is embedded into the latch and this does not

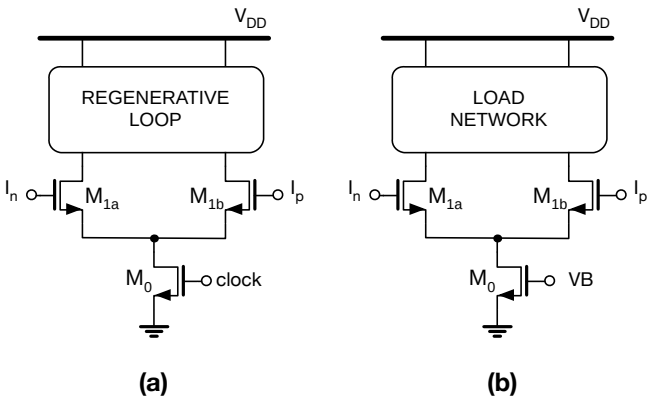

Fig. 2.12 Comparison between input stages of dynamic latch and preamplifier. (a) M_0 is a switch. (b) M_0 is a current generator.

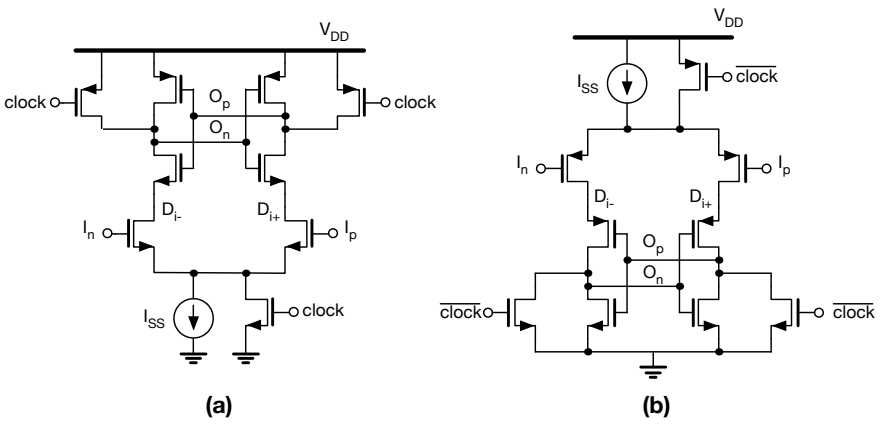

Fig. 2.13 Improved sense amplifier latch schematic. (a) nMOS input stage. (b) pMOS input stage.

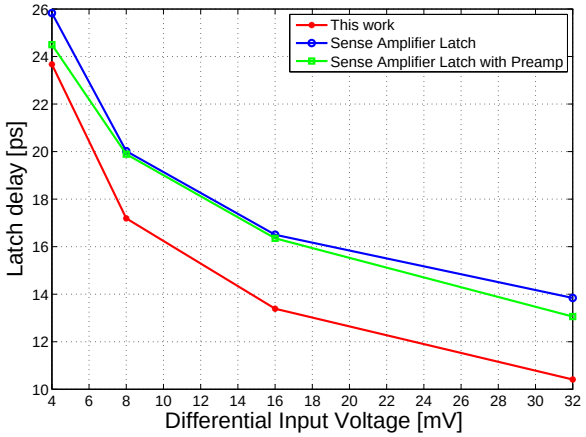

Fig. 2.14 Simulated pre-layout time response versus differential input for this work, the SA latch and the preamplified SA latch.

increase the parasitic capacitance that limits the dynamic gain. Second, the comparator starts the latch phase with its outputs already unbalanced like in the case of a static class AB comparator.

2.3.5 Preamplifier with embedded thresholds generation

The small value of the quantization step in the two phases of the SAR conversion does not provide a reliable operation for the latches, at the required bandwidth. Therefore, a preamplifier is required for relaxing the offset specifications of the comparator. Besides, the need of preamplification has been combined with the need for generating the thresholds for the converter, reducing notably the power consumption.

Fig. 2.15 describes the conceptual approach. It is a simple differential stage with resistive load, a circuit solution that grants high speed. The resistive load on the right branch is divided in two parts, so that equal voltages V_A and V_C require an input shift, V_{sh}, across the differential pair. Supposing that the shift causes a negligible signal current, it is necessary to have

$$2R_T g_m V_{sh} \simeq R_X \frac{I_B}{2}$$

The preamplifier gain is

$$A_P = 2g_m R_T$$

The required shift voltage depends on the design quantities W/L, I_B, and R_X/R_T. Suitable values of those parameters provide V_{sh} = ±1, ±2, ±3, ±6, ±10 LSBs.

The accuracy of the shift depends on the accuracy and linearity of g_m, as the ratio among the resistors is well matched. For the first step of the SAR, the possible error is compensated for by the redundancy. For the second step, the circuit uses foreground calibration. The control of the bias current, I_B, provides a rough global calibration, before the fine calibration embedded in the latch. The nominal value of I_B is 500 μA, ensuring very low power operation of the preamplifier.

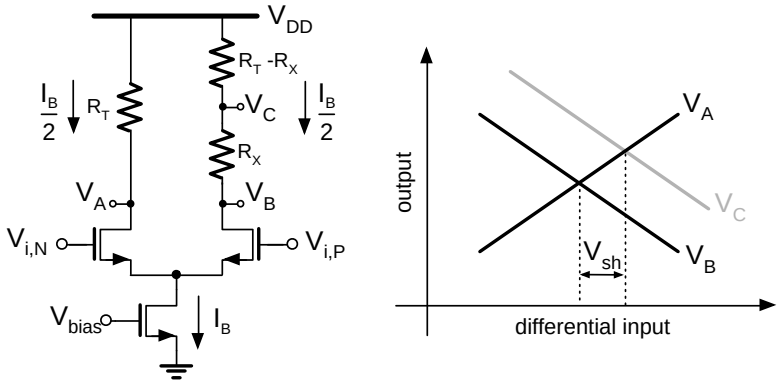

Fig. 2.15 Preamplifier with embedded thresholds generation.

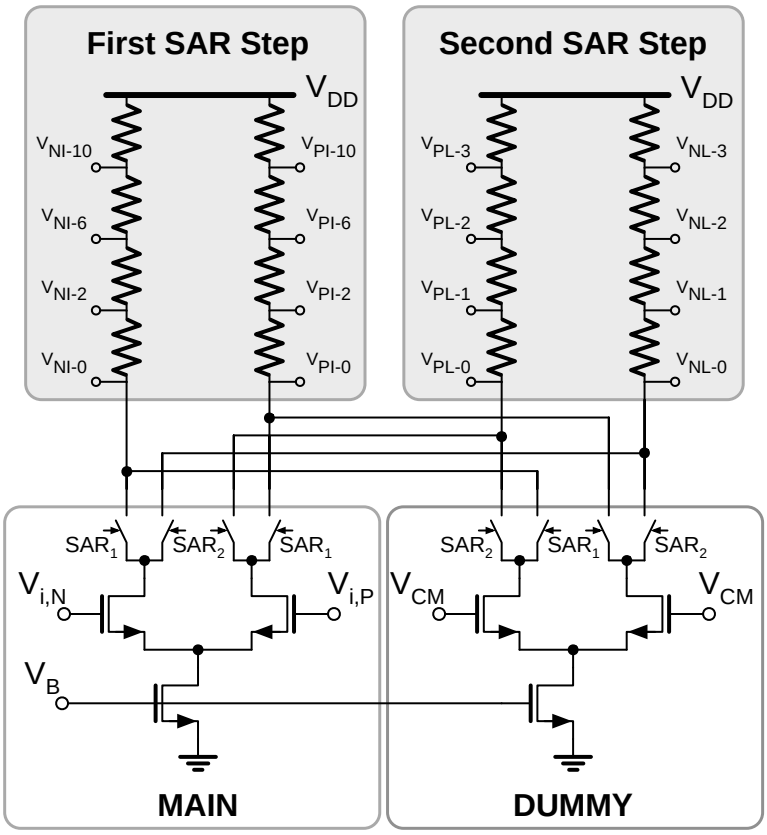

Fig. 2.16 Preamplifier schematic with dummy structure and double output branch.

Fig. 2.16 shows the schematic diagram of the multi-output preamplifier. It uses a single differential pair that can be connected to two resistive string loads, one for the first step of the SAR, the other for the second one. The values of the resistors optimize the gain for the two cases. The use of the same differential pair ensures a good matching of the operational conditions in the two modes. In order to prevent output voltages switching when the resistive load is not used, a dummy differential pair replaces the main structure in the disconnected resistive loads.

The output voltages drive the latches following the connection scheme shown in Table 2.1. The latches used in the SAR section section are again the one presented in Fig. 2.13(a).

Table 2.1 Latches bank connections to preamplifier outputs.

First SAR step latch	$\mathbf{V}_{ip}$	$\mathbf{V}_{in}$	Second SAR step latch	$\mathbf{V}_{ip}$	$\mathbf{V}_{in}$
-10 LSB	V_{PI-0}	V_{NI-10}	-3 LSB	V_{PL-0}	V_{NL-3}
-6 LSB	V_{PI-0}	V_{NI-6}	-2 LSB	V_{PL-0}	V_{NL-2}
-2 LSB	V_{PI-0}	V_{NI-2}	-1 LSB	V_{PL-0}	V_{NL-1}
+2 LSB	V_{PI-2}	V_{NI-0}	0 LSB	V_{PL-0}	V_{NL-0}
+6 LSB	V_{PI-6}	V_{NI-0}	+1 LSB	V_{PL-1}	V_{NL-0}
+10 LSB	V_{PI-10}	V_{NI-0}	+2 LSB	V_{PL-2}	V_{NL-0}
			+3 LSB	V_{PL-3}	V_{NL-0}

2.3.6 Calibration system

The calibration system is embedded in the latches of the fine step, as shown in Fig. 2.17. The solution uses an extra differential input pair, connected to an off-chip differential signal, for forcing an offset to the comparator. A foreground calibration of CAL_n and CAL_p generates the required offset that compensates for the error in the threshold generated by the preamplifier. The ratio between the input differential pair and the auxiliary one is chosen to be 4 in order to guarantee enough trimming range, without reducing the sensitivity of the comparator to the actual input signal.

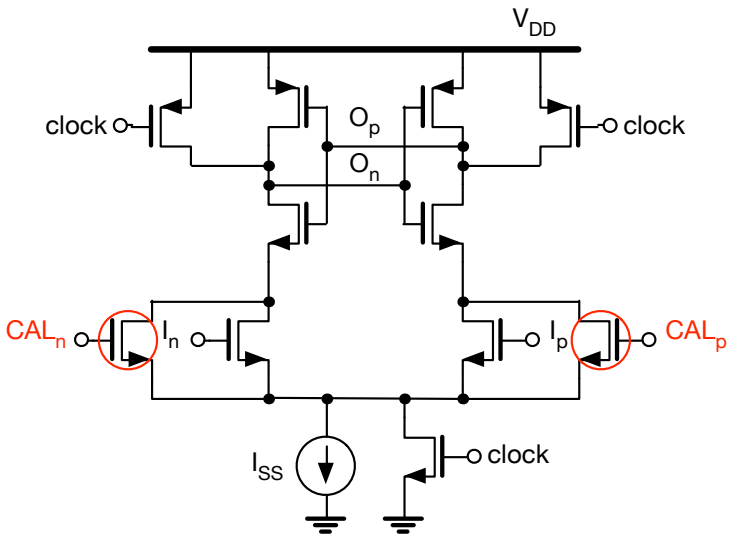

Fig. 2.17 Calibration system embedded in the latch.

2.4 Measurement Results

This ADC has been fabricated in a 65-nm 1.2-V CMOS process. The design uses a standard multi-chip module of 1000 x 1500 μm^2, but the active area of the converter is 150 x 220 μm^2. Fig. 2.18 depicts the whole chip microphotograph and a magnified view of the active area where the main circuit blocks have been highlighted. The track & hold circuit is placed in the top part of the ADC. A tree structure brings the sampling clock and the input signals to the flash ADC and to the capacitive DAC. At the bottom, the preamplifier with the latches bank forms the comparators of the SAR ADC. The logic is distributed along the chip and does not occupy a significant amount of area. The output is decimated on chip by a factor 25, in order to relax the measurement equipment operation speed.

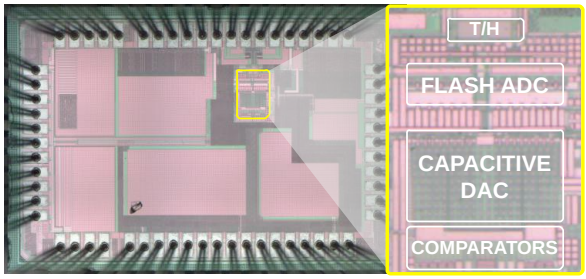

Fig. 2.18 Chip microphotograph.

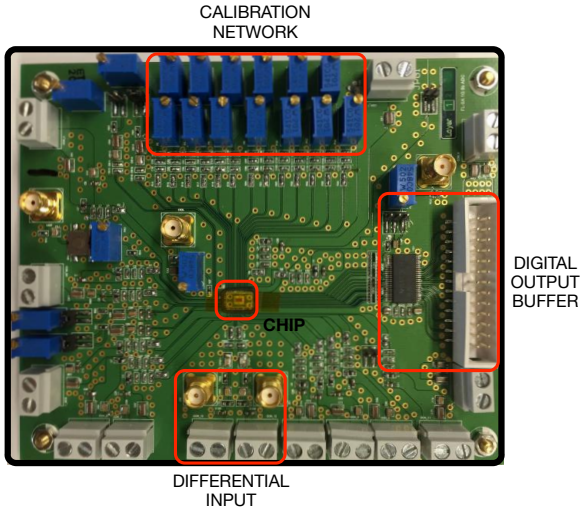

Fig. 2.19 Test board.

Fig. 2.19 shows the test board used for measuring the ADC. The chip is directly bonded to the board in order to reduce the parasitics for the high-speed traces, especially the one that brings the clock signal. The outputs of the converter are decimated on-chip, and a buffer in the board connects them to the logic analyzer. The calibration network is generated on-board by a set of resistive dividers on the top side of the board. The remaining input signals (voltage references and supply voltages) are provided directly by the lab instrumentation.

Fig. 2.20 shows the SNDR measured with a full-scale sine wave input signal as a function of the sampling frequency for different supply voltages. At the nominal supply voltage (V_{DD} = 1.2 V), the ENOB is 7.5 bits up to f_s = 550 MS/s and slightly drops at higher sampling frequencies. At f_s = 700 MS/s, the ENOB is 7.4 bits. The

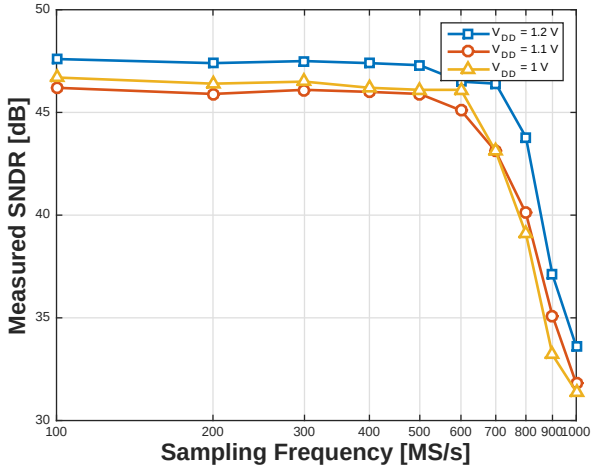

Fig. 2.20 Measured SNDR as a function of the sampling frequency for different supply voltages.

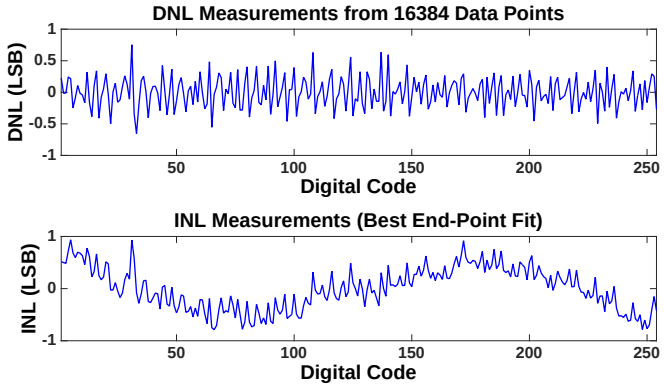

Fig. 2.21 Measured DNL and INL.

figure shows that the circuit looses about 0.25 bit at lower supply voltages and shows a lower speed of operation.

Fig. 2.21 shows the measured DNL ([-0.65 : +0.75] LSBs) and the best fit INL ([-0.79 : +0.94] LSBs). In order to account for possible non-linearities occurring at high speed, the figures result from the histogram method with a sampling frequency as high as f_s = 700 MS/s.

Fig. 2.22 gives the measured output spectra for f_s equal to 500 MS/s when the input frequency is low (Fig. 2.22(a)) and when it is near Nyquist (Fig. 2.22(b)). The achieved SNDRs are 47.3 dB and 45.2 dB while the ENOBs are 7.56 bits and 7.22 bits, respectively. Third harmonic tones at -57 dB$_{FS}$ and -52 dB$_{FS}$ limit the spurious free dynamic range (SFDR). The FFTs have 16384 points and the outputs were decimated by 25x. Similar tests were performed for f_s equal to 700 MS/s, Fig. 2.23. The achieved SNDRs are 46.4 dB and 41.6 dB while the ENOBs are 7.42 bits and

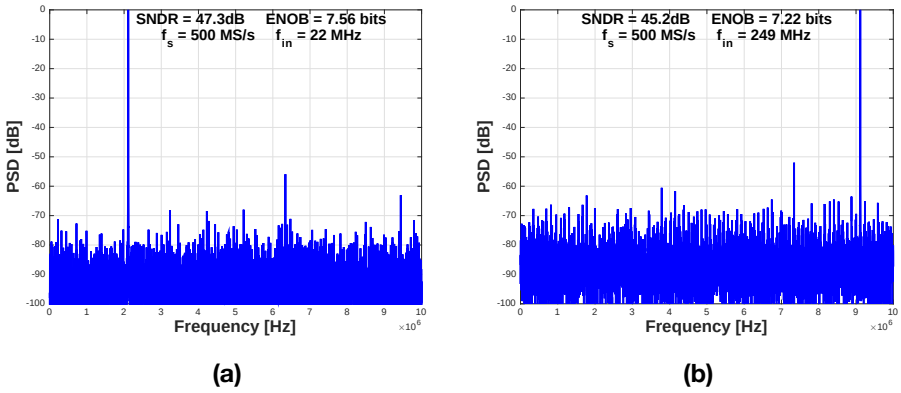

Fig. 2.22 Measured output spectrum at f_s = 500 MS/s. (Output decimated by 25x). (a) Input signal at 22 MHz. (b) Input signal at 249 MHz.

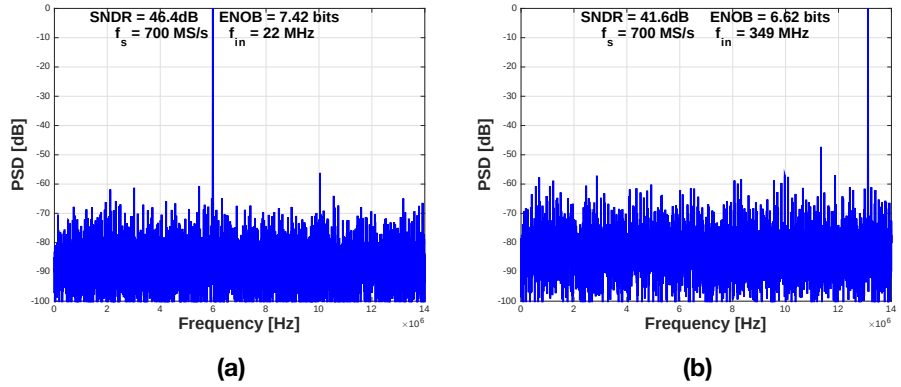

Fig. 2.23 Measured output spectrum at f_s = 700 MS/s. (Output decimated by 25x).(a) Input signal at 22 MHz. (b) Input signal at 349 MHz.

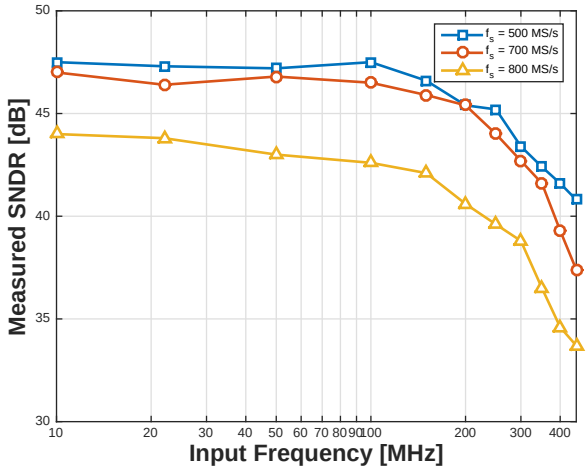

Fig. 2.24 Measured SNDR as a function of the input frequency for different sampling frequencies.

6.62 bits, respectively. Third harmonic tones at -56 dB$_{FS}$ and -47 dB$_{FS}$ limit the spurious free dynamic range (SFDR).

Fig. 2.24 shows the measured SNDR at the nominal supply voltage as a function of the input signal frequency for different sampling frequencies. The performances drop significantly for f_s = 800 MS/s for input frequencies higher than 200 MS/s. The drop at near Nyquist frequencies is due to the jitter noise introduced by the sampling network.

The total power consumption is 5.96 mW (V_{DD} = 1.2 V). The figure of merit at f_s = 0.7 GS/s is 86.7 fJ/conversion-step. Fig. 2.25 shows the power breakdown of

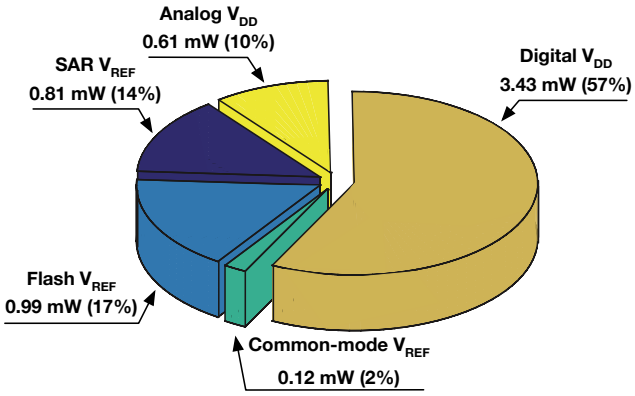

Fig. 2.25 Power breakdown of the ADC.

Table 2.2 Performance summary and comparison table.

	[9]	[10]	[11]	**This Work**
Technology	28 nm	32 nm	65 nm	**65 nm**
Resolution	**8 bits**			
Supply Voltage	1 V	1 V	1.2 V	**1.2 V**
SNDR near Nyquist	43.3 dB	39.3 dB	44.5 dB	**41.6 dB**
Sampling Speed	0.75 GS/s	1.2 GS/s	0.4 GS/s	**0.7 GS/s**
Power	4.5 mW	3.06 mW	4 mW	**5.96 mW**
FoM/conv.-step	50 fJ	34 fJ	73 fJ	**86.7 fJ**
Area	0.004 mm^2	0.0015 mm^2	0.024 mm^2	**0.03 mm^2**

the ADC, identifying in the digital section and the latches as the power hungry part of the circuit. Scaling down the technology to 32 nm would reduce by a factor 4 that contribution, with a reduction of the consumed power by about 45%.

Table 2.2 summarises the ADC performance and provides a comparison with state-of-the-art single channel SAR ADCs. This work results faster than latest single channel ADCs presented in the same technology node with 8-bit resolution.

2.5 Conclusions

In this chapter, the prototype of a 700 MS/s single channel Flash-SAR ADC in 65-nm CMOS process was presented. A multi-bit per cycle search algorithm is used in order to speed up the conversion. Redundancy and a novel resistive interpolated preamplifier are implemented to overcome the thresholds generation limit and to reduce the calibration procedure complexity. A novel latch structure that shows a significant improvement in speed was presented. A simple, yet effective solution for the flash ADC sampling network solves the asymmetry problems in single-ended architectures. A divider-based phase generator gets rid of the conventional shift register approach in the SAR ADC, and a dynamic logic minimizes the feedback loop delay of the converter.

The main limitation for the achievable bandwidth of the ADC is the sampling network, while the architecture proves its effectiveness even at higher speeds than 700 MS/s. A technology scaling would be beneficial, especially in the power consumption reduction, as the major contribute to it comes from the digital logic blocks.

Measurement data show competitive results, especially if compared to same technology node ADCs. The achieved figure of merit at Nyquist is 86.7 fJ/conv-step with a sampling rate equal to 700 MS/s. This results places itself close to the state-of-the-art in the $\mathbf{FoM}_W$ **vs** $\mathbf{f}_S$ plot from Murmann's dataset [12], shown in Fig. 2.26. For fair

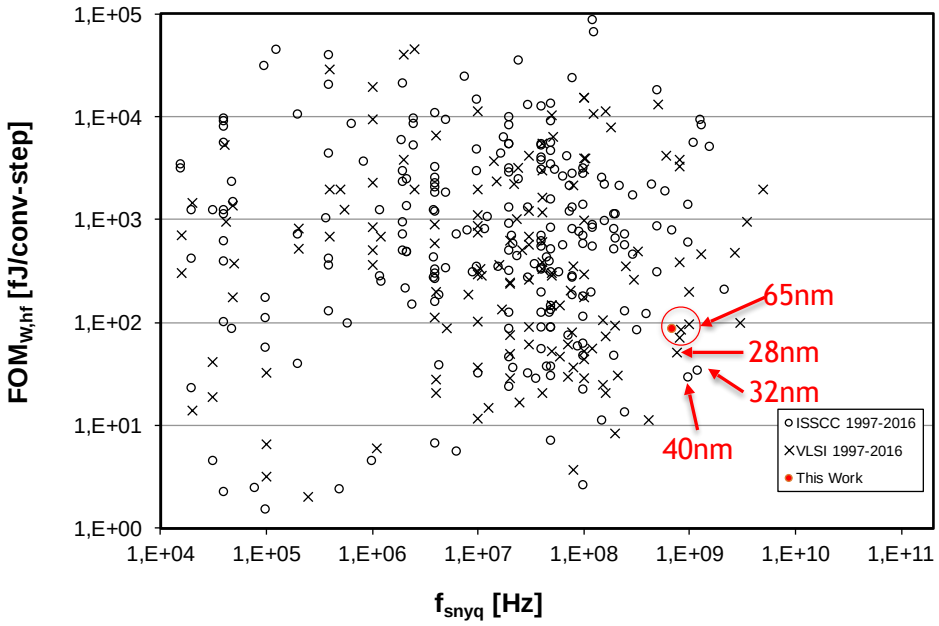

Fig. 2.26 Walden figure of merit at Nyquist ($FoM_{W,hf}$) as a function of the conversion rate (f_{snyq}) for single-channel ADCs with ENOB higher than 5 bits presented in the IEEE International Solid-State Circuits Conference (ISSCC) from 1997 to 2016. Data extrapolated from [58].

comparison, only single-channel ADCs with ENOB higher than 5 bits are displayed in the figure.

The description of this ADC appeared in the proceedings of the *IEEE European Solid State Circuits Conference* (ESSCIRC) in September 2016, [13].

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Chapter 3
A 14-b 33.6 V DR Extended Range ADC for Battery Monitoring

Abstract This project was done in collaboration with AMS Italy and its goal was to design an ADC for monitoring the voltages of a stack of 8 Li-Ion batteries. The converted voltage range for each battery is 3 - 4.2 V, with a maximum nominal input voltage of 33.6 V. High-voltage switches and a single high-voltage capacitor make the high-voltage track & hold. The remaining part of the circuit operates at a nominal 5-V supply. An interleaved extended-range ADC makes the architecture. It converts the 8 channels in 720 μs. The battery monitor has been fabricated in a 0.35-μm triple-well 5V HV CMOS process with drain extended MOS high-voltage devices. The prototype active area is 1300 x 650 μm^2 and the measured total power consumption is 3.64 mW. The measured input referred noise and residual offset are 177.9 μV and 642.5 μV, respectively.

3.1 Introduction

The management of Li-Ion batteries used in electric vehicles requires to measure the voltage across each battery about every 1 ms with an accuracy of 1 mV or better. Since the voltage of a Li-Ion cell can go up to 4.2 V, stacking several elements requires complex high-voltage circuit solutions. This prototype monitors up to 8 batteries, with a relatively simple high-voltage section.

The circuit provides a digital conversion of each single cell voltage for a suitable processing of the battery monitor. Existing solutions [1–3] employ level shifters and high-voltage control logic for a sequential sampling of the inputs; then, a SAR or a ΣΔ ADC estimates the outputs. Having multiple high voltage sections grows the silicon area; moreover, sampling the inputs sequentially is not optimal since a common need is to provide the A/D result of (almost) simultaneous samples. The need of "nearly simultaneous" conversion derives from the high dynamic load changes seen by the batteries and from the necessity to measure all the cell voltages under the same condition. The solution in [4] uses a parallel approach with multiple level shifters and multiple ADCs. Although this provides a simultaneous conversion,

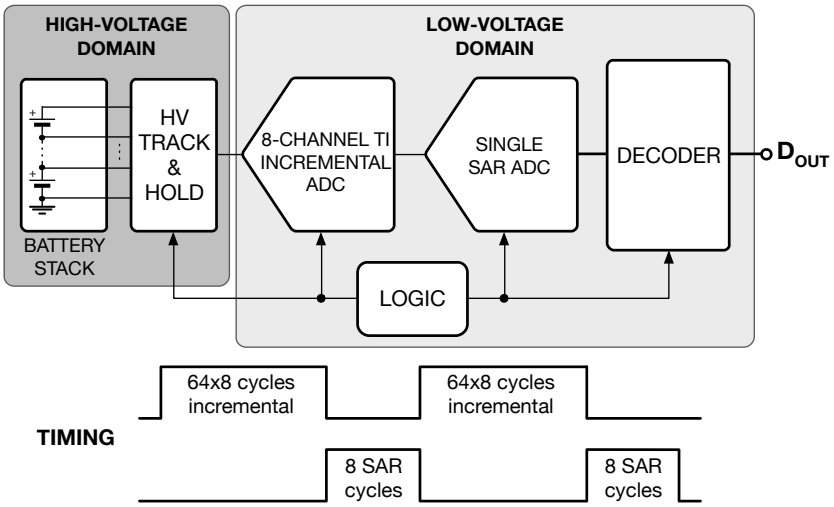

Fig. 3.1 Battery monitor architecture.

inter-channel mismatch becomes a major limitation to the achievable resolution in this kind of architectures.

This design employs the time-interleaving (TI) of 8 extended range ADCs, [5,6], made by a 6-bit first order incremental converter and an 8-bit SAR. The track & hold uses only one high-voltage capacitor and 8 high-voltage switches to sample the input, as shown in Fig. 3.1. The architecture shares the comparator used in the incre-

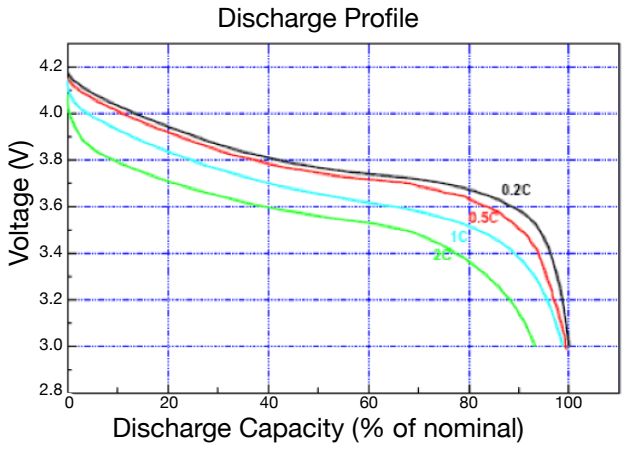

Fig. 3.2 Battery discharge profile.

mental section and uses a single SAR ADC for all the eight channels. The ADC dynamic range is set accordingly to the Li-Ion battery charge-discharge profile, Fig. 3.2, resulting in a conversion range from 3 to 4.2 V.

This ADC has been fabricated in a 0.35-μm triple-well 5V HV CMOS process with drain extended MOS high-voltage devices. The prototype active area is 1300 x 650 μm^2. The master clock frequency and the measured total power consumption are 1 MHz and 3.64 mW, respectively. The measured input referred noise is 177.9 μV and the residual offset is 642.5 μV.

3.2 Architecture

The extended-range conversion of this design foresees two steps. First, a coarse conversion is carried out by an 8-channel time-interleaved first-order incremental ADC. With an oversampling ratio (OSR) equal to 64, the coarse resolution is 6 bit. Each incremental step requires 10 clock cycles (1 for reset, 1 for a dummy channel, and 8 for all the channels), resulting in 640 clock cycles for the coarse stage. Once the first phase is completed, part of the incremental converter is re-arranged as a SAR ADC for the residual voltage conversion. The fine conversion is carried out in 10 clock cycles for each channel, resulting in 80 clock cycles for the whole fine stage. In total, 720 clock cycles are required for measuring the whole battery stack. Hence, the sampling rate of the overall ADC is equal to 11.1 kS/s (1.39 kS/s each channel), if f_{clk} = 1 MHz. In order to achieve the 14-bit resolution required for the entire ADC, the incremental stage uses a two-stage op-amp with large DC gain and suitable bandwidth. Simulation results show that a DC gain of 115 dB and a bandwidth of 20 MHz obtained by a chopper stabilised two-stage amplifier (with a cascode as first stage) match the requirements. The comparator is a dynamic latch with a single stage preamplifier.

3.2.1 Coarse step: 8-channel TI incremental ADC

Fig. 3.3 shows the ADC architecture during the incremental phase. A high-voltage MIM capacitance, C_S, works as sampling element of all the channels. C_{CM} provides a shift equal to $V_{CM,B}$ = 3.6 V, so that a reference voltage of ±0.6 V makes the conversion range from 3 to 4.2 V. Eight nominally equal feedback capacitors, $C_{ch,i}$, accumulate the charges of the interleaving architecture, and the capacitive bank, C_{SAR}, made by a combined 5b-binary and 3b-C-2C structure (Fig. 3.6), operates as an injection element as required by the ΣΔ incremental function. The left plate of C_S steps up by one cell at each cycle and injects into the virtual ground, together with C_{CM} and C_{SAR}, the charge

$$Q_{inj,in} = C_S V_{B,i} - C_{CM} V_{CM,B} + C_{SAR} \frac{V_R}{2} (2D_i - 1) \tag{3.1}$$

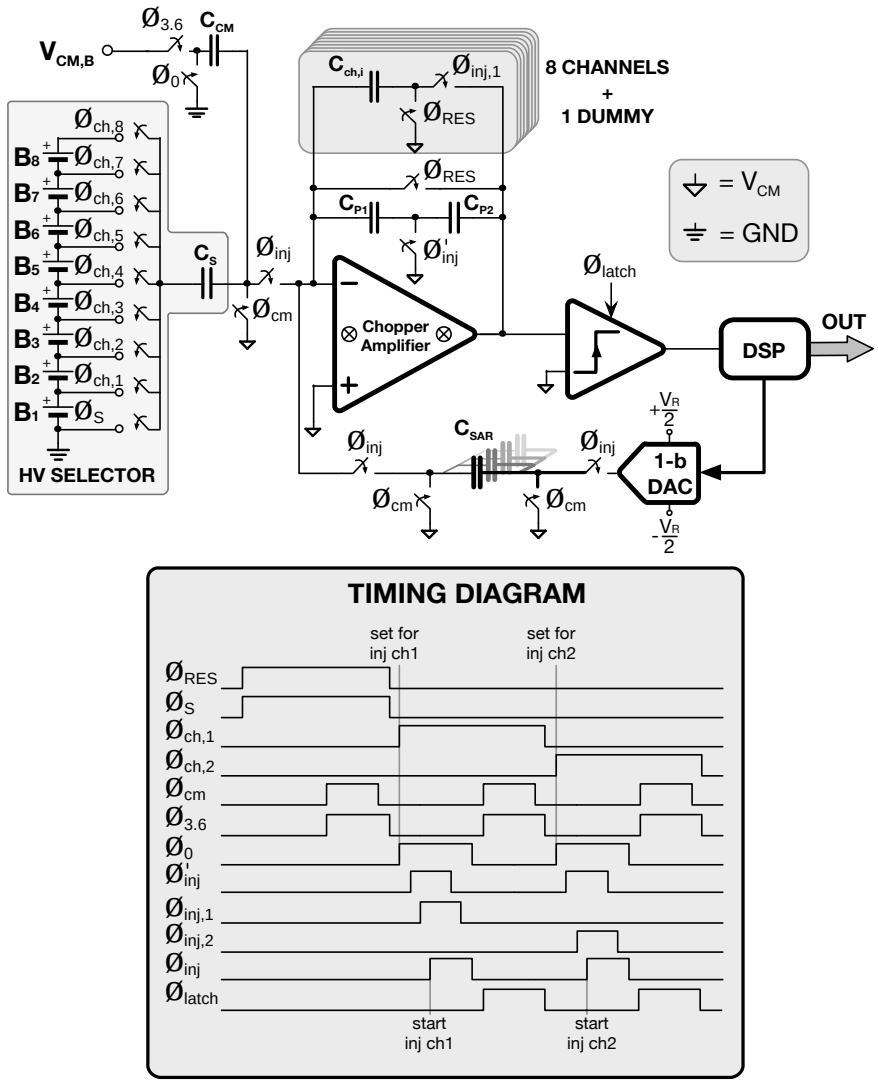

Fig. 3.3 Battery monitor during incremental conversion with timing diagram of the phases.

where D_i is the output of the comparator at each cycle, V_R = 1.2 V the reference voltage, and $V_{B,i}$ the battery cell voltage. C_{CM} is implemented as a high-voltage capacitor in order to be nominally equal to C_S, and C_{SAR} is designed to achieve a gain of the incremental stage equal to 1. A possible gain error is compensated for by trimming the value of V_R.

TI architectures that share the op-amp can suffer from crosstalk between the multiplexed channel. Therefore, it is required to maintain the charge fidelity at the summing node, which is the input node of the op-amp. A crosstalk problem would rise if an off-channel injects some charge during the active phase of another channel, typically due to charge injection of the sampling switch that opens. This architecture does not suffer from crosstalk because there is only one single injecting element, named C_S, and an approach "set and then inject" is used. Basically, the left plate of the injecting capacitor is always connected to a fixed voltage, and whenever there is a switching activity on this side, the injecting switch on the right side is kept open. This is simply done by adjusting the clock phases in the logic. This means that in Fig. 3.3, whenever the track&hold phases $\phi_{ch,i}$ are changing, ϕ_{inj} is low and ϕ_{cm} ties the summing node to the common-mode voltage, avoiding any possible crosstalk.

Before each conversion, all the feedback capacitances are discharged. A dummy channel captures the charge injected by the feedback reset switch opening. This avoids a clock feedthrough mismatch on the first battery voltage measurement, V_{B1}.

C_{P1} and C_{P2} avoid the open loop connection by providing a feedback path to the operational amplifier when no channel capacitor is connected.

Standard solutions call for a low-pass filter in front of the ADC, [1–3]. This is usually implemented with external components and results into a filter pole in the range of [0.1 - 10] kHz. In this design, the 64 times sampling of the battery voltage introduces a low-pass FIR filter with 64 taps. This relaxes the need of using external components and reduces the cost.

After 64 full cycles, the residual charge stored into each feedback capacitor is

$$Q_{RES,i} = \sum_{i=1}^{N_{inc}} C_{SAR} \frac{V_R}{2}(2D_i - 1) - N_{inc}(C_S V_{B,i} - C_{CM} V_{CM,B}) \tag{3.2}$$

where $N_{inc} = 64$ is the number of incremental cycles.

Since the signal is accumulated 64 times and the noise is quadratically superposed 64 times, the incremental phase attenuates the kT/C noise request by $\sqrt{64} = 8$.

The use of a chopper-stabilised op-amp, [7–10], significantly reduces the input referred offset. The residual offset is mainly due to the charge injection mismatch caused by the opening of the switches connected to the virtual ground. A careful design and layout of the op-amp keeps the error below 0.5 LSB and no calibration is required.

3.2.2 Fine step: SAR ADC

The 64 x 8 incremental cycles obtain a 6-bit resolution for each channel. The $C_{ch,i}$ capacitors store the residual charges. For extending the range, the architecture is re-arranged as in Fig. 3.4 to form a SAR ADC. Fig. 3.5 shows the transfer of the residual voltage from the $C_{ch,i}$ capacitors to C_{SAR}. The chopper operation is disabled and the C_{SAR} array is pre-charged to the offset of the op-amp in an auto-zero fashion

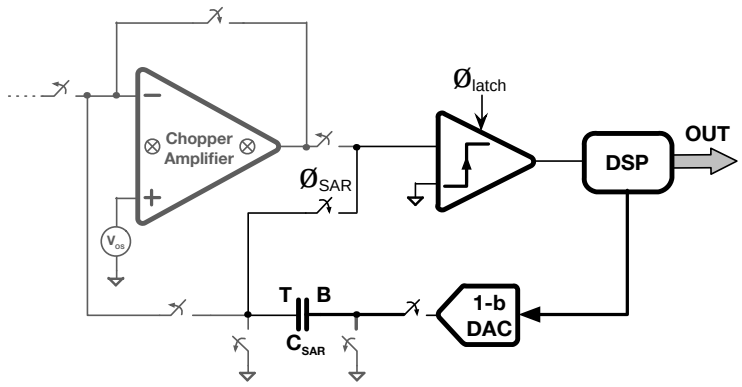

Fig. 3.4 Battery monitor during SAR phase.

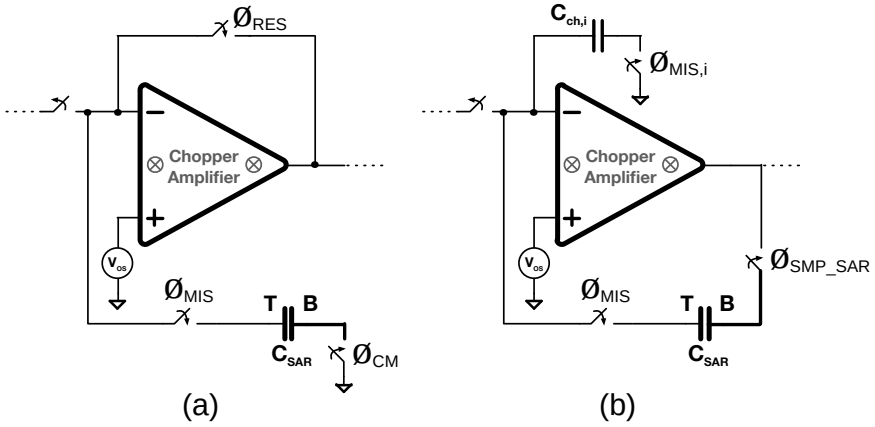

Fig. 3.5 Mismatch cancellation technique during charge transfer to C_{SAR}. (a) Auto-zero phase. (b) Charge transfer from incremental channel to SAR array.

(Fig. 3.5(a)), [11]. Then, the residual charges are sequentially transferred to C_{SAR} in order to perform the SAR conversion cycles (Fig. 3.5(b)).

The relaxed accuracy constraints of the second conversion stage allow using a DAC array, C_{SAR}, made by a combined binary and C-2C structure (Fig. 3.6). The array is composed by 41 poly capacitors C_U of 40 fF. The total capacitance results in C_{TOT} = 1.64 pF. The SAR uses the same comparator of the incremental converter and recycles the 1-b DAC to control the bottom plates of the capacitances.

Since both incremental and SAR steps use C_{SAR} for balancing the input, there is no mismatch between the two phases. Moreover, input sampling and voltage shift use the same type of high-voltage capacitors. A minor limit can come from the

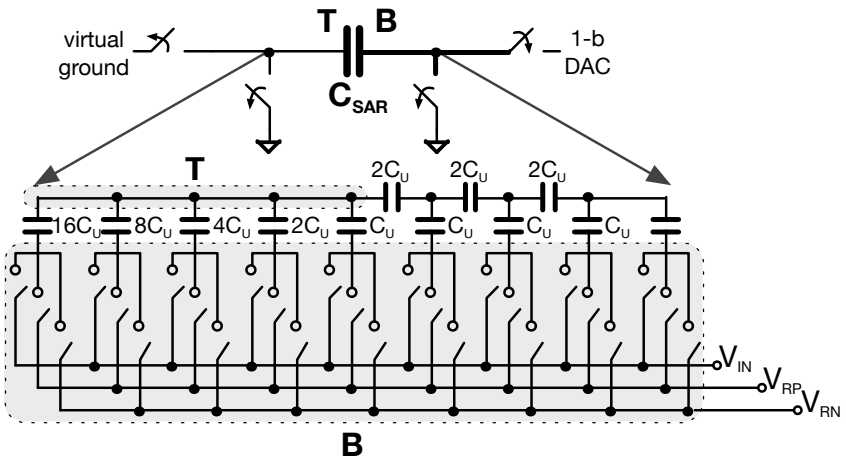

Fig. 3.6 C_{SAR} array architecture. 5 bits are implemented in a binary fashion, and 3 bits use a C-2C structure.

mismatch between feedback channel capacitors, $C_{ch,i}$. Their role is to generate the voltage driving the comparator during the incremental phase. Since the mismatch changes the amplitude but not the sign, the possible error is in the dynamic output of the op-amp. It is just necessary to keep the operation in the linear region for avoiding harmonic distortion.

3.3 Circuit Blocks Design

Apart from the logic generating the control signals for the ADC, the architecture requires only a track & hold, an operational amplifier and a comparator for monitoring the battery stacks.

3.3.1 High Voltage Track & Hold

Fig. 3.7(a) shows the scheme commonly used for a bi-directional high-voltage switch driven by a low-voltage logic control. A back-to-back pMOS configuration with extended drain avoids diode forward biasing when the biasing of the switch reverses. In order to turn on the transistors, a low-voltage clock signal, CLK, is used. When the clock signal is high, the current I_{SW} through the resistor R_{SW} generates the proper V_{sg}. A high-voltage nMOS transistor, tied to $V_{DD,LV}$ = 5 V, ensures that

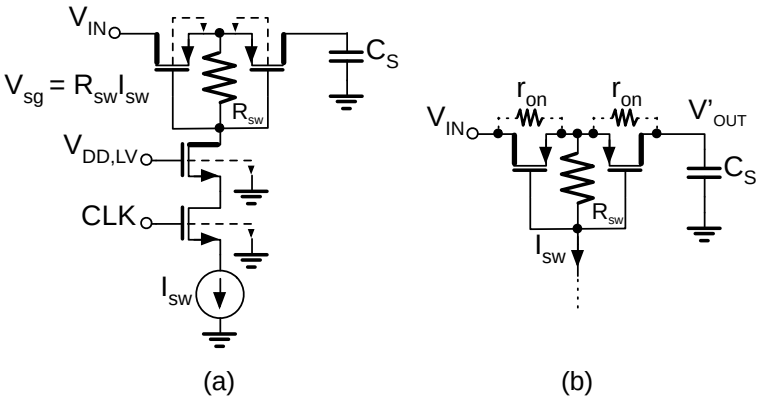

Fig. 3.7 High-voltage track & hold. (a) Schematic. (b) Offset due to r_{on}.

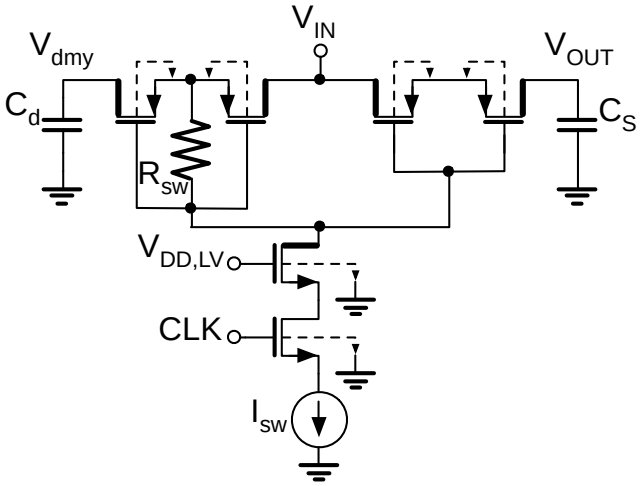

Fig. 3.8 Proposed high-voltage track & hold with dummy structure.

the drain node of the low-voltage transistor does not exceed ($V_{DD,LV}$ - V_{th}). This solution is suitable for low accuracy or logic signals. For precise applications, the current I_{SW} flowing in R_{SW}, used to turn on the transistors, also flows through one of the two back-to-back p-channel elements and this causes a non-linear drop ΔV that generates an offset affecting the sampled voltage, Fig. 3.7(b).

The value of V_{sg} chosen to give rise to the on-condition is the R_{SW} I_{SW} product. The choice of the V_{sg}, the R_{SW} value and the required speed of operation determine the minimum (non-linear) r_{on}. Indeed, there is a maximum size for the transistors, since their gate capacitance and the value of R_{SW} give rise to a time constant that

might limit the speed of the switch. It is possible to reduce the time constant with lower values of R_{SW} but I_{SW} increases and augments the generated offset. The result is that the speed of operation critically affects the on-resistance of the switch. Extensive simulations at the transistor level show that the offset (the product of I_{SW} and the on-resistance) is, for a sampling frequency of 1 MS/s, much larger than the expected LSB. This circuit solves the problem by using a matched dummy structure that generates the proper V_{sg}. The control voltage is then used to drive the actual switch, as shown in Fig. 3.8. In this way, no static current flows through the sampling switch and the required accuracy is achieved. The non-linearity of the on-resistance is ineffective if the sampling period is a suitable number of time constants $r_{on}C_S$.

This design uses an optimal power, speed and silicon area trade-off that leads to I_{SW} = 80 µA, R_{SW} = 50 kΩ and W/L = 10/1 µm/µm. The HV sampling capacitance is 1.6 pF, the obtained r_{on} is about 5 kΩ leading to a time constant as small as 8 ns.

Fig. 3.9 shows the sampling error as a function of the input voltage for the standard solution and the actual switch. The error for the circuit in Fig. 3.7 is non linear and can be as large as 320 mV. In particular, for input voltages lower than 5 V, the drop across the switch is lower since the low input voltage is pushing the current mirror implementing the current generator I_{SW} in the triode region, thus decreasing the I_{SW} value. By contrast, the actual switch works very well. It shows an error that is a linear function of the input voltage and is just 1.5 µV at the nominal full scale voltage V_{IN} = 33.6 V.

The simple structure of the switch results in an area-per-switch of 0.006 mm^2, significantly smaller than the solutions in [12, 13]. Moreover, the circuit implementation does not require high-voltage capacitors to operate.

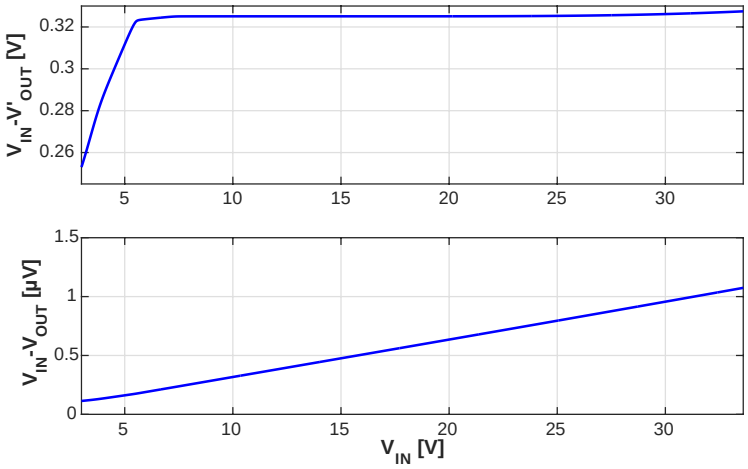

Fig. 3.9 Sampling error as a function of the input voltage. (a) Standard approach. (b) Proposed solution.

3.3.2 Operational amplifier with chopping technique

Fig. 3.10 shows the schematic of the used operational amplifier. It is a two stage amplifier with a telescopic cascode as the first stage and an inverter with active load as second stage. The first stage uses a high-compliance current mirror for increasing the voltage room for the input pair and the current generator. The op-amp is designed to drive a capacitive load as large as 2 pF.

The amplifier is Miller compensated. A *zero-nulling* resistance, R_0, further increases the phase margin. C_M = 4 pF and R_0 = 550 Ω, allow achieving a phase margin of 65°. A biasing current of 100 μA is used and a DC gain of 120 dB and a bandwidth equal to 20 MHz are obtained.

Equation (3.1) does not account for the offset of the op-amp. When considering it, (3.1) becomes

$$Q_{inj,in} = C_S(V_{B,i} - V_{os}) + C_{CM}(-V_{CM,B} - V_{os}) + C_{SAR}\left(\frac{V_R}{2}(2D_i - 1) - V_{os}\right) \quad (3.3)$$

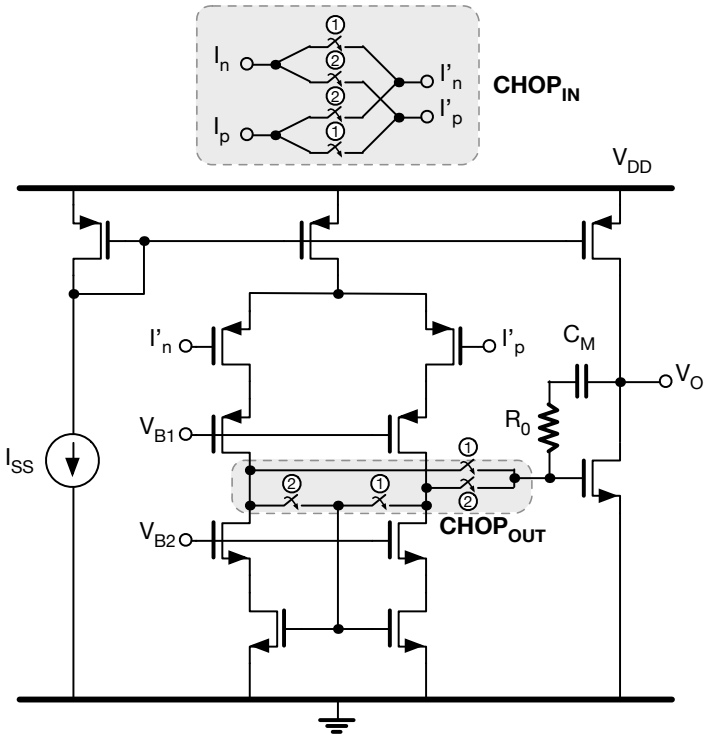

Fig. 3.10 Schematic view of the operational amplifier with chopping technique.

where V_{os} is the offset of the op-amp. Assuming, for simplicity, that all the injecting capacitors C_S, C_{CM} and C_{SAR} are equal and called C_{inj}, then (3.3) becomes

$$Q_{inj,in} = C_{inj}\left(V_{B,i} - V_{CM,B} + \frac{V_R}{2}(2D_i - 1) - 3V_{os}\right) \tag{3.4}$$

and the residual charge would present an error due to the offset injection at each clock cycle, resulting in

$$Q_{RES,i} = C_{inj}\left(\sum_{i=1}^{N_{inc}} \frac{V_R}{2}(2D_i - 1) - N_{inc}\,(V_{B,i} - V_{CM,B}) - 3N_{inc}V_{os}\right) \tag{3.5}$$

The residual voltage is derived from the residual charge, by simply dividing it by the integrator capacitor, $C_{ch,i}$. Again for simplicity, this is considered equal to C_{inj}, resulting in a residual voltage equal to

$$V_{RES,i} = \sum_{i=1}^{N_{inc}} \frac{V_R}{2}(2D_i - 1) - N_{inc}\,(V_{B,i} - V_{CM,B}) - 3N_{inc}V_{os} \tag{3.6}$$

This would lead to an error due to the offset that is larger than the LSB. The cancellation of offset and low-frequency noise is conventionally obtained with auto-zero, [11], or chopper methods, [7–10]. The proposed solution uses a chopped amplifier to deal with this problem.

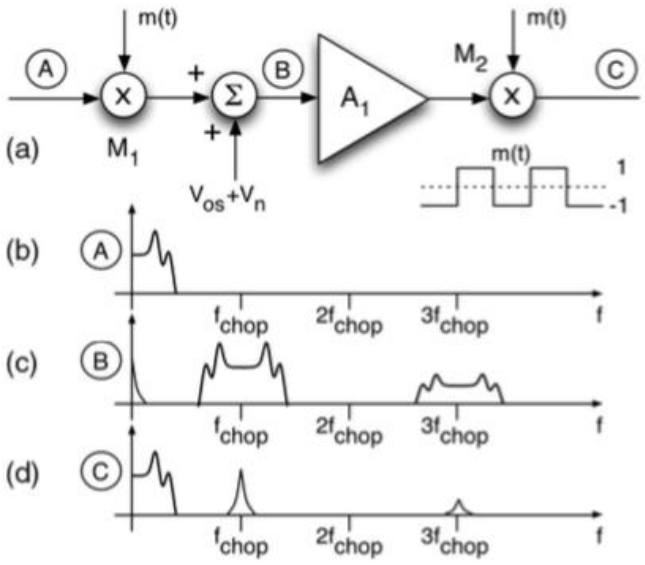

Fig. 3.11 Chopper technique basic scheme.

The chopper technique transposes the input signal to high frequency by modulation, as done by the multiplier M_1 of Fig. 3.11(a), and then demodulates it back to the baseband with the multiplier M_2 after amplification. The modulating signal is a square-wave signal, $m(t)$, with period $T = \frac{1}{f_{chop}}$. After the first modulation, offset and $1/f$ noise (V_{os} and V_n, respectively) corrupt the signal, but they are transposed to high frequency by the action of M_2. Fig. 3.11(b)-(d) depicts the spectra of the signal involved in the relevant points of the processing chain. The frequency noise added to input of A_1, modulated by M_2 and replicated at multiple of f_{chop}, is lowpass filtered by the finite bandwidth of A_1. M_1 and M_2 are implemented in the op-amp architecture by the $CHOP_{IN}$ and $CHOP_{OUT}$ networks shown in Fig. 3.10.

Due to mismatch in the circuit, there is a residual offset at the end of the conversion, $V_{os,res}$, that affects (3.7) in the same way as the original offset

$$V_{RES,i} = \sum_{i=1}^{N_{inc}} \frac{V_R}{2}(2D_i - 1) - N_{inc}\left(V_{B,i} - V_{CM,B}\right) - 3N_{inc}V_{os,res} \tag{3.7}$$

The input voltage can be derived from 3.7 as

$$\left(V_{B,i} - V_{CM,B}\right) = \left(\frac{\sum_{i=1}^{N_{inc}}(2D_i - 1)}{2N_{inc}}\right)V_R - \frac{V_{RES,i}}{N_{inc}} - 3V_{os,res} \tag{3.8}$$

where the first term is the digital representation of the input signal, the second one the quantisation error, and the final one the offset error. Therefore, the residual offset has to introduce an error that is negligible if compared to the LSB of the SAR stage. Thus, the residual offset needs to be smaller than

$$V_{os,res} < \frac{V_R}{3 \cdot 2^{N_{SAR}}} \tag{3.9}$$

With V_R = 1.2 V and N_{SAR} = 8 bits, the residual offset cannot exceed 1.5 mV. This is easily achievable with the used chopping technique.

At the end of the incremental phase, the charge stored in the feedback capacitors is transferred to the DAC array, C_{SAR}. In this case, since the operation is single, the chopping technique is not effective. Instead, an auto-zero technique is used. In phase one, Fig. 3.5(a), C_{SAR} is reset to the offset of the op-amp, leading to

$$Q_{C_{SAR}} = V_{os}C_{SAR} \tag{3.10}$$

$$Q_{C_{ch,i}} = Q_{RES,i} \tag{3.11}$$

C_{SAR} is then connected in feedback and the charge in $C_{ch,i}$ is injected into it, as shown in Fig. 3.5(b). The final charge in C_{SAR} becomes

$$Q_{C_{SAR}} = Q_{RES} + V_{os}C_{SAR} - V_{os}C_{ch,i} \tag{3.12}$$

The error due to the offset, in this phase, is only caused by the mismatch in the capacitors C_{SAR} and $C_{ch,i}$, and it can be expressed as

$$V_{err} = V_{os}\frac{(C_{SAR} - C_{ch,i})}{C_{SAR}} \tag{3.13}$$

Choosing a large enough C_{SAR} ensures this error to be negligible.

3.3.3 Voltage Comparator

Fig. 3.12 shows the schematic diagram of the voltage comparator used in this design. The structure uses a single stage preamplifier for improving the noise performances. This is a single-ended stage with active load. The latch is a standard sense-amplifier based latch [14]. A biasing current equal to 25 μA ensures a bandwidth large enough to accommodate the 1 MHz clock operations.

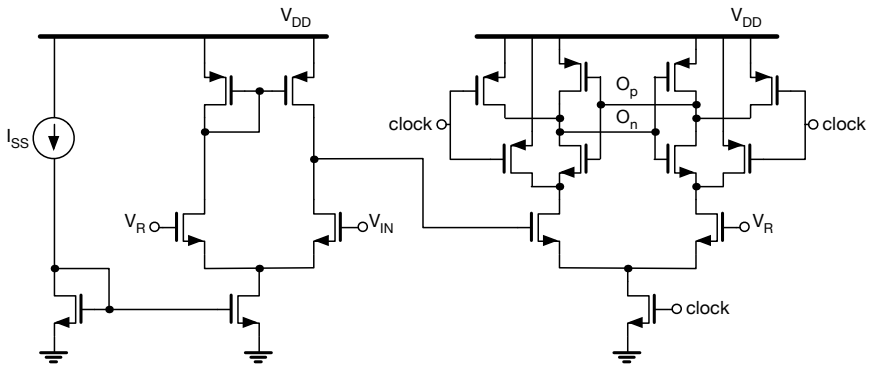

Fig. 3.12 Comparator schematic view of the comparator with preamplifier.

3.4 Measurement Results

This ADC has been fabricated in a 0.35-μm triple-well 5V HV CMOS process with drain extended MOS high-voltage devices. The prototype has been measured with the nominal supply voltage of 5 V and its active area is 1300 x 650 μm^2. Fig. 3.13 depicts the whole chip microphotograph and a magnified view of the active area, where the main circuit blocks have been highlighted. The large area occupied by the high-voltage front-end is due to comply with the minimum ESD distance rules of the used technology. The low voltage section is formed by the op-amp, the voltage

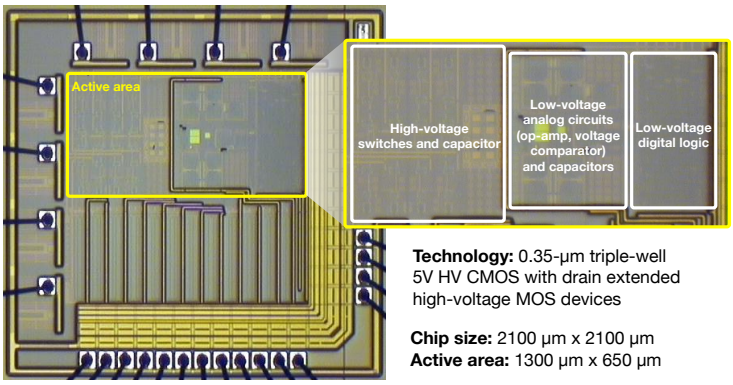

Fig. 3.13 Chip microphotograph.

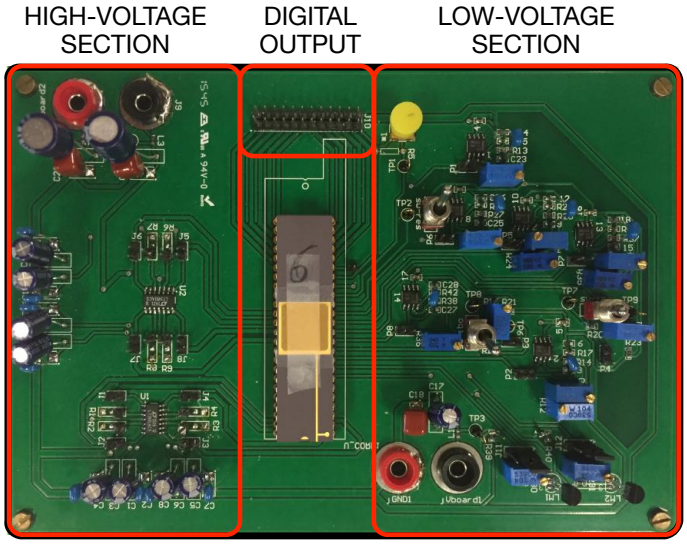

Fig. 3.14 Testing board.

comparator and the capacitors bank (8 channels, 1 dummy channel, 1 SAR/feedback bank). The capacitor injecting the battery common-mode, C_{CM}, and C_S are both high-voltage with a well matched layout in the HV section. Finally, the low-voltage digital logic provides all the control signals to the system.

Fig. 3.14 shows the testing board that was implemented for the measurement setup. The high-voltage section provides the input signals to the battery monitor, while the low-voltage section generates all the reference voltages (V_{RP}, V_{RN}, V_{CM} and $V_{CM,B}$) and the supply voltages (AV_{DD} and DV_{DD}) for the ADC. Finally, the

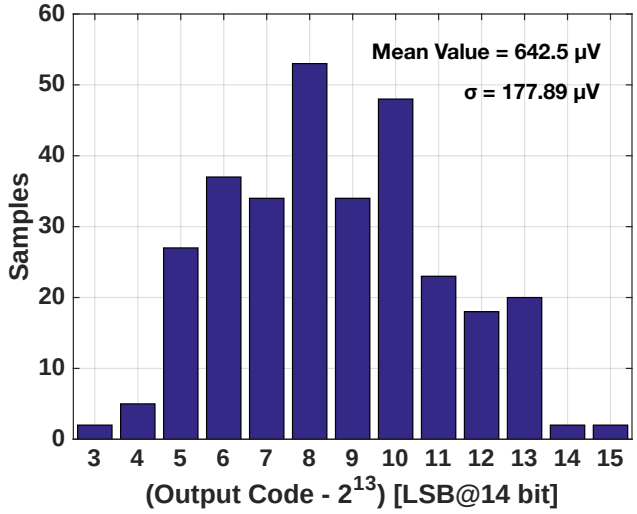

Fig. 3.15 Histogram of 300 repeated measures with $V_{IN} = V_{CM}$.

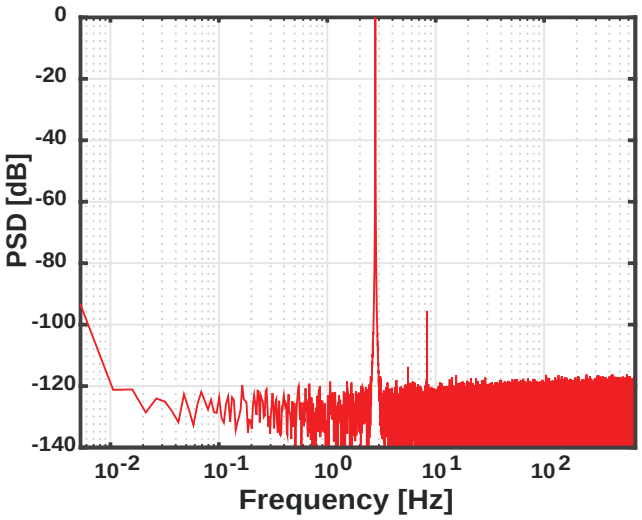

Fig. 3.16 Measured output spectrum (FFT with 2^{18} points).

digital output is collected by means of a logic analyzer and the data is processed in Matlab environment.

Fig. 3.15 shows the histogram of 300 repeated measurements on channel 1, with the input shorted to V_{CM}, which is at half scale of the converter. It measures the

input referred noise, whose variance is 177.9 μV, and the residual offset, equal to 642.5 μV.

Fig. 3.16 gives the measured output spectrum with a full scale sine wave (0.6 V peak value) at 2.78 Hz applied on channel 8. The SNDR is 76.7 dB (12.45 bit). The harmonic tones amplitude is very low and limits the SFDR at -96 dB_{FS}.

Figg. 3.17 and 3.18 show the measured INL and DNL resulting from the histogram of a full scale input sine wave on channel 4. The INL is in the [-2,0.5] LSB range and the DNL is in the [-1,0.8] LSB range. Similar both static and dynamic results have been collected from all the channels. The endpoint fit line INL shows a good linearity of the high-voltage capacitor C_S in the ±0.6-V range. The linearity over the full 33.6-V range depends on the voltage coefficients of the high-voltage capacitor, $C_S(V) = C_S(0)(1+\alpha V)$. Fig. 3.19 shows the nonlinearity error of the mea-

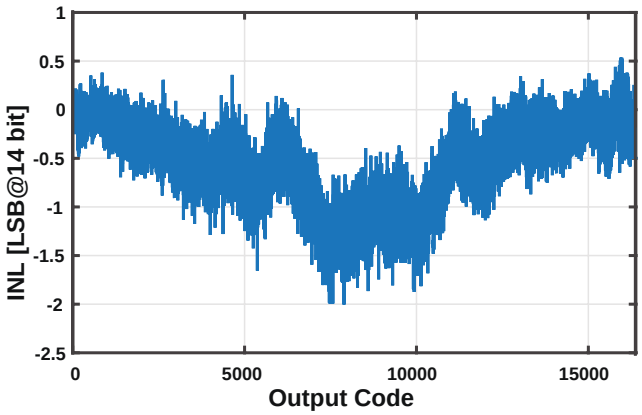

Fig. 3.17 Measured INL.

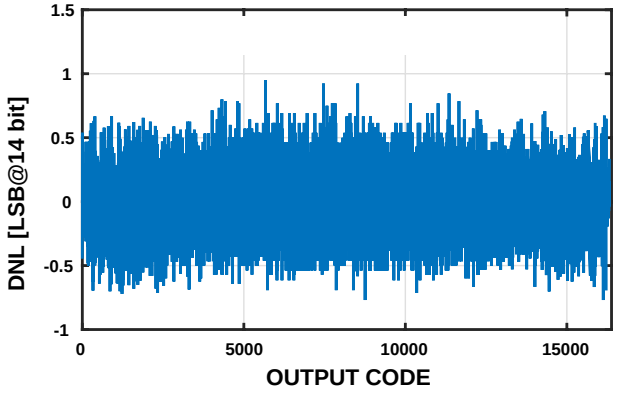

Fig. 3.18 Measured DNL.

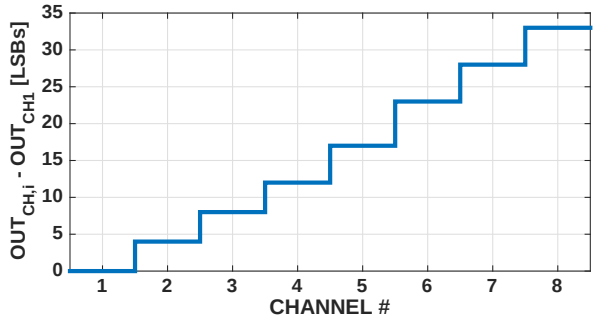

Fig. 3.19 Measured output (average of 100 measurements) of the ADC when the same input is applied to all the channels.

sured outputs (average of 100 measurements) when the same input is applied to all the channels ($V_{B,i}$ = 3.6 V). The result is the difference with respect to the first channel output and is expressed in LSBs (14-bit). The figure shows a voltage coefficient of 96 ppm/V. The error is almost the same for all the available chips and can be corrected in the digital domain.

Fig. 3.20 shows the system power breakdown with 1 MHz of master clock frequency. The total power consumption is dominated by the digital logic and is equal to 3.64 mW.

Table 3.1 summarises the battery monitor performances and provides a comparison with existing solutions. The comparison is performed by using the Schreier figure of merit, FoM_S = SNR + 10 log(BW/P), [15]. In this design the SNR, the bandwidth and the power consumption are 76.7 dB, 700 Hz and 3.64 mW, respectively. The resulting FoM_S is 129.5 dB. The achieved results are competitive, con-

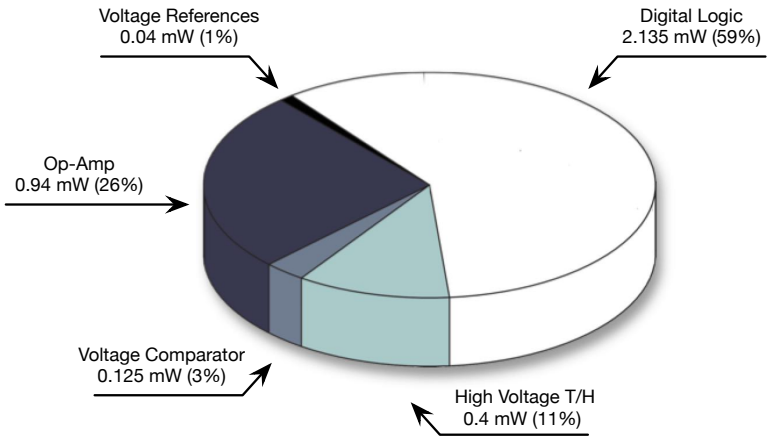

Fig. 3.20 Measured battery monitor power breakdown.

Table 3.1 Performance summary and comparison table.

	This Work	[1]	[2]	[3]	[4]
Supply Voltage	**5 V**	[7.2 - 27] V	[10 - 55] V	[8 - 30] V	[5.2] V
Cell Input DR	**1.2 V**	4.5 V	5 V	4 V	2.5 V
Resolution	**214 μV**	380 μV	1.5 mV	980μV	2.3 mV
ENOB	**12.45 b**	13.5 b	11.7 b	12 b	10.1 b
SNR	**76.7 dB**	83 dB	72.2 dB	74 dB	62.5 dB
Offset	**642.5 μV**	calibrated	500 μV	610 μV	-
Measured Cells	**8**	6	8[1]	6	6
Bandwidth	**700 Hz**	11.9 kHz	55.5 Hz	83.3 kHz	200 kHz
Total Power Consumption	**3.64 mW**	13.1 mW[1]	10.7 mW[2]	42.5 mW[1]	-
FoM_S	**129.5 dB**	142.6 dB	109.4 dB	136.9 dB	-

[1]Reduced to 8 for this comparison. [2] can measure up to 12 cells.
[2]Estimated power consumption - 25% of total power consumption

sidering that the works reported in [1] and [3] can measure only up to 6 cells. The system in [4] implements a parallel solution that uses 6 transimpedance amplifiers (TA) as level shifters, and 6 $\Sigma\Delta$ ADCs. This overhead in complexity is likely paid in larger power consumption and occupied area. Besides, the inter-channel matching becomes a major concern in parallel architectures.

3.5 Conclusions

In this chapter, a battery monitor system was presented. The architecture uses a time-interleaved incremental converter for coarse conversion and a single SAR ADC for fine conversion. The use of the same ADC for all the channels in the fine step relaxes the matching requirements in the time-interleaved structure. A HV track & hold with low-voltage logic control interfaces the A/D with the battery stack. This solution achieves high linearity and low cost.

The battery monitor has a resolution of about 0.2 mV, consuming 3.64 mW with an area of 1300 x 650 μm^2. All channels are measured in 720 μs. The measured residual offset is 642.5 μV. The dynamic input range of the system can be as large as 33.6 V, and the achieved figure of merit is 141.9 dB.

The description of this ADC and the measurement results were presented in a paper published in the *IEEE Transactions on Circuits and Systems - II: Express Briefs* titled “High-Resolution Time-Interleaved 8-Channel ADC for Li-Ion Battery Stack”, [16].

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Chapter 4
A 200 μW 12-b 8 MS/s SAR ADC for Ultrasound Systems

Abstract During the period spent in the Microsystems Technology Laboratories at the Massachusetts Institute of Technology, a 12-bit 8-MS/s SAR ADC was designed for a wearable transcranial doppler ultrasound system. This was done in collaboration with the principal investigator of the project, Sabino Joseph Pietrangelo. A hybrid capacitive and resistive DAC was implemented in order to match the area constraint for the 64 channels system. Post-layout *noise-transient* simulation results show an ENOB equal to 11.3 bits in the band of interest, [1.8 - 2.2] MHz. The ADC was designed in 65nm LP CMOS Technology, occupies 0.04 μm2 and consumes 200 μW with a nominal supply voltage of 1.2V. The resulted figure of merit is 9.9 fJ/conversion-step

4.1 Introduction

The project carried out in the Microsystems Technology Laboratories at the Massachusetts Institute of Technology details *the design of a transcranial Doppler (TCD) ultrasound system to measure cerebral blood flow velocity (CBFV) at the middle cerebral artery (MCA). TCD sonography has been clinically indicated in a variety of neurovascular diagnostic applications. Acceptance of conventional TCD methods, however, has been primarily impeded by several constraints, including restrictive system form factors, measurement reliability concerns, and the need for a highly-skilled operator. The goal of this work is to reduce the effects of such limitations through the development of a highly-compact, wearable TCD ultrasound system for autonomous CBFV measurement.* [1]

Fig. 4.1 shows the architecture used for implementing the transcranial Doppler ultrasound system. Pulse excitation waveforms are generated in the processing unit and are relayed to each independent high-voltage (HV) pulser channel. The HV pulsers transform digital excitation waveforms into HV transmit pulses. Within the transducer array, each element is connected to a HV pulser channel. The piezoelectric transducer elements convert the HV transmit pulses into acoustic energy, which

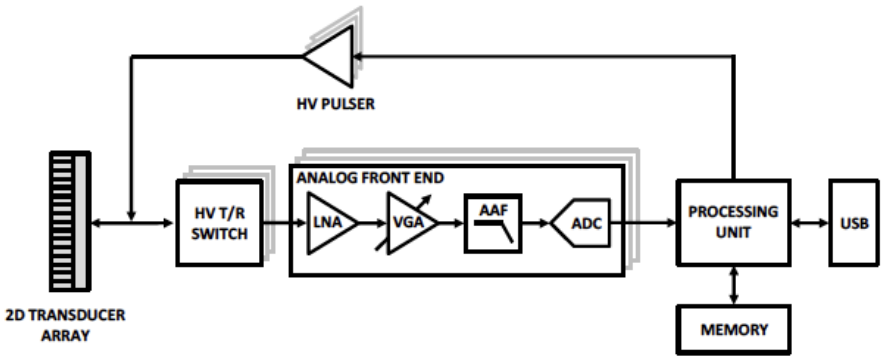

Fig. 4.1 Architecture of the transcranial Doppler ultrasound system. [1]

is radiated into the propagating medium. During transmit, the HV transmit/receive (T/R) switches - one per transducer element - are open to protect sensitive receive electronics from HV signals.

During receive mode, acoustic energy is converted into a low-level electrical signal at each transducer element. The HV T/R switches close, providing a path to the low noise amplifier (LNA) of the analog front end (AFE), with one AFE per transducer element. A variable gain amplifier (VGA) further amplifies the received signals such that signal levels are within the ADC operating range. An anti-aliasing filter (AAF) is used to low-pass filter the signal so that spectral content beyond the Nyquist frequency does not result in aliasing. The analog signals are then digitised and the resulting bitstreams are sent to the processing unit. Receive beamforming is achieved in post-processing through simple delay and sum methods (i.e., time delaying each channel and adding the resulting outputs). Data can be further manipulated within the processing unit to obtain velocity estimation, stored to memory, or transferred to a computer via USB for data collection and further analysis.

The implementation of a discrete prototype of this architecture, done by the main investigator S. J. Pietrangelo, allowed to extract the specifications for the integration of the AFE blocks. The data output by the ADC of each channel is decimated and sum up by the post-processing unit. This allows to relax the requirements on the non-linearities introduced by the ADC. In particular, only non-harmonic tones introduced into the output spectrum are a problem. These tones are mainly generated by coupling of the analog blocks of the converter to the supply voltage noise, and by the noise introduced by the digital clocking. Table 4.1 summarises the specification requirements for the single-channel ADC described in this chapter.

Specification	Value
Resolution	12 bits
Sampling Frequency	8 MS/s
Power Consumption	<250 μW
SNDR	>68 dB
SFDR (non-harmonic)	>75 dB
Area	<0.05 mm^2

Table 4.1 ADC specifications.

4.2 Architecture

Fig. 4.2 shows the architecture of the SAR ADC. A combined resistive and capacitive DAC, [2, 3, 8] reduces the area occupied by the converter. The input is sampled on the bottom plate of the capacitive section of the DAC (C-DAC). The differential structure provides the input to the comparator, which is implemented as a double-tail latch, [9]. The output of the comparator controls the switch driving registers, that controls the bottom plate of the DAC. A decoder for the resistive steps of the converter drives the resistive string that implements the R-DAC. A self timing logic controls the shift register and optimises the phase generation for the converter, implementing an asynchronous ADC, [10]. In order to reduce the power consumption, a power switch disconnects the string during the first 7 cycles, when the C-DAC is operating, so that no static current flows through it. The last resistor in the string is intentionally made smaller , in order to compensate for the *on* resistance of the power switch.

4.2.1 R-C DAC tradeoff

The design choices of the C-DAC structure in conventional SAR ADCs depend on two factors: the $\frac{kT}{C}$ noise requirements, and the mismatch accuracy. These constraints limit the minimum unit capacitance used in the converter, and the total array area. While the first factor is an absolute limit on the value of the sampling capacitance, the second factor is technology related and depends mainly on the area occupied by the array. In this particular application, the harmonic distortion generated by the capacitor mismatches is not a major concern. Hence, the only limit in the choice of the C-DAC array is on the $\frac{kT}{C}$ noise.

The LSB value in this ADC is equal to $V_{LSB} = \frac{V_R}{2^{N_{bit}}} = 293$ μV, where the reference voltage V_R is 1.2 V and $N_{bit} = 12$ bits. A 7-bits binary capacitive array consists of 128 unit capacitances. Metal-Insulator-Metal capacitors (MIM) are chosen because of their reduced parasitics and better mismatch characteristics respect to other

capacitors available in the technology used. The minimum MIM capacitor in this process is 9.5 fF, which leads to a total sampling capacitance of 1.2 pF. This results into a $\frac{kT}{C}$ noise contribution equal to 58.8 μV, which is safely below the LSB value.

This choice is compliant with the noise requirements of the system and it is an optimum trade-off between the area occupied by the C-DAC and the complexity of the R-DAC decoder. In fact, every extra bit implemented in the R-DAC doubles the complexity and the area occupied by the decoder of the resistive string, as well as the area of the resistive string itself. This is true, because the resistive string is implemented in a thermometric fashion in order to ensure the monotonicity of the converter.

4.2.2 ADC timing and searching algorithm

This converter uses a standard binary searching algorithm. A self-time logic clocks the ADC and provides the control signals to the shift register and the comparator. A delay block allocates a fixed time-slot for the DAC settling. Different sizing for the switches driving the bottom plates of the C-DAC ensures a similar RC constant time for each step, thus optimising the time-distribution for this action. After the DAC settles, the comparator is latched. A digital block senses the output of the comparator and provides a feedback signal, *done*, to the self-timing logic that moves on to the next step of the shift registers. Consequently, the switch driving registers changes the code of the DAC and the searching algorithm proceeds. The resulting timing diagram is the one in Fig. 4.3. As explained above, the DAC_i slots are decided by a

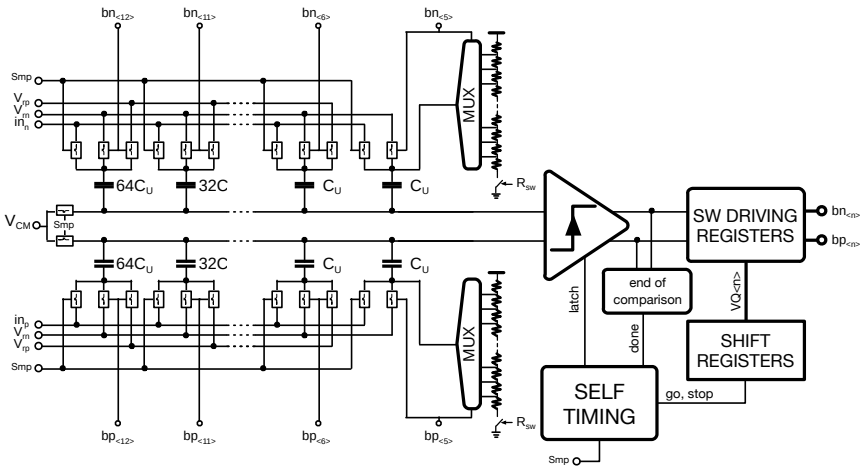

Fig. 4.2 Architecture of the SAR ADC.

delay block inside the self-timing that is controlled by the system, while the CMP_i slots are variable and depend on the decision time of the comparator at each cycle.

Fig. 4.3 Timing diagram of the SAR ADC.

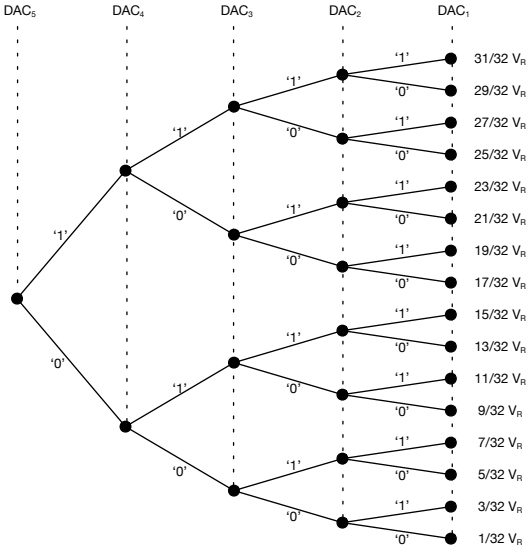

Fig. 4.4 R-DAC steps for the last 5 LSBs conversion.

The first 7 MSBs of the DAC code, $b_{<12:6>}$, control the bottom plates of the capacitive array during the capacitive searching steps. The last 5 LSBs are explored by the resistive string connected at the bottom of the last unit capacitor of the capacitive array and follow a binary search like in Fig. 4.4. The reference voltages of the resistive string are multiplexed by the control signal $b_{<5>}$. The output of the multiplexer is then divided by the C-DAC passive network providing the required steps at the input of the comparator. In particular,

$$V_{in,cmp} = V_{C-DAC} + \frac{V_{R-DAC}}{2^7}$$

the voltage on the top plates of the array is equal to the voltage provided by the C-DAC code plus the voltage provided by the R-DAC attenuated by 2^7.

4.3 Circuit Blocks Design

In this section, the circuital design of the main blocks of the converter are described. They are the digital logic, the DAC and the comparator.

4.3.1 Digital Logic

Fig. 4.5(a) describes the logic circuit that implements the self-timed phase generation used for this ADC. This block generates the clock of the comparator, *latch*, and sets the timing of the converter operation. It also provides two signals, *go* and *stop*, that are needed for starting and stoping the shift register used in the SAR algorithm.

The logic is based on a set/reset latch (SR latch), that is triggered by the signal *done* and its delayed version. Basically, every time the latch comparison is finished, the signal *done* goes high, and *latch* is reset. After a controlled delay, the SR latch is set and a new comparison is done. At the beginning of the conversion cycle, the *latch* signal is set by a *start* strobe generated from the falling edge of the sampling clock. Either *start* or *done* trigger a D-flipflop with its input tight to '1', the output, delayed by a current limited inverter, sets the SR latch. The controls of the latch are masked by the *go* and *stop* in order to leave the *latch* signal low when the converter is not running. Fig. 4.5(b) describes the timing diagram of the block, while Fig. 4.5(c)

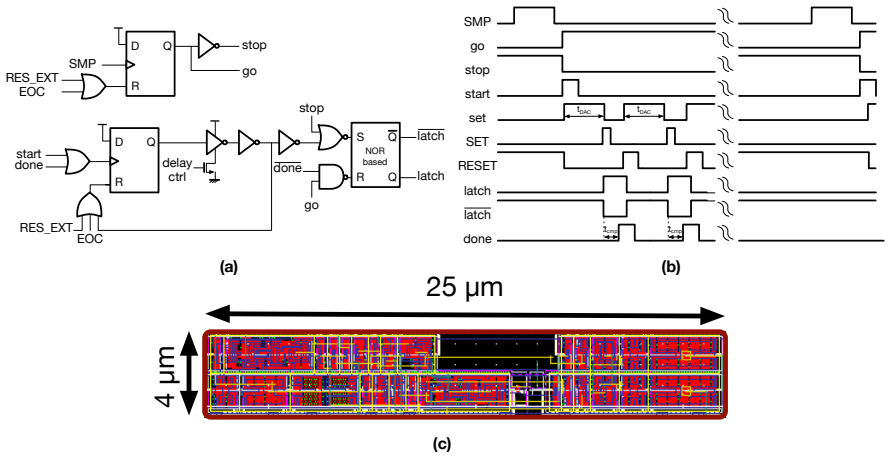

Fig. 4.5 Self-timed phase generator. (a) Schematic view. (b) Timing diagram. (c) Layout view.

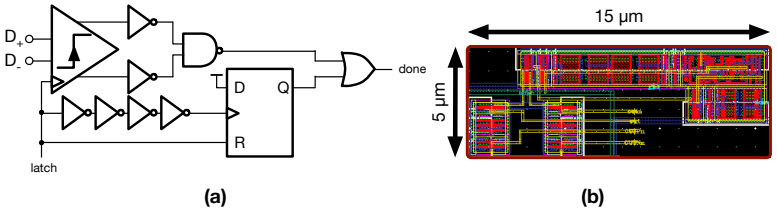

Fig. 4.6 End of comparison logic block. (a) Schematic view. (b) Layout view.

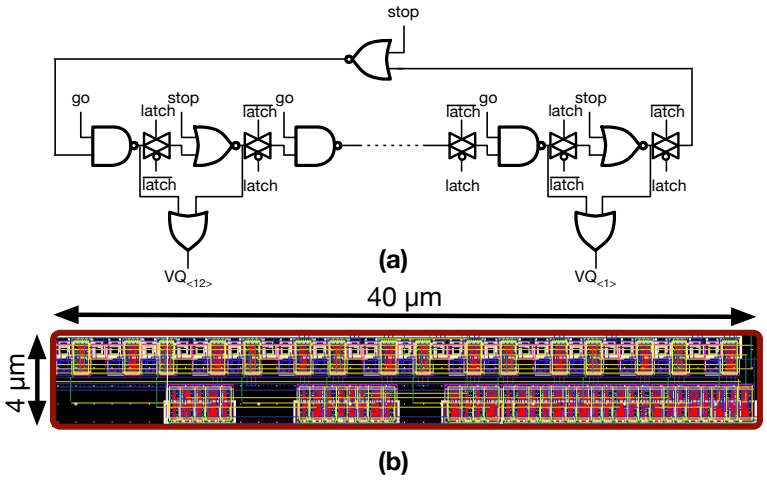

Fig. 4.7 Shift register block. (a) Schematic view. (b) Layout view.

shows the layout view of the self-timed phase generator. The simple structure allows to occupy only an area of 25 x 4 μm^2.

The signal *done* used in the phase generator is provided by an *end of comparison* logic, shown in Fig. 4.6(a). The logic senses when the differential output of the comparator has settled to either '10' or '01'. In case of metastability, a control path triggers the *done* signal and the outcome of the comparator is assumed to be '0'. The logic waits a given time, decided by design, before forcing the end of comparison. The delay is implemented as a chain of inverters, properly sized. The delay and the comparator are designed such that the probability of metastability is very low in case of a differential input larger than half LSB. This ensures that an arbitrary decision on the output of the comparator, in case of metastability, does not introduce an error larger than the quantization one. Fig. 4.6(b) shows the layout view of the logic (the comparator is not included). The area occupied is 15 x 5 μm^2.

Fig. 4.7(a) shows the shift register used for implementing the SAR algorithm. The structure is a delay line clocked by the *latch* signal. At the end of each con-

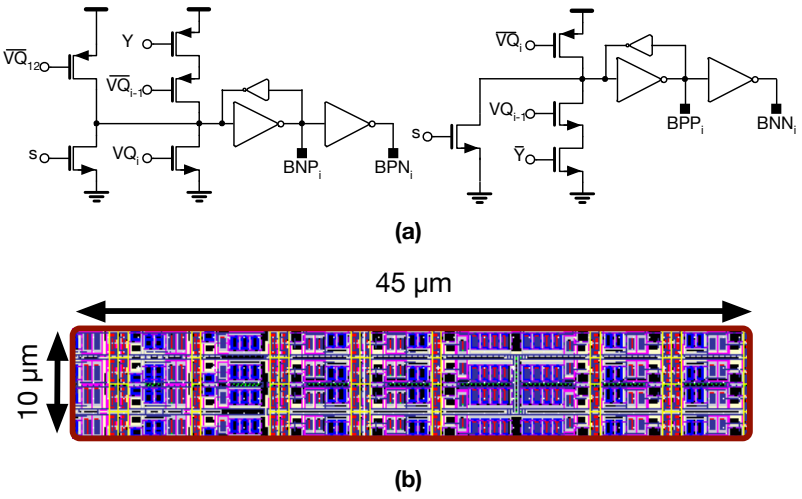

Fig. 4.8 Switch driving registers for the capacitive steps of the DAC. (a) Schematic view. (b) Layout view.

version cycle, *go* and *stop* reset the shift register to a known starting point. Instead, at the beginning, a pulse, generated by the feedback path, propagates through the delay line like in a standard shift register. Extra logic generate the $VQ_{<i>}$ masks that will be used in the switch driving registers. Fig. 4.7(b) shows the layout view of the shift register. The area occupied is 40 x 4 μm^2

The $VQ_{<i>}$ masks are strobes that are used to time the converter steps. They are used in the switch driving registers to control both the bottom plates of the capacitive DAC and the resistive string multiplexer. Fig. 4.8 shows the single cell of the switch driving register used for the capacitive steps of the DAC. The outputs of the cell directly control the switches to V_{RN} and V_{RP} at the bottom plates of the capacitive array. In particular, BPN and BPP control the positive and negative reference switches of the positive section of the differential DAC, while BNP and BNN control those of the negative section.

During the input sampling, the signal s resets the decoder and disables all the reference switches. At the first SAR cycle, the signal $\overline{VQ}_{<12>}$ sets the positive array to V_{RN} and the negative one to V_{RP} according to the SAR searching algorithm. This is not the case for the cell controlling the capacitor defining the most significant bit (MSB), as it has to be set to the opposite values (V_{RP} for the positive array and V_{RN} for the negative one). At the i step, the signals $VQ_{<i>}$ and $\overline{VQ}_{<i>}$ set the i significant bit (iSB) to the test position (V_{RP} for the positive array and V_{RN} for the negative one). One clock cycle later, at the $i-1$ step, the signals $VQ_{<i-1>}$ and $\overline{VQ}_{<i-1>}$ capture the output of the comparator Y and $\overline{Y}$ and store them in the decoder. The memory function is done by placing a minimum size inverter in positive feed-

back between the BNP and BPP nodes and the intermediate node of the decoding cell.

This decoder serves the capacitive DAC and helps to implement the conversion of the 7 MSBs. The remaining 5 least significant bits (LSBs) are explored by the resistive string connected to the last unity capacitor of the array, as in Fig 4.2. During this phase, the power switch connects the resistive string to the supply, so that the reference voltages are available.

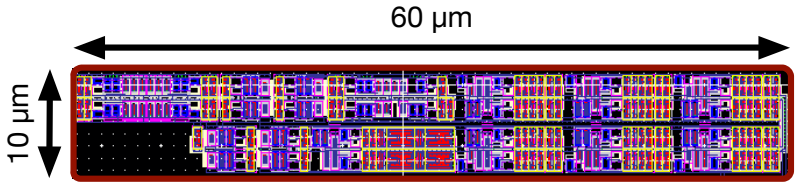

Fig. 4.9 Layout view of the switch driving registers and the decoder for the resistive steps of the DAC

The structure of the switch driving registers for the resistive DAC is similar to the one illustrated for the capacitive DAC. The main difference lies in the way the output of the comparator is masked. If only the signal $VQ_{<i>}$ was necessary before, in this case, an extra mask is required to recognise the path that the conversion algorithm has taken. In particular, at each step the R-DAC would step up or down according to the output of the comparator, following the paths described in Fig. 4.4. For example, for $i = 3$, a positive output of the comparator would move the R-DAC to either 3/8 V_R or 7/8 V_R. In order to provide the correct code to the DAC, it is necessary to know the decision made in the previous step. Doing this, an extra mask is generated for differentiating the two options. The generation of these masks is more complicated as we increase the resolution of the R-DAC. This is the main trade-off in the division between capacitive and resistive DAC for the converter. The proposed solution does not introduce an excessive overhead for the resistive decoder, as Fig. 4.9 shows. In fact, the area is slightly bigger than the one that it would be required for only-capacitive switch driving registers. The total area for both the decoder and the switch driving registers for the resistive steps of the DAC is 60 x 10 μm^2, while the one occupied by the switch driving registers for the capacitive steps is 45 x 10 μm^2.

Implementing 5 bits with a resistive DAC introduces a negligible overhead, if compared to the advantage of having a capacitive array that is 32 times smaller. This solution, if compared to others like split-DAC [4, 5] and C-2C [6, 7], achieves similar benefits in terms of the area occupied with a simpler structure. Besides, non-linearities issues are not a major concern in R-C DACs, while they become the main limiting factor in split-DACs and C-2C DACs.

4.3.2 DAC

The differential C-DAC uses a quasi common-centroid structure that balances as much as possible the boundary conditions and maintains a simple interconnection network. In fact, the systematic non-linearities generated by a capacitive DAC depends mainly on the systematic mismatch between the top-to-bottom parasitic capacitance of each capacitor in the array. The top-to-bottom parasitics come from the coupling between the top plate and the bottom plate of the same capacitor, or the ones of adjacent capacitors. Ideally, if every capacitor presents the same boundary condition, the parasitic capacitance for the array is systematically matched. Yet, the capacitors at the border of the array present a different condition, as one or two sides of the capacitor are adjacent to a dummy structure connected to ground. This translates into a top-to-ground and bottom-to-ground parasitic coupling and introduces a systematic mismatch in the DAC array. The idea, shown in Fig. 4.10, is to balance the number of unit capacitors placed at the border of the array in order to improve the matching. In the proposed solution, the 3-MSB capacitors are matched by ensuring 28 border connections to 2^7C_U, 14 to 2^6C_U and 6 to 2^5C_U. This approach allows to reduce the mismatch error in the C-DAC operation well below the LSB value, and keeps a common-centroid approach for optimum random matching of the array.

Fig. 4.11 shows the layout view of the implemented DAC. The block is composed by the described differential C-DAC, two thermometric R-DAC, the driving switches at the bottom plate of the C-DAC, and the sampling and tracking switches with the bootstrap logic.

The sampling switches connect the top plate of the arrays to the common-mode voltage during the sample phase, while the tracking switches are connected to the bottom plates of the arrays and track the input signals. The bootstrap clock is gen-

Fig. 4.10 Layout placement of the C-DAC for limiting systematic mismatch.

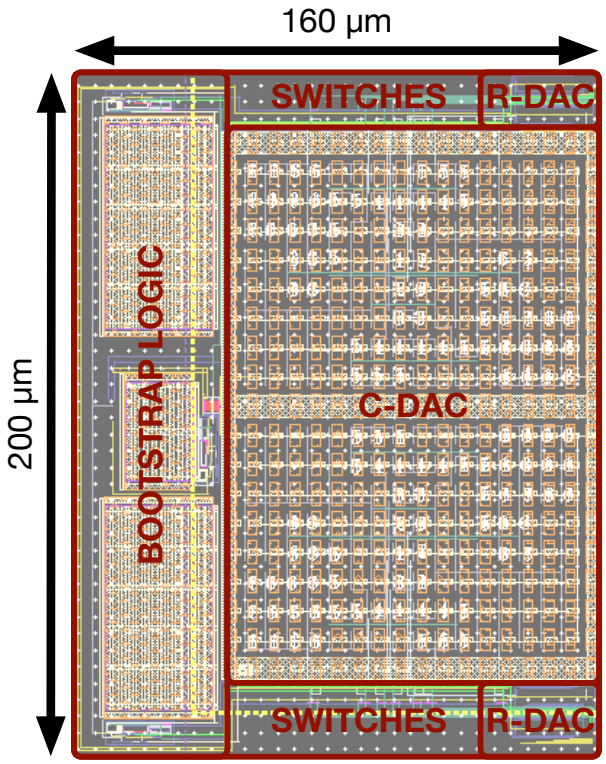

Fig. 4.11 Layout view of the DAC, including the DAC switches and the bootstrap logic.

erated by the circuit in Fig. 4.12, presented in [11]. During $\overline{CLK}$, the capacitor C_B is pre-charged to V_{DD} by M_1 and M_2. M_3 and M_4 tights to ground the output clock CLK_{OUT} and turn off M_8 and M_{10}, while M_5 turns off M_7. When CLK goes high, M_6 turns on M_7 which turns on M_8. M_8, together with M_9, sample V_{IN} at the bottom plate of C_B. This boost the top plate of C_B to $V_{DD} + V_{IN}$. M_7 provides to the output CLK_{OUT} this value attenuated by the parasitic capacitance C_P. The main contribution to this parasitic is the one of the bulk parasitic of M_7. In fact, the maximum voltage experienced by M_7, as well as by M_2, is not V_{DD}, but the top plate of C_B, which can rise up to $2V_{DD}$. For this reason, the bulk of M_7 and M_2 are connected to this node. Therefore, there is a tradeoff between the effectiveness of the bootstrap logic and the maximum sampling speed achievable by the circuit. In this design, a bigger C_B is used for the tracking switch clocks in order to ensure the required linearity in the sampling period. This is not necessary for the sampling switch clock, as the switch is connected to a constant reference voltage. M_4 reduces the V_{DS} and V_{GS} applied to M_3 during the CLK phase, while M_{10} ensures that the V_{SG} of M_7 never exceed V_{DD}.

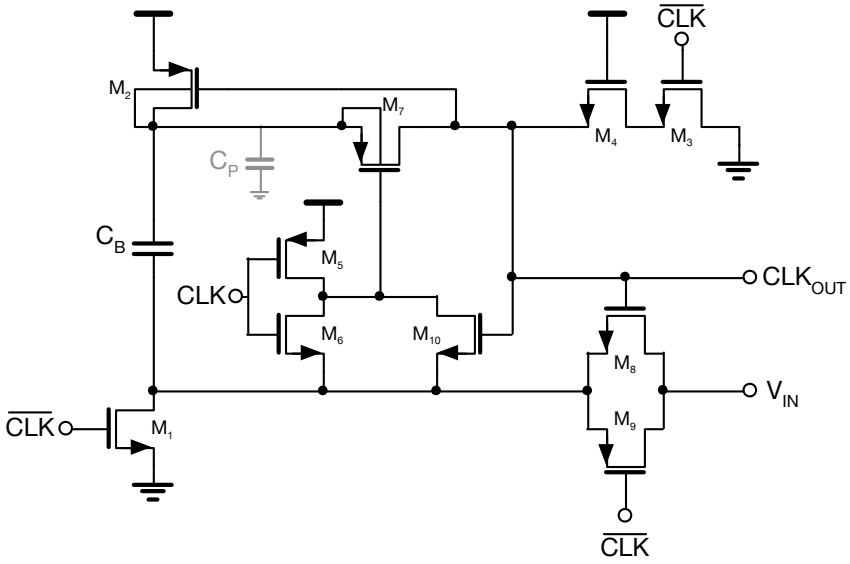

Fig. 4.12 Schematic view of the bootstrap logic.

The area occupied by the C-DAC, the R-DAC, the switches and the bootstrap logic is 220 x 160 μm^2.

4.3.3 Comparator

The comparator used in the converter is the one in Fig. 4.13. When the clock signal is low, the nodes D_+ and D_- are reset to V_{DD} by the couple M_{3a-b}. The two couple M_{7a-b} and M_{8a-b} reset to ground the latch formed by M_{4a-b} and M_{5a-b}, M_{6a-b} are open. When the clock signal goes high, a differential current is generated in the couple M_{2a-b} that discharges the nodes D_+ and D_- at a rate proportional to IN_+ and IN_-. As D_+ and D_- discharge, M_{8a-b} start to provide current to the latch, that sense the difference between IN_+ and IN_- and completes the comparison operation providing the digital output O_+ and O_-.

This solution provides two main benefits. The first one consists in the separation between the input and the output nodes which reduces the kickback noise. The second is the possibility to generate two different tail currents for the input stage and the output stage. This is done by properly sizing M_1 and M_{6a-b}. In this way, it can be optimised both the speed of the regenerative loop and the noise and offset characteristics of the differential input pair. The implemented comparator occupies an area of 15 x 10 μm^2.

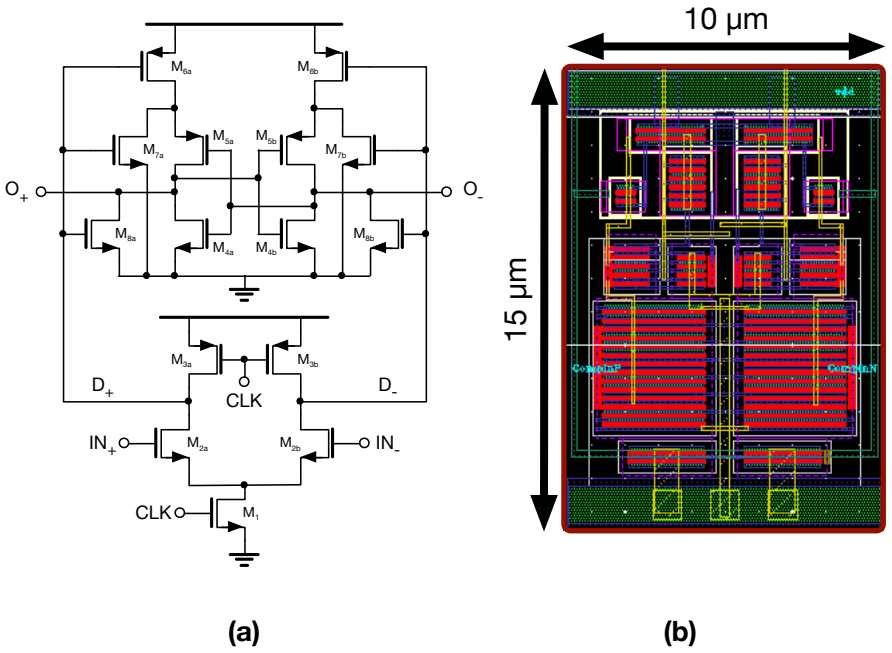

Fig. 4.13 Double-tail latch. (a) Schematic view. (b) Layout view.

4.4 Simulation Results

The ADC has been verified at a simulation transistor level, with a post-layout extracted view, using a 65-nm technology node. Fig. 4.14 shows the post-layout simulated output spectrum (the fft has 1024 points) for an input frequency f_{in} = 2.21 MHz and a sampling frequency f_s = 8 MS/s. The achieved signal-to-noise-and-distortion ratio (SNDR) is 72 dB, that results in an effective number of bits (ENOB) equal to 11.7 bits. The spurious free dynamic range is limited by a tone at 3.06 MHz with amplitude -78 dB. The tone is a non-linear intermodulation between the 5^{th} order input harmonic and the 2^{nd} order sampling harmonic. This distortion derives from the power supply rejection ratio (PSRR) of the comparator. Anyhow, the tone amplitude is 3 dB below the specifications so it does not introduce an issue.

Fig. 4.15 shows the post-layout *noise-tran* simulated output spectrum (the fft has 1024 points) for an input frequency f_{in} = 1.79 MHz and a sampling frequency f_s = 8 MS/s. The SNDR in presence of thermal noise, in a band of 1 GHz, is degraded by less than 3 dB, resulting in an ENOB = 11.3 bits. The SFDR is limited by a tone at 940 KHz with amplitude -78 dB. As expected, the distortion does not change in the presence of thermal noise. SNDR and SFDR specifications are met also in *noise-tran* simulations.

Fig. 4.16 shows the simulated ADC power breakdown. The total power consumption is 200 µW. Main contribution to this are the reference voltages for the

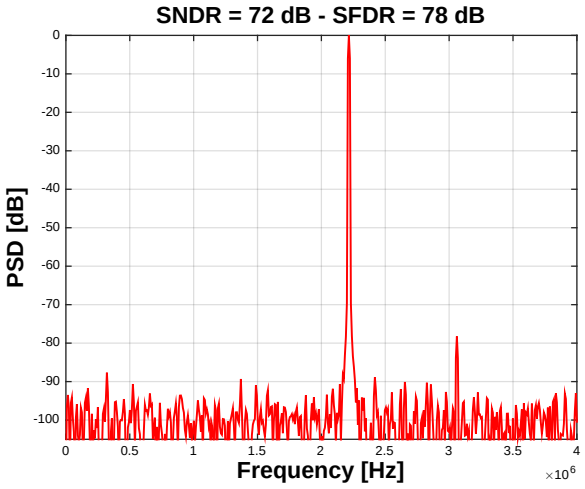

Fig. 4.14 Post-layout simulated output spectrum for f_{in} = 2.21 MHz and f_s = 8 MS/s.

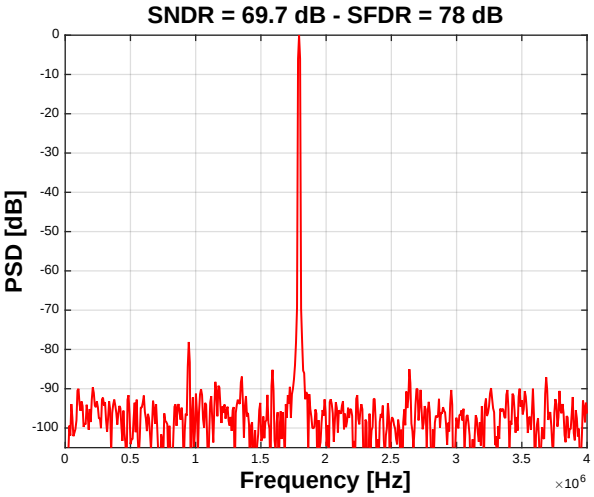

Fig. 4.15 Post-layout *noise-tran* simulated output spectrum for f_{in} = 1.8 MHz and f_s = 8 MS/s.

DAC (41%), and the digital logic (32%). The rest of the power is consumed by the input drivers (18%) and the comparator (9%). The input driver power consumption is estimated, using ideal voltage generators in the simulation setup and considering an efficiency of 75%.

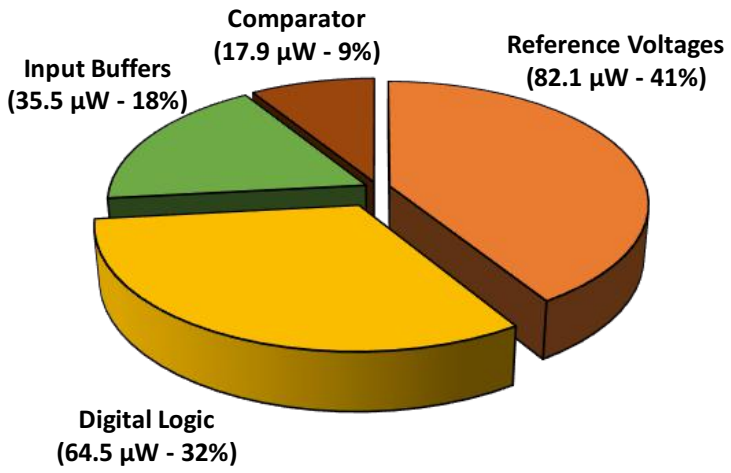

Fig. 4.16 Simulated ADC power breakdown.

4.5 Conclusions

The design of a compact ADC for a transcranial Doppler ultrasound system to measure cerebral blood flow velocity has been demonstrated. The most area-hungry block for a standard SAR ADC is usually the capacitive array implementing the DAC structure. Taking advantage of the post-processing present in the system, the matching requirements for it were significantly reduced. A resistive and capacitive structure was used in order to reduce the area occupied by the DAC. An optimum trade-off between the two sections has been chosen considering the kT/C requirements and the resistive string decoder complexity.

The proposed solution proves the feasibility of using SAR ADCs for analog front-ends in ultrasound system. In fact, a compact and reliable solution can be provided with very little design effort. This particular design achieves an SNDR = 69.7 dB at 8 MS/s, while consuming only 200 µW and it occupies 0.04 mm^2. The resulting figure of merit is 9.9 fJ/conversion-step.

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Chapter 5
Conclusions

Interest in SAR ADCs has increased in recent years, as they stand out as a high-performing solution for multiple applications. Their versatility and scalability perfectly match the new trends in data converter research activities. A look at the state-of-the-art shows how the SAR algorithm is spreading not only as a stand-alone or time-interleaved architecture, but also as a hybrid solution that further pushes away the limits of other types of converters, such as pipeline or oversampled ADCs.

Chapter 1 presented a short overview on the most common ADC architectures and provided an analysis on the evolution of these topologies in the last decades. As a result of this study, the SAR algorithm appeared to be a very flexible approach for applications ranging from ultra low-power to ultra high-speed, always maintaining cutting edge figures of merit. A summary of the state-of-the-art of SAR ADCs proved this to a be a reasonable outcome, showing stunning results from previous designs.

From this assumption, this thesis attempt was to explore the intrinsic potential of the SAR algorithm designing and prototyping three different ADCs, designed for very different applications. In this way, some of the most promising features of the SAR algorithm were studied: the high efficiency for high-speed applications, the possibility to merge easily with other architectures to further improve the performances of the converter, and the simplicity and compactness for ultrasound systems.

In Chapter 2, the prototype of a high-speed single channel Flash-SAR ADC in 65-nm CMOS process was presented and the experimental results were illustrated. The achieved measured figure of merit at Nyquist is 86.7 fJ/conv-step with a sampling rate equal to 700 MS/s and a nominal supply voltage of 1.2 V. The use of a flash approach for the MSBs conversion and a multi-bit per cycle SAR for the LSBs increases the speed of operation maintaining a very competitive efficiency. The thresholds generation in the SAR ADC is done by means of a novel resistive interpolated preamplifier that reduces the power consumption and relaxes the resolution constraints of the comparator. A divider-based phase generator gets rid of the conventional shift register approach in the SAR ADC, and a dynamic logic minimizes the feedback loop delay of the converter.

In Chapter 3, a battery monitor system was presented. The SAR approach was used to extend the dynamic range of a first order time-interleaved incremental ADC. The use of the same ADC for all the channels in the fine step relaxes the matching requirements in the time-interleaved structure, and allows a high-resolution converter with very simple analog blocks. A HV track & hold with low-voltage logic control interfaces the A/D with the battery stack, achieving high linearity and low cost. The battery monitor has a resolution of about 0.2 mV, consuming 3.64 mW with an area of 1300 x 650 μm^2. All channels are measured in 720 μs. The measured residual offset is 642.5 μV. The dynamic input range of the system can be as large as 33.6 V, and the achieved figure of merit is 141.9 dB.

In Chapter 4, the design of a compact ADC for a transcranial Doppler ultrasound system to measure cerebral blood flow velocity has been demonstrated. A very simple approach with a hybrid resistive-capacitive DAC and a self timed logic was used. This case study proved the effectiveness of the SAR algorithm for fast prototyping requirements in modern system-oriented projects. In fact, a compact and reliable solution can be provided with very little design effort using the countless techniques proposed by the research community in this field. This particular design achieves an SNDR = 69.7 dB at 8 MS/s, while consuming only 200 μW and it occupies 0.04 mm^2. The resulting figure of merit is 9.9 fJ/conversion-step.

The work done during the Ph.D. activity, between University of Pavia and the Massachusetts Institute of Technology, focused on interface systems for data acquisition applications, especially on the design of high-performance ADCs. This led to the fabrication and characterisation of two different chips and the design of another ADC, and the publication of six papers in conferences and journals listed below.

1. D.G. Muratore, A. Akdikmen, E. Bonizzoni, F. Maloberti, U-F. Chio, S.-W. Sin, R. P. Martins, **"An 8-bit 0.7-GS/s Single Channel Flash-SAR ADC in 65-nm CMOS Technology"**, *To appear in the Proc. of IEEE European Solid State Circuits Conference (ESSCIRC)*, 2016.

2. D. G. Muratore, E. Bonizzoni, S. Verri, F. Maloberti, **"High-Resolution Time-Interleaved 8-Channel ADC for Li-Ion Battery Stack"**, *IEEE Transactions on Circuits and Systems - II: Express Briefs*, DOI: 10.1109/TCSII.2016.2597358, 2016.

3. D.G. Muratore, E. Bonizzoni, and F. Maloberti, **"A Pipeline ADC for Very High High Conversion Rates"**, *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1446 - 1449, 2016.

4. D.G. Muratore, E. Bonizzoni, F. Maloberti, and Carlo Fiocchi, **"A Capacitive Sensor Interface for High-Resolution Acquisitions in Hostile Environments"**, *Proc. of IEEE Latin American Symposium on Circuits and Systems (LASCAS)*, pp. 167-170, 2016.

5. D.G. Muratore, A. Akdikmen, and F. Maloberti, **"Very High-Speed CMOS Comparators for multi-GS/s A/D Converters"**, *Proc. of IEEE Conference*

on Ph.D. Research in Microelectronics and Electronics (PRIME), pp. 240-243, 2015.

6. D.G. Muratore, E. Bonizzoni, and F. Maloberti, **"A Split Transconductor High-Speed SAR ADC"**, *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2433-2436, 2015.