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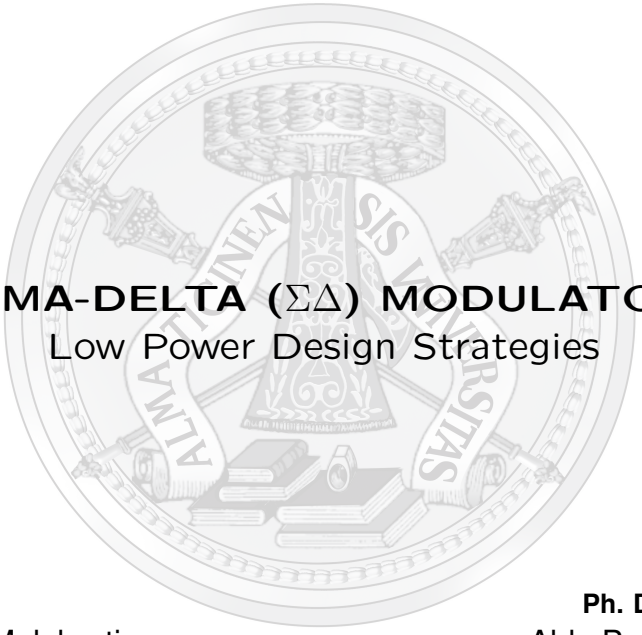
Integrated Microsystems Laboratory

Thesis Submitted as a Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy



SIGMA-DELTA ($\Sigma\Delta$) MODULATORS
Low Power Design Strategies

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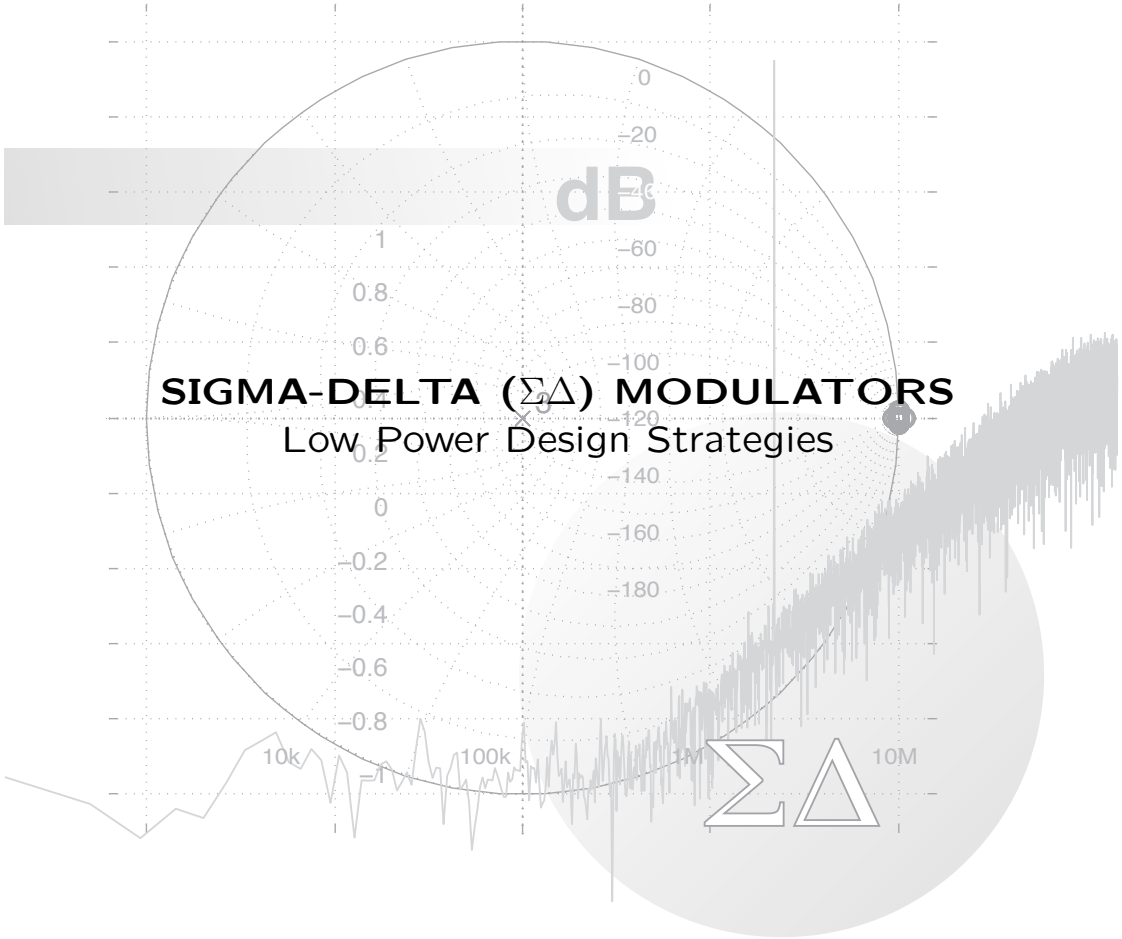

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Chapter 1

Introduction

Sigma-Delta ($\Sigma\Delta$) data converters have received a lot attention in numerous fields of signal acquisition and processing, such high-quality digital audio, instrumentation and measurement, and integrated transducer and sensor applications. However designing $\Sigma\Delta$ modulators requires a proper understanding of its operation principle. In this chapter a general background knowledge of the $\Sigma\Delta$ conversion and its benefits for medium-high resolution applications are explained. Furthermore, the main specifications, which give the general information and describe the features and limits of the modulator, are an important issue discussed here. A design guideline for minimum power consumption as well as the kT/C noise considerations give a clear overview of the optimum trade-off between resolution and consumed power. Finally, a brief description of recently state-of-the-art $\Sigma\Delta$ architectures and its design techniques for targeting both low power an the expected noise shaping benefit are included.

1.1 A Brief Overview of $\Sigma\Delta$ Concepts.

In recent years, portable electronics, such as personal wireless communication devices, digital cameras, personal audio devices, etc., find booming markets. Powered by batteries, their supply voltage is often limited, and the battery lifetime is of great importance for these devices. All these factors address the requirements of low-voltage low-power system building blocks. Furthermore the same scaling of VLSI technology, that makes possible the continuing dramatic improvements in digital signal processor performance, also severely constrains the

dynamic range available and forcing the design to work at lower supply voltage. However, low voltage environments make challenging the interface implementation between the digital and analog representation of signals.

As an important building block, analog-to-digital-converters (ADCs) are widely used in various systems where the need for low power, high accuracy and small area size are of critical importance [1], [2], [3], [4], [5], [6] . Among different ADC topologies, sigma-delta ($\Sigma\Delta$) modulators efficiently trade speed for accuracy, providing an effective way to implement high resolution ADCs without stringent matching requirements or calibration in low voltage environment. By means of oversampling ratio (OSR) and noise shaping, the $\Sigma\Delta$ architecture transfers most of the signal processing tasks to the digital domain where the power consumption can be drastically reduced by the technology scaling down and supply voltage decreasing.

Although the term sigma-delta ($\Sigma\Delta$) was used by some of the earliest researchers in the field [7], [8], [9] the term $\Sigma\Delta$ has also become almost synonymous with noise shaping ADCs.

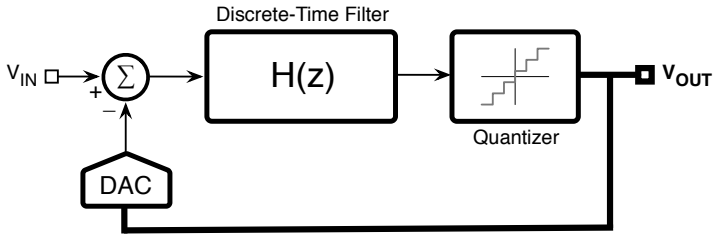


Figure 1.1: Basic structure of a $\Sigma\Delta$ modulator.

Fig. 1.1 shows the basic structure of a $\Sigma\Delta$ modulator. The architecture consists of a discrete-time filter, H(z), and a coarse quantizer enclosed in a feedback loop by a digital-to-analog-converter (DAC) [10], [11]. The output, V_{OUT}, is subtracted from the input signal, V_{IN}, which has been sampled at a rate much larger than the Nyquist rate. The result, after passing through the discrete-time filter, H(z), serves as an input to the quantizer itself, which usually has a reduced number of levels. If the gain of the filter is high in the interval of frequency of interest (F_B), and low out of it, the quantization error (defined as the difference between the output of the filter and that of the quantizer) is attenuated in said band due to the feedback loop. This behavior has resulted in the qualifier noise shaping.

The linear model of Fig. 1.2(a) represents the quantization error with the additive noise, ϵ_q, that is a second input of the circuit. The model includes a digital decimation filter connected at the output of the modulator [11]. Since the analog input signal, V_{IN}, is sampled at the sampling frequency, F_S, which is much greater than the Nyquist rate (see Fig. 1.2(b)), out of band quantization noise is eliminated, without affecting the signal band, with the digital decimation filter that also resamples the signal at the Nyquist rate.

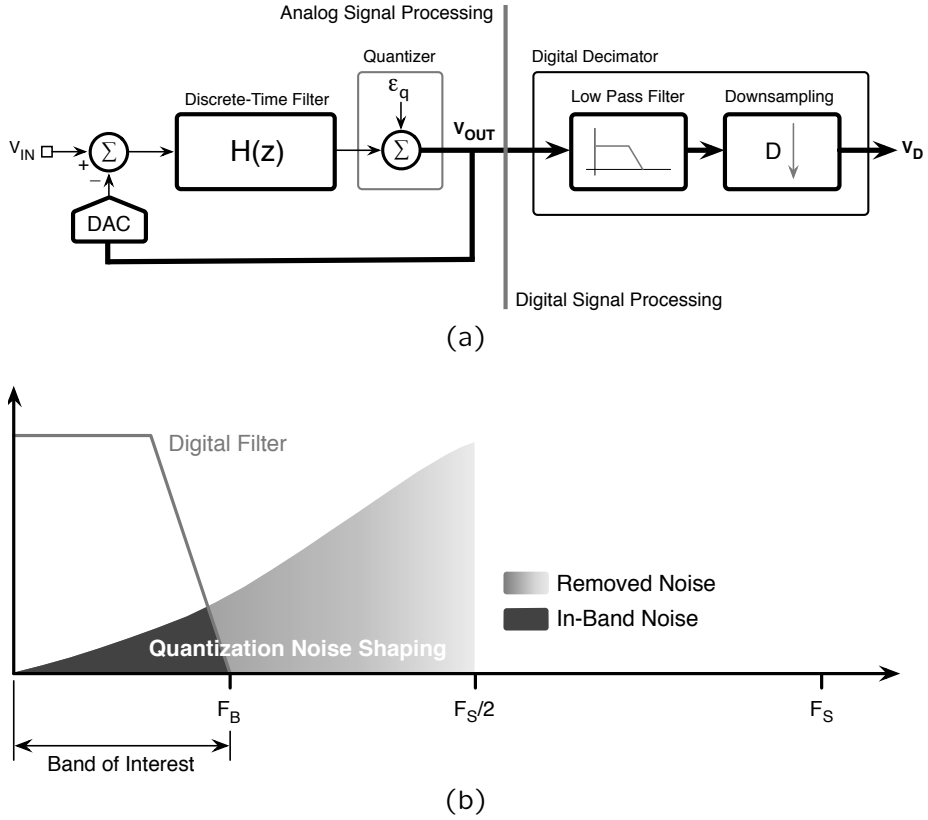


Figure 1.2: (a) Linear model of the $\Sigma\Delta$ modulator. (b) Signal processing of the $\Sigma\Delta$ conversion.

The modulator in Fig. 1.2(a) can be viewed as a two-input, $v_{in}(t)$ and $\epsilon(t)$, one output, $v_{out}(t)$, system, which in the Z-domain can be represented by

$$V_{OUT}(z) = V_{IN}(z) \cdot STF(z) + \epsilon_q(z) \cdot NTF(z) \tag{1.1}$$

where $V_{IN}(z)$ and $\epsilon_q(z)$ are the Z-transform of the input signal and quantization noise, respectively; and $STF(z)$ and $NTF(z)$ are the respective signal transfer function and noise transfer function. Equation (1.1) shows that the signal and the quantization noise are processed differently by the modulator and the exact form of both functions will depend of the architecture.

The simplest $\Sigma\Delta$ architecture is shown in Fig. 1.3. It is a first-order loop wherein the discrete-filter consists of a single integrator with delay. The modulator implements the quantization function with a n-bit ADC, which is equivalent to the addition of a quantization error ϵ_q of Fig. 1.2(a) [10].

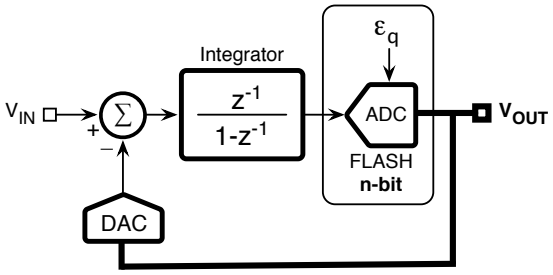


Figure 1.3: First-order ΣΔ modulator.

By inspection of the circuit the output of the modulator in the Z-domain is

$$V_{OUT}(z) = V_{IN}(z) \cdot z^{-1} + \epsilon_q(z) \cdot (1 - z^{-1}) \tag{1.2}$$

Notice that input signal is passed through of a delay while the quantization noise is processed by the high-pass $(1 - z^{-1})$. This transfer function gives a *first-order noise shaping performance*, thus the architecture of Fig. 1.3 is called first-order ΣΔ modulator.

Higher order ΣΔ modulators can be obtained by addign more than one integrator in the forward path. This kind of architectures obviously obtains high-order noise transfer functions

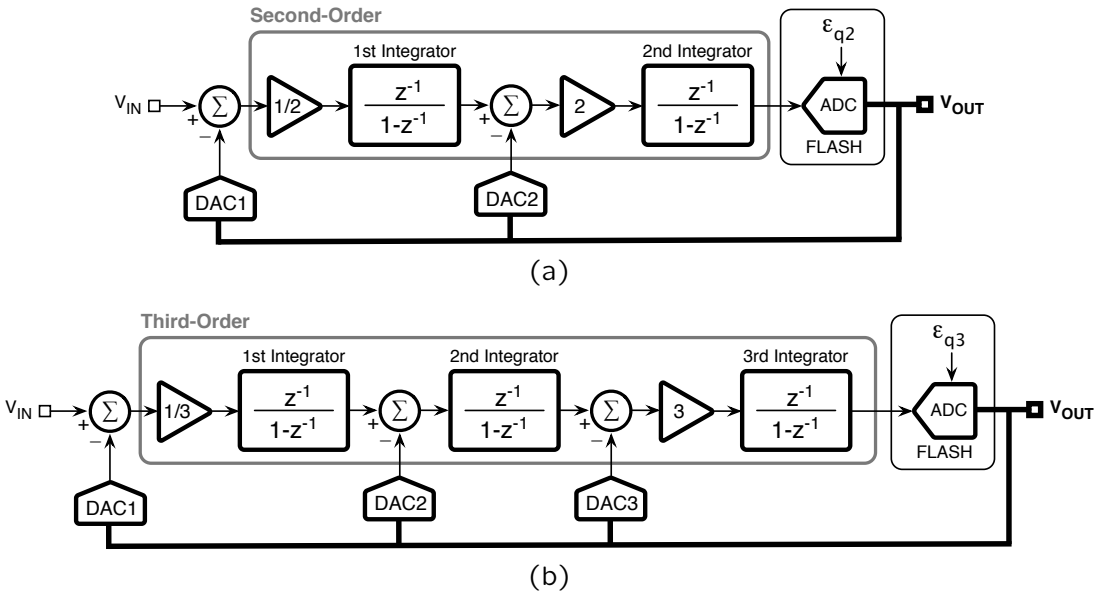


Figure 1.4: Conventional ΣΔ modulators. (a) Second-order architecture. (b) Third-order architecture.

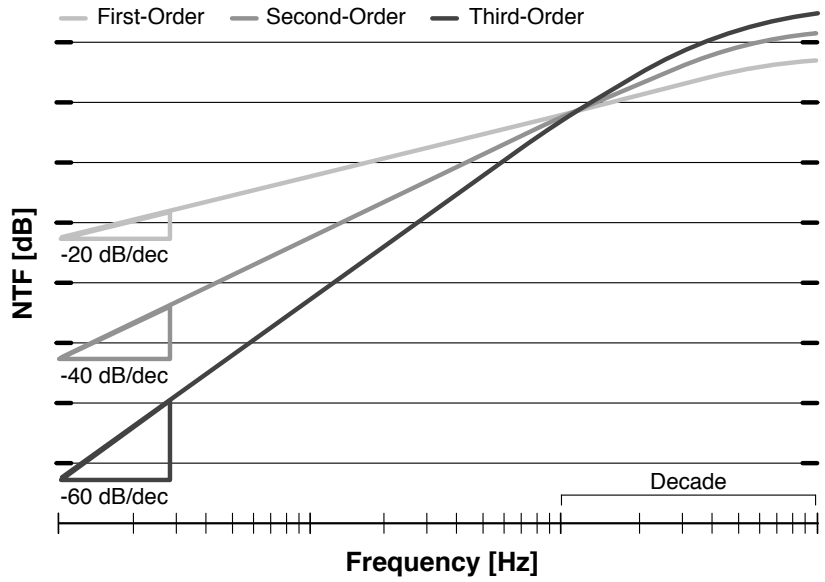


Figure 1.5: Conceptual noise shaping comparison.

and gives the potential of increased resolution, but at the same time suffer special challenges for the design and stability [12], [13].

Fig. 1.4 shows the block diagrams of a conventional second [14] and third-order [15] modulators with the proper scaling coefficients for the delayed integrators. Considering ϵ_{q2} and ϵ_{q3} the quantization noise of the second and third order architecture respectively, the equations that describe the modulator outputs are

$$V_{OUT}(z) = V_{IN}(z) \cdot z^{-2} + \epsilon_{q2}(z) \cdot (1 - z^{-1})^2 \tag{1.3}$$

$$V_{OUT}(z) = V_{IN}(z) \cdot z^{-3} + \epsilon_{q3}(z) \cdot (1 - z^{-1})^3 \tag{1.4}$$

The former equation exhibits a double delay for the signal transfer function and the noise transfer function is $(1 - z^{-1})^2$, the square of the result obtained by a first order modulator. A similar analysis exhibits equation (1.4) but it obtains and additional delay for the signal transfer function and the expected third-order noise transfer function.

Fig. 1.5 shows the conceptual comparison of the noise shaping behavior of the architectures of Fig. 1.3 and Fig. 1.4. Since with a first order $\Sigma\Delta$ modulator it is necessary to use high sampling frequencies to secure high resolution, better performances and features are obtained by using two or three integrators around the loop. At low frequencies, the NTF of the first and second-order modulator are 20 dB/decade slope and 40 dB/decade slope respectively, while the NTF of the third-order modulator has a 60 dB/decade slope.

An alternative solution for high-order architectures, not discussed in this thesis work, is the cascade of low-order modulators that obtain high-order noise shaping without incurring in stability troubles [16], [17]. However, these architectures (also named MASH, *multi stage noise shaping*) call for precise gain matching between the individual low-order sections, a requirement that conflicts with the goal of designing A/D converters that are specially insensitive to parameter tolerances and component mismatch.

A large set of specifications are used to characterize the performance of $\Sigma\Delta$ converters [11]. These give general information and describe the features and limits of the modulator. The most popular specifications and its technical terms are explained as follows.

- ***Oversampling Ratio (OSR).*** In signal processing, oversampling is the process of sampling a signal with a sampling frequency, F_S, significantly higher than twice the signal bandwidth F_B. Oversampling helps avoid aliasing, improves resolution and reduces noise but increases the consumed power of the modulator. The oversampling ratio is defined as

$$OSR = \frac{F_S}{2 \cdot F_B} \tag{1.5}$$

- ***Signal-to-Noise-Ratio (SNR).*** The SNR defines how much a signal has been corrupted by noise. The SNR is defined as the power ratio between the signal and the total noise produced by quantization and the noise of the circuit. The SNR accounts for the noise in the entire Nyquist interval. Moreover the SNR can depend on the frequency of the input signal and it decreases proportional to the input amplitude. Because many signals have a very wide dynamic range, the SNR is often expressed using the *decibel scale* (dB) and defined by

$$SNR\,|_{dB} = 10 \cdot log \frac{P_{sign}}{P_{noise}} \tag{1.6}$$

  where P_{sign} and P_{noise} are the power of the signal and the power of the noise in the band of interest.

- ***Signal-to-Noise-and-Distortion-Ratio (SNDR or SINAD).*** Is similar in definition to the SNR however, non linear distortion terms, produced by the input signal, are also included. The SNDR is defined as the ratio between the root-mean-square (rms) of the signal and the root-sum-square (rss) of harmonics components plus noise, but excluding the DC component. The SNDR is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion. This parameter is often plotted for various input amplitudes and frequencies. It is usually given in dB.

- ***Spurious-Free-Dynamic-Range (SFDR).*** Is the ratio between the rms of the signal and the rms of the highest spurious spectral component in the first Nyquist Zone. With large input signals the highest (or worst) component is given by one of the harmonics of the signal. Quoted in dB, the SFDR is an important specification in communications systems because it represents the smallest value of signal that can be distinguished from a large interfering signal.

- ***Effective-Number-of-Bits (ENoB).*** This parameter measures the SNDR (or SINAD) using bits. An often used definition for ENoB, where the SNDR is expressed in dB, is

$$ENoB = \frac{SNDR\,|_{dB} - 1.76}{6.02} \tag{1.7}$$

  The above equation is obtained from the theoretical SNR of an ideal n bit ADC converter with a sine-wave excitation [11].

- ***Dynamic-Range (DR).*** Typically expressed in dB, dynamic range is the value of the input signal at which the SNR or SNDR is 0 dB. The DR specification is useful for $\Sigma\Delta$ architectures that do not obtain their maximum SNR or SNDR at full-scale input amplitude (0 dB_{FS}).

- ***Figure-of-Merit (FoM).*** This parameter establish the power effectiveness of Modulator. The FoM used in this thesis work is expressed in *Joules-by-conversion-level* (J/conv-level) and is given by the following expression

$$FoM = \frac{P_W}{2^{ENoB} \cdot BW} \tag{1.8}$$

  where P_W is the total power consumption of the modulator, BW is the bandwidth of the input signal and ENoB is the effective number of bits described before. Effective solutions show an FoM below than 500 fJ/conv-level. The figure of merit depends on the architecture of the modulator and the line-width of the technology. Moreover, there are several definitions of the FoM. In some cases the dynamic range is used instead of ENoB [10], in other definitions the sampling frequency replaces the signal bandwidth [18].

1.2 kT/C Considerations and Design for Minimum Power Consumption.

The sampled thermal noise (defined as kT/C noise) is a major limitation of switched-capacitor (SC) circuits, and must be taken into account in the design. This unavoidable limit is

associated with the sampling switch. Considering the noise voltage as $\sqrt{kT/C}$, sampling any signal using a sampling capacitance of 1 pF leads to 64.5 μV noise voltage. If the sampling capacitance increases by α factor, the noise voltage diminishes by $\sqrt{\alpha}$ [11].

When designing a $\Sigma\Delta$ modulator, it is important to find a good balance between the contributions of all noise sources. It means that all noise sources are scaled in a way that makes the circuit implementation affordable for the required application.

A defined full scale input, V_{FS}, and a given n bit resolution establish the total noise power budget defined by [10], [11]

$$P_{N,tot} = V_{n,budget}^2 = \frac{V_{FS}^2}{12 \cdot 2^{2 \cdot n}} \tag{1.9}$$

A designer must then divide this available noise budget between various noise sources, predominantly, quantization noise P_Q, kT/C noise $P_{kT/C}$, interference noise P_{IT} and noise coming from references P_{REF}. The trade-off between various design constraints determines the fraction of the noise budget that can be allocated for the kT/C sources and thus the minimum value of the sampling capacitance can be estimated. Since for low power applications kT/C is the major concern, the quantization noise must be a fraction of the total budget. A reasonable example of the noise power budget assignment is as follows (see Fig. 1.6)

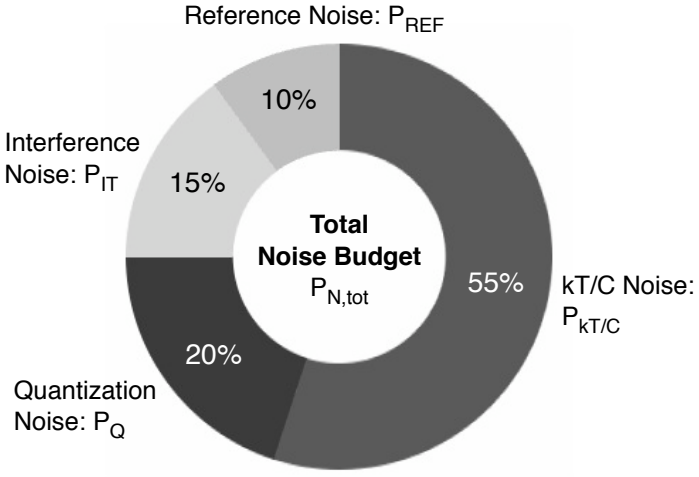


Figure 1.6: Example of noise power budget assignment.

$$\begin{aligned} P_{kT/C} &= 0.55 \cdot P_{N,tot} \,; P_Q = 0.20 \cdot P_{N,tot} \\ P_{Int} &= 0.15 \cdot P_{N,tot} \, P_{Ref} = 0.10 \cdot P_{N,tot} \end{aligned} \tag{1.10}$$

where $P_{N,tot}$, $P_{kT/C}$, P_Q, P_{Int} and P_{Ref} are the total, kT/C, quantization, interference and reference noise power, respectively. Therefore, noise shaping must be able to bring the quantization noise below specification by 12 dB. This provides room to the more power hungry kT/C term.

Design parameters controlling power consumption of sigma-delta modulators are the supply voltage, the oversampling ratio, the order of the modulator and the number of bit of quantization. Lowering the supply voltage at constant current reduces power. However, a reduced supply voltage diminishes the full scale of the converter, V_{FS}, and, in turn, increases the relevance of the kT/C noise. For kT/C limited design, the SNR is $OSR \cdot {V_{FS}}^2 C/(16kT)$. Therefore, a reduction of V_{FS} requires to increase the sampling capacitance. A given OSR, accuracy and input band determines the product gain bandwidth, f_T (or GBW), of the op-amp. In turn, the f_T is proportional to g_m/C. If transistors are in sub-threshold, g_m is $I_D/(nV_T)$, while for transistors in saturation region g_m depends on bias current as $\gamma I_D^{1/2}$. Therefore, SNR becomes

$$\begin{aligned} SNR|_{sub-treshold} &= OSR \cdot k_1 \frac{{V_{FS}}^2 \cdot I_D}{f_T} \\ SNR|_{saturation} &= OSR \cdot k_2 \frac{{V_{FS}}^2 \cdot I_D^{1/2}}{f_T} \end{aligned} \tag{1.11}$$

where k_1 and k_2 are design constants. Equation (1.11) shows that reducing by a factor α the supply voltage, that reduces by the same factor V_{FS}, asks for compensation with an increased current in the transistor pair granting the transconductance gain. The current increase is by α^2 for transistors in sub-threshold and α^4 in saturation. Therefore, reducing the supply voltage is detrimental to power effectiveness: *the designer should use the nominal voltage allowed by technology and not less*.

A second design option is to increase the oversampling ratio. As known, it improves SNR by an extent that depends on the order of the modulator. To secure one more bit, OSR should increase by 1.32 for a second order and by 1.21 for a third order modulator. However, higher sampling frequency requires an equally augmented bandwidth of op-amps. It is proportional to the bias current of the input pair in sub-threshold and to the square root of bias current with transistors in saturation. Therefore, one more bit in a second or third order modulator demands for an augmented current by 32% or 21% in the input pair in sub-threshold and 74% or 46% when in saturation. Therefore, increasing the oversampling ratio to augment SNR must be carefully considered in low-power applications.

The number of op-amps equals the order of the modulator. Supposing to use same power in op-amps, the ones of a third order modulator consume 1.5 times more than a second order, but the modulator obtains higher SNR because of more effective noise shaping. The benefit on SNR depends on the OSR. Since there is a fixed cost $\pi^{2L}/(2L+1)$ (L is the modulator

order) [11] equal to 12.9 dB (2.1 bit) for second order and 21.4 dB (3.5 bit) for third order, the advantage, in bit, is $[log_2(OSR) - 1.4]$. With OSR = 8, the use of a third order instead than a second one gives 1.6 more bit and with OSR = 16, 2.6 bit. The figure is more power effective than increasing the OSR of a second order modulator, even at OSR = 8.

Another design option is the number of quantization levels that, obviously, costs an equivalent power. To ensure one extra bit, it would be necessary to double the power of the flash. This, for relatively low resolution, leads to an affordable cost because power consumed by a comparator is a small fraction of the op-amp power. For set of specifications in the video range (i.e., bandwidth higher than 5 MHz), a comparator consumes the 2-3% of an op-amp. Therefore, increasing the flash resolution from 3 to 5 bits, that means using 24 more comparators, costs 24-34% op-amps power with second order modulators and 16-24% with third order. Since accuracy increases by 2 bit, the power benefit is evident. However, many bits in the flash and, hence, in the DAC can be problematic when Dynamic Element Matching (DEM) [19] becomes necessary.

The points discussed above provide the guidelines for a proper low power design. Since SNR and SNDR requirements are relatively low, the first choice is to use 5 bit quantization that, with OSR = 12 and second order noise shaping, grants a maximum theoretical SNR equal to 72.6 dB. The same resolution, OSR = 8 and third order noise shaping lead to an SNR equal to 73.4 dB. Since both expected SNRs allocate the required margin, the choice between two options depends on power. As discussed above, with transistors in sub-threshold region, the power consumption would be the same for both solutions, but, for transistors in saturation, as actually needed to satisfy our speed requirements, the third order solution is the right choice because it consumes less.

1.3 State-of the-Art Techniques for Low Power Consumption.

A low power efficiency $\Sigma\Delta$ modulator can be accomplished by a proper choice of three main design parameters: *oversampling ratio (OSR), the order of the modulator (L) and the number of bits used for the quantization*. High oversampling grants good resolution but high sampling frequencies leads to high consumed power in the op-amps. The use of high-order modulators secures high resolution but requires a large number of op-amps, thus an aggressive noise shaping performance is power demanding. The use of multi-bit architectures benefits in obtaining extra bits, however multi-bit structures making the design relatively complex and imposes the need of a flash converter with the necessary number of comparators to ensure the quantization levels. Moreover, multi-bit DAC is source of harmonic distortion that can be fixed by using DEM [20].

Several design techniques, motivated by the above considerations, have been reported recently. This solutions, as will be discussed shortly, benefit the power consumption and keeping the noise shaping performance while reducing, in some cases, the number of the op-amps used in the modulator, and in other cases, the dynamic output swing in the integrators.

Time-sharing technique [21], [22], has been used in many schemes to reduce the silicon area and, more important, to limit the power consumption. The technique has been effectively used in switched-capacitor filters [23], [24] where normally the two-phases are used, one for sampling the signal and the other for the processing. Since the sampling is passive and the processing requires an op-amp, during the sampling phase, the op-amp is not used. Therefore, suitable modifications enable the use of the op-amp when its action is not required. For example, a high order filter that uses an op-amp during one phase and another op-amp during the other phase can be re-arranged to perform with a single op-amp the two functions, [25]. The time-sharing approach has also been used in pipeline data converters, [26], architectures that generate an analog residual during one phase and another one during the complementary phase can share the op-amp required. It is difficult to use the time sharing approach in sigma delta modulators because the quantizer needs a time-slot for its operation and, since the time-sharing delays the operation of one of the performed functions, the time slot used for the time-sharing is at the expenses of the one needed by the quantizer. Furthermore, since the power of the op-amp must increase because of the increased slew-rate performance, the power benefit is lower than 50%.

A more effective way for reducing the number of op-amps is proposed in [27]. The method is an extension of the approach proposed in [28] and can be extended to any modulator order. Moreover, the technique does not require using a specific time slot for an op-amp time sharing function. The method, as shown in Fig. 1.7, uses a general $\Sigma\Delta$ modulator with the cascade of n integrators followed by an A/D converter and n feedbacks from the output of the modulator.

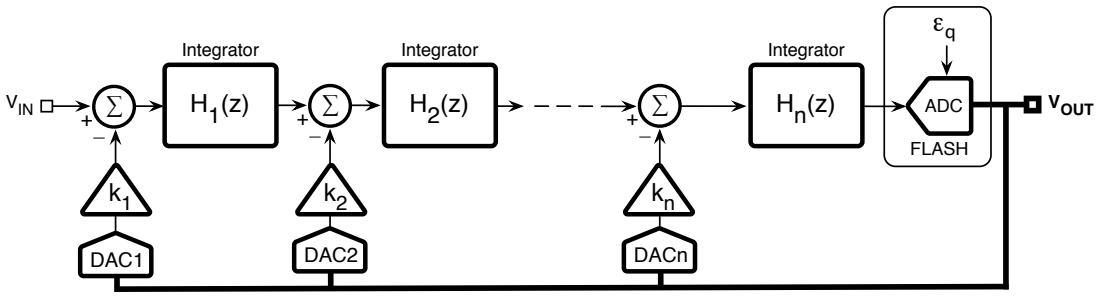


Figure 1.7: General $\Sigma\Delta$ modulator with n integrators and n feedbacks.

The used technique move the feedback path, at the input of the $i-th$ stage, to the input of the previous $(i-1)-th$ stage by diving its contribution by the transfer function $H_{i-1}(z)$. After

to move all the feedback factors to the first feedback position (see Fig. 1.8), the total feedback coefficient results in

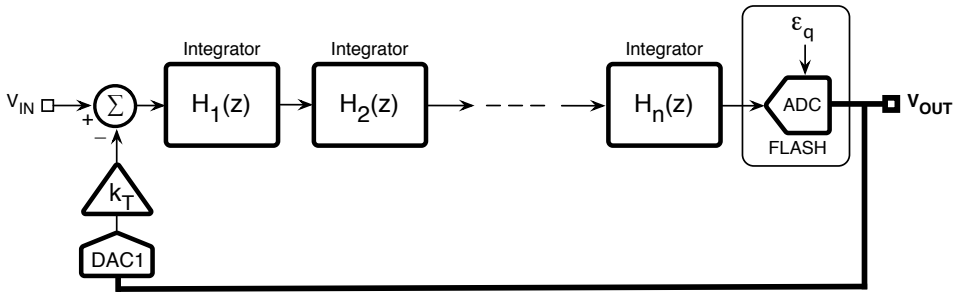


Figure 1.8: General $\Sigma\Delta$ modulator with n integrators and n feedbacks.

$$k_T = k_1 + \frac{k_2}{H_1(z)} + \ldots + \frac{k_n}{\prod_1^{n-1} H_i(z)} \tag{1.12}$$

while the transfer function of the cascade is obtained by the product of the single blocks $H_1(z)$,...,$H_n(z)$ and is given by

$$H_T(z) = \frac{z_p}{(1 - z^{-1})^n} \tag{1.13}$$

where n is the number of cascaded integrators and p is the total delay around the loop. Since the final architecture employs a DAC from the output of the modulator, the signal processing of k_T can be performed in the digital domain before the DAC.

As is know double sampling is a powerful technique to achieve an effective sampling frequency that is twice the actual modulator clock frequency [29]. This efficient solution allows the speeding up of the operation of switched-capacitor integrators thanks to the active operation of the op-amp during both phases. Moreover, in $\Sigma\Delta$ architectures doubling-sampling techniques improves the SNR, without increasing the op-amp power consumption, as $3(2{\cdot}L{+}1)$ dB, where L is the order of the modulator. Nevertheless, double sampling shows several disadvantages that limit its applications. In its simplest implementation with two sampling capacitors in push-pull mode operation, any mismatch in the two paths introduces the modulation of the input signal which results in the folding of the spectrum around F_S/2 to the baseband [30]. This problem can be tackled by introducing an SC integrator with a fully floating input branch [30] or with its modified version presented in [31]. The other major limitation is the critical timing constraints because the integrator uses the full clock period, and therefore the quantization process is performed primarily during the non-overlapping times of the clocks. The solution presented in [32] solves this problem by adding to the modulator architecture two fully-cycle

delayed branches. One is from the modulator input while the other branch comes from the modulator output, both branches are connected in a summing node in front of the quantizer.

Analog feedforward path (AFF) [11] is a efficient technique for reducing the power consumption of the op-amps in $\Sigma\Delta$ architectures. Feedforward solutions offer several advantages since minimizes the op-amp output swing: *the slew-rate and bandwidth requirements are relaxed, favor better linearity, enables the implementation of power effective op-amp schemes like single stage telescopic topologies and allows operation at low power supply voltages*. The method works well for all integrators of the modulator by using an analog summing block connected in front of the flash converter. Fig. 1.9 shows a conventional second-order feedforward $\Sigma\Delta$ topology with reduced sensitivity to op-amp non linearities [33].

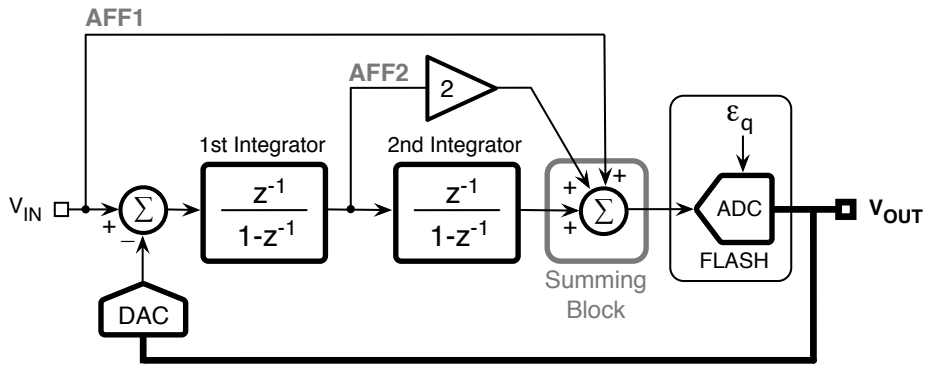


Figure 1.9: Second-order feedforward $\Sigma\Delta$ modulator.

With feedforward solutions the integrators output goes down to the quantization noise level that, for multi bit structures, means a fraction of the maximum input. There are several ways to implement the summing function. A method employs a SC summing op-amp to add all the feedforward paths [34], [35]. This implementation is usually used to meet the stringent headroom requirements and to provide high sufficient gain, however induces a large output swing of the summing block, adds design complexity and increases the power consumption of the modulator. Another summing circuit using charge sharing is presented in [36], [37]. The summing operation is accomplished trough charge sharing realized with a switched-capacitive network connected at each comparator input. Furthermore, to maintain the signal swing at the flash input, the reference voltage must be scaled down from its nominal value by a factor equal to the voltage drop across the passive network, thus comparators with higher sensitivity are required. This approach eliminates the need for a summing op-amp, but the signal swing and the step in the quantizer threshold voltages are attenuated due to parasitics associated with the passive network. These limits result in increased power dissipation and mismatch effects at the quantizer, but are substantially compensated by using additional compensation capacitances connected to the SC network [37].

To overcome the drawbacks of the above analog implementation, an alternative solution proposed by [38] performs the summing operation in the digital domain. The technique employs digital feedforward (DFF) at the input of the last integrator as well as after the quantizer, and analog feedforward for the first integrators, thus an additional flash converter is used to obtain the quantized version of the input signal of the modulator. The solution is well effective in multi-bit structures where the number of bits for the quantization is large. Moreover, thanks to the swing reduction technique the total number of comparators goes down.

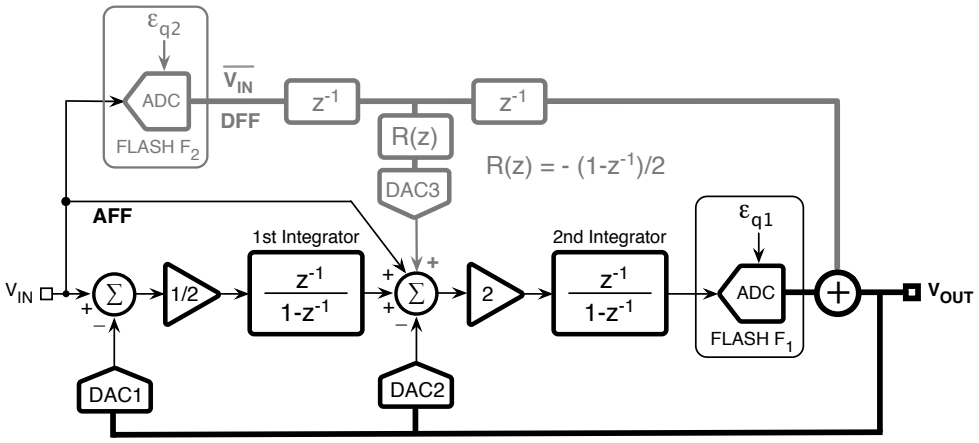


Figure 1.10: Conventional second-order $\Sigma\Delta$ modulator with digital feedforward (DFF) path.

In particular, for a conventional second-order $\Sigma\Delta$ modulator, like the one shown in Fig. 1.10, with 4 bits in the main flash converter (F_1) and 3 bits in the additional flash (F_2), the total number of comparators used by the modulator is 12 (5 from F_1 and 7 from F_2) instead of 23. Furthermore, since the extra flash converter injects additional quantization noise (ϵ_{q2}) at the modulator output, the digital feedforward path at the input of second integrator whit gain $R(z) = -(1 - z^{-1})/2$, is utilized to cancel the effect of ϵ_{q2} at the output of the modulator itself. Notice that digital feedforward solution does not requires additional branches at the input of the integrators that worsen the feedback factor.

A fully digital feedforward solution is presented in [39]. The method, as depicted in Fig. 1.11, uses a second-order $\Sigma\Delta$ modulator with unity gain STF and an extra flash converter (F_2) for implement the feedforward path in the digital domain. The loop filter is designed such that the modulator output is

$$V'_{OUT} = V_{IN} + (1 - z^{-1})^N \cdot \epsilon_{q1} + (1 - z^{-k}) \cdot \epsilon_{q2} \tag{1.14}$$

where N is the order of the loop filter, ϵ_{q1} and ϵ_{q2} are the quantization noise of the main and additional flash converter, respectively, and k is a design parameter. Similarly to the above

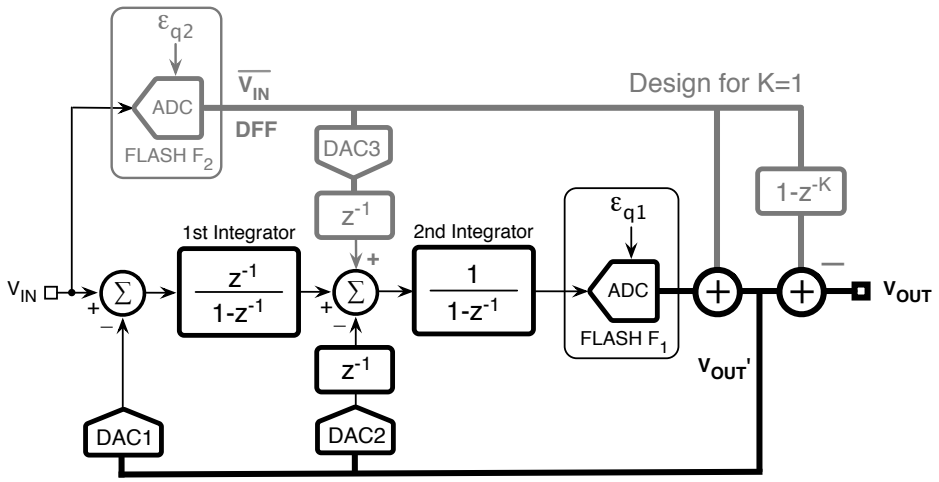


Figure 1.11: Fully digital feedforward (DFF) path in a conventional second-order $\Sigma\Delta$ modulator.

technique, the additional quantization noise (ϵ_{q2}) is canceled at the modulator output without affecting the STF. The output (V_{IN}+ϵ_{q2}) of the extra flash converter is multiplied by $(1 - z^{-k})$ and subtracted in the digital domain from the output of the main flash converter. For a design with $k = 1$ any leakage of the additional quantization noise ϵ_{q2} is shaped to first-order [39].

An effective alternative fully digital feedforward technique has been reported in [40]. Contrary to the above solution, the method avoid the quantization noise cancellation done after the main flash converter, before and after the loop filter. Considering ϵ_{q2} the quantization noise of the additional flash converter, the main contribution term of each integrator output, $V_{IN} \cdot H(z)$ (where V_{IN} is the input signal and $H(z)$ is a transfer function due to the integrator process), is compensated with its quantized version $\overline{V_{IN}} \cdot H(z)$ (whit $\overline{V_{IN}} = V_{IN} + \epsilon_{q2}$), which is added and subtracted at the output of each integrator without change the overall result. To obtain the desired term cancellation, the quantity $-\overline{V_{IN}} \cdot H(z)$ is moved back to the input of the actual integrator dividing it by the transfer function of the integrator itself. For the last integrator of the modulator the reconstruction at its output is realized in the digital domain after the flash converter. Final topological modifications lead an architecture with distributed digital feedforward that reduce the integrators output swing and reconstruct both the original NTF and STF after each integrator.

An improved third-order $\Sigma\Delta$ modulator has been introduced in [35]. The architecture employs a second-order feedforward $\Sigma\Delta$ topology to ensure low output swing in the integrators. Moreover, the modulator increases the noise shaping performance from second to third-order by the injection of shaped quantization noise into the loop. The shaped quantization noise is obtained, as shown in Fig. 1.12, from the conventional modulator topology by including an

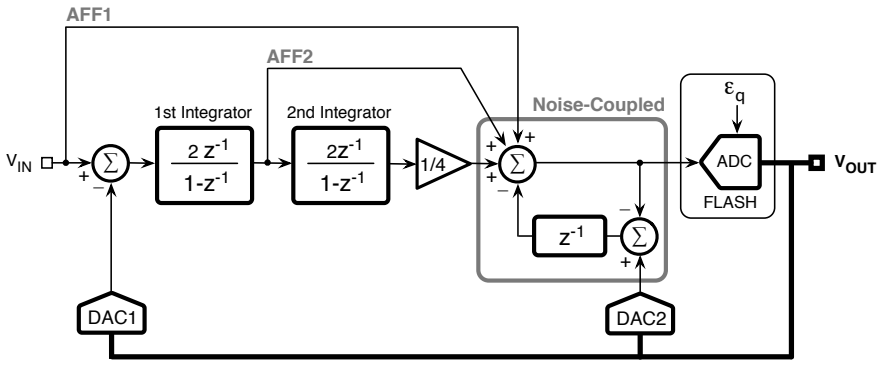


Figure 1.12: Third-oder $\Sigma\Delta$ modulator with noise coupled injection technique.

additional branch, where the quantization noise is delayed by one clock period and subtracted at the summing node before the quantizer. The enhancement does not change the STF of the modulator, however is equivalent to adding one more integrator to the loop filter. The use of an extra op-amp provides the virtual ground for both summing function and noise coupling injection. The technique is effective, but the use of an additional active adder at the quantizer input vanishes the power reduction benefit.

1.4 Structure of the Thesis.

This thesis work describes power efficiency $\Sigma\Delta$ architectures addressing the earlier low power strategies. The proposed modulators keeping low the oversampling ratio and achieve the expected noise shaping performance with reduced number of op-amps and low integrators output swing. Fig. 1.13 summarizes the general structure of this thesis work, which is organized as follows.

Chapter 2 presents the design of a third-order $\Sigma\Delta$ topology suitable for Digital Video Broadcasting Handled (DVB-H) requirements. The specifications of the given application are also outlined. Topological modifications that lead an architecture with only two op-amp in a conventional third-order $\Sigma\Delta$ modulator are described with detail. Moreover, a new design technique, which enables op-amp swing reduction in the last integrator and further reduces the number of comparators needed in the flash, is also discussed. This feature is based on the good correlation between two successive input samples in the flash converter. A circuital description of the main blocks and a switched-capacitor implementation are presented. Simulation results of the modulator at behavioral level with MATLAB (considering the op-amp limitations) and measurements results that confirm the effectiveness of the modulator are well discussed. This chapter concludes with the summary performance of the modulator, integrated in a 0.18 μm standard

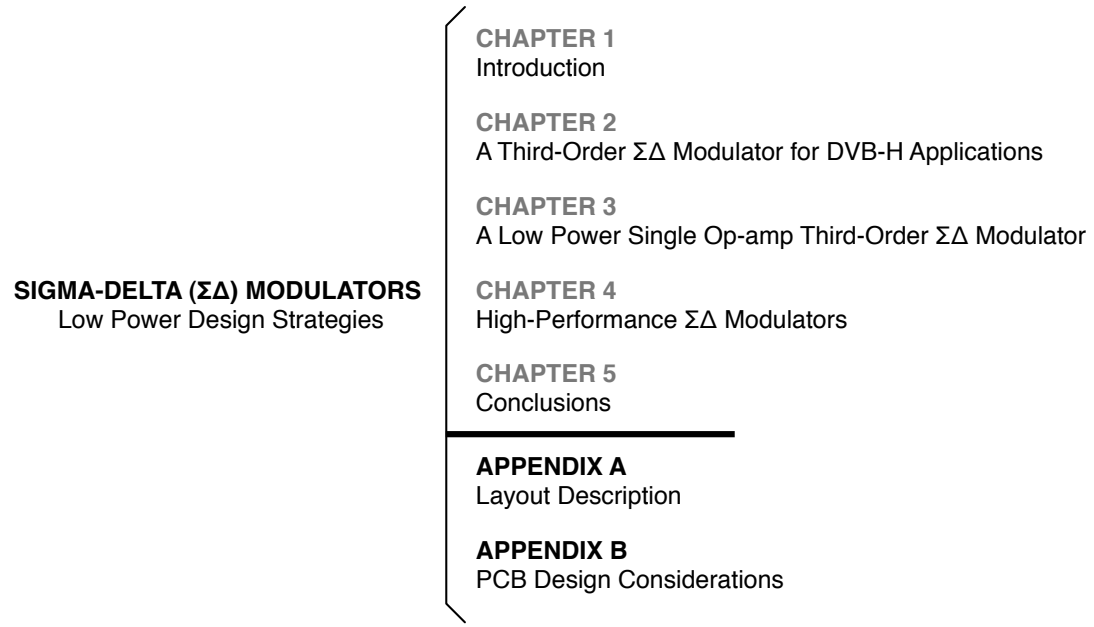


Figure 1.13: Thesis structure.

CMOS technology, and its comparison whit other similar state-of-the-art $\Sigma\Delta$ modulators.

In **Chapter 3** a novel low power efficiency $\Sigma\Delta$ modulator is introduced. The design process of the final architecture based of a NTF synthesis technique is described. The modulator employs only one operational amplifier and targeting low output swing reduction, thus its performance is involved in wireless sensor networks applications which design specifications are also depicted. Another important issue discussed here is the auxiliary monitor circuit that boost the slew-rate performance of the op-amp only when is required. Moreover, a single Kelvin divider used to implement all DACs in the modulator completely cancels the error caused by gradient in the resistance values. A detailed switched-capacitor implementation and the circuital description of the main blocks of the modulator are highlighted. The prototype was fabricated by using a 0.18 μm standard CMOS technology. Finally, measurement results that confirm the behavioral study of the modulator and the power effectiveness of the architecture are found at the end of this chapter.

Chapter 4 deals two high-performance $\Sigma\Delta$ modulators for wide-band applications. The first modulator, proposed to solve the critical time constraints in double sampling schemes, obtains an additional delay for the quantization process. The approach, described with more detail in this chapter, is called Analog Look Ahead (ALA) technique. The proposed method is applied in a conventional second-order $\Sigma\Delta$ modulator with feedforward topology. A possible switched-capacitor network used to implement the summing block is also presented. The

second proposed $\Sigma\Delta$ architecture exhibits a third-order noise shaping enhancement thanks to the complex conjugate zeros in its NTF. As is described in the chapter, the result is achieved by the cascade of two active blocks that make one zero at z = 1 and two complex ones with imaginary part α/2. Also discussed here is the switched-capacitor structure of the second block that allows the improvement of the SNR by approximately 8 dB. Moreover, a fully digital feedforward solution that secures a low reduction in the integrators output swing is described. Considering the op-amp limitations, the chapter includes several simulations results at behavioral level that show the effectiveness of both proposed modulators.

Chapter 5 covers the general conclusions resulting of this thesis work.

Additional material is included in two appendices. **Appendix A** focuses the layout and schematic diagrams of the main blocks of the two third-order $\Sigma\Delta$ prototypes described in Chapter 2 and Chapter 3, respectively. **Appendix B** deals with several recommendations for the design of multilayer boards used for testing data converters, thus the layout of the test boards used for the measurement results reported in this thesis work are also included.

Chapter 2

A Third-Order $\Sigma\Delta$ Modulator for DVB-H Applications

This low-power $\Sigma\Delta$ modulator targets the Digital Video Broadcasting Handheld (DVB-H) requirements and achieves about 10 bit with 6 MHz signal band. Suitable topological modifications enable the realization of a third-order modulator with two operational amplifiers. Moreover, a technique for swing reduction of the last operational amplifier strongly reduces the number of comparators needed in the flash converter. The power reduction techniques limit the consumption to 6.18 mW, thus yielding a FoM of 0.58 pJ/conversion-level. Fabricated with a 0.18 μm analog CMOS technology, the active area of the circuit is 0.32 mm^2. Experimental measurements confirm the behavioral study made accounting for the op-amps limitations.

2.1 Specifications for Digital Video Broadcasting-Handheld (DVB-H).

DVB-H (Digital Video Broadcasting-Handheld) is the digital broadcast standard for transmitting broadcast content to handheld terminal devices, developed by the International DVB (Digital Video Broadcasting) Project [41], [42]. This standard is based on the earlier European terrestrial digital TV standard DVB-T (Digital Video Broadcast-Terrestrial) but tailored to the special requirements of the portable, pocket-size, battery-operated class of receivers. DVB-H

particularly features an IP (Internet Protocol) interface for easy network integration, a high capacity downstream, strong protection against transmission errors, and long battery usage time.

The typical user environment of a DVB-H handheld terminal is very quite comparable to the cellular radio environment. The term handheld terminal includes multimedia cellular phones with color displays as well as personal digital assistant (PDA) and pocket PC types of equipment. All these kinds of devices have a number of features in common: *small size, light weight, and long battery operation*. These properties are a precondition for mobile usage but also imply several severe restrictions on the transmission system.

The terminal devices lack an external power supply in most cases and have to be operated with a limited power budget. Low-power consumption, typically less than 10 mW, is necessary to obtain reasonable usage and standby cycles. DVB-H shall be designed in such a way that channels of 5, 6, 7, and 8 MHz bandwidth can be used.

The above demanding requirements can be satisfied with ΣΔ solutions. Furthermore ΣΔ modulators require minimum analog accuracy to enable their implementation in digital technologies, relatively low oversampling ratio (OSR) to obtain medium-high resolution and high power effectiveness (or low figure of merit, FoM) to meet the low power requirements. This design addresses the above-mentioned specifications, namely 6 MHz band and 60 dB SNR, with the goal of power consumption well below 10 mW, as shown in Fig. 2.1.

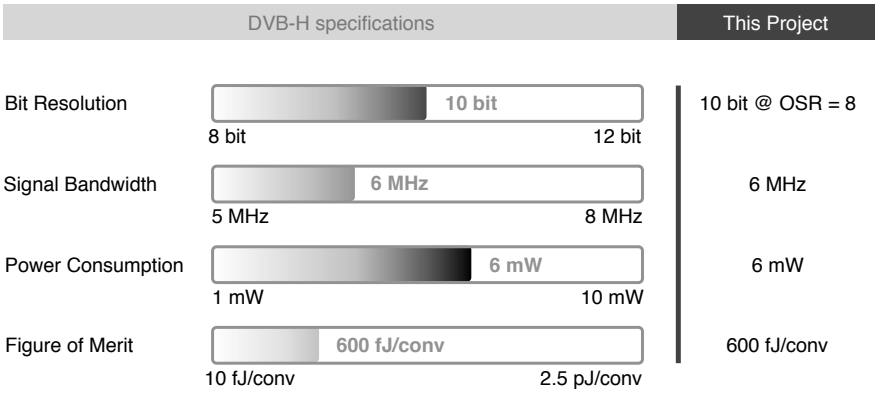


Figure 2.1: Digital Video Broadcasting-Handheld and project specifications.

2.2 Low Power ΣΔ Architecture.

In order to reduce the power consumption it is necessary to identify power hungry components, to limit their power request and possibly, their number. Since the power of an op-amp

increases in a quadratic way with its bandwidth, it is mandatory to keep at the minimum the clock frequency and, accordingly, the OSR. However, with low OSR, it is necessary to use high-order modulators, that means more op-amps, or to augment the resolution in the flash converter, that means more comparators. The trade-off depends on the power required by the single blocks. For this reason, preliminary transistor level simulations with 0.18 μm analog CMOS technology were made. Simulation results shown that an op-amp with 600 MHz bandwidth, 300 V/μs slew rate and 60 dB of gain consumes 2.3 mW, and a comparator with 5 mV sensitivity clocked at 100 MHz consumes about 60 μW. The numerical result provides the architecture recommendation: *use the maximum number of bit in the flash converter and the lowest OSR*.

2.2.1 Reduction of the Number of Op-amps.

Power is further reduced using only two operational amplifiers to obtain third-order noise shaping performance. The method used is described in this subsection. Fig. 2.2 shows the selected third-order ΣΔ scheme, [43]. It is based on a cascade of two integrators without delay and the last one with delay.

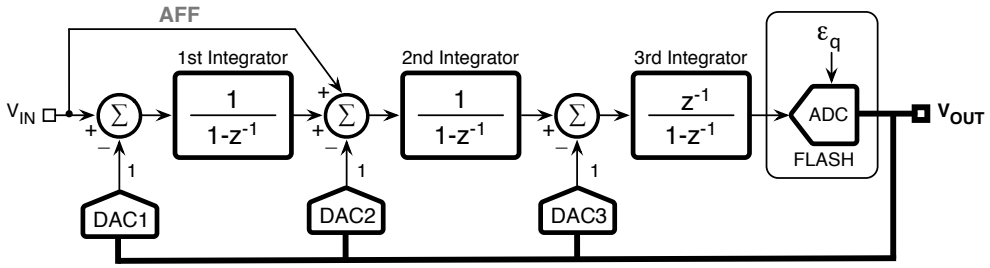


Figure 2.2: Conventional third-order ΣΔ modulator.

The analog feed-forward (AFF) path limits the output voltage swing of the first op-amp to the quantization noise level. Feedback coefficients necessary to make the noise transfer function (NTF) equal to $(1 - z^{-1})^3$ are all 1. Therefore, this architecture optimizes the feedback factors at the expenses of using integrators without delay. High feedback factors admit lower bandwidth; integrators without delay impose higher bandwidth. Overall, the op-amp bandwidths turn out to be lower in this architecture without delays.

Starting from Fig. 2.2, a number of topological modifications eliminate one of the op-amps [27]. First, the feedback at input of the third integrator is moved at input of second integrator multiplied by $(1 - z^{-1})$, as shown in Fig. 2.3 (a).

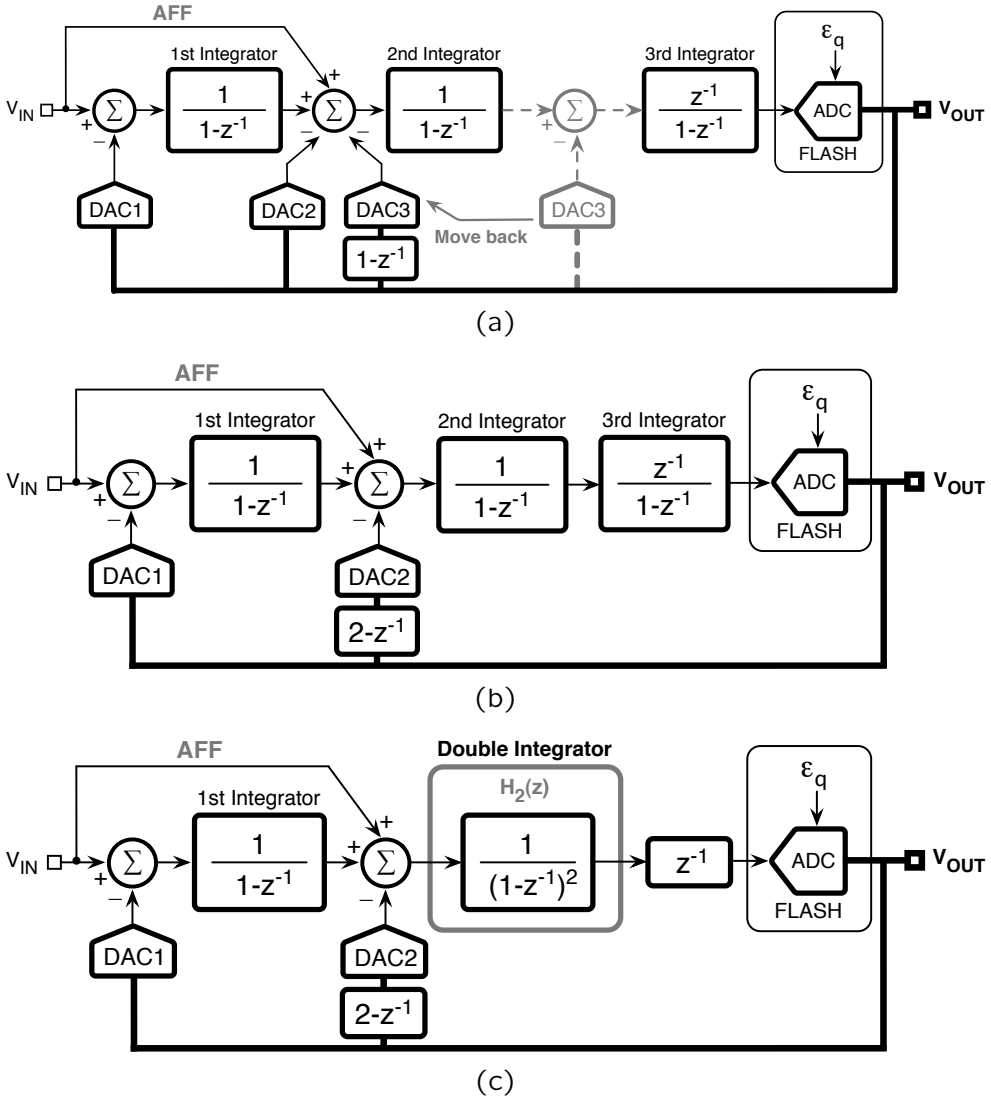


Figure 2.3: Topological modifications. One op-amp is eliminated.

The feedback of the second integrator, that becomes $(2 - z^{-1})$ as shown in Fig. 2.3 (b), requires a simple processing in digital domain before the second DAC.

The scheme after removing intermediate feedback includes a double integrator, Fig. 2.3 (c), which can be realized by one op-amp capable to implement the overall transfer function

$$H_2(z) = \frac{1}{(1 - z^{-1})^2} = \frac{1}{(1 - z^{-1}) - z^{-1} + z^{-2}} \tag{2.1}$$

The implementation of a double integrator, as shown in Fig. 2.4, consists in a conventional

integrator with two extra feedback terms, one with single delay (P-path) and another one with double delay (Q-path). The circuit, realized in the sampled data domain, requires a limited increase of the op-amp power consumption (about 30%). Therefore, the solution saves 70% of power burnt by a single op-amp.

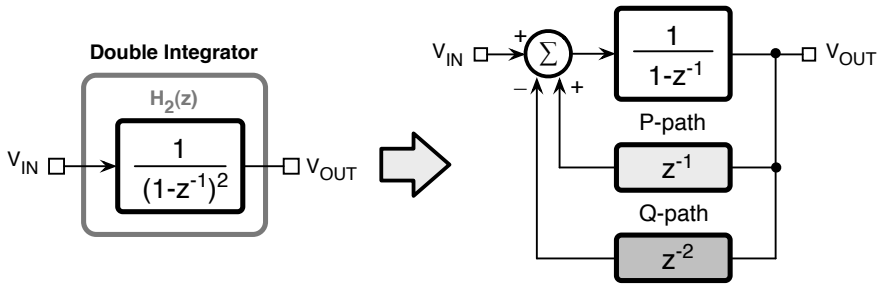


Figure 2.4: Double integrator block diagram.

2.2.2 Reduction of the Number of Comparators.

To further reduce power consumption, this design uses a second strategy for limiting the power of flash and, indirectly, the power of the second op-amp. The method is based on the observation that, for a given OSR, there is a good correlation between two successive flash input samples.

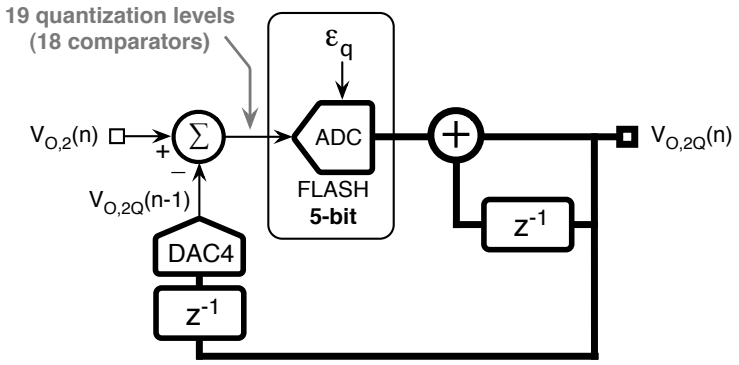


Figure 2.5: Five bit flash converter with reduced input range.

Moreover, with 5 bit, the quantization noise is low. Because of that, the output voltage increment of the second op-amp, equal to

$$\Delta V_{O,2} = [V_{in} z^{-1} + \epsilon_Q(-3z^{-1} + 3z^{-2} - z^{-3})](1 - z^{-1}) \tag{2.2}$$

turns to be lower than $V_{O,2}$ because the increase in the noise term is less than the reduction granted by $V_{in}(1 - z^{-1})$. The feature suggests the scheme of Fig. 2.5, that uses as input of the flash the difference between $V_{O,2}$ and its delayed and quantized version. Then, in the digital domain, the subtracted part is reestablished at the output of the modulator by a summing operation implemented, for example, with full adders.

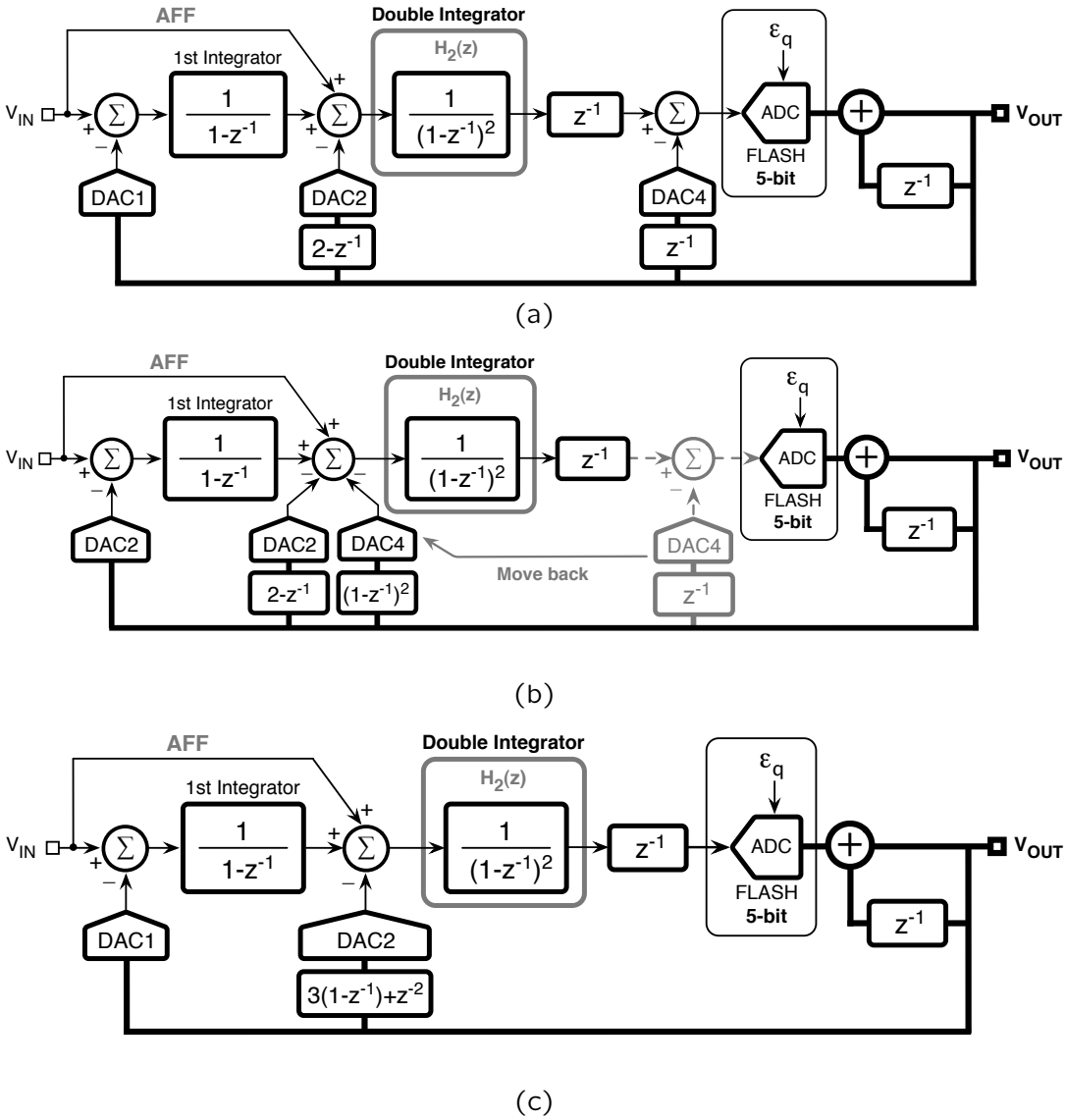


Figure 2.6: Topological modifications by considering the flash converter with reduced input range into the third-order modulator.

Since the input swing of the flash diminishes, comparators never used can be removed. For this design, the number of comparators goes down from 31 to 18. The power reduction in the flash is therefore 40%. The flash power reduction leads to the diagram of Fig. 2.6(a). Since the subtraction at the input of the flash converter would require an additional active block, this branch is moved back to the double integrator input multiplied by $(1-z^{-1})^2/z^{-1}$, as shown in Fig. 2.6(b). Combining the result with the existing $-(2-z^{-1})$ feedback, it results $-3(1-z^{-1})-z^{-2}$, see Fig. 2.6(c). However, since the flash output is already $V_{out}(1-z^{-1})$, its use avoids the $(1-z^{-1})$ multiplication in digital domain. The result is the final ΣΔ modulator of Fig. 2.7.

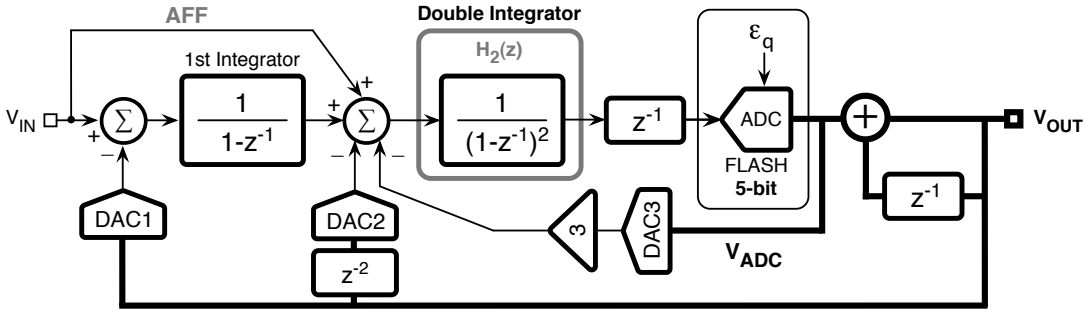


Figure 2.7: Final architecture of the third-order ΣΔ modulator.

2.3 Circuit Implementation of the ΣΔ Modulator.

The switched-capacitor (SC) integrated circuit used to implement Fig. 2.7 reduces by two times the multiplication of the quantized feedback. This is obtained by augmenting by 1.5 the DAC quantization step, made possible by a reduced dynamic range of the flash. As shown in Fig. 2.8, the circuit uses two hybrid capacitive-resistive DACs controlled by V_{ADC} (DAC3) and $z^{-2}V_{out}$ (DAC2). The resistive divider of both DACs uses 32 equal resistances of 200 Ω. The feedback DAC of the first integrator (DAC1) uses 18 resistances of 300 Ω and two terminations of 500 Ω. The use of distinct resistive dividers increases the power consumption, but avoids interferences. The cost, however, is only the 15% of the total. As depicted in the Fig. 2.8 the two analog signals of DAC2 and DAC3 is obtained with a unity capacitance (C_U). The DACs charges are injected during ϕ_2 to relieve the feedback factor at ϕ_1. The latch strobe occurs just before the end of ϕ_1 to allow flash and logic to drive the DAC during ϕ_2. For simplicity, the circuit shows a single-ended implementation.

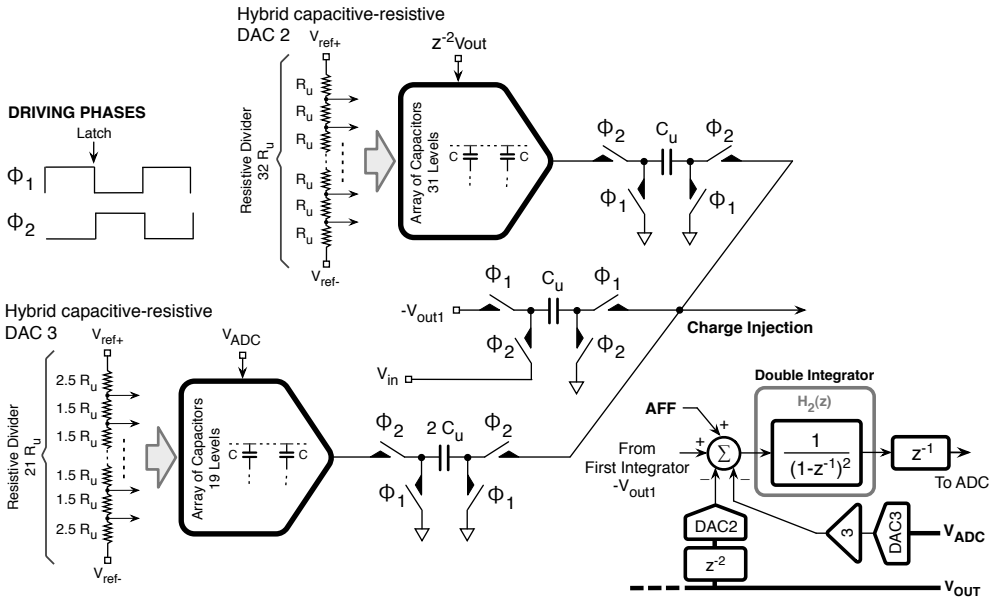


Figure 2.8: Input switched-capacitor network of the double integrator.

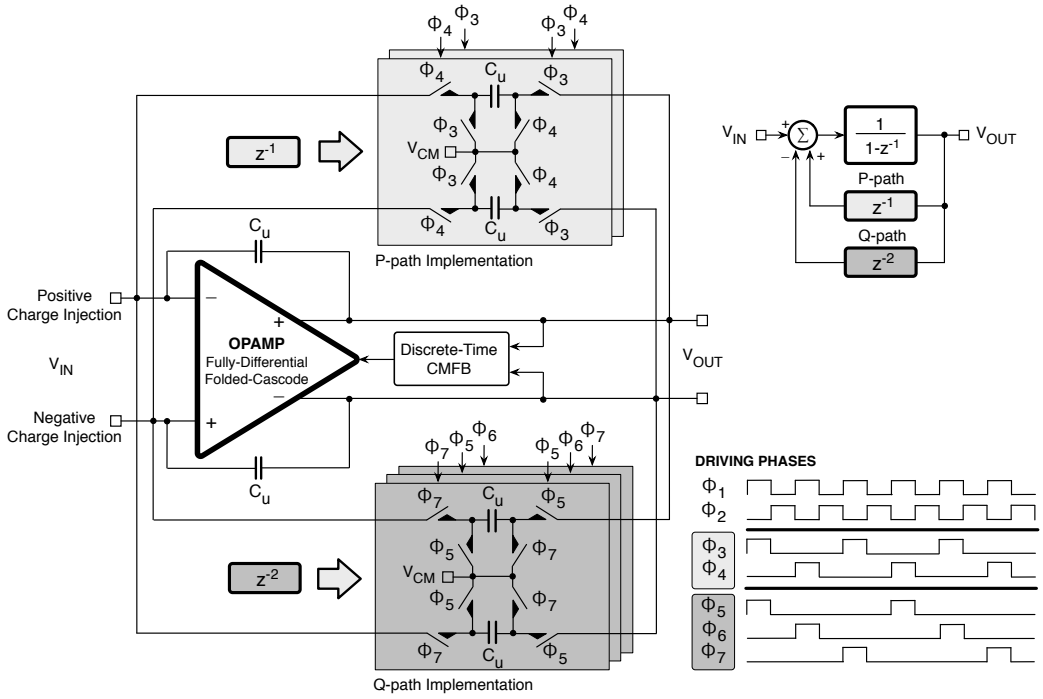


Figure 2.9: Switched-capacitor implementation of the double integrator and driving phases.

The double integrator requires the two feedbacks: *the P-path and Q path of Fig. 2.4*. Both inject during ϕ_1. Since the sampling of the second integrator output can be done at ϕ_1, because during ϕ_2 is available a new injection, the SC networks implementing the P-path and Q-path by using two and three unity capacitors, as shown in Fig. 2.9. In the same figure the driving phases are included. Input and integrator capacitors of the first integrator are both $80\ fF$ to limit the kT/C noise budget as specified by equation (1.10) in the previous chapter section 1.2. The value includes the parasitic of wire metal lines matched with a careful layout. The total voltage noise budget with $V_{FS} = 1\ V$ is about 220 μV, while $\sqrt{2kT/(C \cdot OSR)}$ gives 113.74 μV. The scheme of Fig. 2.9 is similar to the one proposed in [28] to realize double sampling, however, this technique is not used in this design.

The two operational amplifiers are fully differential folded cascode with discrete-time common mode feedback (DTCMFB) [44]. The schematic diagram of the architecture is shown in Fig. 2.10.

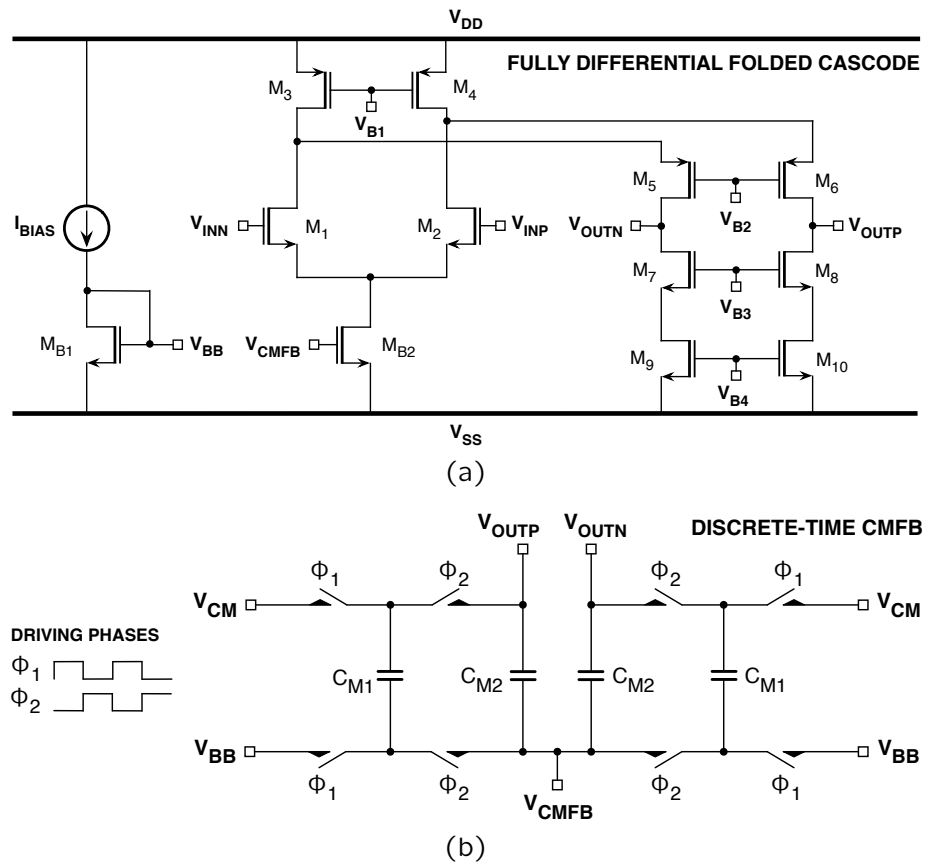


Figure 2.10: Operational Amplifier. (a) Fully differential folded cascode architecture. (b) Discrete-time common mode feedback (DTCMFB).

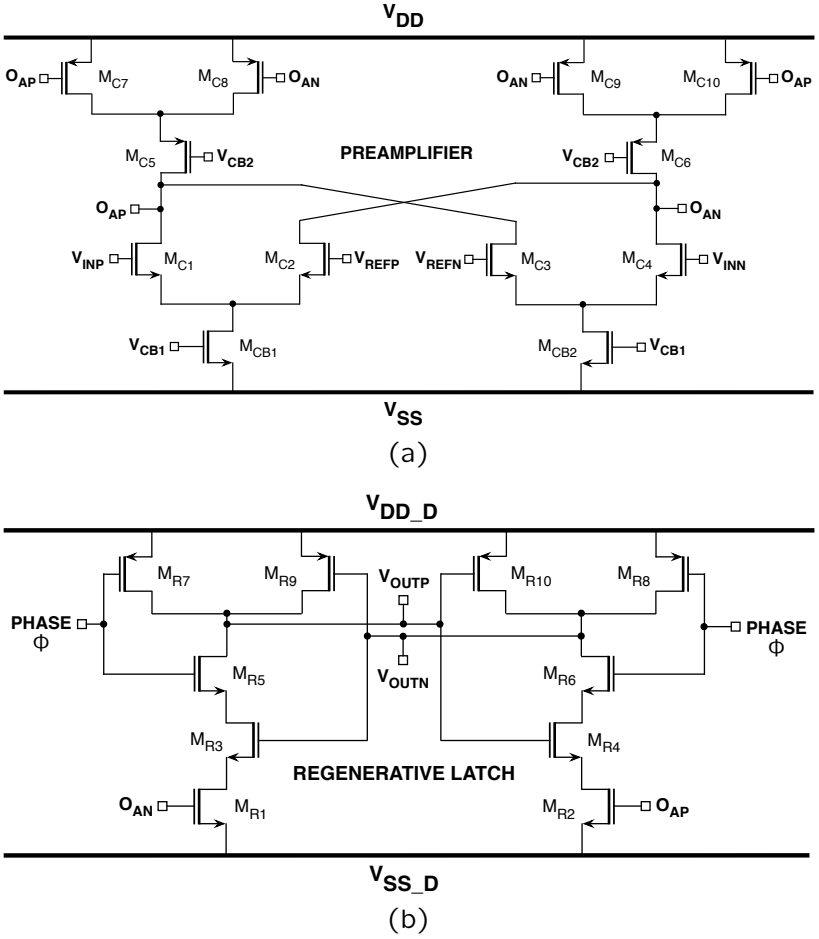


Figure 2.11: Schematic diagram of the comparator. (a) Preamplifier. (b) Regenerative latch.

Fig. 2.11 shows the schematic of the voltage comparator [45], [46]. It is a two stage fully differential scheme with a preamplifier with gain 9.3 dB, continuous time common mode feedback (CTCMFB) and regenerative latch. The dimension of all transistors are depicted in the figure. The response time of the comparator is about 2 ns with 2 mV at input. The bias current of the preamplifier is 25 μA. The preamplifier is used to moderately increase the signal and, much more important, to limit the kick-back from the latch.

2.4 Simulation and Measurement Results.

The effectiveness of the architecture has been verified with Matlab-Simulink^{TM} by using the behavioral models reported in [47]. The simulated swing reduction at the input of the flash

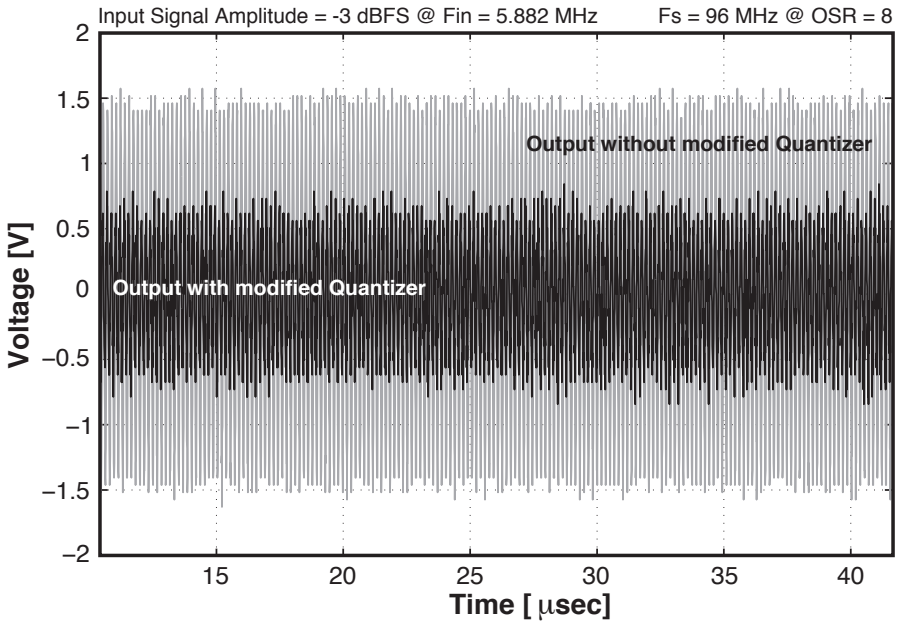


Figure 2.12: Output dynamic range of the double integrator.

converter decreases the number of required comparators from 31 to 18 but, also, relaxes the op-amp specifications, namely, linearity and slew-rate. Fig. 2.12 shows the comparison of the output dynamic range in the double integrator with and without use of the architecture described in Fig. 2.5. The MATLAB simulation was made by considering an input amplitude of -3dB$_{FS}$ and an input signal frequency very close to the Nyquist rate.

The third-order ΣΔ modulator has been implemented at transistor level with CADENCE by using a 0.18 μm, double poly, 5 metal levels CMOS technology. The op-amps use different bias currents to meet the DC gain, slew-rate and bandwidth requirements as summarized in Table 2.1. The nominal power supply of the modulator is 1.8 V.

Table 2.1: Performance of the Operational Amplifiers

0.18 μm, double poly, 5 metal levels CMOS technology, 1.8 V supply voltage

Parameter	Symbol [Unit]	First Integrator	Double Integrator
Bias Current	I_{BIAS} [mA]	1.055	1.33
DC Gain	Av [dB]	51	48
Slew-Rate	SR [V/μs]	300	400
Unity Frequency	GBW [MHz]	580	890
Phase Margin	Φ_M [Degree]	60	61

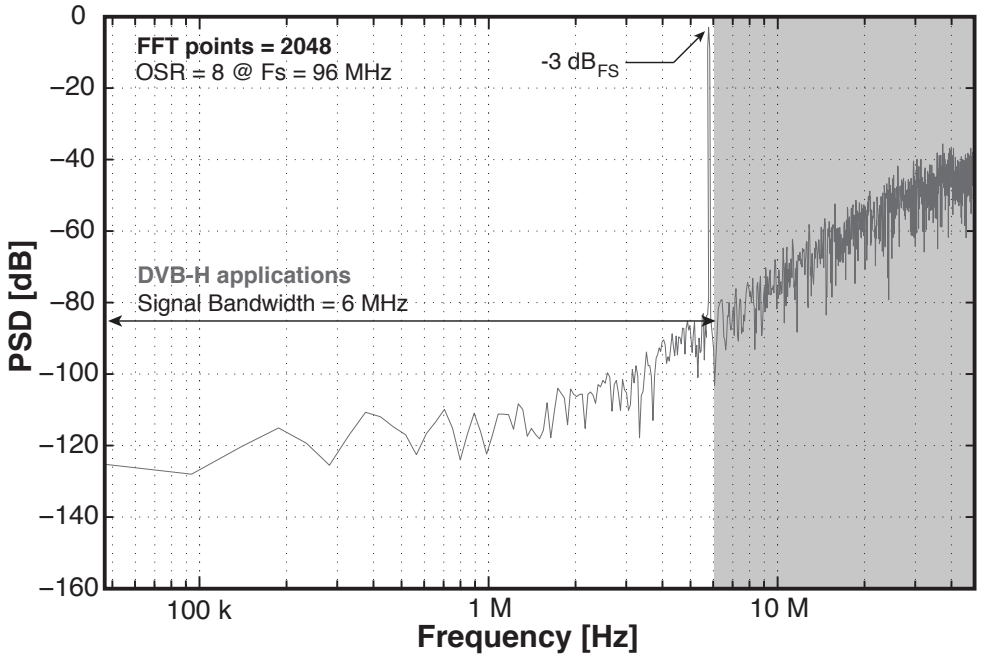


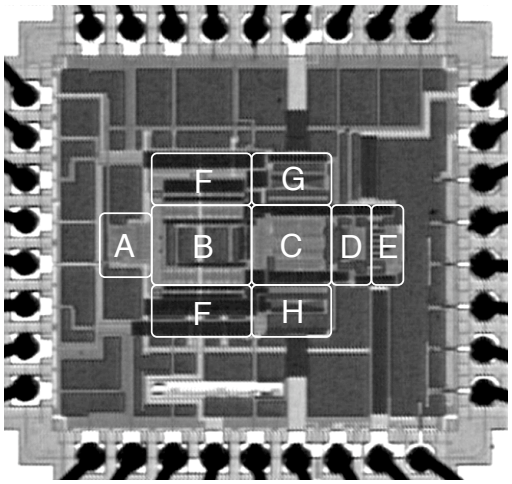
Figure 2.13: Simulated power spectral density of the modulator. Transistor level implementation.

The simulated third-order power spectral density is shown in Fig. 2.13. The expected SNR with a -3 dB$_{FS}$ input signal is 65 dB, which corresponds to 10.5 bits. The frequency of the input tone is 5.65 MHz approximately.

The $\Sigma\Delta$ modulator has been integrated in a 40 pins LLP package. Fig. 2.14 shows the die microphotograph where the main circuital blocks are highlighted. The chip active area is 0.32 mm^2. Reference voltages are external and no internal buffers enforces the strength of references. However, multiple bonding for references moderates the effects of bonding inductances.

Fig. 2.15 shows the measured power spectral density of the modulator with a sampling frequency of 96 MHz and 767 kHz input signal frequency. Noise integrated over a 6 MHz band (OSR = 8) yields an SNDR of 60.7 dB, corresponding to 9.8 bit. The spectrum shows second and third harmonic tones at -88 and -77 dB$_{FS}$, respectively. A small mismatch in the input differential signals causes the second harmonic tone. Non-linearity of the circuit gives rise to third order harmonic.

The floor of the spectrum (larger than the expected kT/C noise) shows in the signal band, above 2 MHz, a first order shaped noise term. It is likely a white noise injected at the input of the double integrator, first order shaped by the architecture. The source is likely associ-



0.18 µm CMOS Tecnology
Dual Poly and 5 Metal Levels

Active Area:	0.32 mm^2
Package:	40 pins LLP
Supply Voltage:	1.8 V

A: Clock Generator
B: First and Double Integrator
C: Flash Converter
D: DAC-1
E: Digital Logic
F: Switched-Capacitors
G: DAC-2
H: DAC-3

Figure 2.14: Chip microphotograph.

ated to the reference voltage of the DACs. The switching load and the bonding inductance cause small ringing that does not extinguish at the sampling times. The problem diminishes with lower clock frequencies, as verified by the measurements summarized in Fig. 2.16. The

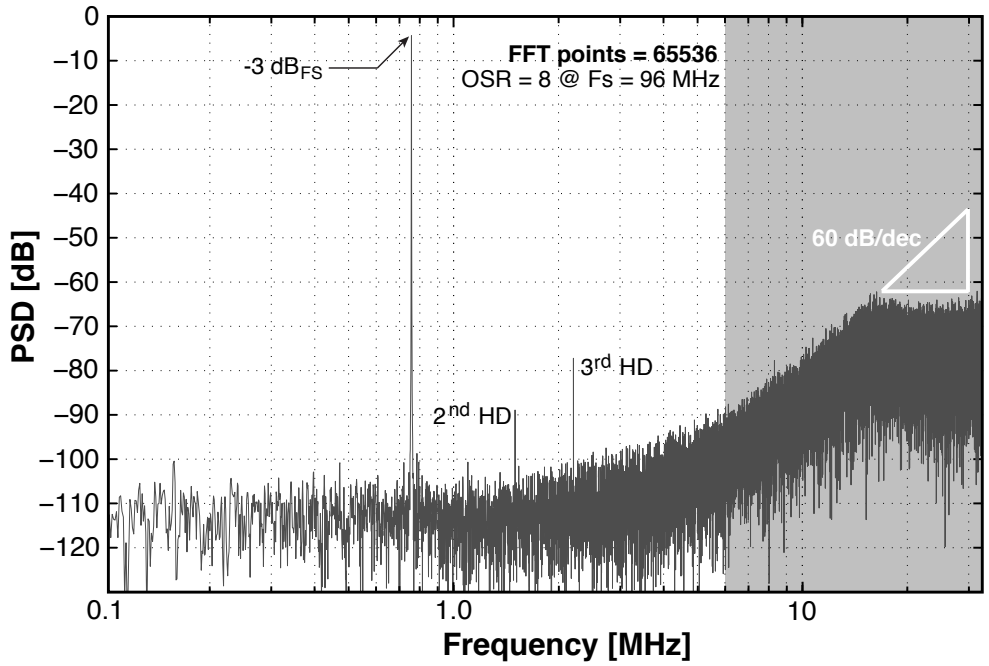


Figure 2.15: Measured power spectral density of the ΣΔ modulator.

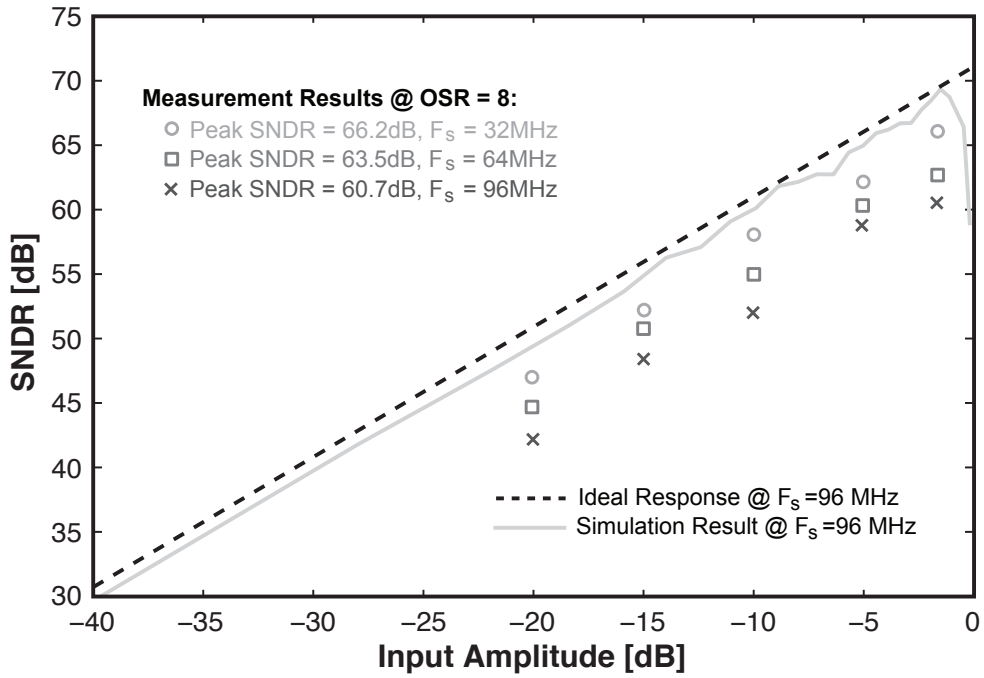


Figure 2.16: SNDR versus input signal amplitude.

SNDR versus input amplitude at low clock frequencies improves and the extra shaped noise disappears. The dashed and solid lines correspond to an ideal and a behavioral simulated result. The measured figures indicate a loss of about 10 dB at full clock speed (F_S = 96 MHz).

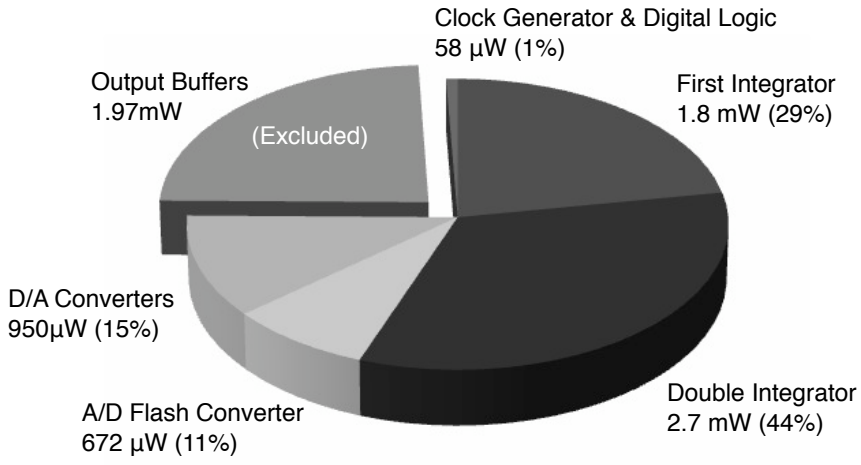


Figure 2.17: Power consumption breakdown of the third-order $\Sigma\Delta$ modulator.

The total power consumption of the modulator sampled at 96 MHz is 6.18 mW (excluding the output buffers). A more detailed power breakdown is illustrated in Fig. 2.17. The achieved Figure of Merit (FoM) defined by

$$FoM = \frac{P_{TOT}}{2^{ENoB} 2BW} \tag{2.3}$$

(where P_{TOT} is the consumed power, $ENoB$ the effective number of bits, and BW is signal bandwidth) is 0.58 pJ/conversion. Table 2.2 summarizes and compares performance of previously reported low-pass sigma-delta modulators, [28], [48]-[51]. The FoM of reference [28] is better than this design being optimized for a 2 MHz signal band.

Table 2.2: Comparison with other State-of-Art ΣΔ Modulators

Feature	Unit	This Work	ISSCC '05 [28]	JSSC '05 [48]	CICC '09 [50]	JSSC '09 [51]	VLSI '09 [49]
CMOS technology	nm	180	90	250	130	180	180
Supply Voltage	V	1.8	1.2	1.2	1.2	1.2	1.8
Oversampling Ratio	OSR	8	9.89	16	48	16	50
Signal Amplitude	dB_{FS}	-3	-3	-4	-6	-1.5	-5
Signal Bandwidth	MHz	6	1.94	1.25	1.92	0.625	1.0
Peak SNDR	dB	60.7	63	89	59	74.6	56.8
ENoB	Bit	9.81	10.18	14.5	9.52	12.1	9.15
Active Area	mm^2	0.32	0.26	8.6	0.36	1.92	1.62
Power Consumption	mW	6.18	1.2	44	3.1	3.2	22.2
Figure of Merit	pJ/conv-level	0.58	0.27	0.76	0.788	0.58	19.6

Chapter 3

A Low-Power Single Op-amp Third-Order $\Sigma\Delta$ Modulator

In this chapter a low-power $\Sigma\Delta$ modulator suitable for high-resolution low power sensor systems is described. It achieves a third-order noise shaping performance with a single operational amplifier. A slew-rate boosting technique enables minimum power consumption in a two stages op-amp. Realized in a 0.18 μm standard CMOS technology, the modulator provides 84 dB SNDR and 88 dB dynamic range in a signal bandwidth of 100 kHz. It dissipates 140 μW with a 1.5 V power supply. The state-of-the-art power efficiency gives a remarkable Figure of Merit (FoM) of 54 fJ/conversion-level, verifying the effectiveness of the proposed modulator architecture.

3.1 Design Specifications for Low-Power Sensor Systems.

Recent advances in micro-electro-mechanical systems (MEMS) technology, wireless communications, and digital electronics have enabled the development of low-cost, low-power, multifunctional sensor nodes that are small in size and communicate untethered in short distances [52]. These tiny sensor nodes, are capable of self organizing into a collaborative network, and subsequently benefit from spatial diversity through data sharing and multi-hop

connectivity. For its wide variety of applications ranging from habitat monitoring to medical diagnose [53], sensor networks have transformed the way as society interacts with the physical world. Besides, it is possible to expand the above classification with more categories such military surveillance [54], chemical processing [55], reconnaissance [56], and damage assessment to environmental forest fire detection [57]. This kind of applications however, always require high-accuracy (at least 12-13 bit), low signal bandwidth (typically 100 Hz-150 kHz) and extremely low power consumption (less than 200 μW) to improve battery life.

Fundamentally, the architecture of an intelligent sensor node consists of an analog-to-digital converter (ADC), a digital signal processing, and a short range radio. Furthermore, to allow large sensors array integration, ADCs must occupy small silicon area.

Successive-approximation-register analog-to-digital converter (SAR ADC) are well suitable topology to meet the above demanding requirements. The architecture exhibits moderate speed, moderate resolution and very low power consumption characteristics [58], [59], [60]. However, emerging design techniques on $\Sigma\Delta$ modulators have been published for applications where low power dissipation is required [1]-[6]. Furthermore, $\Sigma\Delta$ architectures typically used in telecommunications applications such as audio signal processing, exploit, as known, oversampling and noise shaping to accomplish high resolution. The reduction of the amplifiers output swing bring down the modulator power consumption and ensures a reduction in the harmonic distortion. Another relevant feature that benefits the consumed power is the minimization of the number of op-amps in the architecture. This can be obtained with topological modifications [27] or, as it will be shown shortly, by using a single operational amplifier working in a multiplexed operation [21], [22] for realizing high-order transfer functions.

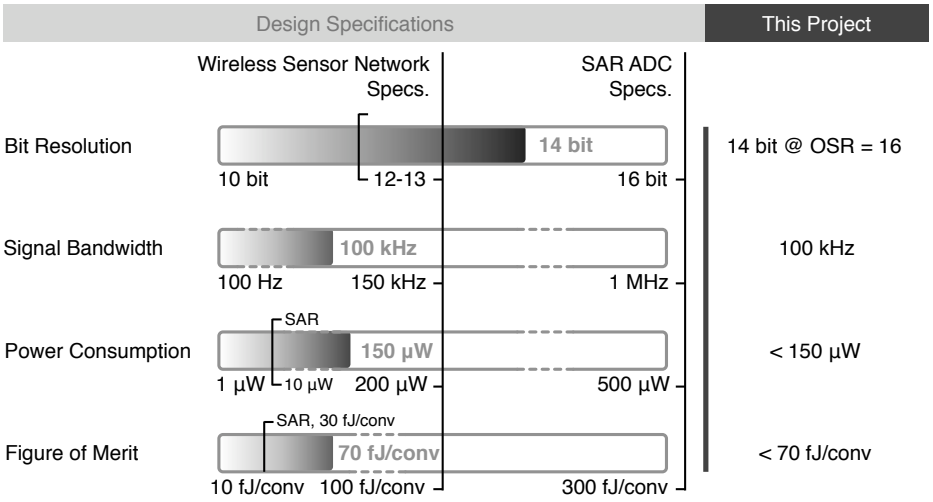


Figure 3.1: Wireless sensor networks, SARs A/D converter and project specifications.

The above design considerations, make of the $\Sigma\Delta$ topologies, an alternative solution for applications where the low speed and medium resolution are not difficult, but the required low power level is a challenging issue.

Fig. 3.1 summarizes the required specifications for wireless sensor network applications. The performance of the SAR A/D converter is also outlined in the figure. The proposed third-order modulator addresses these low power requirements since its power consumption is less than 200 μW and the expected resolution is more than 12 bits.

3.2 Proposed Third-Order $\Sigma\Delta$ Modulator.

The architecture for the proposed third-order $\Sigma\Delta$ modulator is conceptually shown in Fig. 3.2. The scheme uses a second-order modulator with two delayed integrators and the noise enhancer block with transfer function H(z). As shown in Fig. 3.2, the suitable injection of shaped quantization noise, ϵ_q, at the input of the second integrator of the $\Sigma\Delta$ scheme, boost the noise shaping performance to third order.

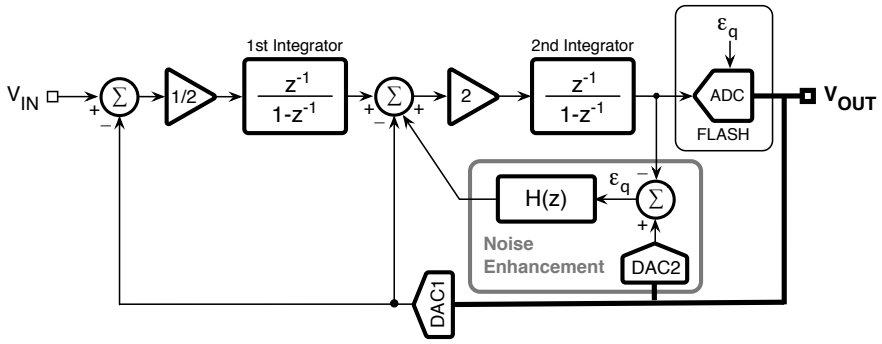


Figure 3.2: Enhancement of the NTF in a conventional second-order $\Sigma\Delta$ modulator.

The noise shaping of a second and third-order $\Sigma\Delta$ modulators are, respectively

$$\epsilon_q(1-z^{-1})^2 = \epsilon_q(1-2z^{-1}+z^{-2}) \tag{3.1}$$

$$\epsilon_q(1-z^{-1})^3 = \epsilon_q(1-3z^{-1}+3z^{-2}-z^{-3}) \tag{3.2}$$

where once again ϵ_q is the quantization error.

The subtraction between (3.1) and (3.2) gives

$$\epsilon_q(-z^{-1}+2z^{-2}-z^{-3}) = -z^{-1}\epsilon_q(1-z^{-1})(1-z^{-1}) \tag{3.3}$$

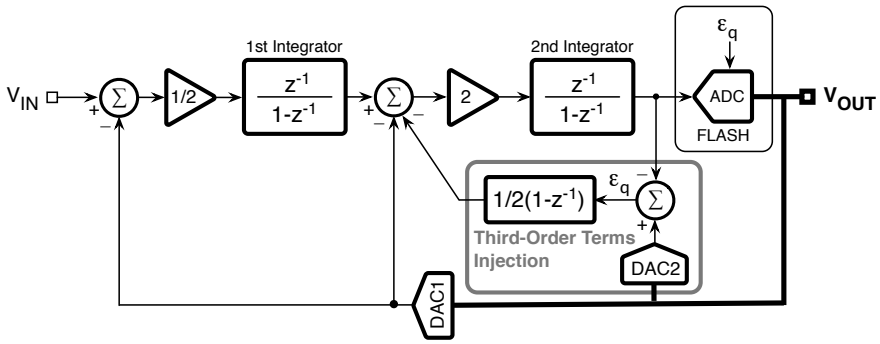


Figure 3.3: Second-order ΣΔ modulator with the block function H(z).

which rearranged yields

$$\epsilon_q[\underbrace{2z^{-1}(1-z^{-1})}_{\text{STF}_2}\underbrace{(-(1-z^{-1})/2)}_{\text{H(z)}}] \tag{3.4}$$

Equation (3.4) shows the two factors needed to obtain the desired third-order noise shaping. The transfer function from the second integrator input is highlighted with STF_2. Therefore, the missing term is $H(z) = -(1-z^{-1})/2$ injected into the second integrator input. This result suggest the architecture of Fig. 3.3 which by inspection leads now

$$V_{OUT} = V_{IN} \cdot STF(z) + \epsilon_q \cdot NTF(z) = V_{IN} \cdot z^{-2} + \epsilon_q \cdot (1-z^{-1}) \cdot (1-z^{-1})^2 \tag{3.5}$$

Notice that the signal transfer function shows a double delay while the noise transfer function has a third-order noise shaping.

The enhancement operation does not require active blocks because the subtraction of analog and quantized signal is done with two separate paths, as shown in Fig. 3.4.

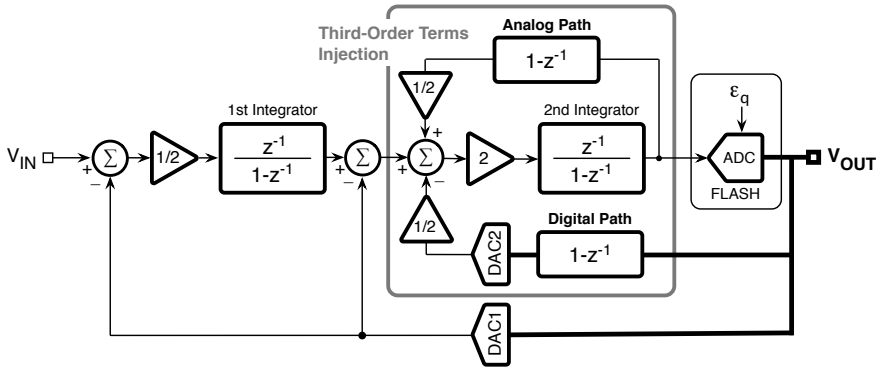


Figure 3.4: Proposed third-order ΣΔ modulator scheme.

3.2.1 Output Swing Reduction of the Integrators.

The proposed modulator of Fig. 3.4 uses, like the previous modulator described in Chapter 2, the same techniques to reduce the output swing in both integrators. As shown in Fig. 3.5, the analog feedforward path (AFF) is used to limit the output swing of the first integrator. The correlation between successive output samples enables a reduction of the second integrator swing (see Fig. 2.5, Chapter 2), from $V_2(nT)$ to $V_2(nT)-1/2\cdot V_{DAC3}(nT-T)$. A lower V_2 moderates the power of the op-amp and limits to 18 the number of comparators used by the flash. The gain by two of the second integrator, transferred to the flash converter, compensates the 1/2 feedback factor of the analog path and reduces the swing of the op-amp at expenses of higher flash sensitivity. A 5 bit flash converter makes relatively low the quantization error and gives robustness to the loop.

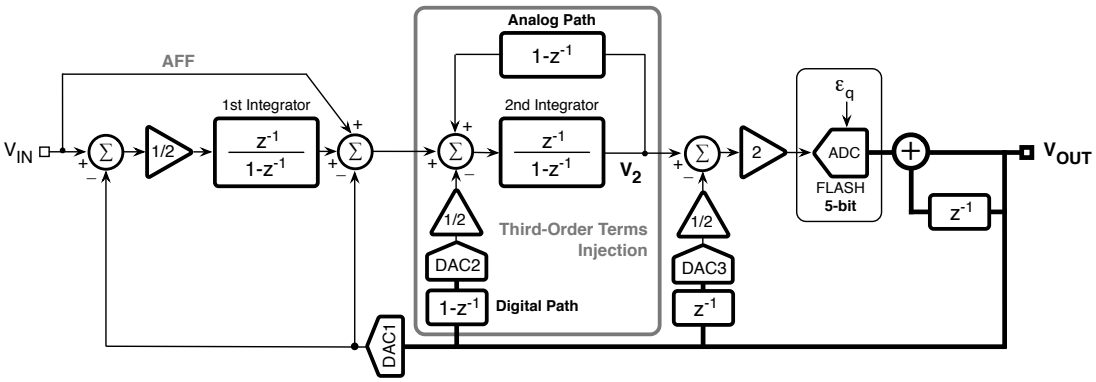


Figure 3.5: ΣΔ modulator with analog feedforward path and flash converter with reduced input range.

Suitable topological modifications, as shown in Fig. 3.6(a), saves the active sum at the input of the flash converter. This point is moved back to the input of the second integrator and multiplied by the function $(1-z^{-1})^2/z^{-1}$, which is given by the inverse of the transfer function of both second integrator and analog path.

The digital processing combination of DAC2 and DAC3 yields

$$E(z) = -1/2\cdot(1-z^{-1}) - 1/2\cdot(1-z^{-1})^2 = 3/2z^{-1} - 1/2z^{-2} - 1 \tag{3.6}$$

which rewritten leads

$$E(z) = (1-z^{-1})\cdot(1/2z^{-1}-1) \tag{3.7}$$

Equation (3.7) enables the architecture of Fig. 3.6(b). A simple processing in the digital domain, after the A/D conversion, builds the quantized output as the addition of the output

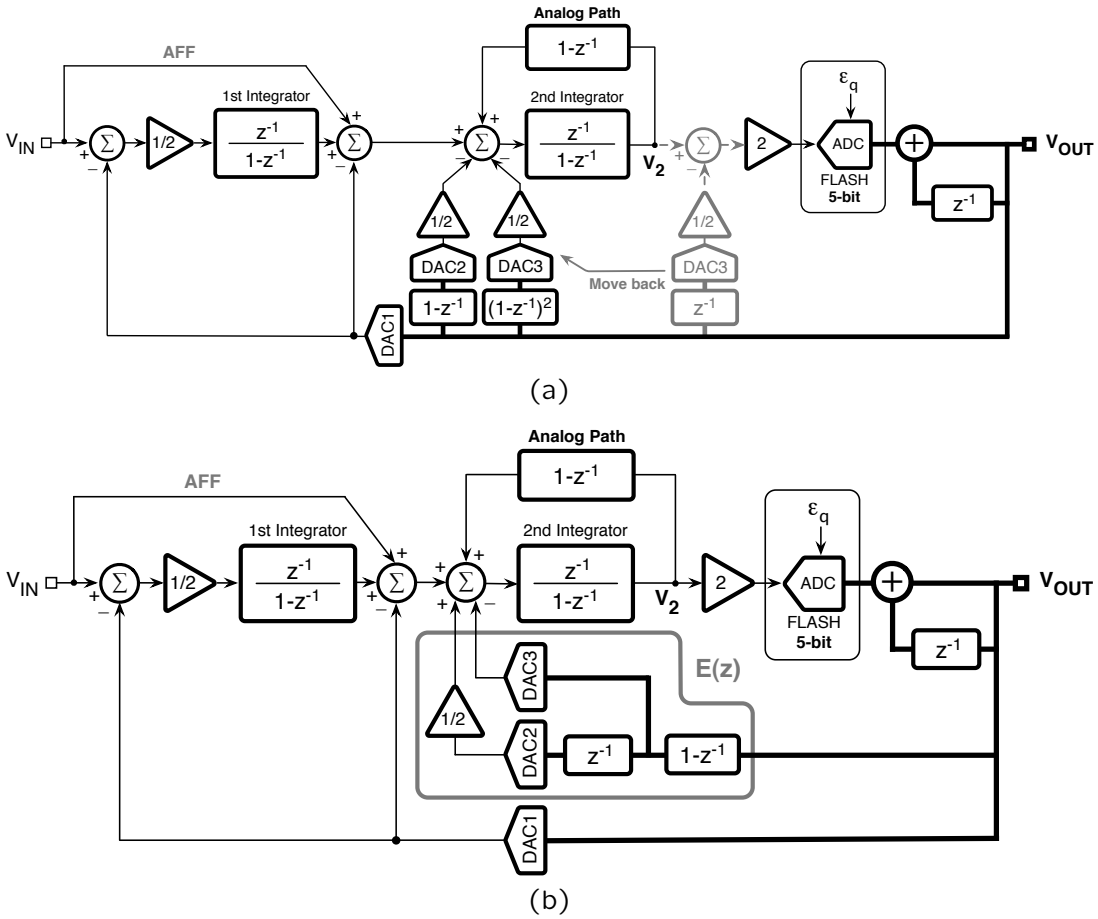


Figure 3.6: Topological modification. (a) Active sum at the input of the flash converter is eliminated. (b) Digital processing combination of DAC2 and DAC3.

of the flash and the previous digital output. This operation is properly used to compensate the digital factor $(1 - z^{-1})$ in the block function E(z). The final result is the third-order $\Sigma\Delta$ architecture of Fig. 3.7, where the conversion of DAC2 and DAC3 are realized from the output of the flash converter and injected at the input of the second integrator.

The three DACs of the modulator are implemented with a single Kelvin divider to generate the differential 5 bit references voltages. This feature, as will be described with more detail in the following section, completely cancels the error caused by gradient in the resistance values. The resistor sizes and the layout of the resistive DAC limit high order distortion terms without the need of digital calibration or dynamic matching of elements (DEM).

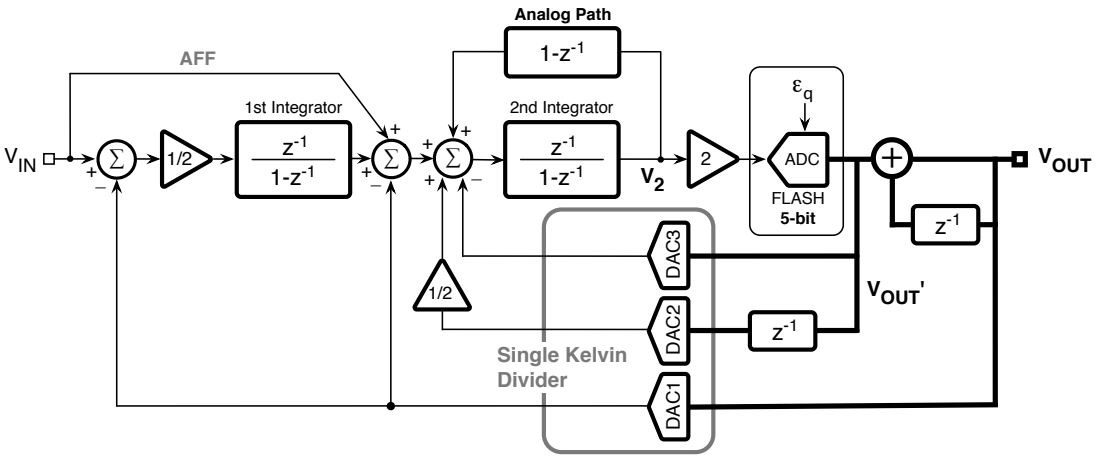


Figure 3.7: Proposed third-order ΣΔ modulator.

3.3 Circuit Implementation of the ΣΔ Architecture.

Minimum power consumption is one of the main targets addressed in this project. Since a third-order ΣΔ modulator can be implemented with two operational amplifiers, the architecture of Fig. 3.7 works with only one operating in a multiplexed fashion [21], [22]. The general time event for the modulator is shown in Fig. 3.8. Two phases with the same duty cycle are required. The first integration is realized during phase one. The second integration, the injection of the $(1 - z^{-1})$ term, the input feedforwarding and the conversion of DAC2 and DAC3 take place during phase two.

Fig. 3.9 illustrates the schematic diagram of the ΣΔ modulator fully differential sampled data implementation. The single operational amplifier serves the first integrator during phase 1. During the complementary phase the op-amp and the additional connected networks operate as second integrator.Fig. 3.9 also reports the phases scheme used to control switches. The first integrator uses $10C_U$ for the input capacitor and $20C_U$ for the feedback capacitor. For limiting the kT/C noise, the unity capacitance, C_U, is equal to 80 fF. The second integrator uses a unity capacitance for the 1/2 z^{-1} path that comes from conversion of DAC2, and two unity capacitances for the other branches, namely feedforward and analog path respectively. The use of feedback capacitors with significant different values is not problematic because the operational amplifier can drive the largest value.

The path feeding back the analog part of the quantization error needs two analog delays. They enables the time multiplexing operation of the op-amp. The first of them uses two switched-capacitor (SC) structures controlled by phases Φ_{1a} and Φ_{1b} operating in a ping-pong fashion. As shown in Fig. 3.9 while the first SC structure sampling the circuit output, $V_{OUT}(n)$, the other transfers the past sampled output, $V_{OUT}(n-1)$, to the integrating capacitor $2C_U$.

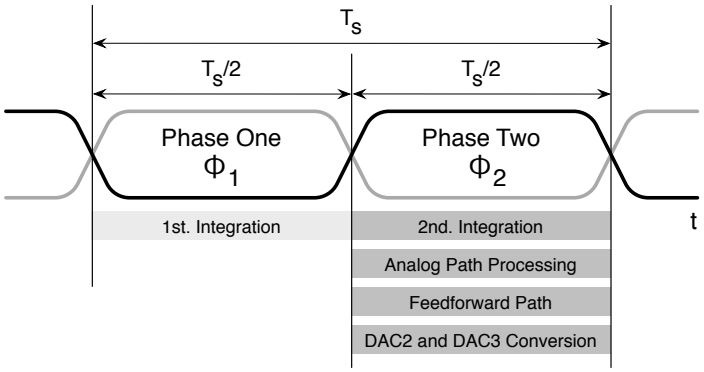


Figure 3.8: General time event of the proposed third-order ΣΔ modulator.

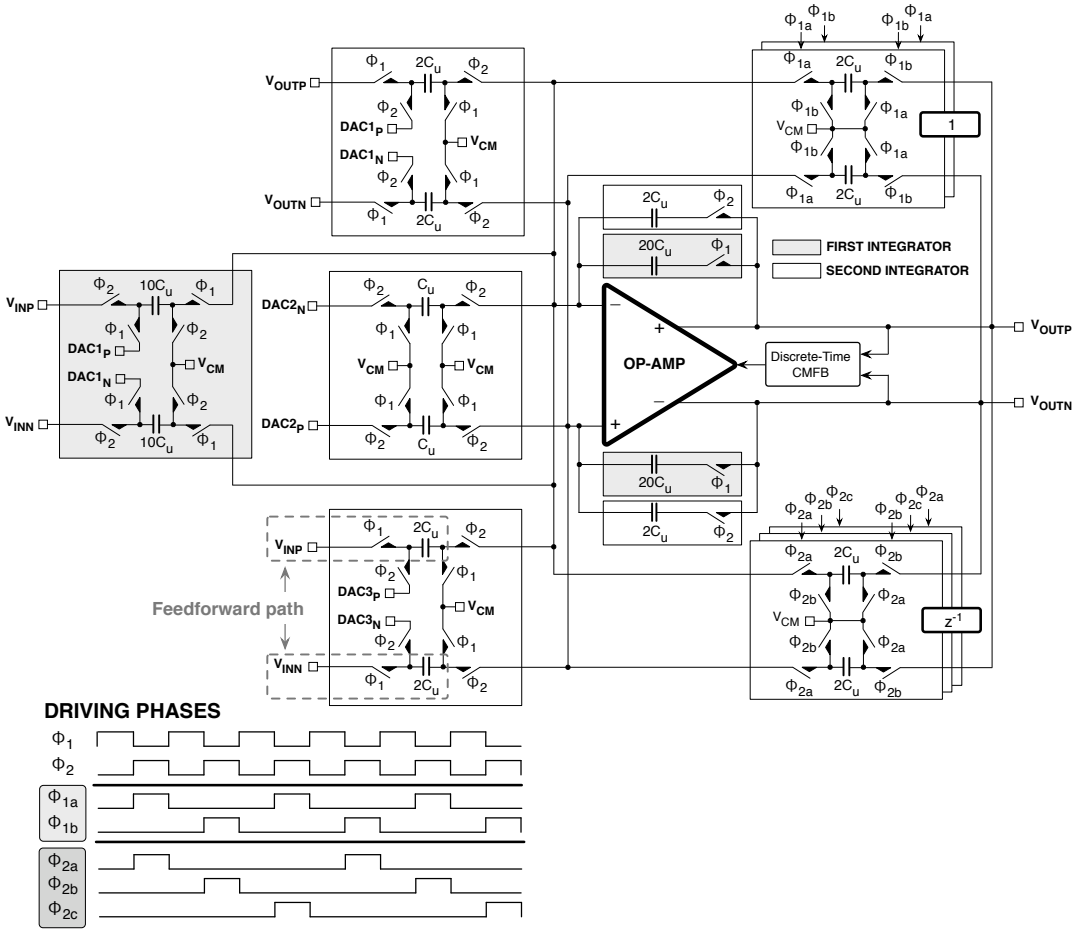


Figure 3.9: Fully differential sampled data implementation of the modulator.

In a similar way three SC structures that work under the control of phases Φ_{2a}, Φ_{2b} and Φ_{2c} realize the required z^{-1} delay of the analog path. These structures alternatively implement the sampling, holding and integrating functions.

Conventional ΣΔ modulators use capacitive based DACs with, when necessary, dynamic elements matching (DEM) [19], [20]. The use of calibration or DEM depends on the requested accuracy of unity elements that, as well know, improves with the area. Moreover, for high-resolution targets, it is often necessary to over design the unity capacitor well above the value required by the kT/C noise limit. In turn, large capacitances involve high power. On the contrary, It can be convenient using a resistive based DACs because enlarging the unity value of resistance does not affect the power consumption and does not limit the speed of operation. Matching improves, but an error caused by the gradient of the resistive properties of the divider occurs [11]. However, the use of the same resistive string to generate differential voltages cancels the gradient error at the first order.

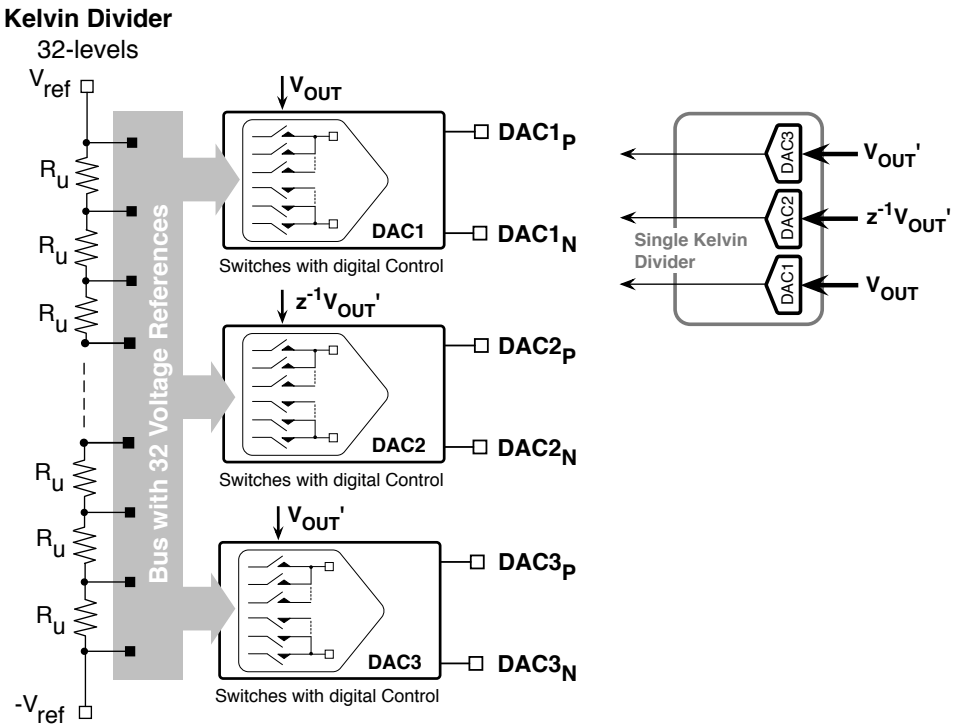


Figure 3.10: Single Kelvin divider to implement three DACs of Fig. 3.7.

This design exploits a simple property of a linear string of resistors to avoid the gradient error. Supposing that the value of the generic k-th resistor is $R_k = R_u + k\delta_R$, the differential voltage becomes

$$V_{diff} = V_{ref} \frac{(N-i)R_u + \delta_R(N-i)(N-i+1) - iR_u + \delta_R i(i+1)}{NR_u + \delta_R N(N+1)} \tag{3.8}$$

that is independent on δ_R. Therefore, it is possible using a linear string of resistors with area that satisfies the matching requirements without caring about gradient limits.

Fig. 3.10 shows a single resistive divider, with 31 equal resistances of 2.2 kΩ, used to implement the three DACs of Fig. 3.7. The Kelvin division generates the 32 reference voltages across the V_{ref} to -V_{ref} range. The digital signals V_{OUT}, $z^{-1}V_{OUT}^{'}$, and $V_{OUT}^{'}$ control the three selection networks to obtain the DACs differential outputs. The digital control is done in one-out-of-N code. The used unity resistors have area equal to 250 μm^2, a large but affordable value. The solution also allows the use of 5 bit in the flash, an unpractical value for DEM techniques. The expected matching is 0.01 $\%$, leading to harmonic distortion of more than 86 dB without calibration.

Fig. 3.11 shows the conceptual block diagram of the main circuits used for the analog-to-digital conversion in the modulator. The flash converter employs 18 comparators thanks to the second integrator output swing reduction. Two extra comparators (not showed in the figure) detect possible overload and activate a reset of the two integrators. This also avoids possible problems at the start-up. The encoder circuit converts the thermometer code of the flash to one-out-of-N code and removes possible bubble errors [45], [61]. The digital bus of the encoder, V_{OUT}', drives the selection networks of DAC2 and DAC3 of the Kelvin divider DAC and serves the digital code to a matrix array used to implement the digital summing block at the output of the modulator (see Fig. 3.11). The result of the summing matrix operation gives the code for control the selection network of DAC1. The matrix array ensures a very fast operation and benefits the power consumption, however, adds layout complexity and increases the area.

Fig. 3.12 shows a detailed implementation of the matrix array. To ensure the 32 levels of the one-out-of-N code, resulting of the summing operation, an array of 32x32 switches is used. The one-out-of-N code of the encoder output is denoted in the decimal range from -9 to 9. The output code of the modulator and its delayed version are both represented from -16 to 15 range. As shown in Fig. 3.12, the output V_{OUT}' controls only one terminal of 18 levels of switches, the resting levels are connected to ground. The other available terminal enables the output of the modulator, V_{OUT}, while the delayed version of this output is fed back to the input of the matrix itself for control the gate of the switches. Since the one-out-of-N code establishes the active bit but the others only one switch is activated during the summing operation between V_{OUT}' and $z^{-1} \cdot V_{OUT}$. Fig. 3.12 shows an example of the addition between 3 (from V_{OUT}') and 9 (from $z^{-1} \cdot V_{OUT}$) decimal values. The expected result is 12 at the output of the modulator.

Fig. 3.13 shows the complete schematic diagram of the comparator used in the flash con-

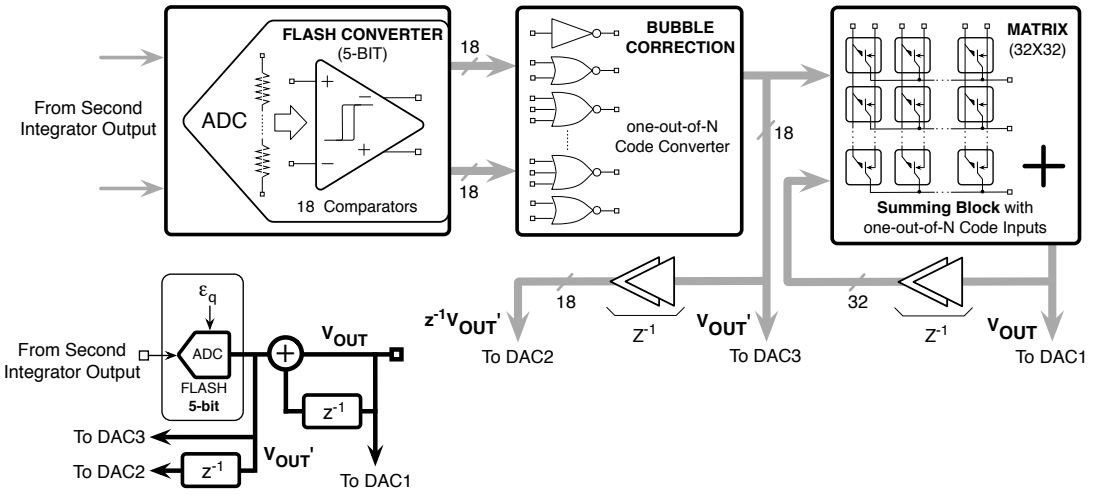


Figure 3.11: Conceptual block diagram of the analog-to-digital conversion in the proposed modulator.

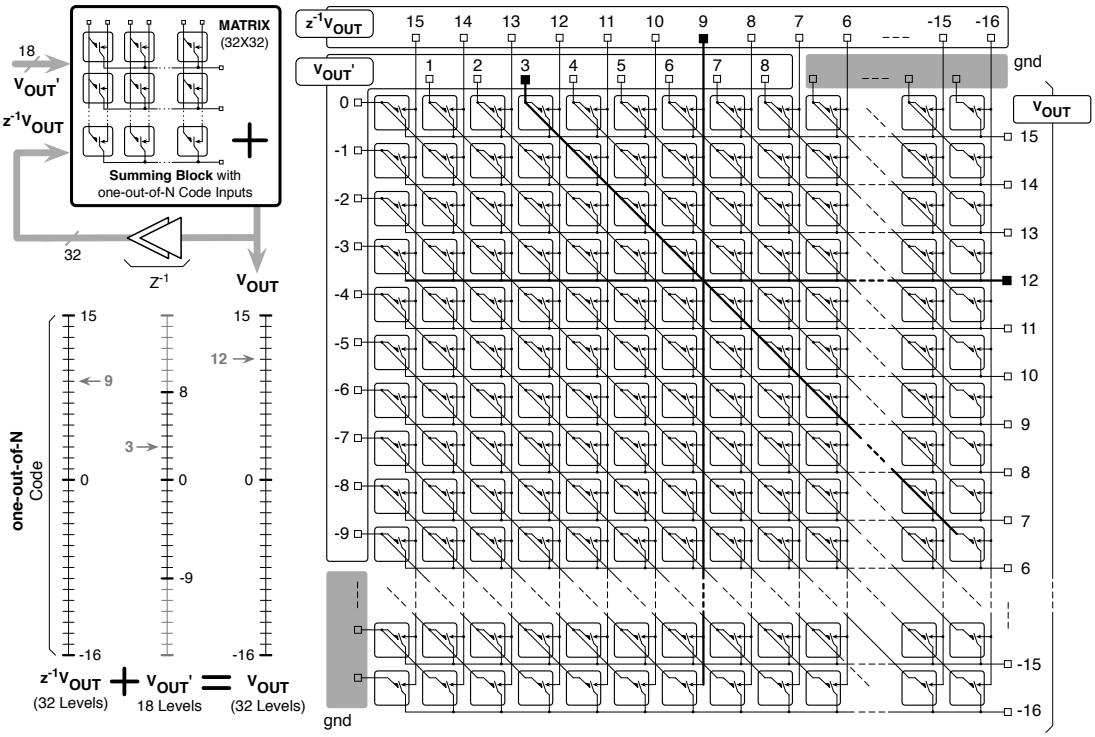


Figure 3.12: Detailed description of the matrix array implementation.

verter [45], [62]. A reset switch M_{SW} is connected between the two output nodes of the preamplifier circuit, as shown in Fig. 3.13(a). This switch enables high-speed operation and avoids the use of common mode feedback. During the reset phase (Φ is low) the reset switch turned on, the differential output follows the differential input and the residual voltage from the previous decision is erased. When Φ goes high the regeneration phase starts, thus the reset switch is opened and transistors M_{R5}, M_{R9} and M_{R6}, M_{R10} form two back-to-back CMOS inverters that generate the small output voltage, found in the beginning of this phase, to full-scale digital levels. The comparator is designed for to have, in the reset phase, an output voltage that is interpreted as the high logic value.

The latch structure of Fig. 3.13(b) is similar to the one used in the previous modulator (see

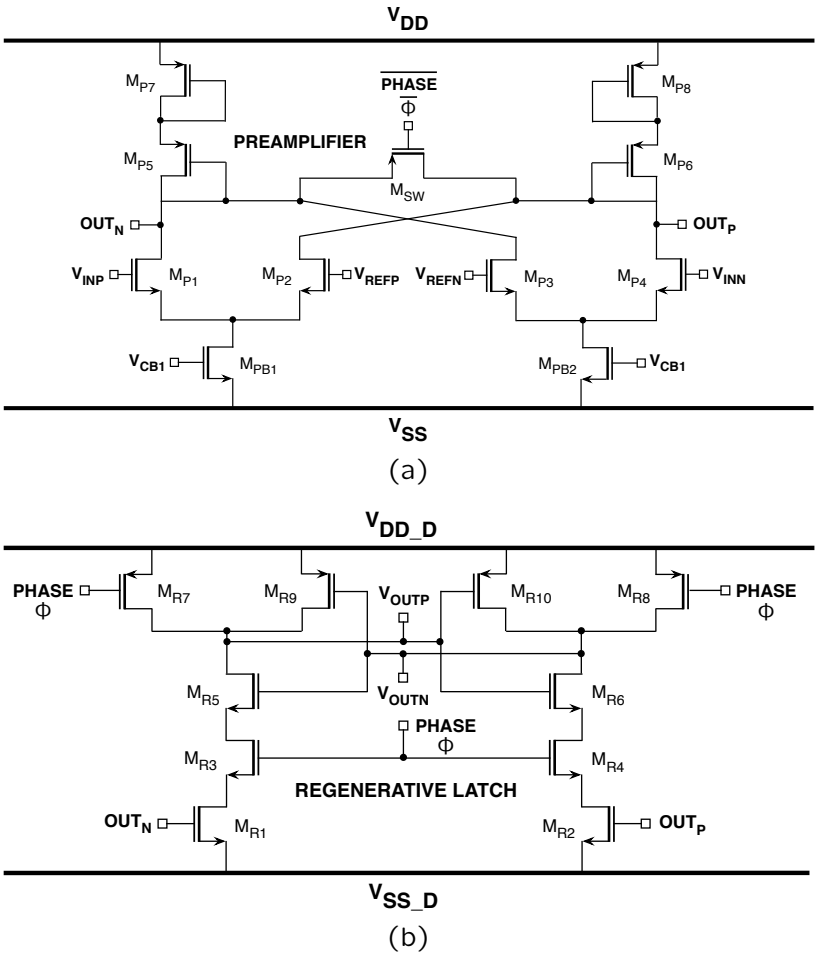


Figure 3.13: Schematic diagram of the comparator. (a) Preamplifier circuit with a reset switch. (b) Regenerative latch circuit.

Fig. 2.11(b)) but exhibits an additional improvement [63]. The gates of transistors M_{R3} and M_{R4} are connected to the output terminals while transistors M_{R5} and M_{R6} are now controlled by the phase signal. This movement significantly reduces the sensitivity to the threshold mismatch and gives rise to excellent Montecarlo results. Moreover, transistors M_{R3} and M_{R4} turning off the circuit in the reset clock period, benefit the dynamic current consumption.

3.3.1 Two Stage Operational Amplifier with Slew-Rate Enhancement.

Two stage amplifiers fulfill moderate gain and high output swing requirements, but the most challenging issues are imposed by the power consumption and by the slew-rate performance limited by the compensation capacitor. One of the possible solutions is to increase the quiescent current of the amplifier, but this leads to a power consumtion penalty.

The slew-rate of a two stage fully differential amplifier, schematically indicated in Fig. 3.14, is limited by the maximum current of the current sources. During positive slewing ($V_{INP} > V_{INN}$), the current through C_C is limited by $I_B - I_{1P}$ while, in the other half circuit, the current through C_C is limited by I_{1N}. In the meantime, I_{2N} must discharge (C_C+C_L). For an optimal slewing operation of a conventional two stage amplifier, it is necessary to have

$$I_2 = I_1 \left(\frac{C_C + C_L}{C_C} \right), 2I_1 = I_B. \tag{3.9}$$

Therefore, for slew-rate enhancement, it is necessary to have a slew-rate monitor, which boosts output current sources I_{1P}, I_{2P} and I_B in one direction, and I_{1N}, I_{2N} and I_B in the other direction. When considering to use a slew-rate enhancement circuit, condition (1) is not strictly necessary anymore since the auxiliary circuit provides the current required to improve

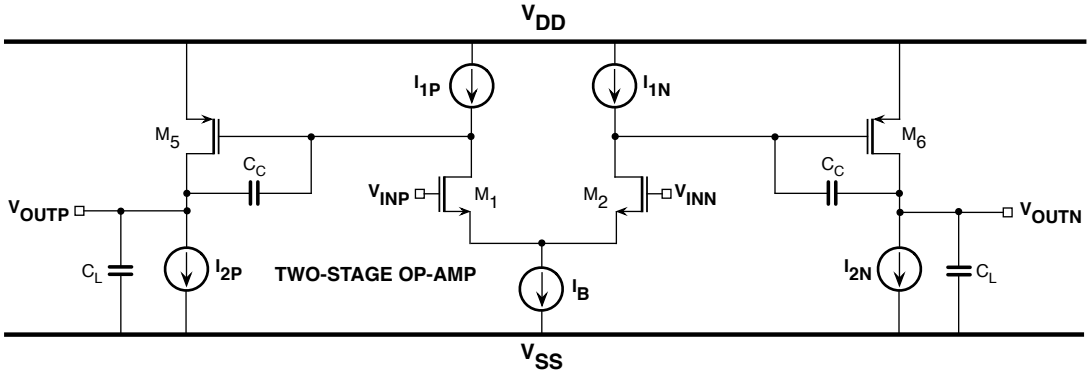


Figure 3.14: Conventional fully differential two stage amplifier

the slew-rate. Suppose, for example, to increases the slew-rate by a factor β; generators I_B and I_1 must be supported by an extra current of $I_{BOOST} = (\beta - 1)I_1$, while the current source I_2 needs an extra current of

$$I_1(\beta - 1)\left(\frac{C_C + C_L}{C_C}\right) \tag{3.10}$$

Therefore, since the faster discharge of (C_C+C_L) is sustained by the extra boosting current, the current in the second stage can be optimum for gain and speed.

The proposed slew-rate enhancement technique is based on the Fig. 3.15 [64]. Basically, there is an additional auxiliary block, driven by the input signal, which monitors the slewing conditions of the op-amp and boosts the slewing performance.

As mentioned above, for improving the slew-rate it is necessary to increase the currents indicated with the symbols I_1, I_2 and I_B in Fig. 3.14. Fig. 3.16(a) shows the used auxiliary slew-rate monitor circuit. This architecture uses the bias current I_B that, obviously, increases the consumed power. The differential pair, M_{M1} and M_{M2}, injects its current in two diode connected transistors, M_{M5} and M_{M6}. The extra current generators αI_B establish the current in M_{M5} and M_{M6}. By inspection of the circuit, in the quiescent conditions, I_{MM5}=I_{MM6}=($\alpha - 1/2)I_B$. Indeed, it has to be distinguished between two cases: $\alpha > 0.5$ and $\alpha \leq 0.5$. In the former case, the output current in the quiescent condition is zero and a minimum unbalance is required for a boosting signal. The maximum current in the diode connected transistors is $(1 - \alpha)I_B$, but, since the quiescent current is zero, the mirror factor can be very large. This

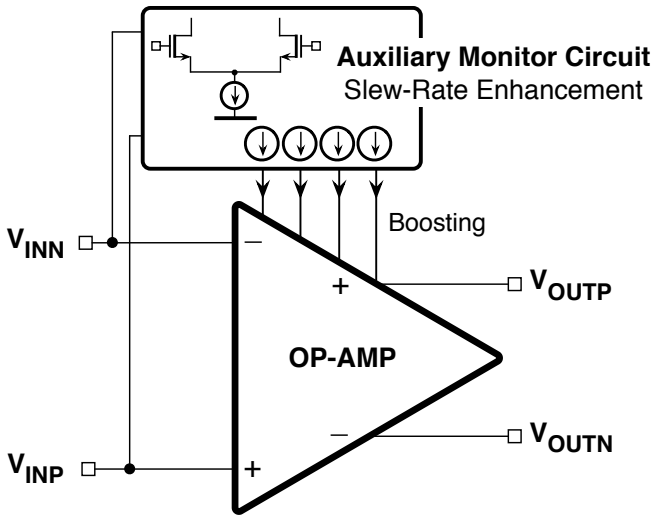


Figure 3.15: General block diagram of an op-amp with slew-rate enhancement.

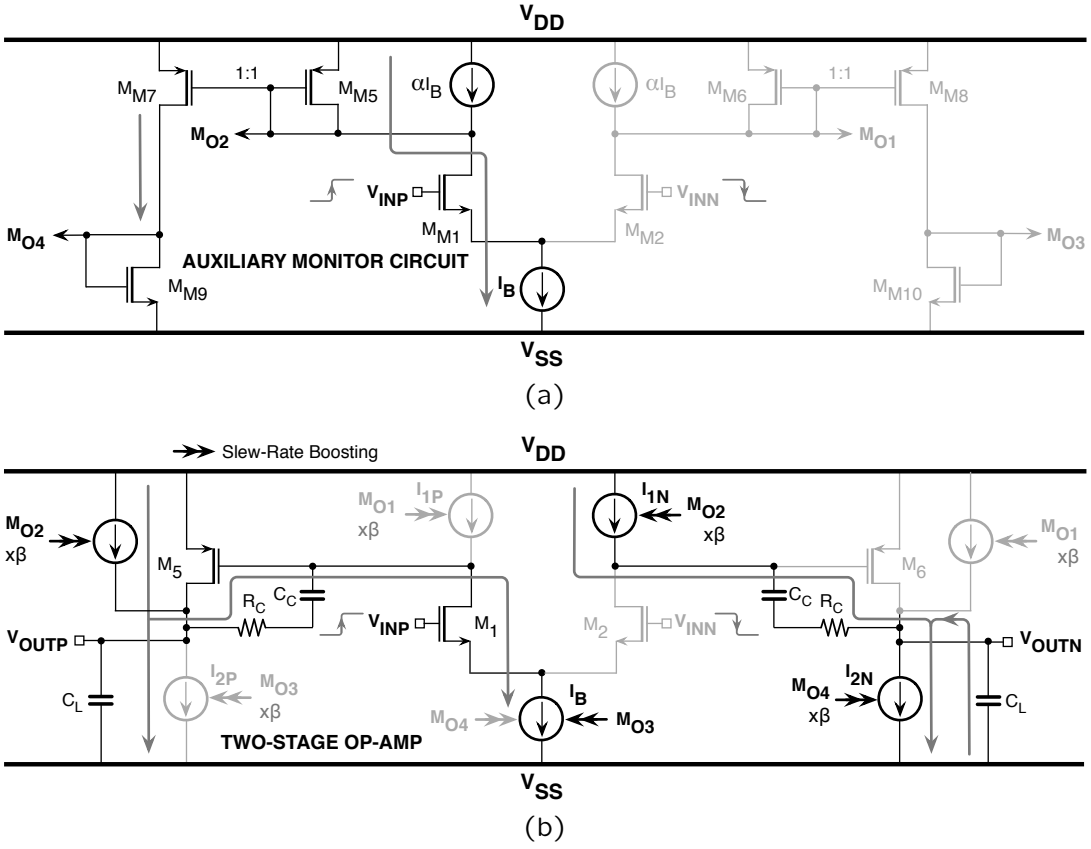


Figure 3.16: Slew-rate behavior for $V_{INP} > V_{INN}$. (a) Auxiliary monitor circuit. (b) Two stage amplifier with slew-rate boosting.

operation can be a good choice for low power applications, however, switching transistors from the off to the on state causes a delay that limits the boost speed. If $\alpha \leq 0.5$ the quiescent current in the diode connected elements is $(1/2 - \alpha)I_m$. A full unbalance brings this current to $(1 - \alpha)I_m$ with a relative increase by $(1 - \alpha)/(1/2 - \alpha)$. Therefore, if $\alpha = 0.3$ the current increases by 3.5, a good figure for practical cases.

The boosting operation in the two stage amplifier is done with additional current sources biased with the four output boosted signals, M_{O1} to M_{O4}, generated by the auxiliary circuit [64]. As shown in Fig. 3.16(b), M_{O1} and M_{O2} boost the current of p-channel transistors in the two stage amplifier while M_{O3} and M_{O4} boost the n-channel transistors. Therefore, when the input differential signal is large, the input pair of the auxiliary circuit delivers the entire bias current I_B toward one of the two diode connected elements and obtains a significant boost of the output control even thanks to a possibly large output mirror factor, described as β in the current sources of Fig. 3.16(b).

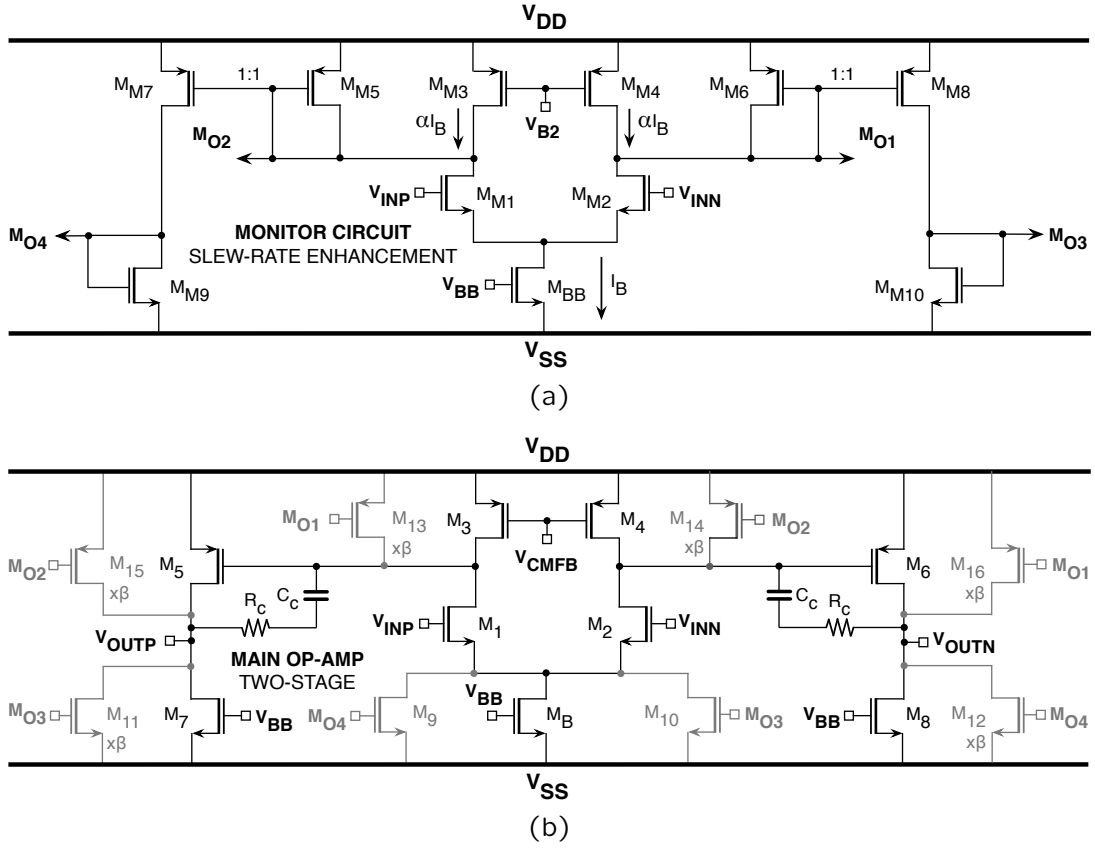


Figure 3.17: Schematic diagram of the complete operational amplifier. (a) Auxiliary monitor circuit. (b) Two stage amplifier.

The complete schematic diagram of the operational amplifier is shown in Fig. 3.17. The two stage amplifier uses four more n-channel transistors in parallel with the current sources M_7, M_8 and M_B. Similarly, four additional p-channel transistors are connected in parallel with the current sources M_3 and M_4 and the output transistors M_5 and M_6. The current in the differential pair is enhanced for slewing in both directions, while transistors M_3 to M_8 are alternately intensified. The controls for n and p-channel boost uses a larger mirror factor (β) to allow a scaling of the current in the second stage. At this purpose, the auxiliary circuit drains a fraction of the current that mirror the p-channel output and diminishes its quiescent value. For the sake of simplicity the same controls augment the differential pair current.

Fig. 3.18 shows the schematic circuit of the used common mode feedback (CMFB) [65]. The common mode control is done directly at the gates of transistors M_3 and M_4 of the main amplifier, as shown in Fig. 3.17(b). The circuit uses a dedicated differential input pair (M_{C1} and M_{C2}) with diode connected loads (M_{C3} and M_{C4}) to obtain relative high voltage

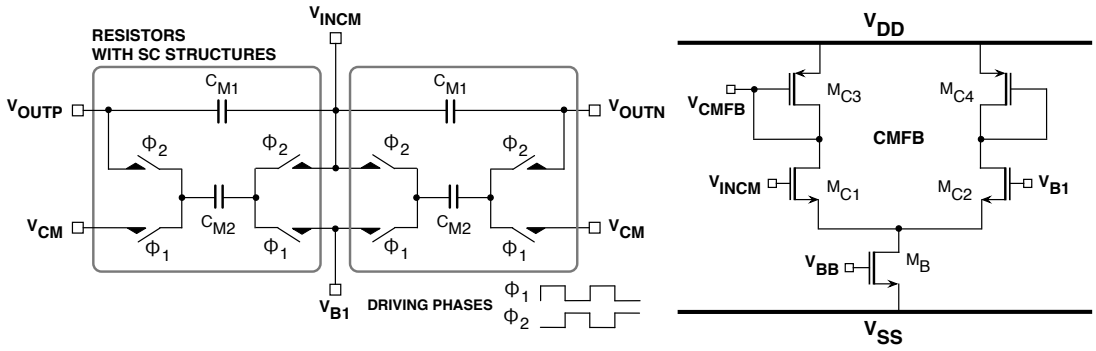


Figure 3.18: CMFB circuit of the two stage amplifier.

gain. Moreover, to sense the output common mode level two switched-capacitor structures implement the resistive sensing [44].

3.4 Simulation and Measurement Results.

The proposed architecture of Fig. 3.7 has been simulated with Matlab-Simulink™ by considering the finite parameters of the op-amp [47]. The further reduction of the output swing in both integrators is shown in Fig. 3.19.

The simulation compares the dynamic ouput voltage with and without the used swing reduction techniques in the proposed third-order modulator. The first integrator output goes down from 1.352 V_{P-P} to 0.201 V_{P-P}, saving by almost 85 $\%$ its dynamic range. The second integrator reduces its swing by approximately 48 $\%$ (0.816 V_{P-P} to 0.427 V_{P-P}), verifying the effectiveness of the analog feedforward path and the flash architecture with reduced input dynamic range.

The single op-amp third-order $\Sigma\Delta$ modulator has been fully simulated at the transistor level by using a 0.18-μm CMOS technology, dual poly and 6 metal levels. The nominal supply voltage is 1.5 V. The two stage amplifier and auxiliary monitor circuit of Fig. 3.17 using a current bias of I_B = 10 μA. The CMFB circuit of Fig. 3.18 uses half.

Fig. 3.20 shows the slew-rate monitor response for different values of α. For α = 0.5, the output current of transistors M_{M5} and M_{M6} is zero in quiescent conditions and starts rising when the differential signal is larger that 10 mV differential. The output current reaches its maximum $I_B/2$ for large unbalance. With α = 0.25 the current in the diode connected transistors ranges from 0.25 I_B to 0.75 I_B in the slewing status. The other displayed case is for α = 0.

For a low power operation the top current generators of the auxiliary circuit are fixed to 7 μA (α = 0.7). Therefore, when the inputs are unbalanced, the slewing condition directs the

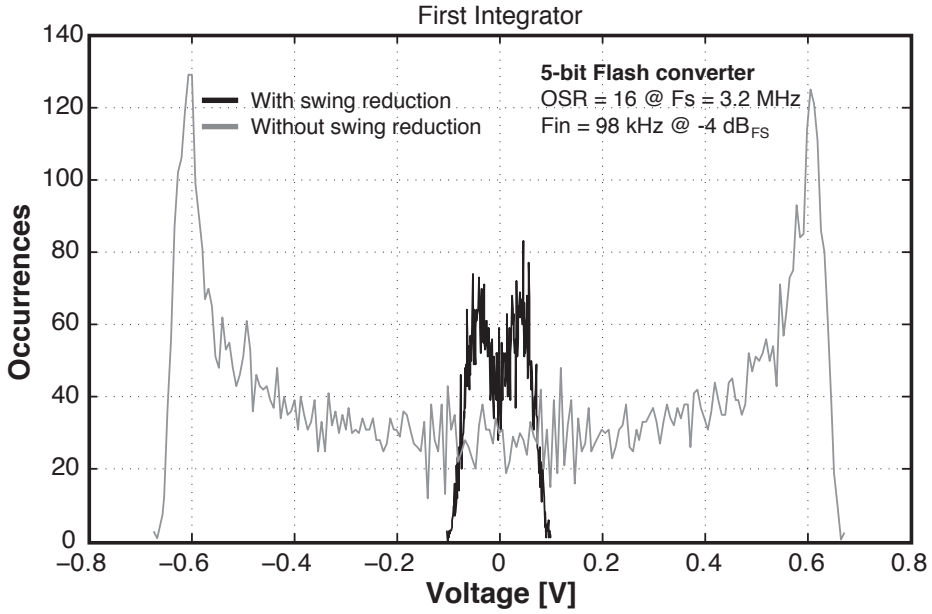


Figure 3.19: Output voltage swing. (a) First integrator. (b) Second integrator.

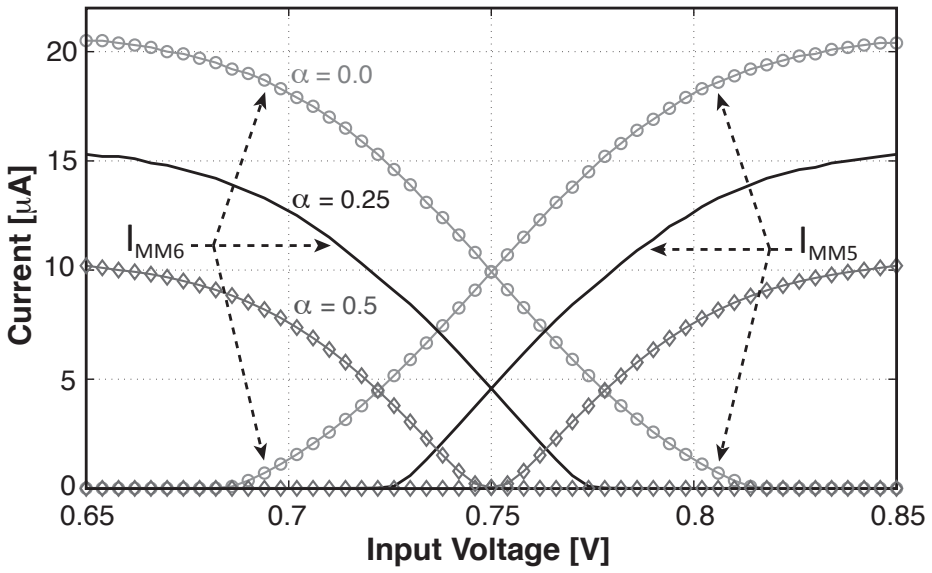


Figure 3.20: Simulated slew-rate monitor circuit response for different values of α..

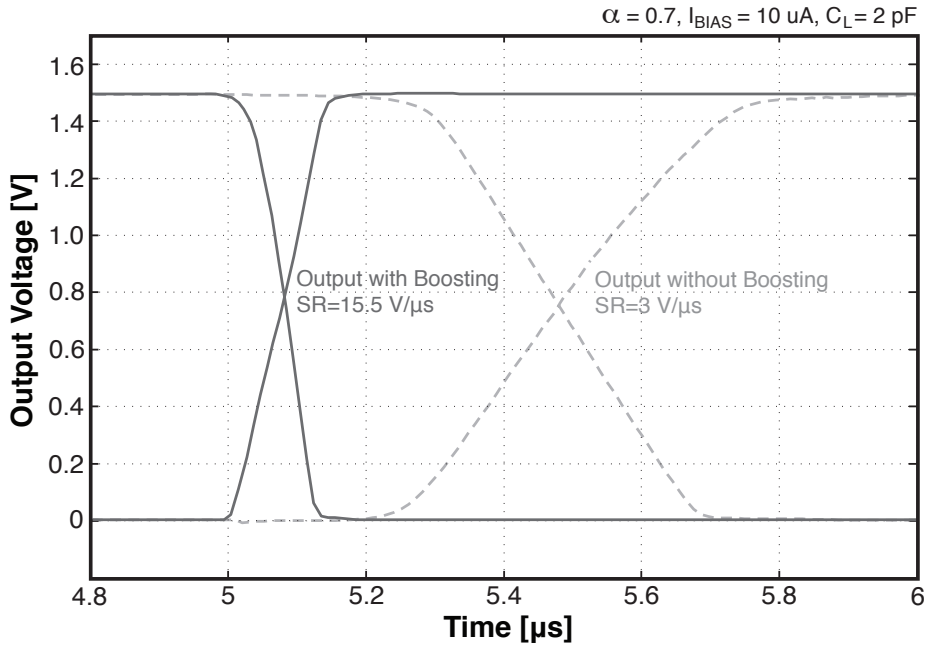


Figure 3.21: Simulated slew rate response.

maximum current in one branch and one of the diode connected transistor drains 3 μA. This current and its mirrored version ($\beta = 4$) augments the output currents of the main amplifier.

Table 3.1: Performance of the Two Stage Amplifier

0.18 μm, double poly, 6 metal levels CMOS technology, 1.5 V supply voltage

Parameter	Symbol [Unit]	Value
Bias Current	I_B [μA]	10
DC Gain	Av [dB]	65
Unit Frequency	GBW [MHz]	25
Phase Margin @ C_L= 2 pF	Φ_M [Degree]	67
Slew-Rate Performance (with Boost)	SR [V/μs]	3 (15.5)
Power Consumption (with Boost)	P_W [μW]	64.5 (67.5)

The slewing responses with a 2 pF load are compared in Fig. 3.21. The figure outlines a slew-rate improvement by approximately 5.2 times (from 3 to 15.5 V/μs) by using the boosting technique. Table 3.1 summarizes the performance of the amplifier. As expected, the power consumption of the boosted scheme is higher than the one of the conventional circuit. However, a proper trimming of the mirror factors enables a good reduction of the current in the second stage of the op-amp. The performance are unchanged while the total consumed power is only 4.5% more than the conventional counterpart.

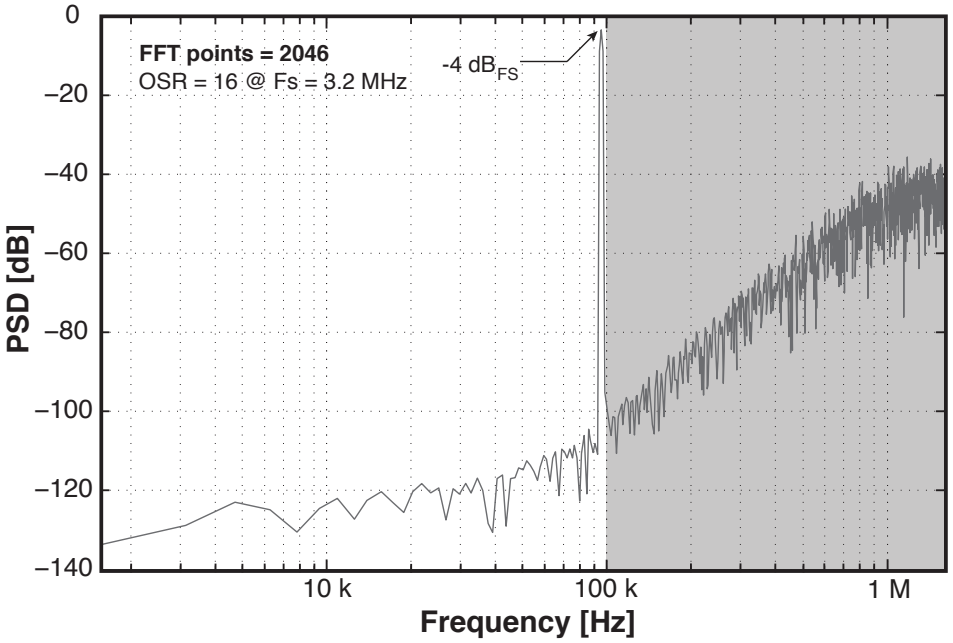


Figure 3.22: Simulated power spectral density.

Fig. 3.22 shows the simulated power spectral density of the modulator. The input signal is at -4 dB_{FS} and its frequency is 98.56 kHz. Considering an oversampling ratio of 16, the modulator achieves a signal to noise ratio (SNR) of 88 dB over a signal bandwidth of 100 kHz.

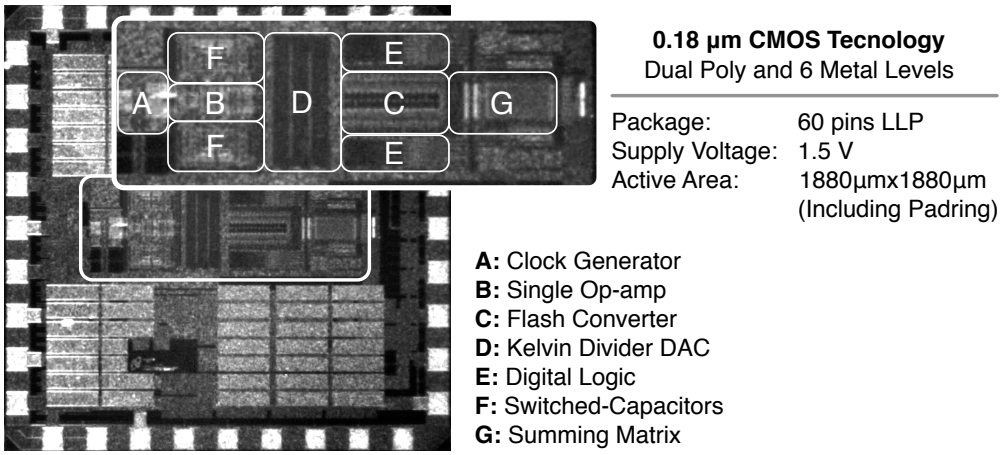


Figure 3.23: Chip microphotograph of the modulator.

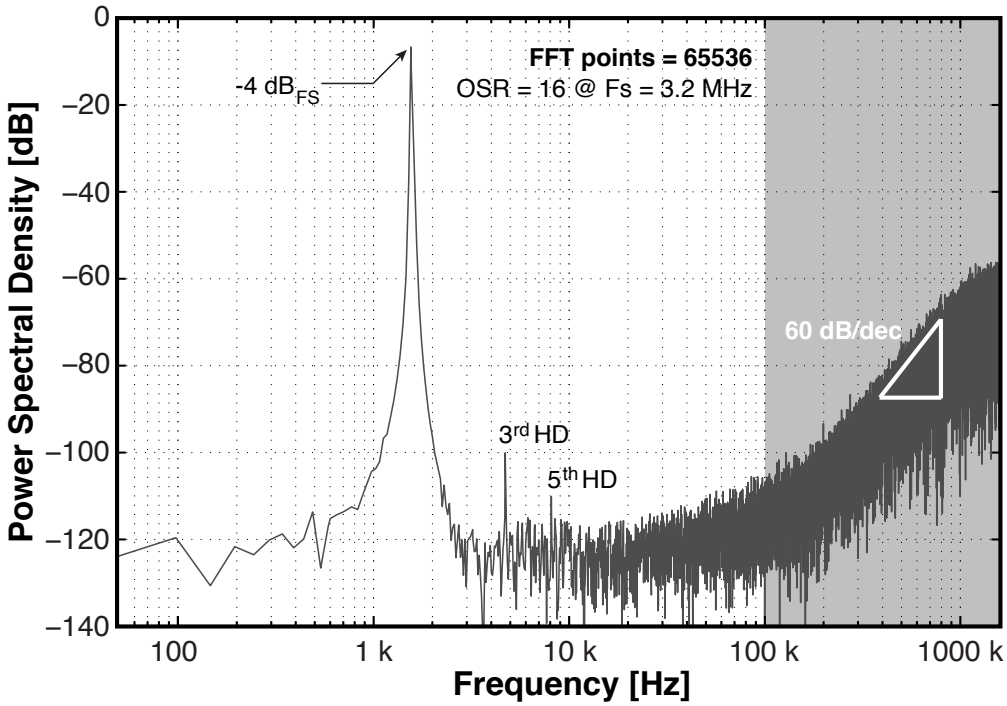


Figure 3.24: Measured power spectral density of the proposed modulator.

The chip microphotograph of the modulator integrated in a 60 pins LLP package is shown in Fig. 3.23. The main circuital blocks are highlighted in the figure. The active area, including padring, is 1880 μm x 1880 μm.

Fig. 3.24 shows the measured power spectrum with a 1.6 kHz input signal at -4 dB$_{FS}$. Sampled at 3.2 MHz (OSR = 16) the accomplished SNDR is 84 dB, corresponding to an effective number of bits equal to 13.6. The FFT is made with 65536 points. Third and fifth harmonic distortion tones are at -100 dB$_{FS}$ and -112 dB$_{FS}$, respectively. The achieved spurious free dynamic range (SFDR) is 96 dB while the measured power consumption of the modulator, clocked at full speed, is 140 μW (the consumed power by output buffers are not considered). The overall power breakdown of the modulator is depicted in Fig. 3.25. The attained FoM; considering once again the expression

$$FoM = \frac{P_{TOT}}{2^{ENoB} 2BW} \tag{3.11}$$

where P_{TOT} is the total power consumption, $ENoB$ the effective number of bits, and BW the signal bandwidth; is 54 fJ/conversion.

Fig. 3.26 shows the measured SNDR versus the input amplitude with OSR equal to 16 and 32. The higher oversampling ratio secures an increase of the SNDR peak at 88.9 dB (approximately 14.5 bit of resolution) with -4 dB$_{FS}$. The dynamic ranges for OSR equal to 16 and 32 are 88 dB and 94 dB, respectively. The higher resolution achieved with OSR = 32 does not benefit the noise shaping because the noise floor is slightly higher than expected. The FoM for the 50 kHz bandwidth is 61 fJ/conversion-level.

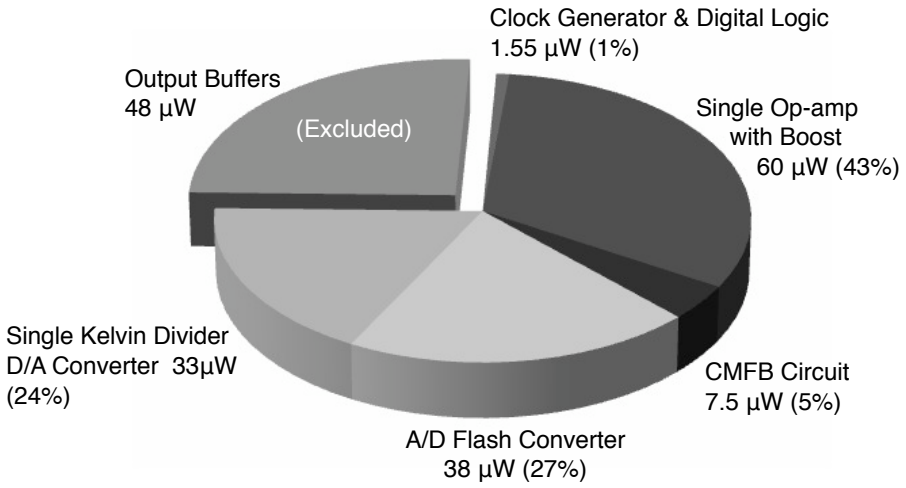


Figure 3.25: Power Consumption of the single-opamp third-order modulator.

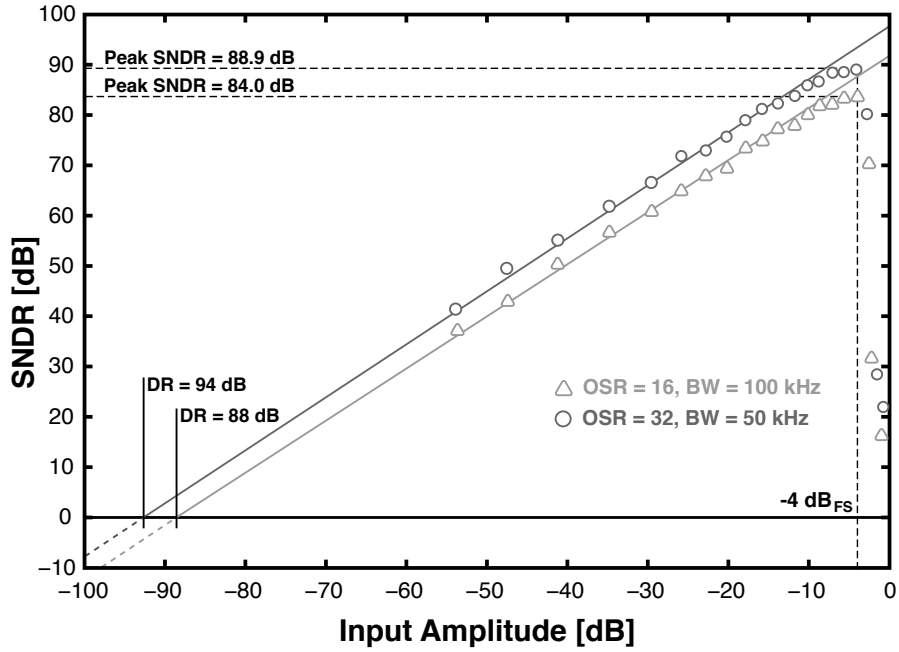


Figure 3.26: Measured SNDR versus signal amplitude for OSR = 16 and OSR = 32.

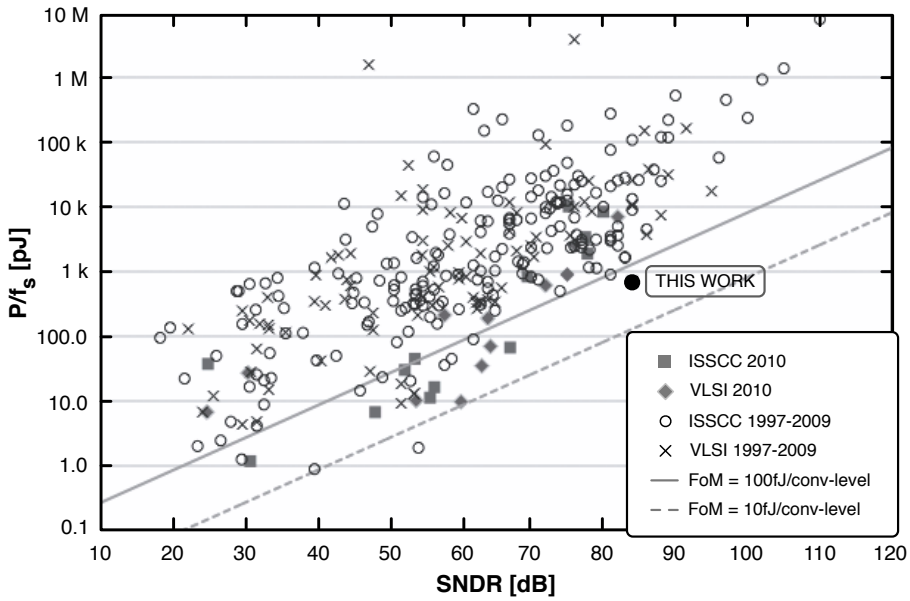


Figure 3.27: Comparison of the proposed ΣΔ modulator with other state-of-the-art A/D converters reported in recent years.

Fig. 3.27 compares the performance of this $\Sigma\Delta$ modulator with other state-of-the-art A/D converters reported in recent years. The power-efficency of the proposed third-order $\Sigma\Delta$ modulator verifies the effectiveness of the architecture. The performance summary of the modulator is given in Table 3.2.

Table 3.2: Summary Performance of the Modulator

0.18 μm, double poly, 6 metal levels CMOS technology, 1.5 V supply voltage

Parameter	**Symbol [Unit]**	**Value**	
Clock Frequency	F_S [MHz]	3.2	
Power Consumption	P_W [μW]	140	
Oversampling Ratio	OSR [–]	16	32
Signal Bandwidth	BW [kHz]	100	50
Peak SNDR	SNDR [dB]	84.0	88.9
Effective Number of Bits	ENoB [Bits]	13.6	14.5
Dynamic Range	DR [dB]	88	94
Figure of Merit	FoM [fJ/conversion-level]	54	61

Chapter 4

High-Performance $\Sigma\Delta$ Modulators

This chapter presents two low-power $\Sigma\Delta$ modulators. The first one corresponds an a double sampled second-order $\Sigma\Delta$ architecture with analog look ahead (ALA) approach. The proposed method provides an extra clock period to be used for the quantization and allows conversion with a relatively high oversampling ratio. The feedforward path in both integrators combined with the reduction of the number of quantization levels in the quantizer, enables a significant reduction in the overall power consumption of the modulator.

The second $\Sigma\Delta$ architecture exhibits a third-order noise shaping by using two operational amplifiers. The modulator achieves complex conjugate zeros that allows obtaining a SNR improvement of about 8 dB. Moreover, the design uses a fully digital solution to reduce both amplifiers output swings. Behavioral level simulations, considering the slew-rate, bandwidth and DC gain limits of the amplifier, demonstrate the effectiveness of the proposed solutions.

4.1 Double Sampled ALA $\Sigma\Delta$ Modulator.

Portable communication systems require wide-band data converters with medium resolution and very low power. The $\Sigma\Delta$ technique is a suitable choice especially with multi-bit DACs that relax the noise shaping requirements. The order of the modulator, the number of bits of the quantizer and the oversampling ratio are the elements that the designer considers

for a minimum power consumption. Furthermore, the modulator can be continuous-time or sampled-data. There are advantages and disadvantages for both solutions. The most relevant benefit of continuous-time is the low power but the noise caused by the clock jitter is a significant limit for very high clock frequencies. Besides, the linearity of the DAC can be a significant source of noise and distortion. Therefore, for medium and high resolution it is prudent to use the sampled data method but the power cost must be carefully considered.

As is known the double sampling technique enables the doubling of the sampling frequency with a negligible extra cost in the op-amp power consumption [28], [29]. This is quite effective for $\Sigma\Delta$ schemes because the number of bits is increased by the order of the modulator plus one. The double sampling method avoids the phase during which the op-amp does not integrate charge and actively operates the op-amp during both phases. Since input and output must be sampled by two different capacitors it is necessary to reduce the effect caused by mismatch but suitable proposed techniques moderate the limit [30], [31]. Indeed, a suitable time-slot for the quantizer must be allocated. In conventional $\Sigma\Delta$ schemes this time is the half of the full period delay unused by the last integrator. Since with double sampling scheme the integrator uses the full period, the time necessary for quantization must be borrowed from the full period. This increases the power of the integrator and the power of the ADC.

This section describes a design method that provides an extra clock period to be used for the quantization. The method, called Analog Look Ahead (ALA), combined with a significant reduction of the slew-rate requirements of the op-amps enables conversion with a relatively high oversampling ratio (OSR) and low power.

4.1.1 Impact of the Dynamics in the Power Consumption.

The power needed for the operation of a sampled-data $\Sigma\Delta$ modulator is mainly the power of the op-amps and the ADC. The power of the digital sections is normally negligible. An effective conversion of wide-band signals seeks for the maximum OSR permitted by technology, while using a given order of the modulator and a reasonable number of bits in the quantizer. However, increasing the clock frequency increases the power because of the request of op-amp bandwidth and slew-rate. Consider, for example, a conventional modulator running at 320 MHz and 1 V_{FS}. The time for integration is 1.56 ns. Simulations with a behavioral model show that the slewing time must be lower than 0.2 the available time. Therefore, with a full swing signal and a small capacitance like 0.2 pF, the bias current of the input differential pair must be

$$I_B = \frac{\Delta V}{\Delta t} C_{eq} = \frac{0.2 \cdot 10^{-12}}{0.2 \cdot 1.56 \cdot 10^{-9}} = 640\ \mu A \tag{4.1}$$

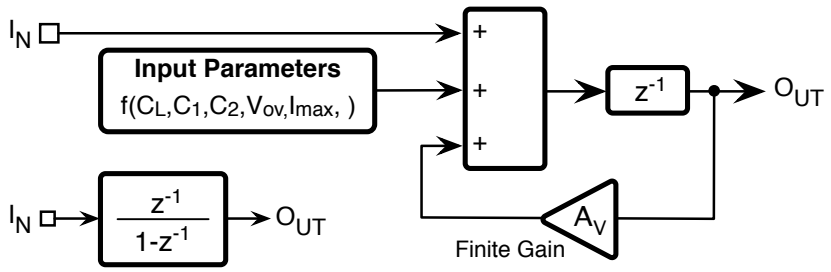


Figure 4.1: Block diagram of the behavioral model.

Supposing to have an overdrive of the input pair of 0.2 V the estimated gain bandwidth product, GBW, is about 2.5 GHz, more than enough for medium resolution. Therefore, being the slew-rate the limit to low power it is necessary to use architectures that reduce the voltage swing of integrators. In addition, a limited voltage swing enables the use of power effective schemes like the telescopic cascode. The error caused by a limited speed of the op-amp used in the second stage is less relevant than the one of the first stage because it is shaped at the first order. As a rule of thumb we can suppose that the current bias of the input pair can be half the one of the first stage op-amp.

The above considerations have been verified with a behavioral model that takes into account the finite bandwidth of the operational amplifiers and the slew-rate condition for the double sampling technique (see Fig. 4.1). The model, which is not discussed in this work, has several input parameters: the load capacitance of the integrator C_L, the input pair overdrive voltage V_{OV}, the integration capacitors C_1 and C_2 and the maximum current that flows through the differential pair I_{max} (considering for example a single stage amplifier). As shown in Table 4.1, the simulations were done achieving the same SNR, for a traditional second order architecture and the one with the forward loops. The modulator of Fig. 4.2 shows the feedforward paths at the input of the second integrator and the quantizer. With this comparison, for

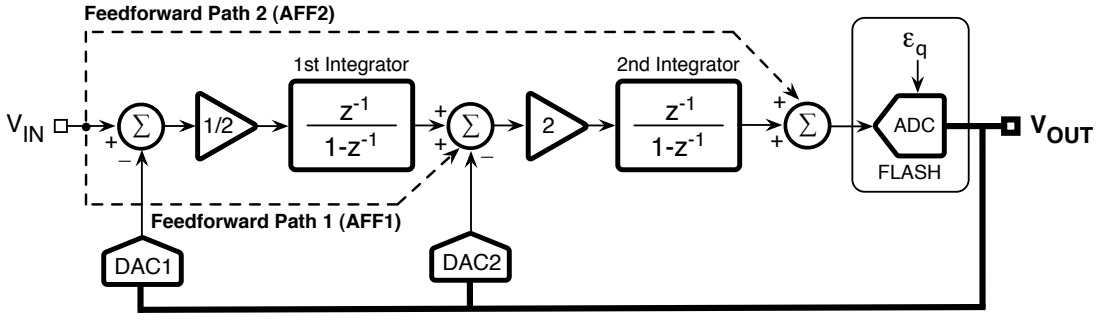


Figure 4.2: Second order ΣΔ modulator with feedforward paths.

Table 4.1: Simulation Results at Behavioral Level
SNR$_{ideal}$ = 68 dB @ -1dB$_{FS}$, F$_S$ = 320 MHz @ OSR = 16
3 bit Flash converter, C$_L$ = 0.2 pF, Overdrive Voltage = 200 mV

Architecture	I_{max} 1st Int. [μA]	I_{max} 2nd Int. [μA]	Total Power [mW]	OSR [–]	SNR [dB]
Conven. single sampled	640	280	1.38	16	67.1
Conven. double sampled	360	180	0.81	8	67.2
AFF single sampled	340	220	8	16	67.1
AFF double sampled	170	120	0.81	8	66.9

the single and double sampling cases, it is possible to emphasize the benefits of reducing the signals swing for the power reduction.

The estimated power consumption of the amplifiers given in Table 4.1 for a 1.5 V power supply assumes that the power is dominated by the input stage. Actually, unless using a telescopic scheme, there is an additional consumed power; therefore, for a quantitative estimation it is necessary to refer to the specific op-amp architectures. However, as Table. 4.1 shows, the power reduction can be as large as 3 times if both output swings are less than the input pair overdrive (assumed in the behavioral model 0.2 V).

Supposing to reduce the power by significantly limiting the output swing, the power is determined by the needed GBW that, for medium resolution is 2-3 times the clock frequency. Under these conditions the double sampling technique is very convenient because the integration time doubles and the needed g$_m$ halves. This reduces by approximately 4 times the bias current (see the current in the first integrator for the traditional single sampled and the feedforward double sampling topologies).

4.1.2 Analog Look Ahead Principle.

For double sampled analog ΣΔ modulators, the use of the full period for the signal integration does not leave any time for the quantization and requires possible modifications of the modulator architecture for relaxing the feedback timing. This discussion is treated in a recent publication [32]. It uses extra branches in the architecture that obtain an extra delay available for the quantizer and therefore the double sampled integration can be done in the complete half cycle. However, the solution requires an extra delay of the input signal that complicates the circuit implementation. The proposed architecture obtains the same result with a different approach, called Analog Look Ahead (ALA) ΣΔ modulator.

In order to explain the method let us start from the single-loop second-order architecture shown in Fig. 4.3.

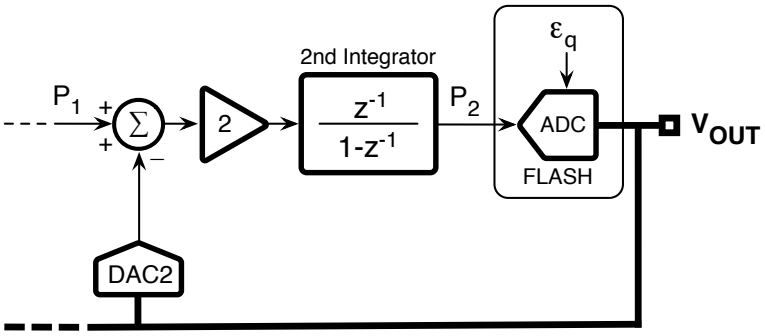


Figure 4.3: Single-loop second order ΣΔ modulator.

The system obtains an extra clock period if the input of the quantizer is the anticipation of the voltage granted at the output of the second integrator, P_2, during the next clock period. This, by inspection of the diagram of Fig. 4.3 is

$$P_2(n+1) = P_2(n) - 2\,V_{OUT}(n) + 2\,P_1(n) \tag{4.2}$$

that in the Z domain becomes

$$P_2(z) = z^{-1}\left[P_2(z) - 2V_{OUT}(z) + 2P_1(z)\right] \tag{4.3}$$

and therefore, a full clock period delay becomes available for the A/D and D/A conversion. The prediction in equation (4.3) can be realized with the architecture shown in Fig. 4.4.

The method can be extended to any ΣΔ architecture to obtain an extra clock period delay for the quantizer. The cost of the method is an additional processing in front of the second integrator. The operation can be implemented with a passive network if the number of com-

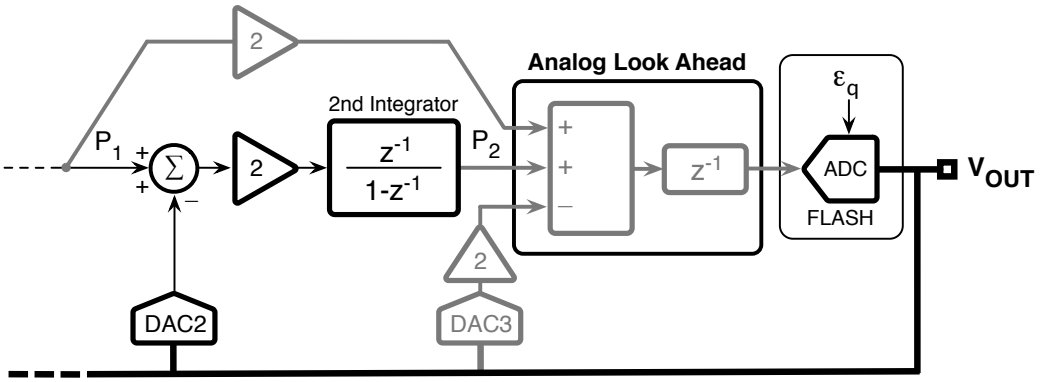


Figure 4.4: The analog look ahead (ALA) principle.

parators used by the flash converter is low (i. e. not more than 5). For many comparators it is necessary to use an extra op-amp within a zero delay scheme.

4.1.3 The Proposed Dynamic Reduction ALA ΣΔ Modulator.

The proposed ALA topology gives the advantage to enable complete clock periods for the injection of the signal at the input of integrators. Moreover there is a complete clock cycle for the quantization of the second integrator that is sampled at the end of the full injection period. These features enable the double sampled ΣΔ schemes whose architectures use in each integrator a pair of switched capacitor inputs working in ping-pong fashion.

As discussed above, doubling the injection time significantly relaxes the op-amp specifications but there is another important feature: to have a low output swing in the op-amps. If it is below the overdrive of the input pair there is no slewing and the full clock period is used for the exponential settling of the output voltage (supposing a single pole transfer function). Therefore, in addition to double sampling capability it is necessary to use architectures that give rise to small outputs.

The two feedforward of Fig. 4.2 reduce the voltage swing of both integrators. These additional branches can be added to the scheme with the ALA addition. Since the first feedforward enters the input of the first integrator, it is necessary to add an extra injection to the ALA equal to the input multiplied by $2V_{IN}$. The second feedforward can be done directly at the input of the ALA giving a total extra term of $3V_{IN}$ the input signal, as is shown in Fig. 4.5.

Another element critical for the power consumption is the flash. Its power depends on three factors: the quantization amplitude, the conversion rate and the number of comparators. The quantization amplitude, Δ_Q, multiplied by the preamplifier transconductance gives the current that charges the parasitic capacitance, C_p, of the latch. Supposing that the latch requires a

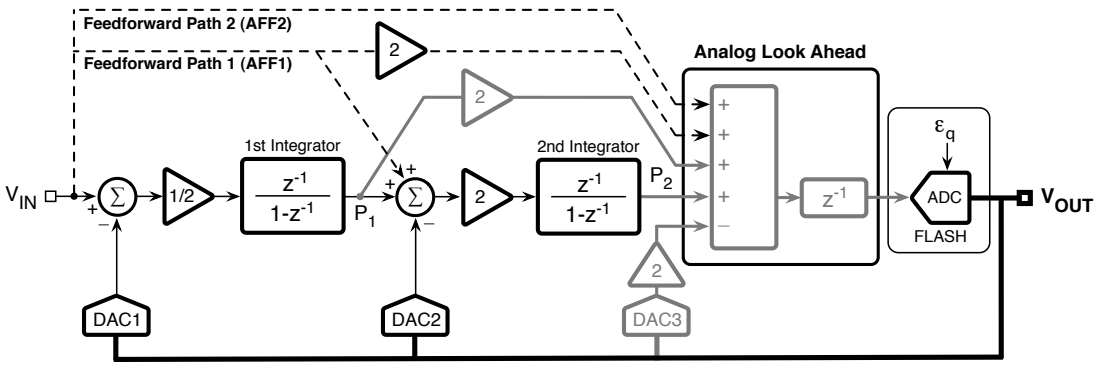


Figure 4.5: Effect of feedforward paths into the ALA topology.

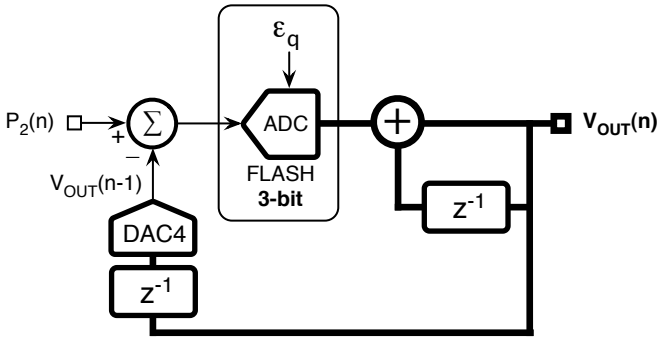


Figure 4.6: Flash converter with reduced input dynamics.

minimum voltage signal Δ V_{min} the charging time

$$\Delta t = \frac{\Delta V_{min} C_p}{g_m \Delta_Q} \tag{4.4}$$

must be a fraction of the clock period. Therefore, since increasing g_m requires a quadratic increase of the bias current, the number of bits of the quantizer must be carefully chosen. According to simulations, 3 or 4 bits are the best trade off with a converter full range of (0.5 - 1) V.

For a given flash resolution and medium OSR the power consumption of the flash can be reduced by observing that the dynamic range at the output of the ALA stage in Fig. 4.5 is the digital output minus the quantization error. This is the full scale (or more for 0 dB_{FS} inputs) and requires to use 2^N - 1 comparators for the flash converter. It is possible to reduce the number of required quantization levels by exploiting the correlation between two successive samples granted at the input of the flash, as shown in Fig. 4.6. The amplitude of P_2(n) - V_{OUT}(n-1) is smaller than P_2(n); therefore quantizing P_2(n) - V_{OUT}(n-1) reduces the number of comparators needed in the flash converter (see Chapter 2, Section 2.2.2).

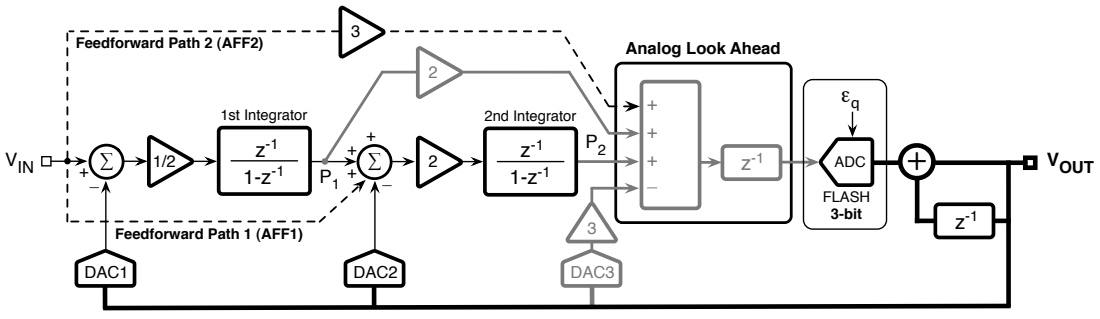


Figure 4.7: ALA modulator with flash converter with reduced input dynamics.

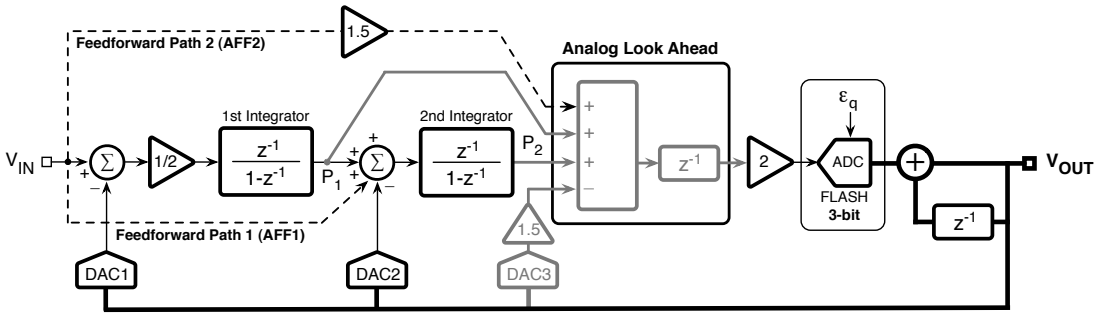


Figure 4.8: Proposed ALA second-order ΣΔ architecture.

The extra branch of Fig. 4.6 added to the already existing ALA input of -2·V_{OUT} gives a total injection of -3·V_{OUT}, as shown in Fig. 4.7. A topological transformation that moves the gain by 2 of the integrator at the input of the quantizer gives the proposed analog double sampled look ahead ΣΔ modulator shown in Fig. 4.8. The reduced dynamic ranges in the integrator's outputs and the reduced quantization levels are obtained because of the prediction realized in the ALA stage.

Notice that the extra delay for the quantization is obtained without the necessity of analog delays in the forward paths. As a result, the architecture can be designed with a switched capacitor (SC) implementation. The forward paths addition can be realized at the input of the second integrator and in the ALA stage, respectively.

There have been reported several architectures to implement the summing function [16],

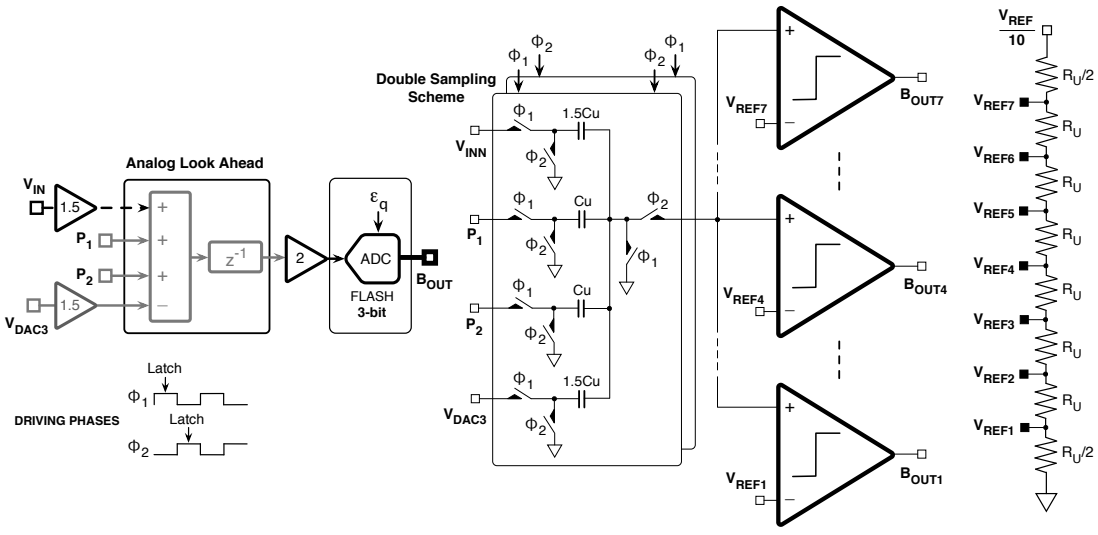


Figure 4.9: Switched-capacitor implementation of the ALA stage.

[34], [35], [37]. Fig. 4.9 shows a possible switched capacitor implementation of the ALA at the input of the flash converter [37]. For sake of simplicity the figure shows a single-ended solution. The complete clock cycle of the ALA stage benefits a double sampling operation thus eight SC structures, controlled by phases Φ_1 and Φ_2, implement its four inputs. The flash converter is latched at half of each phase control. An unity capacitance, C_U, is charged by the output of the first an second integrator respectively, while an unity capacitance of $1.5C_U$ is used for the feedforward path and the output of DAC3. The reference voltage of the flash is attenuated by approximately 10 times to satisfy both, the gain of two at the output of the ALA stage and the attenuation factor given by the summing operation. This circuital solution avoids the use of an additional operational amplifier but demands more sensitivity in the comparators. However since with 3 bits the number of necessary comparators is only 4 the passive network of Fig. 4.9 can be affordable without significant extra power.

The digital operations which make the reduction of the quantization levels in the flash A/D converter barely increase the area and power consumption. The reduction of the signal dynamics within the ALA ΣΔ modulator gives the possibility to use operational amplifiers with relaxed characteristics.

4.1.4 Simulation Results with Matlab-Simulink.

The analog look ahead ΣΔ modulator was simulated in Matlab Simulink by considering the behavioral model described early. In order to find the position of the proposed architecture on the state of the art in analog ΣΔ modulators, the simulation results are compared under the same conditions with one of the most recent architectures reported [32].

Fig. 4.10 shows the power spectrum of the double sampling ALA ΣΔ modulator for several cases. The input signal frequency is set to 9.45 MHz with -1 dB_{FS}. The sampling clock frequency is 320 MHz. The SNR is almost equal to the ideal value with a current in the input transistors equal to 61 μA and 78 μA respectively (the swing in the second op-amp is higher). Lowering the current supply to 20% reduces the SNR by 3 dB, as shown in Table 4.2.

The relaxed feedback timing ΣΔ modulator has a similar signal dynamic behavior for the first and second integrators and the slew-rate limits are similar to the proposed ALA technique. On the other hand the ALA architecture yields a reduced input dynamic in the flash converter. This is traduced in a reduction in the number of quantization levels and so in the number of comparators (from 7 to 4) needed in the flash. The flash input for the proposed double sampling ALA modulator and the double sampling time relaxed architecture [32] are compared in Fig. 4.11. The principal characteristics are summarized in Table 4.2.

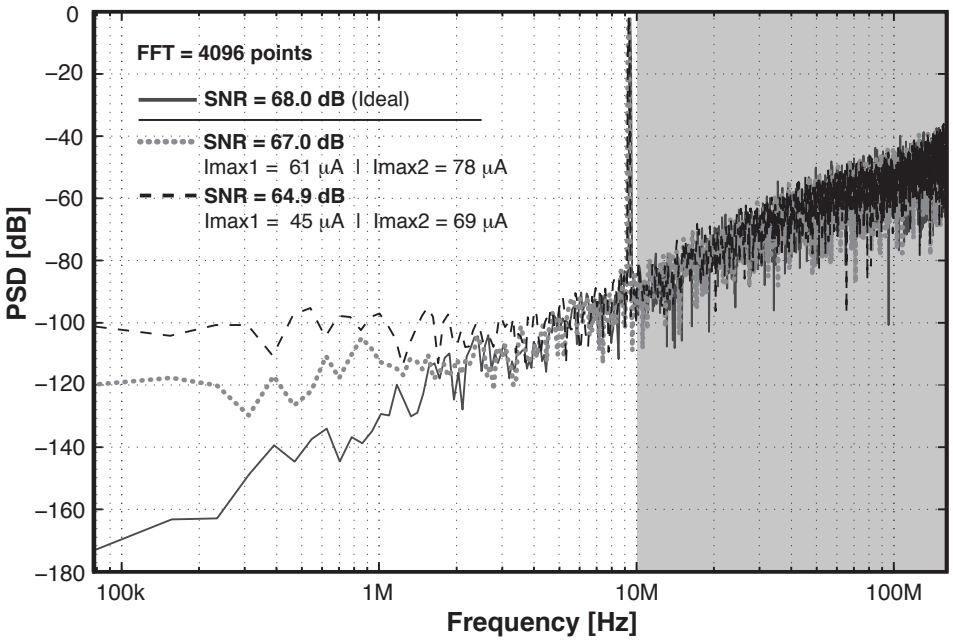


Figure 4.10: Simulated power spectral density of the ALA modualtor.

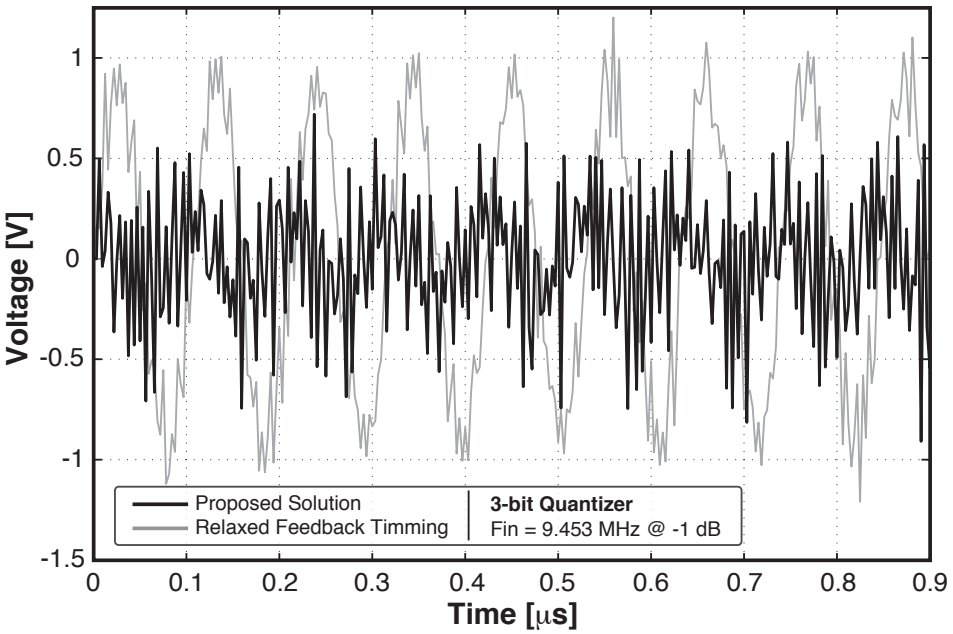


Figure 4.11: Comparison of input voltage swing of the flash converter.

Table 4.2: Simulation Results of the Proposed Double Sampled ALA ΣΔ Modulator
SNR$_{ideal}$ = 68 dB @ -1dB$_{FS}$, F$_S$ = 320 MHz @ OSR = 8
C$_L$ = 0.2 pF, Overdrive Voltage = 200 mV

Architecture	I$_{max}$ 1st Int. [μA]	I$_{max}$ 2nd Int. [μA]	Total Power [mW]	SNR [dB]	Bit	Comparators
Time Relaxed [32]	80	60	0.21	67.1	3	7
ALA (this work)	61	78	0.20	67.0	3	4

4.2 Third-Order ΣΔ Modulator with Complex Conjugate NTF Zeros.

Today portable communications market demands for high-performance analog to digital converters (ADCs) with severe requirements on power consumption, wide signal bandwidth and high resolution. To meet specifications, ΣΔ modulators are more and more addressed because provide good performance by taking advantage of the noise shaping. Furthermore, ΣΔ architectures have several design parameters that require special attention to modulator design: flash converter resolution, loop filter order and oversampling ratio (OSR). Increasing any of these parameters improves the SNR. For wide-band applications the OSR of the modulator cannot be to high because increases the power requirements of the amplifiers. Consequently, one of the options to meet the demanding target with low OSR is increasing the modulator order. However, a modulator with higher order loop filter will also results in more power dissipation by adding more active blocks. A further benefit for high order schemes is to have complex conjugate zeros [66]. For medium resolutions, the signal-to-noise (SNR) ratio can be about 8 dB better than having all the zeros at z = 1. Moreover, the use of low voltage swing operational amplifiers enable relaxed slew-rate requirements, better linearity, low power consumption and allows operation at low power supply voltage.

The following proposed ΣΔ modulator obtains the all the above features. It realizes with two operational amplifiers a third-order noise shaping; a fully digital solution reduces the amplifiers output swing and achieves complex conjugate NTF zeros.

4.2.1 Third-Order ΣΔ Modulator with Complex Conjugate Zeros.

Suitable topological changes of a third-order architecture obtains a scheme with two integrators, see Chapter 2. This proposed modulator obtains the result with complex conjugate zeros in the noise transfer function (NTF) by the direct cascade of two blocks, shown in Fig. 4.12, that realizes a zero at z = 1 and two complex ones with imaginary part α/2.

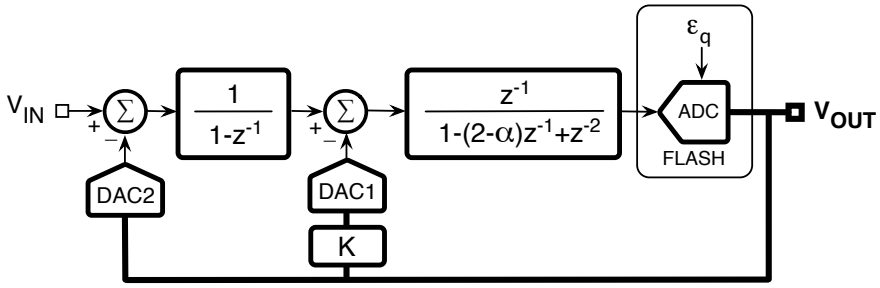


Figure 4.12: Block diagram of a third-order ΣΔ modulator with complex conjugate zeros.

The block K before DAC1 serves to avoid the denominator in the signal and noise transfer functions. By inspection of the scheme, the denominator is

$$D = NTF + z^{-1}[1 + (1 - z^{-1})K] \tag{4.5}$$

where

$$NTF = (1 - z^{-1})[1 - (2 - \alpha)z^{-1} + z^{-2}] \tag{4.6}$$

is the expected noise transfer function. The denominator becomes one if

$$K = (2 - \alpha) - z^{-1} \tag{4.7}$$

Thus, the NTF is accomplished and the signal transfer function (STF) becomes z^{-1}. The scheme of Fig. 4.13 implements the second block of the architecture of Fig. 4.12. Its transfer function is obtained by

$$\frac{(x - Py)z^{-1}}{1 - z^{-1}} = y \tag{4.8}$$

that results in

$$H(z) = \frac{y}{x} = \frac{z^{-1}}{(1 - z^{-1}) + Pz^{-1}} \tag{4.9}$$

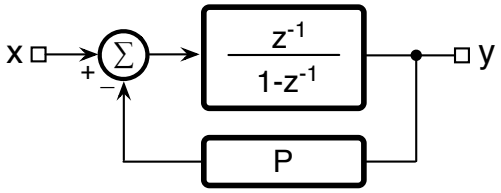


Figure 4.13: Block diagram of the second block of Fig. 4.12.

Therefore, it is necessary to have

$$P = z^{-1} - (1 - \alpha) \tag{4.10}$$

that requires to use a delay obtainable in the analog domain.

4.2.2 Fully Digital Swing Reduction.

Several methods, [33], [38], [39], [40], obtain op-amps output ranges reduction in multi-bit architectures. This design uses fully digital methods to avoid extra branches at the input of the op-amps. Fig. 4.14 shows the technique used to reduce the swing at the first integrator. An additional ADC (FLASH-2) converts the input signal V_{IN} and obtains an input feedforward toward the input of the second block.

By inspection of the circuit, the output of FLASH-1 is

$$V_{OUT'} = V_{IN} \cdot z^{-1} + \overline{V_{IN}} \cdot z^{-1}(1 - z^{-1}) + NTF \cdot \epsilon_q \tag{4.11}$$

where ϵ_q is the quantization error and $\overline{V_{IN}}$ is the quantized version of the input signal, V_{IN}. Therefore, we can eliminate in the digital domain the term $P_1(z) \cdot \overline{V_{IN}} = \overline{V_{IN}} \cdot z^{-1}(1 - z^{-1})$, as shown in Fig. 4.14, to obtain the original response.

For the swing reduction of the second block, notice that its output is

$$O_2 = V_{IN} \cdot z^{-1} + \overline{V_{IN}} \cdot z^{-1}(1 - z^{-1}) + \epsilon_q \cdot (NTF - 1) \tag{4.12}$$

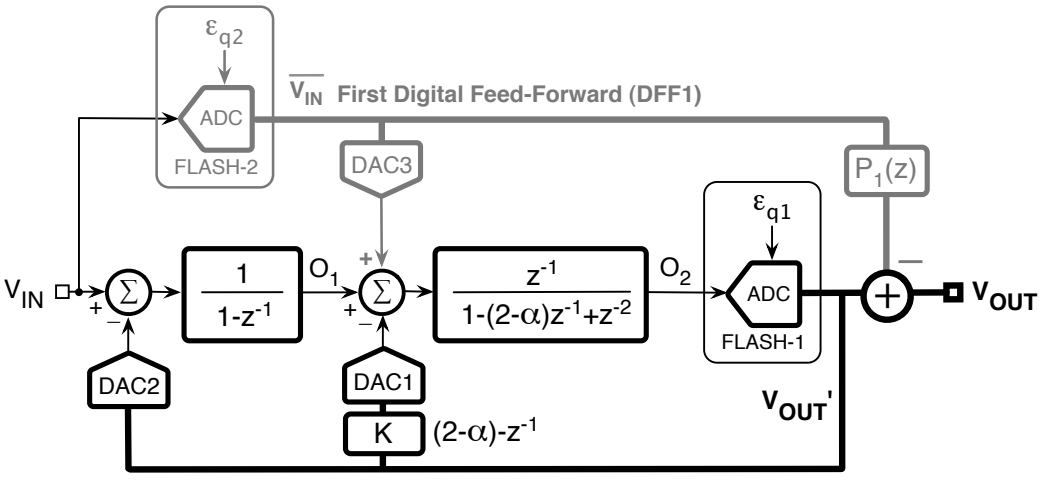


Figure 4.14: Digital swing reduction of the first integrator output.

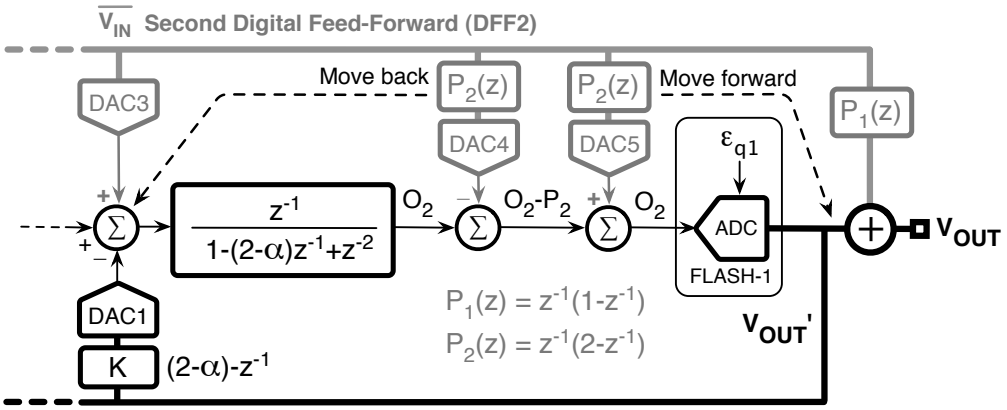


Figure 4.15: Digital swing reduction at the output of the second amplifier.

With a suitable number of bits in FLASH-1 and FLASH-2, the dominant part of O_2 is

$$\overline{V_{IN}} \cdot P_2(z) = \overline{V_{IN}} \cdot z^{-1}(2 - z^{-1}) \tag{4.13}$$

Suppose to add and subtract that term to O_2, as shown in Fig. 4.15. This operation does not change O_2. Then, the addition is moved in the digital section to obtain $(O_2 - P_2)$. The final step is to move the subtraction to the input of the second block, as depicted in Fig. 4.15. The output of the block becomes $(O_2 - P_2)$. Obviously, moving $-P_2(z)$ at the input of the block requires to divide $-P_2(z)$ by the block transfer function. Thus, the reduction of the swing of the second block requires a second extra injection at its input, as shown in Fig. 4.16

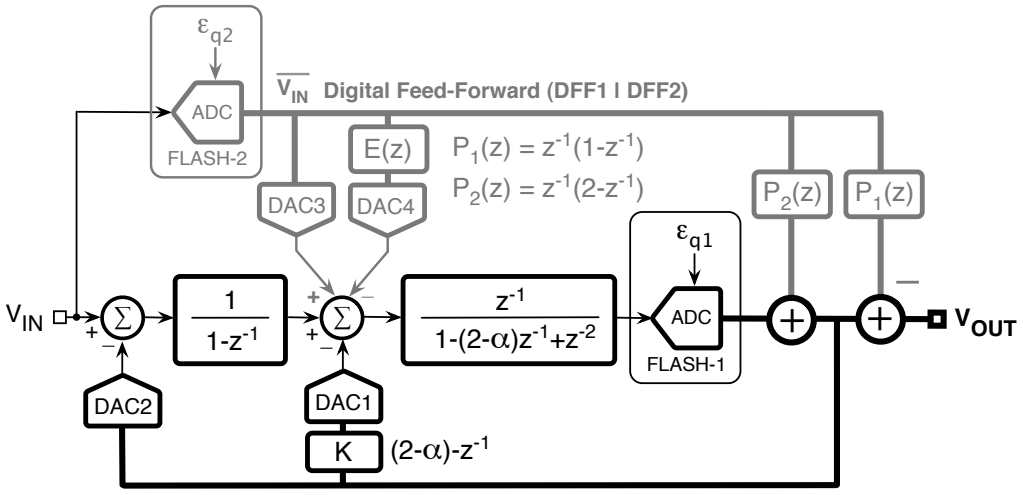


Figure 4.16: Third-order ΣΔ modulator with fully digital swing reduction.

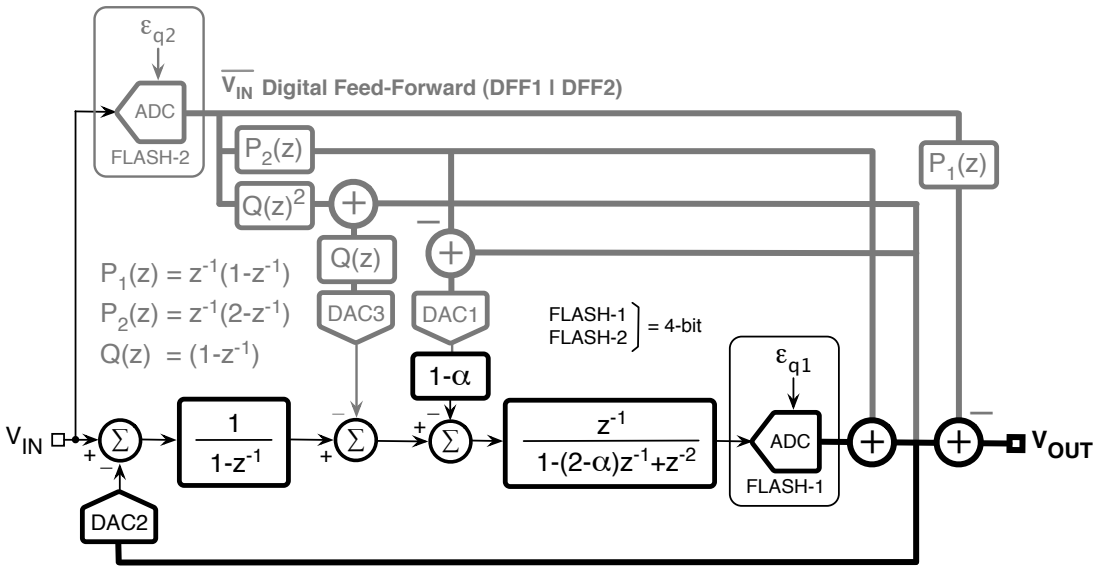


Figure 4.17: Proposed Third-order ΣΔ modulator.

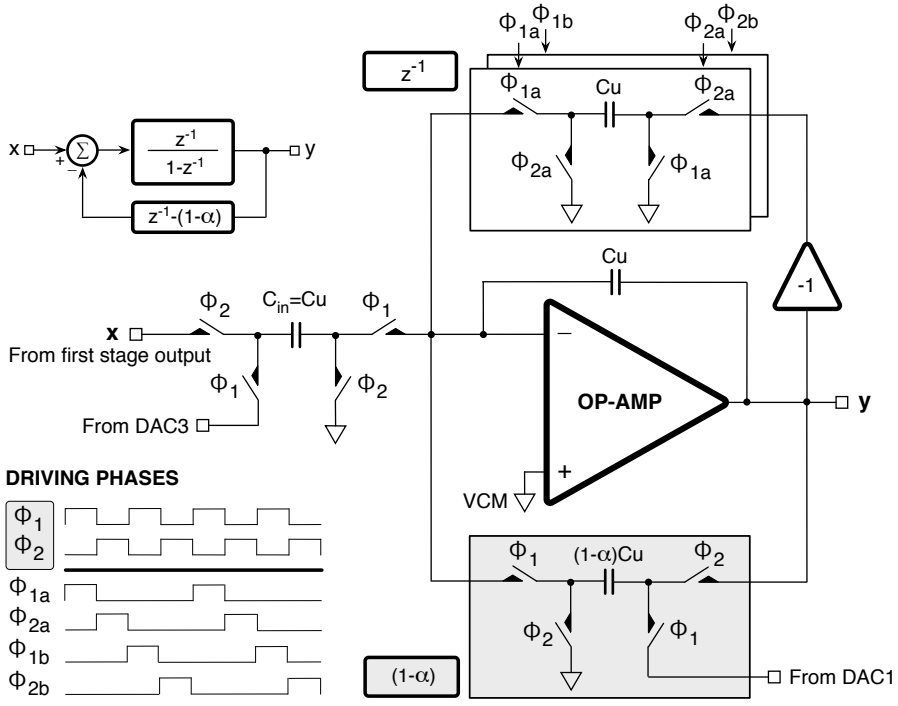


Figure 4.18: Possible single-ended SC implementation of the block diagram of Fig. 4.13.

Suitable combinations of digital terms lead the proposed $\Sigma\Delta$ scheme of Fig. 4.17. Fig. 4.18 shows a possible single-ended SC implementation of the modulator. The analog delay of (4.10) is realized with two capacitors working in interleaved fashion. The term $(1-\alpha)$, distinguished from the rest in Fig. 4.17, is realized by using the capacitor $(1-\alpha)C_u$ of Fig. 4.18. This capacitor serves also to implement the conversion of DAC1. Moreover, to implement DAC3, can be used the input capacitor C_{in}, whose left terminal is available during Φ_1. The figure includes the driving phases for switches control.

4.2.3 Simulation Results with Matlab-Simulink.

The proposed third-order $\Sigma\Delta$ modulator with reduced amplifiers output swing and complex conjugate zeros has been simulated at the behavioral level [47] with Matlab-Simulink™. The zeros placement depends on the accuracy of the capacitor that realizes this coefficient.

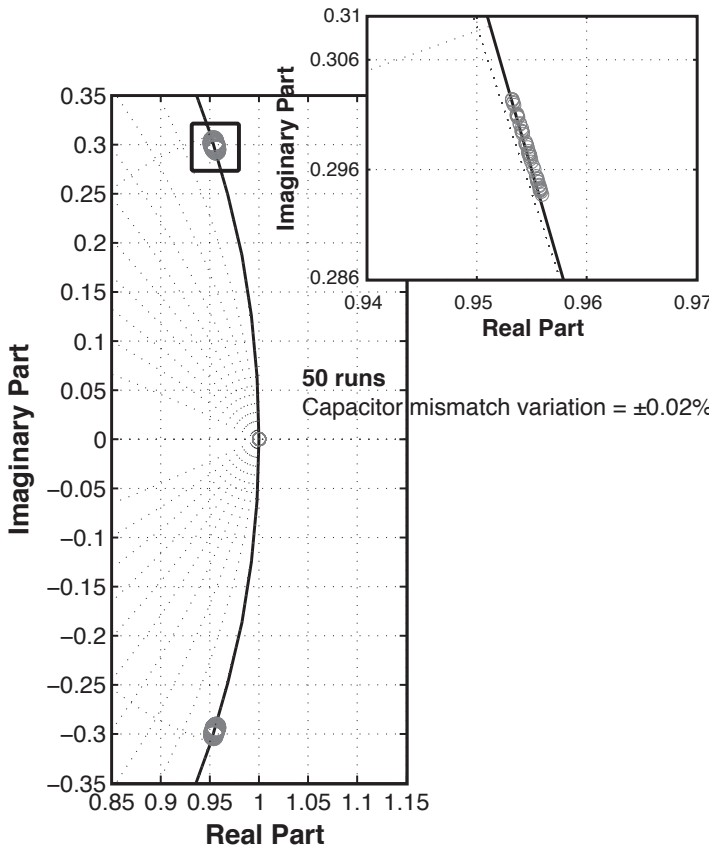
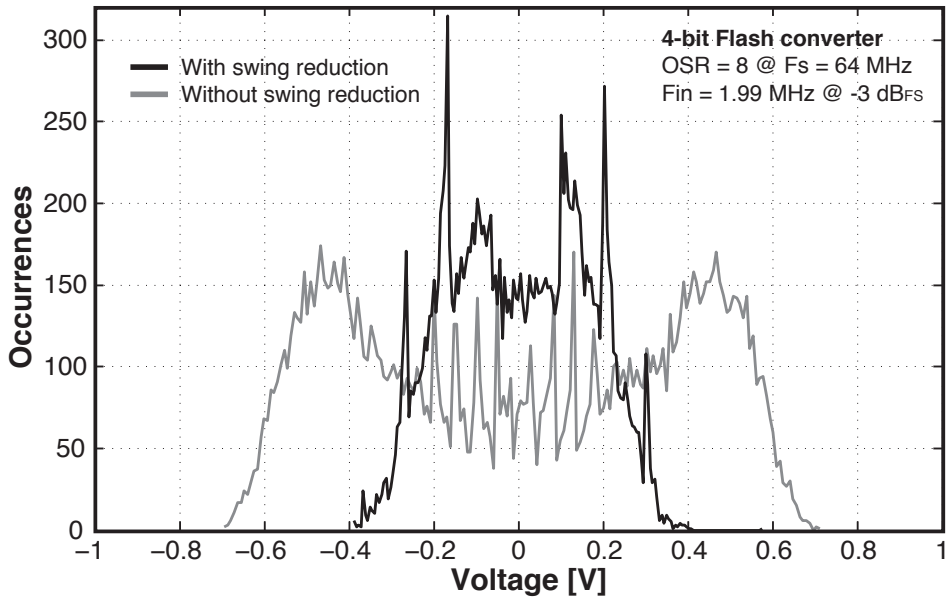
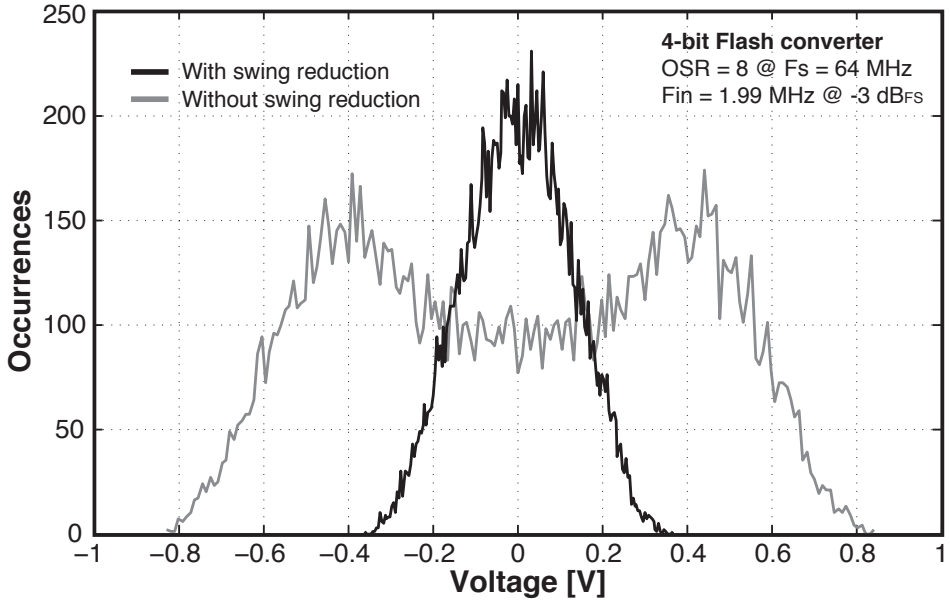


Figure 4.19: NTF zeros placement.



(a)



(b)

Figure 4.20: Simulated output voltage with and without digital swing reduction. (a) First integrator. (b) Second integrator.

Typical modern CMOS technologies ensure capacitors matching within $\pm 0.02\%$. Monte-carlo simulations (50 runs) obtain the root locus of equation (4.6), shown in Fig. 4.19. The mismatch minimally affects the position of the complex conjugate zeros.

Fig. 4.20 shows the output voltage swing of the first integrator and the following block when applying an input signal at -3 dB_{FS} at the upper limit of the bandwidth with and without swings reduction. The first and second output swings are reduced by about 43% (from 1.4 V_{P-P} to 0.8 V_{P-P}) and 56% (from 1.64 V_{P-P} to 0.73 V_{P-P}), respectively, thus demonstrating the effectiveness of the approach. Notice that the circuit implementation grants $z^{-1/2}$ delay for FLASH-2 operation. Moreover, since the swing of the second block is 56% of the full scale, the number of comparators of FLASH-1 goes down from 15 to 8.

The overall consumed power is reduced despite the need of 8 more comparators. The architecture spares the third op-amp (whose power need is about 50% of the first op-amp) and does not need more power on the second block.

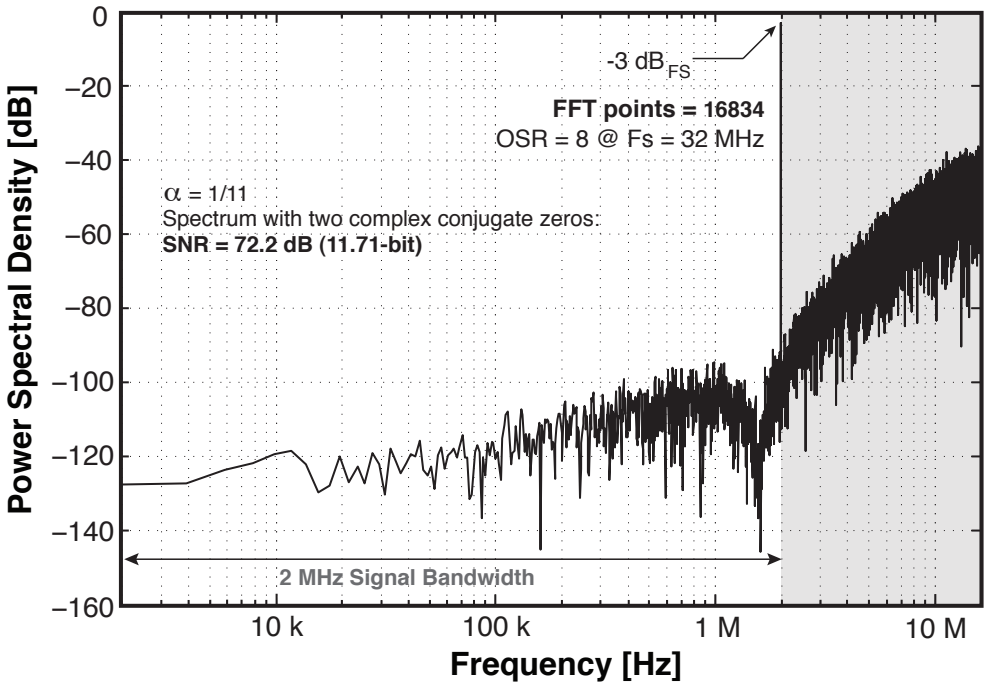


Figure 4.21: Simulated power spectral density of the proposed modulator.

Simulation results show that the use of op-amp with bandwidth and slew-rate equal to the ones of the first and second op-amps of a conventional counterpart obtains the noise spectrum of Fig. 4.21. With 4 bit flash and OSR = 8, the SNR with all NTF zeros at z = 1 is 64.1 dB. Making complex conjugate two zeros with α = 1/11 optimizes the SNR that becomes

72.2 dB. The simulation supposes a signal bandwidth of 2 MHz and amplifiers gain bandwidth product GBW_1 = GBW_2 = 64 MHz. The performance summary of the modulator is shown in Table 4.3.

Table 4.3: Summary Performance of the Proposed Modulator

Parameter	**Symbol [Unit]**	**Value**	
Clock Frequency	F_S [MHz]	32	
Oversampling Ratio	OSR [–]	8	
Signal Bandwidth	BW [MHz]	2	
Complex Conjugate Zeros Factor	α	1/11	0
Signal to Noise Ratio	SNR [dB]	72.2	64.1
Effective Number of Bits	ENoB [Bits]	11.71	10.35

Chapter 5

Conclusions

This thesis has been focused on the design of $\Sigma\Delta$ architectures well suitable for low power applications. The used design strategies (namely reduction of the number of op-amps and comparators as well as integrators output swing reduction) further reduce the overall power consumption of the modulators but keeping the desired noise shaping peformance. The measured power efficiency of two $\Sigma\Delta$ prototypes have been verified the effectiveness of the proposed architectures.

Two high-performance $\Sigma\Delta$ modulators have been proposed for wide band applications. Several simulation results at behavioral level have been done to verify the benefits of the architectures. Therefore, the main contributions of this thesis work can be divided in three parts.

5.1 Reduction of the Number of Op-amps.

The third-order $\Sigma\Delta$ modulator, explained in detail in Chapter 2, exploits suitable topological modifications in a conventional third-order modulator. The method eliminates one active sum in the loop filter leading an a final architecture with only two operational amplifiers. The called double integrator, resulted of these modifications, consist in a single integrator without delay with two extra feedback terms (one with single and another with double delay), that can be easily implemented with switched-capacitor structures. The measurement performance of the $\Sigma\Delta$ prototype, integrated in a 0.18-μm CMOS technology, leads a FoM (0.58 pJ/conv) well

suitable for Digital Video Broadcasting Handheld (DVB-H) requirements.

The proposed third-order $\Sigma\Delta$ modulator, described in Chapter 3, benefits the power consumption by using a conventional second-order $\Sigma\Delta$ modulator. A properly injection of shaped quantization noise at the input of the second integrator boost the noise shaping performance from second to third-order. The additional enhancer block, which process the quantization noise, is obtained from the synthesis of the given third-order noise shaping. Furthermore, the modulator saves one integrator by employing a single operational amplifier working in a multiplexed operation. Fabricated in a 0.18-μm CMOS technology, the $\Sigma\Delta$ prototype targets the low power requirements of wireless sensor networks.

5.2 Integrators Output Swing Reduction.

Minimizing the op-amp output swing in $\Sigma\Delta$ modulators brings several advantages that secure consumed low power. Operation at low power supply voltages, better linearity and relaxed bandwidth and slew-rate requirements, are the main characteristics obtained from this feature. The prototypes of Chapter 2 and Chapter 3 employ feedforward solution, to limit at the quantization noise level, the output swing of the first integrator. The Analog Look Ahead (ALA) second-order $\Sigma\Delta$ architecture presented in Chapter 4, uses the same approach for reducing the output swing in both integrators at expenses of an additional summing block before the quantizer. This active (or passive) addition however, is exploited by the architecture since the proposed method ALA provide an extra clock period for the quantization process. The ALA $\Sigma\Delta$ modulator has been proposed to solve the critical timing constraint in double sampling schemes.

The good correlation between two successive flash input samples benefits not only the output swing reduction at the output of the second integrator but also allows the reduction of the number of comparators needed in the flash. With this approach the flash saves by almost 40$\%$ its power consumption. In particular, for a 5 bit quantizer the required number of comparators are only 18 instead of 32 while for a 3 bit quantizer the number of comparators decreases from 7 to 4. The former case was verified in the two $\Sigma\Delta$ prototypes and at behavioral level in the second architecture of Chapter 4. The second case was simulated at behavioral level in the first architecture described in Chapter 4.

5.3 Noise Shaping Enhancement.

High resolution $\Sigma\Delta$ architectures are more and more addressed for wide-band portable communication systems because taking advantage of the noise shaping. Moreover low power consumption is an a critical issue to keep for long time the battery life. The second modulator

of Chapter 4 meet all these features since it attains high resolution by exploiting complex conjugate NTF zeros and uses a fully digital feedforward path to reduce the amplifiers output swing. The latter feature adds quantization noise into the loop filter given by the additional flash converter, however it is eliminated at the output of the modulator in the digital domain. The proposed architecture employs two operational amplifier and achieves an enhanced third-order noise transfer function by placing a zero at z = 1 and two complex ones with imaginary part α/2. Simulations results at behavioral level shows that the proposed architecture obtains an improvement of the SNR by almost 8 dB. Moreover, Montecarlo simulations with capacitor mismatch of $\pm$0.02$\%$ demonstrate a minimum effect in the position of the complex conjugate zeros. Finally, the output swing of the first integrator is reduced by almost 43$\%$ while the second integrator output swing improves by approximately 56$\%$.

Appendix A

Layout Description

The additional material presented in this appendix, aims to show the layout description of the main blocks used to implement the power-efficiency $\Sigma\Delta$ prototypes of Chapter 2 and Chapter 3. The first layout corresponds to the design of a third-order $\Sigma\Delta$ modulator suitable for Digital Video Broadcasting-Handheld (DVB-H) applications. The second layout describes the design of a third-order $\Sigma\Delta$ modulator capable to meet the low power design specifications of wireless sensor networks. The layout of the switched-capacitor (SC) implementation of the integrators as well as the different analog and digital blocks involved in the design of the two prototypes are shown in detail. Furthermore, the schematic circuits of the amplifiers and comparators (including dimension of the transistors) are also included.

A.1 First Layout Description (1LD).

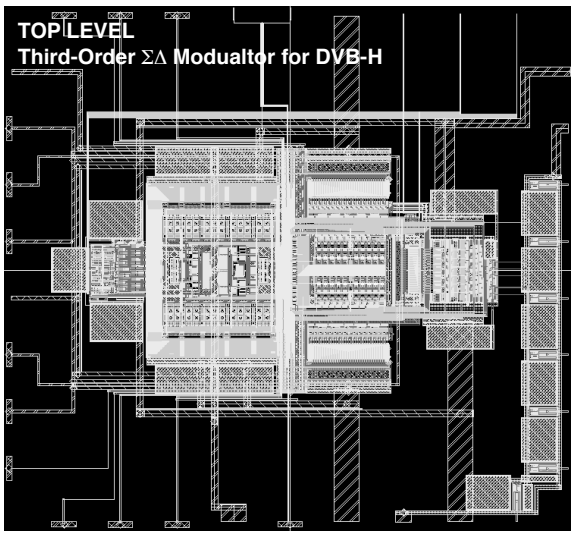


Figure A.1: 1LD. Top level of the ΣΔ modulator without padring.

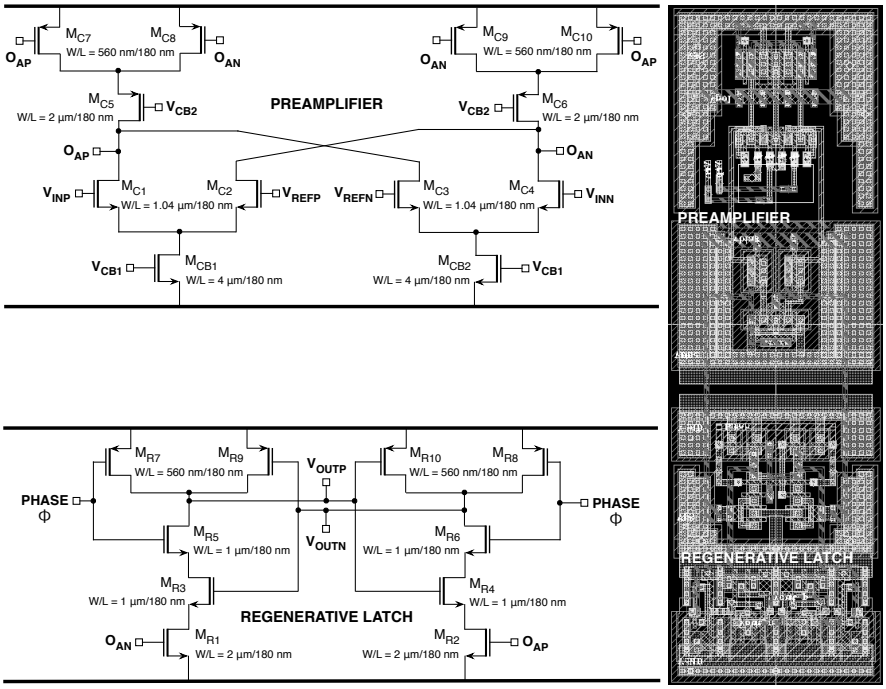
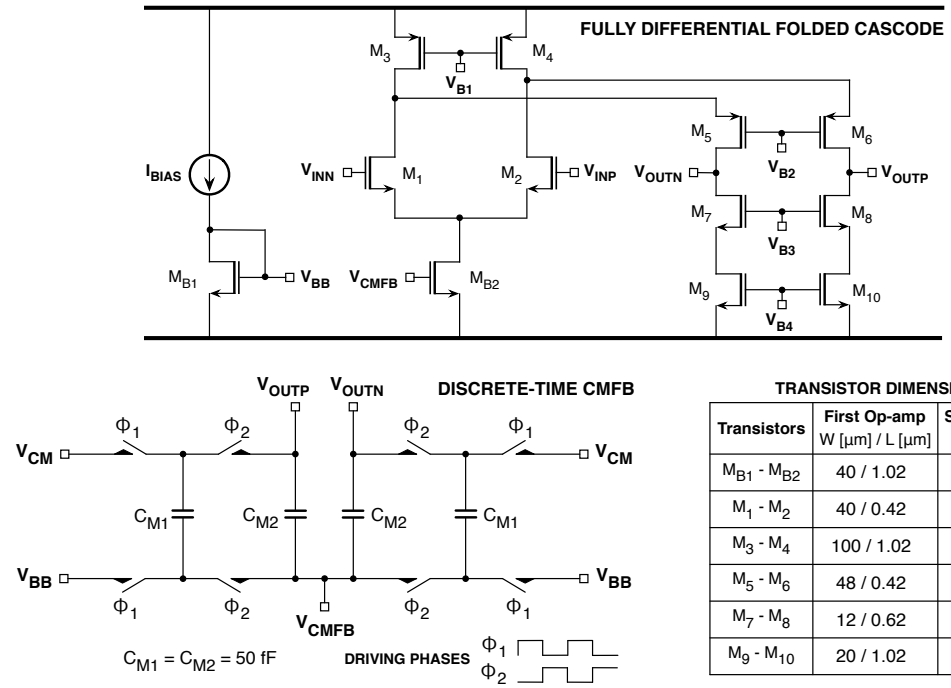


Figure A.2: 1LD. Preamplifier and regenerative latch of the comparator.



TRANSISTOR DIMENSIONS

Transistors	First Op-amp W [µm] / L [µm]	Second Op-amp W [µm] / L [µm]
M_{B1} - M_{B2}	40 / 1.02	80 / 0.82
M_1 - M_2	40 / 0.42	120 / 0.22
M_3 - M_4	100 / 1.02	180 / 1.02
M_5 - M_6	48 / 0.42	48 / 0.42
M_7 - M_8	12 / 0.62	40 / 0.82
M_9 - M_{10}	20 / 1.02	20 / 0.82

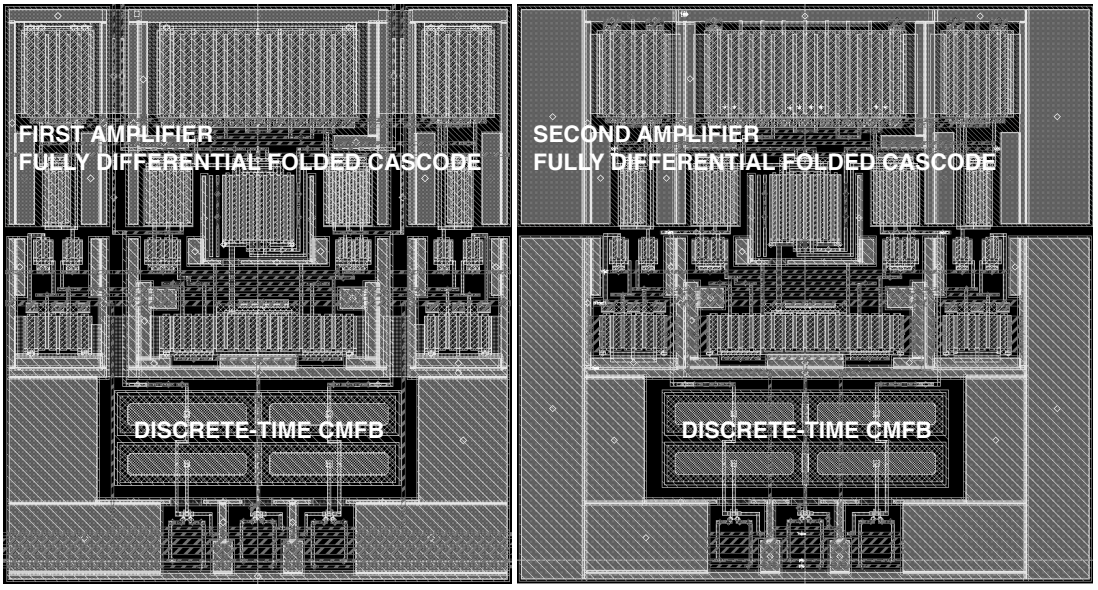


Figure A.3: 1LD. Fully differential folded cascode amplifiers with Discrete-Time CMFB.

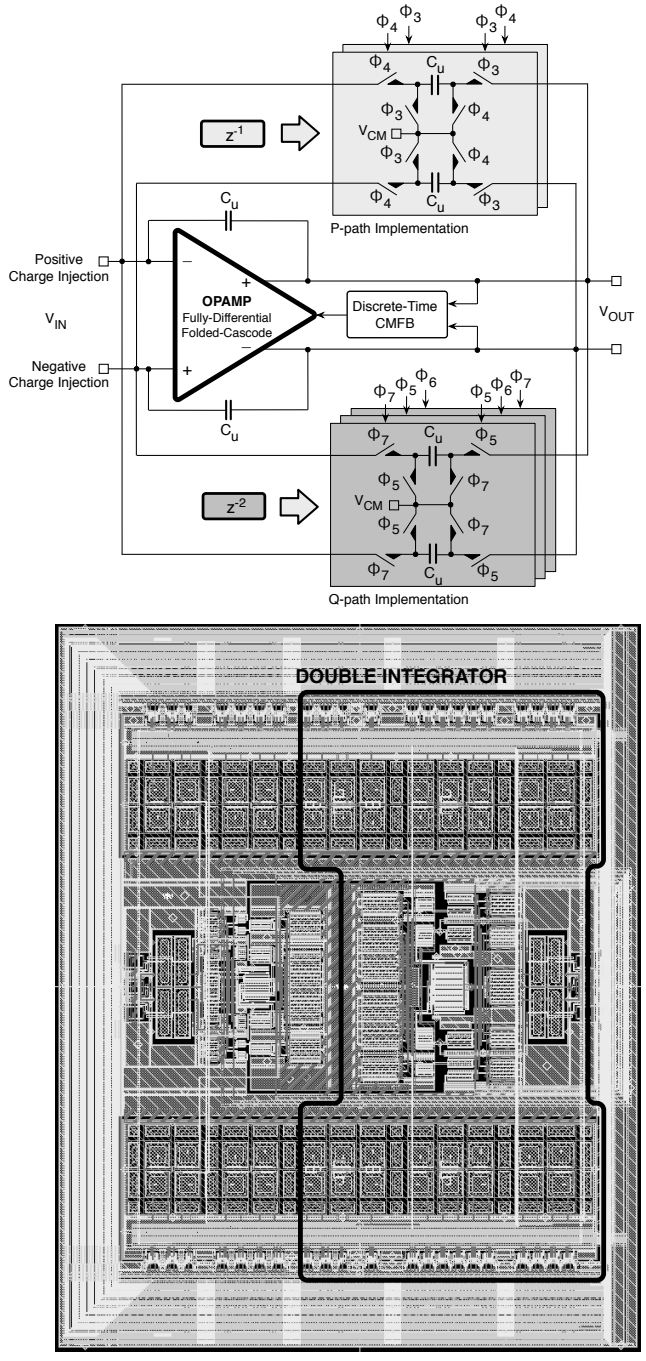


Figure A.4: 1LD. Switched capacitor (SC) implementation of the double integrator. The layout of the first integrator is also shown.

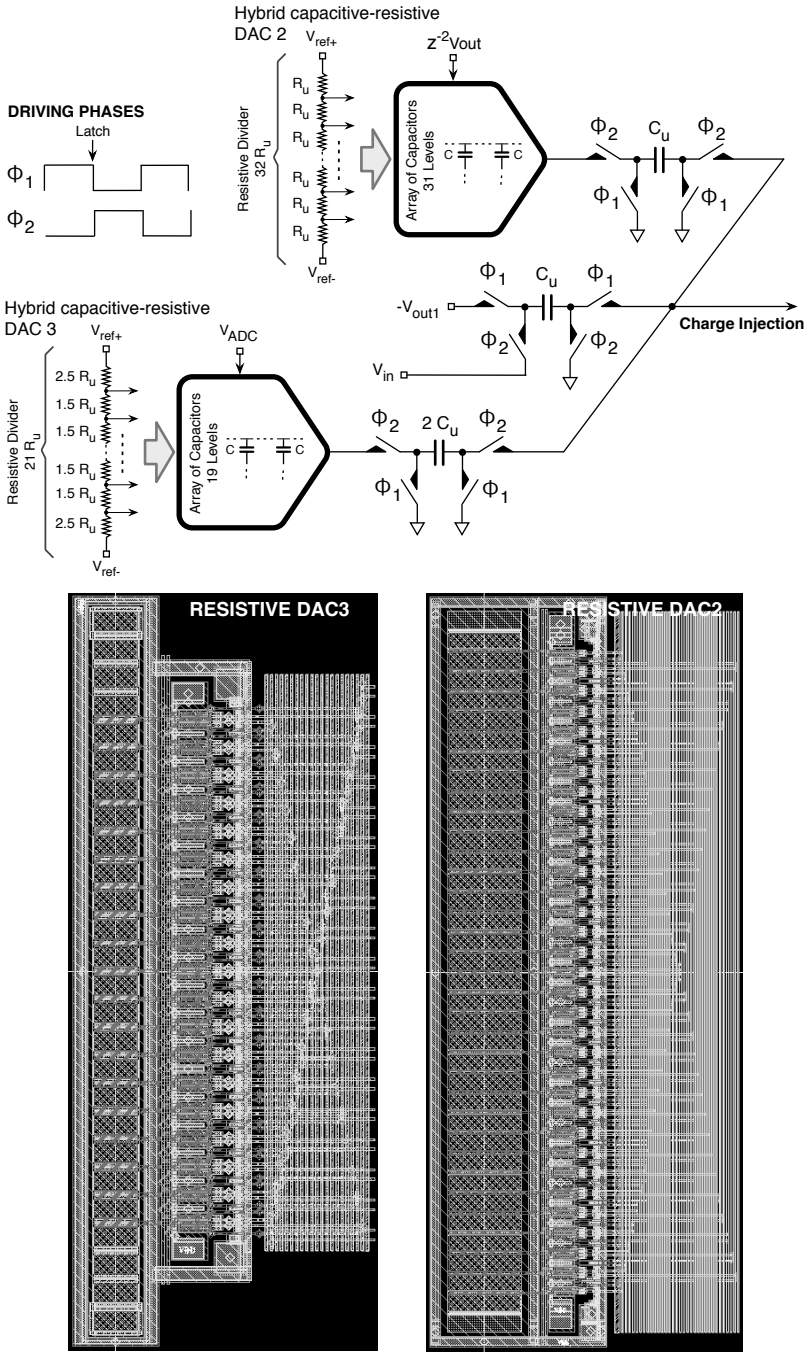


Figure A.5: 1LD. Implementation of DAC2 and DAC3. Switched-capacitor (SC) networks are not included.

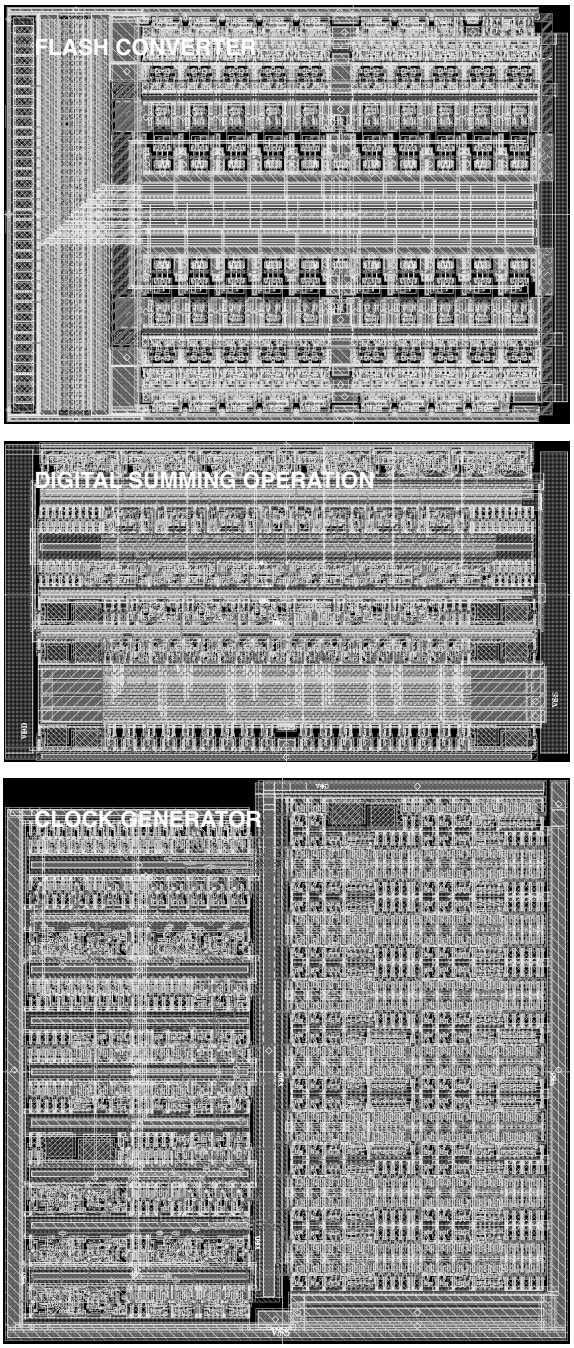


Figure A.6: 1LD. Complementary layout circuits: flash converter, digital summing operation and clock generator.

A.2 Second Layout Description (2LD).

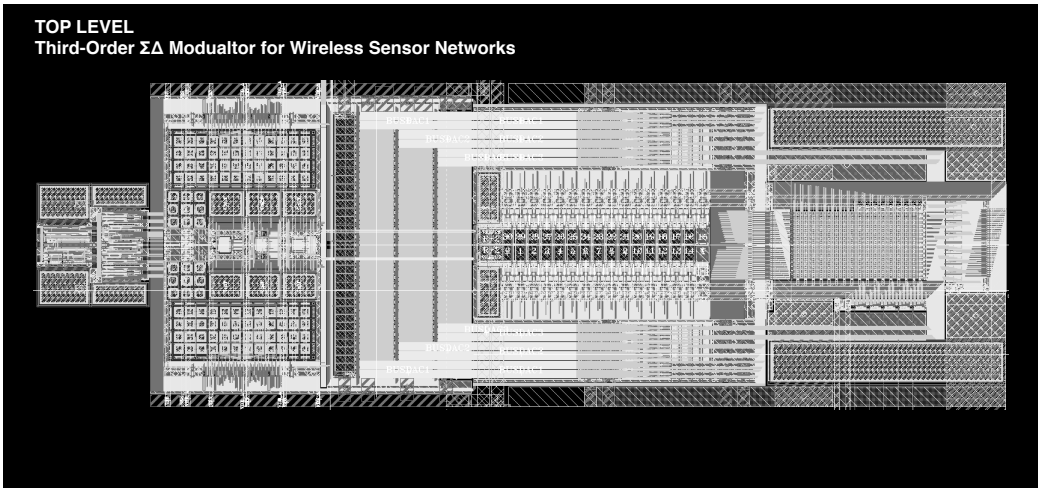


Figure A.7: 2LD. Top level without padring of the third-order $\Sigma\Delta$ modulator.

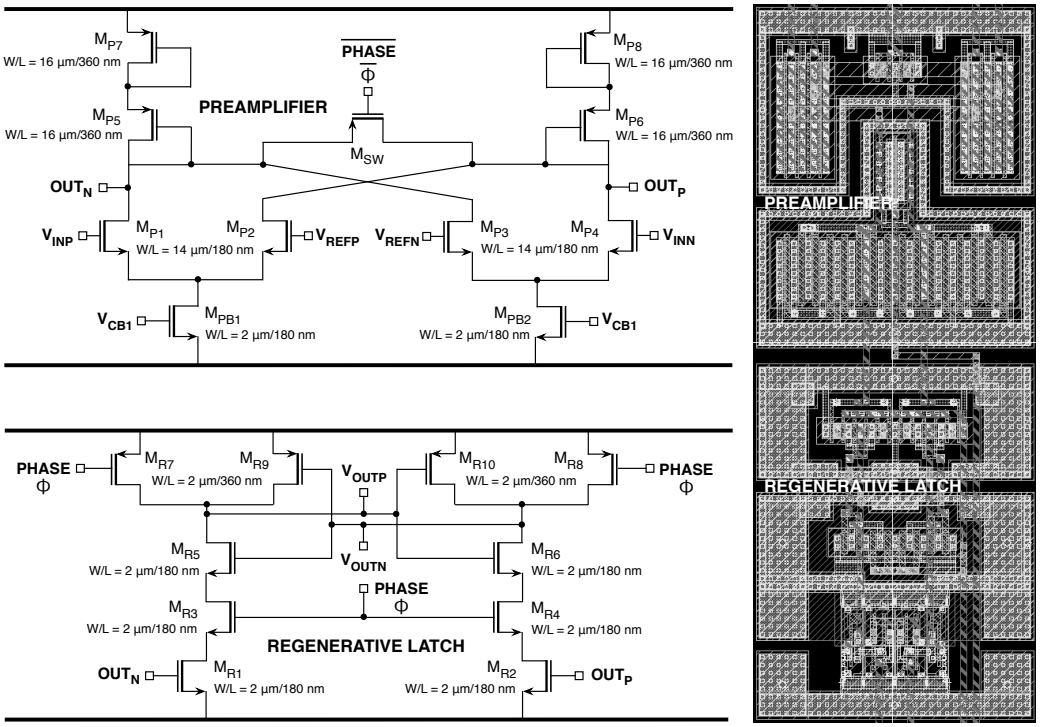
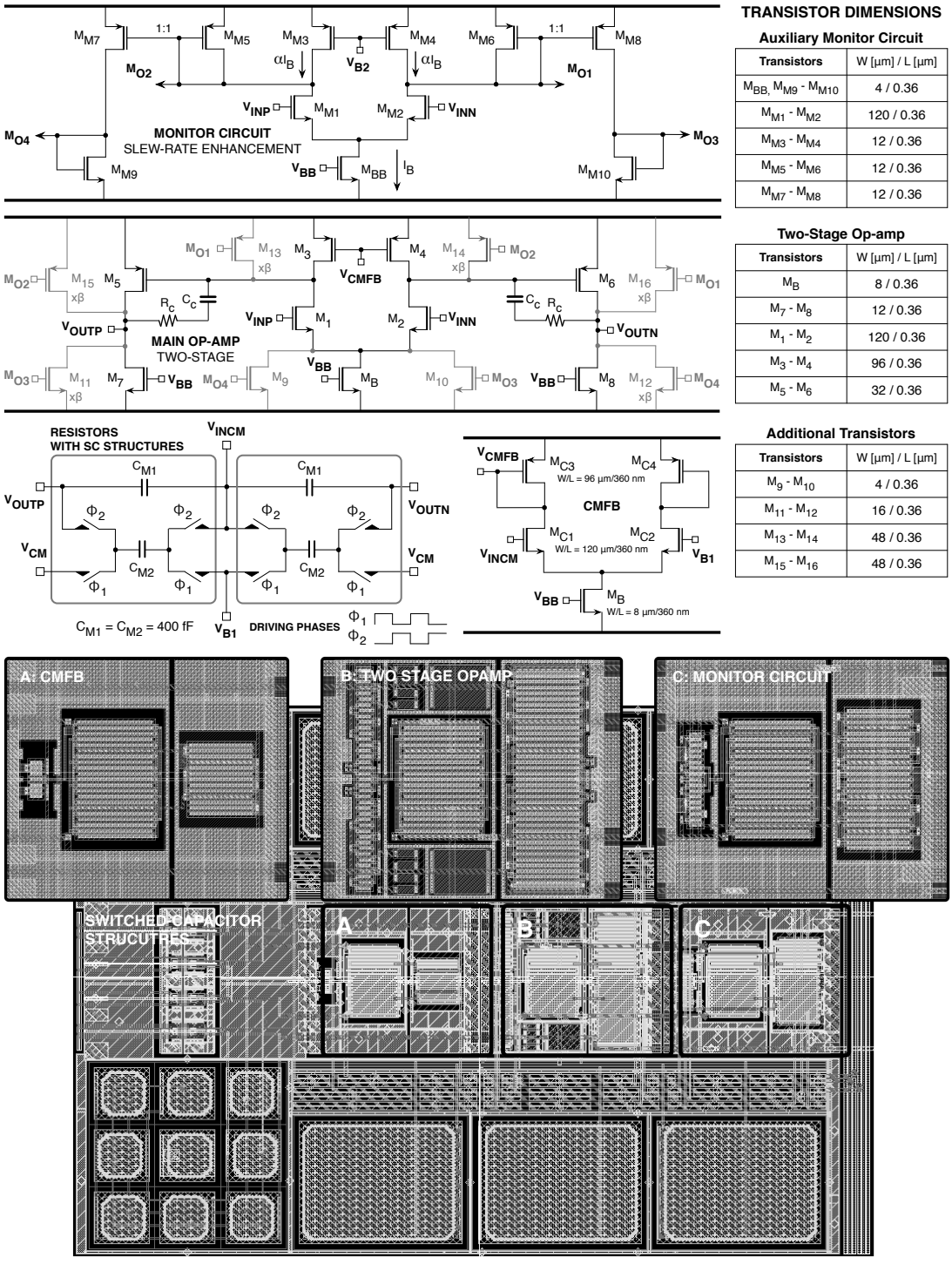


Figure A.8: 2LD. Comparator schematic with preamplifier and regenerative latch.



TRANSISTOR DIMENSIONS

Auxiliary Monitor Circuit

Transistors	W [µm] / L [µm]
M_{BB}, M_{M9} - M_{M10}	4 / 0.36
M_{M1} - M_{M2}	120 / 0.36
M_{M3} - M_{M4}	12 / 0.36
M_{M5} - M_{M6}	12 / 0.36
M_{M7} - M_{M8}	12 / 0.36

Two-Stage Op-amp

Transistors	W [µm] / L [µm]
M_B	8 / 0.36
M_7 - M_8	12 / 0.36
M_1 - M_2	120 / 0.36
M_3 - M_4	96 / 0.36
M_5 - M_6	32 / 0.36

Additional Transistors

Transistors	W [µm] / L [µm]
M_9 - M_{10}	4 / 0.36
M_{11} - M_{12}	16 / 0.36
M_{13} - M_{14}	48 / 0.36
M_{15} - M_{16}	48 / 0.36

Figure A.9: 1LD. Complete operational amplifier with auxiliary monitor circuit and CMFB.

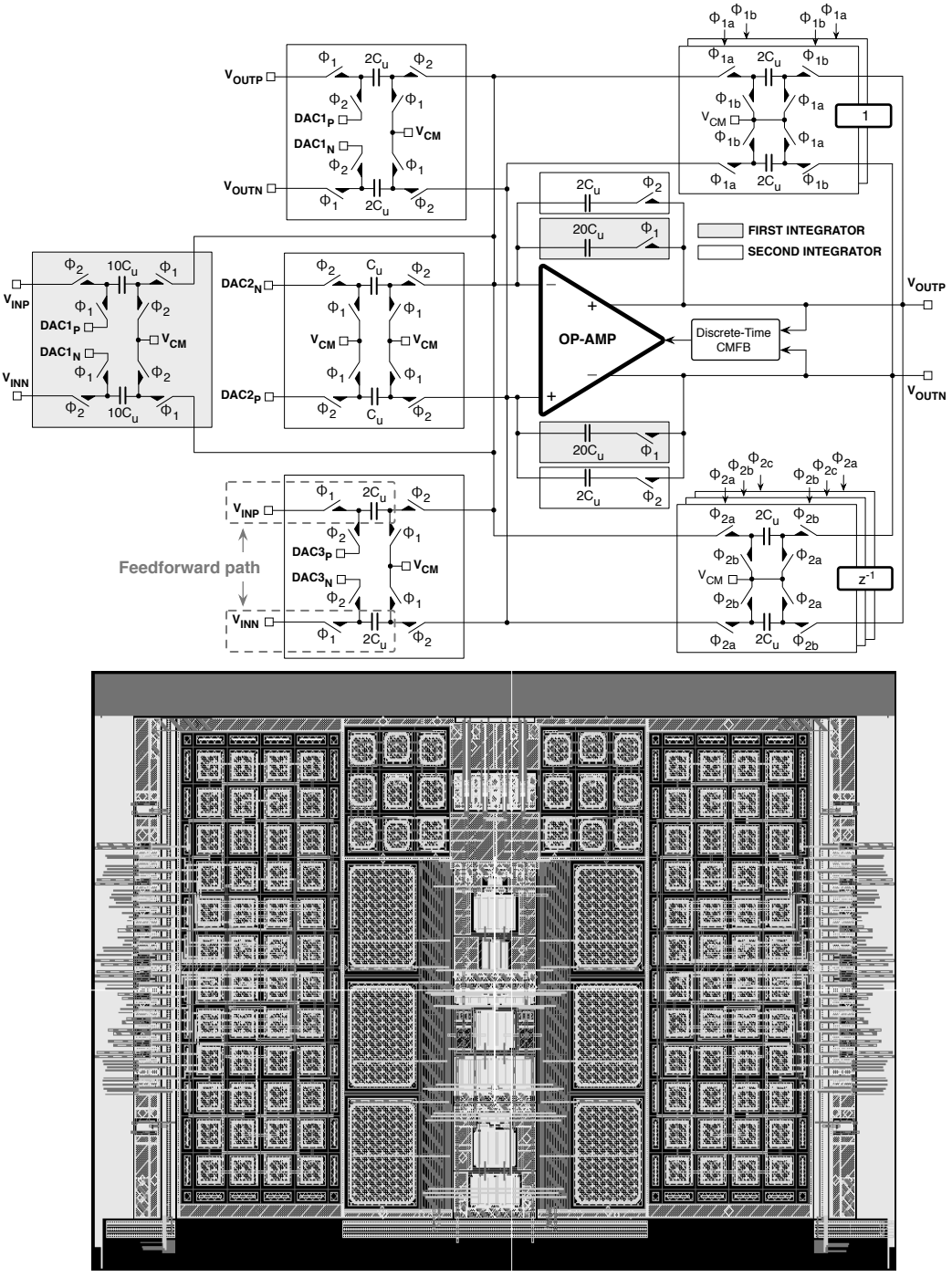


Figure A.10: 2LD. Fully differential switched-capacitor (SC) implementation of the first and second integrator.

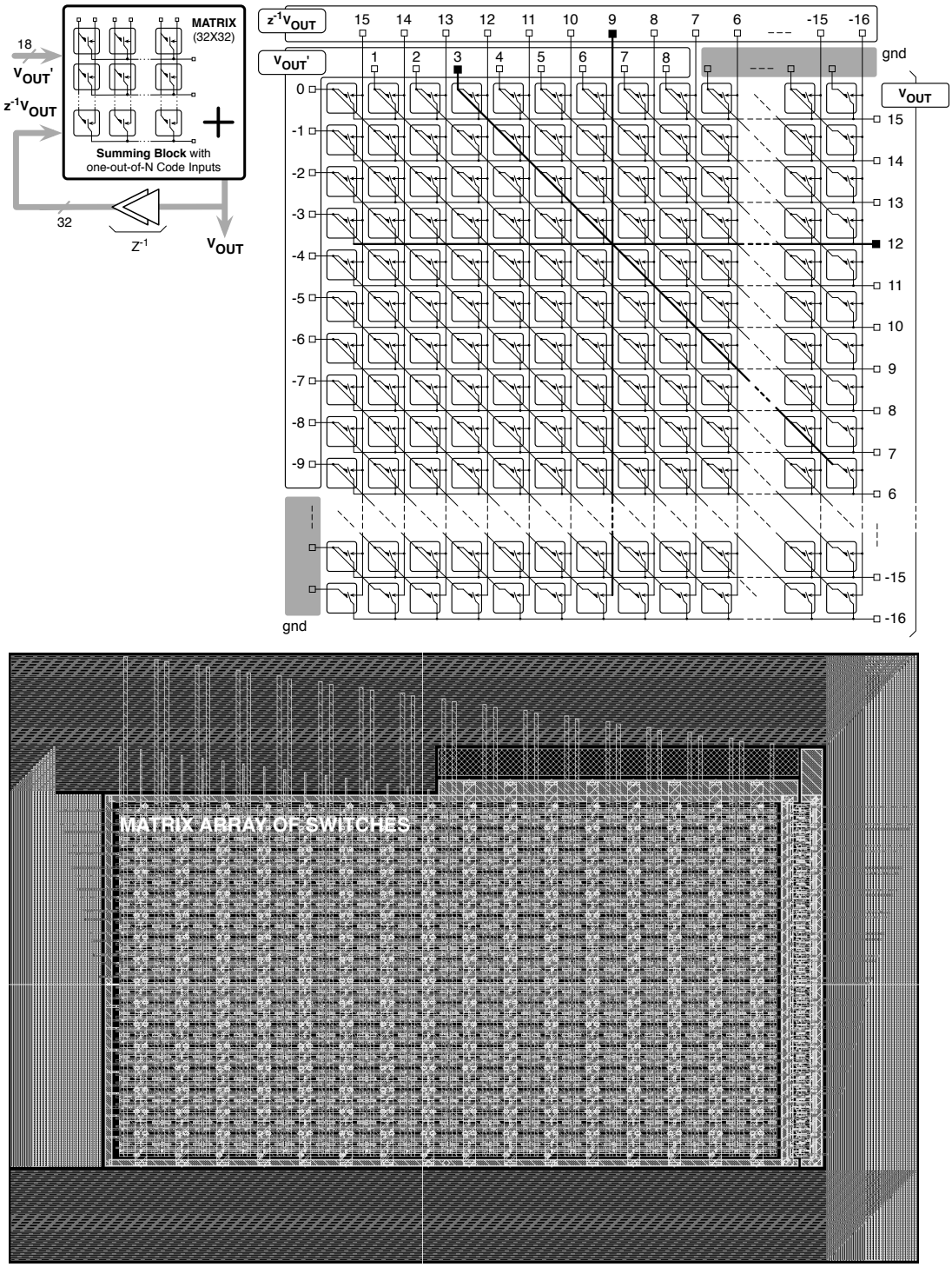


Figure A.11: 2LD. Matrix array used for implement the digital summing block at the output of the modulator.

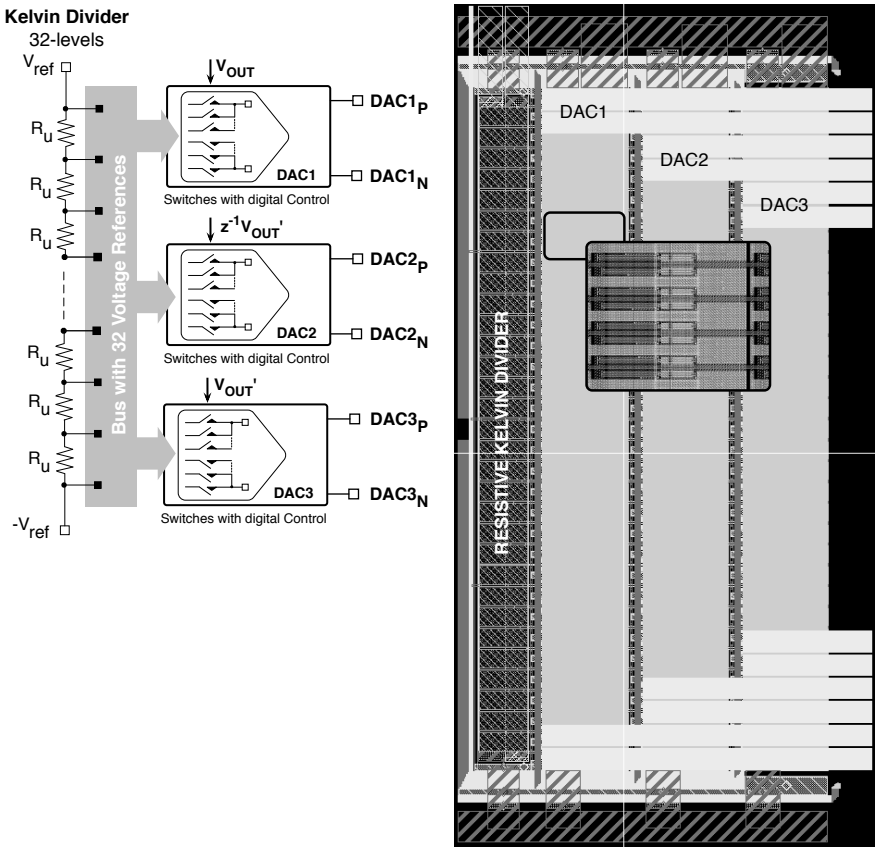


Figure A.12: 2LD. Single Kelvin divider that implements three DACs.

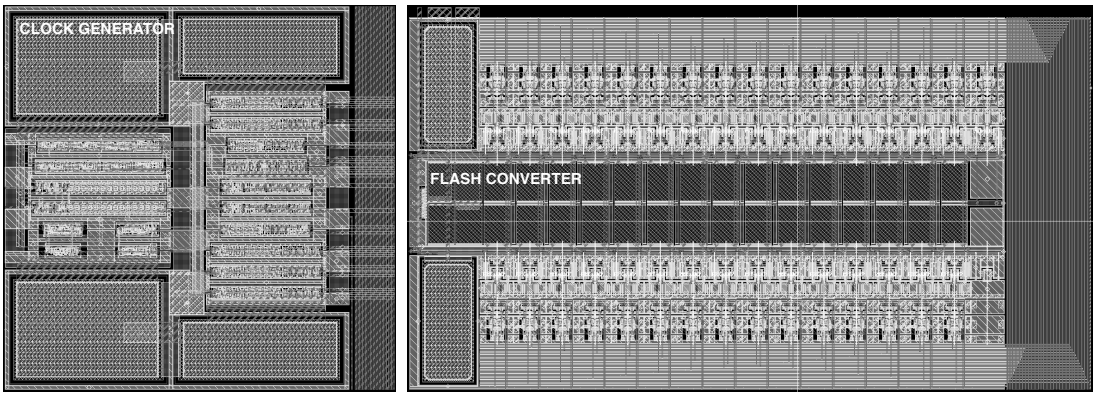


Figure A.13: 2LD. Complementary layout circuits: clock generator and flash converter.

Appendix B

PCB Design Considerations

The PCB (Printed Circuit Board) used for validating and, more important, for testing data converters must be carefully designed to preserve the quality of the parameters being measured and to avoid false errors that hamper the results. The design of the interface board requires good design techniques such proper signal routing, decoupling, and grounding when measuring Signal-to-Noise-and-Distortion-Ratio (SNDR), Spurious-Free-Dynamic-Range (SFDR) and other dynamic features in data converters with conversion rates of hundreds of MS/s. The ADC evaluation board generally contain an on-board low-jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference. The purpose of this appendix, is to provide to the designer some practical layout recommendations to avoid inaccuracies in the PCB that can totally mask the performance of the involved integrated circuits. The appendix also contains the layout of the evaluation boards used in the experimental setup of the two $\Sigma\Delta$ prototypes explained in Chapter 2 and Chapter 3.

B.1 Driving the Analog Inputs.

Differential modes of operation with either an ac or dc input provide the best THD performance over a wide frequency range [11], [43]. Since not all applications have a signal preconditioned for differential operation, there is often a need to perform single-ended-to-differential conversion. Differential inputs allow much improvement in performance on-chip as signals are

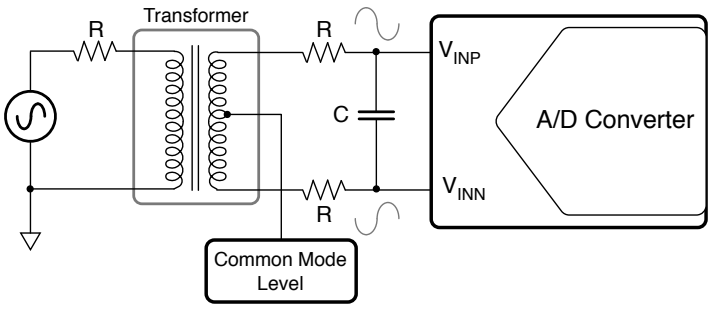


Figure B.1: Using an RF transformer to generate differential inputs.

processed through attenuation and gain stages. Most of the improvement is a result of differential analog stages having high rejection of even order harmonics. There are also benefits at the PCB level [67]. First, differential inputs have high common mode rejection to stray signals such as ground and power noise. Also, they provide good rejection to common mode signals such as a local oscillator feed-through.

In systems that do not need to be dc-coupled, an RF transformer [68], [69] with a center tap offers a good solution to perform a single-ended-to-differential conversion (and vice versa). Transformers also can perform the additional functions of galvanic isolation, step-up or step-down of voltages, and impedance transformation. For these reasons, transformers will always find uses in certain applications [67]. Fig. B.1 shows how a transformer is used for single-ended-to-differential conversion [70], [71], [72].

It provides the benefits of operating the ADC in the differential mode without contributing additional noise and distortion. The center tap is used to shift the differential signal to the common-mode level required. An RF transformer also has the benefit of providing electrical isolation between the signal source and the ADC.

Another alternative method of applying differential drive to the converter is to use a differential amplifier, such as the AD8138 [73]. The AD8138 can be used in applications where dc coupling is required and can be operated as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. The AD8138 is as easy to use as an op amp, and greatly simplifies differential signal amplification and driving. Fig. B.2 shows the typical application circuit of the AD8138 [70], [71], [73] in a single-ended-to-differential amplifier configuration. The differential outputs of the AD8138 helps balance the input-to-differential ADCs, maximizing the performance of the ADC.

Moreover, the AD8138 eliminates the need for a transformer with high performance ADCs, preserving the low frequency and dc information. The positive and negative outputs of the amplifier are connected to the respective inputs on the converter with a pair of series resistors to minimize the effects of switched capacitance on the front end of the converter.

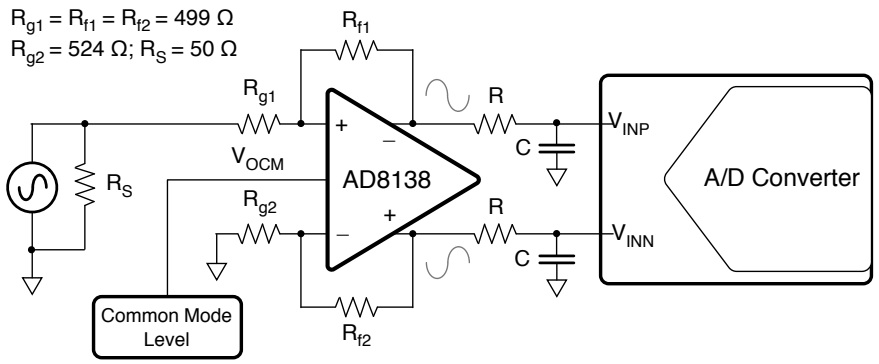


Figure B.2: Using the AD8138 as a Single-Ended-to-Differential Amplifier.

The RC low-pass filter on each analog input (mounted as close to the converter as possible) is recommended in ac applications to remove the high frequency components of the analog input. The architecture of the AD8138 results in outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. If the analog input source being used has zero impedance, then all four resistors (R_{f1}, R_{f2}, R_{g1} and R_{g2}) should be the same. If the source has a 50 Ω impedance and a 50 Ω termination (see Fig. B.2), for example, the value of Rg2 should be increased by 25 Ω to balance this parallel impedance on the input and thus ensure that both the positive and negative analog inputs have the same gain [73].

B.2 Low and High Frequency Decoupling.

The power supply pins should be bypassed as close as possible to the device to the nearby ground plane. The power supply traces should be as a large as possible (approximately $3\ mm$ wide or more) to provide low impedance paths and reduce the effects of glitches on the power supply line [72]. Good surface-mount high frequency ceramic chip capacitors should be used to achieve minimum trace length, low impedance, and low parasitic capacitance. This bypassing should be done with a capacitance value of $0.01\ \mu F$ to $0.1\ \mu F$ for each supply [71], [70]. Further away, low frequency bypassing should be provided with $10\ \mu F$ electrolytic capacitors from each supply to ground. At each individual analog stage, further local, high-frequency-only filtering is required at the individual IC package power pins.

Fig. B.3 shows in both correct (left) as well as incorrect example (right) of supply filter implementations [67]. In the left example, a typical $0.1\ \mu F$ chip ceramic capacitor goes directly to the opposite PCB side ground plane, by virtue of the via, and on to the ICs GND pin by a second via. In contrast, the less desirable setup at the right adds additional PCB trace

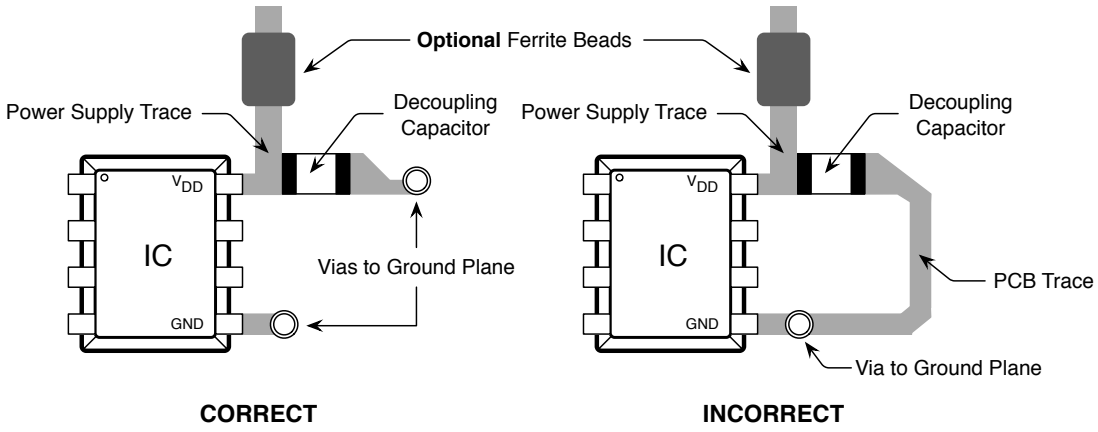


Figure B.3: Power supply filter implementation.

inductance in the ground path of the decoupling capacitor, reducing effectiveness. All high frequency (i.e., $\geq$10 MHz) ICs should use a bypassing scheme similar to Fig. B.3 for best performance. The ferrite beads are not 100$\%$ necessary, but they will add extra high frequency noise isolation and decoupling, which is often desirable

The signal routing should be short and direct in order to avoid parasitic effects. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This will reduce the radiated energy and make the circuit less susceptible to interference.

B.3 Double-Sided Vs. Multilayer PCBs.

Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved. The ground layer should be checked carefully to make sure there are no isolated ground because IC ground pins located in this zones have no current return path to the ground plane. In the other hand, auto-routing board layout techniques will generally lead to a layout disaster on a mixed-signal board, so manual intervention is highly recommended.

Systems that are densely packed with surface mount ICs will have a large number of interconnections; therefore multilayer boards are mandatory. This allows at least one complete layer to be dedicated to ground. As shown in Fig. B.4, a simple 4-layer board would have

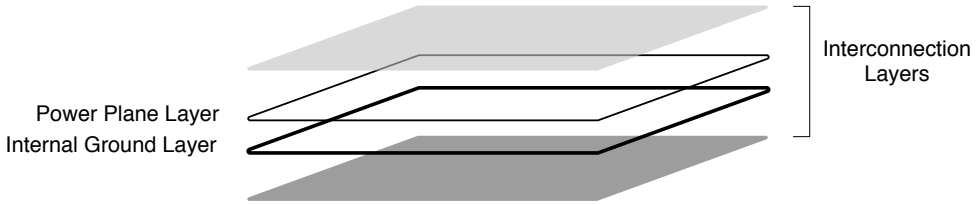


Figure B.4: Multilayer board. Conceptual 4-layer example.

internal ground and power plane layers with the outer two layers used for interconnections between the surface mount components. Placing the power and ground planes adjacent to each other provides additional inter-plane capacitance which helps high frequency decoupling of the power supply and ensure highest level of signal integrity [11], [67].

B.4 Separating Analog and Digital Ground Planes.

In mixed-signal systems such data converters, it is highly desirable to physically separate sensitive analog components from noisy digital components. Separate power supplies for analog and digital circuits are also highly desirable, even if the voltages are the same. It may also be beneficial to use separate ground planes for the analog and the digital circuitry. These planes should not overlap in order to minimize capacitive coupling between the two. It is then further recommended that the analog ground (AGND) and digital ground (DGND) pins of a converter be tied together and that the analog ground and digital ground planes be connected at that same point as shown in Fig. B.5 [67]. This essentially creates the system *star* ground at the mixed-signal device.

With this approach all noisy digital currents are isolated from the sensitive analog section of the board. However, for systems that have several ADCs or DACs on different PCBs (or on

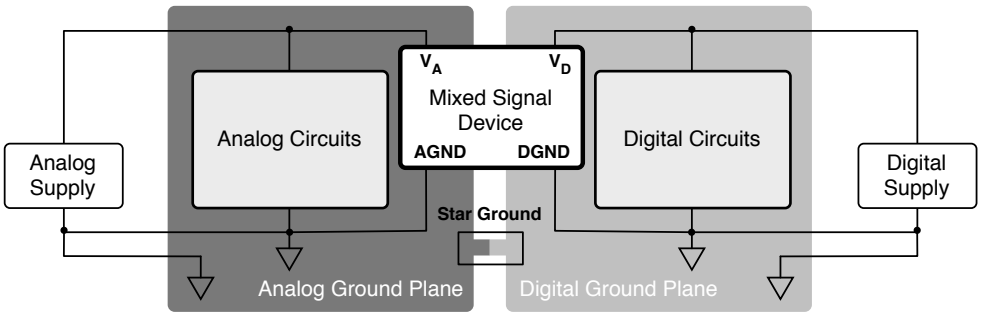


Figure B.5: Grounding mixed signal ICs: the analog ground and digital ground planes are connected at that same point.

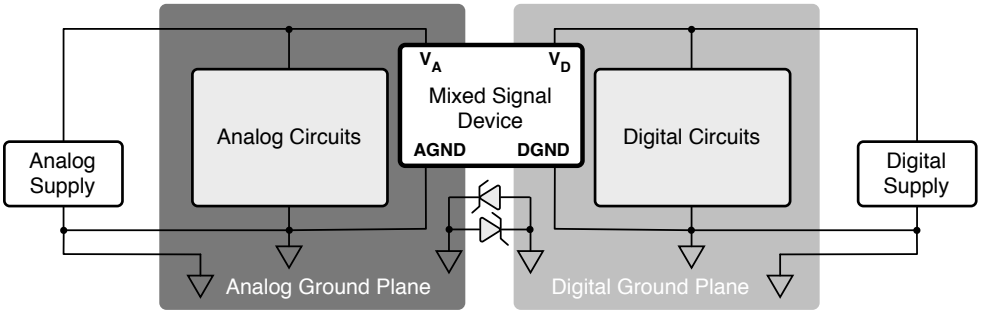


Figure B.6: Grounding alternative: the back-to-back Schottky diodes connect the analog ground and digital ground planes.

the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point *star* ground system impossible.

Fig. B.6 shows optional Schottky diodes in back-to-back configuration for connect the analog and digital ground planes [67]. The Schottky diodes are preferable because of their low capacitance and low forward voltage drop. The low capacitance prevents ac coupling between the analog and digital ground planes. Moreover, these devices prevent large dc voltages or low frequency voltage spikes from developing across the two planes. These voltages can potentially damage the mixed signal IC if they exceed 300 mV because they appear directly between the AGND and DGND pins. As an alternative to the back-to-back Schottky diodes, a ferrite bead provides a dc connection between the two planes but isolates them at frequencies above a few MHz where the ferrite bead becomes resistive. This protects the IC from dc voltages between AGND and DGND, but the dc connection provided by the ferrite bead can introduce unwanted dc ground loops and may not be suitable for high resolution systems.

B.5 Clock Signal and Final Considerations.

Fast switching signals, such as the clock signal, should be shielded with digital ground to avoid radiating noise to other sections of the board [11]. In many cases, the clock signal is derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. Thus, it is extremely important route high speed digital signal traces well away from all the sensitive analog traces.

There are a number of important points to be considered when making signal and power connections. First, the noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals.

Second, the ground plane can act as a shield where sensitive signals cross. Thus, all sensitive areas must be isolated from each other and signal paths are placed as short as possible avoiding 90 degree turns. Finally, multiple ground pins are important because keep down the ground impedance at the junction between the board and the ground planes.

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC PC board in the system. The actual evaluation board layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files). In many cases, the layout of the various layers appears on the data sheet for the device.

B.6 Evaluation Board Layouts.

The main purpose of this section is to show the layout of the multilayer evaluation boards used for the experimental results of the two $\Sigma\Delta$ prototypes presented in Chapter 2 and Chapter 3. The PCBs have been designed by following the practical recommendations described above. The schematic circuit as well as every layer level of each board are highlighted.

The first evaluation board (EB1) has been used for testing a third-order $\Sigma\Delta$ modulator which targets DVB-H applications. The second evaluation board (EB2) was designed for testing a third-order $\Sigma\Delta$ modulator, implemented with only one operational amplifier, that accomplishes the wireless sensor network specifications.

B.6.1 First Evaluation Board (1EB).

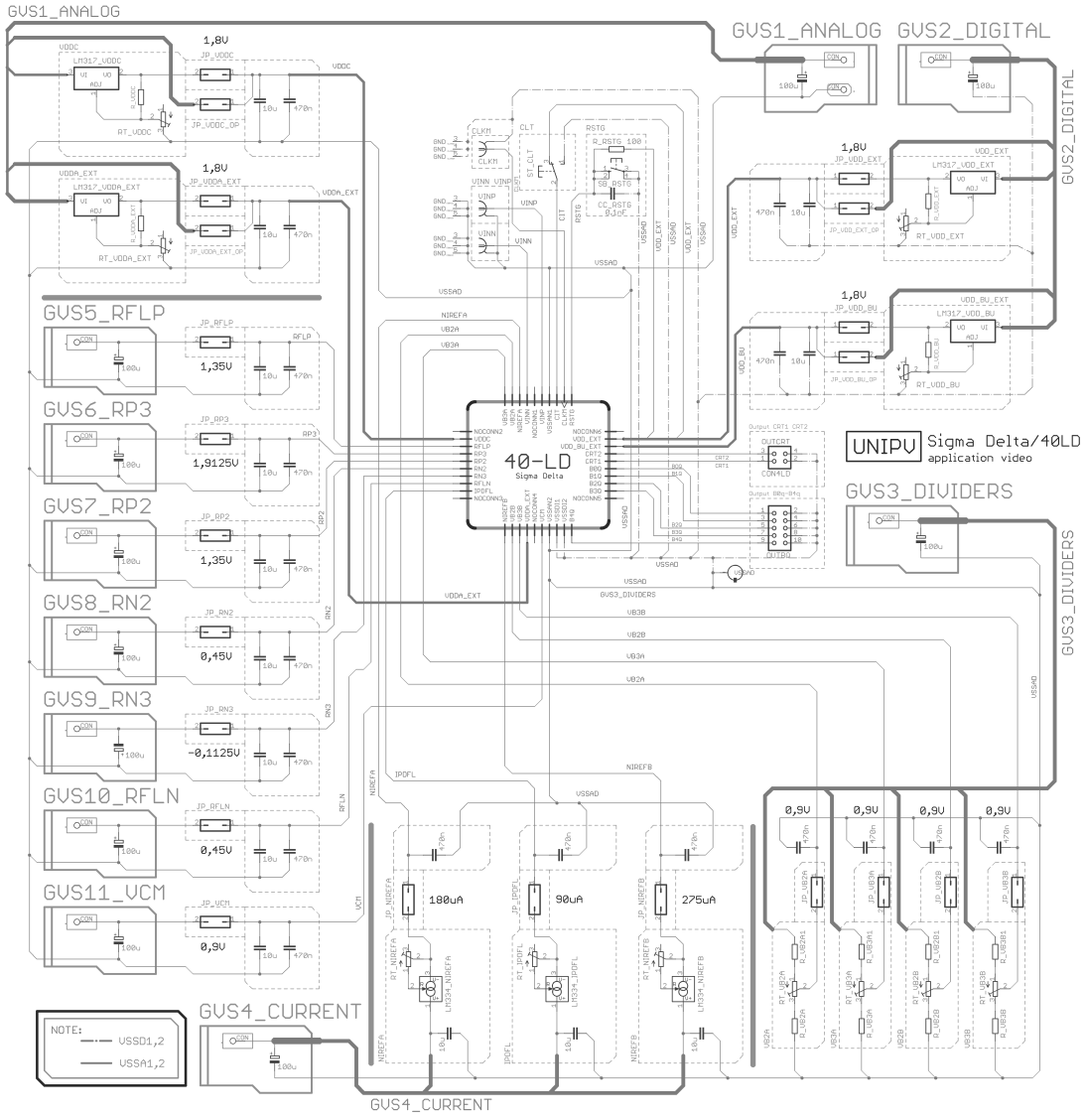


Figure B.7: 1EB. Evaluation board schematic. Test board of a third-order $\Sigma\Delta$ modulator for DVB-H applications.

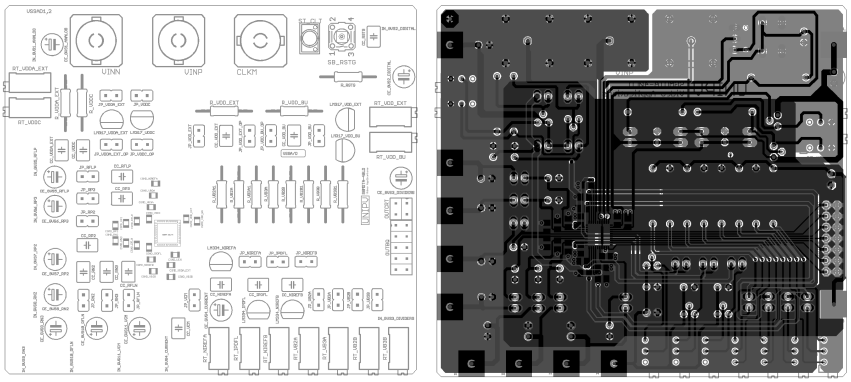


Figure B.8: 1EB. Silkscreen layer (Left) and all layers (right).

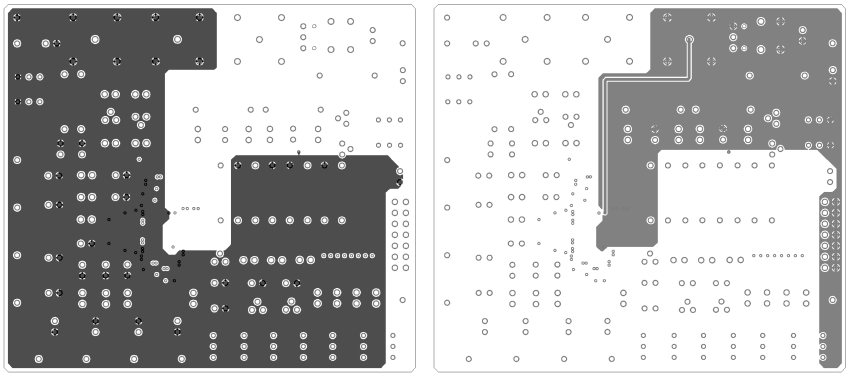


Figure B.9: 1EB. Analog (left) and digital (right) ground plane Layers.

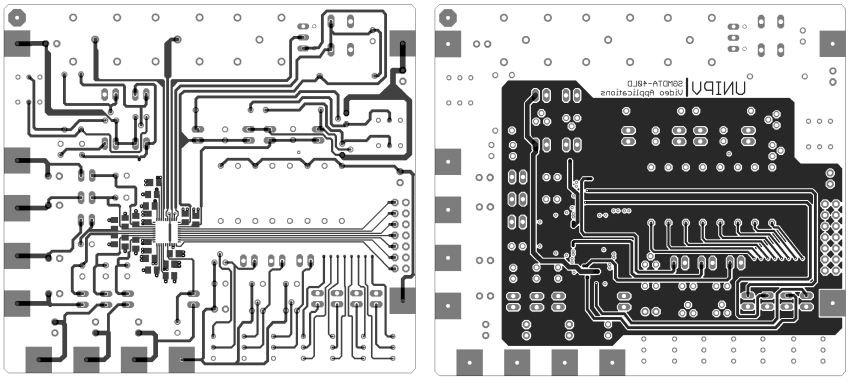


Figure B.10: 1EB. Top signal level (left) and bottom signal level (right).

B.6.2 Second Evaluation Board (2EB).

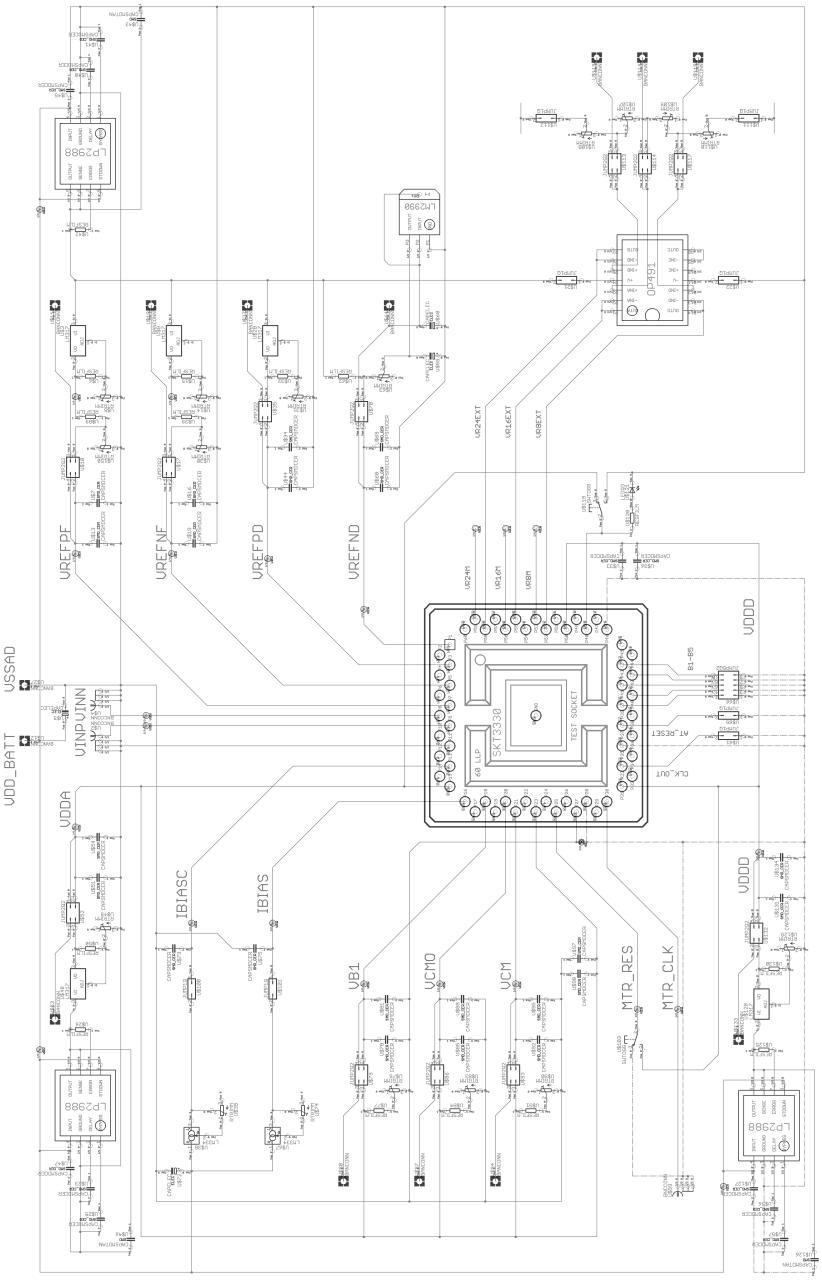


Figure B.11: 2EB. Evaluation board schematic. Test board of a single op-amp third-order $\Sigma\Delta$ modulator for wireless sensor network applications.

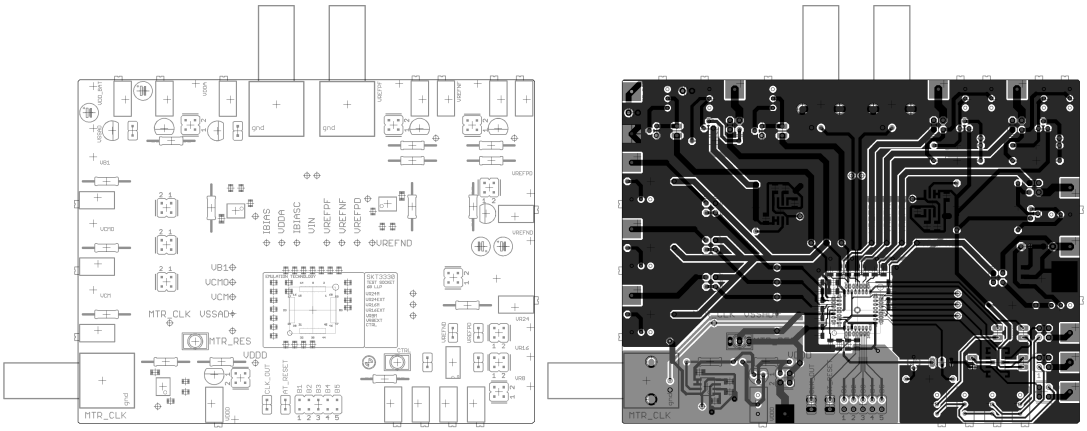


Figure B.12: 2EB. Silkscreen layer (Left) and all layers (right).

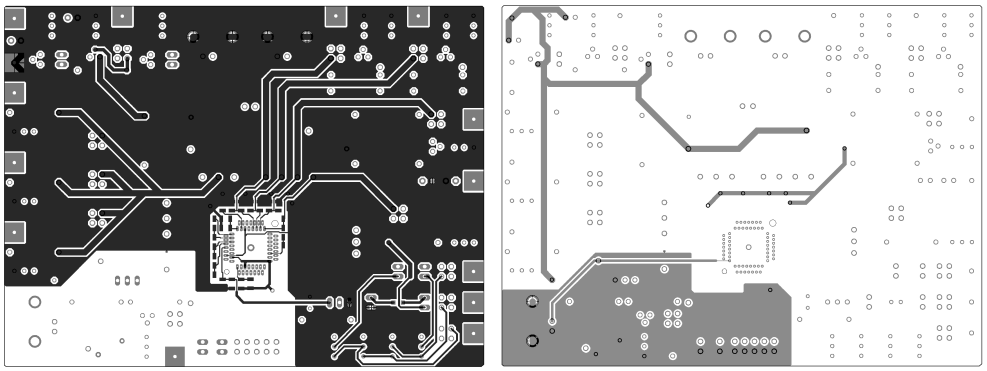


Figure B.13: 2EB. Analog (left) and digital (right) ground plane Layers.

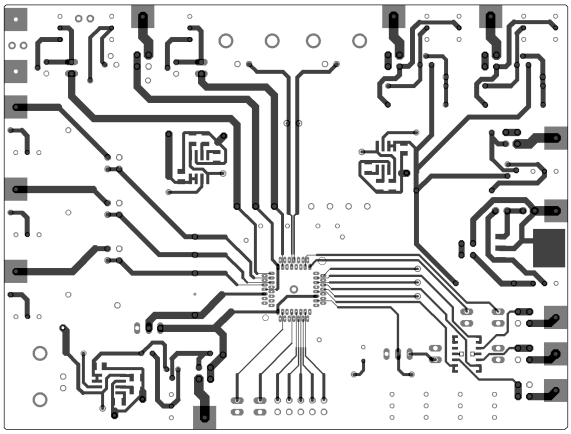


Figure B.14: 2EB. Top level routing layer.

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International Conferences

1. **International Solid State Circuit Conference (ISSCC)−2011. Accepted**.
   A. Peña-Perez, E. Bonizzoni, and F. Maloberti, "A 84 dB SNDR 100 kHz Bandwidth Low-Power Single Op-Amp Third Order $\Sigma\Delta$ Modulator Consuming 140 μW".

2. **European Solid State Circuit Conference (ESSCIRC)−2008**
   E. Bonizzoni, A. Peña Perez, F. Maloberti, M. Garcia-Andrade, "Third Order $\Sigma\Delta$ Modulator with 6 dB SNR and 6 MHz Bandwidth Consuming 6 mW" *Proc. of the 34th European Solid-State Circuits Conference, (ESSCIRC)*, pp. 218-221, 15 - 19 September 2008.

3. **International Symposium on Circuit and Systems (ISCAS)−2011. Submitted**.
   A. Peña-Perez, E. Bonizzoni, and F. Maloberti, "A Low-Power Third-Order $\Sigma\Delta$ Modulator Using a Single Operational Amplifier".

4. **International Symposium on Circuit and Systems (ISCAS)−2010.**
   A. Peña-Perez, V. R. Gonzalez-Diaz, and F. Maloberti, "Double-Sampling Analog-Look-Ahead Second Order $\Sigma\Delta$ Modulator with Reduced Dynamics", *Proc. of International Symposium on Circuit and Systems, (ISCAS)*, pp. 2422-2425, May 30 - June 2 2010.

5. **International Symposium on Circuit and Systems (ISCAS)−2009.**
   A. Peña-Perez, N. Kumar Y.B., E. Bonizzoni, and F. Maloberti, "Slew-Rate and Gain Enhancement in Two-Stage Operational Amplifiers" *Proc. of International Symposium on Circuit and Systems, (ISCAS)*, pp. 2485-2488, May 2009.

6. **International Conference on Electronics, Circuits, and Systems (ICECS)−2010. Accepted**.
   A. Peña-Perez, Oscar Belotti, E. Bonizzoni and F. Maloberti, "A Two Op-Amps Third-Order SD Modulator with Complex Conjugate NTF Zeros".

7. **Midwest Symposium On Circuits And Systems (MWCAS)−2009.**
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8. **International Analog VLSI Workshop−2008.**
   A. Peña-Perez, E. Bonizzoni, F. Maloberti, "Non-Conventional $\Sigma\Delta$ Architectures for Very Low-Power and Medium Resolution Applications" *Proc. of the 2008 IEEJ International Analog VLSI Workshop*, pp. 135-139, July 30 - August 1.

Journals

1. **Accepted for publication in:**
   Journal of Analog Integrated Circuits and Signal Processing.
   E. Bonizzoni, A. Peña-Perez, F. Maloberti, M. Garcia-Andrade, "Two Op-amps Third-Order $\Sigma\Delta$ Modulator with 61-dB SNR, 6-MHz Bandwidth and 6 mW Power Consumption".

CHAPTER 1 | Introduction

CHAPTER 2 | A Third-Order $\Sigma\Delta$ Modulator for DVB-H Applications

Presented at: **European Solid State Circuit Conference (ESSCIRC)**
Edinburgh International Conference Centre, Scotland, UK
September 2008

Based on: Edoardo Bonizzoni, Aldo Peña Perez, Franco Maloberti and Miguel A. Garcia-Andrade **"Two Op-amps Third-Order $\Sigma\Delta$ Modulator with 61-dB SNDR, 6-MHz Bandwidth and 6-mW Power Consumption"**, Accepted for publication in: *Journal of Analog Integrated Circuits and Signal Processing.*

CHAPTER 3 | A Low-Power Single Op-amp Third-Order $\Sigma\Delta$ Modulator

Accepted to: **International Solid State Circuit Conference (ISSCC)**
San Francisco, California
February 2011

The two-stage operational amplifier is based on: Aldo Peña Perez, Nithin Kumar Y.B., Edoardo Bonizzoni and Franco Maloberti **"Slew-Rate and Gain Enhancement in Two Stage Operational Amplifiers"**, *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2485-2488, May 2009.

CHAPTER 4 | High-Performance $\Sigma\Delta$ Modulators

Based on:
Aldo Peña Perez, V.R. Gonzalez-Diaz, and Franco Maloberti **"Double-Sampling Analog-Look-Ahead Second Order $\Sigma\Delta$ Modulator with Reduced Dynamics"**, *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2422-2425, May 2010.

Aldo Peña Perez, Oscar Belotti, Edoardo Bonizzoni and Franco Maloberti **"A Two Op-amps Third-Order $\Sigma\Delta$ Modulator with Complex Conjugate NTF Zeros"**, accepted to *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, December 2010.

CHAPTER 5 | Conclusions

APPENDIX A | Layout Description

APPENDIX B | PCB Design Considerations

Publications