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# Integrated Microsystems for Safety Applications

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Ai miei amici

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# *Introduction*

Over the past few years, research has been increasingly focusing on building systems for observing humans and understanding their appearance and activities. Furthermore, home assistance and protection, especially for the elderly, has become an important topic in sensor systems. In fact, the European population that is 65 years or older and may be in need of assistance is becoming wider and wider, i.e. of the order of 40 million in year 2000 and expected to be around 55 million before the year 2025 [1]. A recent survey of systems for the automatic detection of falls of elderly people is reported in [2]. Solutions based on this kind of approach are important not only for the health aspects regarding the assisted people, but also for social advantages, as the possibility for elders to live longer in their own familiar environment and to care-giver institutions to employ more efficient and optimized services in a more convenient way.

In particular, recent miniaturization [3] and cost reduction of MEMS accelerometers and availability of reliable wireless communication technologies enabled the realization of affordable wearable monitoring systems, based on accelerometers, that can be worn by people performing their normal daily activities. Furthermore, in order to prevent false or missed alarms in fall detection, the use of multi-sensor systems is mandatory and the wearable accelerometer has the fundamental role to validate system decisions.

The developed system is mainly composed of a triaxial accelerometer, an FPGA and a transmitter module at 2.4GHz. The device has the aim of detecting variations of acceleration due to the movements of the elderly person, and distinguishing the variation of acceleration due to fast movements from that due to a fall. A capacitive sensor is used because they have the advantages of higher sensitivity, lower power consumption and better temperature performance, and are less sensitive to drift than piezoresistive sensors. The capacitance variation of the sensor due to variations of acceleration is then converted by the read-out interface into voltages which match correctly with an ADC placed after the interface. The signal obtained must then be processed digitally with an FPGA using an algorithm which detects falls by analyzing the

intensity and form of the signal. After this the accelerometer module sends this information to the central system, which gathers the data coming from all the sensors and decides upon what action to take.

It is important in this kind of system to have voltage reference sources (low-drop-out, LDO, voltage regulators) which are stable under changes of temperature and feature low noise, so that the signal produced by the sensor, due to small variations of capacitance, might be influenced as little as possible. Moreover, the quiescent current of the reference source must be very low because it is used in portable devices which must always be on.

A LDO regulator is typically used inside capacitive MEMS accelerometer interface circuits as a voltage reference for the sensor. To charge the sensor capacitor quickly, the LDO regulator must be able to supply high values of current (of the order of milliamperes).

The algorithms for fall detection have been developed exploiting a fall data archive, gathered in a preliminary data collection with real actors performed within the Netcarity project in 2008. The algorithms were first implemented with the simulation system Matlab and then tested with a system composed of commercial integrated devices; a MEMS accelerometer with digital output, an FPGA and a ZigBee wireless transceiver module.

So to summarize, this work describes three different blocks relevant in the Ambient Assisted Living (AAL) safety field:

- A read-out interface for high precision capacitive sensors.
- A linear regulator with high precision and low consumption, able to provide a high value of current.
- An algorithm to detect falls.

# Chapter 1

# HIGH PRECISION AND LOW NOISE READ-OUT CIRCUIT FOR CAPACITIVE SENSORS

## 1.1 INTRODUCTION

With new miniaturization technology we can obtain electromechanical structures integrated on silicon, such as MEMS – Micro Electro Mechanical System. Thanks to this technology it is now possible to create both the sensor and the read-out circuit on the same chip or in the same package.

Integrated inertial sensors can be either piezoresistive or capacitive [4]. They use the deformation of a mobile mass which is translated into a variation of resistance in the first case and into a variation of capacitance with respect to a fixed electrode in the second. In this project we have chosen to develop an interface circuit for capacitive sensors. These have various advantages over piezoresistive sensors: they are more sensitive, more robust under variations of temperature and, above all, they have zero consumption of static power. However, capacitive sensors often have the problem of providing responses which do not vary linearly with the physical quantity measured, therefore

requiring a slightly more complex read-out interface circuit, which conditions and amplifies the signal. Furthermore the values of capacitance are particularly sensitive to parasitics because they are very small.

### *1.1.1 Capacitive accelerometer*

MEMS capacitive accelerometers, introduced in the last decade, have improved precision, linearity and temperature stability and have reduced the complexity of calibration with respect to previous devices [6]. In MEMS accelerometers capacitors can be used both as sensors and as electrostatic actuators. In fact, if voltage U is applied to the capacitive structure, electrostatic forces proportional to $U^2$ act on the mobile structure. This dual nature of the capacitive detection and the electrostatic drive is one of the clear advantages of this type of accelerometer, which makes possible, for example, an easily implemented option of self-testing, required mostly in those accelerometers used for the safety systems of cars.

There are various structures of capacitive accelerometers, but they all have the base components in common: the proof mass and cantilever beams, realized with the micromachining technique. Capacitive accelerometers are characterized by small capacitances, for which the presence of parasitics cannot be neglected, thus the read-out circuits are necessary.

In capacitive sensors the deflection of the proof mass is often translated into the variation of capacitance of a differential capacitor.

While the proof mass is coming closer to one fixed electrode, increasing the corresponding capacitance value, it is simultaneously going further away from the other fixed electrode, decreasing the corresponding capacitance value.

There are many electronic circuits which enable the transformation of these capacitance variations into voltages. Some examples are: switched capacitor circuits, sigma-delta converters, etc. In most cases the output voltage of capacitance-voltage converters is proportional to [7]:

$$\frac{C1-C2}{C1+C2}=\frac{\Delta x}{x_0} \qquad (1.1)$$

where $\Delta x$ is the deflection of the proof mass, $x_0$ is the nominal distance between the plates of the capacitor, and $C_1$ and $C_2$ are the values of capacitance which constitute the differential structure of the sensor.

An example of sensor is shown in Figure 1. 1 [5]. It is made with the surface micromachining technique and it is integrated on a single chip along with the electronic circuit which implements the necessary functions for achieving an analog output proportional to the acceleration.

In the schematic of the sensor shown in Figure 1. 1, the central rectangular block is the proof mass. It is suspended and supported between two folded springs anchored to the substrate.

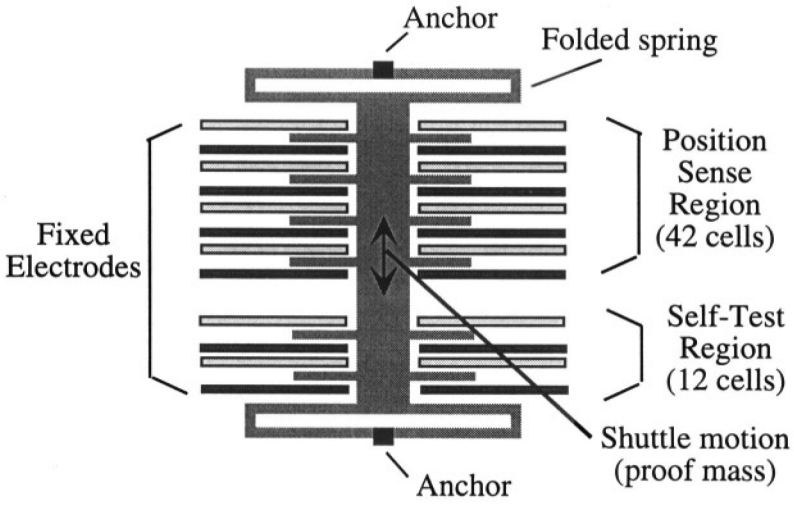


**Figure 1. 1 Schematic illustration of the design of the sensor portion of ADXL150 accelerometer.**

The proof mass presents its “fingers” sideways and each of them is placed between two fixed electrodes. Therefore every electrode connected to the proof mass is a mobile electrode, which follows the movements of the mass when the system is experiencing acceleration, and is positioned between two fixed electrodes so as to form an integrated differential capacitor. In the part of the sensor labeled “position sense region” in Figure 1. 1, there are 42 such repeating units, while in the “self-test region” there are 12. The “self-test region” is made up of electrodes connected to a drive circuit that can apply an electrostatic force on the proof mass, displacing the proof mass for self-test purposes.

The “position sense region” translates acceleration into a variation of capacitance. If we consider a single “finger” of the proof mass placed between two fixed electrodes, it forms a capacitor with each of them, creating a pair of

differential capacitors as shown in Figure 1. 2 [5].

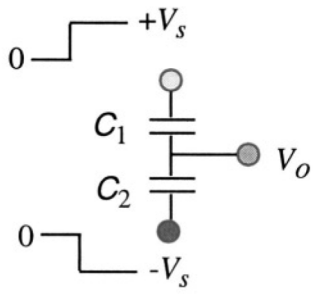


**Figure 1. 2 A typical circuit use of a differential capacitor.**

When an acceleration is occurring, the proof mass moves and its mobile electrode gets closer to one of the fixed electrodes and, consequently, further away from the other.

The output voltage depends linearly on the placement of the mobile electrode, and from this we can determine the acceleration.

### *1.1.2 Read-out interface circuit*

The read-out circuit which we have designed is based on a switched capacitor structure. It uses the principle of charge transfer to convert a capacitive signal into a voltage signal [3], [6]. Using a circuit like this is advantageous because it allows a difficult reading of capacitance to happen in a simple way and, above all, with low power consumption, while also allowing for the cancellation of the effects of offset in the operational amplifier (opamp). This solution, however, suffers from problems of clock-feedthrough and charge injection due to the switches; but thanks to a careful design we are able to greatly reduce these problems without influencing the precision of the circuit.

The strong points of the interface circuit designed in this thesis are the low contribution of noise introduced and the high precision achieved.

The circuit is implemented using a 0.35μm CMOS technology with a minimum supply voltage of 2.2V.

## 1.2 SWITCHED CAPACITOR READ-OUT CIRCUIT

### *1.2.1 Switched capacitor structure*

A capacitance-to-voltage converter based on a switched capacitor structure uses the principle of charge transfer to convert a capacitance variation into a voltage [8]. Let us consider capacitor C connected between two voltages $V_1$ and $V_2$, as shown in Figure 1. 3.

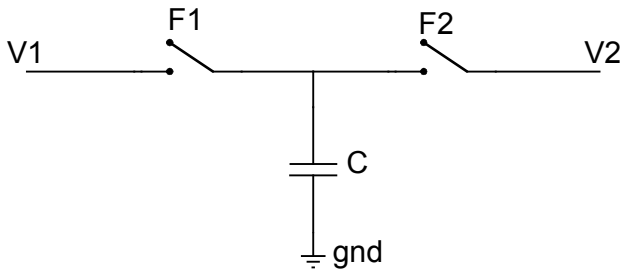


**Figure 1. 3 Schematic to illustrate the operating principle of a switched capacitor circuit.**

The two switches which connect capacitor C to voltages $V_1$ and $V_2$ are driven by two clock phases, as shown in Figure 1. 4.

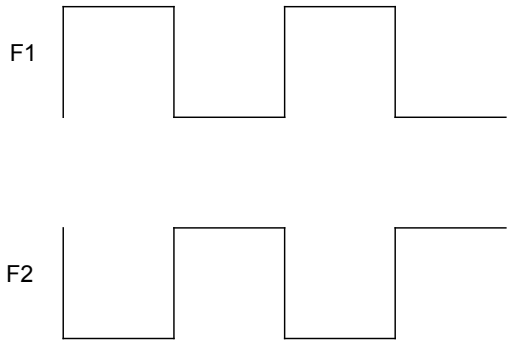


**Figure 1. 4 Phase relationship of $F_1$ and $F_2$**

In phase $F_1$ the charge accumulated on the capacitor is given by:

$$Q_1 = C * V_1 \tag{1. 2}$$

During phase $F_2$, the charge on the capacitor is given by the following formula:

$$Q_2 = C * V_2 \tag{1. 3}$$

As a consequence, a net transfer of charge occurs from the node at voltage $V_1$

to the node at voltage $V_2$, according to

$$\Delta Q = C * (V_1 - V_2) \tag{1.4}$$

In (1.4) one can use the fact that the transferred charge is proportional to capacitance C.

Considering that the two phases which drive the switches have period $T_{ck}$, then if the input voltage varies at a frequency much lower than $1/T_{ck}$, the system behaves like a resistor. The resistance depends on the switching frequency, with the following relationship:

$$R_{eq} = \frac{(V_1 - V_2) * T_{CK}}{\Delta Q} \tag{1.5}$$

Combining this formula with (1.4) we get:

$$R_{eq} = \frac{1}{C} T_{CK} = \frac{1}{C * f_{CK}} \tag{1.6}$$

where $f_{ck}=1/T_{ck}$. Therefore, utilizing only capacitors and switches a resistance has been realized. This kind of resistor has advantages over integrated resistors, in terms of occupation of area and accuracy. In fact, integrated resistors are not very reliable because of variations in the manufacturing process which give rise to variations in the resistance.

The capacitive sensor is made of two capacitors in the configuration shown in Figure 1. 5

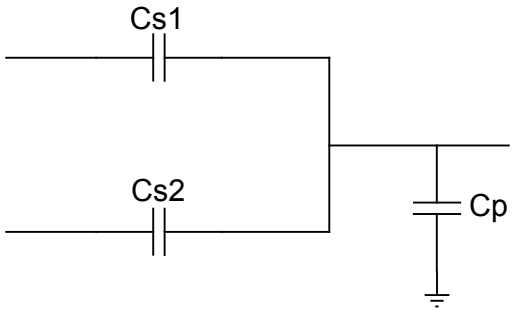


**Figure 1. 5 Configuration of the half bridge of the capacitive sensor.**

The capacitor $C_p$ represents the parasitic capacitance.

### *1.2.2 Read-out circuit*

The schematic of the read-out circuit for such a sensor is shown in Figure 1. 6 [9].

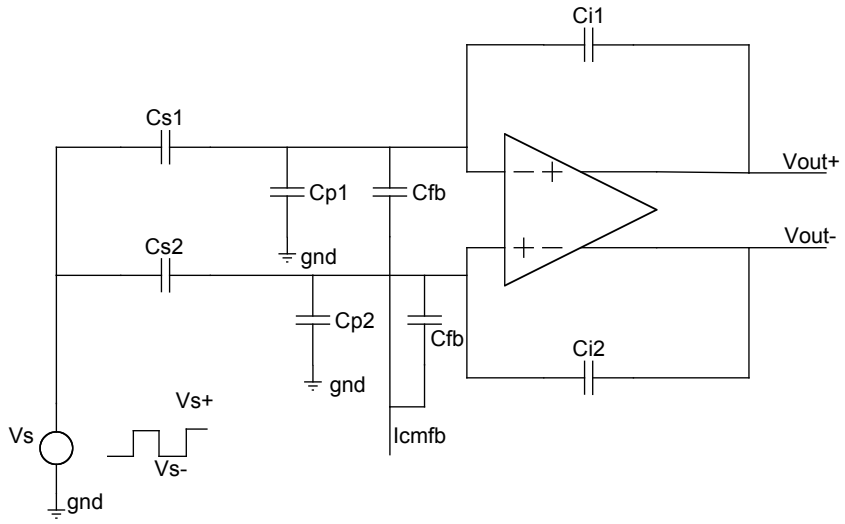


**Figure 1. 6 Schematic of the read-out circuit for capacitive sensors.**

The circuit is based on a fully-differential structure: the difference of charge $\Delta Q$, provided by the two capacitors which constitute the capacitive sensor, is integrated on the capacitors $C_{i1}$ and $C_{i2}$.

The integration of $\Delta Q$ is obtained by applying pulses of voltage to the mid point of the capacitor half bridge. An imbalance between the two capacitors of the sensor, due to variation in the measured level, means that a different amount of charge is transferred into the feedback capacitor $C_i$. As a result of the step in voltage the amount of charge stored in the two capacitors $C_{s1}$ and $C_{s2}$ changes. If

$$\Delta V_s = V_{s+} - V_{s-} \tag{1. 7}$$

then

$$\Delta Q = Q_{s1} - Q_{s2} = -\Delta C_s(\Delta V_s - \Delta V_{icm}) \tag{1. 8}$$

where $\Delta Vi_{cm}$ is the variation of the common mode input voltage due to the step in voltage. The quantity $\Delta V_s - \Delta V_{icm}$ represents the variation in voltage across the plates of the capacitors of the sensor due to the pulses of voltage used.

When the charge given by (1.8) comes from the integration capacitors, and the differential voltage at the input of the opamp is forced to zero, the output voltage becomes

$$\Delta V_{out} = V_{out+} - V_{out-} = -\frac{\Delta C_s}{C_i}(\Delta V_s - \Delta V_{icm}) \quad (1.9)$$

Because the common mode voltage variation at the input of the opamp is given by:

$$\Delta V_{icm} = \Delta V_s(\frac{C_s}{C_s + C_p + C_i}) \quad (1.10)$$

(1.9) can be rewritten as:

$$\Delta V_{out} = -\Delta V_s \frac{\Delta C_s}{C_i}(1 - \frac{C_s}{C_s + C_i + C_p}) \quad (1.11)$$

Because of the mismatches between the pairs of parasitic capacitors $\Delta C_p$ and integration capacitors $\Delta C_s$, additional charge flows into the integration capacitors as consequence of the displacement of the common mode voltage.
This additional charge produces a fixed voltage error at the output, given by the equation:

$$\Delta V_{err} = \frac{\Delta C_i + \Delta C_p}{C_i} \frac{C_s}{C_s + C_i + C_p} \quad (1.12)$$

Since this offset error can be large, the dynamic range of the sensor can be compromised.
Furthermore, the input common mode voltage introduces some contraints in the design of the operational amplifier. This must have a large input range and must have an excellent common mode rejection ratio, to avoid errors at the output due to the displacement of the input common mode voltage. Also the peak to peak amplitude of the input voltage must be kept low, to avoid the situation where the operational amplifier goes outside the input common mode voltage range in which it operates correctly.
All of these problems can fixed by a circuit which stabilizes the input common mode voltage called an input common mode feedback (ICMFB) circuit, shown in Figure 1. 7 [10].

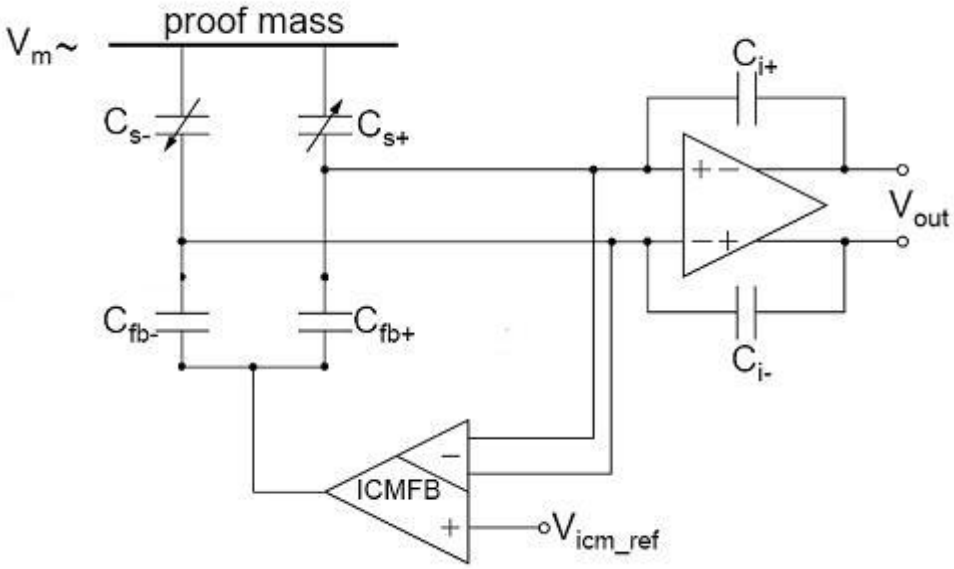


**Figure 1. 7 Read-out circuit including ICMFB.**

The circuit measures the input common mode voltage of the opamp.

Then, a feedback voltage is applied equally to both inputs of the opamp through the two capacitors $C_{fb}$. These voltages cancel out the displacement of input common mode. The voltage value at the output of the integrator is given by:

$$\Delta V_{out} = -\Delta V_s\left(\frac{\Delta C_s}{C_i} - \frac{C_s}{C_{fb}C_i}\Delta C_{fb}\right) \qquad (1.\ 13)$$

The input common mode feedback circuit, with the differential feedback given by capacitor $C_i$ (Figure 1. 7), maintains a voltage value close to ground potential at both input terminals of the amplifier, thus avoiding the problems related to common mode voltage.

The circuit in Figure 1. 6 has the following disadvantages:

1) The opamp input nodes are not biased in DC, therefore small charge quantities injected in these nodes can take the input common mode voltage out of the correct working range of the opamp (also for ICMFB).

2) The Flicker noise and the offset components, directly coupled with the integrator, generate a large error signal at the circuit output.

3) During the two clock phases, the feedback voltage is sent to the sensor by means of an opamp feedback capacitor, taking the voltage down to zero at the plates of the sensors. To avoid overdriving the opamp, the sensor must be disconnected from the read-out circuit during the reset phase putting the voltage

difference across the plates to zero.

The simplified schematic of the read-out circuit with switched capacitors, which also contains a second gain stage, is illustrated in Figure 1. 8.

One must observe that during the reset phase the input terminals of the opamp sample the offset and the low-frequency noise.

These are subtracted from the signal coming from the sensor, thus implementing the autozero technique.

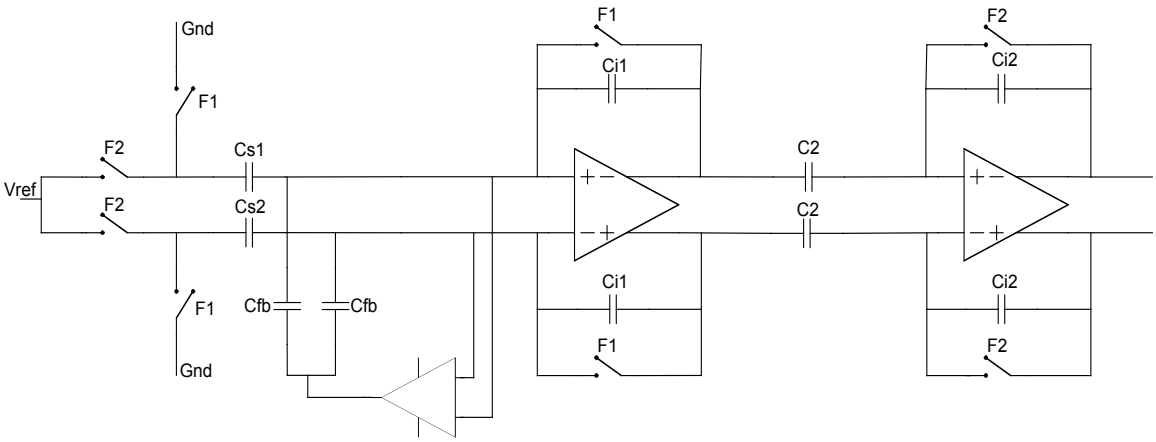


**Figure 1. 8 Simplified schematic of the read out circuit.**

The circuit includes the autozero technique in both stages, however the blocks for the offset correction and for the gain calibration have not been shown. They will be added later.

The third problem can be solved by inserting switches between the capacitor half-bridge and the opamp input. In the reset phase the read-out circuit is effectively isolated from the sensor; in fact the plates of the sensor capacitor are set at the same potential by means of the aforementioned switches.

With reference to Figure 1. 8 we briefly describe the operation of the circuit in the two clock phases, whose behavior is shown in Figure 1. 9.

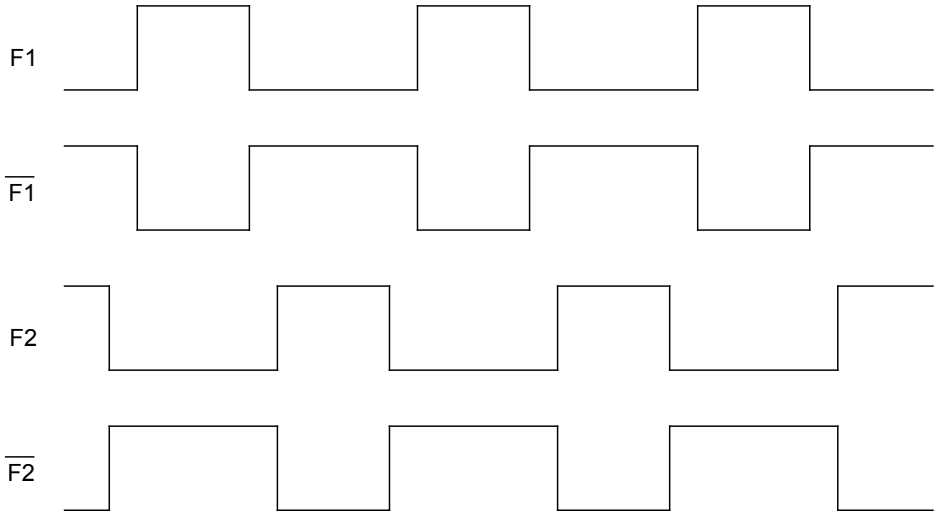


**Figure 1. 9 Clock phases**

- Phase 1: the first stage is in the reset phase while the second stage is in the read phase; the switches F1 isolate the sensor from the read-out circuit.
- Phase 2: the first stage delivers the proper signal at the output, which is proportional to the variation of sensor capacitance; this signal is sampled on the input capacitors of the second stage, which will appear suitably amplified at the output during the next phase F1.

The phases are disoverlapped so that the switches are not closed at the same time. The complementary phases necessary to drive the CMOS switches are also shown.

## 1.3 SPEFICICATIONS

In Table 1. 1 the specifications of the read-out circuit are shown.

| **Parameters** | **Conditions** | **Value** | |
|---|---|---|---|
| **Voltage supply** | | min<br>max | 2.3 V<br>3.6 V |
| **Current consumption** | VDD=3V | max | 2 mA |
| **Settling** | $F_{ck}$=1.2 MHz | typ | 16 bit |
| **Output common mode** | | typ | 1.2 V |
| **Differential output** | | typ | ± 720 mV |
| **Output noise** | OSR = 600 | | 14 bit |
| **PSRR** | VDD = 2.3-3.6 V | min | 50 dB |
| **Clock frequency** | | min<br>typ<br>max | 1 MHz<br>1.2 MHz<br>1.4 MHz |
| **Temperature range** | | min<br>max | -40 °C<br>125 °C |
| **Range capacitve sensor** | | min<br>typ<br>max | 475 fF ΔC=15fF<br>596 fF ΔC=50fF<br>865 fF ΔC=225fF |

**Table 1. 1 Specifications.**

## 1.4 PRELIMINARY NOISE AND POWER CONSUMPTION ANALYSIS

Before describing the design details of the developed read-out circuit, it is useful to perform a preliminary noise and power consumption analysis based on an ideal model.

### *1.4.1 Equivalent circuit*

The equivalent circuit of the sensor read-out block for capacitive sensor is reported in Figure 1. 10.

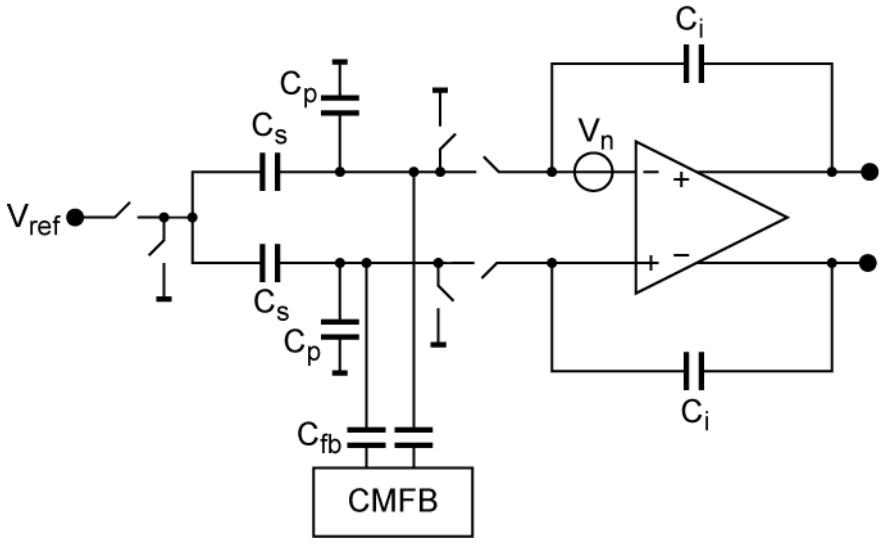


**Figure 1. 10 Equivalent circuit of the sensor read-out block for capacitive sensor.**

The noise analysis is performed on a fully differential circuit. The main advantage of the fully-differential circuit is that the reference voltage $V_{ref}$ represents a common mode signal and hence its noise is rejected (or at least strongly attenuated).

The noise sources considered in the equivalent circuit of Figure 1. 10 are:

-Thermal noise of the input branch

-Thermal noise of the common-mode feedback branch

-Operational amplifier noise

-Reference voltage noise

All of the noise contributions are referred to the input in terms of charge on the sensor capacitance, in order to allow comparison with the input signal (also expressed in charge).

The full-scale input signal expressed in terms of charge on the sensor capacitance is given by:

$$Q_{s,fs} = \Delta C_s V_{ref} \tag{1. 14}$$

.

The allowed noise level for 15 bits of resolution (R) expressed in terms of charge on the sensor capacitance results

$$Q_N = \frac{Q_{s,fs}}{2^R} = \frac{\Delta C_s V_{ref}}{2^R} \tag{1. 15}$$

### *1.4.2 Thermal noise of the input branch*

The thermal noise due to the switches for each sampling capacitor, expressed in terms of charge on the sensor capacitance, is given by

$$Q_{n,C} = \sqrt{\frac{k \cdot T \cdot C_s}{M}} \tag{1. 16}$$

,

where k is the Boltzmann constant (k = 1.38E-23 J/K).

### *1.4.3 Thermal noise of the common-mode feedback branch*

The thermal noise due to the switches for each capacitor of the common-mode feedback circuit, expressed in terms of charge on the sensor capacitance, is given by

$$Q_{n,fb} = \sqrt{\frac{k \cdot T \cdot C_{fb}}{M}} \tag{1. 17}$$

,

where k is the Boltzmann constant (k = 1.38E-23 J/K).

The presence of two capacitors in the CMFB doubles the noise contribution given by equation (1.17).

### *1.4.4 Operational Amplifier Noise*

The operational amplifier noise $V_n$ when referred to the output of the stage is amplified by a factor

$$\frac{V_{n,out}}{V_n} = 1 + \frac{C_s + C_p + C_{fb}}{C_i} \tag{1. 18}$$

.

Assuming a single-pole opamp frequency response, when sampled, because of aliasing the noise power spectral density referred to the output becomes

$$V_{n,out} = V_n \cdot \sqrt{\frac{C_s + C_p + C_i + C_{fb}}{M \cdot C_i} \cdot \frac{g_m}{C_{out}}} \tag{1. 19}$$

where $C_{out}$ is the load capacitance of the operational amplifier and $g_m$ the transconductance of the input transistors. Assuming that $V_n$ is dominated by the input transistors noise and neglecting the flicker noise component (autozero is assumed in the circuit), we have

$$V_n = \sqrt{\frac{8}{3} \cdot \frac{k \cdot T}{g_m}} \tag{1. 20}$$

,

and hence, considering that the thermal noise is amplified by a factor 2 by the autozero, and expressing the noise in terms of charge on the sensor capacitance, we obtain

$$Q_{n,o} = \sqrt{\frac{4}{3} \cdot \frac{k \cdot T \cdot \left(C_s + C_p + C_i + C_{fb}\right) \cdot C_l}{M \cdot C_{out}}} \tag{1. 21}$$

.

By increasing $C_{out}$ and correspondingly increasing $g_m$, in order to maintain the same bandwidth, we can make $Q_{n,o}$ as small as required, at the expense of power consumption. Therefore, we can allocate a noise contribution for the operational amplifier equal to one fourth of the noise contribution from the input branch ($Q_{n,o} = 0.25\ Q_{n,C}$).

### *1.4.5 Reference voltage noise*

The reference voltage noise, expressed in terms of charge on the sampling capacitance, is given by

$$Q_{n,ref} = \frac{V_{n,ref} \cdot \Delta C_s}{\sqrt{M}} \quad (1.22)$$

.

where $V_{n,ref}$ is the integrated noise voltage (from dc to infinity) produced by the reference voltage generator.

We assume $Q_{n,ref} = Q_{n,C}/4$, obtaining $V_{n,ref}$.

### *1.4.6 Total noise*

The total noise, expressed in terms of charge on the sensor capacitance, is given by

$$Q_{n,T} = \sqrt{\frac{2 \cdot k \cdot T \cdot C_s}{M} + \frac{2 \cdot k \cdot T \cdot C_{fb}}{M} + \frac{4}{3} \cdot \frac{k \cdot T \cdot \left(C_s + C_p + C_i + C_{fb}\right) \cdot C_i}{M \cdot C_{out}} + \frac{\left(V_{n,ref} \cdot \Delta C_s\right)^2}{M}} \quad (1.23)$$

### *1.4.7 Power consumption*

The operational amplifier output capacitance as a function of the operational amplifier noise is given by

$$C_{out} = \frac{4}{3} \cdot \frac{k \cdot T \cdot \left(C_s + C_p + C_i + C_{fb}\right) \cdot C_l}{M \cdot {Q_{n,o}}^2} \quad (1.24)$$

Assuming a proper value for $C_i$, we obtain $C_{out}$. In order to achieve the required settling accuracy, the following equation must be verified:

$$2^{-R} = e^{-\frac{1}{2 \cdot f_{ck} \cdot \tau}} \quad (1.25)$$

where

$$\tau = \frac{C_{out}}{g_m} \cdot \frac{C_s + C_p + C_i + C_{fb}}{C_i} \quad (1.26)$$

is the closed-loop time constant of the operational amplifier.

By solving equation (1.25) and (1.26) in terms of $g_m$, we obtain

$$g_m = \frac{C_{out} \cdot \left(C_s + C_p + C_i + C_{fb}\right) \cdot R \cdot \ln\left(4\right) \cdot f_{ck}}{C_i} \quad (1.27)$$

Assuming an overdrive voltage $V_{ov} = V_{GS} - V_{TH}$ equal to 30mV for the input transistors, and considering that

$$g_m = \frac{2 \cdot I_i}{V_{ov}} \tag{1. 28}$$

the current $I_i$ flowing in the input transistors is given by

$$I_i = \frac{V_{ov}}{2} \cdot \frac{C_{out} \cdot \left(C_s + C_p + C_i + C_{fb}\right) \cdot R \cdot \ln\left(4\right) \cdot f_{ck}}{C_i} \tag{1. 29}$$

Then, the total current in the operational amplifier $I_1$, assuming a folded cascode architecture can be assumed to be four time $I_i$.

The current value satisfies also the slew rate requirements since

$$\Delta t = \Delta V_{out} \cdot \frac{C_{out}}{I_i} < \frac{1}{8} \cdot \frac{1}{f_{ck}} \tag{1. 30}$$

where $\Delta V_{out} = V_{ref} \Delta C_s / C_i$ , i.e. the slewing time is less than 1/4 of the available time for settling at the desired resolution.

Assigning the same current to the second gain stage required to obtain the desired output swing ($I_2 = I_1$) and half of the current for the common mode feedback operational amplifier ($I_{fb} = I_1$), we obtain a total cuttent $I_{tot} = I_1 + I_2 + I_{fb}$.

## 1.5 READ-OUT CIRCUIT DESIGN

In the next paragraphs we will describe the detailed design of the read-out circuit. As already mentioned, the circuit consists of two stages.

The main aim of the first stage, besides satisfying the conditions of high slew-rate and low power consumption, is that the noise produced should be low, because this stage is at the head of the chain and therefore influences the noise of the whole circuit.

### *1.5.1 Operational amplifier*

The chosen topology for the opamp has been the folded cascade structure [11]. This type of structure allows for a greater dynamic output compared to the telescopic cascode, whilst maintaining a high gain. The large dynamic output range is necessary to avoid the opamp output going out of the range when there is maximum imbalance of the sensor capacitors as well as maximum values of the sensor offset (100 fF). Also, to eliminate the fixed offset of the circuit and to have a greater immunity to interferences in the power supply, we have opted for a fully differential structure.

In Figure 1. 11 the schematics for the fully differential opamp are shown.

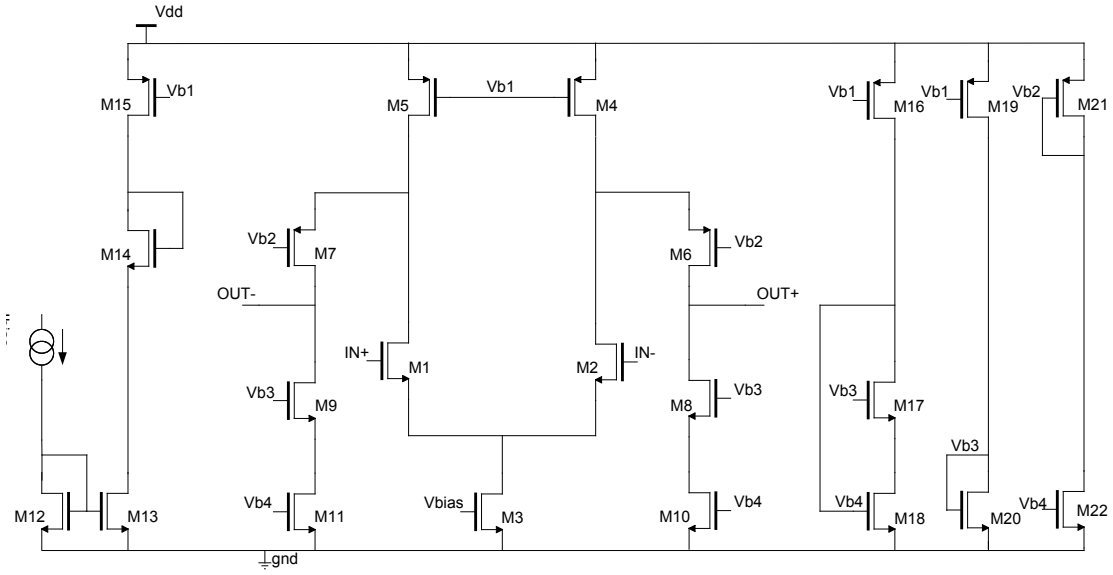


**Figure 1. 11 Circuit schematics of the first stage opamp.**

Such a structure allows for a high gain with a single stage of amplification, without requiring internal compensation.

To reduce the total power consumption of the analog components, the critical transistors are biased in the weak inversion region. In this way one can obtain higher gains, in exchange for a slight reduction of bandwidth.

From the equation of the current of a MOS transistor which works under threshold level we can observe that the behavior of the transconductance versus the current is:

$$I_D \approx e^{q(V_G - V_T)/kT} \tag{1.31}$$

The value of $g_m$ varies in line with the current, giving an advantage in terms of gain with a reduced loss in term of bandwidth and with savings in term of power consumption.

The drain-source resistance of the MOS transistor is given by:

$$r_{ds} = \frac{1}{\lambda I_D} \tag{1.32}$$

where λ is the parameter of channel length modulation.

We should now consider the parameters on which the frequency response of the opamp is based.

The dominant pole of the circuit is due to the load capacitor $C_2$ in parallel to the output resistance $R_{out}$:

$$\omega_p = \frac{1}{R_{out} C_L} \tag{1.33}$$

Therefore the resulting gain-bandwidth product is given by:

$$GBW = \frac{g_m}{C_L} \tag{1.34}$$

where $g_m$ is always the transconductance of the input transistors.

We must now consider the parasitical capacitors present at every output node of the differential amplifier. The gain-bandwidth product is inversely proportional to the output capacitance, which is made up of the sum of the load capacitance $C_1$ and the parasitic capacitance due to MOS transistors $M_6$ and $M_8$ in Figure 1. 11 (always taking into consideration one of the two differential outputs, the positive one in the present example; the consideration is similar for the negative output, considering transistor M7 and M9 as a parasitic load).

The output capacitance is therefore given by:

$$C_{OUT} = C_L + C_{bd6} + C_{gb6} + C_{gd,ov6} + C_{bd8} + C_{gb8} + C_{gd,ov8} \quad (1.35)$$

### 1.5.2 ICMFB

The job of the ICMFB circuit, which works in a closed loop, is to maintain constant the input common mode voltage of the opamp.

To study the behavior of the ICMFB circuit, we can consider the equivalent circuit shown in Figure 1. 12.

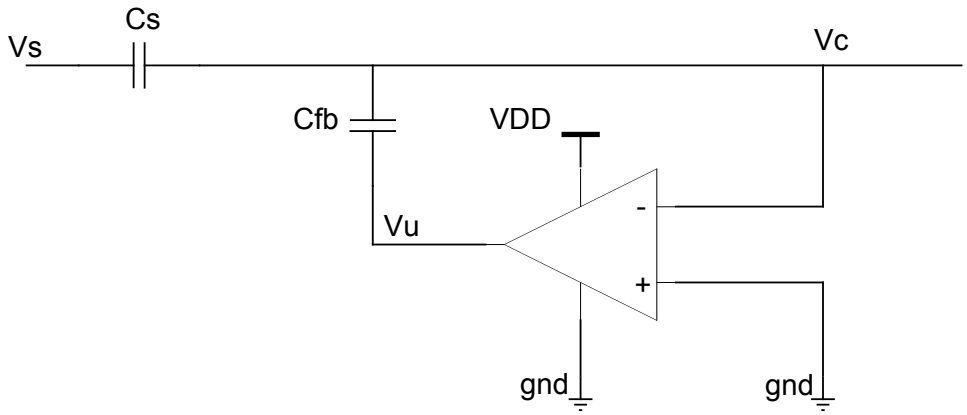


**Figure 1. 12 Equivalent circuit for the ICMFB circuit.**

The input voltage of the main amplifier of the read-out circuit, $V_c$, is given by the formula:

$$V_c = V_s \frac{C_s}{C_s + C_{fb}} + V_u \frac{C_{fb}}{C_{fb} + C_s} \quad (1.36)$$

Taking the following expression into account:

$$V_u = -Av_c \quad (1.37)$$

$$\alpha = \frac{C_s}{C_s + C_{fb}} \quad (1.38)$$

(1.36) can be simplified to

$$V_c = \frac{\alpha V_s}{1 + \beta A} \quad (1.39)$$

If the loop gain βA is large enough, this gives:

$$\frac{V_c}{V_s} = \frac{\alpha}{\beta A} << 1 \qquad (1.40)$$

The stability of common mode voltage for small signals is then considered. The circuit is designed using an opamp with two gain stages, as shown in Figure 1. 13.

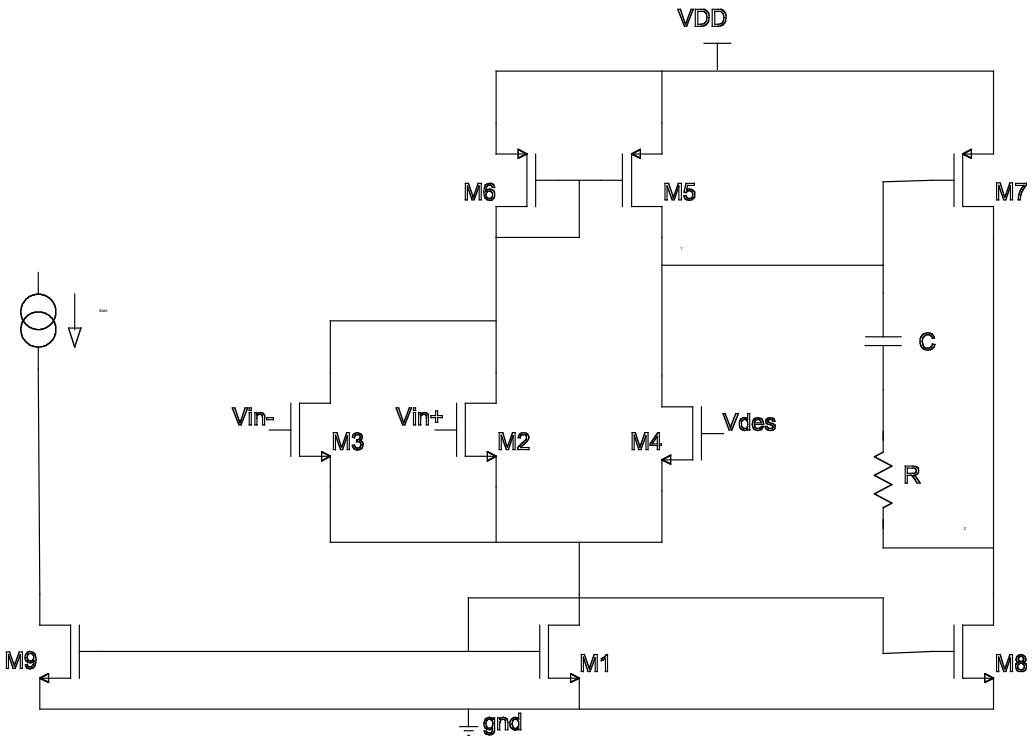


**Figure 1. 13 Schematic of the opamp used for the ICMFB circuit.**

There are three inputs to the opamp, since a transistor in the differential pair is split in two equal parts. The same inputs as the main opamp are connected to the split transistor, while the desired common mode voltage is connected to the other transistor of the differential pair.

In this way the average of the two input signals is obtained and it is compared with the common mode voltage. By means of the feedback the input voltage of the opamp is kept close to the desired value.

The gain of this opamp is given by:

$$A_d = A_1 A_2 = 2 g_{m2} (r_{ds4} // r_{ds5}) g_{m7} (r_{ds7} // r_{ds8}) \qquad (1.41)$$

Because of the two gain stages there are two poles; their frequencies are given by the following expressions:

$$\omega_{p1} = \frac{1}{R_1 C_1} \tag{1. 42}$$

$$\omega_{p2} = \frac{1}{R_2 C_2} \tag{1. 43}$$

where $R_1$, $C_1$, $R_2$, $C_2$ are the resistors and the capacitors at node 1 and at node 2, respectively.

To guarantee system stability – i.e. a phase margin higher than 45° – it has been necessary to introduce a compensation network consisting of capacitor C in series with resistor R (Figure 1. 13), so that the second pole falls after the unity gain-frequency and the influence of the zero created by the introduction of capacitor C (Figure 1. 13) is eliminated.

In the circuit design we have tried to keep the size of the input transistors very small to reduce the parasitic capacitance at the input nodes of the main opamp, so as not to worsen its performance.

### *1.5.3 Switches*

In circuits containing switched capacitors one must pay special attention to interference and noise introduced by the switches. Because they are not ideal, these switches end up influencing the voltage at the plates of the capacitors present in the circuit, and as a consequence the output of the system. One of the problems which affect this type of circuit is the injection of charge from the channel of the transistors composing the switches when they are turned off.

Another problem caused by the switches is clock feedthrough; when the switch is turned off, the parasitic capacitances of the transistors form a voltage partition with the capacitors of the circuit, causing a voltage variation on the drain or source terminals of the transistors.

Considering the circuit in Figure 1. 14 this voltage is given by:

$$\Delta Vout = \frac{C_{gd}}{C_{gd} + C} VDD \tag{1. 44}$$

where $C_{gd}$ is the gate-drain parasitic capacitance (the same applies for the parasitic capacitance gate-source if the output is in the direction of the source). Its value is

$$C_{gd} = C_{ox} W L_{ov} \tag{1. 45}$$

where $L_{ov}$ shows the length of the overlap between the drain and the source and $C_{ox}$ is the oxide specific capacitance.

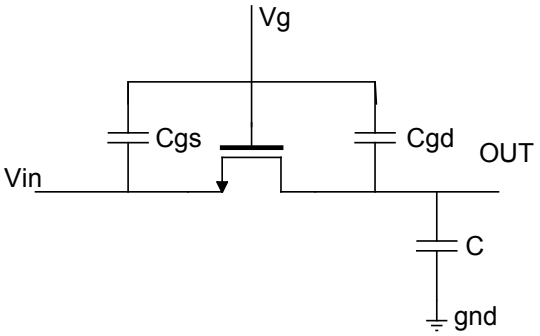


**Figure 1. 14 Schematic for the evaluation of the clock feedthrought effect**

To contain this problem it is important to reduce the dimensions of the switch transistors to the lowest acceptable level, considering the constraints on the switch on-resistance.

A structure which limits the problem both of charge injection and of clock feedthrought is shown in Figure 1. 15.

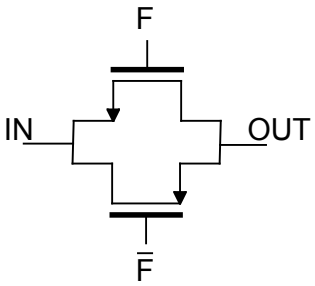


**Figure 1. 15 Complementary switches.**

The equivalent resistance of this switch is given by the parallel between the resistance of the PMOS and NMOS transistors.

Since the expression for the resistance of a transistor working in a triode region is:

$$R = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})} \tag{1. 46}$$

it is necessary design the aspect ratio in the appropriate way so that a

sufficiently low on-resistance is obtained.
Furthermore, to compensate for the clock-feedthrought as much as possible, we preferred to maintain the same dimensions for both transistors. In fact, because the two transistors are driven by opposite voltages, if the capacitances are equal the injected charges with opposite sign tend to cancel each other and reduce the problem.

### *1.5.4 T Switch*

As shown in the previous paragraph, to reduce clock feedthrough, we have decided to use the switches with the smallest channel. Obviously, a trade-off between on-resistance and parasitic capacitance has been accepted, considering that the read-out circuit aims at obtaining high precision.
At such high resolution leakage currents even of order of pA are not tolerated well. For this reason, in different parts of the circuit we had to use the switches described in the previous paragraph in a special configuration, called T-structure. This is shown in Figure 1. 16.

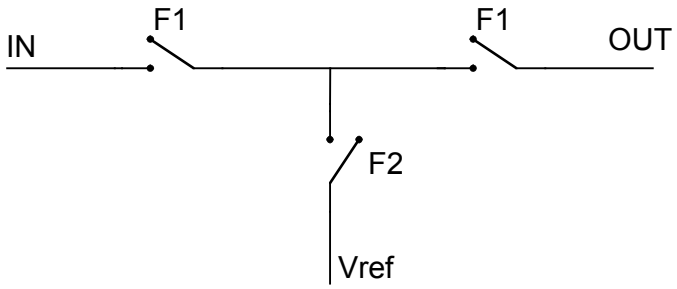


**Figure 1. 16 Switch T-structure.**

A particularly critical situation from this point of view has been found during the amplification phase of the first stage. During this phase, the switch which short-circuits the output with the main opamp input in Figure 1. 17 is open and a voltage difference which depends on the amplitude of the output step is present across it.
This voltage difference can reach values of 700-800 mV.
As consequence, due to a limited switch off resistance, to have leakage currents lower than 1pA, it is necessary to have a resistance of the order of 1GΩ. Such a resistance is not easy to achieve and would produce large

parasitic capacitances because of the length of the channel.

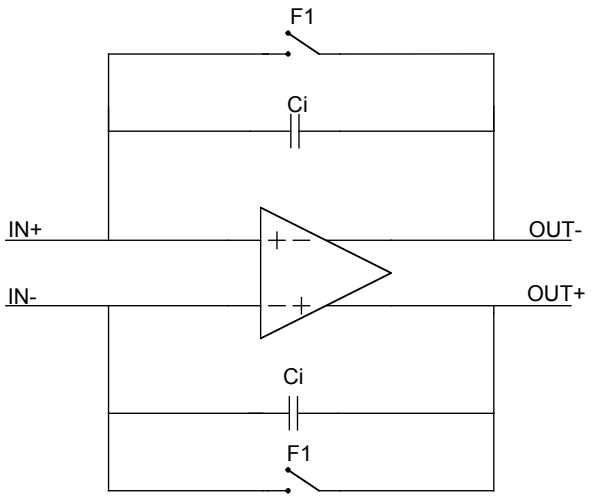


**Figure 1. 17 Reset of the opamp of the first stage.**

Thanks to the T-structure chosen for the switches, during the amplification phase, the common mode voltage ($V_{ref}$ in Figure 1. 16) allows the leakage current to flow to ground and so to greatly reduce the output disturbance.
The disadvantage of this type of switch is that it takes up three times as much space as the simple switch.

### *1.5.5 Second stage*

Also in the second stage a folded cascode structure is used for the opamp, since it is still important to have a large output range. The noise of this opamp is about the same as that of the first stage and hence it becomes negligible compared to the other sources of noise present in the rest of circuit, since it is divided by the first stage gain.
Ultimately in the second stage it has not been necessary to introduce the input common mode feedback block since the first stage which drives the input capacitors of the second stage takes care of maintaining the input voltage at the proper common mode voltage.
The load capacitors of the read-out circuit are equal to 600 fF, which is the input load of the analog-to-digital converter which follows the read-out circuit.
In the second stage of the read-out circuit, the gain and offset calibration is implemented.

### 1.5.6 Gain calibration

The gain calibration block has been realized with an array of capacitors driven by an appropriate digital control circuit which can be programmed. Figure 1. 18 shows this block. It consists of seven capacitors placed in parallel in feedback around the opamp, each linked to an activation switch.

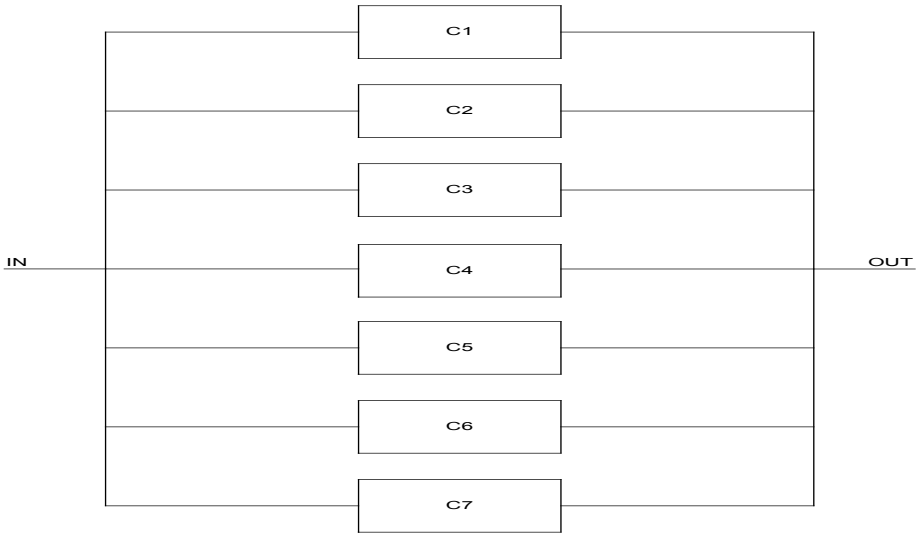


**Figure 1. 18 Schematic of the gain regulation block.**

Every block in the Figure 1. 18 ($C_1$, $C_2$, etc.) represents a capacitor placed between two operating switches.

The total gain of the read-out circuit is given by the product of the gain of the first and second stages as described in the following expression:

$$G = G_1 * G_2 = \frac{\Delta Cs}{Ci_1} * \frac{C_2}{Ci_2} \qquad (1.47)$$

where $\Delta C_s$ is the sensor full scale variation, $C_{i1}$ and $C_{i2}$ are the feedback capacitors of the opamps of the first and the second stage, respectively, while $C_2$ is the input capacitor of the second stage.

Therefore, when there is a full scale variation, in order to keep the gain constant, it is necessary to assign an appropriate value to $C_{i2}$.

According to the specifications the sensor full scale lowest value is 15 fF.

Therefore, on the basis of (1.47), to guarantee that in these condition the gain remains unchanged and the output achieves a value near 720 mV, as required, it is necessary to use a very small feedback capacitance.

This reduces the bandwidth of the opamp because of the feedback factor and can also cause instability within the circuit.

To solve this problem an opamp has to be designed which would use more current than in the first stage, thus increasing the transcoductance and therefore the bandwidth. Furthermore a gain calibration block has been introduced also in the first stage, to reduce the highest gain value needed in the second stage.

In fact, lowering capacitance $C_{i1}$, the first stage gain is increased, and the second stage gain can be slightly reduced. The opposite is true, however, for high full scale sensor. The output voltage at the first stage goes out range because of the high gain level, thus causing distortion.

As a consequence, a further capacitor had to be introduced to lower the gain of the first stage in this case. To select one or the other capacitor, one can use a single bit. Figure 1. 19 shows the schematic of this solution.

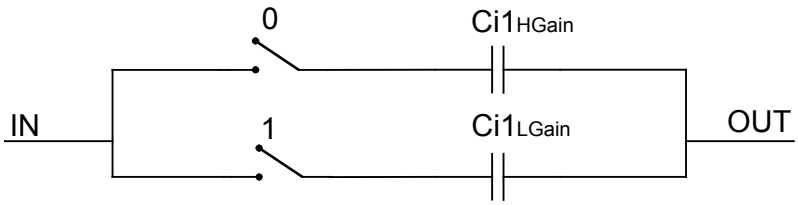


**Figure 1. 19 Schematic of the first stage gain calibration**

The choice of the number of capacitors to use in the second stage and their values is important. In fact through the combination of the feedback capacitors one must have a configuration which covers all the possible values of the full scale of the sensors (15fF-225fF).

To make the best choice a Matlab code is implemented which shows by way of a graph the coverage of the available output voltage range for different combinations of the values chosen for the capacitance array.

Therefore, the values of capacitance which guarantee the maximum and minimum gain are chosen and intermediate values are found.

To guarantee that the capacitors placed on the disconnected branches do not disturb the rest of the circuit and do not cause a leak of current, the switches are designed as shown in Figure 1. 20.

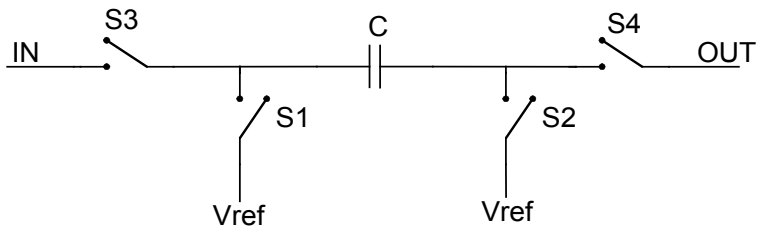


**Figure 1. 20 Schematic of a single capacitor in the array for the gain calibration**

In this way, when $S_3$ and $S_4$ are open, the capacitors which are not active are short-circuited to $V_{ref}$ by the switches $S_1$ and $S_2$ which are on.

### *1.5.7 Offset correction block*

The circuit shown in Figure 1. 21 is used to reduce the offset of the sensor.

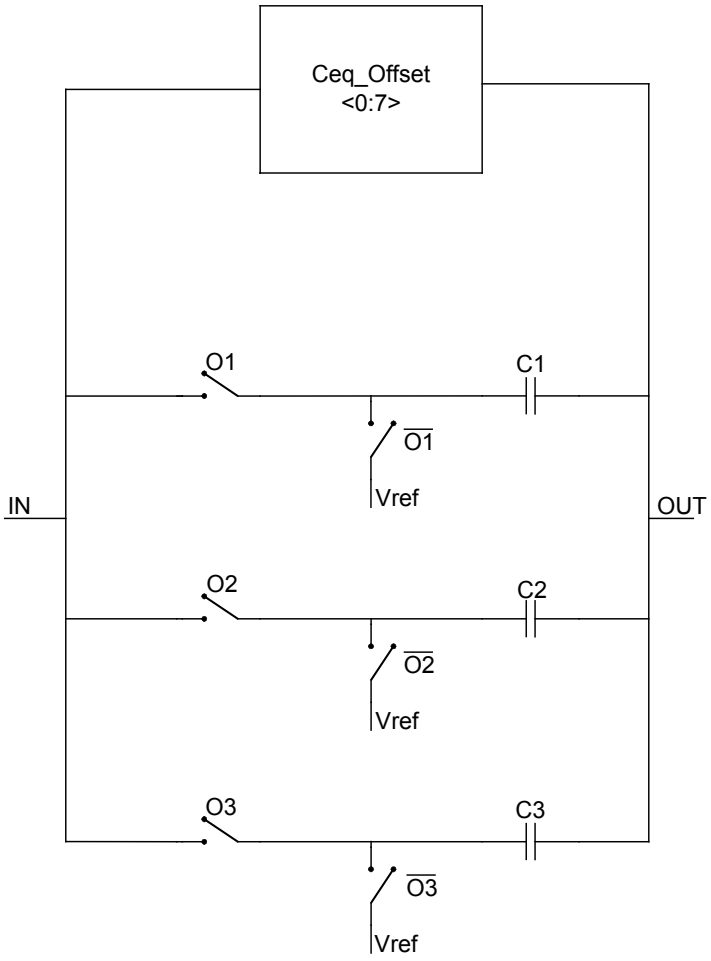


**Figure 1. 21 Schematic of the offset correction block.**

Switches $O_1, O_2$ and $O_3$ enable capacitors $C_1$, $C_2$ and $C_3$, respectively, while

switches $\overline{O_1}, \overline{O_2}$ and $\overline{O_3}$ disable them, keeping them without charge. The block called $C_{eq\_offset}$ in Figure 1. 21, represents eight sub-blocks, each made up of an equivalent capacitor. With the various combinations of capacitors placed in parallel, we can correct a sensor offset of up to 100fF, as required by the specifications.

To cancel out the offset with enough precision to guarantee a coverage of the output range equal to at least 83%, it was necessary to use some capacitors as small as 4.47fF, placed in parallel.

Since the technology used does not allow to build such small capacitors with sufficient precision, the circuit shown in Figure 1. 22, which is able to obtain small values of capacitance starting from larger values, was used.

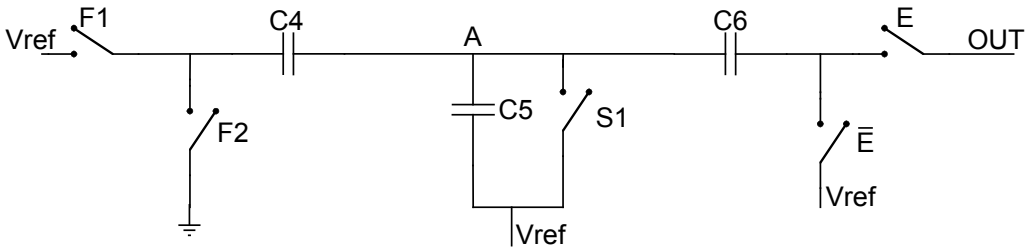


**Figure 1. 22 Schematic to obtain the capacitor of 4.47fF, for offset correction.**

The lowest value of capacitance used in the block in Figure 1. 22 is therefore 30fF.

Analyzing the circuit it is easy to understand that the value of the equivalent capacitors is given by the following formula:

$$C_{eq} = \frac{C_6^2}{C_5 + 2(C_4 C_6)} \qquad (1.48)$$

Switch $S_1$ is always turned off and is used to guarantee through its off-resistance that charge is not accumulated on capacitor $C_5$.

The inconvenience of this circuit is that node A during phase 2 reaches a voltage almost equal to 900mV, leading to a difference of potential of about 400 mV across switch $S_1$.

This, as already analyzed, introduces a small leakage current, which is badly tolerated because of the high precision of the circuit and the high number of equivalent capacitors needed to cancel out the sensor offset of 100fF. To tackle this problem, it is not possible to use switches in T configuration.

It has therefore been decided to design the capacitors $C_1$, $C_2$ and $C_3$ with dual weight, using dual control signals. Only eight structures like those in Figure 1. 22 are used, thus significantly reducing the lost current.

The value of the capacitor is such that the cancellation of the offset is always guaranteed, also foreseeing a possible error of 20% in the manufacturing of the capacitors themselves.

By means of the switch $E$, the desired capacitance is enabled and connected to voltage $V_{ref}$ when it is not used by means of switch $\overline{E}$.

## 1.6 LAYOUT

In Figure 1. 23 is shown the Layout of the device designed. Its area is 0.28mm$^2$ (350µm*800µm).

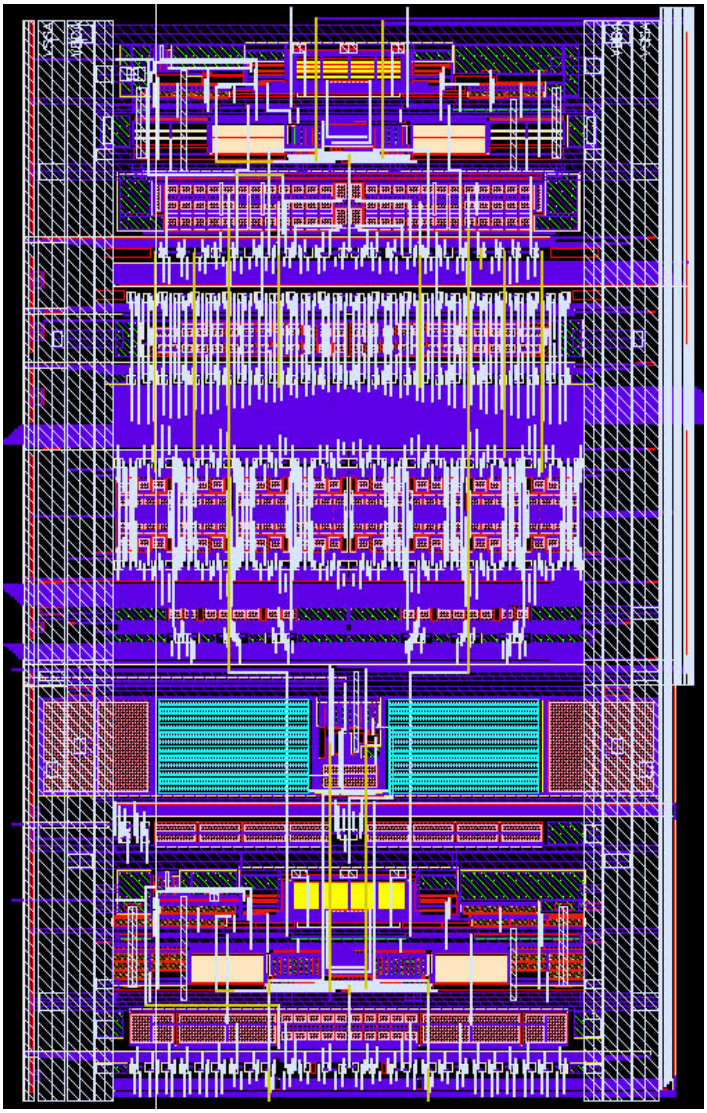

**Figure 1. 23 Layout of the read-out circuit.**

## 1.7 SIMULATIONS

In this subsection simulation results of the designed readout-circuit will be presented. All reported performance values have been achieved in post-layout simulations considering both resistive and capacitive parasitics. Typical as well as the most significant corner conditions have been taken into account. Temperature coefficient, settling accuracy, input equivalent noise charge and power consumption will be reported in the following.

### *1.7.1 Temperature coefficient*

The temperature coefficient parameter has been evaluated at post-layout simulation level with typical supply voltage and varying the process conditions, by considering output voltage settling at two different operating temperatures: 27°C and 72°C, i.e. a difference of 45°C. The output voltage drift considering temperature is thus normalized with respect to signal amplitude and applied temperature difference. *Table 1. 2* reports the temperature coefficient performance summary in typical conditions and over most significant process corners. *Figure 1. 24* reports the output settling while investigating temperature coefficient in typical conditions (TM), while *Figure 1. 25* and *Figure 1. 26* show the output voltage of the interface circuit considering slow process (WS) and fast process (WP) respectively. While evaluating temperature coefficient of the read-out circuit typical capacitive sensor values ($C_0$=594fF, $\Delta C_{max}$=50fF) have been considered.

| Figure n. | Model | Vout@27 (mV) | Vout@65 (mV) | ΔVout (µV) | Termic Coeff (ppm/°C) |
|---|---|---|---|---|---|
| Figure 1. 24 | TM | 685.328 | 685.173 | -156 | -6.10 |
| Figure 1. 25 | WS | 692.209 | 691.936 | -273 | -10.67 |
| Figure 1. 26 | WP | 679.073 | 679.671 | 598 | 23.38 |

**Table 1. 2 Temperature coefficient.**

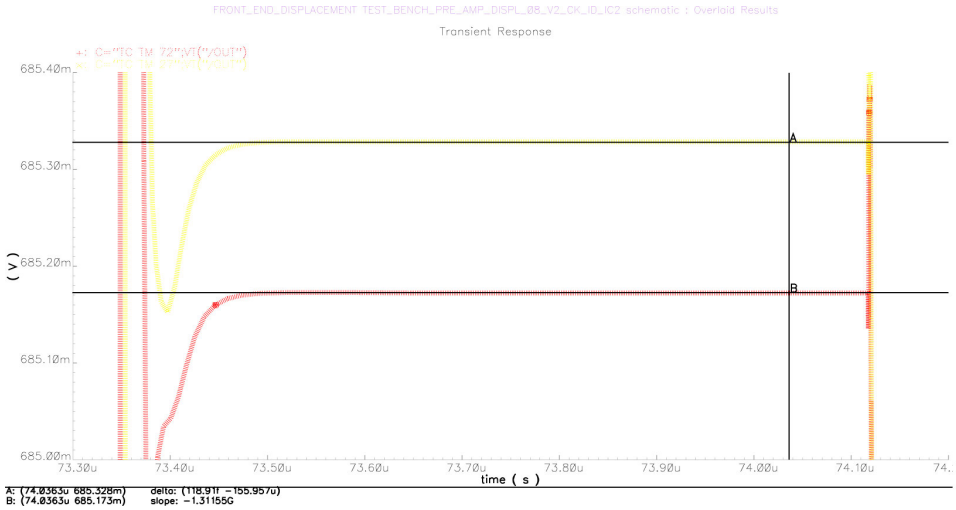


**Figure 1. 24 Temperature coefficient investigation with typical process and supply voltage.**

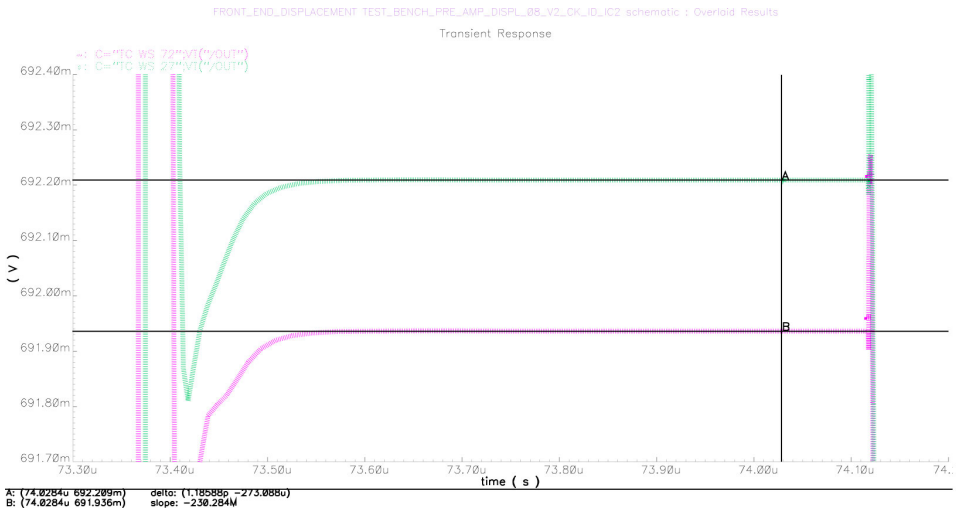


**Figure 1. 25 Temperature coefficient investigation with slow process and typical supply voltage.**

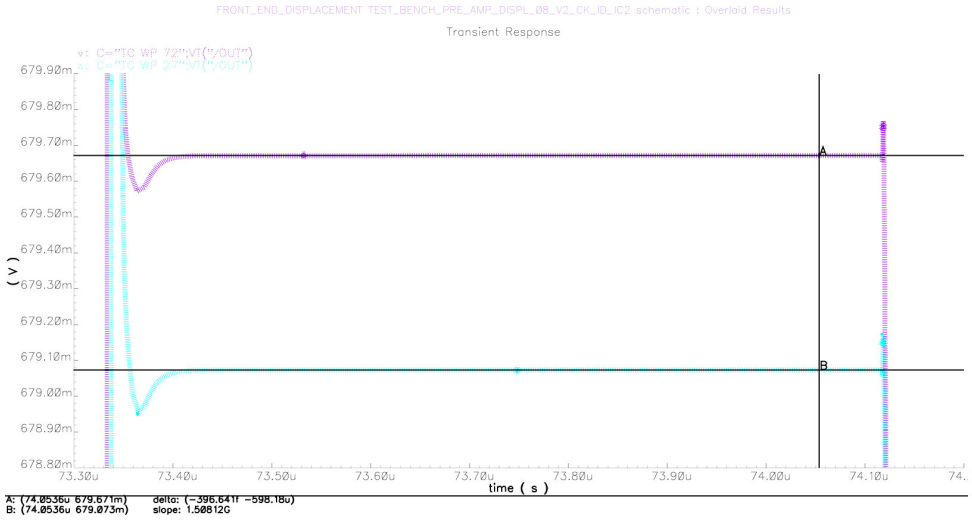


**Figure 1. 26 Temperature coefficient investigation with fast process and typical supply voltage.**

### *1.7.2 Settling accuracy*

Dynamic settling accuracy of the read-out circuit have also been evaluated in post layout simulations, considering typical conditions and the most significant process, supply voltage and temperature corners. In the reported simulation results (*Table 1. 3*) noise contribution is not considered. As reported in *Table 1. 3* the CMOS process corners taken into account in the simulation settling accuracy summary are: fast (WP), slow (WS), and worst one (WO), while the considered resistor-related corners are instead fast (WP) and slow (WS). Also capacitor process corners have been conidered in slow (WS) and fast (WP) cases, respectively. Finally temperature and supply voltage have been swept betwen [-40°C, 125°C] and [3.6 V, 2.3V], respectively, leading to a worst case resolution in terms of equivalent number of bits (ENOB) of 17.2. While evaluating settling accuracy of the read-out circuit typical capacitive sensor values ($C_0$=594 fF, $\Delta C_{max}$=50 fF) have been considered.

| Corner | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| **Model** | CMOSWP | CMOSWS | CMOSWS | CMOSWO | CMOSWO |
| **Res.** | RESWP | RESWS | RESWS | RESWP | RESWS |
| **Cap.** | CAPWS | CAPWS | CAPWS | CAPWP | CAPWS |
| **Temp. (°C)** | -40 | -40 | 125 | -40 | 125 |
| **Supply (V)** | 3.6 | 2.3 | 2.3 | 3.6 | 2.3 |
| **Resol.(bit)** | 22.55 | 18.99 | 17.91 | 18.86 | 17.20 |

**Table 1. 3 Settling accuracy.**

### *1.7.3 Noise*

The interface circuit has been finally evaluated at post-layout simulation level also in terms of noise performance. Three different summary tables are reported: **Table 1. 4** , **Table 1. 5** and **Table 1. 6** reporting noise peformance of the circuit with connected minimum, typical and maximum possible capacitive sensor values, respectively. For each connected sensor type two different process corners have been considered: typical (TM) and slow (WS). Also temperature is swept in simulations in the range [-40°C, 125°C].

| Simulation | Model | Temperature (°C) | $V_{n,Out}$ (μV) | $Q_{n,In}$ (aC) |
|---|---|---|---|---|
| **Typical** | TM | 27 | 5.878 | 1.763 |
| **Corner 1** | WS | 125 | 7.191 | 2.157 |
| **Corner 2** | WS | -40 | 5.489 | 1.647 |

**Table 1. 4 Output noise with typical sensor.**

| Simulation | Model | Temperature (°C) | $V_{n,Out}$ (μV) | $Q_{n,In}$ (aC) |
|---|---|---|---|---|
| **Typical** | TM | 27 | 5.719 | 1.716 |
| **Corner 1** | WS | 125 | 7.158 | 2.147 |
| **Corner 2** | WS | -40 | 5.330 | 1.599 |

**Table 1. 5 Output noise with minimum sensor.**

| Simulation | Model | Temperature (°C) | $V_{n,Out}$ (μV) | $Q_{n,In}$ (aC) |
|---|---|---|---|---|
| **Typical** | TM | 27 | 4.225 | 2.958 |
| **Corner 1** | WS | 125 | 5.171 | 3.620 |
| **Corner 2** | WS | -40 | 3.892 | 2.724 |

**Table 1. 6 Output noise with maximum sensor.**

### *1.7.4 Current consumption*

The current consumption simulations are reported in Table 1. 7. Some simulation results with different process models (TYP, WS and WP) are shown and also different temperature values have been considered. All simulations have been carried out at nominal voltage supply value of 3.0V.

The maximum current consumption over all considered corners is always less than 1.6mA.

| | Model | Temperature (°C) | Tot Current (mA) |
|---|---|---|---|
| **Typical** | CMOSTM | 27 | 1.386 |
| **Corner2** | CMOSWS | -40 | 0.851 |
| **Corner3** | CMOSWS | 125 | 1.369 |
| **Corner4** | CMOSWP | -40 | 1.540 |

**Table 1. 7 Current consumption.**

## 1.8 MEASUREMENTS

For all reported measurements, the gain settings have always been chosen in a way that the hypothetical output voltage of the read-out circuit would be near to but not greater than 720 mV, i.e the full scale of the subsequent ADC input.

### *1.8.1 Noise*

In Table 1. 8 the most significant noise measurement results over different read-out chip samples are reported in terms of equivalent number of bits resolution (ENOB).

| Sample | Gain (mV/fF) | ENOB |
|---|---|---|
| **1** | 15.1 | 14.4 |
| **2** | 3.5 | 15.9 |
| **3** | 32 | 15.5 |
| **4** | 50 | 13.2 |

**Table 1. 8 Noise.**

Figure 1. 27 ishows the noise contribution of five different samples (two are actually exhibiting the same contribution) as a function of the considered oversampling ratio (OSR) an thus of the system conversion speed.

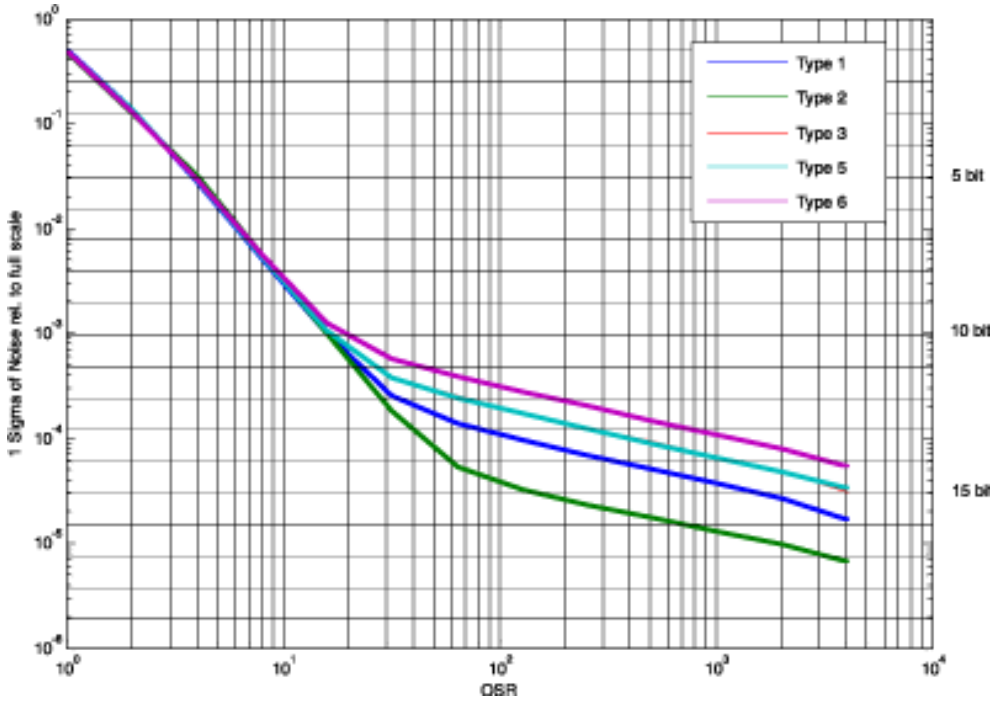


**Figure 1. 27 Noise vs OSR.**

### *1.8.2 Gain resolution*

Figure 3.5 shows the slope (i.e. the measured gain) referred to the used gain setting and compared to the ideal slope (i.e. the calculated gain). As may be seen, the desired full output swing of the read-out circuit is almost covered in all reported examples (83%), thus fulfilling the required coverage specification of 4/5 of full-scale (80%).

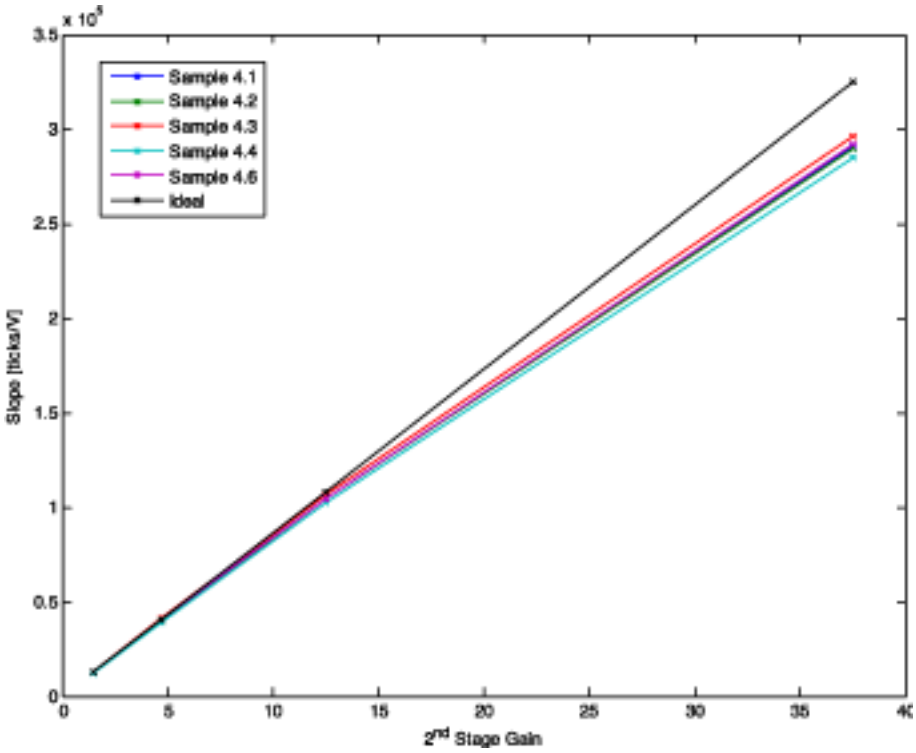


**Figure 1. 28 Slope vs gain setting.**

### *1.8.3 Power Supply Rejection Ratio*

The rejection of disturbances on the power supply (PSRR) have been verified over different chip samples. Figure 1. 29 shows the PSRR performance of 5 different samples over a large frequency range [1Hz – 1MHz] putting in series with the main voltage supply a large AC signal (100mV). PSRR performance is reported expressing he output voltage in dB with respect to the signal applied on the supply. The minimum value (worst case) obtained in the frequency sweep of interest for every sample represents the actual PSRR performance for the considered sample. In normal operating mode, considering an OSR of 600, the frequency interval of interest is up to 1kHz.

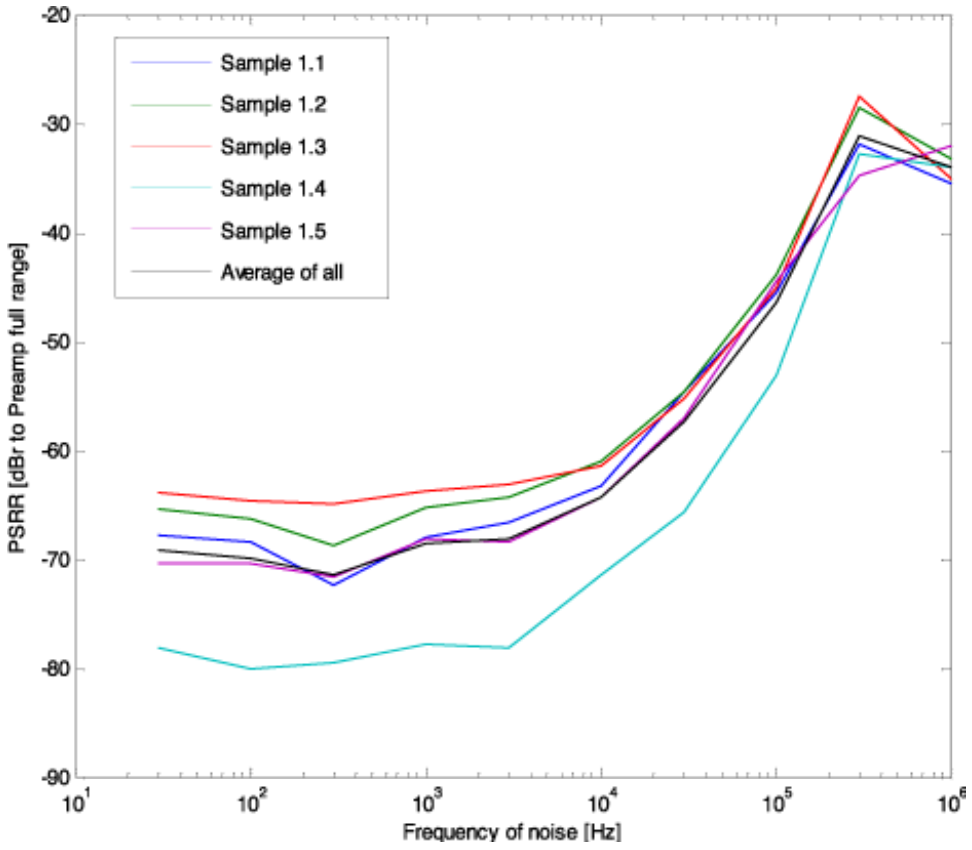


**Figure 1. 29 PSRR.**

### *1.8.4 Linearity*

The full scale linearity is calculated from a measurement in minimum gain configuration, where the full scale is nominally represented by the interval [0.61, 1.84] V for $V_{ref,ext}$. Figure 1. 30 shows the linearity error over this range for the five samples analyzed. For reference purpose, the measurement uncertainty due to limited precision of the voltage meter used is sketched.

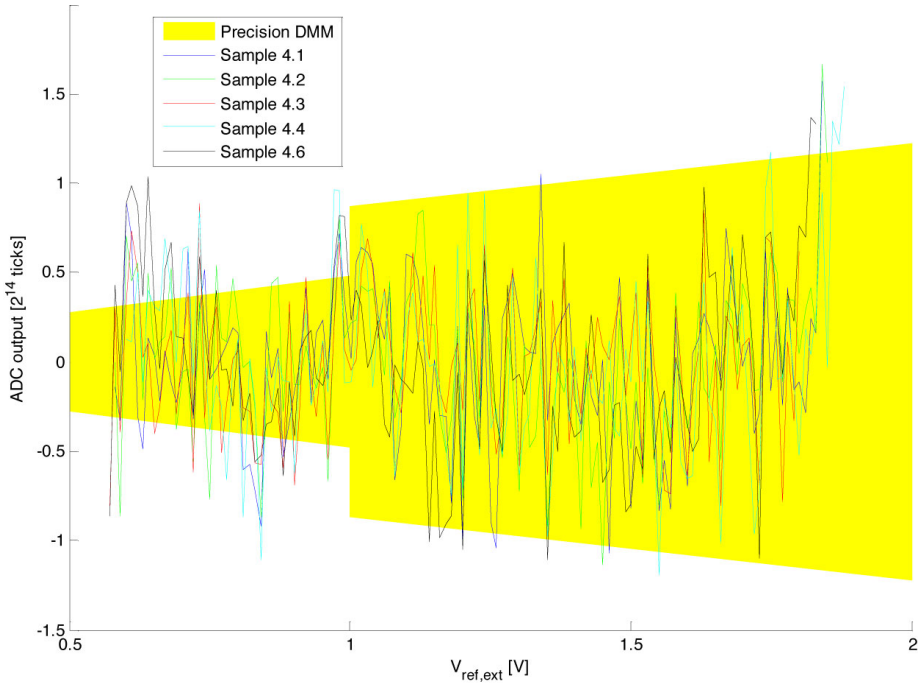


**Figure 1. 30 Linearity.**

The linearity error is defined as the difference between the measured value at the output and the linear fit of all measured values of one chip. In Table 1. 9, the linearity error is compared to the full range (±720 mV at ADC input) and calculated back to the input as estimated equivalent input linearity error.

| **Sample** | **1** | **2** | **3** | **4** | **6** |
|---|---|---|---|---|---|
| **Linearity error RMS (ticks)** | 0.45 | 0.45 | 0.45 | 0.45 | 0.45 |
| **Linearity error max ± (ticks)** | 1.57 | 1.66 | 0.89 | 1.54 | 1.37 |
| **Rel to full scale (bit)** | 13.2 | 13.1 | 14 | 13.2 | 13.4 |
| **At input (aF)** | 59 | 62 | 33 | 58 | 51 |

**Table 1. 9 Summary from full scale linearity measurement.**

*Chapter 2*

# REGULATORS IN POWER MANAGEMENT SYSTEMS

## 2.1 INTRODUCTION

Supplying and conditioning power are among the key aspects of an electrical system. A loading application, be it a cellular phone, pager, or wireless sensor node, can not sustain itself without energy, and can not fully perform its functions without a stable supply. The fact is that transformers, generators, batteries, and other off-line supplies incur in substantial voltage and current variations across time and over a wide range of operating conditions.

The role of the voltage regulator is to convert these unpredictable and noisy supplies to stable, constant, accurate, and load-independent voltages, attenuating these ill-fated fluctuations to lower and more acceptable levels. The regulation function is especially important in high-performance applications where systems are increasingly more integrated and complex. A system-on-chip (SoC) solution, for instance, incorporates numerous functions, many of which switch simultaneously with the clock, demanding both high-power and fast-response times in short consecutive bursts **Error! Reference source not**

**found.**. Not responding quickly to one of these load-current transitions (i.e., load dumps) forces storage capacitors to supply the full load and subsequently suffer considerable transient fluctuations in the supply. The bandwidth performance of the regulator, that is, its ability to respond quickly, determines the magnitude and extent of these transient variations.

Regulators also protect and filter integrated circuits (ICs) from exposure to voltages exceeding junction-breakdown levels.

A voltage regulator is normally a buffered reference: a bias voltage cascaded with a non-inverting op-amp capable of driving large load currents in shunt-feedback configuration.

The purpose of a regulator is to regulate the output voltage against all possible operating conditions, from load and supply to temperature variations. They differ from references only in that they supply load current, but this seemingly insignificant fact adds considerable complexity and challenges to the problem. However, linear regulators, when compared with switching regulators, are simpler, faster, and less noisy, but they suffer from limited power efficiency, that is because low dropout voltages (LDO) are so appealing in linear regulators for portable, battery-powered applications where single-charge battery life is crucial. Consequently, among other categories, like power level and frequency-compensation strategy, dropout voltage is an important metric in linear regulators.

Due to high variations in battery operating voltages, virtually all battery-operated applications require regulators. Furthermore most designers find it necessary to include regulators and other power supply circuits on-chip in order to improve the overall performance.

Limited energy and power densities are the key points of such a market, requiring circuits to yield high power efficiency and demand low quiescent-current flow to achieve reasonable lifetime performance as it is described in the following [14], [23]. Current efficiency ($\eta_i$), which refers to a proportionately lower quiescent current when compared against the load current, is vital. In particular, quiescent current ($I_Q$) must be as low as possible during zero-to-low loading conditions because it amounts to a significant portion of the total drain current of the battery.

During heavy loading events, on the other hand, higher quiescent current is

acceptable because its impact on total drain current and therefore battery life is short, which is why current efficiency ($\eta_I$) and not absolute quiescent current, is important. :

$$\eta_I = \frac{I_{LOAD}}{I_{TOTAL}} = \frac{I_{LOAD}}{I_{LOAD} + I_Q} \tag{2.1}$$

where $I_{LOAD}$ is the output load current and $I_Q$ is the quiescent current of the LDO regulator.

Thus, the load determines the lifetime of the battery during high load-current conditions and the regulator quiescent current during zero-to-low loading events.

The capacity of a battery, defined in ampere-hours [Ah] and the average drain current sets the battery life of the electronic system which can be written as follows:

$$Life[h] = \frac{Capacity[Ah]}{I_{DRAIN(ave)}} = \frac{Capacity[Ah]}{I_{Q(ave)} + I_{LOAD(ave)}} \tag{2.2}$$

where $I_{DRAIN(ave)}$ is the average of the sum of the quiescent current ($I_Q$) with the load current ($I_{LOAD}$).

Relationship (2.2), together with the fact that the majority of portable devices stays idle most of the time, implies that battery life is a function of low load-current conditions, that is of $I_{Q(ave)}$ which can be controlled by an accurate designing of the regulator.

Today's most popular secondary (i.e., rechargeable) battery technologies are lithium ion (Li Ion), nickel cadmium (NiCd), and nickel metal hydride (NiMH), the first of which ranges from 2.7V when completely discharged to 4.2V when fully charged and the latter two from 0.9V to 1.7V. Microscale fuel cells have even lower voltages, approximately at 0.4V–0.7V per cell. Ultimately, the variable nature of these relatively low-voltage technologies superimposes stringent requirements on the regulator, limiting their supply headroom voltage and their available dynamic range to considerably low levels.

Low-voltage operation is also a consequence of advances in process technologies. The run for higher packing densities forces technologies to improve their photolithographic resolution, fabricating nanometer-scale junctions, which have inherently lower junction breakdown voltages. A typical

0.18μm CMOS technology, for instance, cannot sustain more than roughly 1.8V. Additionally, since financial considerations limit the complexity of the process, that is, the number of masks used to fabricate the chip and therefore the variety of devices available, only standard CMOS and stripped BiCMOS process technologies are most desirable, which translates to less flexibility for the designer because a low-voltage environment is restrictive for analog ICs. Thus many traditional design techniques are prohibitive under these conditions, limiting flexibility and sometimes system performance.

For example cascoding devices, emitter and source followers, and Darlington configured bipolar-junction transistors, which are useful for increasing gain, bandwidth, and current-driving capabilities, require additional voltage headroom, which is a precious commodity in battery-operated devices. Low voltages also imply increased precision, pushing performance down to fundamental limits. A 1% 1.8 V regulator, for example, must have a total variation of less than 18 mV, which includes 5–12 mV of load and line regulation effects, extended commercial temperature extremes (e.g., −40°C–125ºC), process variations, noise and variations in the supply, and so on. Moreover, since dynamic range suffers in a low-voltage environment, the demand for improved percent accuracy increases to sub-1% levels.

These issues typically give rise to more complex and usually more expensive ICs (i.e., more silicon area and/or more exotic circuit and/or process technologies), encouraging the designer to be more resourceful and innovative.

Linear regulators are also classified as low or high dropout (LDO or HDO), which refers to the minimum voltage dropped across the circuit or, in other words, the minimum difference between the unregulated input supply and the regulated output voltage ($V_{DO}$ in Figure 2. 1).

This voltage is important because it represents the minimum power dissipated by the regulator, since the power lost is dependent on the product of the load current and this dropout voltage. Low-dropout regulators (LDO) consequently dissipate less power than their higher dropout counterparts and have therefore enjoyed increasing popularity in the market, especially in battery-operated environments.

Linear regulators with dropout voltages below 600mV belong to the low-dropout class, but typical dropout voltages are between 200 and 300mV.

Figure 2. 1 also illustrates the three regions of operation of a linear regulator: linear, dropout, and off regions [16].

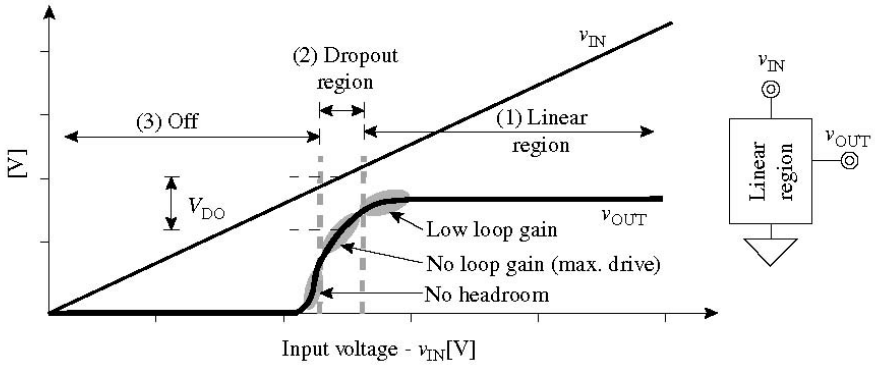


**Figure 2. 1 Typical input-output voltage characteristics of a linear regulator.**

When the circuit is operating properly, that is to say, when it regulates the output with some finite and non-zero loop gain, the regulator is in the linear region. As input voltage $V_{In}$ decreases, passed a certain point, one of the transistors in the loop enters the triode region (or low-gain mode) during which time the circuit still regulates the output, albeit at a lower loop gain and consequently with some gain error. As $V_{In}$ decreases further, the loop gain continues to fall until it becomes, for all practical purposes, zero, when it reaches its driving limit. At this point, the regulator enters the dropout region and the power switch supplies all the current it can to maintain the highest possible output voltage. The voltage difference between $V_{In}$ and $V_{Out}$ in this region is the dropout voltage $V_{DO}$, and although $V_{DO}$ is at first approximately constant, it tends to increase with decreasing values of $V_{In}$ (datasheets often quote the equivalent resistance during the mostly linear portion of the dropout region). The *off* region is where the circuit reaches its headroom limit, when the input supply voltage is too low for the transistors to work properly, and more specifically, for the negative feedback control loop to understand that $V_{DO}$ is below its target and keep some drive applied to the power switch.

In summary, linear regulators can be high or low power, externally or internally compensated (as it will be discussed in paragraph 2.6) and high or low dropout.

As it can be easily understood low-dropout voltage regulators are necessary in all applications which need efficient power management. The increasing

demand is especially evident in mobile battery-operated products such as cellular phones, pagers, camera recorders, and laptops. Such space-efficient designs only use a few battery cells, thereby necessarily decreasing the available input supply voltage.

## 2.2 ARCHITECTURE OF LDO REGULATORS

The circuit presented in this thesis is a high precision LDO which is made up of two main blocks, as shown in Figure 2. 2 [17]. The first block is a second order temperature compensated bandgap voltage reference (BG) and the other one is an error amplifier (EA).

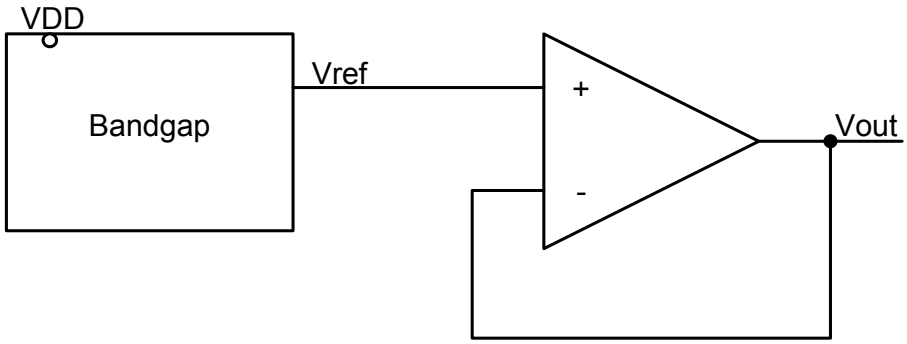


**Figure 2. 2 Block diagram of the precision voltage reference under development.**

The reference voltage is generated by a current based bandgap cell. This voltage drives the error amplifier, which provides to the load up to a maximum bidirectional current of ±5 mA, exploiting a class AB output stage. It has been decided to design the bandgap cell to deliver directly the required reference voltage $V_{ref}$ = 1.25 V in order to avoid the use of a resistive divider in the error amplifier loop. By avoiding the resistive divider, for the input differential pair of the error amplifier bipolar devices can be used (the base current would be a problem with a resistive divider), also minimizing offset and flicker noise, without requiring very large MOS transistors.

The control loop, in essence, reacts to offset and cancel the effects of load current, input voltage, temperature, and an array of other variations on the output. The reference block provides a stable dc-bias voltage that is impervious to noise, temperature, and input-supply-voltage variations.

Between the reference voltage generator and the error amplifier there is a low pass filter to reduce the noise from the BG.

## 2.3 OUTPUT LOAD

As shown in Figure 2. 3, dc current $I_{Load}$, equivalent load resistance $R_{Load}$, and equivalent load capacitance $C_{Load}$ are the most important parameters because they set the biasing condition of the regulator and its small-signal loading impedance, which affects its stability conditions. Load current $I_{Load}$ spans the maximum range specified for the regulator and incurs the worst-case load dumps for the system during transient conditions, which amounts to the maximum possible load step in the shortest time possible.

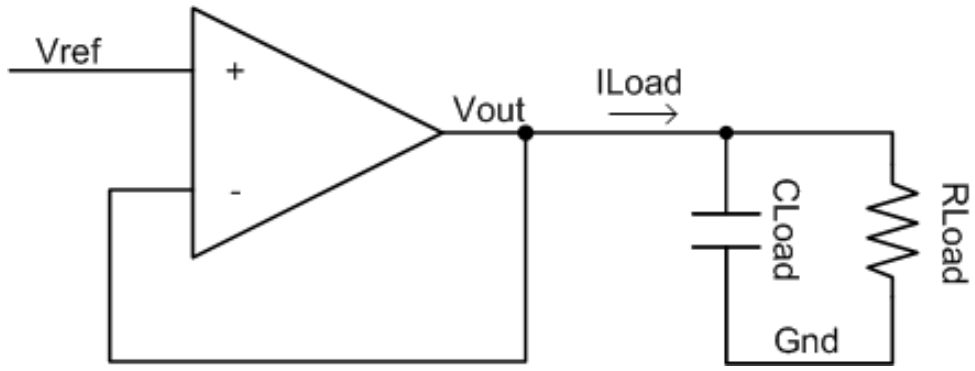


**Figure 2. 3 Equivalent Load of LDO.**

Not knowing the exact nature of the load makes it impossible to predict $R_{Load}$ accurately, yet its impact on stability and circuit requirements can be very demanding from the designing point of view.

The designer, for reliability concerns, must therefore consider all extreme conditions: 1) load is purely resistive $I_{Load}$ is zero and $R_{Load}=V_{out}/I_{Load}$) and 2) load is only a current sink ($R_{Load}$ is infinitely large or altogether removed). Simply assuming the load is purely resistive may be limiting. In the case of internally compensated LDOs, for instance, whose output pole is parasitic to the system, a purely resistive load places the output pole at optimistically higher frequencies. Subjecting this LDO to a higher impedance load pulls the output pole to lower frequencies, compromising the stability of the system. Similarly, assuming the load is purely active, that is, only a current sink, may be unrealistically optimistic in the case of externally compensated LDOs, where the dominant low-frequency pole is at the output and a high-impedance load optimistically places this pole at lower frequencies. A lower impedance load

pushes the output pole to higher frequencies, closer to the parasitic poles of the system, where stability may be compromised.

The effective loading elements include the parasitic devices associated with the package of the IC, filter capacitors, PCB, and loading circuits. In **Figure 2. 4** is shown the typical loading environment of a linear regulator IC.

Output capacitor $C_{out}$ suppresses transient noise on the output voltage, as mentioned earlier, and for the case of externally compensated regulators, sets the dominant low-frequency pole of the controlling negative-feedback loop. The output capacitance is normally on the order of several μF, as is for input filter capacitor $C_{in}$, which is also used to suppress transient noise in light of the parasitic effects.

These external capacitor devices as shown in Figure 2. 4, exhibit a parasitic equivalent-series resistance (ESR) denoted in the figure as $R_{ESR}$, the value of which can be up to several ohms. Ceramic and ceramic multilayer chip (CMC) capacitors have low ESR values and consequently lend themselves for higher frequency applications and improved transient-noise suppression [16].

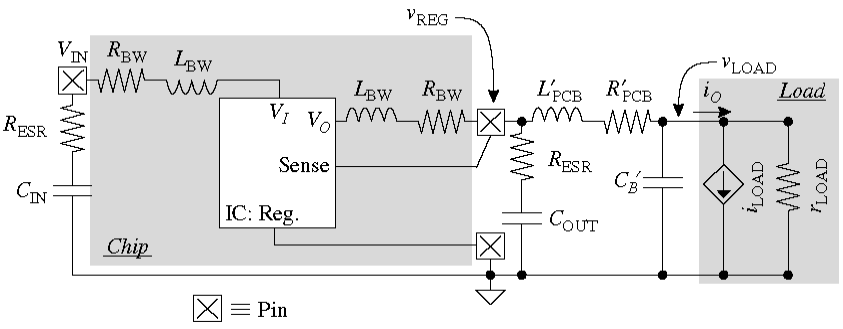


**Figure 2. 4 Typical loading environment of a linear regulator IC.**

Capacitors also exhibit an equivalent-series inductance (ESL), the magnitude of which is typically less than 5nH. The effects of this parasitic inductance are often negligible in low-power and low-bandwidth applications. A 10mA load dump, for example, through a 5nH inductor in 1μs produces an ESL voltage of 50μV ($L\Delta I/\Delta t = 5nH \cdot 10mA/1\mu s$). In general, all parasitic devices present in the power path of the regulator cause negative effects on dc, transient, and efficiency performance.

Series parasitic bond wire and PCB resistors $R_{BW}$ and $R_{PCB}$ introduce load-

dependent series dc ohmic voltage drops and power losses, producing a lower-than-anticipated voltage at the load and higher than expected power losses. Parallel multiple bond wires appeal to the designer because they produce lower series resistances and inductances. For similar reasons, loads that are close to the regulator (with short and wide PCB traces) also produce lower voltage drops and power losses.

## 2.4 SPECIFICATIONS

The specifications of the project presented in this thesis are summarized in Table 2. 1. The specification must be satisfied with an input voltage ($V_{in}$) of 5V, a load current ($I_{Load}$) of 0A and a load capacitor ($C_{out}$) of 1µF, unless otherwise specified.

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{out}$ | Output Voltage | $T_{amb}$,corners | 1.24875 | 1.25 | 1.25125 | V |
| TC | Output Voltage Temp coeff | $I_{out}$=0A, $T_{min}<T<T_{max}$ | | | 10 | ppm/°C |
| $\Delta V_{out}/\Delta V_{in}$ | Line Regulation | $T_{min}<T<T_{max}$ $V_{inmin}<Vin<V_{inmax}$ | | | 100 | ppm/V |
| $\Delta V_{out}/\Delta I_{out}$ | Load Regulation | $-5mA<I_{out}<5mA$ $T_{min}<T<T_{max}$ | | | 100 | ppm/mA |
| $e_{out}$ | Noise Voltage | 0.1Hz<f<10Hz | | 40 | | µVpp |
| $T_r$ | Turn On settling Time | $V_{out}$ to 0.1% of final value | | 2 | | ms |
| $V_{in}$ | Supply Voltage range | | 1.8 | | 5.5 | V |
| $I_Q$ | Quiescent supply current | | | | 8 | µA |
| $I_{Load}$ | Max Load current | $Vi_{nmax}<Vin<V_{inmin}$ | | | ±5 | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $C_{out}$ | Load Capacitor range | | 0.1 | 1 | 10 | µF |
| **T** | Temp range | | -40 | 25 | 125 | °C |

**Table 2. 1 Specifications of the designed circuit.**

It can be seen that the circuit must have high precision: the maximum thermal coefficient must be less than 10ppm/ºC. This forces the designer to choose a voltage reference with a second order temperature compensation. The circuit must work correctly with a supply voltage of 5.5V and, consequently, it is necessary to use MOS transistors with a thick gate oxide, which can be driven by voltage differences greater than 2.5V. This causes a problem due to increasing of the threshold voltage of this type of transistor. This makes the design particularly critical with low supply voltages and with very high load currents.

The large range of load capacitance and load current values (100nF÷10 µF and –5mA÷5mA) as shown in Table 2. 1 makes the stability of the circuit very demanding from the design point of view. Under these conditions the output pole changes a lot as these values vary. Consequently the stability of the LDO is not simple to obtain in all the working conditions by using conventional design. For this reason we adopded particolar circuit solutions as it will be discussed later in paragraph 2.3.

Also the current consumption must be very low (~8µA) and therefore it is necessary to use resistors with high values (up to 50MΩ) within the voltage references. The resistors used must have a high resistivity (Ω/square) in orderd to reduce area occupation.

The LDO must drive both positive and negative currents so an error amplifier with an AB output stage has been designed. The control of the output quiscent current is realized by a specifically designed circuit.

To satisfy the specifications concerning noise, a filter is placed between the first and second stage as mentioned before in paragraph 2.2.

The technology used in this project is the ST Microelectronics HF7CMOS.

## 2.5 BANDGAP REFERENCE

The most important performance parameters of a voltage reference circuit are represented by temperature behavior, power supply rejection ratio, transient response and, for the latest designs, by low-power low-voltage operation [18]. Depending on the load requirements, the output of the circuit can be regulated or unregulated. In order to reduce the sensitivity of the reference voltage with respect to the supply voltage variations, modified cascode structures can be implemented, a trade-off between line regulation and low-voltage operation being necessary in this case. A large bandwidth of the voltage reference improves the transient behavior of the circuit, implying also a good noise rejection.

Referring to the possibilities of implementing a voltage reference circuit, two different approaches could be identified: voltage-mode and current-mode topologies as depicted in Figure 2. 5. It is also possible to design a mixed-mode voltage reference.

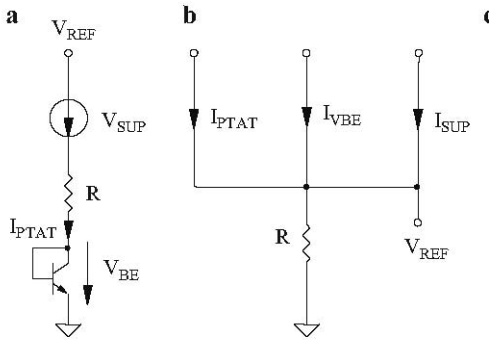


**Figure 2. 5 PTAT Voltage mode (a); current mode (b).**

Most voltage references are based on voltage-mode architecture (a), the PTAT (proportional to absolute temperature) voltage across resistor *R* compensating the linear dependence on temperature term from $V_{BE}(T)$, while $V_{SUP}(T)$ voltage contains nonlinear terms, complementary to the nonlinear components of $V_{BE}(T)$. The most important disadvantage of the voltage-mode references is that the minimal reference voltage obtainable is about 1.2V (the silicon bandgap energy), so these architectures are not suitable for very low-voltage

applications. In order to obtain reference voltages lower than 1.2V, a current-mode design (b) can be used. The compensation of the reference voltage temperature dependence is obtained by summing within resistor R three currents with different temperature dependencies: a base–emitter derived current $I_{VBE}$, a PTAT current $I_{PTAT}$, and a superior-order correction current $I_{SUP}$. As the reference voltage depends on the ratio of resistors, their temperature coefficient does not strongly affect the overall performance of the circuit, only superior-order terms being slightly influenced by the resistor temperature dependence. For this project the current mode has been chosen.

The fundamental methods for designing voltage references are adapted to the implementation of these circuits in bipolar and CMOS technology, with the advantages and limitations associated with each technology. The first-order analysis is followed by the study of errors introduced by the second-order effects that affect the active device operation. The weak inversion biasing of MOS transistors allows obtaining low-power operation for circuits designed in CMOS technology, while the current-mode operation and specific design techniques assure a low-voltage operation of voltage references. The improvement of the power supply rejection ratio of the designed circuits is achieved by proposing simple and cascode self-biasing methods for the elementary structures.

In the following paragraph the design of the BG will be described analyzing first the structure with a first order compensation and secondly adding the non linear compensation in order to obtain the precision of 10ppm/ºC shown in Table 2. 1.

### *2.5.1 First order bandgap compensation*

There are two main components that build up the output voltage of a bandgap reference. One is the voltage across a directly biased diode (base–emitter voltage) and the other is a term proportional to the absolute temperature (PTAT). The negative temperature coefficient of the former term compensates for the positive temperature coefficient of the latter. If $V_T = kT/q$ is used to obtain a PTAT voltage, it is well known that we have to multiply it by approximately 22 to compensate for the temperature dependence of the diode voltage. If this condition is satisfied, the generated bandgap voltage becomes approximately

1.2 V.

The bandgap voltage is given by:

$$V_{BG} = V_{BE} + n\frac{kT}{q} \tag{2.3}$$

We achieve a fraction of the traditional bandgap voltage by scaling both terms of (2.1), using currents terms proportional to $V_{BE}$ and to $V_T$, respectively. These currents are suitably added and transformed into a voltage with a resistor. We compensate for the temperature dependence of the resistors used by fabricating them with the same kind of material. Figure 2. 6 shows the schematic diagram of a circuit, which implements the described operation [19].

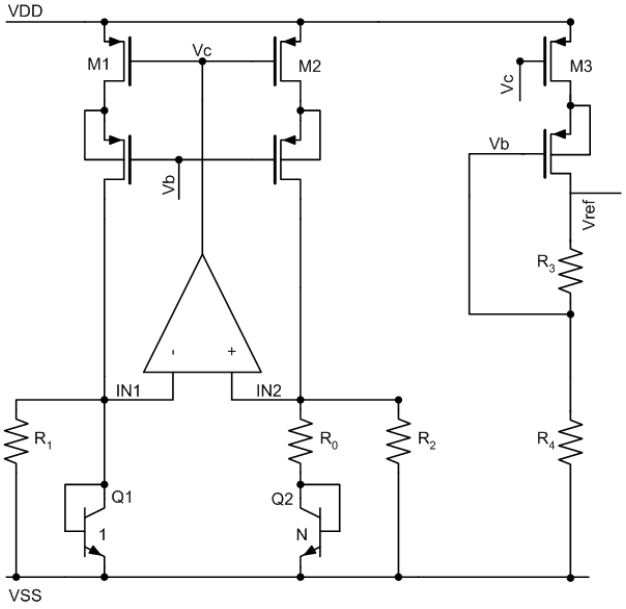


**Figure 2. 6 Bandgap structure.**

Two diode connected bipolar transistors with different emitter area ratio drain the same current, leading $\Delta V_{BE}$ to be equal to $V_T \ln(N)$. Therefore, the current in $R_0$ is PTAT. The operational amplifier forces the two voltages $V_{in1}$ and $V_{in2}$ to be equal, thus producing a current in the nominally equal resistors $R_1$ and $R_2$ proportional to $V_{BE}$. As a result, the current in $M_1$, $M_2$ and $M_3$ is the same and is given by:

$$I_1 = \frac{V_T \ln(N)}{R_0} + \frac{V_{BE}}{R_1} \tag{2.4}$$

The output voltage is then given by:

$$V_{OUT} = I_1(R_3 + R_4) = \frac{(R_3 + R_4)}{R_1}\left[\frac{R_1 \ln(N)}{R_0}V_T + V_{BE} + \frac{R_1}{R_{5,6}}V_{NL}\right] \quad (2.5)$$

The compensation of the temperature coefficients of $V_T$ and $V_{BE}$ is ensured by choosing values of N and of the ratio $R_1/R_0$ which satisfy:

$$\frac{R_1 \ln(N)}{R_0} = 22 \quad (2.6)$$

In particular, to minimize the spread of the resistors, we chose N=24.

Moreover, since transistors $M_1$, $M_2$ and $M_3$ maintain almost the same drain–source voltage $V_{ds}$, independently of the actual supply voltage, the power supply rejection ratio of the circuit is only determined by the operational amplifier.

By inspection of the circuit, we observe that the minimum supply voltage is determined by the $V_{BE}$ plus a saturation voltage of a p-channel transistor. Therefore, 1V can be enough to operate the circuit. However, the supply voltage used must ensure proper operation of the operational amplifier and, indeed, this is the true limit of the circuit.

The bandgap circuit needs an operational amplifier whose input common-mode voltage is around 0.65V (the $V_{BE}$ value). Moreover, since the output node drives p-channel current sources, its output quiescent voltage should be below $V_{DD} - V_{th}$. Moreover, the gain of the operational amplifier must be around 60dB without any bandwidth constraints.

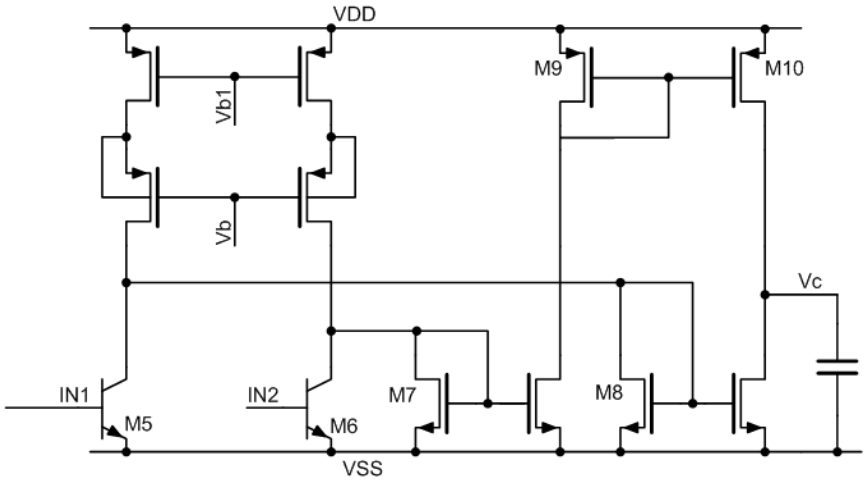


**Figure 2. 7 Structure of the bandgap operational amplifier.**

Figure 2. 7 shows the circuit schematic of the proposed two-stage operational amplifier. The circuit does not use an input differential stage but two grounded BJT transistors ($M_5$ and $M_6$).

The bias current in the differential stage of a conventional operational amplifier is controlled with a suitable current source. However, the current source needs at least a saturation voltage to operate properly, thus subtracting at least 0.15V from the supply voltage budget. The circuit in Figure 2. 7 spares this component. Therefore, the currents in the input stage of the operational amplifier do not need control, being a replica of the current in the bandgap structure. The bias voltage $V_{b1}$, generated within the startup circuit, is also obtained from the bandgap circuit by mirroring the PTAT current of (Figure 2. 6). The signal current generated by the input differential pair $M_5$–$M_6$ is folded and collected by two diode connected MOS transistors ($M_7$ and $M_8$).

The second stage is a push–pull circuit. Since the quiescent value of the output voltage is one $V_{gs,p}$ below $V_{DD}$, the $V_{ds}$ voltages of $M_9$ and $M_{10}$ match, and the systematic offset of the second stage is practically zero as well. Moreover, for the same reason, we achieve excellent power supply rejection ratio and common-mode rejection ratio. The bias current in the operational amplifier matches the current flowing in the bandgap, which in turn is designed low. However, since the bias current of the circuit has a PTAT feature, power consumption will increase proportionally to the absolute temperature.

The compensation capacitance C ensures the stability of the whole bandgap circuit under any operating conditions.

The operational amplifier was designed using ST Microelectronics HF7CMOS version 6.5.

Its simulated features are summarized in Table 2. 2.

| | |
|---|---|
| **Voltage supply** | 5V |
| **Gain** | 76 dB |
| **Phase margin** | 58° |
| **Maximum power consumption (T=125°C)** | 1.7uA |
| **Maximum thermal coefficient (-40<T<125)** | ≈5 ppm/°C |

**Table 2. 2 Performance summary of the operational amplifier used in the bandgap reference.**

### 2.5.2 Start-up circuit

The proposed bandgap reference needs a more effective startup circuit than those usually adopted, consisting of simple pull-up or pull-down capacitors.
In order to turn on the diodes of Figure 2. 7 ($Q_1$ and $Q_2$), a significant amount of current has to flow in the resistors ($R_1$ and $R_2$). The startup circuit shown in Figure 2. 8 ensures that additional current is continuously provided to the diodes and the resistors until the bandgap circuit reaches the proper operating point.

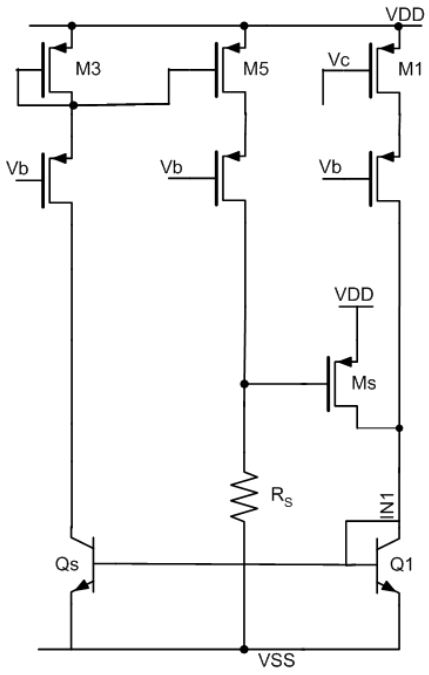


**Figure 2. 8 Schematic of the start-up circuit.**

In particular, if the current in $IN_1$ (Figure 2. 8) is zero, the current in $M_3$ is zero as well, and the p-channel current source $M_5$ is off. The gate of $M_s$ is pulled down to ground, thus injecting a significant current into $Q_1$ and $R_1$ (Figure 2. 8). At the end of the startup phase, when the circuit reaches the normal operating conditions, the current in $M_5$ and the value of $R_s$ used bring the gate of $M_s$ close to $V_{DD}$, thus turning off the startup circuit. To reduce the leakage current in $M_s$ it was necessary to use a very large resistor for $R_s$.

### 2.5.3 Second order bandgap compensation

The simple bandgap circuit in Figure 2. 6 compensates for the temperature dependences of the output voltage at the first order only.

In fact, the voltage $V_{BE}$ of a BJT does not change linearly with the temperature but, according to the relationship:

$$V_{BE}(T) = V_{BG} - (V_{BG} - V_{BE0})\frac{T}{T_0} - (\eta - \alpha)V_T \ln\frac{T}{T_0} \tag{2.7}$$

where $\eta$ depends on the bipolar structure and is around 4, while $\alpha$ is equals 1 if the current in the BJT is PTAT and goes to 0 when the current is temperature independent. The simple bandgap architecture shown in Figure 2. 9 corrects the first term in (2.7) only, thus leading to a second-order temperature dependence.

Various approaches to compensate for the nonlinear term have been proposed in [20], [21]. The basic idea used in this work is to correct the nonlinear term by a proper combination of the voltage across a junction with a temperature-independent current ($\alpha$=0) and the voltage across a junction with a PTAT current ($\alpha$=1). By inspection of the circuit in Figure 2. 6, we observe that the current in the bipolar transistors ($Q_1$ and $Q_2$) is PTAT ($\alpha$=1), while the current in the p-channel MOS transistors is at first-order temperature independent. Therefore, if we mirror the current flowing in p-channel MOS transistors (with $M_4$) and we inject it into a diode connected bipolar transistor ($Q_3$), as shown in Figure 2. 9, across $Q_3$ we produce a $V_{BE}$ with $\alpha$ close to zero. Using (2.7), the $V_{BE}$ of bipolar transistors $Q_3$, $Q_1$ and $Q_2$ can be expressed as:

$$V_{BE.Q_3}(T) = V_{BG} - (V_{BG} - V_{BE0})\frac{T}{T_0} - \eta V_T \ln\frac{T}{T_0} \tag{2.8}$$

and

$$V_{BE,Q_{1,2}}(T) = V_{BG} - (V_{BG} - V_{BE0})\frac{T}{T_0} - (\eta - 1)V_T \ln\frac{T}{T_0} \tag{2.9}$$

respectively. The difference between $V_{BE,Q3}$, $V_{BE,Q1}$ and $V_{BE,Q2}$ leads to a voltage proportional to the non linear term of (2.7), given by:

$$V_{NL} \cong V_{BE,Q_3}(T) - V_{BE,Q_{1,2}}(T) = V_T \ln\frac{T}{T_0} \tag{2.10}$$

Curvature compensation can now be achieved by subtracting from both $I_{M2}$ and $I_{M1}$ a current proportional to $V_{nl}$ .In the complete bandgap circuit shown in Figure 2. 9, this is obtained by introducing resistors $R_5$ and $R_6$ (nominally equal), which

drain from $M_1$ and $M_2$ the required current, thus leading to:

$$V_{out} = V_T(\frac{R_3 \ln(N)}{R_0}) + V_{BE}(\frac{R_3}{R_1}) + V_{NL}(\frac{R_3}{R_{4,5}}) = \frac{R_3}{R_1}(\frac{R_1 \ln(N)}{R_0} V_T + V_{BE} + \frac{R_1}{R_{4,5}} V_{NL}) \quad (2.11)$$

The value of $R_5$ and $R_6$ which leads to the proper curvature correction, derived by comparing (2.9) and (2.11), is given by:

$$R_{4,5} = \frac{R_1}{\eta - 1} \quad (2.12)$$

The simulator helps us to obtain the precise value to optimize the thermal coefficient.

The proposed implementation of the curvature compensation principle requires an additional current mirror and two resistors only.

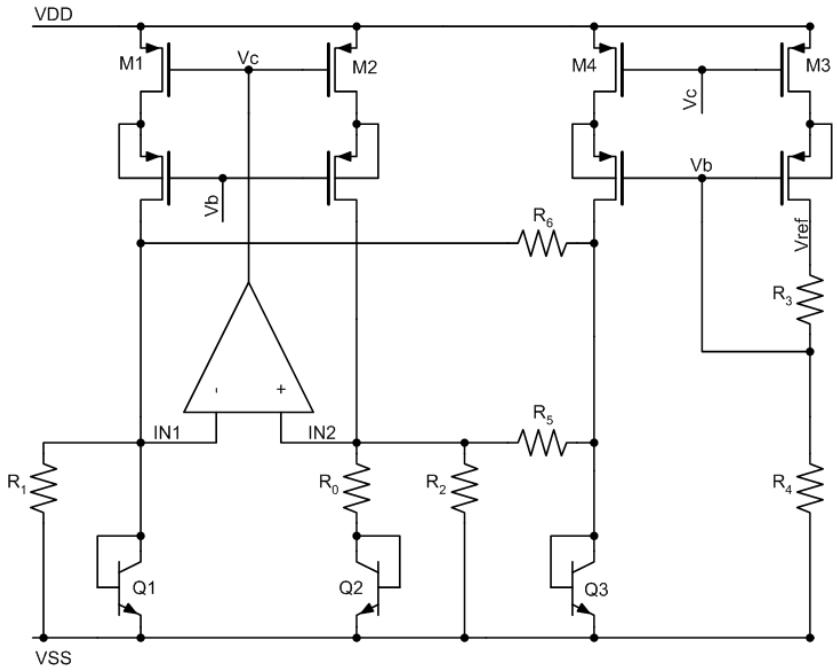


**Figure 2. 9 Bandgap circuit with secon order compensation.**

To obtain a good PSRR we have used cascode loads [12]. This is necessary to satisfy the specifications of line regulation. Besides, current consumption is limited to 1.7μA because some MOS are working in the weak inversion region.

### 2.5.4 Trimming

The typical temperature coefficient is of the order of 5ppm/K, but Montecarlo simulations show in few runs a quite relevant degradation, with peaks also of the order of 30ppm/K. In order to perform a single-shot calibration, it has been decided to measure the output voltage at two different temperatures (T=27°C and T=65°C) at wafer level before packaging and bonding the IC (integrated circuit). The difference between the voltage values obtained at the two temperatures provides information about the variation of the LDO output temperature coefficient of the considered sample (in which both process and mismatch are responsible of drift from the desired value). By correcting the value of $R_0$, exploiting the data obtained from Moltecarlo simulations reported in Table 2. 3, it is possible to lower the temperature coefficient below 5ppm/K in almost all runs.

| #MC | $\Delta V_{OUT}$ | TempCo (before) | $R_0$ (kΩ) adjustment | TempCo (after) |
|---|---|---|---|---|
| **0** | 7.1857e-5 | 5.2969 | +0 | |
| **5** | -7.3709e-5 | 5.6679 | +0 | |
| **14** | 5.5621e-5 | 3.7528 | +0 | |
| **39** | -7.8174e-5 | 5.6853 | +0 | |
| **40** | -7.9051e-5 | 5.7278 | +0 | |
| **49** | -7.8940e-5 | 4.4356 | +0 | |
| **1** | 2.0329e-4 | 9.4569 | +1 | 6.5635 |
| **4** | 2.7593e-4 | 9.8307 | +1 | 6.8512 |
| **18** | 1.4527e-4 | 8.1896 | +1 | 5.5864 |
| **6** | 5.1126e-4 | 14.2854 | +4 | 5.4173 |
| **23** | 4.3414e-4 | 13.2800 | +4 | 7.1002 |
| **26** | 3.8671e-4 | 13.0356 | +4 | 4.1059 |
| **27** | 3.8082e-4 | 12.7040 | +4 | 5.6977 |
| **10** | 5.5917e-4 | 13.7503 | +4 | 5.3873 |
| **13** | 5.6236e-4 | 17.0166 | +4 | 5.6949 |
| **16** | 5.5644e-4 | 15.9561 | +4 | 4.8562 |
| **17** | 4.7418e-4 | 14.0423 | +4 | 4.4635 |
| **19** | 5.9669e-4 | 14.7018 | +4 | 4.9780 |
| **34** | 3.8082e-4 | 13.7040 | +4 | 5.2363 |
| **33** | 6.3117e-4 | 18.3580 | +4 | 4.8491 |
| **43** | 5.1954e-4 | 19.7137 | +4 | 6.2340 |
| **35** | 8.2697e-4 | 20.2540 | +6 | 4.0892 |
| **41** | 8.2808e-4 | 22.6011 | +6 | 5.0866 |
| **31** | 1.0759e-3 | 28.3151 | +9 | 4.9372 |

| | | | | |
|---|---|---|---|---|
| **42** | 1.1062e-3 | 27.0588 | +9 | 6.5601 |
| **37** | 1.2427e-3 | 31.6918 | +9 | 5.5021 |
| **50** | 1.3371e-3 | 33.1388 | +9 | 6.9490 |
| **3** | 1.3626e-3 | 33.7244 | +9 | 5.4708 |
| **2** | -2.0329e-4 | 7.2318 | -1 | 5.4106 |
| **11** | -3.4606e-4 | 7.5957 | -1 | 5.3211 |
| **21** | -1.3574e-4 | 6.6370 | -1 | 4.8006 |
| **25** | -1.8978e-4 | 8.4541 | -1 | 5.2895 |
| **36** | -1.2708e-4 | 8.4643 | -1 | 7.0303 |
| **48** | -1.1023e-4 | 8.3470 | -1 | 6.5746 |
| **47** | -2.8727e-4 | 8.7903 | -1 | 6.7331 |
| **7** | -6.9050e-4 | 13.7075 | -5 | 7.8973 |
| **8** | -7.0483e-4 | 19.0673 | -5 | 7.2348 |
| **20** | -6.4341e-4 | 14.4025 | -5 | 4.5909 |
| **29** | -7.9508e-4 | 19.1730 | -5 | 9.9025 |
| **30** | -6.9790e-4 | 19.1877 | -5 | 4.3221 |
| **32** | -7.5136e-4 | 18.2201 | -5 | 4.4708 |
| **38** | -5.2435e-4 | 12.9392 | -5 | 9.0730 |
| **45** | -4.8915e-4 | 17.9111 | -5 | 5.8613 |
| **9** | -1.1699e-3 | 33.1840 | -9 | 5.8998 |
| **44** | -1.1387e-3 | 31.3893 | -9 | 5.3962 |
| **12** | -1.3831e-3 | 33.1534 | -11 | 5.8910 |
| **24** | -1.4409e-3 | 35.4527 | -11 | 7.5269 |
| **46** | -1.3611e-3 | 33.5094 | -11 | 5.5324 |
| **22** | -1.6380e-3 | 39.9939 | -12 | 4.7108 |

**Table 2. 3 Thermal coefficient trimming table.**

Finally, in order to guarantee, after temperature coefficient calibration, that the absolute output voltage is also correct, a second trimming table is provided (Table 2. 4). We must remind that both corrections must be made in one shot since, during post-fabrication calibration it is not possible to perform multiple measurements and corrections.

| #MC | TempCo (before) | $V_{ref}$ (before) | $R_0$ (Ω) adjustment | TempCo (after) | $V_{ref}$ (after) | $R_3$ (Ω) adjustment | TempCo (final) | $V_{ref}$ (final) |
|---|---|---|---|---|---|---|---|---|
| **0** | 3.2969 | 1.25015 | | | | | | |
| **1** | 7.4569 | 1.24235 | +1k | 4.5635 | 1.24091 | +58k | 4.0075 | 1.25066 |
| **2** | 5.2318 | 1.25136 | -1k | 3.4106 | 1.25280 | -16k | 3.2984 | 1.25008 |
| **3** | 31.7244 | 1.26102 | +9k | 3.4708 | 1.24798 | +16k | 3.8997 | 1.25069 |
| **4** | 7.8307 | 1.25619 | +1k | 4.8512 | 1.25474 | -23k | 5.0932 | 1.25083 |
| **5** | 3.6679 | 1.25450 | +0k | 3.6679 | 1.25451 | -23k | 3.8917 | 1.25060 |
| **6** | 14.0381 | 1.24046 | +4k | 3.4173 | 1.23468 | +99k | 4.0278 | 1.24956 |
| **7** | 11.7075 | 1.24346 | -5k | 5.8973 | 1.25075 | +0k | 5.8973 | 1.25075 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **8** | 17.0673 | 1.25893 | -5k | 5.2348 | 1.26615 | -97k | 4.7749 | 1.24951 |
| **9** | 31.1840 | 1.24588 | -9k | 3.8998 | 1.25919 | -55k | 3.6062 | 1.24981 |
| **10** | 13.4814 | 1.25072 | +4k | 3.3873 | 1.24493 | +28k | 3.1431 | 1.24966 |

**Table 2. 4 Absolute voltage regulator simulated calibration, including both thermal coefficient and $V_{ref}$ compensation.**

## 2.6 ERROR AMPLIFIER

In the design of the error amplifier (EA) we first considered some of the main specifications which have most heavily dictated the choice of topology for the amplifier, and which have caused most difficulties:

- the large range of load capacitance;
- the large range of load current;
- the large range of supply voltage;
- driving both positive and negative currents;
- the low quiescent current.

The schematic of the designed operational amplifer is shown in Figure 2. 10.

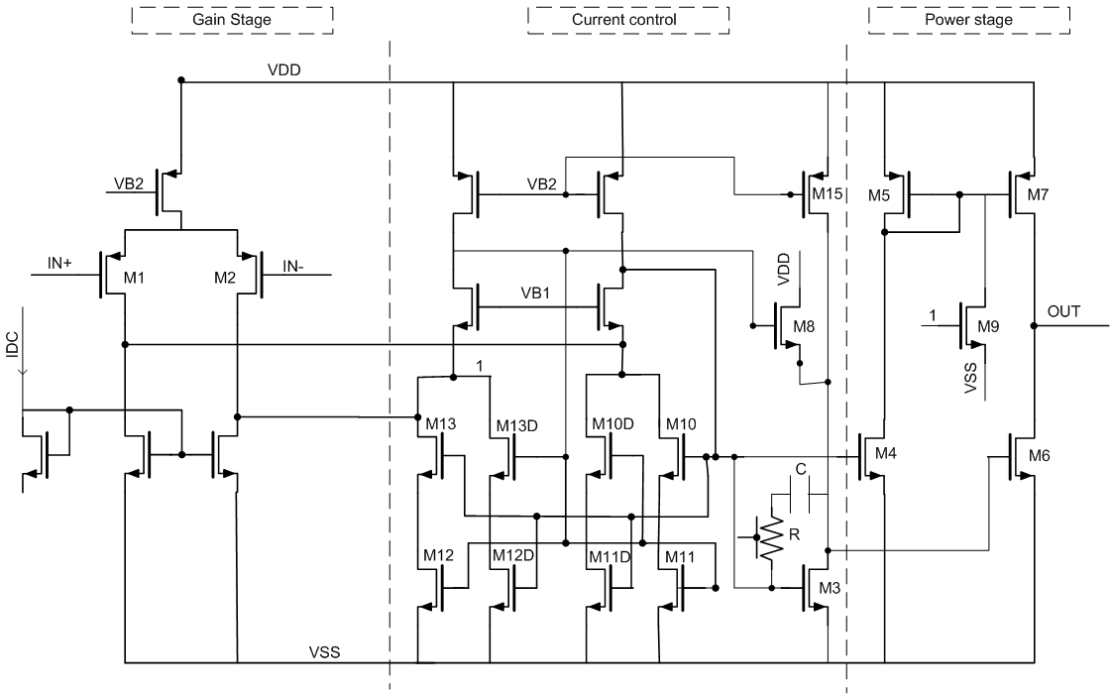


**Figure 2. 10 Schematic of the error amplifier.**

It is made up of a gain stage and a current control stage, which controls the quiescent current of the power stage, which is a push-pull output stage.

Now let us move on to the analysis of the circuit, starting by describing the control circuit for quiescent current in the output branch.

### 2.6.1 Quiescent current control

In class A output stages, the maximum current is equal to the bias current. Class B output stages combine high output current capability with very low quiescent current but introduce crossover distortion. The common-source class AB stage, presents a good trade-off between distortion and quiescent power dissipation. The output transistors are biased with a small quiescent current compared to the maximum output current, which reduces crossover distortion in comparison with class B output stage. To obtain the class AB control of the output stage, a non-linear function such as the one in Figure 2. 11 is necessary and can be accomplished by a translinear MOS circuit [22].

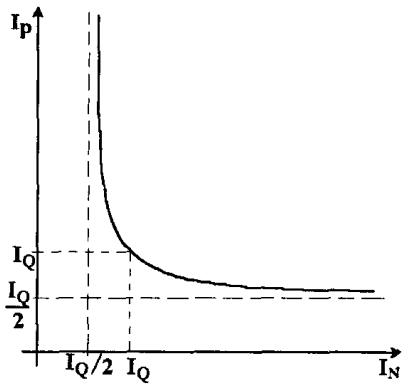


**Figure 2. 11 Function of the control current circuit.**

There are several forms to implement the characteristic represented in Figure 2. 11. One of them, based on the minimum current selector circuit of Figure 2. 12, was used in this work.

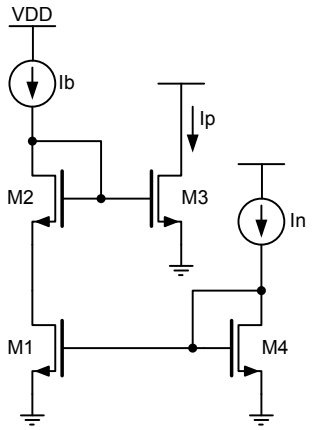


**Figure 2. 12 Schematic of the current control circuit.**

For the analysis of the circuit in Figure 2. 12, assume that all transistors have the same dimensions. When $I_n$ is much larger than $I_b$, transistor $M_1$ operates in the linear region; consequently, $V_{gs,M2}=V_{gs,M3}$ and $I_p=I_b$. When $I_p$ is much larger than $I_b$, the voltage $V_{d,M1}$ increases forcing $M_1$ to operate in saturation and $I_n=I_b$. Finally, for $I_n=I_p$ $V_{gs,M3}$ = $V_{gs,M4}$; consequently, $M_1$ and $M_2$ behave as the series association of two transistors. Therefore, $I_n=I_p=2I_b$.

The minimum current selector circuit as presented in Figure 2. 12 is asymmetric. To convert it into a symmetrical circuit, $M_1$ and $M_2$ are divided into $M_{1A}$, $M_{1B}$, $M_{2A}$, and $M_{2B}$, as shown in **Error! Reference source not found.**.

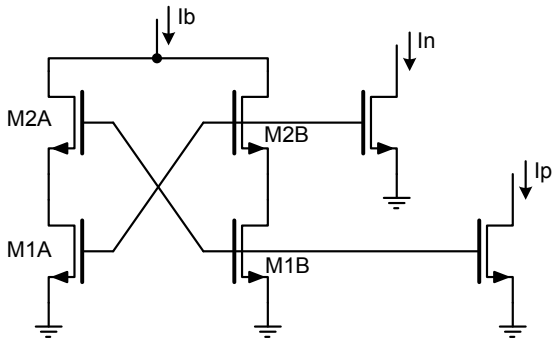


**Figure 2. 13 Modified structure of Figure 2.12.**

The LDO regulator must work with a maximum supply voltage of 5.5V. For this reason many internal nodes in the circuit reach high voltages. In particular, there are differences of gate-source and gate-drain voltages greater than 2.5V. This makes it necessary to use MOS transistors with greater thickness of gate oxide and consequently with greater threshold voltages. This makes the biasing of the circuit more problematic when the voltage supply is 1.8V and the load current is high. Therefore, to ensure that the LDO works correctly also in these conditions, it is necessary to enlarge the width W of the channel of the power transistors to reduce their gate voltage. There is consequent enlargement of the gate capacitance that further complicates the stability study.

### *2.6.2 Description of the LDO regulator*

Refering to Figure 2. 10 we can analize the circuit of LDO regulator.

The gain stage is formed by a differential amplifier ($M_1$ and $M_2$), followed by a cascode stage. The second gain stage is a push-pull amplifier ($M_6$ and $M_7$)

which is the power stage as well. The current control stage is formed by two minimum current selectors, given by transistors $M_{10}$-$M_{13}$ and $M_{10D}$-$M_{13D}$. The output quiescent current is given by:

$$I_{M7} = 2I_{M1}\frac{(W/L)_{M4}}{(W/L)_{M10}} \bullet \frac{(W/L)_{M7}}{(W/L)_{M5}} \tag{2.13}$$

The power transistor $M_7$ in Figure 2. 10 is particularly critical. Its dimensions (in terms of width of the channel) are very large. It must be able to supply a current of 5mA, and besides it must do so in such a way that its gate voltage maintains a value which enables the circuit to work correctly also at 1.8V and with maximum current.

Observing the circuit in Figure 2. 10 it is evident how the gate voltage of $M_7$ must be at least equal to:

$$V_{g,M7} = V_{DD} - V_{TP} - V_{OV} \tag{2.14}$$

The fact that the values of load capacitance and load current change so much complicates the stability of the circuit: the output pole, due to the output resistance and load capacitance, moves a lot. Moreover, to drive currents this large (±5mA) it is necessary to use power MOS transistors with corresponding large parasitic capacitance which introduces poles at low frequencies. To ensure stability to the circuit, we have decided to drive the gate of $M_7$ with low impedance in order to pull the pole to higher frequency; and we have put an R-C network to reduce the effect of the pole associated with the gate of $M_6$ by means of a zero. Because the output capacitance is large (minimum capacitance 100nF) we have decided to adopt a compensation in which the dominant pole is the one associated with the output node.

To drive $M_7$ a MOS ($M_5$) in diode configuration has been used. In this way the pole, due to the parasitic capacitance of MOS $M_7$ and the resistances ($R_{ds}$) of the transistors $M_4$, $M_5$ and $M_9$, is placed at higher frequency.

The dimensions of $M_6$ are smaller than those of $M_7$. $M_6$ is driven by the drain of the MOS $M_3$ which, along with $M_{15}$ creates an intermediate branch between the first and the second stage. In this stage it is possible to introduce a zero, necessary to stabilize the circuit by way of the R-C network.

The transistors $M_8$ and $M_9$, driven by the appropriate signal, respectively inject and absorb a large current for some μs. Therefore capacitor C in Figure 2. 10 is quickly charged and discharged and the amplitude of overshoot is reduced

during the transient response if the load current goes from -5mA to 5mA quickly. This will be more evident from the simulations.

To control the quiescent current in this branch we must use a specific control circuit. Moreover, the low current consumption required by the specifications makes the stabilization of the operational amplifier and the transient response more complicated.

## 2.7 NOISE FILTER

It is necessary to put a filter between the BG and the operational amplifier (shown in Figure 2. 14) to reduce the noise of the first stage. This is the main source of noise and also the first stage of the chain, while the noise of the second stage is divided by the gain of the first. During the initial phase the MOS transistor $M_{P1}$ remains ON for some ms. Therefore when the output voltage reference is stabilized, the transistor turns OFF and, due to its very high resistance whilst OFF and due to the capacitance C, a filter is created which cuts the bandwidth to a low frequency. $M_{P0}$ and $M_{N0}$ form the control circuit for $M_{P1}$ and are driven by a start-up signal.

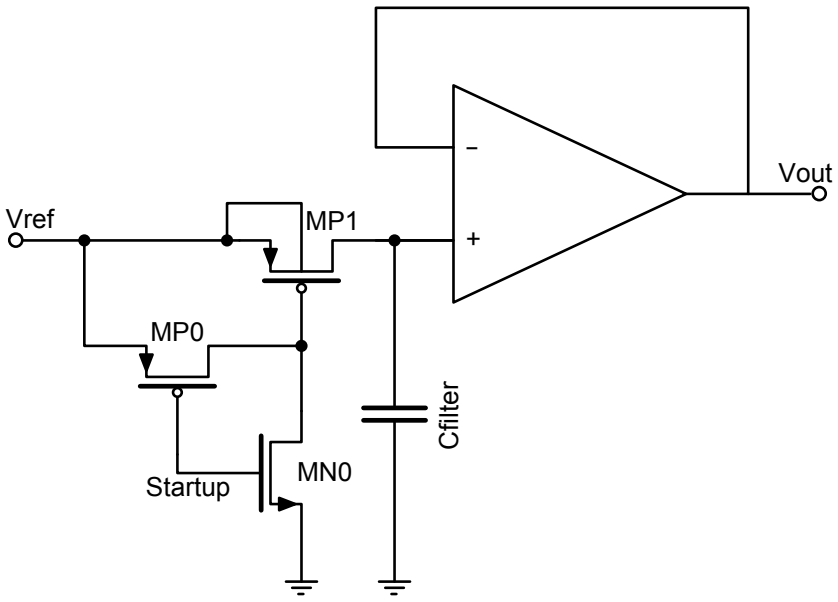


**Figure 2. 14 Block scheme of the filter.**

## 2.8 SIMULATIONS

In this paragraph simulations results will be presented. Three parameters describe the operating performance of a linear regulator:

- dc- and ac-regulating (accuracy) performance,
- power characteristics,
- operating requirements.

The regulating performance refers to the ability to regulate its output against variations in its operating environment. The metrics used to gauge this performance include load regulation, line regulation, power-supply rejection, temperature drift, transient load-dump variations, and dropout voltage. All these parameters essentially portray the behavior of the circuit with respect to load current, input voltage, and junction temperature. Quiescent-current flow, sleep-mode current, power efficiency, and current efficiency as well as dropout voltage, indirectly, depict the power characteristics of the regulator. Sleep-mode current is the current flowing through the circuit while disabled, if an enable-disable function exists, or during low-performance mode (i.e., low-bandwidth setting). Current efficiency refers to the ratio of load to input current, which is especially important during low load-current conditions.

The operating limits of the input voltage, output voltage, output capacitance (and associated ESR), and load current, define the environment within which the regulator must operate functionally and within parametric compliance.

In the following paragraphs simulations results of the designed LDO regulator and bandgap will be presented.

### *2.8.1 Temperature drift*

In more generalized terms, any variation in the reference propagates to the output of the regulator through the equivalent closed-loop gain of the regulator. As such, any temperature effects on the reference, as in the case of ripple-rejection analysis with supply-derived noise, also have adverse effects on the regulated output. These effects are in addition to the temperature effects of the regulator, which manifest themselves through temperature dependence in the input-referred offset voltage. The metric that gauges the extent of the impact of

temperature on the output is fractional temperature coefficient (TC), which is the percentage variation of the output in response to temperature changes per degree of temperature change.

The temperature coefficient of the voltage regulator is defined as the difference between maximum and minimum voltage divided by the nominal voltage and by the temperature range:

$$TC = \frac{(V_{Out(T1)} - V_{Out(T2)})}{V_{REF}} \bullet \frac{1}{(T_1 - T_2)} \tag{2.15}$$

where $T_1$-$T_2$ is the temperature range and $V_{REF}$ is the nominal output of the BG.

In Figure 2. 15 is shown the temperature coefficient (TC) of the voltage regulator. It is of the order of 5ppm/K and satisfies the specifications in Table 2. 1 of 10ppm/K. The value of TC obtained is less than that required, because after the trimming and packaging there can be a small worsening of the temperature coefficient.

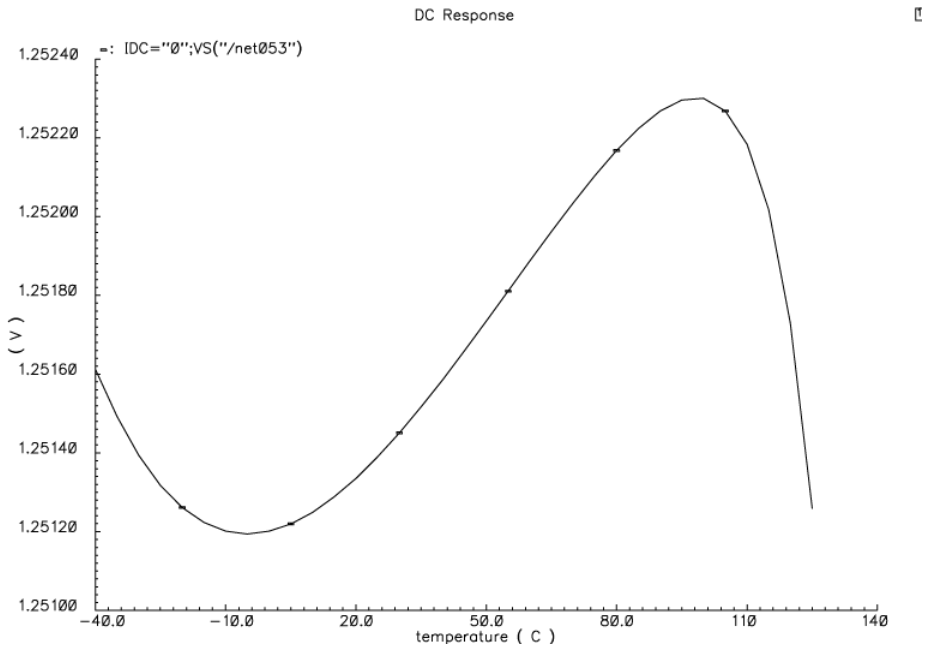


**Figure 2. 15 Simulation results of the temperature coefficient of the voltage regulator.**

Figure 2. 16 shows the TC obtained from 100 Montecarlo simulations, including both process variations and mismatch, the maximum value obtained is less than 40ppm/°C.

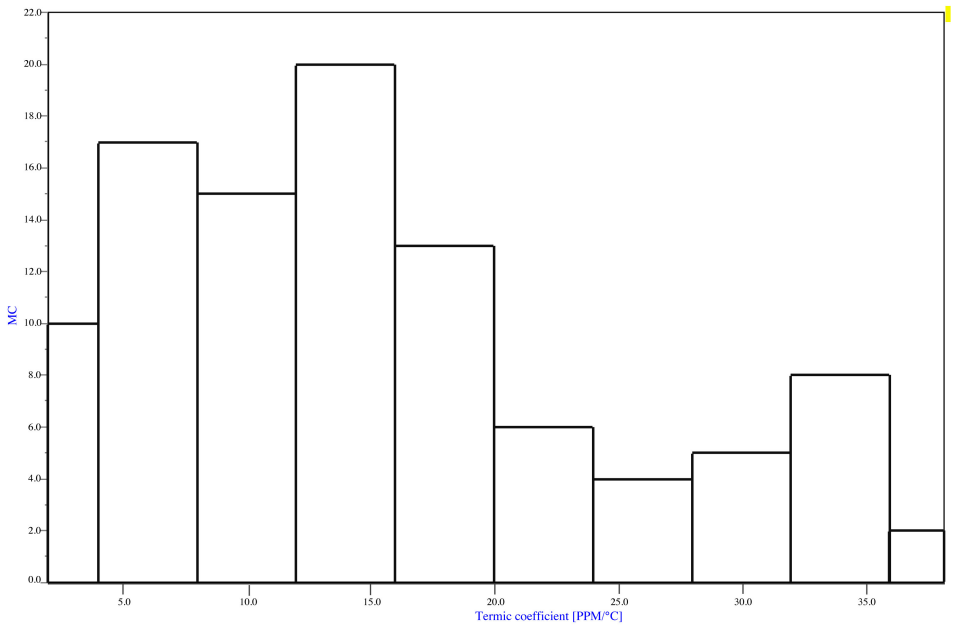


**Figure 2. 16 Montecarlo simulations of the TC.**

### *2.8.2 Transient response*

According to the specifications in Table 2. 1, the output voltage must be 1.25V with an error margin of 0.1% in 2ms, a load capacitance of 1uF, no load current and a voltage supply of 5V. To keep within these specifications, it is important both that the voltage reference charges the output capacitance quickly and that the error amplifier has sufficient bandwidth. The main output capacitance of bandgap is that of the filter, which is 40pF. From Figure 2. 17, and in particular from its close-up (Figure 2. 18), it can be seen that its settling time is 1.7ms, being in specification.

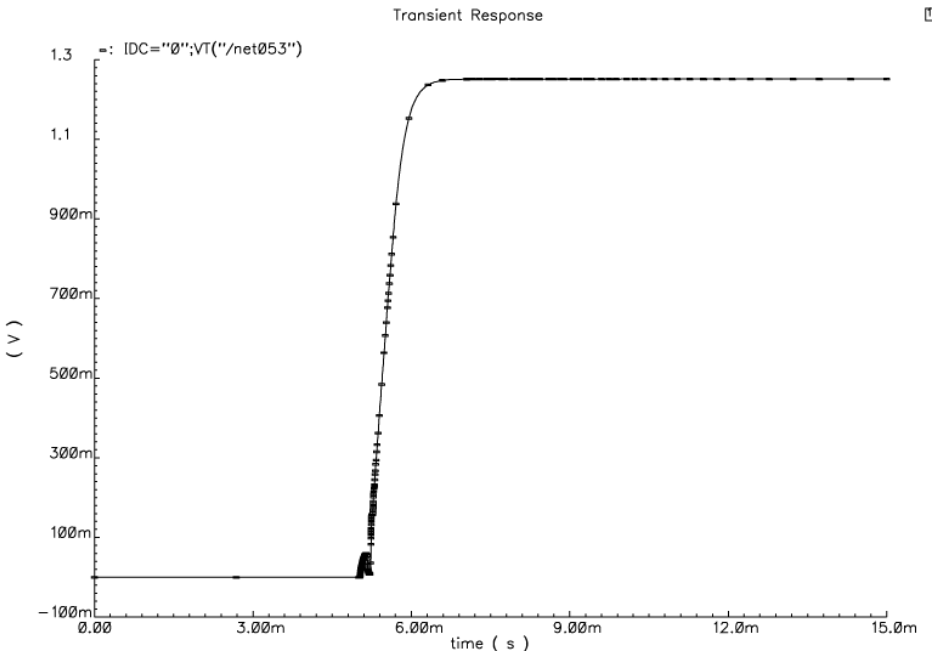


**Figure 2. 17 Transient response of the LDO regulator.**

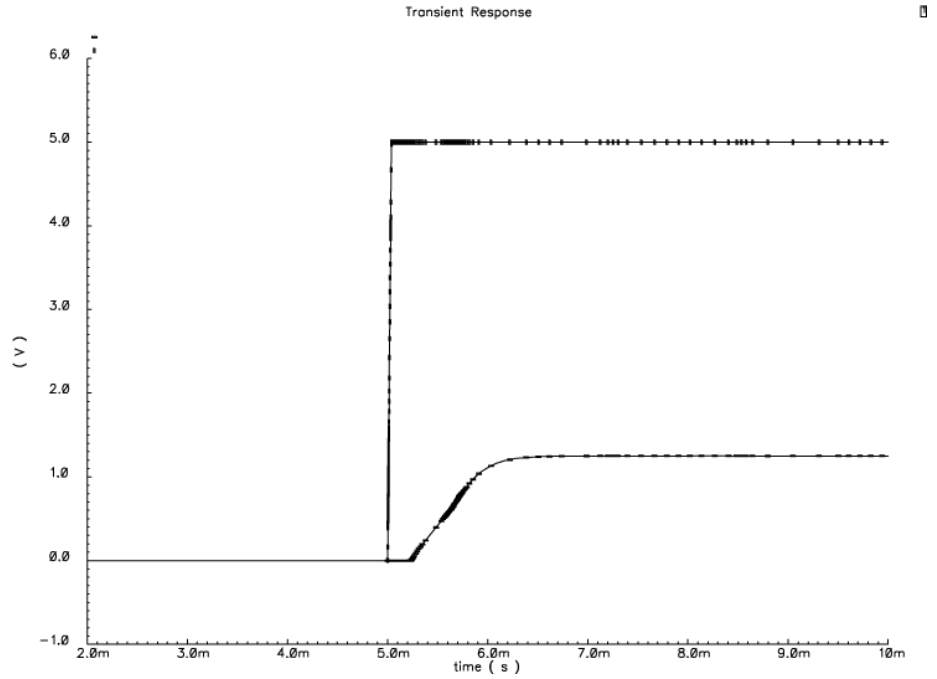


**Figure 2. 18 Close-up image of the transient response of the LDO regulator.**

### *2.8.3 Load regulation*

Voltage variations in the output ($\Delta V_{out}$) resulting from dc changes in load current ($\Delta I_{Load}$) define the load regulation (LDR) performance, which ultimately constitutes an ohmic voltage drop, that is, a linearly load-dependent voltage drop at the output of the regulator.

The specifications require a maximum value for load regulation of 100ppm/mA. This value is found using the formula:

$$C_{Load\,\mathrm{Re}\,g} = \frac{(V_{Out(T1)} - V_{Out(T2)})}{V_{REF}} \bullet \frac{1}{(I_1 - I_2)} \tag{2.16}$$

where the quantity ($I_1$-$I_2$) is the variation of the load current and $V_{REF}$ is the nominal output of the BG.

In Figure 2. 19 it can be seen how the maximum variation of the output voltage, over the whole range of temperatures and with a load current which goes from –5mA to 5mA, is equal to 880μV. The curves in Figure 2. 19 were obtained forcing in the output node, with an ideal current generator, ten different currents from –5mA to +5mA. Therefore from formula (2.16) we get a value of load regulation equal to 6 ppm/°C. Figure 2. 20 shows a close-up of the LR of the proposed LDO shown in Figure 2. 19.

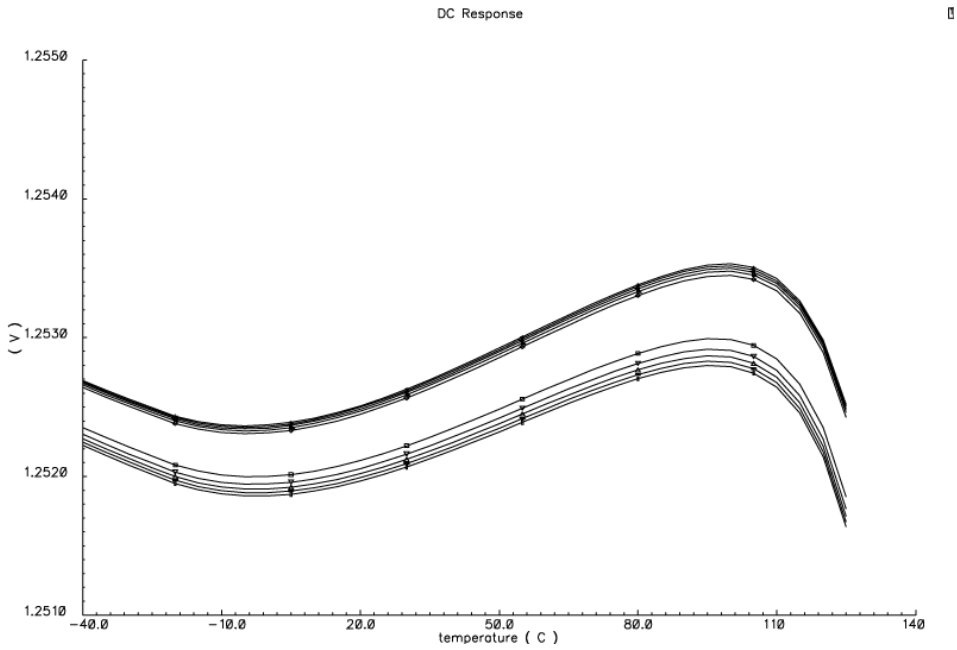


**Figure 2. 19 Simulated LR of the LDO regulator.**

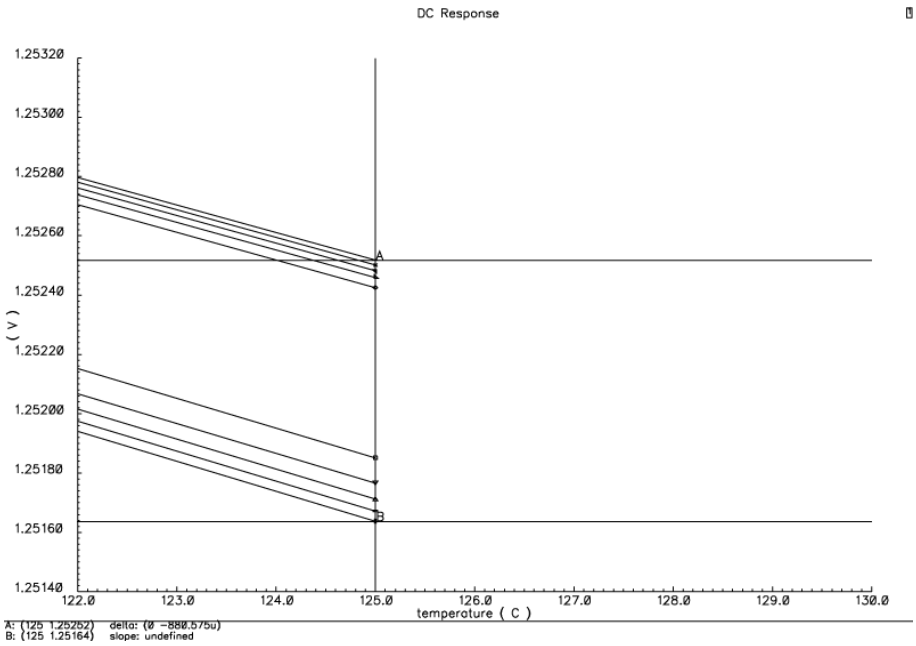


**Figure 2. 20 Close-up of the LR of the LDO regulator.**

### *2.8.4 Line regulation*

Line regulation (LNR) performance, like load regulation, is also a dc parameter and it refers to output voltage variations arising from dc changes in the power supply, in other words, to the low-frequency supply gain of the circuit.

The specifications require a maximum value for line regulation of 100ppm/V. This value is found using the formula.

$$C_{Line\,Reg} = \frac{(V_{Out(T1)} - V_{Out(T2)})}{V_{REF}} \bullet \frac{1}{(VDD_1 - VDD_2)} \tag{2.17}$$

where the quantity ($V_{DD1}$-$V_{DD2}$) is the range of variation of the power supply and $V_{REF}$ is the nominal output of the BG.

In Figure 2. 21 we can see how the maximum variation of the output voltage, over the whole range of temperatures and with a variation of supply voltage of 3.7V (from 1.8V to 5.5V), is equal to 280μV. Therefore from formula (2.17) we get a value of line regulation equal to 66ppm/V.

Figure 2. 22 shows a closer view of Figure 2. 21.

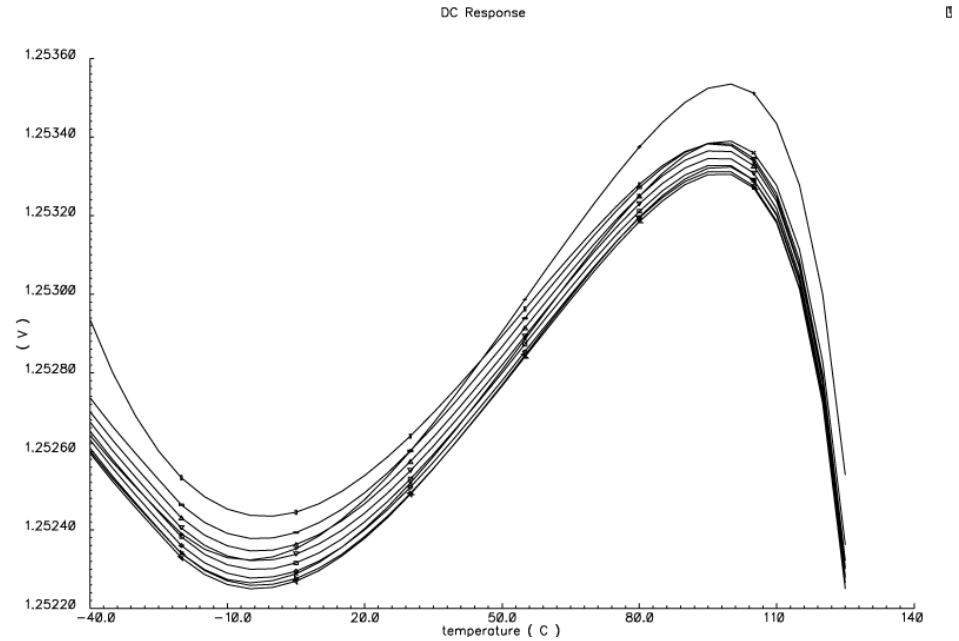


**Figure 2. 21 Simulated LNR of the LDO regulator.**

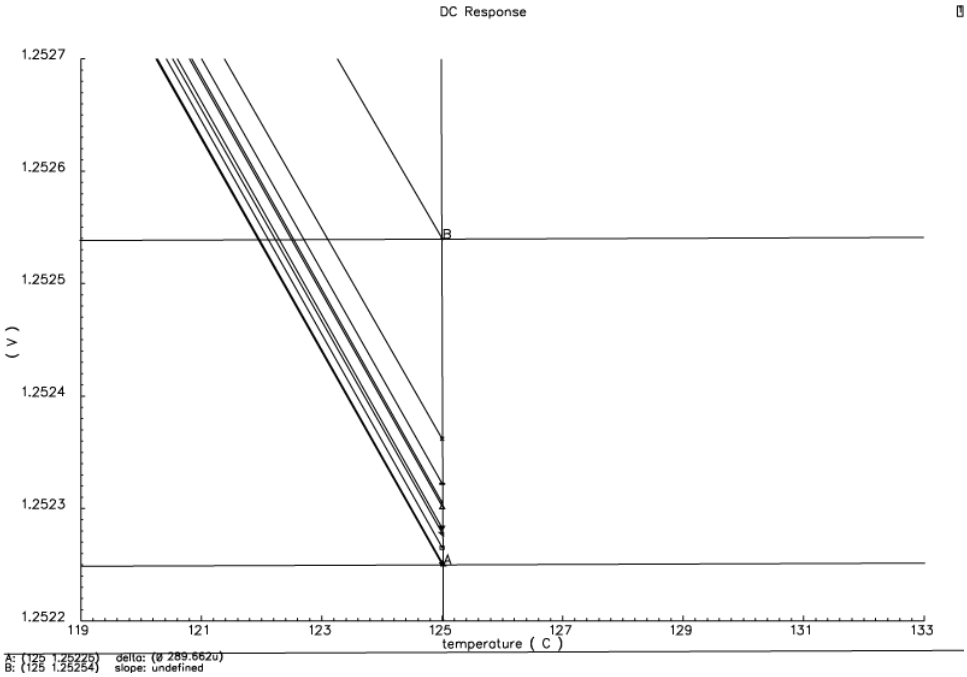


**Figure 2. 22 Close-up of the LNR of the LDO regulator.**

## *2.8.5 Transient variations*

Transient variations are a very critical aspect of this type of circuit. Figure 2. 23 shows a simplified LDO schematic for the purpose of transient analysis which is described as follows.

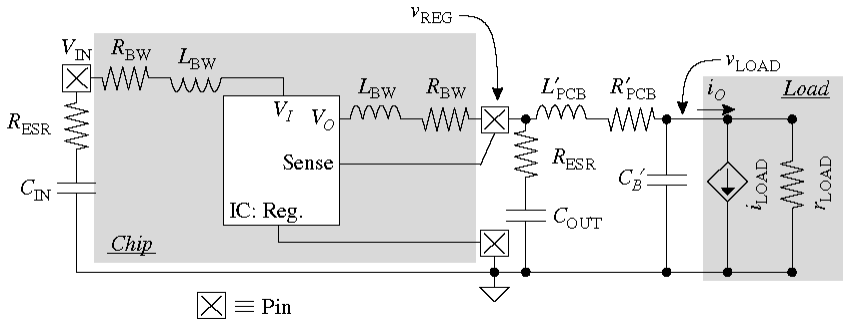


**Figure 2. 23 Simplified LDO schematic for the purpose of transient analysis**

In a worst-case transient load-dump event, the load current ramps up or down to its extreme values in a short time. Considering a positive load dump, for instance, when load current rises quickly, the LDO is at first unable to supply the load because it needs time to react and adjust the output voltage (i.e., it has limited bandwidth). Capacitors $C_{out}$ (Figure 2. 23) therefore supply this initial jump in current. The net effect is an instantaneous voltage drop across $L_{PCB}$ ($V_L = L'_{PCB} \cdot dI_{LOAD}/dt$) that lasts as long as $I_{LOAD}$ is changing, another instantaneous voltage drop across $R_{ESR}$ and $R'_{PCB}$ ($\Delta I_{LOAD} \cdot (R_{ESR} + R'_{PCB})$) and a voltage-droop response across $C_{OUT}$, the latter two of which last until the LDO responds and supplies the full current ($\Delta I_{LOAD}/BW \cdot C_{OUT}$). All of these parasitic effects amount to an undesired transient voltage drop in load voltage $V_{LOAD}$. Eventually, the circuit supplies the full load and again reaches steady-state operation. For negative load dumps, similar effects occur and $V_{LOAD}$ temporarily rises above its ideal targeted value.

Transiently induced voltage variations also contribute to the overall ac accuracy of the regulator. The worst-case variation occurs when the load current suddenly goes from its lowest rated value to its maximum peak, or vice versa, which comprise the positive and negative load-dump conditions.

To reduce the effect of load dump in this project we use two MOS transistors ($M_8$ and $M_9$) which, driven by two signals from inside the circuit, reduce the transient overshoot, injecting much current for a few µs.

### 2.8.6 Load transient

Now we examine the transient response of the output voltage to a jump of the current load from –5mA to 5mA (Figure 2. 24). We can see that the voltage overshoot is not above 70mV. The time taken to restore, which is the time taken for the output voltage to return to the desired voltage (taking into account the error margin of 0.1%) is less than 200µs, so it satisfies the specification in Table 2. 1 Specifications of the designed circuit..

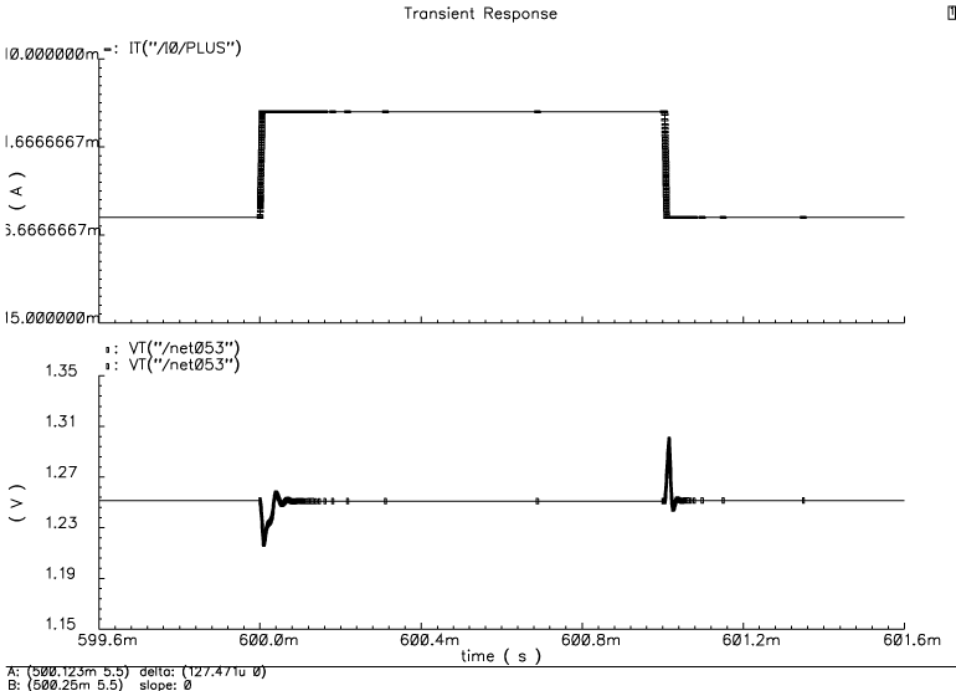


**Figure 2. 24 Transient response to a jump of the current load from -5mA to 5mA.**

### 2.8.7 Line transient

Figure 2. 25 shows the response of the output voltage to a voltage step of amplitude 0.5V on the power supply. The overshoots are only a few mV and the time taken to restore is less than 100µs. The results satisfies the specification in Table 2. 1 Specifications of the designed circuit..

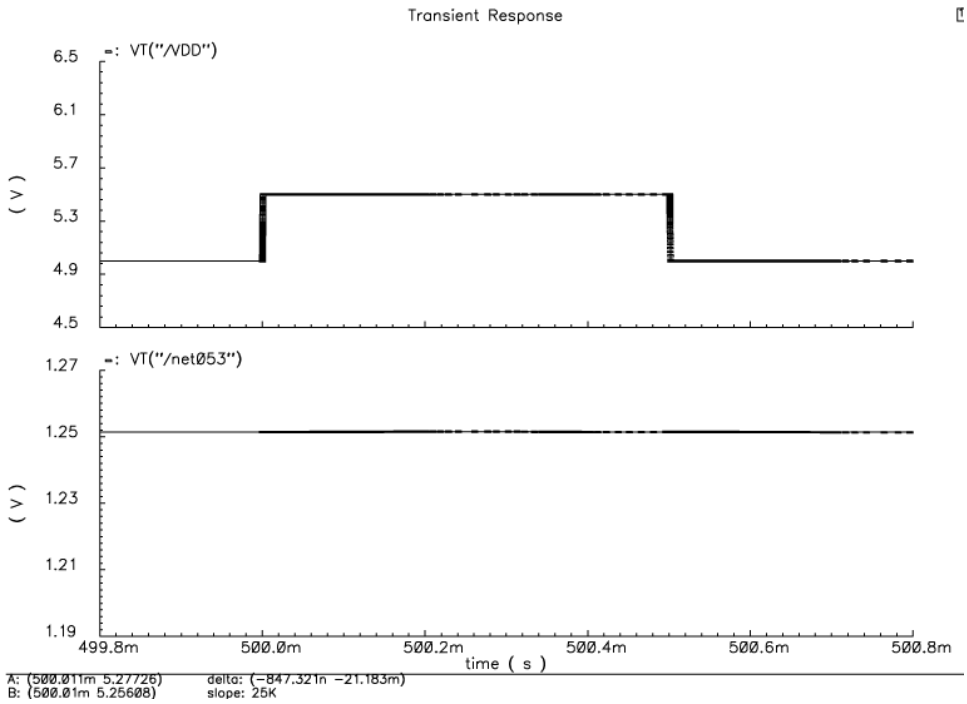


**Figure 2. 25 Transient response of the output voltage to a variation of the supply voltage of 0.5V.**

### 2.8.8 Noise

To verify that the specification on the noise is respected we can refer to **Figure 2. 26** in which the output noise, from 0.1 Hz to 10Hz is shown. The value of noise integrated in this band is equal to 16μV.

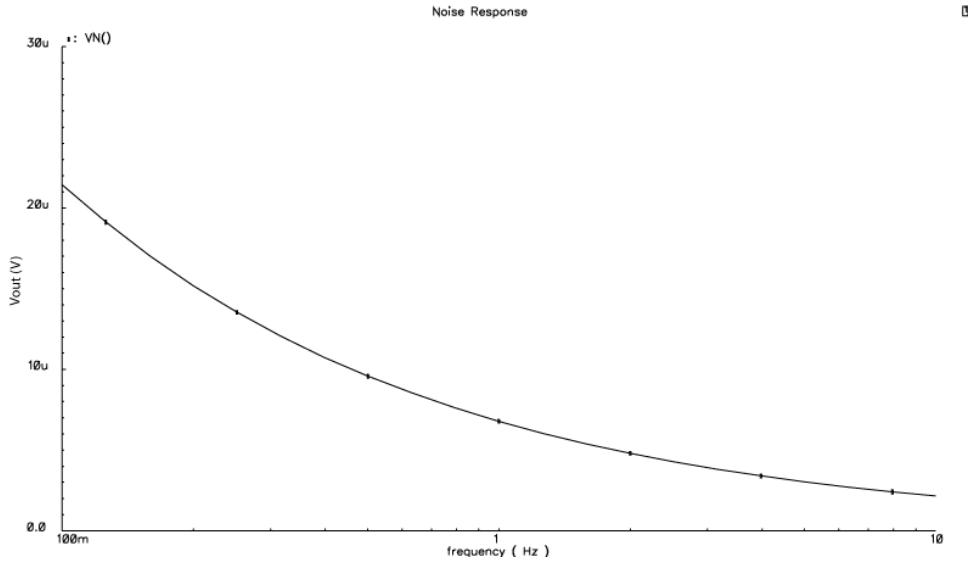


**Figure 2. 26 Noise.**

### 2.8.9 Current consumption

Figure 2. 27 shows the current consumption of the BG and LDO over all the temperature operating range as result of 100 Montecarlo simulations with process variations and mismatch. The current consumption is less than 6μA and the control of quiescent current works correctly.

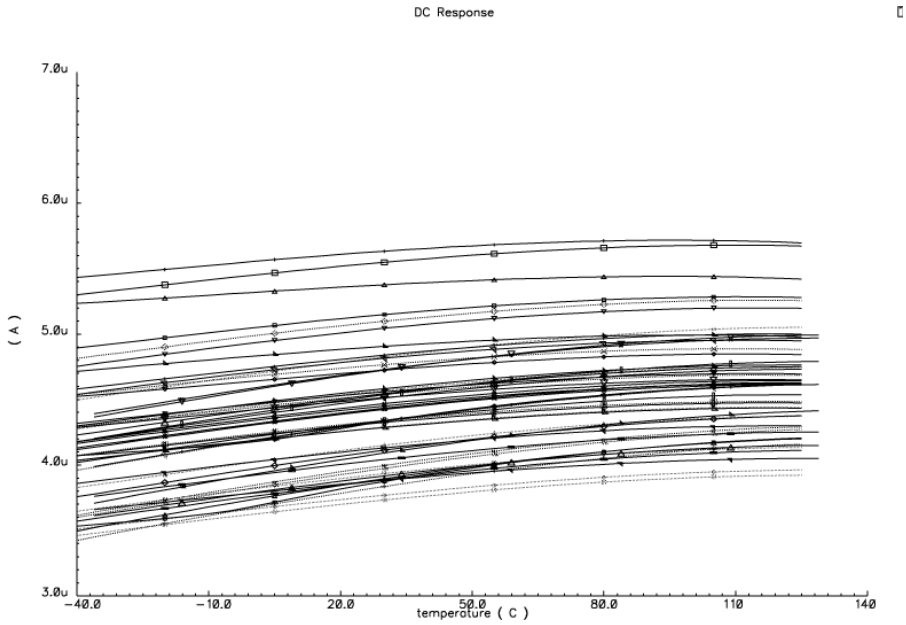


**Figure 2. 27 Current consumption as results of 100 Montecarlo simualtions over the temperature range of operation.**

# *Chapter 3*

# ALGORITHMS TO DETECT THE FALLS IN DOMESTIC ENVIREMENT

## 3.1 INTRODUCTION

Over the past few years, research has been increasingly focusing on building systems for observing humans and understanding their appearance and activities. Furthermore, home assistance and protection, especially for the elderly, has become an important topic in sensor systems. In fact, the European population that is 65 years or older and may be in need of assistance is becoming wider and wider, i.e. of the order of 40 million in year 2000 and expected to be around 55 million before the year 2025 [1]. A recent survey of systems for the automatic detection of falls of elderly people is reported in [2]. Solutions based on this kind of approach are important not only for the health aspects regarding the assisted people, but also for social advantages as the possibility for elders to live longer in their own familiar environment and to care-giver institutions to employ more efficient and optimized services in a more convenient way. For this reason, various projects and consortia have been formed and funded under the coordination of the European Community, including the Netcarity project [23] , within which the work described in this thesis has been developed. From the bare sensing technology development

point of view, the aim of the project is the design of a networked multisensory system, envisaged for assisting older people at home in terms of health care, safety and security. In particular, in this work, emerging sensing technologies [2], [24] are exploited in order to detect possible falls of older people in the home environment, delivering an alarm flag to emergency operators or relatives. Traditionally, many of these systems are employed as stand-alone recognition devices. In contrast, this work aims to eventually lead to a data fusion approach in order to provide robustness to the framework and to reduce false alarms typical for this type of systems. The developed architecture includes three different sensors: a 3D time-of-flight range camera, a wireless wearable MEMS accelerometer and an off-the-shelf microphone. These devices are connected with ad-hoc interface circuits to a central host embedded PC (e_PC) that receives and processes the information employing a multi-threading approach. All information gathered from the sensors is only temporarily stored on the e_PC hard-drive for processing and is subsequently discarded; only alarms and their motivation are transmitted to care-givers outside the home, in order to ensure privacy for the assisted person. To train and evaluate the performance of the developed system, data collection based on the guidelines reported in [2] was conducted. In the following sections, the proposed architecture is described, and preliminary experimental results are reported.

Two different "Pilot Sites" with different cultural and sociological background from the central/northern part of Europe (The Netherlands) and southern Europe (Italy), chosen for their pre-existing know-how and good practices, and including all the relevant stakeholders, have been choosen:

- In The Netherlands (Eindhoven): an urban area with “everything” nearby; to some extent, an anonymous and closely confined test site with all required services at walking distance.
- in Italy (Trento), two test sub-sites: the first one in a rural (Alps valleys) and the other in an urban area. This configuration will require a greater involvement of all relevant actors and stakeholders (care and medical services, social services, local governmental bodies, legislative bodies, training sites, third age universities, non-profit organizations, etc.)

## 3.2 FALL DETECTOR FRAMEWORK OVERVIEW

The hardware framework is reported in **Error! Reference source not found.** and the block diagram of the complete system is depicted in Figure 3. 2. The information provided by the 3D camera allows us to describe the environment quantitatively, in terms of appearance and depth images at QCIF resolution. In addition, a wearable three-axis accelerometer [1], by means of a ZigBee wireless module, delivers acceleration components to the e_PC, which recognizes specific patterns related to falls. Finally, acoustic scene analysis is performed.

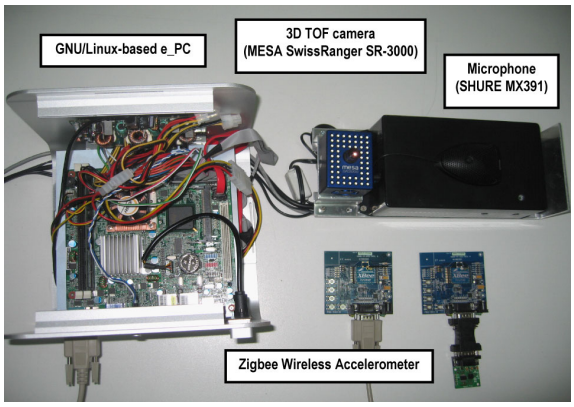


**Figure 3. 1 The proposed position detector framework architecture based on commercial sensors.**

As already mentioned, our goal is to improve the state-of-the-art by exploiting a multi-sensory approach for fall detection, adopted to minimize false alarms. For this purpose, the data delivered by each sensor is first processed by separate algorithms, as described in this work. Eventually, data fusion over a given time window will be performed subsequently by the e_PC. A brief outline of the employed devices is given in the following.

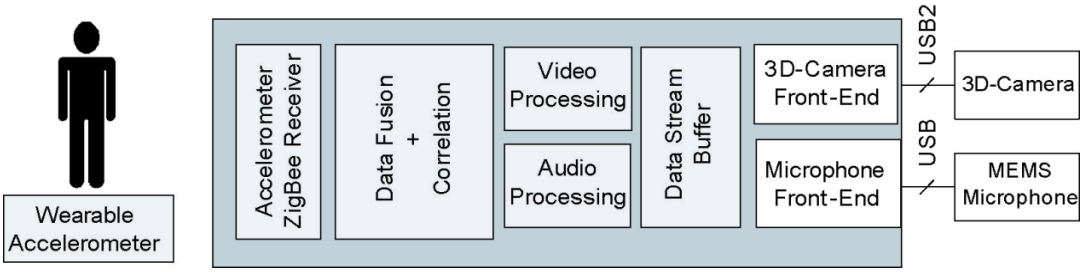


**Figure 3. 2 Block diagram of the proposed framework.**

### 3.2.1 3D Camera

The vision sensor is a time-of-flight camera MESA SwissRanger 3000 [26], able to measure both the gray scale of the scene and the depth measure for each pixel. The information coming from the camera is processed to extract the blobs (moving regions), detect moving people and track them in the scene. The employed commercial 3D camera works with an integrated, modulated infrared light source. The target depth is estimated by measuring the phase shift of the signal round-trip from the device to the target and back. Due to the modulation frequency (20 MHz), the device provides a non-ambiguity range of 7.5 meters, and it can be properly used in indoor environments. The built-in band-pass optics remove the background light, allowing the use of simple computer vision algorithms. The data provided by the camera via USB 2.0 connection include both raw input and on-board FPGA-processed data for noise reduction, correction, and 3D coordinate evaluation, so that for each frame the vision-based fall detector computes almost 396 KBytes of information.

### 3.2.2 Wireless accelerometer

The wearable wireless accelerometer sub-system is made up of three main blocks: the 3-axial MEMS LIS3LV0 [27] sensors with $I^2C$/SPI digital output, a low power FPGA with embedded fall detection routines and a ZigBee radio module to deliver potential fall alarms together with their level of confidence to the coordinator. Figure 3. 3 is a photograph of the wireless accelerometer prototype.

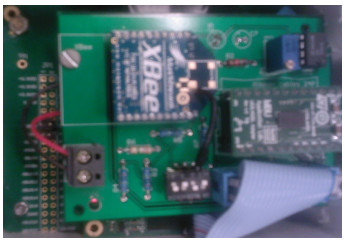


**Figure 3. 3 Accelerometer sub-system prototype photograph.**

The device may operate between 2.2V and 3.6V, allowing the use of batteries without additional voltage regulators. The acceleration bandwidth which may be processed by the micro-machined device is about 150Hz, which has been demonstrated to be sufficient to detect falls in preliminary testing. Also full-scale values available for the chosen device, which lie between ±1g to ±6g are satisfactory for this system. In the preliminary data collection, the full-scale has

been set to ±2g, in order to provide maximum sensitivity, while avoiding saturation. Analog acceleration information is processed by the FPGA and delivered to the wireless module as a UART serial data stream (in streaming mode). The employed ZigBee wireless module fulfills this requirement, being able to transmit data from 9600 bps to 250 kbps. With the available acceleration full-scale values, the 10-bit acceleration information leads to an output sensitivity from 0.003g for minimum FS range to 0.012g for maximum FS range. This preliminary module, as mentioned, has been basically developed for studying the algorithms and has not yet been optimized in terms of power efficiency. In the final device, fall detection algorithms are loaded on an onboard FPGA, and the acceleration streaming mode is replaced by a fall-flag transmission mode, turning on the transmitter only in case of an alarm.

### *3.2.3 Microphone*

In order to obtain fall acoustic patterns or requests for help, a commercial Shure microphone is also employed, directly connected to the 16-bit audio card of the embedded PC. The Shure Microflex MX391 series microphones [28] are small surface-mounted electret condenser microphones, designed for use on conference tables, stage floors, and lecterns. Their high sensitivity and wide frequency range make them suitable for picking up speech and other acoustic events in sound reinforcement and recording applications.

## 3.3 EXPERIMENTAL DATA ALGORITHMS

The following sub-sections describe the architecture of the single sub-system algorithms, whose outputs represent suitable input variables for the envisaged sensor fusion process. Each sub-system presents a set of different possible events recognized by the processing algorithms, together with a probability distribution which indicates the confidence level of the recognized event (fall). For every given sensor, an example of data acquisition and interpretation is also given. The data acquisition campaign has been performed with 13 different actors that produced more than 450 events including approximately 210 falls. A total of 32 sessions are annotated with different labels for each type of fall. Among them, 20 sessions are used for training, 5 sessions are used as a held-out set, and 7 sessions (containing data from 3 separate actors) are used for algorithm testing. Detection performance is evaluated in terms of reliability –

i.e., the number of correct system output events divided by the number of system output events – and efficiency – namely, the number of correctly detected reference events divided by the number of reference events.

### *3.3.1 3D imaging analysis*

The proposed framework employs a people detection and tracking algorithm to provide quantitative information about the person in the scene and to determine the distance of its center-of-mass from the floor. Moreover, an ad-hoc software allows us to detect a fall event by thresholding the center of mass distance to the floor. The 3D vision-based fall detector has been implemented in C++ on a Linux-based architecture. The main steps of the algorithmic framework are discussed in the following. In the first activity, a background model is estimated, and a depth image of the scene is provided, where no people or moving objects are present. The background modeling is realized according to a statistical technique known as mixtures of Gaussians (MoGs) [29]. The detection of a moving person is obtained through Bayesian segmentation. The use of depth information provides important improvements in the segmentation, since it is not affected by typical problems of traditional passive vision, such as shadows, mimetic appearances and extreme illumination conditions. A particle filter (Condensation algorithm [30]) is used to track the person in the scene, allowing to obtain its movement. Once the foreground is extracted (people silhouettes), the vision-based sub-system analyzes the silhouettes to check whether the condition of a fall event is met. A crucial step is the extraction of reliable features to detect critical behaviors (falls). For the proposed architecture, the distance of the centroid of the segmented blob from the ground-floor is evaluated through a system coordinate changing transformation.

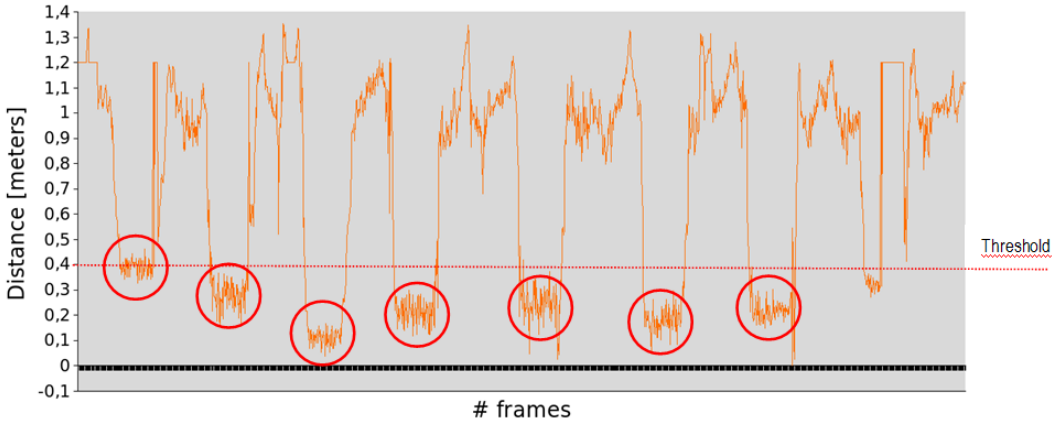


**Figure 3. 4 Pattern of the centroid height.**

Again, a fall event is detected by thresholding the height of the centroid (in meters) from the floor. In particular, the fall event is characterized: (1) by a centroid distance lower than a prefixed value (0.4 meters constitute a good choice in our experimental setup to avoid false alarms) and (2) an unchangeable situation (negligible movements in the segmented image) for at least 15 consecutive frames (about 1.5 seconds). Figure 3. 4 shows the typical pattern of the centroid distance when fall events occur (red circles): in these situations the distance is lower than the threshold, and the ad-hoc software detects the critical events. In order to evaluate the performance of the 3D vision-based fall detector, a two-class (fall, non-fall) clustering approach has been defined, and the confusion matrix has been studied to evaluate performance metrics (**Error! Reference source not found.**). In particular, the performance is affected by several misclassifications due to total occlusion situations (i.e., the person falls behind a big object). Again, the performance deteriorates when poor segmentation occurs due to an unstable background model (i.e., the fall occurs during the transient period of background modeling).

| Threshold for centroid height | Efficiency | Reliability |
|---|---|---|
| **0.3 meters** | 51.1 % | 99.2 % |
| **0.4 meters** | 80.0 % | 97.3 % |
| **0.5 meters** | 81.3 % | 89.3 % |

**Table 3. 1 3D vision alarm efficiency and reliability.**

### *3.3.2 Accelerometer analysis*

Analyzing the output of each of the accelerometer axes over more than 20 experimental acquisition sessions, containing about 10 fall events each, an algorithm has been developed. An example of the waveform output from the accelerometer is reported in Figure 3. 5. It is possible to note that a fall event is characterized by an acceleration peak, followed by some relatively constant values [31], and again followed in the experimental sessions by a peak due to the rise of the actor. The output data stream of each of the axes is analyzed, and an alarm is generated whenever at least one of the three axes detects a fall.

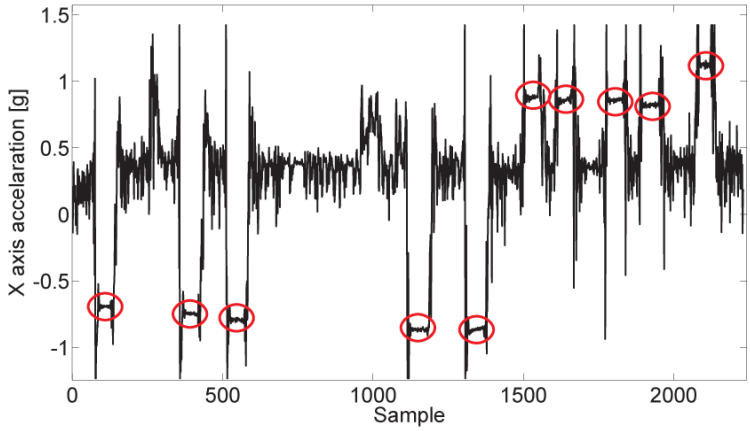


**Figure 3. 5 X-axis acceleration data.**

The output bit-stream of each of the axes of the accelerometer is computed separately. A digital block compares the absolute value of the distances between every consecutive four samples to a threshold. When the sum is higher than the threshold, it means that the person has fallen. If the threshold is set low, some events, such as sitting down, can be confused with a fall event, while when it is set high some fall events are not detected at all. Since this algorithm is supposed to work together with additional sensors, and being practically impossible to detect all fall events with zero error rate, the above reported strategy has been improved. Three different values of the threshold have been used: TH_L$_{ow}$, TH_M$_{edium}$, and TH_H$_{igh}$. This method leads to three different alarm signals, each one described by the efficiency and reliability reported in Table 3. 2 that will be considered in a different way by the request-for-help system gateway. The alarm generated by the circuit with TH_L$_{ow}$ detects almost all possible events but generates also a considerable number of false alarms. By contrast, using TH_H$_{igh}$, false alarms are very rare, but some fall events remain undetected. The TH_M$_{edium}$ specification constitutes a reasonable trade-off. Again, in the future, post-processing of the accelerometer data together with the other sensors will permit to detect the maximum number of fall events, while minimizing the number of false alarms.

| **Threshold parameter** | **Efficiency** | **Reliability** |
|---|---|---|
| **Low (TH_L)** | 98.0 % | 56.0 % |
| **Medium (TH_M)** | 88.4 % | 79.3 % |
| **High (TH_H)** | 50.1 % | 96.2 % |

**Table 3. 2 Accelerometer alarm efficiency and reliability.**

### 3.3.3 Acustic signal analysis

For acoustic scene analysis, we have developed a statistical approach based on hidden Markov models (HMMs). These HMMs are analogous to whole-word speech models, with a separate model used for each acoustic event class of interest. The HMMs have a left-to-right topology consisting of 50 states to impose certain length constraints to the acoustic events. HMM training commences with a flat start that employs the Viterbi algorithm, using 13-dimensional Perceptual Linear Prediction (PLP) features as the front-end. Following training, recognition of the acoustic events employs an HMM network, similar in fashion to speech recognition decoding [32]. An acoustic event is considered to be correctly detected, when its temporal center lies within the reference timestamps or vice versa. Table 3. 3 depicts the system performance under different decoding parameters, where the acoustic weight specifies how much the acoustic scores contribute to the final score.

| Acoustic weight | Efficiency | Reliability |
|---|---|---|
| **0.005** | 59.6% | 59.1% |
| **0.025** | 80.9% | 42.2% |
| **0.25** | 83.0% | 35.2% |

**Table 3. 3 Audio alarm efficiency and reliability.**

It turns out that the fall acoustic class gets mostly confused with background and door slamming noises. There are lots of false alarms that contribute to the low reliability depicted in Table 3. 3. We plan to further improve performance, by using linear discriminant analysis (LDA) to differentiate falls from other sounds. In addition, we plan to experiment with the maximum-a-posteriori (MAP) approach, which may be more suitable than maximum likelihood (ML) for HMM training for the particular problem at hand.

## 3.4 DEVELOPED SYSTEM ARCHITECTURE

The developed system is composed by commercial integrated devices: in particular, as can been seen in Figure 3. 6, by a MEMS accelerometer with digital output, by a FPGA and by a ZigBee wireless transceiver module.

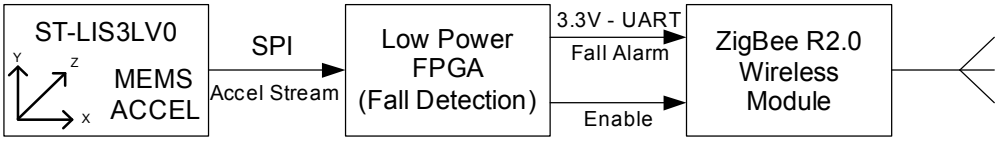


**Figure 3. 6 Block diagram of the developed wearable wireless accelerometer.**

The core of this system is the FPGA that controls the accelerometer, reads-out its digital output and delivers the necessary information to the ZigBee radio module, in order to have it transmitted to the gateway. Two operating modes are available for the device: in the first one, more useful during test campaign, the FPGA sends all the raw data acquired from the accelerometer to the ZigBee transmitter, and, of course, eventual alarms. By contrast, during the normal operative condition, the transmitted data are limited to the eventual alarms and to a signal useful to determine if the system is working and, of course, if the accelerometer has been worn. In both operating modes the control of the MEMS accelerometer is comprehensive of an initial setting of the control registers, that allows the choice of the most suitable characteristics for this particular application: among them, for example, the device full-scale, the resolution and the read-out rate. Once the setting phase is performed, the FPGA keeps querying the accelerometer, switching among the three axes. The accelerometer replies to every request with one word, containing the instantaneous acceleration experienced. This procedure is done continuously at the selected rate, which has been set by default at 10 Hz for overall acceleration query. In normal operating mode, the acceleration information, when its value crosses the wake-up threshold defined within the algorithm, is saved into suitable registers for 32 cycles, thus acquiring the amount of information necessary to the algorithm that has been developed in order to properly reveal falls.

## 3.5 HARDWARE DETAILS

The employed integrated accelerometer is shown in Figure 3. 7, mounted on a custom board for preliminary test. This particular 3-axis MEMS device has been chosen also because of the availability of digital SPI interface, that allows a simple communication with the FPGA without requiring an external A/D converter, and the good flexibility obtained through the programming of some essential parameters. The most important information regarding the accelerometer is summarized in the data sheet reported in Table 3. 4.

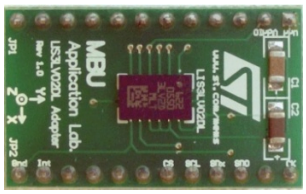


**Figure 3. 7 Employed MEMS accelerometer mounted on its test board.**

| | |
|---|---|
| **Power supply** | 2.5 V – 3.3 V |
| **Sensor I/O interface** | IIC/SPI |
| **Acceleretion bandwith** | up to 640 Hz |
| **Internal A/D converter resolution** | Up to 16 bits |
| **Number of axes and data format** | 3 axes (6 Bytes) |
| **Availability ranges** | ±2g; ±6g |
| **Sesnsitivity** | 0.1 mg |

**Table 3. 4 Accelerometer main specifications.**

As mentioned, since the developed device needs to be worn, it has to be wireless interfaced to the gateway and, of course, battery-operated. The ZigBee based transceiver, (a couple of devices is shown in Figure 3. 8), has been chosen because of its low cost and, even more important, its low power consumption, in order to guarantee a reasonable battery autonomy. More in detail the Zigbee is a wireless mesh networking standard. This kind of architecture can be exploited making the accelerometer based module interact with other sensors and understand if the person in the house has fallen, eventually sending an alarm through the gateway. Few details from the

transceiver data sheet have been summarized in Table 3. 5. On the basis of these specifications, Xbee family modules are suitable for in-house wireless communication with the gateway. For battery autonomy reasons a low power transmitter module (XBee) is preferred, but, when the house conformation requires it, also a higher transmitter power module is available (XBee PRO).


**Figure 3. 8 Couple of Xbee family tranceivers (ZigBee protocol).**

| **Specification** | **Xbee** | **Xbee Pro** |
|---|---|---|
| **Indoor/Urban Range** | Up to 30 m | Up to 90 m |
| **Transmit Power Output** | 1 mW | 18 mW |
| **RF Data Rate** | 250000 bps | 250000 bps |
| **Serial Interface Data Rate** | 1.2 – 250 kbps | 1.2 – 250 kbps |
| **Supply Voltage** | 2.8 - 3.4 V | 2.8 - 3.4 V |
| **Transmit Current (peak)** | 45mA (@ 3.3 V) | 250mA (@3.3 V) |
| **Receive Current** | 50mA (@ 3.3 V) | 55mA (@ 3.3 V) |
| **Power-down Current** | < 10 µA | < 10 µA |

**Table 3. 5 Xbee family module data sheet summary.**

The FPGA used for this project is a Spartan 3, mounted on a suitable test board, that allows several features useful for the purposes of the project. The test board is produced by Opal-Kelly and is shown in Figure 3. 9. In particular it

contains several PLL circuits, which allow the synthesis of different clocks. In fact, at least two clocks are necessary: one for the master circuit of the SPI to read-out the accelerometer and the other one to transmit processed data at the desired speed for the UART output interface, which interconnects the FPGA with the Xbee transceiver. Also a PROM is necessary in order to allow an automatic boot when the FPGA is powered up, avoiding to download every time the programming code by a computer through the USB connection.

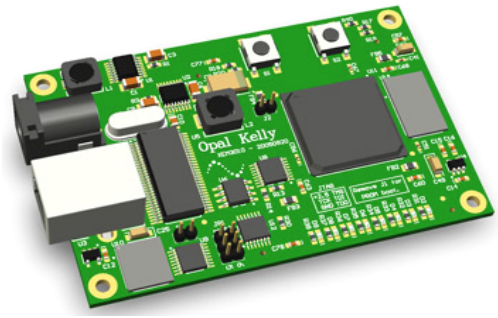


**Figure 3. 9 FPGA test board programmable via USB cable.**

## 3.6 ALGORITHMS

The FPGA runs in parallel six different routines for fall detection: two for each axis. The first routine measures the stress in terms of acceleration, while the second checks the acceleration shape. The MEMS device is also able to provide information about how gravity is distributed over the three axes (i.e. how the device is absolutely oriented). All dynamic acceleration components are referred to the gravity and an additional digital low-pass filter is used to retrieve such reference DC information. The main concept that is behind this algorithm is that every time a fall event occurs, the acceleration changes significantly and after that the person lays down so that the accelerometer orientation with respect to the gravity changes. Sometimes the fall event happens fast, while other times the event is slow. In order to check the quantity of acceleration stress within an over-threshold event, observing the acceleration data over a window of about 0.5 s seems to be the best compromise between effectiveness, complexity and low power consumption. The raw data coming from the accelerometer go to two different blocks. The first one processes the data d(k) using a low pass filter, to extract the gravity information, split into three axes according to the three-axial nature of the MEMS device. This information, $D_{STAND}(K)$, will be used by the subsequent block and compared to the raw data. In fact, the algorithm for the acceleration shape evaluation and the one for the acceleration stress evaluation are enabled only if the difference between the raw data and $D_{STAND}(K)$ is larger than a threshold, called TH1. The idea is to limit the data process in order to save power whenever it is possible and, therefore, to process data only when the person does some movements that could be considered a fall in terms of stress and timing. The acceleration stress evaluation then sums the unsigned distances of five consecutive samples and compares the obtained sum with a second threshold TH2. Finally, the acceleration shape evaluation algorithm, when the raw data d(k) exceeds $D_{STAND}(K)$ by more than TH1 waits for 16 samples, that corresponds to the typical transient part of a fall and then analyzes the following 16 samples. If at least 8 of 16 of the remaining values exceed $D_{STAND}(K)$ by more than a threshold, then the alarm for the axis is activated. This last comparison is done with three different thresholds giving alarms with different confidence level. In fact, using a large threshold, the number of false alarms decreases but only few events are detected. By contrast, using a low threshold, a larger number of events is detected, but the occurrences of false alarms increase. Being the accelerometer based system supposed to be used together with other systems based on different sensors, it is important to deliver not only the eventual fall

event but also how much the information should be trusted by the receiver. In order to generate the overall fall message, the three axis alarm information is merged. If at least two axis alarms are present within a three-axial 5-sample time window, the gateway will confirm a fall-event, fusing such information with other sensor data, which are actually validated, if present, by the accelerometer.

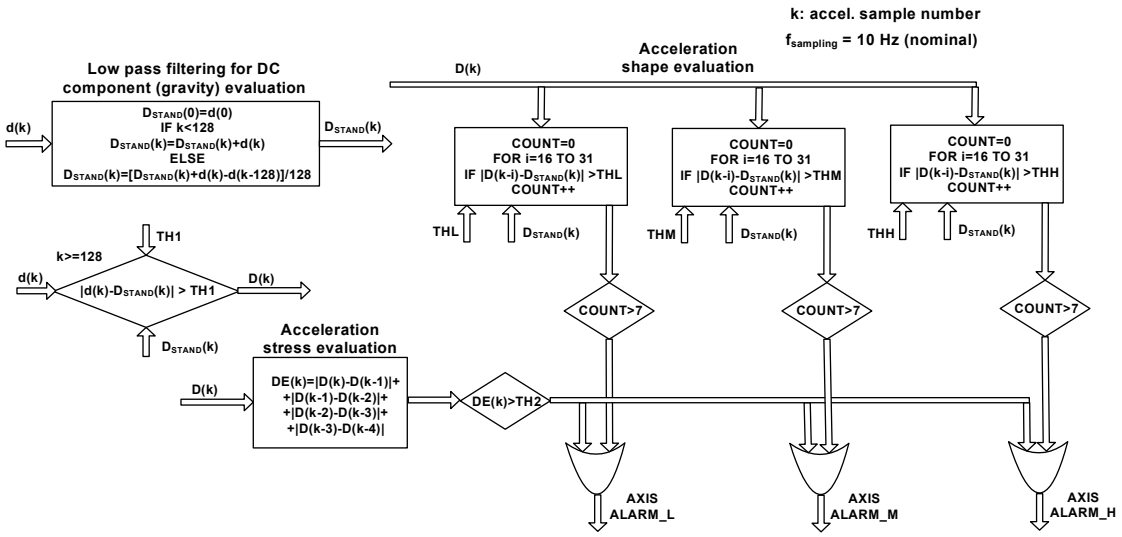


**Figure 3. 10 Flow chart description of the developed fall-detection algorithm (for one axis).**

## 3.7 MEASUREMENTS

The measurements have been done setting the MEMS device to the full-scale range of ±2 g, leading to an absolute sensitivity in terms of acceleration exhibited by the wireless module of 0.1mg considering 16-bit resolution. The average current consumption at 3.3V supply is of the order of 200μA when waiting for an acceleration event, about 1.5mA while processing the event (considering 10 sample/s per axis) and 35mA when transmitting a fall-flag or in streaming mode. Since the algorithm has been developed based on the data acquired, the data collection really played a fundamental role. Such data collection has been carried out by measuring the acceleration during various activities, like walking, bending, sitting, standing by 15 different human actors. It has been crucial to use several people to collect the data, in order to define an algorithm as general as possible. Moreover, in the performed recording sessions, the kind of fall has been varied several times for each person (falling forward, backward and sideward). To evaluate the performance of the algorithms while being developed and optimized, two parameters have been exploited: efficiency and reliability. The efficiency has been defined as the number of false alarms over the total amount of detected events and the reliability as the number of false alarms over the total amount of really happened events. By exploiting the above mentioned routines different thresholds have been evaluated using data from several sessions for training. After that, the performance of the algorithm has been evaluated on the remaining collected data and the results are shown in **Table 3. 6** [33].

| **Threshold** | *Efficiency* | *Reliability* |
|---|---|---|
| **Low (THL)** | 98 % | 61 % |
| **Medium (THM)** | 85 % | 80 % |
| **High (THH)** | 55 % | 97 % |

**Table 3. 6 Wearable accelerometer performance.**

An example of a plot of the acceleration along one axis (Y) has wearable accelerometer performance been reported in Figure 3. 11. It is possible to verify that every fall origins a spike in the acceleration that is followed by some oscillations and then the value remains stable at a sensibly different value from the starting one. In Figure 3. 11 we also indicated the action that the actor was

performing when the acceleration data was recorded and we enlightened the portion of time during which the data are evaluated by the algorithm.

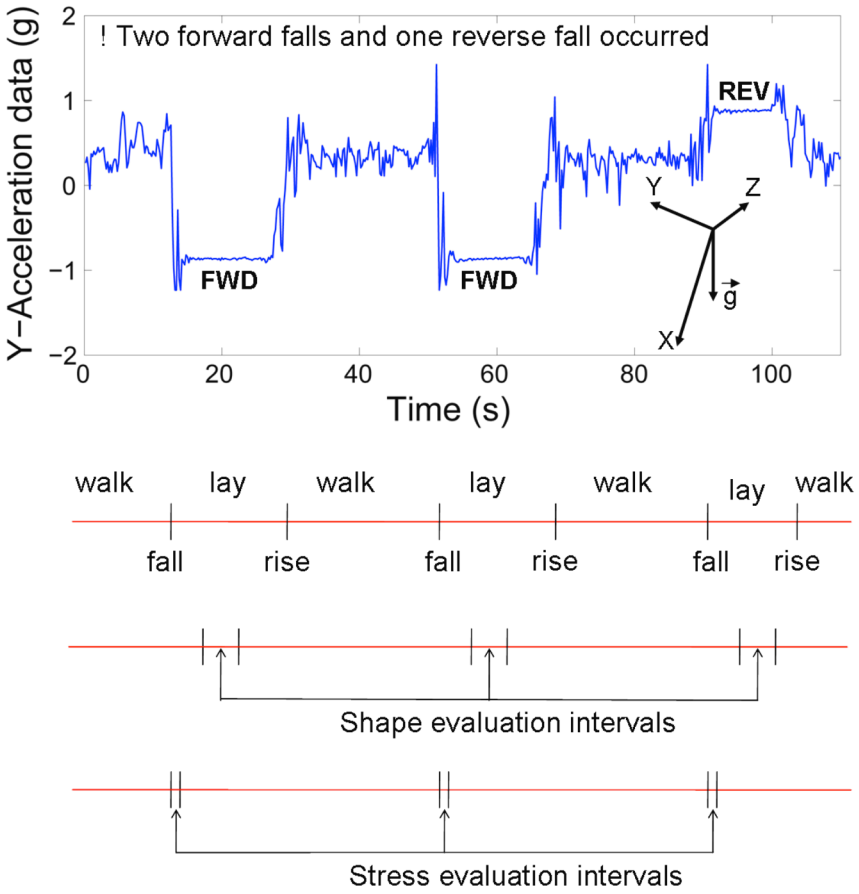


**Figure 3. 11 Acceleration data stream session measured along Y-axis with wireless device worn on the belt. The Y-axis is orthogonal to the belt.**

The FPGA runs the algorithms and sends the results to the ZigBee transmitter implementing a UART protocol. During the test of the device the data regarding the acceleration are transmitted in loop for each axis as ASCII strings as follows: the name of the axis (“X”, “Y”, or “Z”) followed by an “=” character and by 4 hexadecimal characters that represent its value expressed in two’s complement and by a comma terminator. Eventual axis alarms are transmitted as soon as they are revealed by the word “ALARM” followed by the level of confidence of the information, that could be a “H”, “M” or “L”. During the normal operation mode the FPGA sends every 5 minutes an “OK” message to shows that the wearable accelerometer is worn and working fine. The timestamps related to data and axis alarm flags are added by the gateway, which is in

charge of data fusion. The gateway (which actually is a compact or embedded PC) is connected to another ZigBee transceiver through its serial port.

# *Conclusions*

Ambient Assisted Living context is certainly an application area with a strong need of sensors as well as of actuators.
Many of the targets may be quite easily fulfilled thanks to the exploitation of the state-of-the art and off-the-shelf technology.
A microsystems based solution is almost mandatory in wearable devices, like non-invasive medical monitoring or accelerometer based people fall detectors.
The MEMS market is partially driven by this kind of applications, in which reliability, size, power consumption and cost are main carriers.
For the Ambient Assisted Living context, and in particular for safety applications, I have designed the following blocks:

- An high precision and low noise Read-Out Circuit for Capacitive Sensors.
- A low power and high precision LDO.
- Algorithms to detect falls in domestic environment.

A wireless system for fall detection, based on an accelerometer controlled by an FPGA has been presented. The algorithm, implemented on the FPGA and developed on the basis of a data-collection realized with several actors performing different kind of falls, has been implemented, tested and evaluated in terms of efficiency and reliability. In future work, the device will be tested again with new actors and the data will be used together with the data coming from other sensors to increase the overall efficiency and reliability.

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