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XXII CICLO

LOW-POWER CMOS TRANSCEIVER DESIGN FOR ZIGBEE APPLICATIONS

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Contents

Introduction

The cost and the power-hunger of mobile handsets have influenced the evolution of wireless networks architectures and with it their diffusion. In the first cellular systems (TACS, AMPS [1]) the use of large cells allowed to cover wide areas (rural and metropolitan districts) with a minimum number of base-stations, sacrificing the amount of coexisting clients in favor of a less-expensive infrastructure. In particular each cell was formed by a central base-station which provided the connectivity between all the mobile terminals (star-network architecture). At the beginning of the 90s, new research in the field of wireless communications, produced low-cost mobile terminals, rising the number of potential users. For this reason the cellular infrastructure was redesigned increasing the cell density around metropolitan areas, introducing the GSM [2] and successively the UMTS [3] systems. The result of this evolution was a much more powerful and versatile system. Nevertheless the star-mesh was preserved as the base of a system formed by low-cost mobile handsets and expensive base-stations able to manage a global communication network. The desire to achieve an additional drop of cost in wireless communication technology, suggested the idea to realize wireless-local or even personal area-networks (WLAN or WPAN) to share the data among a small group of users. In this case the easier management of the clients, has allowed to discard the star-mesh in favor of a more flexible peer-to-peer architecture. Within this evolving scenario, the ZigBee [4] and the other wireless sensor networks (WSN) standards represent an additional step towards an even more flexible system able to reshape itself dynamically. Due to their nature, these systems do not require any base-station, since they are formed by autonomous short-range wireless nodes, which monitor and control the environment defining the working area by their spatial distribution. Since the high density of units makes the system more flexible and relaxes the sensitivity of the single receiver, in ZigBee networks performance is exchanged with the possibility of having long-lasting and cheap devices [5]–[12]. Unfortunately, high efficiency and low-cost trade-off with each other. As an example the use of resonant loads minimizes power consumption, while an inductor-free approach saves die area,

resulting in a cheaper device. Within this scenario, a ZigBee transceiver based on the LMV cell [13] was designed.

In ***Chapter 1*** the IEEE 802.15.4 (ZigBee) standard main features are reported in terms of channel, bandwidth and modulation. This description is followed by an overview of the techniques used at the state of the art in order to satisfy the requirements of power and area saving in wireless sensor networks (WSN) transceivers.

Chapter 2 deals with the analysis of the LMV cell [13], which performs all the RF front–end functionalities in a single circuit, stacking a low–noise–amplifier (LNA) and a self–oscillating–mixer (SOM) [14] [15]. After optimizing its conversion gain, this cell is used to build a single coil quadrature front–end receiver, where the potential negative effects of the LC tank sharing are analyzed, in order to reduce them.

In the first part of ***Chapter 3*** the noise and linearity specs to design a ZigBee compliant receiver are derived from the standard definition document [4], while in the second part the connection between the LNA and the SOM is discussed, leading to two different quadrature generation and input matching solutions. The resulting receiver architectures are described together with the base–band design details. Finally, a complete set of experimental measurements carried out on two $90nm$ integrated receivers prototypes are reported and some conclusions are drawn.

Chapter 4 deals with the transmitter design. After a brief introduction to justify the choice of an all–digital frequency–locked–loop to lock the oscillator in RX mode and to modulate the signal in TX mode, the required phase noise profile is derived. From these specs, the TDC and DCO resolution can be obtained. The TDC and the DCO design details, together with the digital loop filter ones, are given. Finally, the last part of the chapter deals with the power–amplifier design.

Chapter 1

ZigBee standard and transceivers state of the art

In these last years the interest on very low–power and low–cost CMOS transceivers has increased thanks to new low–data–rate applications in commercial, game, personal health–care, automation and industry fields. Since the target is to obtain a dense and inexpensive low data–rate *wireless* personal area network (LR–WPAN), these applications require devices working for months or even years without changing the battery.
In this chapter, the standard which regulates LR–WPANs (the IEEE 802.15.4 [4]) is introduced, describing its main features. In particular the focus is on the frequency bands, on the modulation and on the advantages deriving from the use of direct–sequence spread–spectrum (DSSS) signals. After this introduction, an overview on the state of the art of low–power and low–cost transceivers for LR–WPANs is proposed, with a particular attention to area and power saving techniques used in several prototypes.

1.1 IEEE 802.15.4 general features

Frequency bands and data–rate

The standard IEEE 802.15.4, works in three different frequency bands: at $868MHz$ in Europe, at $915MHz$ in America and at $2.45GHz$ globally. It establishes different modulations and spreading formats, which are summarized in table 1.1.

27 channels are available: 16 in the higher frequency band at $2.45GHz$, 10 in the intermediate $915MHz$ band, while only one channel is available in the $868MHz$ one. Since this work is tailored to the higher frequency band, hereafter only this band is considered. In the $2.45GHz$ band, each channel

		Spreading param.		Data param.		
PHY (MHz)	**Freq. Band (MHz)**	**Chip rate (kch/s)**	**Mod.**	**Bit rate (kbit/s)**	**Symbol rate (ksym/s)**	**Symbol**
868/915	868-868.6	300	BPSK	20	20	Binary
	902-928	600	BPSK	40	40	Binary
2450	2400-2483.5	2000	OQPSK	250	62.5	16-ari Orth.

Table 1.1: Frequency bands and data–rate

has a bandwidth of $2MHz$, with a $5MHz$ channel spacing, as shown in figure 1.1.

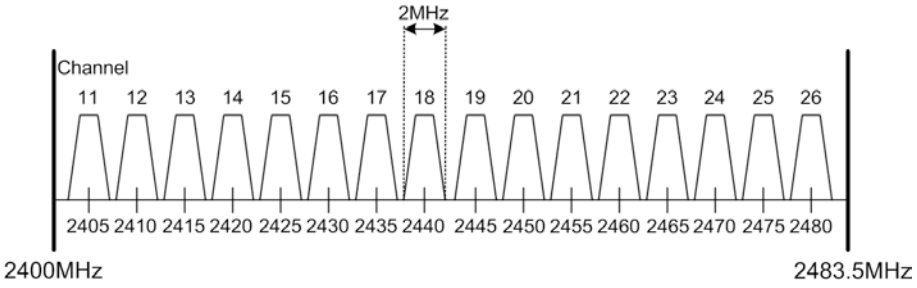

Figure 1.1: ZigBee channels at 2.45 GHz

The ratio between the channels distance and the bandwidth is quite high ($\Delta f/BW_{CH} = 2.5$). This, together with the adjacent and alternate channel rejection of $0dB$ and $30dB$ respectively, relaxes the channel selection requirement. Moreover, the needed image rejection (IR), is higher than the signal–to–noise–ratio ($SNR = 6dB$ and therefore $IR > 6dB$)) [7]. Since such a relaxed target is easy to achieve, a higher image rejection can be obtained with no high design complication, improving the receiver robustness [7].

Signals modulation

Referring to table 1.1 for the $2.45GHz$ band the standard establishes an O–QPSK modulation (*Offset Quadrature Phase Shift Keying)* with half–sine shaping. This modulation can be obtained using a circuit like the one in figure 1.2 [16].

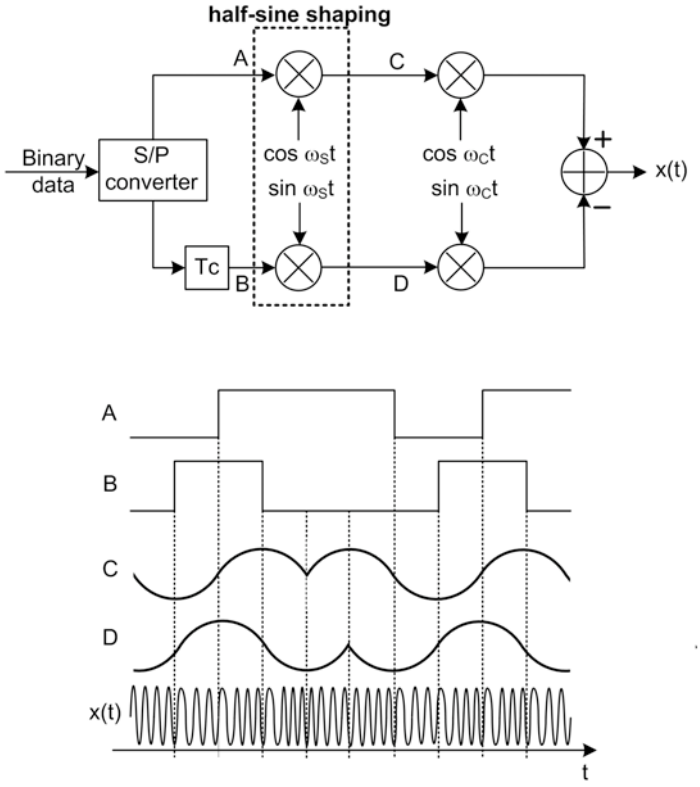

Figure 1.2: O–QPSK modulator with sine shaping

The I and Q data streams are offset in time by half the symbol period, avoiding simultaneous transitions in waveform in nodes A and B. This produces phase steps of only ±90 degrees, instead of the 180 degrees steps obtained without the T_C delay, eliminating concerns about undesired envelope variations which would require a linear amplifier to avoid spectral regrowth [16]. Therefore power amplification can be performed by means of efficient power–amplifiers (PAs), which reduce the power consumption at the cost of a lower linearity. Nevertheless this does not affect the proper working of the system when no information is contained in the amplitude of the modulated signal. Moreover, since the half–sine shaping reduces the occupied bandwidth, the modulated signal has also a good spectral efficiency.

Processing gain

The IEEE 802.15.4 standard uses *Direct Sequence Spread Spectrum* (DSSS) signals, which introduce a processing gain. Before transmission, the signal of interest is multiplied by the chip sequence, and its bandwidth spreads, becoming equal to the chip–rate, as shown in figure 1.3.a. This results in a reduction of the power spectral density, since the total power is distributed over a wider bandwidth. When this signal is received, it is decoded through the same code used in transmission, and its bandwidth despreads to its initial value (figure 1.3.b). Thus, the power spectral density of the signal increases if compared with noise and interferers, introducing a processing gain (G_P in figure 1.3.b).

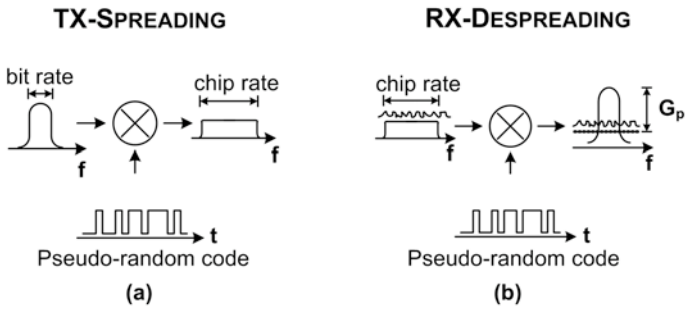

Figure 1.3: TX spreading and RX despreading

This gain depends on the chip–rate and on the bit–rate as follows:

$$G_P|_{dB} = 10Log_{10}\frac{ChipRate}{BitRate} \tag{1.1}$$

The processing gain, which is about $9dB$ for the IEEE 802.15.4 standard, represents an improvement on the *Signal to Noise Ratio* in RX mode. In fact the standard requires a minimum SNR of $6dB$, which corresponds to a packet error rate (PER) lower than 10^{-2}. To increase the design robustness some margin is taken and the chosen target value for the SNR is $10dB$. Thanks to the processing gain, the effective required SNR becomes $1dB$.

1.2 Low–power transceivers state of the art

The IEEE 802.15.4 features, together with the RX-TX specs which will be derived in chapter 2 and 4, show that the standard does not impose severe constraints, which can be satisfied by designing simple power and area–saving

circuits. Since in this last years some interesting techniques to reduce circuit complexity have been proposed, the state of the art of LR–WPAN transceivers is summarized in this chapter, where beginning from the architectural choice, an overview on the proposed power and area minimization technique is reported.

1.2.1 Transceiver architecture choice

Receiver architecture

A LR–WPAN receiver has to successfully demodulate a desired signal in presence of interferers and noise, while minimizing power consumption and costs. Since cost reduction requires to minimize the number of expensive external components [7], the robust and performing heterodyne receiver architecture, which down–converts the RF received signal to a lower RF frequency [16], becomes inadequate. In fact it requires external high–Q band–pass filters for the image rejection and the channel selection, which increase the cost as well as the transceiver size.
These external filters can be eliminated using a two–steps architecture [10], where two high frequency local oscillator signals (LOs) translate the input spectrum to an intermediate frequency and subsequently to DC. Nevertheless this solution is unsuitable for very low–power applications, since it requires two radio–frequency synthesizers in order to generate the local oscillator signals.
The only candidates for low–power and low–cost applications are therefore the direct–conversion and the low–IF architectures. Both of them do not require discrete external components and use only one frequency synthesizer. Their working principle is exactly the same, since the input signal is down–converted by a mixer driven by a radio–frequency local–oscillator. They only differ for the frequency of down–conversion, which is DC for the direct conversion scheme, while it is a low intermediate frequency for the low–IF architecture, as the name itself suggests. The use of the direct conversion oversimplifies the design of the base–band, since to perform channel selection a low–pass filter with the lowest possible cut–off frequency is needed. Nevertheless this solution suffers from some drawback: it is sensitive to dynamic DC offsets (including the one introduced by the second order non linearity of the mixer), and to the flicker noise of CMOS transistors, which covers nearly the entire signal band in narrow–band receivers [16]. These drawbacks can be overcome using current–mode passive mixers with very good noise and linearity performances

([6], [8]), or simply shifting the signal band to a low–IF [16]. Tacking this last choice, image rejection (IR) has to be implemented. In fact when complex–valued mixing process are involved, the non–perfect balance of the in–phase and quadrature signal degrades the receiver image rejection. Nevertheless, since the required IR for proper demodulation is quite relaxed ($6dB$), this topology can be successfully used in the design of an IEEE 802.15.4 compliant receiver. Moreover, using a channel selection complex filter, with an asymmetrical transfer function respect to the frequency origin (chapter 3), the problem of image rejection can be overcome, increasing the receiver robustness [7].
From these considerations, the low–IF architecture with complex channel selection filter is chosen to design the receiver section presented in this work.

Transmitter architecture

A transmitter has to perform modulation, up–conversion and power amplification, with the first two combined in some cases. Even if the panorama of transmitter architectures is quite wide, at the state of the art the preferred ones for LR–WPANs applications are the direct conversion and the voltage–controlled–oscillator (VCO) direct modulation schemes ([5], [7], [8], [11]).
The direct conversion architecture performs the I/Q modulation and up–conversion through up–conversion mixers, whose outputs can be combined by adding currents and then transmitted after power amplification [5]. In this case, since the ZigBee standard is time–division the frequency synthesizer, which sets the LO frequency, and the mixer can be used both in TX and RX modes.
A more aggressive approach used to reduce power consumption is the direct modulation ([7], [8]), where frequency modulation is performed within the frequency synthesizer loop. After modulation, the LO signal is amplified by a non–linear PA, with no mixing and low–pass filtering required. The direct VCO modulation can be realized open–loop or closed–loop. The open loop technique requires to close the loop to set the desired channel frequency, and after that to open it, applying the modulating signal to the VCO control terminal. Even if this solution is very simple, its robustness is reduced since any leakage current from the VCO varactor or any undesired perturbation can cause a drift of the carrier center frequency. This problem can be solved by choosing a closed–loop solution, where the VCO always works in a closed loop and the frequency modulation is obtained by changing the division ratio in the loop itself. Even if this solution potentially suffers from bandwidth limita-

tion, it is suitable for LR–WPANs applications, which does not require wide bands in order to satisfy the data–rate requirements. Also in this case the cost advantages deriving from functional blocks sharing can be exploited, since a single frequency synthesizer can be used both in TX and in RX mode.
In this work, the direct VCO modulation scheme has been preferred to the direct conversion one. The choice is strictly related to the major flexibility of the structure, which is suitable both for an analog and a digital implementation, as it will be discussed in chapter 4.
In figure 1.4 a block diagram of the complete transceiver described in this thesis is reported.

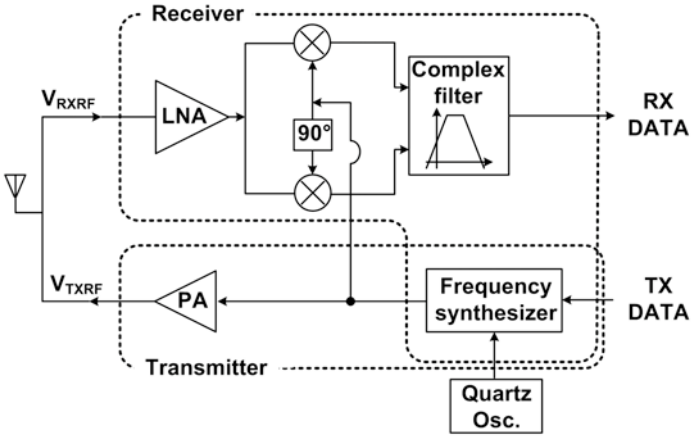

Figure 1.4: Transceiver block diagram starting point

The scheme shows a conventional quadrature low–IF receiver and a direct VCO modulation transmitter, which is the starting point for the transceiver design. The design details and some change in the architecture will be proposed in the following chapters.

1.2.2 State of the art of low–power design strategies

A proper architectural choice is crucial to obtain good levels of performance, costs and power dissipation. Nevertheless it is only the first step towards the design optimization, which can be reached only by proper choices down to transistor level. In particular, much attention in the optimization process is paid to the radio–frequency blocks, which are the most promising for power and area reduction, since they are more expensive and power–hungry than the low–frequency ones. In this section several design approaches are analyzed, in order to find the most effective area and power minimizing strategies proposed

at the state of the art.

Song low–power receiver design

The solution proposed by Song et al. [12] aims to minimize power consumption in a modified direct conversion receiver. The most power–hungry block in a receiver front–end, is the frequency synthesizer, and therefore reducing its power consumption introduces a big saving on the whole receiver power dissipation. Since the higher the frequency, the higher the power consumption, a possibility to obtain power–saving is to reduce the working frequency. This consideration is at the basis of the proposed receiver, whose scheme is reported in figure 1.5 [12].

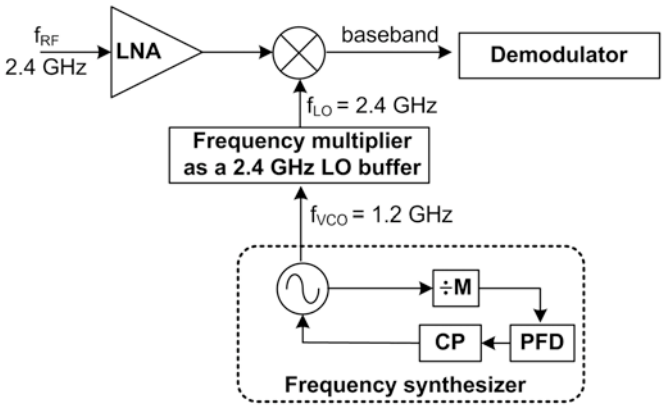

Figure 1.5: RX architecture proposed by Song

In a conventional direct conversion receiver, the LO and the RF input signal frequencies are equal, in order to directly translate the input to DC. In the proposed modified solution, the LO frequency is halved respect to RF, and then the LO signal is processed by a frequency multiplier to generate the desired RF frequency for direct conversion. Thus, both the VCO and the frequency divider work at $1.2GHz$ instead of $2.4GHz$, resulting in power reduction. This is obtained at the cost of a phase noise worsening, which is anyway maintained in an acceptable range for LR–WPANs applications.
The VCO is optimized, maximizing its output swing for a given bias current. This is obtained considering that the LC oscillator amplitude depends on the LC tank equivalent resistance (R_{tank}) and on the first harmonic coefficient (A_1) of the periodic current flowing in the tank itself ($V_{osc} = A_1 R_{tank}$). Since the R_{tank} value is limited by the LC tank quality factor, the LO amplitude

can be maximized by increasing the Fourier coefficient of the first harmonic. It can be shown [12] that under the same average bias current, a narrower pulse current with a higher peak value produces a larger oscillation amplitude. Therefore the power optimization can be obtained by increasing the bias voltage at the gate of M_{VCOP} in figure 1.6. This reduces the conduction angle of the VCO switching pair at the cost of increasing non–linearities.

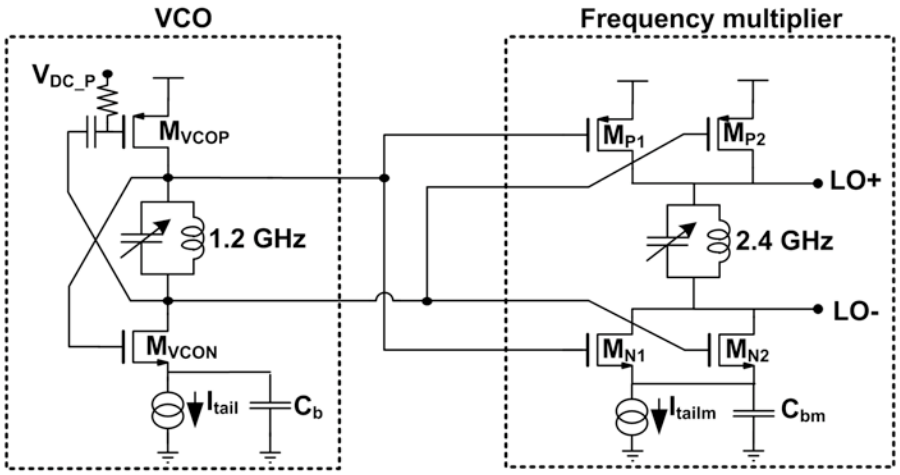

Figure 1.6: Song VCO and multiplier design details

Figure 1.6 shows also the frequency multiplier schematic, which is based on two differential current sharing pinch–off clippers. The differential LO signals are obtained through second harmonic generation. In particular the second harmonic output of the pMOS has inherently an opposite phase compared with that of the nMOS, regardless of the phase of the input signals [12]. The power consumption of this circuit is minimized exploiting the stacking of the pMOS and nMOS pinch–off clippers, which share the DC bias current. Moreover power minimization is obtained also thanks to the buffering effect of the frequency multiplier. In fact it prevents injection–locking phenomena [16], making unnecessary the introduction of additional power–hungry buffers.
In conclusion, Song reduces power consumption not only halving the frequency of operation of the most power–hungry RF building–blocks, but also minimizing the bias current through bias and devices sharing. Nevertheless the power optimization is obtained increasing costs, since this design requires two integrated coils only to obtain the desired LO frequency.

Cook low–power transceiver design

Since the power dissipation of a transceiver is strictly connected to its bias current (I_{BIAS}) and voltage supply (V_{DD}), power can be saved reducing both I_{BIAS} and V_{DD}. The approach proposed by Cook focuses mainly on the supply voltage minimization [8]. This choice requires to design a passive and differential front–end, in order to increase the available voltage swing and to have a good noise figure (NF) and linearity at minimum power. Figure 1.7 shows the block diagram of the proposed $400mV$ V_{DD} transceiver.

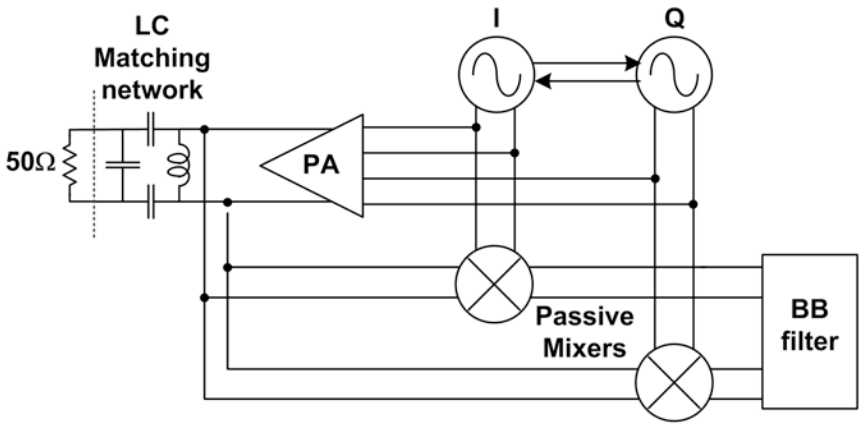

Figure 1.7: Cook Transceiver block diagram

The antenna matching network is an integrated LC structure, which is shared between the receiver and the transmitter, in order to reduce the number of inductors and therefore the silicon area. This network, which introduces a passive gain, replaces the traditional LNA, saving power consumption.
Quadrature is provided by a back–gate quadrature VCO (figure 1.8) [17], which reduces power consumption respect to the traditional cross–coupling quadrature generation technique.

Since the system is time division, the back–gate quadrature VCO can be shared between the receiver and the transmitter, reducing design efforts and area occupation. Moreover, since in transmit mode, the PA and mixer are driven directly from the high quality factor LC tank of the VCO without buffering, the whole differential VCO output swing is amplified, saving power and improving performances.
In conclusion, power–saving in this case is mainly due to the voltage supply minimization. Nevertheless other design choices help to reduce furthermore the power consumption, such as the LNA elimination in the receiver, the use

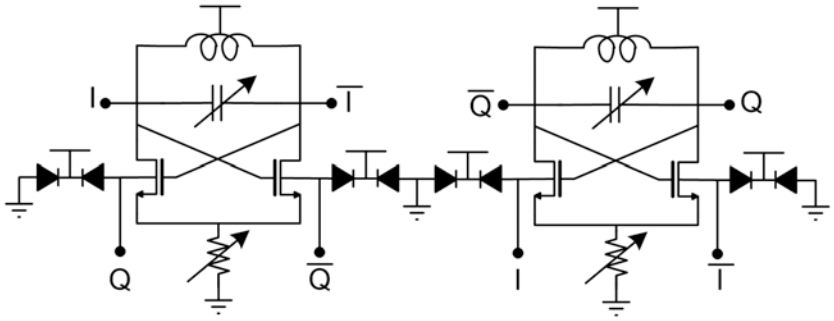

Figure 1.8: Quadrature VCO using back gate coupling

of the whole differential VCO output swing in TX mode and the choice of the quadrature generation technique. Cost minimization is obtained sharing the input matching network and the quadrature VCO between the receiver and the transmitter.

Kluge low–power transceiver design

Focusing on a low–IF receiver, direct VCO modulation transmitter, Kluge et al. proposed an original approach to low–power design (figure 1.9).

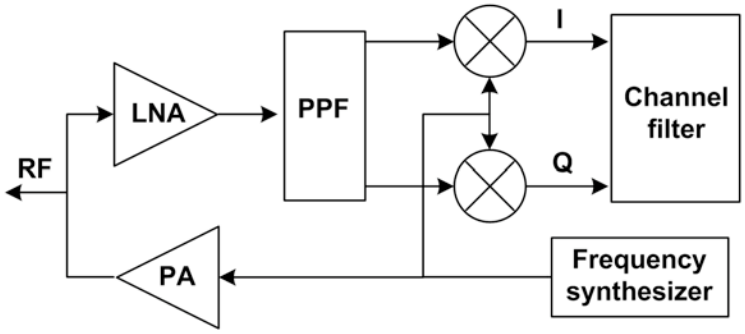

Figure 1.9: Kluge Transceiver block diagram

The proposed architecture uses a single oscillator signal, saving the power needed to generate and buffer the quadrature LO signal. Quadrature is generated in the RF signal path, where the low–noise amplified signal is split into I and Q components using a passive 2 stage poly–phase–filter (PPF). Even if quadrature generation in the RF path generally entails severe noise–power–gain trade–offs [16], it can be an acceptable solution in LR–WPANs applications, where the performances required to the transceiver are quite re-

laxed, and power and cost minimization are most severely constrained.
The down–conversion mixer can be implemented as a passive switching device, lowering not only the power consumption, but also the flicker noise respect to a Gilbert cell. Thus, the only power consuming element of the receiver front–end is the LNA, which has also to compensate losses introduced by the poly–phase–filter and mixer. Therefore the LNA gain has to be increased using two low–noise amplification stages, as shown in figure 1.10.

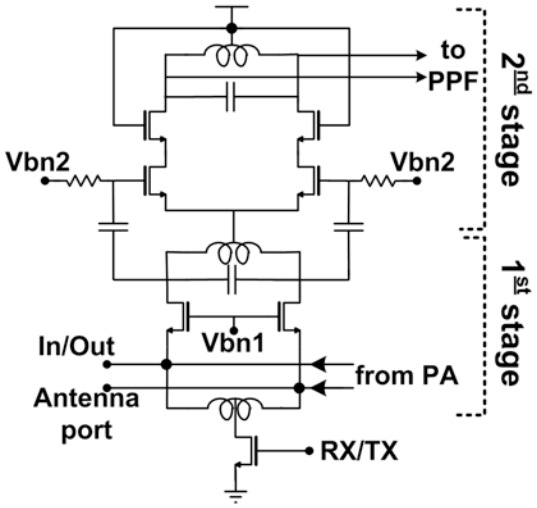

Figure 1.10: Kluge LNA simplified schematic

The proposed two–stages LNA is formed by two stacked elements, sharing the bias current.
For what concern the transmitter chain, the VCO frequency modulation is performed within the loop. This allows to power–amplify the modulated signal without any mixing and low–pass filtering needed, which helps to reduce power consumption. Moreover the constant envelope frequency modulation allows to maximize the PA efficiency, minimizing the dissipated power for a given transmitted one.
Therefore Kluge reaches power minimization using a single VCO and generating quadrature in the RF path. This choice requires a careful design of the LNA, where power consumption can be minimized exploiting the bias sharing. Also the choice of a power–efficient PA assures power–saving, while the area optimization is limited to a high level of integration obtained by a proper architectural choice. As it results form [7], the required silicon area is dominated by the presence of a high number of integrated inductors, which increases the

chip cost while assuring high power efficiency.

Liscidini low–power receiver design

Bias and device sharing is a widely used power–saving approach, which is exploited at its maximum level in the LMV cell [13]. The acronym stands for LNA–Mixer–VCO, meaning that this structure performs low–noise RF amplification, mixing and LO generation in a single circuit, resulting in a very low power and small area solution (figure 1.11).

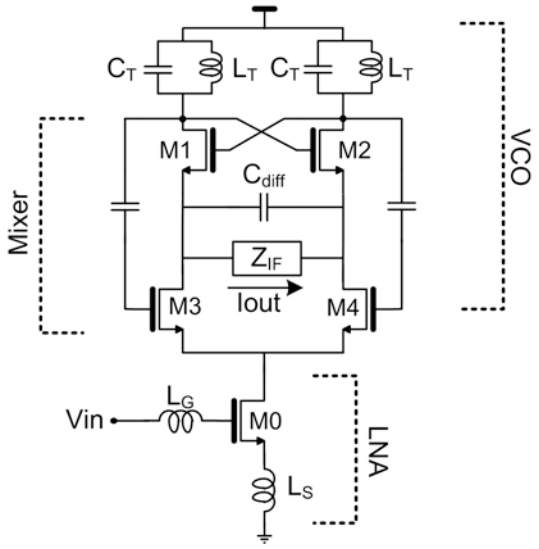

Figure 1.11: LMV cell schematic

This topology is built up stacking blocks and merging their functionalities. When blocks are in series between ground and V_{DD} they can be easily and independently optimized, but there is a limit on the stacking which depends on the voltage supply which is right along reduced with the technology scaling–down. On the contrary, merging functionalities does not suffer from the reduction of voltage supply, but it reduces the degrees of freedom in the circuit design. The LMV cell is built starting from these considerations, and it overcomes the described issues. In fact this cell does not require a high voltage supply, since the minimum needed V_{DD} is a threshold voltage plus three overdrives. Moreover, even if the merging of the building blocks prevents to optimize them individually, a certain degree of flexibility is preserved, and the LMV cell can be easily inserted in a conventional loop for quadrature LO generation.
This cell was not specifically built for LR–WPANs applications, and it was

used as the core of a GPS receiver prototype [13], where it aimed to minimize power–consumption maximally exploiting current reuse.

1.3 Conclusions

As it is shown at the beginning of this chapter, the IEEE 802.15.4 general features are compatible with the requirements of low–power and low–cost, since they are quite relaxed, and they can be satisfied by designing quite simple circuits.
Even if the power and area minimization require a careful choice of the transceiver architecture, they can be reached only combining this choice with proper design strategies. As shown in the state of the art overview, cost minimization requires to reduce the number of integrated coils and external components. This can be obtained e.g. sharing the matching network and the oscillator between the transmitter and the receiver. On the other hand the most promising solution to save power consumption seems to be bias and device sharing. In particular the LMV cell maximizes this saving, while maintaining a good flexibility, which can be exploited to optimize the design. This cell, which is chosen as the starting point for this work, is presented and optimized in chapter 2, and its optimized version is used as the core of the transceiver.

Chapter 2

Low–power quadrature RF front–end

Current reuse among different functional blocks is a favored technique to obtain vanishing power consumption in ultra–low–power applications. This technique is exploited also by the LMV cell [13] introduced in chapter 1, which is chosen as the starting point for the design of the ZigBee transceiver.

In this chapter, starting from a description of the LMV cell working principle, an improvement of the original structure is proposed. The improved LMV cell is then used to build a single resonator quadrature receiver front–end, where the amplitude and phase mismatches due to the LC tank sharing are studied and minimized.

2.1 The LMV cell

In order to describe the LMV cell working principle, the same path proposed in [13] is followed. The cell is built starting from a traditional LC tank oscillator, where the mixing functionality is intrinsically performed. Referring to figure 2.1, the switching pair M1–M2 up–converts to the oscillator frequency the DC bias current of M0, while it down–converts any RF component of the drain current of M0.

This down–converted signal cannot be read in this topology, because of the filtering effect of the high–Q resonant LC tank, which amplifies the up–converted signal at the LO frequency and filters–out all the other frequency components. The IF signal can be read at the output of the VCO only degrading the LC tank quality factor, and therefore the oscillator phase noise. To overcome this issue the bias generator M0 is split into two transistors (M0a and M0b in figure 2.2), allowing to read the down–converted signal at M1–M2 sources.

The oscillation is sustained by the capacitance C_{diff} which closes the loop

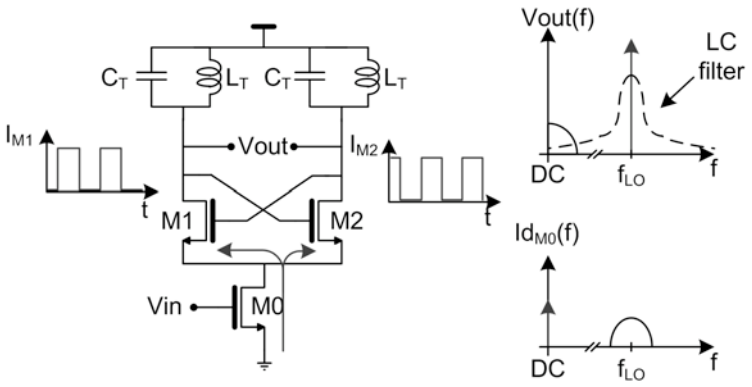

Figure 2.1: LC tank oscillator.

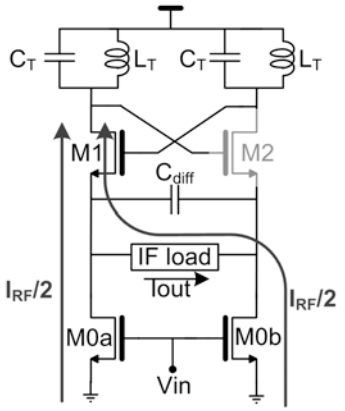

Figure 2.2: Bias splitting self–oscillating–mixer.

at RF, while showing high impedance at IF. Notice that at RF the structure is exactly a traditional LC tank oscillator, which preserves its tuning capability and which can be inserted in a traditional phase or frequency locked loop (FLL or PLL) architecture. Since C_{diff} degenerates the sources of M1 and M2 at RF, its value has to be chosen in order to obtain a sufficient loop gain (G_{LOOP}). G_{LOOP} depends on the LC tank equivalent resistance ($R_{tank} = \omega L_T Q_T$), and on the admittance seen from the M1 and M2 drains to ground (Y_d), which can be expressed as follows:

$$Y_d(s) = \frac{g_{m1,2}}{1 + \frac{g_{m1,2}}{sC_{diff}}} \tag{2.1}$$

Thus, to have $|Y_d R_{tank}| > 1$ [16] C_{diff} has to satisfy the following condition:

$$C_{diff} > \frac{2g_{m1,2}}{\sqrt{g_{m1,2}^2 L_T^2 Q_T^2 \omega^4 - 4\omega^2}} \tag{2.2}$$

Once the capacitance C_{diff} has been properly chosen, the down–converted signal can be read at the sources of M1 and M2 over an IF load. In the time domain, when M1 is on and M2 is off (see figure 2.2), the signal from M0a ($I_{RF}/2$) flows directly in M1, while the signal from M0b ($I_{RF}/2$) flows in M1 after passing through the IF load. Therefore only half of the total current flows into the IF load, leading to a maximum conversion gain equal to $1/\pi$ [13]. This loss can be eliminated adding a differential pair (M3–M4) between the current generator and the differential pair M1–M2, as shown in figure 2.3. In this topology all the M0 current flows into the IF load, with a maximum conversion gain of $2/\pi$. The radio frequency current is multiplied for a square–wave. This current flows through the IF load without having any effect on the oscillator, since the IF load degenerates M1 and M2 sources only at low–frequency.

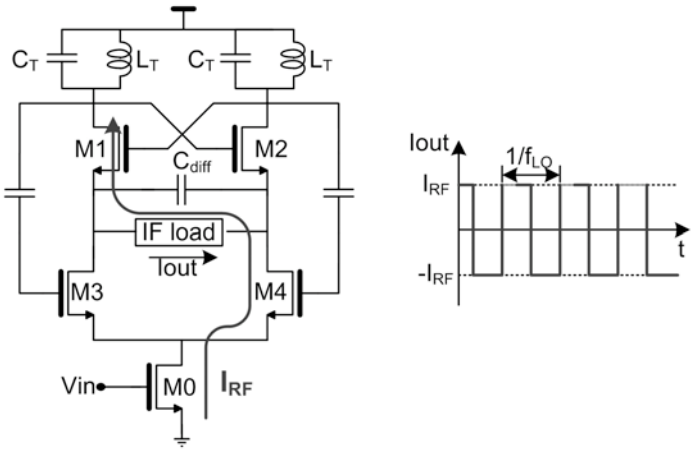

Figure 2.3: Double switching pair self–oscillating–mixer.

The cell in figure 2.3 performs the VCO and mixer functionalities. The LNA can be inserted without any additional active device, by exploiting transistor M0 at RF, i.e. transforming M0 into an inductive degenerated low noise amplifier, as shown in figure 2.4.

LNA, mixer and VCO are not simply stacked between the supply voltage and ground, but they also share some devices, which perfom different functionalities at RF and IF without conflicts between the two domains. In fact transistor M0 in figure 2.4 sets the VCO bias current at low–frequency, while

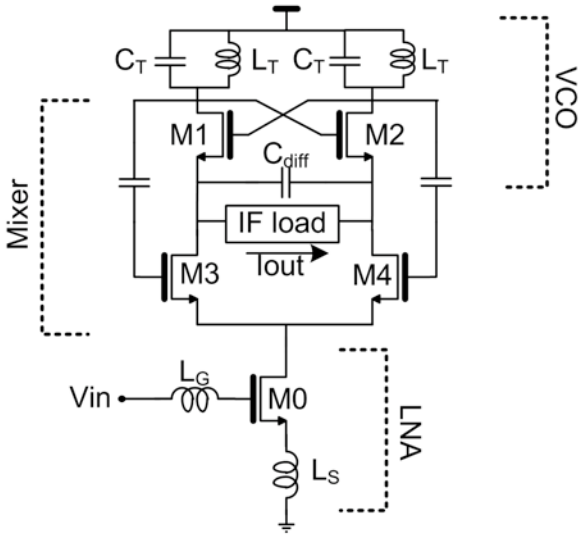

Figure 2.4: The LMV cell topology.

it acts as an LNA at radio–frequency. Moreover M1 and M2 perform the mixing task while contributing together with the capacitance C_{diff}, to the VCO operations at RF.
The number of transistor is minimized and the cell is compatible with low supply voltages. In fact, although three transistors are stacked, the minimum voltage supply required is equal to only one threshold plus three overdrive voltages. Therefore the LMV cell merges several apparently contrasting tasks, such as current reuse, device sharing without spur interaction issues, transistors count reduction, and compatibility with a low supply voltage. Moreover the LMV cell maintains some degree of flexibility, since it can use either a high impedance load (voltage mode LMV) or a virtual ground load (current mode LMV). While the use of a high impedance load produces a high voltage gain and therefore a negligible base–band noise contribution, using a virtual ground that shorts–out the sources of M1 and M2 also at low frequency,assures a more robust control on the conversion gain, as it will be shown in the following section.

2.2 Loss mechanisms in the LMV cell

The LMV cell efficiency is limited by loss mechanisms, which have different impact on the conversion gain depending on the IF load impedance. In this section these mechanisms are described and their effect on the conversion gain

is evaluated.

2.2.1 Losses due to an unwanted equivalent resistance

Even if the IF load is neglected, the LMV cell shows an finite impedance at the sources of M1 and M2 which limits its conversion gain. If the oscillator is current limited and hard switching is supposed, this resistance (R_x) depends on the quality factor of the LC tank [13]:

$$R_x = 4\omega_{LO} L_T Q_T \tag{2.3}$$

Since Q_T is typically in the range between 10 and 20, for a GHz application with a nH inductor, R_x is in the $k\Omega$ order. Thus, if the down–converted signal is read over a virtual ground, the effect of R_x can be neglected, while it has to be considered if the IF load impedance is comparable to R_x.

2.2.2 Losses due to parasitic capacitors

The parasitic capacitors connected between the IF nodes and ground are mainly due to the parasitics of transistors M1, M2, M3 and M4 and of the amplifier used to sense the IF nodes. These capacitors limit the conversion gain of both the voltage and current LMV solutions, even if their impact is considerably different in the two cases. The analytical study of losses in presence of capacitances at the output nodes is complicated by the time–variance of the structure. To simplify the analysis, it can be noticed that assuming the transistor M0 in figure 2.4 working as an ideal current source, the drain currents of the transistor pair M3–M4 can be expressed as follows:

$$\begin{aligned} I_{M3} &= \frac{I_{M0}}{2}(1 + sign(\cos(\omega_{LO} t))) \\ I_{M4} &= \frac{I_{M0}}{2}(1 - sign(\cos(\omega_{LO} t))) \end{aligned} \tag{2.4}$$

The currents flowing in M3 and M4 can be seen as the sum of two portions with the same peak amplitude equal to $I_{M0}/2$: a common mode one and a differential one multiplied by $sign(\cos(\omega_{LO} t))$. Therefore the double switching pair SOM can be transformed in the parallel of two bias splitting SOM as shown in figure 2.5, whose current sources inject a differential signal at $(\omega_{RF} - \omega_{LO})$ and a common mode one at ω_{RF}.

Based on this equivalent model, the losses due to the parasitic capacitances both at low frequency and at RF can be evaluated.

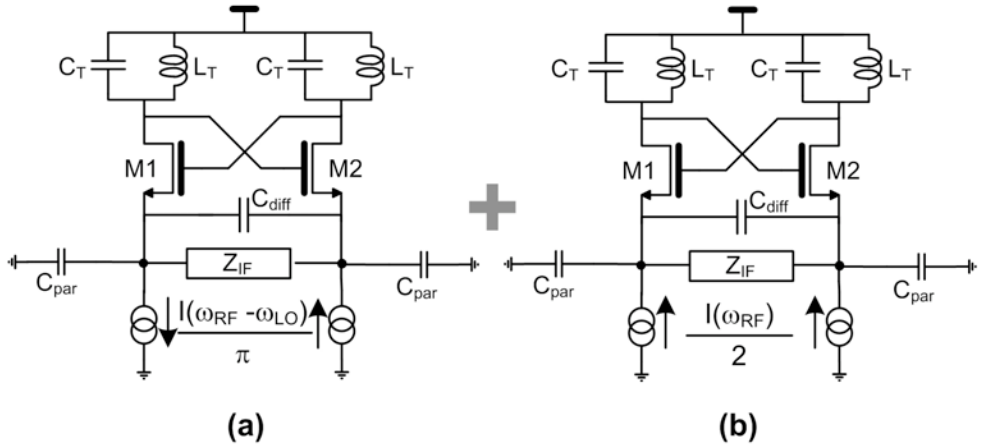

Figure 2.5: (a) Low frequency and (b) RF loss mechanisms.

Low–frequency losses

Considering the circuit in figure 2.5.a, the parasitic capacitors C_{par} at the output nodes are discharged by transistors M1 and M2. Since the charging/discharging frequency (ω_{RF}) is much higher than the frequency at which losses are evaluated (ω_{IF}), a switched capacitor approach can be used. Assuming the transistors acting like switches driven by a signal at ω_{LO}, M1 and M2 redistribute the C_{par} charge, producing an equivalent resistance in parallel with the IF load (R_{eq}). Since losses depend on the current partition between Z_{IF} and R_{eq}, they increase with the IF load impedance. If Z_{IF} is much lower then R_{eq} these losses becomes negligible, and the resulting conversion gain due to the differential low–frequency component is close to $1/\pi$.

Radio–frequency losses

When the common mode radio–frequency current is considered (figure 2.5.b), the parasitic capacitors C_{par} are in parallel with the current generator injecting the signal. Since at RF the sources of M1 and M2 are shorted by C_{diff}, to evaluate RF losses the circuit in figure 2.5.b can be modified as proposed in figure 2.6.

The current flowing in the parasitic capacitors depends on the partition between C_{par} and the impedance Z_x at the sources of M1 and M2, and is independent from the IF load impedance.

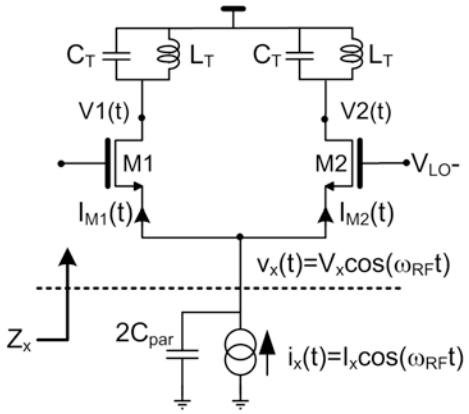

Figure 2.6: Circuit for the evaluation of RF losses.

2.2.3 Considerations on loss mechanisms

After this overview on losses mechanisms, it results that the LMV cell with a virtual ground as IF output load (current LMV) suffers only of losses at RF, while being immune to any unwanted equivalent resistance at the output nodes. On the contrary, choosing a high impedance IF load (voltage LMV), makes the LMV cell more sensitive to the parasitic capacitances because it experiences losses both at low–frequency and high–frequency. The presence of a fundamental upper bound on the achievable gain and the major sensitivity to the parasitic elements of this last solution, suggest to prefer a virtual ground IF load. In the next section the analytical expression of the conversion gain for the current LMV configuration is derived.

2.3 Current mode LMV conversion gain

The current mode LMV cell losses can be evaluated starting from the circuit in figure 2.6, from which the expression of Z_x can be obtained. As shown in [13], the impedance Z_x can be derived opening the oscillator loop and driving the M1 and M2 gates with sinusoidal voltages at ω_{LO}. The impedance is obtained using a test current (i_x) at ω_{RF} , and evaluating the produced voltage (v_x) at M1 and M2 sources. Currents flowing in M1 and M2 can be expressed as follows:

$$\begin{aligned} I_{M1}(t) &= I_x \cos(\omega_{RF} t) \cdot \frac{1}{2}(1 + sign(\cos(\omega_{LO} t))) \\ &= \frac{I_x}{2}\cos(\omega_{RF} t) + \frac{I_x}{\pi}\cos((\omega_{RF} \pm \omega_{LO})t) + hh \\ I_{M2}(t) &= I_x \cos(\omega_{RF} t) \cdot \frac{1}{2}(1 - sign(\cos(\omega_{LO} t))) \\ &= \frac{I_x}{2}\cos(\omega_{RF} t) - \frac{I_x}{\pi}\cos((\omega_{RF} \pm \omega_{LO})t) - hh \end{aligned} \tag{2.5}$$

where *hh* stands for *higher harmonics*. The LC tank in figure 2.6, has a filtering effect on the currents in (2.6). In fact it filters–out all the higher harmonics (*hh*) and the terms at low–frequency, leaving only the radio–frequency common mode component. Thus voltages V1(t) and V2(t) in figure 2.6 can be expressed as:

$$V1(t) = V2(t) = \frac{I_x}{2}\cos(\omega_{RF} t) Z_{tankCM}(\omega_{RF}) \tag{2.6}$$

Moreover the voltage v_x can be expressed as a function of V1(t) and V2(t), being:

$$v_x(t) = \frac{V1(t) + V2(t)}{2} + \frac{V1(t) - V2(t)}{2} sign(\cos(\omega_{LO} t)) \tag{2.7}$$

Thus, from (2.6) and (2.7) it results:

$$v_x(t) = \frac{I_x}{2}\cos(\omega_{RF} t) Z_{tankCM}(\omega_{RF}) = V_x \cos(\omega_{RF} t) \tag{2.8}$$

where $V_x = Z_{tankCM}(\omega_{RF}) I_x/2$. Thus the impedance Z_x at M1–M2 sources, can be written as:

$$Z_x(\omega_{RF}) = \frac{V_x}{I_x} = \frac{Z_{tankCM}(\omega_{RF})}{2} \tag{2.9}$$

The down–converted signal (I_{IF}) can be evaluated as a partition of the input current between C_{par} and $Z_{tankCM}/2$. To obtain the analytical expression, it is necessary to consider the circuit in figure 2.7 and to assume M1 and M2 working in linear region with negligible on resistance.

Since V1(t)=V2(t), $I_{p1}(t) = I_{p2}(t)$ and the current flowing in the IF load is:

$$I_{IF}(t) = \frac{1}{2}(I_{M1}(t) - I_{M2}(t)) \tag{2.10}$$

Assuming full current switching, I_{M1} and I_{M2} can be expressed as follows:

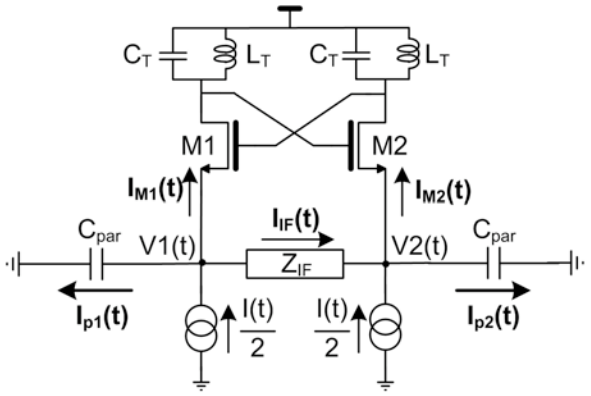

Figure 2.7: Circuit to obtain the analytical conversion gain expression.

$$\begin{aligned} I_{M1}(t) &= (I_{M1}(t) + I_{M2}(t)) \cdot \frac{1}{2} \cdot (1 + sign(\cos(\omega_{LO}t))) \\ I_{M2}(t) &= (I_{M1}(t) + I_{M2}(t)) \cdot \frac{1}{2} \cdot (1 - sign(\cos(\omega_{LO}t))) \end{aligned} \tag{2.11}$$

From (2.10) and (2.12), the I_{IF} current expression becomes:

$$I_{IF}(t) = \frac{1}{2}(I_{M1}(t) + I_{M2}(t)) sign\cos(\omega_{LO}t) \tag{2.12}$$

Thus the down–converted current is the total current flowing in M1 and M2 multiplied for a square–wave. The sum $I_{M1}(t) + I_{M2}(t)$ has only RF component, and can be evaluated considering the partition between the parasites and $Z_{tankCM}/2$, as shown in the following equation:

$$I_{M1+M2} = I(\omega_{RF}) \cdot \frac{1}{1 + j\omega_{RF}C_{par}Z_{tankCM}(\omega_{RF})} \tag{2.13}$$

From (2.12) and (2.13), the down–converted current becomes:

$$I_{IF} = \frac{1}{\pi} \frac{1}{1 + j\omega_{RF}C_{par}Z_{tankCM}(\omega_{RF})} I(\omega_{RF} - \omega_{LO}) \tag{2.14}$$

To obtain the total conversion gain, the output current due to the common mode component of the input signal has to be added to the contribution of the differential component, given by $I(\omega_{RF} - \omega_{LO})/\pi$. Thus the total conversion gain can be expressed as:

$$CG = \frac{1}{\pi} \frac{2 + j\omega_{RF}C_{par}Z_{tankCM}(\omega_{RF})}{1 + j\omega_{RF}C_{par}Z_{tankCM}(\omega_{RF})} \tag{2.15}$$

This equation shows that losses increase both when large parasites are present at the IF output, and when Z_{tankCM} is maximum.
Z_{tankCM} depends on the LC tank topology chosen. The topology used in [13] is the one reported in figure 2.4. It will be indicated hereafter as common mode LC tank since it resonates for both common mode and differential signals. In this case the impedance Z_{tankCM} at the oscillator frequency (ω_{LO}) is equal to $\omega_{LO}L_TQ_T$, resulting in the following conversion gain expression:

$$CG_{CMtank} = \frac{1}{\pi}\frac{2 + j\omega_{LO}C_{par}\omega_{LO}L_TQ_T}{1 + j\omega_{LO}C_{par}\omega_{LO}L_TQ_T} \tag{2.16}$$

In figure 2.8 the theoretical and simulated conversion gain is reported as a function of C_{par} (with f_{LO} equal to $2.45GHz$, an L_T of $2nH$ and a qulity factor Q_T equal to 20) and Q_T (with $f_{LO} = 2.45GHz$, $L_T = 2nH$ and $C_{par} = 100fF$).

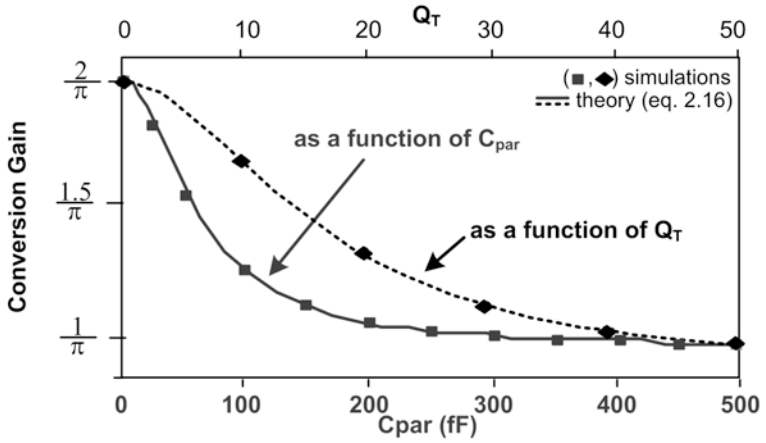

Figure 2.8: Conversion gain of the SOM with a common mode resonator.

The maximum gain is equal to $2/\pi$, and it can be obtained when C_{par} or the LC tank quality factor Q_T are null. Nevertheless in a real circuit neither C_{par} nor Q_T can be zero, respectively because switching pairs transistors introduce parasitics, and because the oscillation start–up condition has to be satisfied [18]. As reported in figure 2.8, as C_{par} or Q_T increases, the conversion gain decreases, tending quickly to the minimum value of $1/\pi$. Since a high Q_T reduces the LMV cell efficiency, while it improves the oscillator figure of merit (FoM[1]), a trade–off is introduced. This issue can be overcome choosing an alternative LC tank topology, with a lower common mode impedance at the

[1]The FoM of an oscillator is a parameter which considers both the noise and the power dissipation, allowing to compare oscillators performance. It can be expressed as follows:

LO frequency. The proposed topology is the differential LC tank in figure 2.9.b, which also provides a differential resonant impedance to set the proper oscillation frequency, and a DC path for SOM bias current. Since a purely differential LC tank can be realized only ideally, capacitors C_{CM} are added in figure 2.9.b. to consider the unavoidable presence of parasitics at the LO nodes.

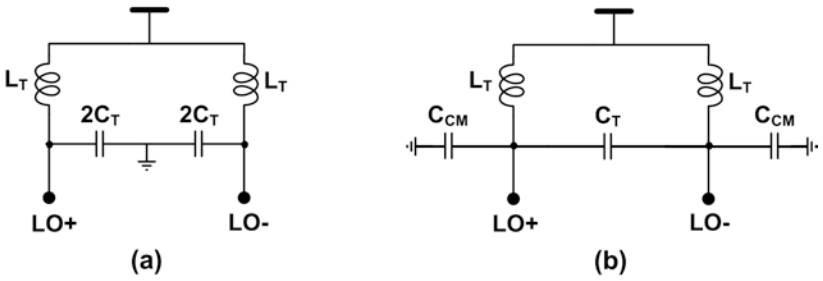

Figure 2.9: (a) Common mode and (b) differential resonant LC tank.

Choosing the differential topology, a further degree of freedom is introduced, since the common mode and differential resonances happen at different frequencies. In particular the common mode resonance frequency, which depends only on C_{CM}, is higher than the differential one, which is centred at the VCO oscillation frequency. Therefore the common mode impedance at $\omega_{RF} = \omega_{LO}$ can be expressed as follows:

$$Z_{tankCM}(\omega_{LO}) = \frac{\omega_{LO} L_T (j + \frac{1}{Q_T}) \frac{1}{j\omega_{LO} C_{CM}}}{\omega_{LO} L_T (j + \frac{1}{Q_T}) + \frac{1}{j\omega_{LO} C_{CM}}} \tag{2.17}$$

Inserting (2.17) in (2.15), the down–conversion gain of the LMV cell with a differential LC tank becomes:

$$CG_{Dtank} = \frac{1}{\pi} \frac{2 + j\omega_{LO} C_{CM} \omega_{LO} L_T (j + \frac{1}{Q_T})}{1 + j\omega_{LO} (C_{par} + C_{CM}) \omega_{LO} L_T (j + \frac{1}{Q_T})} \tag{2.18}$$

Figure 2.10 reports a graph with the theoretical and simulated conversion gain when $L_T = 2nH$, $f_{LO} = 2.45GHz$ and $C_{CM} = 150fF$. The conversion gain Vs. C_{par} has been considered when $Q_T = 20$, while the parasitic capacitance used to plot the graph of the conversion gain Vs. Q_T is equal to $100fF$.

$FOM = 20Log_{10} \frac{\omega_{LO}}{\Delta\omega} - PN(\omega_{LO} - \Delta\omega) - Pdiss|_{dBm}$
Since the phase noise (PN) decreases when Q_T increases [16], the FOM benefits of a high quality factor inductor.

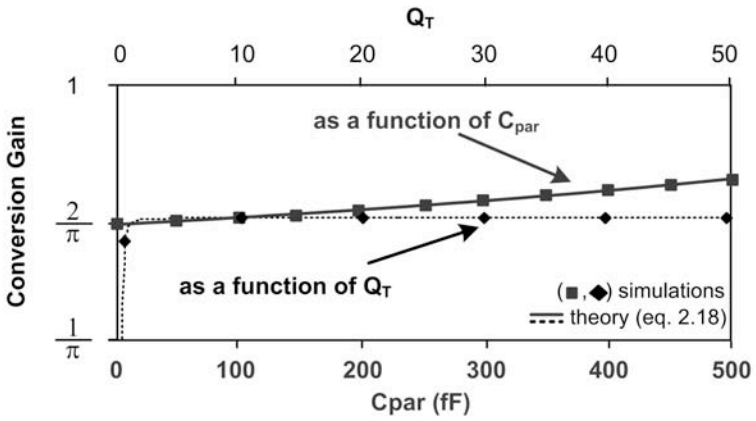

Figure 2.10: Conversion gain of the SOM with a differential resonator.

From figure 2.10, the Q_T effect on the SOM efficiency is negligible, and the conversion gain can be even higher than $2/\pi$. This effect is strictly related to Z_{tankCM} which resonates with the parasitic capacitors at the IF output nodes (C_{par}) producing a current amplification as occurs in shunt LC networks. Due to this effect, the conversion gain tends to its minimum value of $1/\pi$ only for very high parasitic capacitances ($\approx 4pF$ with the chosen L_T, f_{LO} and C_{CM}), which are not realistic in an actual design.

This analysis proves that the LMV cell conversion gain is strictly related not only to the choice of the IF load, but also to the LC tank topology. In particular the mixer efficiency is maximized when a low impedance IF load and a differential LC tank are used. In this case the conversion gain is less sensitive to parasitics and it is independent from the inductor Q_T, allowing to exploit the power and FoM benefits deriving from the use of high quality factor inductors.

2.4 Single coil quadrature front–end

In the LMV cell quadrature down-conversion can be performed cross–coupling in quadrature two identical cells [13]. Even if cross–copling assures a good quadrature accuracy, it requires to use two LMV cells in parallel. From the point of view of area, the use of two LC tanks is a significant penalty, which cannot be accepted in applications where area occupation is one of the most severely constrained targets [19]. A possible alternative, is to share the LC tank between the I and Q path, using a single coil, as shown in figure 2.11.

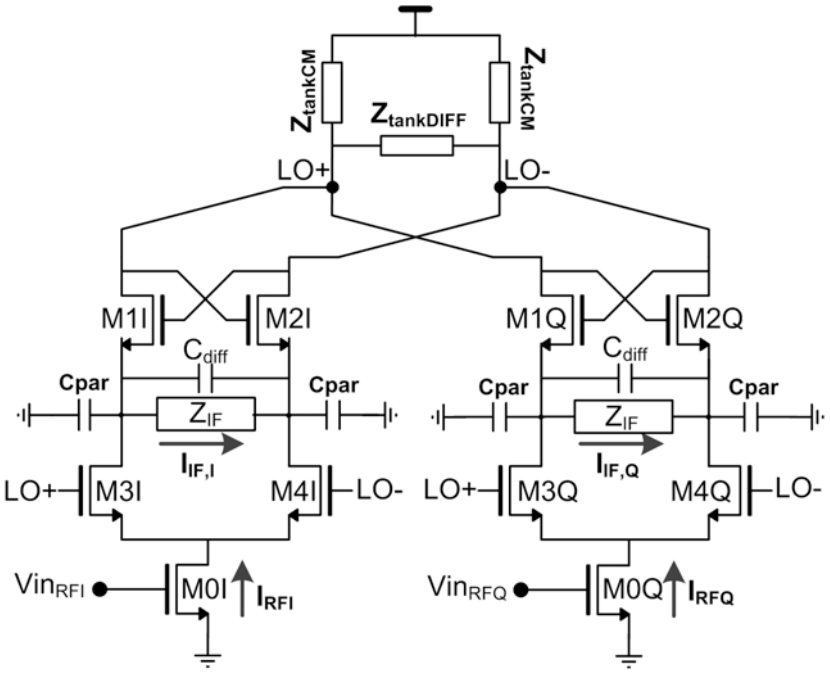

Figure 2.11: Quadrature SOM with LC tank sharing.

In this case an oscillator at twice the frequency of interest can be used together with frequency dividers to generate the I and Q LOs. Nevertheless, since in the LMV cell the switching pairs are driven by signals at the same frequency, this solution cannot be used in this design. For this reason an alternative architecture for I and Q generation is here presented. The proposed solution uses a single LO together with an LNA with I and Q outputs. The main drawback of this solution is the extra noise and eventual power consumption due to the circuits that perform the quadrature operation. However, in the case of sensor networks and ZigBee, the required noise figure is sufficiently relaxed that the extra noise can be tolerated [7], making such a topology the one of choice for the front–end. Nevertheless the LC tank sharing introduces additional mechanisms for amplitude/phase mismatches in the I and Q paths conversion gain. These mismatches will be studied and minimized in the following paragraph.

2.4.1 Amplitude/phase mismatches

To evaluate the I and Q conversion gains in the quadrature SOM, the circuit in figure 2.6.b has to be modified introducing the Q path, resulting in figure

2.12.

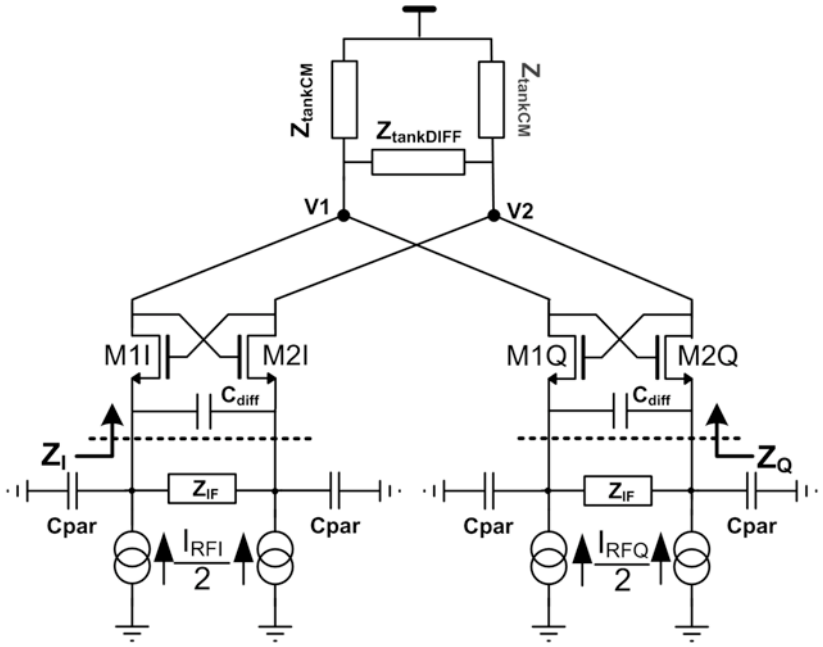

Figure 2.12: Circuit for the evaluation of RF losses in the quadrature front–end

Amplitude and phase mismatches mechanisms can be understood considering that losses in the I and Q paths depend on the partition between the impedances Z_I and Z_Q, and the parasitic capacitors at the IF nodes. Z_I and Z_Q can be derived as shown at the beginning of section 2.3, giving the following expressions:

$$\begin{aligned} Z_I(\omega) &= \frac{Z_{tankCM}}{2}(1-j) \\ Z_Q(\omega) &= \frac{Z_{tankCM}}{2}(1+j) \end{aligned} \tag{2.19}$$

These impedances are complex conjugated, producing an amplitude and phase mismatch in the current partitions which occur in the I and Q paths. Z_I and Z_Q depends only on the common mode portion of the LC tank impedance in analogy with the single cell. As it will be shown, the lower Z_{tankCM} is, the lower is its effect on the amplitude/phase mismatch.

In order to obtain the I and Q conversion gain expressions, the circuit can be transformed into the one reported in figure 2.13, exploiting the superposition of quadrature signals (a) and shortening nodes 1 and 2 for common mode

signals (b). In this scheme, the transistors are replaced by ideal switches, and Z_x is equal to $Z_{tankCM}/2$, being the parallel of Z_I and Z_Q in (2.19).

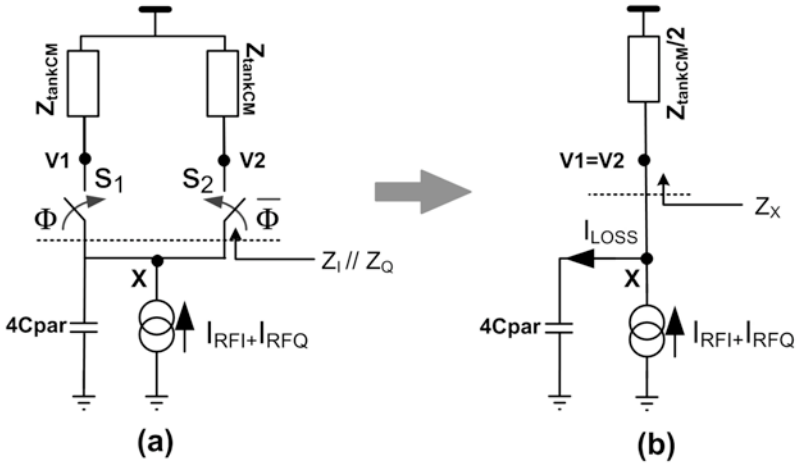

Figure 2.13: Quadrature SOM simplification: (a) superposition of effects and (b) shortening of nodes 1 and 2.

The total current loss due to the partition between the parasitics and Z_x, experienced in the I and Q paths can be expressed as follows:

$$I_{LOSS} = \frac{Z_{tankCM}}{Z_{tankCM} + \frac{1}{2j\omega C_{par}}}(I_{RFI} + I_{RFQ}) \tag{2.20}$$

Half of the losses in (2.20) occurs in the I path, while the other half in the Q path, allowing to derive the expression of the currents flowing in the LC tank at ω_{RF}. These currents are finally down–converted, giving a total conversion gain which is a function of Z_{tankCM}:

$$\begin{aligned} CG_I &= \frac{1}{\pi}\frac{2 + (\omega_{RF}C_{par}Z_{tankCM}(\omega_{RF}))(3j+1)}{1 + 2j\omega_{RF}C_{par}Z_{tankCM}(\omega_{RF})} \\ CG_Q &= \frac{1}{\pi}\frac{2 + (\omega_{RF}C_{par}Z_{tankCM}(\omega_{RF}))(3j-1)}{1 + 2j\omega_{RF}C_{par}Z_{tankCM}(\omega_{RF})} \end{aligned} \tag{2.21}$$

In particular when a differential resonator is used, the conversion gain at $\omega_{RF} = \omega_{LO}$, for $Q_T > 10$ becomes:

$$\begin{aligned} GC_{I-Dtank} &= \frac{1}{\pi}\frac{2(1 - \omega_{LO}^2 L_T C_{CM}) - (3-j)\omega_{LO}^2 L_T C_{par}}{1 - \omega_{LO}^2 L_T C_{CM} - 2\omega_{LO}^2 L_T C_{par}} \\ CG_{Q-Dtank} &= \frac{1}{\pi}\frac{2(-1 + \omega_{LO}^2 L_T C_{CM}) + (3+j)\omega_{LO}^2 L_T C_{par}}{-1 + \omega_{LO}^2 L_T C_{CM} + 2\omega_{LO}^2 L_T C_{par}} \end{aligned} \tag{2.22}$$

The corresponding theoretical and simulated amplitude and phase mismatches are reported in figure 2.14, where $f_{LO} = 2.45GHz$, $L_T = 2nH$, $C_{CM} = 300fF$ are assumed. Moreover a $C_{par} = 200fF$ is considered when the mismatches are evaluated as a function of Q_T, while a $Q_T = 40$ is used when the errors are evaluated as a function of C_{par}.

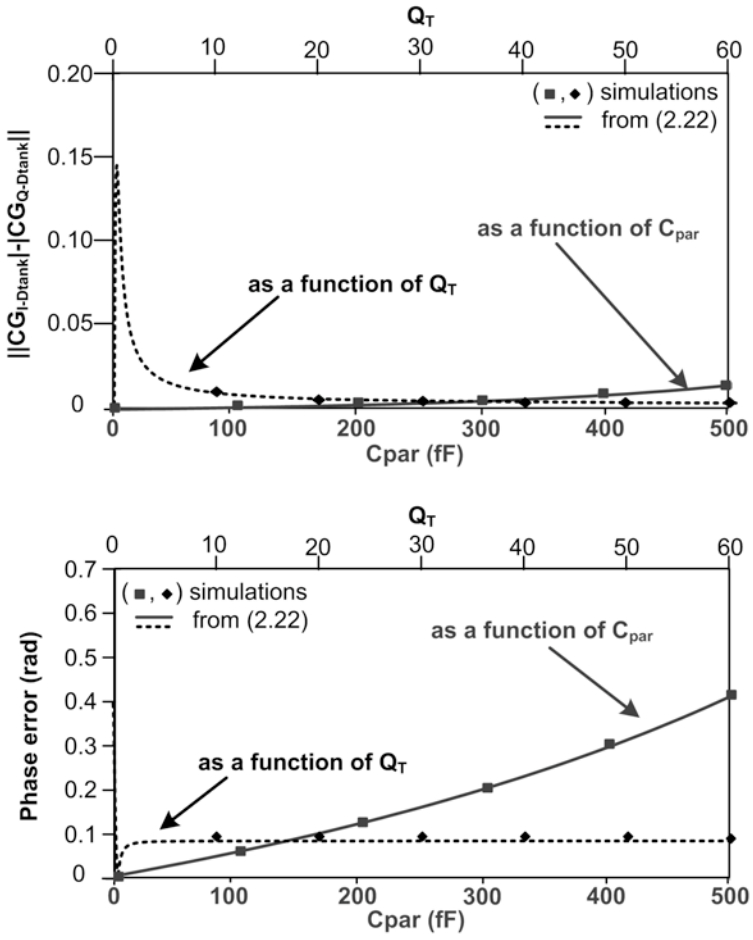

Figure 2.14: Amplitude and phase errors in the quadrature SOM with a differential resonator.

Theory and simulations show that with a differential LC tank the maximum amplitude mismatch is about 3% of the LMV cell gain, remaining in this range for C_{par} up to $500fF$ and for Q_T higher than 50. The phase error is constant with Q_T, while it increases with C_{par}, remaining in an acceptable range for ZigBee applications up to $300fF$ parasitics. In fact higher C_{par} values produce phase mismatches which compromise the receiver proper working.
If a common mode LC tank is used in the quadrature SOM, the I and Q

conversion gains are:

$$CG_{I-CMtank} = \frac{1}{\pi}\frac{2+\omega_{LO}^2 C_{par} L_T Q_T (3j+1)}{1+2j\omega_{LO}^2 C_{par} L_T Q_T}$$
$$CG_{Q-CMtank} = \frac{1}{\pi}\frac{2+\omega_{LO}^2 C_{par} L_T Q_T (3j-1)}{1+2j\omega_{LO}^2 C_{par} L_T Q_T} \tag{2.23}$$

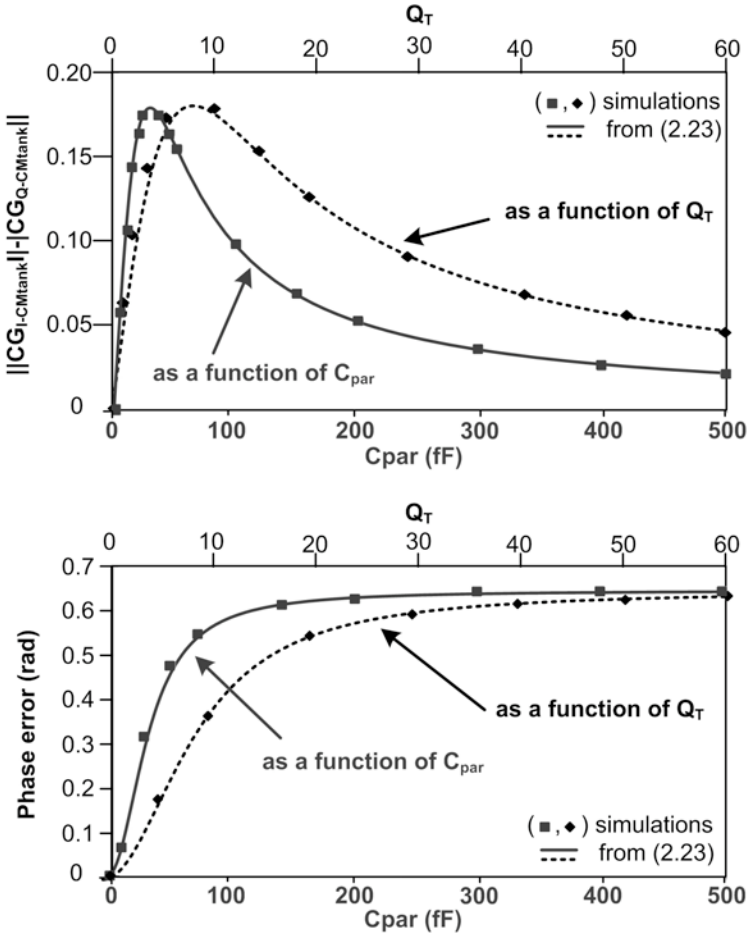

Figure 2.15: Amplitude and phase errors in the quadrature SOM with a common mode resonator.

As shown in figure 2.15 the amplitude mismatch between the I and Q paths decreases as C_{par} or Q_T increases (i.e. they tend to zero when the conversion gain tends to $1/\pi$). The phase error is high, except for very low C_{par} value.

Comparing figures 2.14 and 2.15, it results that the differential LC tank assures a lower amplitude and phase mismatch when it is shared between the

I and Q paths in a quadrature front–end. Nevertheless the parasitics at the IF output nodes have to be minimized in order to generate a quadrature error which is compatible with the requests of the standard IEEE 802.15.4.

2.5 Conclusions

In this chapter the LMV cell was presented [13] as the starting point for a very low–power and cheap RF front–end. The working principle of the cell is described and an improvement technique is proposed and demonstrated in order to maximize its conversion gain.
The described structure is then introduced in a single coil quadrature front–end, whose amplitude and phase mismatches due to the LC tank sharing between the I and Q paths are studied. The analysis shows that both the conversion gain and the I and Q mismatches can be optimized using a differential LC tank in the quadrature SOM.

Chapter 3

The receiver design

To design an IEEE 802.15.4 transceiver, both the RX and TX specs have to be derived starting from the standard definition document [4]. In particular this chapter focuses on the receiver, deriving the noise, linearity and minimum–maximum signal targets. After the specs definition, two front–end which differ for the noise performance and for the LC tank quality factor are proposed. The receiver is then completed with a base–band section, which is formed by a virtual–ground which reads the down–converted signal, and by a complex filter, which performs channel selection and image rejection.

3.1 IEEE 802.15.4 Specs

The IEEE 802.15.4 standard defines some tests to design a compliant receiver. The RX section passes the tests if its signal–to–noise ratio (SNR) is at least of $5 - 6dB$, with an input signal level between $-85dBm$ and $-20dBm$. The minimum required signal to noise ratio (SNR_{min}) is expressed in terms of acceptable noise figure, IIP3 and IIP2, and phase noise [16], which take account respectively of the noise introduced by the circuits, of their nonlinearities and of the LO non–idealities. These parameters are completely independent from the receiver architecture chosen, and their target values for an IEEE 802.15.4 compliant receiver are calculated in this section.

3.1.1 Receiver noise figure

The receiver noise figure (NF) requirement can be calculated from the *sensitivity test* defined by the standard. NF indicates the SNR degradation from the circuit input to its output [16] , and it can be defined as follows:

$$NF|_{dB} = 10Log_{10}\frac{SNR_{in}}{SNR_{out}} \tag{3.1}$$

From (3.1), the noise figure can be rewritten as:

$$NF|_{dB} = S_{in}|_{dBm} - N_{floor}|_{dBm} - SNR_{min}|_{dB} - Margin \tag{3.2}$$

where S_{in} is the sensitivity, and it is equal to $-85dBm$, while the N_{floor} is the noise at the receiver input. It corresponds to the thermal noise of the receiver input resistance (R_s), and depends on the channel bandwidth as follows:

$$N_{floor}|_{Watt} = \frac{V_{noise}^2}{2R_s} = kTB \tag{3.3}$$

With a $2MHz$ channel bandwidth, the noise floor is about $-111dBm$. Considering also the processing gain (chapter 1) and some margin, the noise figure of an IEEE 802.15.4 compliant receiver has to be lower than $20dB$.

3.1.2 Receiver IIP3

Unwanted spurs can be translated in the desired channel because of inter–modulation phenomena (in particular of the second and third order), affecting the system SNR [16]. To evaluate the acceptable third order inter–modulation, the IEEE 802.15.4 standard *intermodulation test* establishes the presence of the signal of interest at frequency f_0, and of two interferers, whose frequencies f_1 and f_2 satisfy the following conditions:

$$f_0 = 2f_1 - f_2 \tag{3.4}$$

$$|f_1 - f_0| = |f_2 - f_1| = \Delta f \tag{3.5}$$

Under these conditions, the required *Input Intercept* 3^{rd} *order Product* (IIP3) [16] can be expressed as follows:

$$IIP3 = \frac{1}{2}(P_{int1} + 2P_{int2} - P_{sig} + SNR_{min}) \tag{3.6}$$

Two different in band tests have to be considered: the minimum signal and the worst–case tests.

Minimum signal IIP3

The minimum signal IIP3 is calculated when the signals in figure 3.1 are at the receiver input.

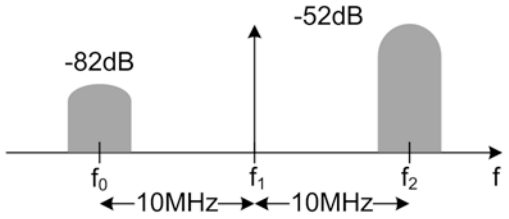

Figure 3.1: Signals for the IIP3 calculus (minimum signal case).

The involved signals are the one of interest with a power level $3dB$ higher than the sensitivity ($S_{in} = -82dBm$), a sinusoidal signal at frequency f_1 and a $2MHz$ band modulated signal at f_2, both with a power $30dB$ higher (and equal to $-52dBm$). Thus, replacing these values in (3.6), the resulting IIP3 requirement is $-36.5dBm$.

Worst–case IIP3

As stated by the standard, the maximum signal power at the receiver input is $-20dBm$. Since the alternate channel rejection requirement is $30dB$, in the worst case the interferer power is $-20dBm$, while the power of the desired signal is $-50dBm$ (figure 3.2).

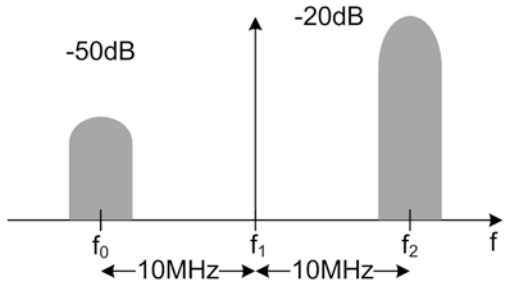

Figure 3.2: Signals for the IIP3 calculus (worst case).

In this case the IIP3 required is at least $-4.5dBm$.

3.1.3 Receiver IIP2

AM modulated interferers can generate second order inter–modulation products at low frequency, introducing an SNR degradation which can be expressed through the *Input Intercept* 2^{nd} *order Product* (IIP2) [16]:

$$IIP2 = 2P_{int} - P_{sig} + SNR_{min} \tag{3.7}$$

In order to pass the *AM interferer suppression test*, the standard requires a system SNR_{min} equal to $1dB$ considering also the processing gain, when at the receiver input there are two interferers at 10 and $20MHz$ offset from the carrier, with a power of $-30dBm$, and the signal of interest with a $30dB$ lower power ($-60dBm$) (figure 3.3).

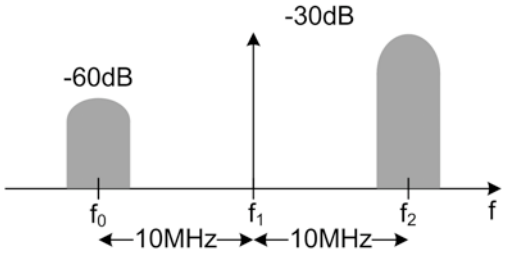

Figure 3.3: Signals for the IIP2 calculus (worst case).

This results in a minimum IIP2 equal to $1dBm$.

3.1.4 Receiver phase noise

The RF front–end down–converts the RF input signal to a lower frequency through a mixing with a local–oscillator tone. Even if ideally the LO should be a single precise tone in frequency, an actual oscillator can only approximate it, producing a larger spectrum with some spurs (figure 3.4) [16].

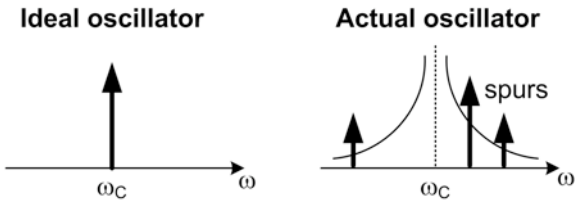

Figure 3.4: Output spectrum of ideal and actual oscillators.

The spectrum enlarging is due to a random variation in the phase of the sinusoid at the oscillator output, and can be evaluated through the phase noise parameter in the frequency domain. This spectrum non–ideality reduces the signal–to–noise ratio (SNR). In fact, in a real receiver the signal of interest may be accompanied by a large interferer in an adjacent channel. When the two signals are mixed with the LO input, the down–converted band consists of two overlapping spectra, with the wanted signal suffering from significant noise due to the tail of the interferer. This effect, which is called *reciprocal*

mixing is shown in figure 3.5.

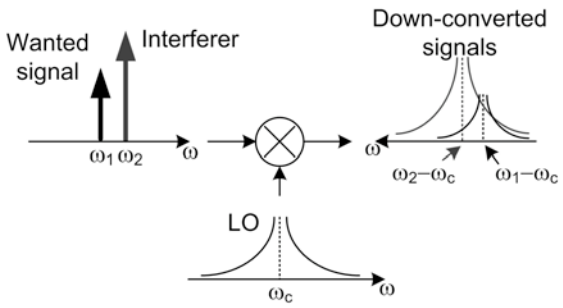

Figure 3.5: Reciprocal mixing.

To quantify the phase noise, the spectra in figure 3.6 are considered. The desired signal at frequency f_1, has a bandwidth equal to B and a power of P_{sig}. It is mixed with the LO, when an interferer with P_{int} power is present at $(f_1 + \Delta f)$.

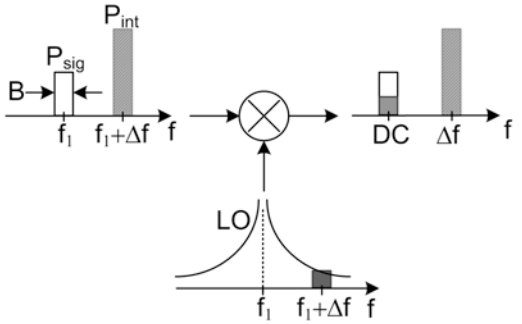

Figure 3.6: Signals to quantify phase noise.

To simplify the calculus, the LO spectrum can be approximated as a constant in the interferer band, whose value is equal to the one it assumes at the center of the channel. The noise down–converted in the signal band (at DC in figure 3.6) is equal to the LO spectrum integral multiplied for P_{sig}. Since the phase noise is referred to the carrier, the noise power is referred to the signal and experiences the same amplification. Thus the P_{noise} on the down–converted signal band, can be expressed as:

$$P_{noise}|_{dB} = P_{int}|_{dB} + PN(\Delta f)|_{dBc/Hz} + 10Log_{10}B \tag{3.8}$$

The phase noise for an IEEE 802.15.4 compliant receiver can be calculated starting from the *blocking test* defined by the standard. In this test the wanted

signal has a power which is $3dB$ higher than the sensitivity. Thus the maximum P_{noise} in presence of an interferer is equal to the input thermal noise ($ThermalNoise_{in} = N_{floor}|_{dBm} + NF|_{dB} = -91dBm$, see paragraph 3.1.1). The phase noise can be calculated as:

$$PN(\Delta f) = ThermalNoise_{in} - P_{int}(\Delta f) - 10Log_{10}B - Margin \tag{3.9}$$

where $PN(\Delta f)$ is the oscillator phase noise atΔ f from the carrier, $P_{int}(\Delta f)$ is the power of an interferer atΔ f from the carrier, B is the signal bandwidth. The standard requires to satisfy the SNR target when the involved signals are the wanted one with $P_{sig} = -85dBm$ and an interferer in the adjacent or alternate channel. Considering an interferer in the adjacent channel the following values have to be replaced in (3.9):

$$\begin{aligned} \Delta f = &\quad 5MHz \\ P_{int}(\Delta f) = &\quad -85dBm \\ B = &\quad 2MHz \end{aligned}$$

resulting in a required phase noise of $-74dBc/Hz$ at $5MHz$ from the carrier considering a $5dB$ margin. With an interferer in the alternate channel, the values to replace in (3.9) become:

$$\begin{aligned} \Delta f = &\quad 10MHz \\ P_{int}(\Delta f) = &\quad -55dBm \\ B = &\quad 2MHz \end{aligned}$$

resulting in a request of $PN(10MHz) = -104dBc/Hz$.
Moreover, since the frequency synthesizer is shared between the receiver and the transmitter, as explained in chapter 1, to establish the actual PN target, also the phase noise requirement in transmission has to be considered.
In the $2.45GHz$ band, the U.S. requirement establishes a TX phase noise worst case of $-101dBm$ at $3.5MHz$ from the carrier. The processing gain of $9dB$ raises the allowed transmitted phase noise for a $0dBm$ transmission to $-92dBm/Hz$ at $3.5MHz$ offset from the carrier. At the maximum level of transmitted power ($10dBm$) the phase noise requirement becomes $-102dBc/Hz$ at $3.5MHz$.
In order to find the most severe requirement, the derived targets have to be referred to the same frequency offset from the carrier, which is chosen to be

$1MHz$. Since in this frequency region the phase noise increases with $20dB$ per decade [16], the phase noise target to satisfy the RX path constraints are $-72dBc/Hz$ and $-84dBc/Hz$, considering respectively the adjacent and alternate channel rejection, while the TX target is $-86dBc/Hz$. This is the hardest constraint on the phase noise, and it becomes the target to design an IEEE 802.15.4 compliant transceiver.

3.1.5 Receiver specs

In table 3.1 all the RX specs to design an IEEE 802.15.4 compliant transceiver are resumed.

Design parameter	**IEEE 802.15.4 target**
NF	$< 20dB$
IIP3	$> -36.5dBm$ (minimum signal)
	$> -4.5dBm$ (worst case)
IIP2	$> 1dBm$
PN(1MHz)	$< -86dBc/Hz$

Table 3.1: ZigBee compliant receiver specs

3.2 RX section design

The core of the receiver is the single coil quadrature SOM described and optimized in chapter 2. This structure requires to generate both the in–phase and quadrature RF signals, at the minimum cost in terms of power consumption. In this section two different quadrature generation techniques and strategies to obtain input matching are proposed, producing two different RX front–end. Regardless of the front–end implementation, the down–converted signal current produced by the SOM circuit is sensed at IF through a virtual ground implemented via two trans–impedance amplifiers (TIAs). The output voltage signal of the TIAs from the I and Q paths are combined through a complex third order filter, as shown in figure 3.7, that performs image rejection and channel selection,. The same base–band is used in the two receivers, associated with the different RF topologies.

In this section all the receivers building blocks design details will be explained, both for the RF front–end and for the base–band signal processing

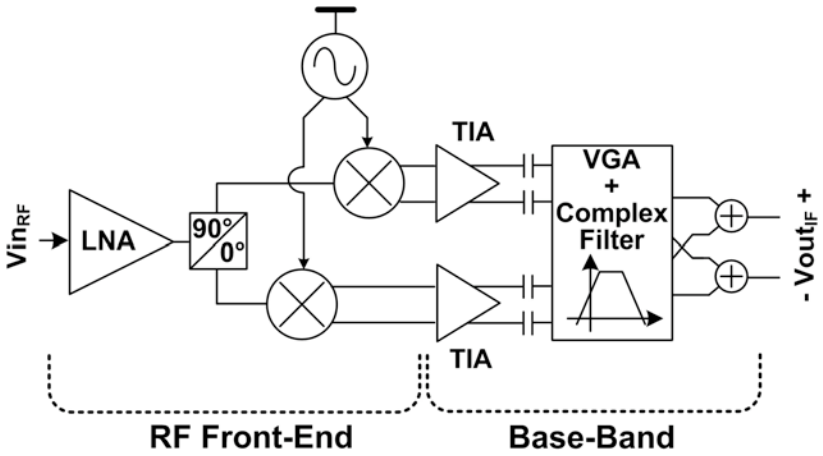

Figure 3.7: Receiver architecture.

units.

3.2.1 Quadrature generation and input matching

Quadrature generation and LNA input matching can be obtained using different techniques, depending on the bias sharing between the LNA and the SOM. In fact the low–noise–amplifier can be stacked with the SOM, or it can be fed by an independent current source. When a low Q_T (less than 20) LC tank is used, the optimal bias current of the VCO is comparable with the one of the LNA, and stacking of all blocks can give matching, RF signal amplification and down–conversion without any extra power consumption besides the one used for the SOM. Although in this case RF signals quadrature can be generated through capacitive degeneration [19], this choice does not allow to inductively degenerate the LNA for a low–noise input matching. To exploit the noise benefits of the source degeneration, it is necessary to choose a different quadrature generation technique, avoiding the stacking of the LNA and SOM. The LNA has to be realized separately, and quadrature can be generated at its output through an RC–CR load [20]. This solution is particularly suitable when a high Q_T inductor (e.g. a bondwire) is used in the SOM. In this case both a small current can be used in the SOM to achieve the desired LO amplitude, and a small current can be used in the efficient source degenerated LNA to obtain the target noise figure. This approach also helps to reduce cost, since it eliminates expensive integrated coils.

Quadrature by capacitive degeneration

When low Q_T integrated coils are used, the current distribution is optimized stacking the LNA with the SOM. In this case, a 90 degrees phase shift is obtained using the circuit in figure 3.8 [19].

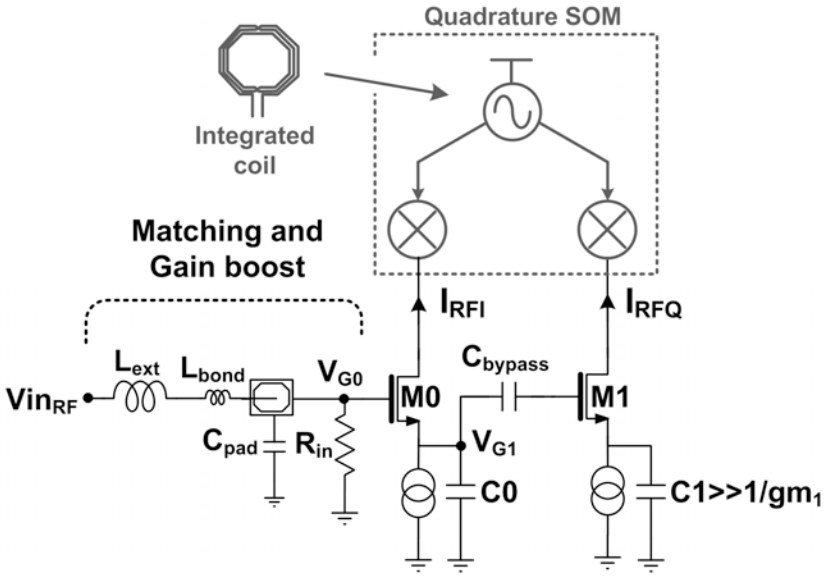

Figure 3.8: LNA input matching and quadrature generation through capacitive degeneration.

The source of transistor M0 is degenerated with a capacitor C0 and its drain current is sent to the mixer for the I signal path. At the same time the voltage at the source of M0 is connected through the bypass capacitor (C_{bypass}) to the input of a common source stage, obtained by placing at the source of M1 a big capacitance C1. The produced M1 drain current is in quadrature respect to the M0 drain current, and it flows into the mixer for the Q signal path. The generated quadrature drain currents (I_{RFI} and I_{RFQ}) can be expressed as follows:

$$\begin{aligned} I_{RFI} &= \frac{j\omega C0 gm_1}{gm_1 + j\omega C0} V_{G0} \\ I_{RFQ} &= \frac{gm_1}{j\omega C0} I_{RFI} \end{aligned} \tag{3.10}$$

From (3.10) the 90 degrees phase shift is guaranteed in a wide frequency range while the amplitude matching is obtained only around the working frequency ω_0 setting $C0 = g_m/\omega_0$. The amplitude error for $\omega \neq \omega_0$ remains

sufficiently low in the frequency range of interest to satisfy with margin the requests of the IEEE 802.15.4 standard. Since the LNA source is degenerated by a capacitance, the input matching through inductive degeneration is not possible. In this case the matching is obtained through an internal resistor R_{in} and a L–match network. Although the use of a passive termination tends to increase the noise figure, this effect is mitigated by the resonant circuit at the input, which boosts the LNA transconductance, providing a voltage gain at the gate of M0. In addition, inductance L_{ext} in figure 3.8, together with the pad capacitance, forms a narrow–band input matching network.
As an inductive degeneration synthesizes a positive resistance, a capacitive degeneration synthesizes an impedance whose real part is negative and can be expressed as:

$$Re[Z_N] = -\frac{gm_0}{\omega^2 C_{gs0} C0} \tag{3.11}$$

Since a negative resistance is present, a stability condition for the circuit has to be found and satisfied. The stability depends on the quality factors of the network formed by the pad capacitance and the resistance R_{in} (which has an impedance equal to Z_P), and of the network formed by transistor M0 and capacitance C0 (which has an impedance equal to Z_N) (figure 3.9).

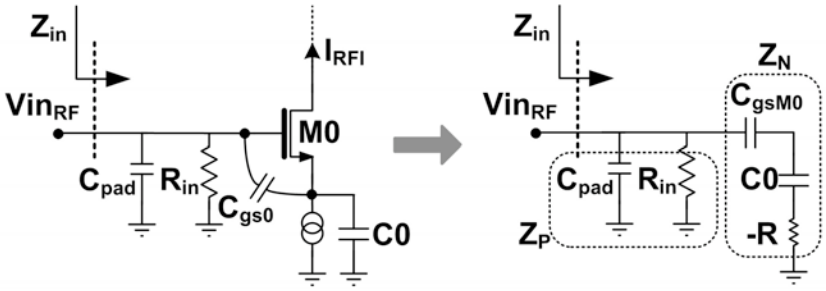

Figure 3.9: LNA input matching and impedance synthesized by a capacitive degeneration.

To guarantee stability, the quality factor of the overall network has to be positive. This requires that the quality factor of Z_P is greater than the absolute value of the quality factor of Z_N. Thus, the positive passive resistance R_{in} has to guarantee input matching taking into account the effect of the unwanted negative resistance that appears in parallel with it.

Quadrature generation through RC–CR load

When the LNA is biased with a separate current and high Q_T inductors are used in the LC tank the use of an RC–CR load at the LNA output becomes the simplest solution to generate quadrature on the RF path [20] as shown in figure 3.10.

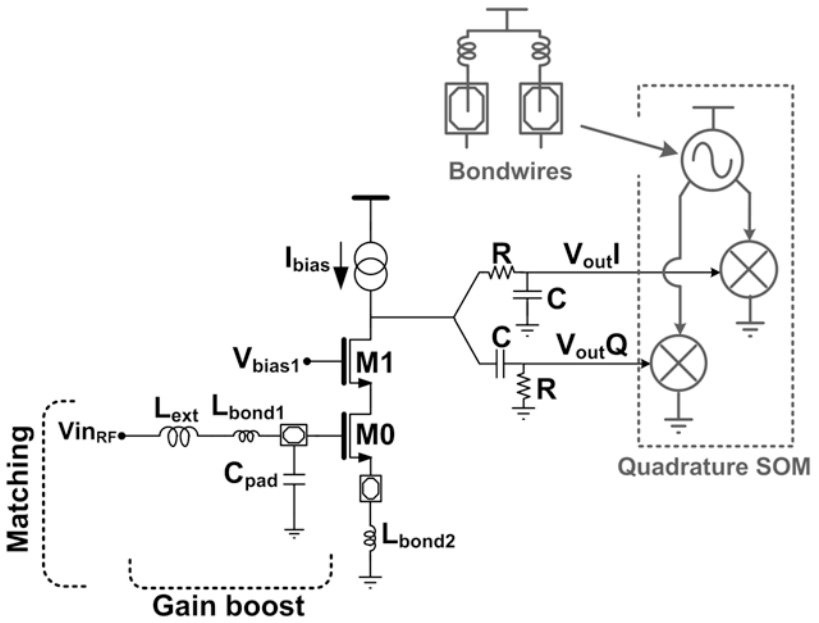

Figure 3.10: LNA input matching and quadrature generation through RC–CR load.

The load network has to be dimensioned in order to synthesize a zero and a pole at the working frequency ω_0, while trading off between minimum noise contribution and area occupation. As in the previous case, even if the amplitude matching is obtained only around the cut–off frequency $1/(2\pi RC)$, the mismatch between the I and Q paths remains sufficiently low in the frequency range requested by the standard.
In this case the LNA input matching can be realized through inductive degeneration. Even if this is the best solution in terms of noise performance, the use of integrated inductors increases the die area. To overcome this issue, the real impedance can be realized by a bond–wire inductive degeneration, which leads to the lowest possible die area [20]. Since there is some concern about bondwire inductors reproducibility, to compensate the variations of $L_{bond1,2}$ and to center the frequency of operation, an external inductor L_{ext} can be added in series with the input bond–wire L_{bond1}. Moreover, the presence of a reso-

nant input matching network has the added benefit to avoid injection–locking phenomena thanks to its narrow–band filtering effect.

3.2.2 Base band design: virtual ground and complex filter

Virtual ground design details

The differential virtual ground is provided by a trans–impedance amplifier in a gain boosted cascode configuration (figure 3.11.a), which allows to synthesize a low impedance over a large bandwidth.

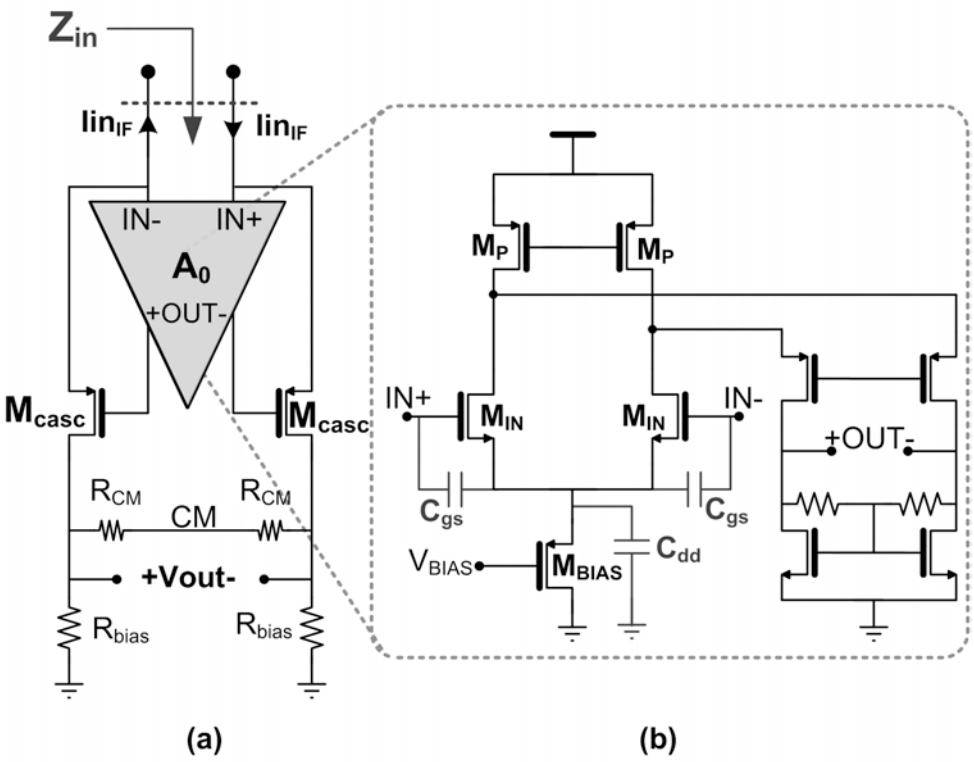

Figure 3.11: Trans–impedance amplifier.

At low frequency the synthesized impedance is:

$$Z_{INdiff} \approx \frac{2}{A_0 gm_{casc}} \tag{3.12}$$

Where A_0 is the DC gain of the core amplifier. From (3.12), to obtain a virtual ground, the product $A_0 gm_{casc}$ should be maximized. gm_{casc} can be increased by choosing a larger aspect ratio for the two transistors M_{casc}, but at the cost of larger parasitic capacitors at the IF output nodes, which affect

the quadrature SOM amplitude and phase mismatches. A higher transconductance of transistors M_{casc} can be obtained also increasing their bias current, at the cost of an increasing dissipation. Since maximizing gm_{casc} introduces some drawbacks, Z_{INdiff} is minimized designing a core amplifier with a high gain A_0, over a large bandwidth ($10MHz$) related to the ZigBee standard requirement ($3MHz$). This gain/bandwidth target, can be satisfied using a folded cascode core (figure 3.11.b), which also minimizes the parasitic capacitive load added at the IF output nodes. In fact, in this case, the capacitive load due to the amplifier is formed by the series of $2C_{gsIN}$ and $C_{ddM_{BIAS}}$.

The designed amplifier has a simulated gain equal to $31dB$ over a $10MHz$ bandwidth, and it synthesizes a differential 20Ω impedance using a total current of $60\mu A$ in transistors M_{casc}. Assuring low impedance over a large bandwidth for the virtual ground, limits current losses and results in high linearity in presence of large interferers.

Complex filter design details

Since a low–IF architecture is chosen for the two ZigBee receivers, image rejection has to be implemented [16]. In the proposed circuit image rejection and channel filtering are combined in the base–band complex filter.
A complex filter can be obtained from a real one, shifting its poles along the imaginary axis. The resulting complex poles are no longer conjugated [21], since the transfer function coefficients become complex. In figure 3.12, an example of the pole shifting is reported for a 3^{rd} order Butterworth filter.

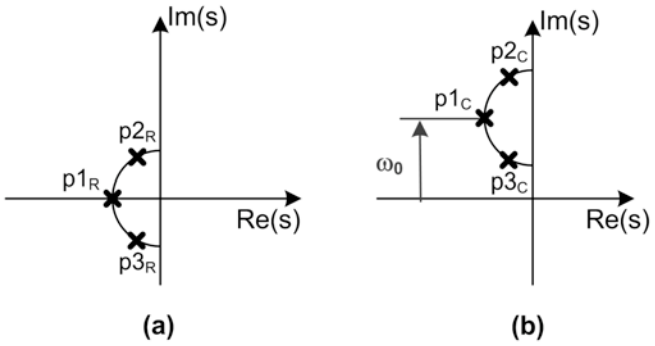

Figure 3.12: (a) Real and (b) complex filter poles.

The poles shifting along the imaginary axis, produces a transfer function shifting along the frequency axis, as reported in figure 3.13: a real third order low–pass Butterworth filter generates a complex band–pass filter through the

linear transformation $j\omega \rightarrow j(\omega - \omega_0)$.

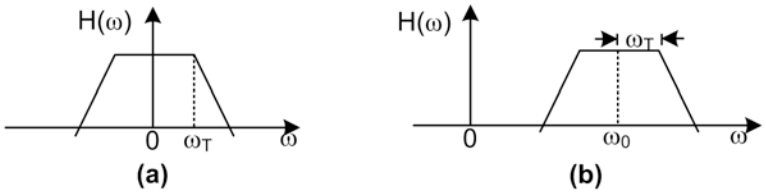

Figure 3.13: (a) Real and (b) complex filter transfer functions.

The band–pass complex filter can be exploited in the low–IF receivers to eliminate the image problem, as shown in a simplified example in figure 3.14. In this case only the positive frequency signal spectrum is considered, with the corresponding image at negative frequencies.

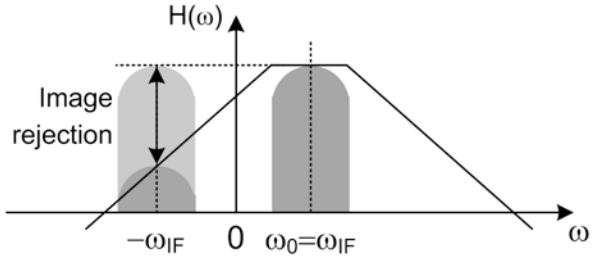

Figure 3.14: Image rejection of a complex band–pass filter.

For the ZigBee the needed image rejection for proper demodulation can be derived from its target adjacent channel rejection ($0dB$) [7], and it results to be better than the SNR ($6dB$). Any higher image rejection value is in excess of the standard requirements and improves the receiver robustness [7].
For the ZigBee receiver a 3^{rd} order complex filter with a central frequency $f_c = 2MHz$ and a bandwidth equal to $1MHz$ is designed, starting from a low–pass real 3^{rd} order Butterworth with a cut–off frequency of $1MHz$. Referring to figure 3.12, the poles of the real filter are:

$$\begin{aligned} p1_R: &\quad -1MHz \\ p2_R: &\quad -0.5MHz + j0.87MHz \\ p3_R: &\quad -0.5MHz - j0.87MHz \end{aligned}$$

The corresponding complex filter poles, are obtained shifting the real ones of $2MHz$ along the imaginary axis, obtaining therefore:

$$
\begin{aligned}
p1_C: &\quad -1MHz + j2MHz \\
p2_C: &\quad -0.5MHz + j2.87MHz \\
p3_C: &\quad -0.5MHz + j1.13MHz
\end{aligned}
$$

Since the linearity required by the ZigBee standard is quite relaxed while the power consumption is more severely constrained, the filter topology chosen is a gm–C one, which tends to trade-off limited linearity with small power for a given bandwidth [22] [23]. To make the design as simple and modular as possible, the 3^{rd} order filter is implemented as the cascade of three simple complex poles. To synthesize a single pole, two gm–C filters with real transfer function are transformed into a complex one by adding an imaginary term which is obtained cross-connecting between the I and Q paths the transconductances gm_{IM} as shown in figure 3.15.

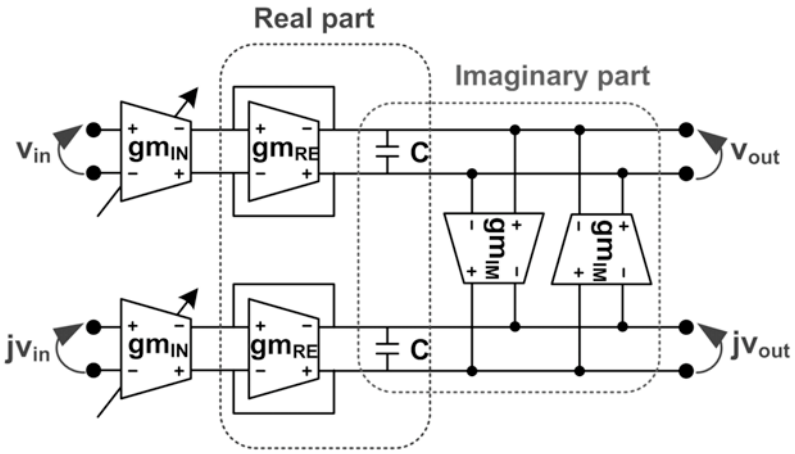

Figure 3.15: Block diagram of the gm–C IF complex filter stage.

The complex pole frequency can be expressed as:

$$\omega_{comp} = \frac{gm_{RE}}{2C} + j\frac{gm_{IM}}{2C} \tag{3.13}$$

where the real part of the synthesized pole fixes the bandwidth, while the imaginary part sets the central frequency. The gain and the pole location of each stage can be calibrated changing the MOS transconductance acting on the bias current I_{BIAS}. Nevertheless it is worth noticing that while the central frequency is well determined, the bandwidth is sensitive to the effects of the

g_{ds} of the other transconductance stages. Therefore, to reduce this effect, each gm is realized through a double–cascode transconductor, as shown in figure 3.16.

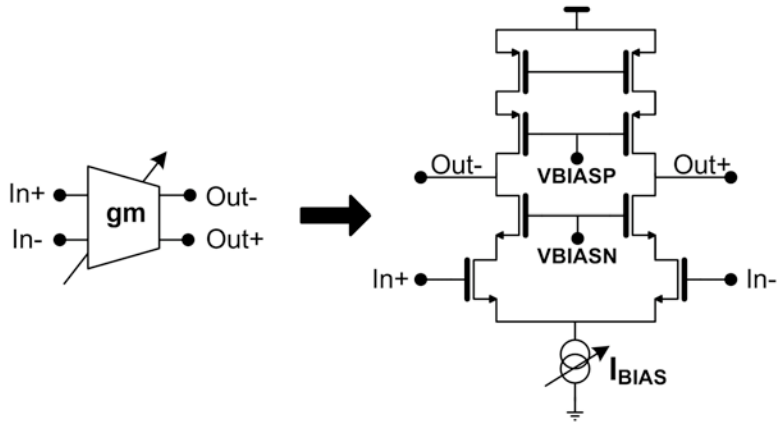

Figure 3.16: Double–cascode transconductor used in the design of the gm–C filter.

3.2.3 Receiver prototypes: measurements and results

The two receivers have been integrated in the same chip using a 90nm CMOS technology. Pads are ESD protected and for the ground and the voltage supply multiple pads with multiple bondings are used. The micrographs of the two integrated prototypes are shown in figure 3.17.

In both pictures the different building blocks have been outlined and marked. Figure 3.17.a shows the coil–free receiver (bond wire inductors), which results in an active die area of $0.23mm^2$. Figure 3.17.b corresponds to the version that makes use of single integrated inductor whose area occupation increases to $0.35mm^2$. The area difference between the two versions becomes much more significant if only the RF portion of the die is considered. In fact, the base band portion is common to the two implementations, and has an area of about $0.2mm^2$ i.e. almost 90% of the coil free version. Contrary to what usually occurs in integrated transceivers, where the limiting factor in the attempt to reduce the die area is the RF front-end, in this case the area is dominated by the base–band section. Considering only RF front-end, the single coil prototype has an area of about $0.15mm^2$, which reduces to only $0.03mm^2$ for the coil–free implementation. The die was bounded on a dedicated RF board, with gold plated microstrips on an FR4 substrate. Properly dimensioned 50Ω strip lines carry the input signal from the SMA connectors to the die itself.

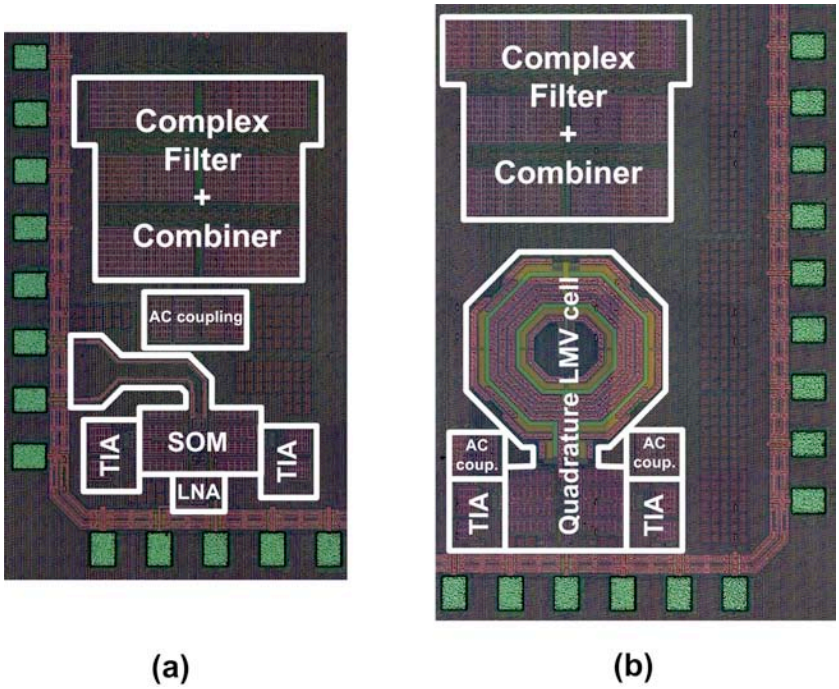

Figure 3.17: (a) Coil–free and (b) single integrated coil receiver prototypes micrographs.

The input reflection coefficient measurements are reported in figure 3.18.

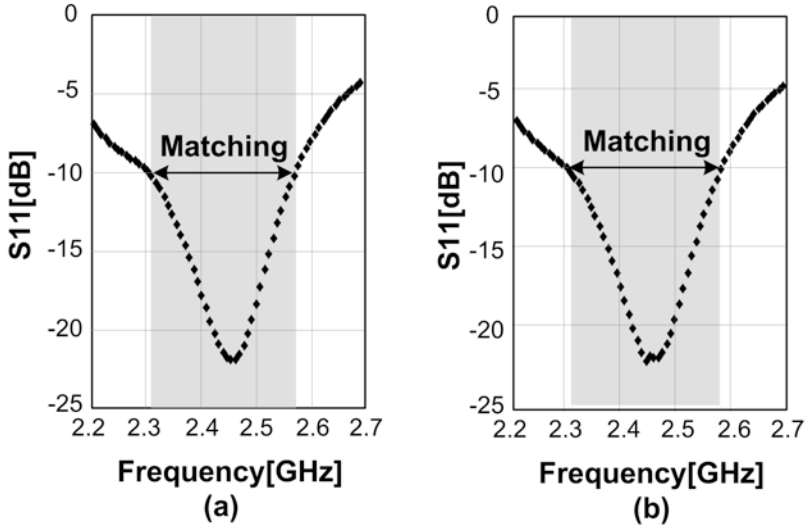

Figure 3.18: (a) Coil–free and (b) single integrated coil receiver prototypes S11 measured.

The two different matching techniques used result in a good input matching

in the ZigBee 2.45GHz band. The frequency response of the receivers at the channel selection filter output is reported in figure 3.19.

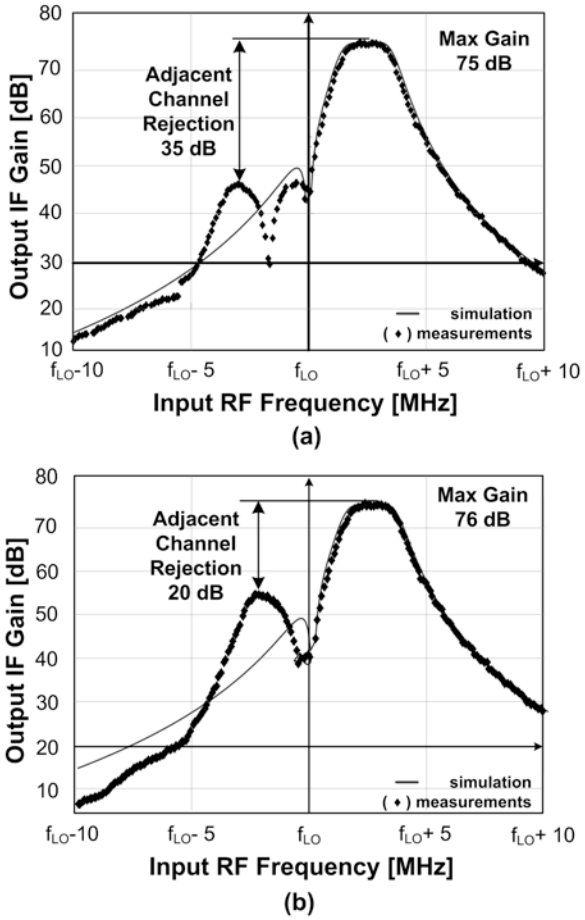

Figure 3.19: (a) Coil–free and (b) single integrated coil receiver prototypes IF gain profile measured.

The maximum in band gain exceeds 75dB (from 1MHz to 3MHz) in both the prototypes, while the image rejection, obtained without any calibration, is quite different in the two cases (20dB versus 35dB respectively). Nonetheless in both cases the achieved value ensures a safe margin form the target spec of 6dB. The reduced image rejection value for the coil free case is due to an incorrect estimation of the parasitic capacitance of the RC–CR network, which introduces an error in the desired 90 degrees phase shift between the I and Q signals. On the other hand, the potential phase error associated with the I and Q SOMs was minimized through the use of a differential resonant tank. Other measurements on the coil–free prototype show a noise figure integrated over the IF band (from 1MHz to 3MHz), of about 10dB, an in band

third order intermodulation IIP3 (at maximum gain) of $-13dBm$ and a VCO phase noise of about $-124dBc/Hz$ measured at an offset of $3.5MHz$ from the carrier (as defined by the ZigBee standard [4]). Similar performance are displayed by the single integrated coil prototype, which achieves an averaged noise figure between $1MHz$ to $3MHz$ of $9dB$, an in band IIP3 of $-12.5dBm$ and a VCO phase noise at $3.5MHz$ offset from the carrier of $-116dBc/Hz$. While comparing the two prototypes performance, it is worth to notice that the NF for the coil–free prototype is larger due to the error in the quadrature generation in the RC–CR network (as explained before) which worsen noise. Both prototypes dissipate $3.6mW$ of power since they are drawing only $3mA$ of currents from a $1.2V$ supply. The required $3mA$ can be divided in $2mA$ used by the RF blocks and $1mA$ by the TIAs and the baseband filter. Moreover, in the coil free prototype the supply voltage can be lowered down to 1V still maintaining proper operation, since the SOM and the LNA are not staked. In Table I all the measurements performed on the two prototypes are reported and compared to the state of the art for complete ZigBee receivers. The coil–free prototype is indicated as *prototype I*, while the single integrated coil is indicated as *prototype II*.

The comparison is made in terms of spurious free dynamic range (SFDR), which accounts for both the noise figure (or, equivalently, sensitivity) and the linearity (IIP3). As it is shown in [16], it can be evaluated from:

$$SFDR = \frac{2(IIP3 - F)}{3} - SNR_{min} \tag{3.14}$$

where $F = -174dBm + NF + 10Log_{10}BW$ and SNR_{min} is assumed to be $1dB$, considering also the gain processing. Both the prototypes presented here show a SFDR in line with the state of the art, but requiring less of half of the die area of previous implementations and/or using much less power consumption. Notice that in both the measured prototypes the oscillator is free running, since the frequency synthesizer is shared between the receiver and the transmitter, and it will be presented in chapter 4.

	[5]	[6]	[7]	[8]	[9]	This work p.I	This work p.II
Gain (dB)	—	—	—	—	33	76	75
NF (dB)	24.7	7.3	5.7	7	7.5	10	9
IIP3 (dBm)	-4.5	-8	-16	-7.5	-10	-13	-12.5
SFDR (dB)	53.5	62.8	58.5	—	61.3	57.7	58.7
PN@3.5MHz	—	—	—	-111	—	-124	-116
Pdiss (mW)	15	6.3	17	1.45	5.4	3.6	3.6
Int. coils	6	2	4	3	2	0	1
Area (mm^2)	2.1	2.075	0.8	1.8	0.235	0.23	0.3
V_{DD}**(V)**	1.8	1.8	1.8	0.4	1.35	1.2	1.2
Tech.(μm)	0.18	0.18	0.18	0.13	0.09	0.09	0.09

Table 3.2: ZigBee compliant receiver state of the art.

3.3 Conclusions

In this chapter, after deriving the ZigBee specs to design a compliant receiver, two possible implementations for the architecture in figure 3.7, which include the front–end plus the base–band are proposed. They differ in the practical way in which the received signal quadrature is obtained. In the first one the circuits which perform quadrature are biased by reusing the current of two LMV cells. The second instead uses an inductively degenerated LNA, biased with a separate current with respect to the SOM, which drives two passive quadrature circuits. The choice between the two implementations is related to the noise target and to the quality factor of the available inductors. The two receivers have been integrated in a $90nm$ CMOS technology. The measurements resulted in a power consumption of $3.6mW$, and an active die area of $0.23mm^2$ when the LNA is separated from the self–oscillating–mixer and high Q_T bond–wire inductors are used in the LC tank, while the active area increases to $0.35mm^2$ when the LNA is stacked with the SOM and an integrated inductor is used. Both prototypes have area and/or power consumption below the state of the art, while providing similar level of performance.

Chapter 4

The transmitter design

In the design of the proposed ZigBee transceiver the reuse of building blocks between the TX and RX path is maximized. The transmitter performs frequency modulation using a frequency synthesizer, which is also used in RX mode to stabilize the local oscillator frequency.
Since the frequency synthesis is performed using a locked–loop, in the first part of this chapter the closed loop noise profile needed to satisfy the IEEE 802.15.4 requirements is derived. After justifying the choice of an all–digital frequency–locked–loop (ADFLL) to implement the frequency synthesizer, the ADFLL building–blocks are described and the design details are provided. Finally, the chapter focuses on the power amplification section, and the designed low–power efficient power amplifier (PA) is proposed.

4.1 Transmitter requirements for ZigBee applications

Since the transmitter is in fact built up by a frequency synthesizer (see chapter 1), the first step to properly design it, is to derive the required phase noise profile, which resumes the standard in band and out of band noise requests.

Required bandwidth

The choice of the bandwidth is a key–point in the design of a frequency synthesizer, since it influences the speed and the stability of the system itself. While the speed requirement sets the minimum bandwidth (BW_{min}), the stability issue introduces a higher limit on the bandwidth (BW_{MAX}).
BW_{min} has to be compatible with the RX–TX turn–around–time (T_{RX-TX}), and with the modulation requirements. In this case T_{RX-TX} has to be lower than 12 symbol periods [4]; since the symbol–rate is $62.5kHz$ in the $2.45GHz$ band (see table 1.1), and therefore BW_{min} is $5.5kHz$.

For what concerns modulation, for ZigBee in the $2.45GHz$ band, it is a 16–ary orthogonal $2Mbit/sec$ O–QPSK (table 1.1). This modulation can also be understood as a frequency modulation where the carrier frequency experiences changes of $500kHz$ [24]. Therefore, in this case the minimum required bandwidth is set by the modulation requirement to $500kHz$.
For what concern BW_{MAX}, it has to be noticed that increasing the bandwidth makes the design more robust, but requires to carefully design the loop building–blocks in order to have a stable system[1]. Therefore a reasonable choice is to take a $100kHz$ margin on the $500kHz$ minimum required bandwidth, and to design a synthesizer with a $600kHz$ bandwidth.

In–band noise requirements

Once chosen the bandwidth, the in band noise plateau depends on the minimum transmitted power and on the signal–to–noise ratio in transmission as follows:

$$PN_{plateau} = P_{TX,min} - 10Log_{10}BW - SNR_{TX} - Margin \tag{4.1}$$

The SNR_{TX} can be derived from the error vector magnitude (EVM) [25]:

$$SNR_{TX}(dB) = 10Log\frac{2}{EVM^2} \tag{4.2}$$

Since the maximum EVM indicated by the ZigBee standard is equal to 35%, and the minimum transmitted power is $-3dBm$, taking a $10dB$ margin, the in band noise plateau has to be lower than $-83dBc$.

Out–of–band noise requirements

As seen in section 3.1.4, the hardest constraint on the out–of–band phase noise is set by the TX U.S. regulatory, and it is equal to $-103dBc/Hz$ at $3.5MHz$ offset from the carrier.

4.1.1 Transmitter specs

Figure 4.1 and table 4.1 resume the phase noise target derived from the standard. Since the in–band–requirement is more relaxed than the cornerone, it has been chosen to introduce a great margin in order to use a first order frequency synthesizer.

[1] Notice that in general when a type I [16] loop is used there is only one pole in the open loop gain (G_{LOOP}) and the system is intrinsically stable.

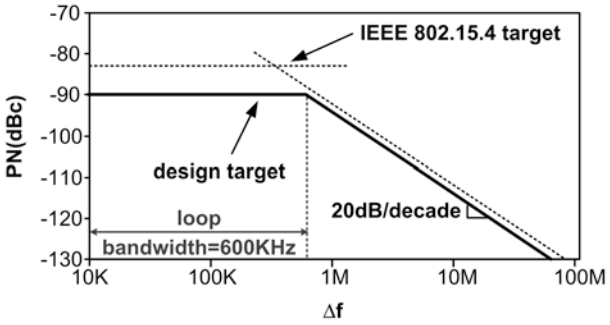

Figure 4.1: Phase noise target.

Design parameter	IEEE 802.15.4 target	Chosen design target
Loop Bandwidth (f_{BW})	$500kHz$	$600kHz$
In band noise	$-83dBc$	$-90dBc$
Noise at corner (at f_{BW})	$-87dBc$	$-90dBc$
Out of band noise slope	$---$	$-20dB/dec$

Table 4.1: ZigBee frequency synthesizer specs

4.1.2 Choice between analog and digital implementation

Once derived the target specs for the transmitter, the choice between analog and digital design can be taken. In fact, even if a proper analog design can reach better performance, its digital counterpart introduces an advantage in terms of area occupation, robustness and programmability [26]. A digital system is more robust respect to the noise injected in the loop and it allows to implement various self–calibration and non–idealities correction algorithms. Moreover the digital design can be synthesized with automatic tools, it is easily portable to a new technology and takes practically only advantages from technology down–scaling, being fully compatible with voltage supply reduction.
From these considerations, the digital design seems to be the better solution when level of performance similar to the ones in table 4.1 are required and area/cost minimization is most severely constrained.

4.2 An introduction to all digital frequency synthesizers

At the state of the art, some all digital frequency synthesizers have been proposed ([27]-[30]). A frequency synthesizer can be a frequency or a phase control loop (FLL or PLL), as shown in figure 4.2.

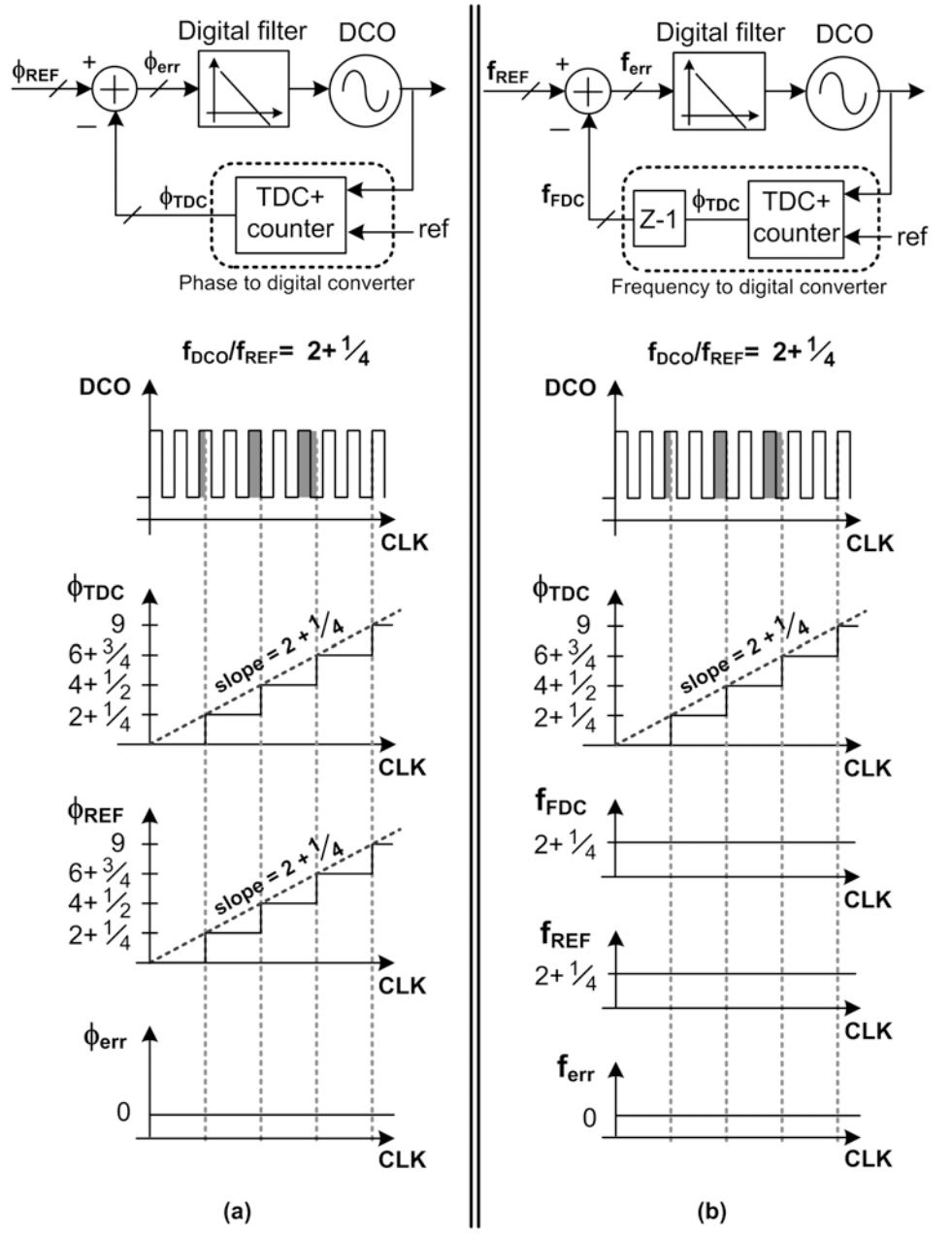

Figure 4.2: Block diagram and signals in a (a) phase and (b) frequency control loop.

Both loops are closed in the digital domain, and they only differs for the presence of the derivation block in the feedback path. The resulting closed loop transfer functions are:

$$H(s)_{CL-PLL} = \frac{H_F(s)\frac{K_{DCO}}{s}}{1 + K_{TDC}H_F(s)\frac{K_{DCO}}{s}} \tag{4.3}$$

$$H(s)_{CL-FLL} = \frac{K_{DCO}H_F(s)}{1 + K_{TDC}K_{DCO}H_F(s)} \tag{4.4}$$

where $H_F(s)$ is the filter tranfer function. Choosing a pure integrator digital filter, the PLL is a type II loop, while the FLL is a type I loop [31]. Thus in the PLL the phase error is null, while in the FLL it is a constant. Nevertheless, since frequency is the derivative of phase, in the FLL the frequency error is zero (see figure 4.2). Since IEEE 802.15.4 requires a constant envelope frequency modulation, a constant phase error can be accepted for the application of interest, and thus a frequency–locked–loop will be designed.

4.3 ADFLL building–blocks design

As shown in figure 4.2.b, an ADFLL is built up by a time to digital converter with a differentiator, a digital filter and a digitally controlled oscillator (DCO). In this section an introduction on the ADFLL building blocks working is given, together with the design details.

4.3.1 The time to digital converter (TDC)

A time to digital converter (TDC) is an analog–to–digital converter, with two analog input frequencies (the local oscillator (f_{DCO}) and the reference frequency (f_{REF})), and an output digital word. Since the output digital word is proportional to the phase difference between the input signals, a derivative operation is needed to translate the phase difference in the frequency domain. This derivative operation transform the time to digital converter into a frequency to digital converter (FDC). The FDC function is to determine at each reference clock cycle the number (N) of DCO periods that are contained in the reference clock itself. In an integer–N frequency synthesizer this number is an integer, an therefore the TDC is in fact simply a counter. Nevertheless this solution suffers from a number of drawbacks [16], which can be overcome by using a fractional–N architecture. As the name says, in this case N has an integer and a fractional part, and the required TDC is built by two different

blocks.
The first one is an integer counter, and it has to count the number of DCO transitions in a reference period. The second one is the real time–to–digital–converter, whose quantization step has to be such that it satisfies the in–band noise–requirements, as it will be shown. The integer and the fractional part have to be synchronized and combined with each others, in order to have the fractional output at each reference clock cycle.

TDC integer part

The integer part of the TDC is basically a counter, which counts the DCO edges and is reset at every reference clock cycle. Its working frequency is the highest f_{DCO} while its dynamic range is equal to the maximum DCO frequency divided by the reference frequency. With $f_{REF} = 27MHz$, and a maximum DCO frequency of about $2.5GHz$, the counter dynamic range is 93, which requires a 7 bits resolution. Since the counter must be read at every reference cycle and then reset before the next reference transition occurs, it has been implemented using two counters [26] as shown in figure 4.3.

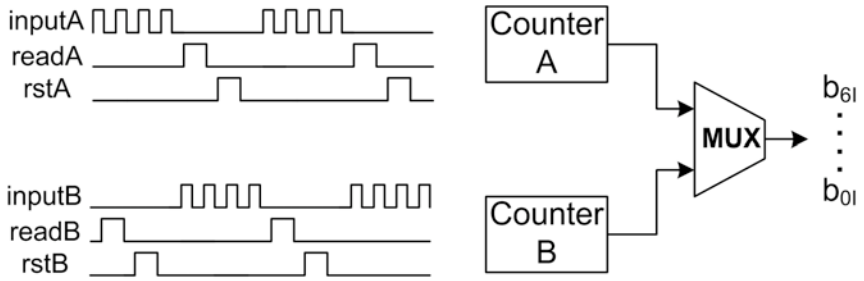

Figure 4.3: Integer counters timing.

During each reference cycle, one counter works, while the other is stopped and its content is loaded, and vice versa in the following cycle. The outputs of the two counters are then multiplexed.
All the input and synchronization signals of the two counters are generated by a specific synchronization block that is also in charge of keeping the consistency between fractional and integer part of the TDC. Despite the very high frequency of operation, this block can be automatically synthesized and routed with the standard digital flow tools [26].

TDC fractional part

The traditional topology of a time–to–digital converter, is reported in figure 4.4.

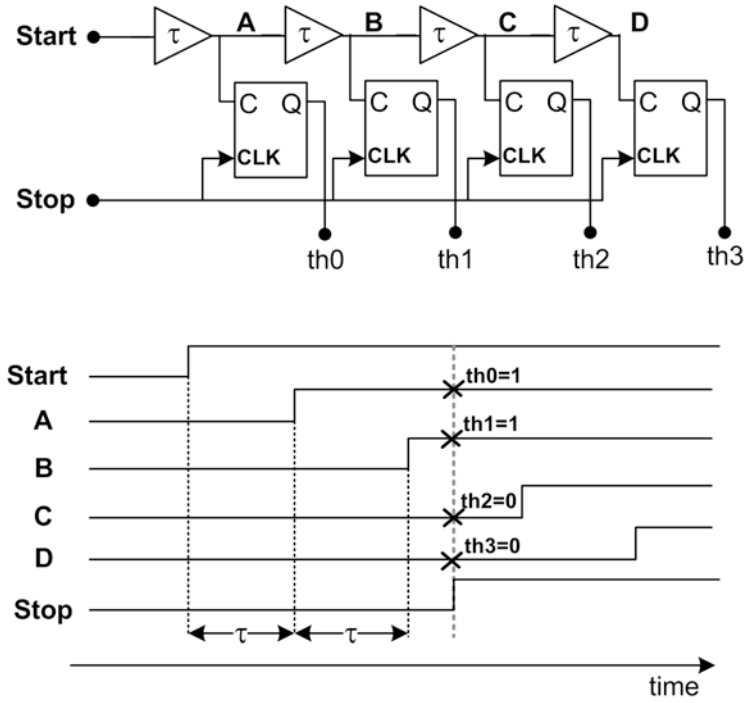

Figure 4.4: Fractional TDC: circuit and transient signals

The output of the TDC is a thermometric word (th0, th1, th2, th3, in the example in figure 4.4) which represents a digital fractional phase and which is determined by passing the DCO clock through a chain of delay elements. The delayed DCO clock is sampled by the reference clock. The number of delay elements sets the TDC resolution (Δt_{res}), and therefore the ADFLL in band noise. In particular the in band phase noise can be expressed as follows [32]:

$$PN = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{res}}{T_{LO}}\right)^2 \frac{1}{f_{REF}} \tag{4.5}$$

To have a phase noise of $-90dBc/Hz$, with f_{DCO} equal to $2.5GHz$ and $f_{REF} = 27MHz$, the required time resolution is about $36ps$. With a maximum oscillator frequency of $2.5GHz$, the required number of delay taps is 11. The digital signal at the output of the fractional TDC is a thermometric code, which has to be converted in a binary one in order to combine it with the output of the integer counter. The number of binary bits needed to perform the

conversion of 11 thermometric bits is 4, which in reality enables to perform the conversion of a 16 bits thermometric code. Therefore the in band noise plateau can be lowered at low cost, using a chain of 16 inverters which introduce 25ps delay each. Nevertheless this delay is not controlled and it can vary as much as $\pm 50\%$ under PVT conditions causing large TDC gain variation. Moreover, the ADFLL in band noise is dominated by the TDC quantization noise, which is proportional to the minimum quantization step. If the delay is higher than expected, the overall in band noise increases, and this can compromise the proper working of the communication system once the ADFLL is used as a direct modulation transmitter. On the contrary if the unit delay is lower than expected, the 16 elements delay chain does not cover the whole DCO period, resulting in an error in the TDC detection. To avoid this problem controllable delay elements should be used in this architecture.

TDC fractional and integer part combination

The output of the integer counter and of the fractional TDC has to be combined at each reference clock, in order to obtain the frequency error (the phase error is zero). This operation requires to perfectly synchronize the two contributors, since an eventual skew can introduce an error, as depicted in figure 4.5.

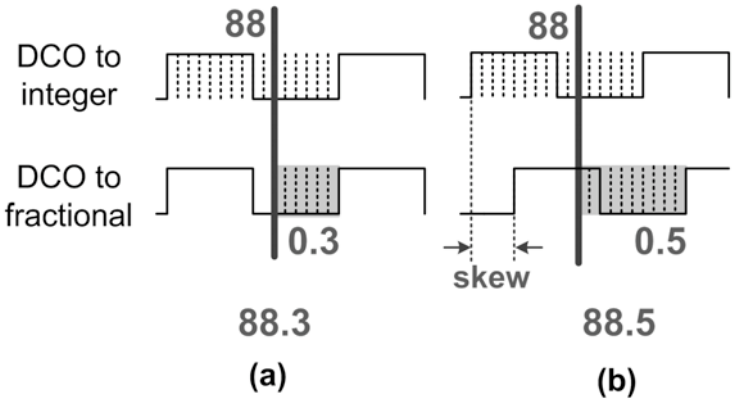

Figure 4.5: Integer and fractional components (a) without skew (b) with skew.

A skew difference between the clocks in the two blocks can cause an error which degrades the in band phase noise performance. Therefore two input synchronization flip–flops are used, in order to synchronize the integer and fractional results (figure 4.6). This solution is sensitive to eventual flip–flops mismatches. Nevertheless this problem can be overcome with a careful layout,

since the skew introduces errors only if it is higher than the minimum delay detectable by the fractional TDC. In figure 4.6 a simplified schematic of the complete TDC functional block is proposed together with its synchronization circuit.

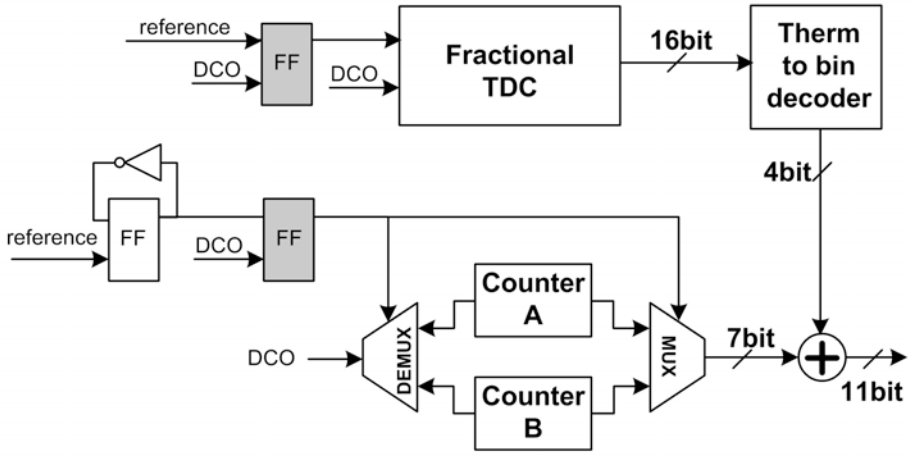

Figure 4.6: Simplified block diagram of fractional and integer TDC with the synchronization circuit.

The maximum error when the DCO and reference clock come at the same time is one LSB of the fractional TDC.

The outputs of the fractional and integer TDC are combined in the frequency domain. The integer counter output is a digital word which indicates a frequency ratio and can be used in the combination process with no more manipulations. On the contrary, since the output of the fractional TDC expresses a phase difference it needs to be differentiated. At each reference clock, the new fractional TDC output is obtained by adding to the present value, the value calculated during the previous cycle changed in sign and augmented by one ($out_{TDCf} = out(T_n) - out(T_{n-1}) + 1$). In order to obtain a proper combination with the integer part, the fractional TDC output has to be written using 5 bits instead of 4, where the fifth one is just a flag which indicates if the fractional number is positive or negative.
The 4 significant bits have to be divided for the number of delay taps in the fractional TDC delay chain. Since the taps are 16, the division can be simply performed using a shift register. After this, the sign bit is inverted and subtracted to the 7 bit integer part. Thus, the complete output of the TDC is an 11 bit word, where the less significant bits are the 4 fractional bits, while

the most significant bits are the integer counter output or the integer counter output minus one, depending on the fractional part sign. This combination algorithm is also resumed in figure 4.7.

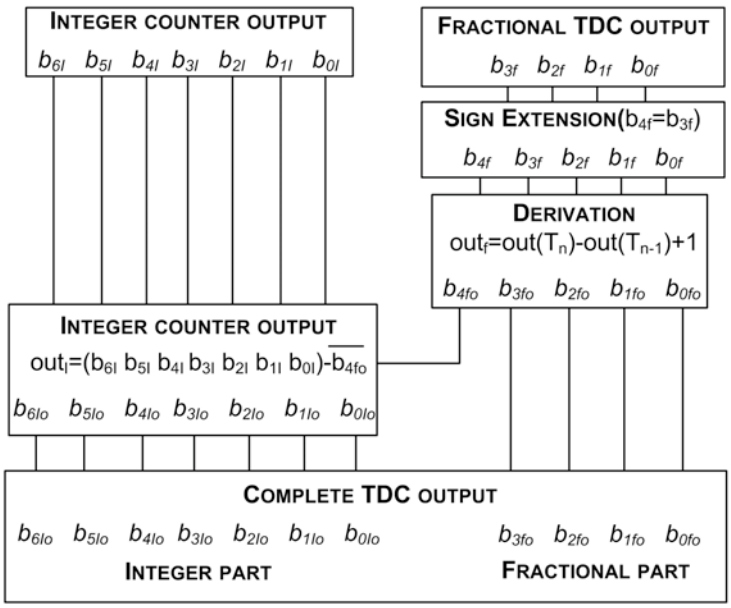

Figure 4.7: Integer counter and fractional TDC outputs combination algorithm.

The complete integer and fractional TDC has been synthesized in a 90 nm CMOS technology. The resulting power consumption is about $1.14mW$. Nevertheless, since the design is completely digital, using a $45nm$ technology the power consumption is expected to halve.

4.3.2 The digitally controlled oscillator

A digitally controlled oscillator is a mixed signal block, which has N input bits and two analog outputs (i.e. the differential LO signals). Since the frequency synthesizer is shared between the RX and TX signal paths, the implemented DCO has the structure of a differential LC tank oscillator, which is a part of the quadrature LMV cell used in the receiver (figure 4.8).

Therefore the DCO design consist on the design of the digitally programmable capacitance which replaces the original voltage controlled varactor in the LC tank. This capacitance is in fact an array, which sets both the DCO tuning range (Δf_{MAX}) and its frequency resolution (Δf_{min}).
The minimum tuning range to cover the ZigBee band, is $86MHz$ around $2.43GHz$. Since some margin is required, in order to consider the PVT vari-

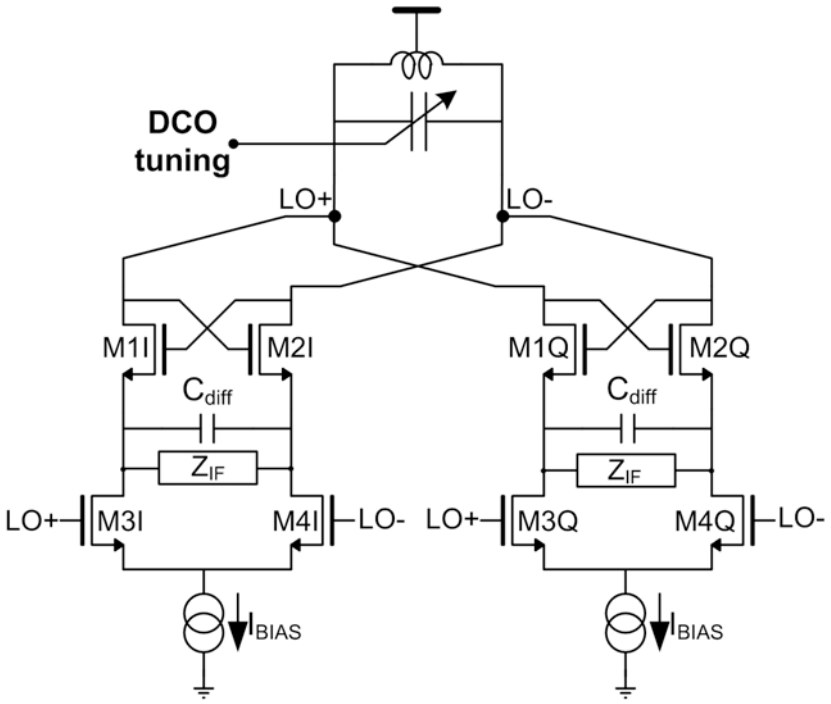

Figure 4.8: LMV core shared between the RX and TX.

ation, the tuning range target is about $200MHz$.
The frequency resolution has to be compatible with the modulation requirement and has to satisfy the out–of–band phase noise and the frequency tolerance targets. The modulation requirement (table 1.1), sets the frequency resolution to $500KHz$ [11], while the out–of–band noise target requires$\Delta\ f_{min} = 342KHz$. This value can be obtained using the following expression [32]:

$$PN(\Delta f) = \frac{1}{12}\Big(\frac{\Delta f_{res}}{\Delta f}\Big)^2 \frac{1}{f_{REF}}\Big(sinc\frac{\Delta f}{f_{ref}}\Big)^2 \tag{4.6}$$

with$\Delta\ f = 600kHz$, $f_{REF} = 27MHz$ and a phase noise at $600kHz$ from the carrier equal to $-90dBm$.
The most severe constraint derives therefore on the frequency tolerance, which is $\pm 40ppm$, corresponding to $98KHz$ for the $2.45GHz$ frequency band.
The digital word which controls the tank capacitance is formed by 13 bits, divided in coarse (5 bits) and fine (8 bits) tuning sections. The first one is used to compensate process and temperature variations, and it covers about $200MHz$ band with a frequency resolution of $10MHz$, while the second one is required for the DCO modulation and covers a $15MHz$ band with a frequency

resolution of $98KHz$.

Coarse tuning

The coarse tuning is obtained using a binary weighted bank (figure 4.9) of varactors in the LC tank, formed by 31 fixed MOM capacitors.

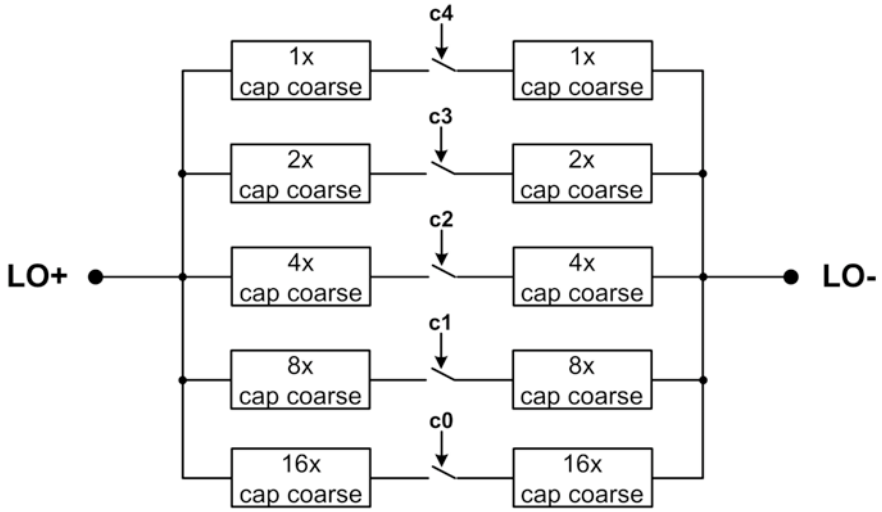

Figure 4.9: Coarse tuning binary weighted bank of capacitors.

The designed elementary cell is depicted in figure 4.10.a. This design, respect to the one reported in figure 4.10.b, minimizes the parasitic capacitance when the switch is off, while halving the parasitic R_{on} when the switch is on. Therefore this implementation reduces the degradation of the capacitors quality factor.

The elementary structure in figure 4.10.a, is dimensioned to obtain the desired $10MHz$ resolution, when a $3nH$ inductor is used in an LC tank which resonates at $2.45GHz$. From (4.7):

$$\Delta f = -f\frac{\Delta C}{2C} \tag{4.7}$$

the requiredΔ $C_{coarse-min}$ can be derived, resulting to be $7fF$. The designed elementary structure synthesizes a $1.5fF$ parasitic capacitor when the switch is open, and a total capacitance of $8.5fF$ when it is closed, producing the neededΔ $C_{coarse-min}$ equal to $7fF$. Introducing this capacitance in the binary weighted array in figure 4.9, a maximum capacitance variation of

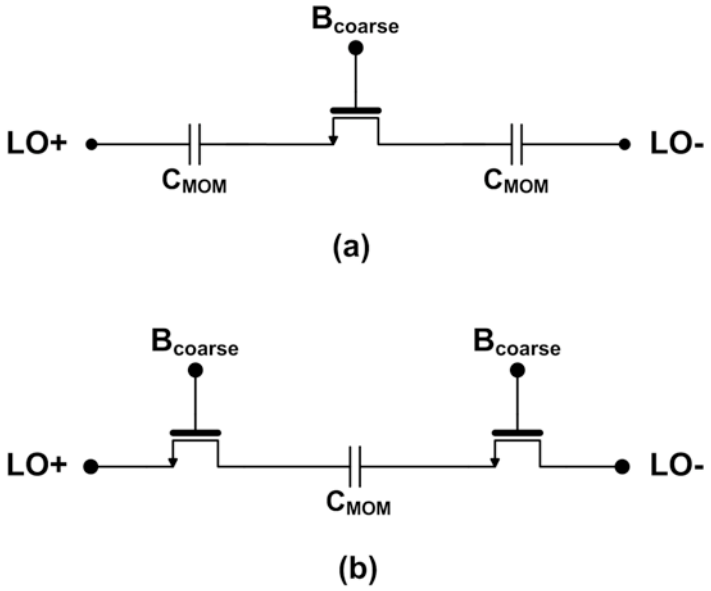

Figure 4.10: (a) Single switch and (b) double switch implementation of the elementary varactor.

$224fF$ is obtained, producing a maximum tuning range of $196MHz$.

Fine tuning

The design of the fine tuning bank introduces some more concern. In fact, replacing in (4.7) the proper values, to obtain the required $98KHz$ resolution a $\Delta C_{fine-min}$ of about $110aF$ is needed. Such a smallΔ $C_{fine-min}$ can be obtained only using a MOS varactor in the LC tank [32]. As shown in figure 4.11.a, the control voltage of this varactor might be the bias across the substrate and the shorted source–drain, while the oscillation appears across the gate and the shorted source–drain itself [33]. Since V_{gs} changes strongly with time, the istantaneous capacitance synthesized by the varactor changes too, as shown in figure 4.11.b.

To overcome this issue and to obtain the desired frequency resolution, a different design approach has been chosen [34]. The idea is to move the fine–tuning array from the drain to the source of the oscillator switching pairs, exploiting the capacitances C_{diff}, which sustains the oscillation in the LMV cell (as reminded in figure 4.8). In order to design the DCO, the LMV cell can be simplified as reported in figure 4.12, where transistors M3–M4 are replaced

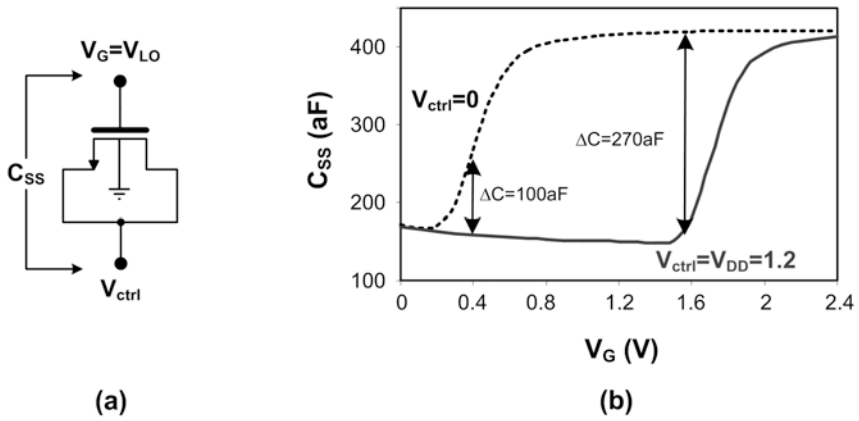

Figure 4.11: (a) MOS varactor and (b) its small signal capacitance.

with bias current generators.

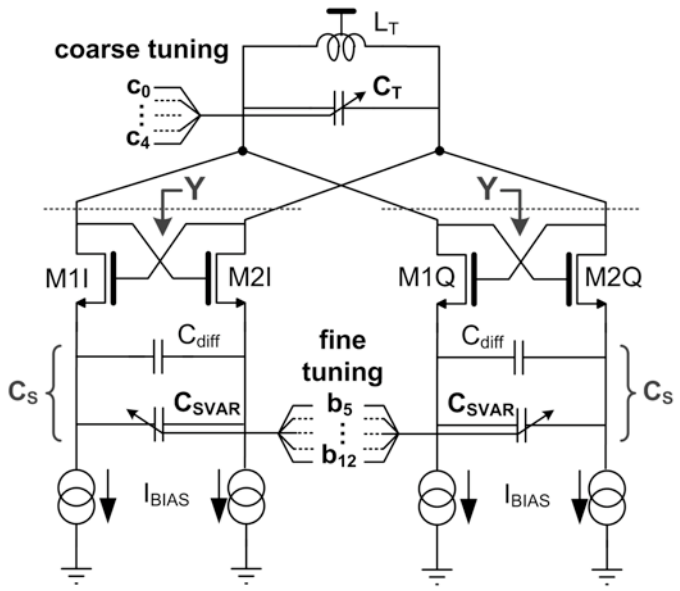

Figure 4.12: Capacitive degeneration tuning scheme.

As seen in chapter 2, the capacitive degeneration modifies the admittance seen at M1–M2 drains, introducing an imaginary term in parallel with the negative resistance. In order to guarantee the oscillation, the capacitance C_{diff} has to satisfy the condition in (2.2). Therefore the total capacitance at M1 and M2 sources (C_S), is formed by a fixed capacitance which sustains the oscillation (C_{diff}), and by a variable one which realizes the fine tuning

(C_{SVAR}). The overall capacitance (C_S) in the two paths is reflected in parallel to the LC tank, reduced by a factor which is proportional to the square of the transistors transconductance. For $g_m << 2\omega_0 C_S$, where ω_0 is the differential LC tank frequency when C_S tends to infinity, the admittance Y in figure 4.12 is:

$$Y = -\frac{gm^2}{2} - j\omega_0 C_S \frac{gm^2}{(2\omega_0 C_S)^2} \tag{4.8}$$

where $-g_m^2/(2\omega_0 C_S)^2$ is the capacitive shrinking factor [34]. As an example, assuming a $gm = 10mS$, $C_S = 5pF$ and $f_0 = 2.4GHz$, the capacitor shrinking factor is about 220. This means that switching on a capacitor of $22fF$ at the sources of M1–M2 produces the same effect produced switching on an capacitor of $100aF$ in parallel to the oscillator tank.
Exploiting this effect, the resonance frequency, which depends on the LC tank and also on the capacitance C_S reflected at the tank itself, can be written as follows:

$$\omega_{LO} = \frac{\omega_0}{2}\sqrt{2 - \frac{gm^2}{2C_S^2\omega_0^2} + \frac{gm^2 L_T}{2C_S} + \sqrt{\frac{4gm^2}{C_S^2\omega_0} + \left(2 - \frac{gm^2}{2C_S^2\omega_0^2} + \frac{gm^2 L_T}{2C_S}\right)^2}} \tag{4.9}$$

From theory and simulation, the circuit in figure 4.12, with $C_{diff} = 800fF$, $gm = 8mS$, $f_0 = 2.41GHz$ and $L_T = 3nH$, produces a $16MHz$ tuning range when C_{SVAR} changes from 0 to $500fF$.

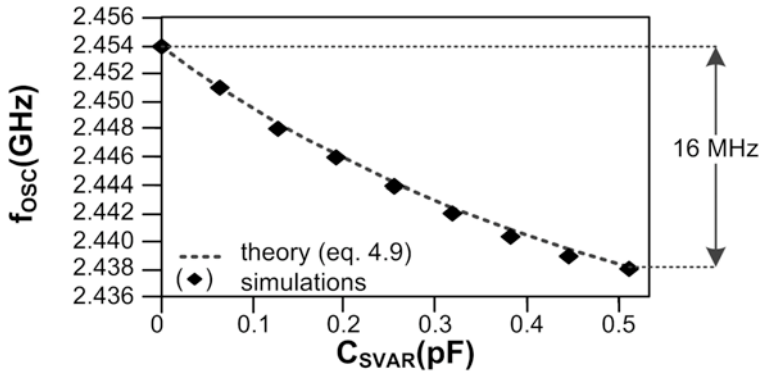

Figure 4.13: Fine tuning range (theory and simulations).

TheΔ $C_{fine-min}$ required to obtain the desired frequency resolution of $98KHz$ is about $2fF$, and can be synthesized using the structure in figure 4.10. In this case the dimensioned elementary structure introduces a parasitic capacitance of $800aF$, while synthesizing a $2.8fF$ capacitance when the switch

is on.
Therefore, the designed DCO assures a tuning range of over $200MHz$ around $2.45GHz$, with a minimum frequency resolution of $98KHz$. The simulated LO amplitude is $1.1V$, and it is obtained with a current consumption of $2mA$.

4.3.3 The digital filter

The first step towards the design of the digital filter is to chose between a finite impulse response (FIR) and an infinite impulse response (IIR). To make the FLL a type I loop, the loop filter has to introduce a pole in the s–plane origin. Therefore, an IIR filter is required, since a FIR filter has all its poles in the z–domain axis origin.
To obtain an IIR filter, two design methods can be followed: indirect synthesis and direct digital synthesis. The indirect synthesis starts from the specifications in the analog domain. In this case the transfer function of the desired filter is derived in the s–domain and then translated in the z–domain using a transformation method (such as derivative approximation or impulse invariance or bilinear transformation). The second design method consists on the direct digital synthesis, and it starts from the specifications in the digital domain. Since the specs we have are in the analog domain, the indirect synthesis method is preferred.
The filter to design is a pure integrator (A_0/s), which makes the FLL a type I loop, assuring that no frequency errors can occur. In the s–domain the closed loop transfer function of the FLL with an integrator becomes:

$$H(s)_{CL-FLL} = \frac{A_0 K_{DCO}}{s + A_0 K_{TDC} K_{DCO}} \tag{4.10}$$

To determine the needed A_0, we have to know the closed loop bandwidth and the value of the product $K_{DCO}K_{TDC}$. The closed loop bandwidth has to be at least $600KHz$, as derived from the standard requirements, while the gain from the DCO input to the TDC output is now discussed. The DCO gain (K_{DCO}) required by the standard is $98kHz/LSB$. The TDC gain (K_{TDC}) can be derived from the TDC time resolution$\Delta\ t_{res}$, which is about $25ps$ for a 16 taps TDC which works with a $f_{DCO} = 2.5GHz$.

The frequency resolution at the TDC output (Δf_{resTDC}) can be expressed as follows:

$$\Delta f_{resTDC} = \left| f_{REF} - \frac{1}{T_{REF} + \Delta t_{res}} \right| \tag{4.11}$$

With a crystal oscillator reference frequency (f_{REF}) equal to $27MHz$, and $\Delta t_{res} = 25ps$, the frequency resolution at the TDC output is about $18KHz/LSB$. Therefore the resulting K_{TDC} is about $55\mu s/LSB$.

Since $K_{DCO}K_{TDC}$ is about 5.4, the required A_0 in the integrator is $700k$. Therefore the analog transfer function of the needed loop filter is:

$$H_F(s) = \frac{700k}{s} \tag{4.12}$$

The corresponding digital filter transfer function can be obtained choosing a proper discretization method [35] [36]. Besides the derivative approximation technique and the impulse invariant transformation, the most common method to transform the analog transfer function in the digital domain is the bilinear transformation technique [35] [36]. This technique allows to obtain H(z) from H(s) simply with the following transformation:

$$s \rightarrow \frac{2}{T}\frac{z-1}{z+1} \tag{4.13}$$

Through this transformation the points in the half–plane $Re(s) < 0$ are mapped into the internal points of the unity circle, while the points in the half–plane $Re(s) > 0$ corresponds to the ones external, as shown in figure 4.14.

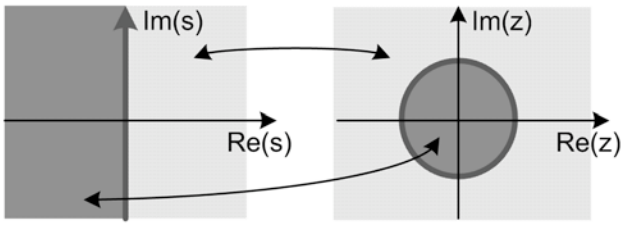

Figure 4.14: Points mapping (s–plane to z–plane) due to the bilinear transformation.

If H(s) is a stable causal system, whose poles are in the left half–plane, H(z) too is a causal stable system. Without focusing on the details of bilinear transformation, which can be found in [35] [36], using this technique the discrete filter transfer function becomes:

$$H_F(z) = \frac{A_0 T_{REF}}{2}\frac{1+z^{-1}}{1-z^{-1}} = 0.013\frac{1+z^{-1}}{1-z^{-1}} \tag{4.14}$$

This transfer function can be implemented using the circuit in figure 4.15.

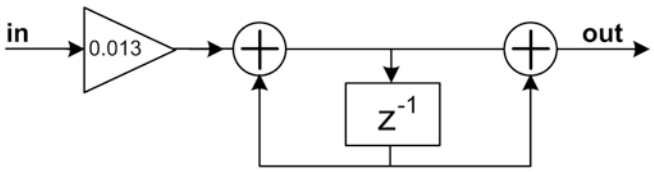

Figure 4.15: IIR digital filter block diagram.

The coefficient 0.013 can be implemented as the sum of $2^{-7} + 2^{-8} + 2^{-9}$, simplifying the circuit. The designed filter has to be described in VHDL and it has to be synthesized.

4.3.4 Designed FLL transfer functions

For sake of completeness, the open loop and the closed loop FLL transfer functions are:

$$\begin{aligned} H_{OL-FLL}(s) = & \quad \frac{A_0}{s} K_{DCO} = \frac{68.6 \cdot 10^9}{s} \\ H_{CL-FLL}(s) = & \quad \frac{A_0 K_{DCO}}{s + A_0 K_{DCO} K_{TDC}} = \frac{68.6 \cdot 10^9}{s + 600 \cdot 10^3} \end{aligned} \tag{4.15}$$

The open loop and closed loop gain are reported in figure 4.16.

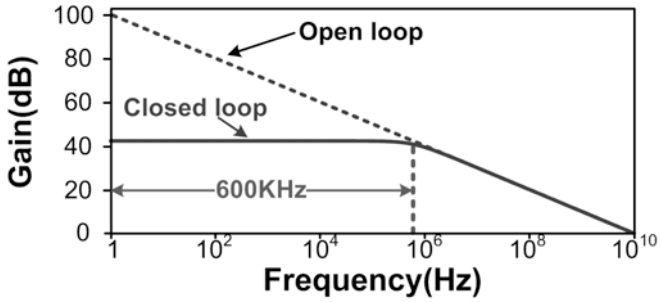

Figure 4.16: Open loop and closed loop gain of the designed FLL.

4.4 Power amplification

Besides frequency modulation, the transmitter has to perform power amplification, in order to send to the antenna a modulated signal with an adequate power, as required by the ZigBee standard. The IEEE 802.15.4 typical transmitted power is $0dBm$, but transmitted power between $-3dBm$ and $10dBm$

are accepted. This power range takes account of a trade–off between the transmitter output power and the receiver sensitivity, which can be expressed by the following equation:

$$P_{RX}(d) = \frac{P_{TX}\lambda^2}{(4\pi d)^2} \tag{4.16}$$

In (4.16) the received power (P_{RX}) is expressed as a function of the transmitted one (P_{TX}) and of the distance between the transmitter and the receiver, when the antenna gains are unitary and the signal propagates in free–space. With a minimum P_{RX} of $-85dBm$ and a noise figure of $20dB$, a ZigBee transceiver can work properly in free space if the distance between the transmitter and the receiver is in the range of $120 - 550$ meters, depending on the transmitted power. This distance drops off with propagation in air and through obstacles (such as e.g. walls). In order to design a robust transceiver, able to work also in environments where the transmitted signal is strongly attenuated, the chosen target for the PA is to obtain a $0 - 5dBm$ output power with the highest efficiency.
When the output power is in this kind of range, designing an efficient transmitter becomes increasingly difficult, since with typical supply voltages of $1 - 3V$ and an antenna impedance of roughly 50Ω, standard power–amplifier topologies becomes quite inefficient when they are required to deliver such a low output power. Therefore in this case an interesting solution seems to be the use of a power oscillator.

4.4.1 Power oscillator analysis

A transmission chain can be modeled as the cascade of two stages, as shown in figure 4.17 [37]: a PA–stage, which is the section loaded by the antenna, and a pre–PA–stage, which performs modulation and up–conversion.

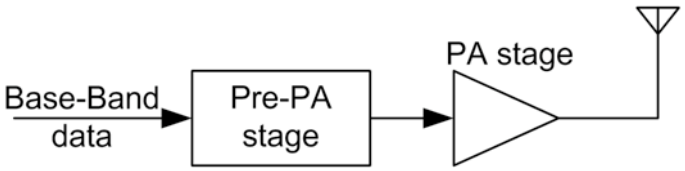

Figure 4.17: Transmitter stages.

In cellular and WLAN applications, the power delivered to the antenna by the PA is much higher than the pre–PA power and the transmitter efficiency is

mainly determined by the PA efficiency itself. On the other hand, in wireless sensor networks applications typical radiated powers are in the order of $1mW$, and the pre–PA power dissipation is usually comparable or higher than the radiated power. For these applications, it is worth to investigate a simple solution which does not use a traditional PA to transfer power to the antenna. This solution directly transfer to the antenna the modulated LO signal, using the power oscillator in figure 4.18. In this circuit the core is the designed DCO and a parallel resistance R_T is added in the LC tank in order to model its finite quality factor.

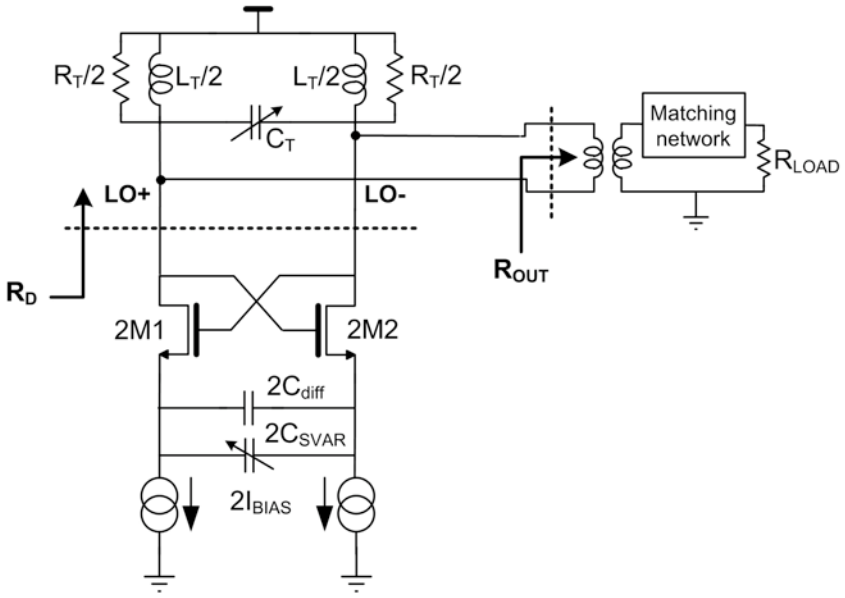

Figure 4.18: Power oscillator.

In this case the modulated local oscillator signal is the one to be delivered to the antenna. The amplitude of this signal depends on the total bias current flowing in the LC tank ($I_{BIAStot}$), and on the total resistance at the drain of transistors M1–M2 (R_D):

$$V_{LO} = \frac{2}{\pi} I_{BIAStot} R_D \tag{4.17}$$

The output power delivered to the antenna, can be therefore expressed as:

$$P_{OUT} = \frac{V_{LO}^2}{2R_{OUT}} = \frac{\left(\frac{2}{\pi} I_{BIAStot} R_D\right)^2}{2R_{OUT}} \tag{4.18}$$

To maximize the output power, once chosen the bias current, it is necessary to properly chose the resistance R_{OUT}, which impacts also on the total drain resistance R_D. In fact, (4.18) can be rewritten as follows:

$$P_{OUT} = \frac{\left(\frac{2}{\pi} I_{BIAStot} \frac{R_T R_{OUT}}{R_T + R_{OUT}}\right)^2}{2R_{OUT}} \tag{4.19}$$

This output power is maximized when R_{OUT} is equal to R_T (whose value is given by $\omega_{LO} L_T Q_T$). Choosing a proper matching network it is possible to increase the 50Ω impedance of the antenna to the desired value, in order to obtain the maximum output power:

$$P_{OUT,MAX} = \frac{I_{BIAStot}^2 \omega_{LO} L_T Q_T}{2\pi^2} \tag{4.20}$$

Moreover, since the DC power can be expressed as the product of the bias current $I_{BIAStot}$ and the voltage supply V_{DD}, efficiency can be calculated as follows:

$$\eta_{MAX} = \frac{I_{BIAStot} \omega_{LO} L_T Q_T}{2\pi^2 V_{DD}} \tag{4.21}$$

From (4.20) and (4.21), both the output power at RF and the efficiency are proportional to the LC tank inductor value (L_T), to its quality factor (Q_T) and to the bias current ($I_{BIAStot}$). Increasing the L_T value the die area grows, while the capacitance C_T decreases, reducing the tuning range of the oscillator. Nevertheless, with a resonance frequency at $2.45GHz$, an adequate tuning range is obtained with an L_T value up to $6nH$. Therefore the transmitted power and the efficiency of the power oscillator in figure 4.18, are calculated in two different cases: when L_T is equal to $6nH$ and has a quality factor of 16.6, and when L_T is equal to $3nH$ with $Q_T = 18$. The results (theoretical and simulated) are reported in figure 4.19.

As expected, both the transmitted power and the efficiency increase with the bias current and the value of the inductor in the LC tank. Increasing the bias current in the LMV cell would push the current generator in linear region, compromising the proper working of the current mirror. With acceptable bias currents (lower than $4mA$), the obtained efficiency is quite low ($\eta_{MAX} < 25\%$). Another possibility to increase the output power and the efficiency is to use bond–wire inductors in the LC tank, producing high Q_T (theory Vs. simulations in figure 4.20).

Nevertheless, also in this case to obtain quite high efficiencies the required bias current is $5 - 6mA$, which is not feasible for the low–power quadrature

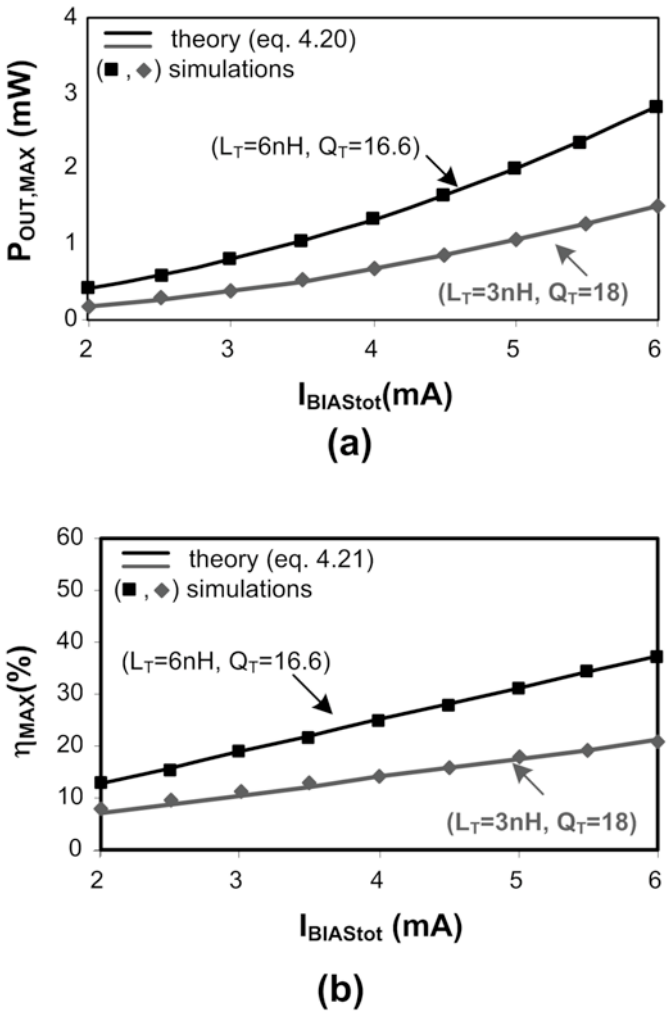

Figure 4.19: (a) Output power and (b) efficiency as a function of $I_{BIAStot}$ for different L_T values ($V_{DD} = 1.2V$ and $f_{LO} = 2.45GHz$).

LMV cell shared with the receiver. Moreover additional losses would be introduced using a real balun to transfer the modulated LO signal to the antenna, reducing furthermore the overall efficiency.
In conclusion, even if it seemed a promising solution, the use of a power oscillator seems not to be suitable for the ZigBee transmitter, since high levels of efficiency are obtained with high levels of bias current.

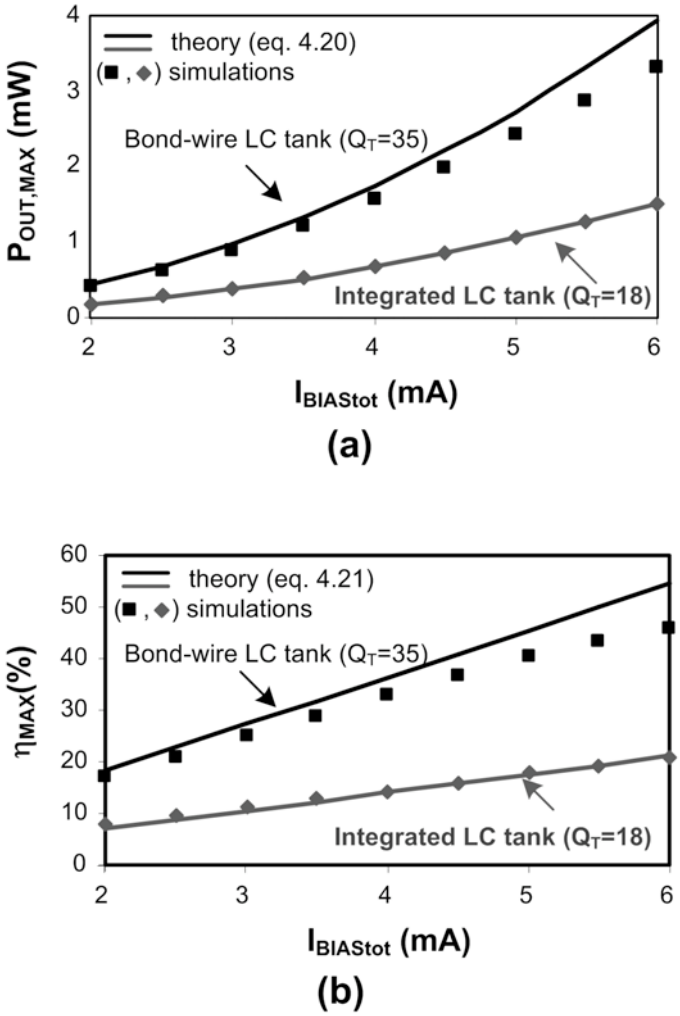

Figure 4.20: (a) Output power and (b) efficiency as a function of $I_{BIAStot}$ for different Q_T values ($V_{DD} = 1.2V$, $L_T = 3nH$ and $f_{LO} = 2.45GHz$).

4.4.2 Traditional PA design approach

Since the modulation scheme uses a constant envelope signal, the PA can be implemented with a nonlinear amplifier, making the higher possible efficiency. To prevent wasting power, the active elements in the PA should be ideal switches, which has not any voltage drop when they are on, and they have a zero current when they are off. Once chosen the PA, its maximum efficiency depends on the load impedance and on the maximum voltage swing at its output [16]:

$$P_{MaxEff} = \frac{v_{0,Max}^2}{2R_L} \tag{4.22}$$

Therefore to design an efficient PA with low output power it is desirable to have a small $v_{0,Max}$ and/or a large R_L.
Since generally the supply voltage depends on the technology, the designer can act on $v_{0,Max}$ only by choosing a proper topology. In figure 4.21, two traditional PA topologies are drawn.

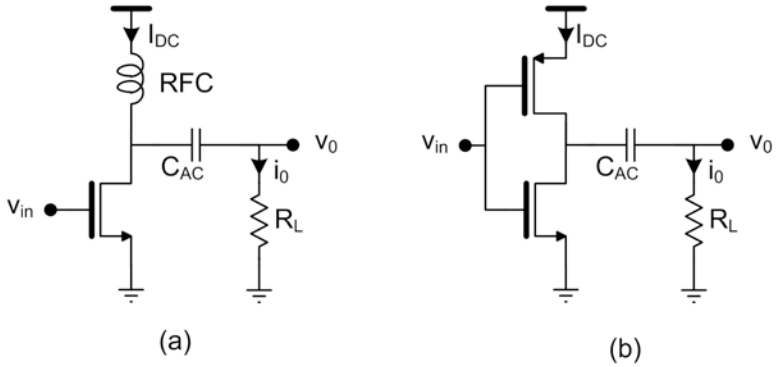

Figure 4.21: (a) RF chocke PA and (b) push–pull PA.

The RF chocke topology can work as a linear or efficient PA depending on the bias current and on the RF signal at the gate of the transistor [16]. If this circuit works in class C, it results:

$$\begin{aligned} v_{0,Max} &= V_{DD} \\ i_{0,Max} &= I_{DC} \\ P_{MaxEff} &= \frac{(V_{DD})^2}{2R_L} \end{aligned}$$

Since the matching network has to be shared with the receiver to reduce costs we have two choices: the first one is to use the antenna to direct load the PA, while the second one is to share the matching network. If the antenna directly loads the PA, when $V_{DD} = 1.2$ and $R_L = 50\Omega$, the output power with maximum efficiency is about $12dBm$, which is too high for ZigBee applications. If the receiver matching network shown in figure 3.8 is shared with the transmitter, it increases the PA output impedance to about 800Ω, resulting in an output power of about $-0.5dBm$. Even if this value is close to the desired range $(0-5dBm)$, the PA in figure 4.21.a requires to use an inductor, increasing the cost of the whole transceiver. On the contrary, choosing the push–pull

topology in figure 4.21.b no integrated or external inductors are required. In this case it results:

$$\begin{aligned} v_{0,Max} &= \frac{V_{DD}}{2} \\ i_{0,Max} &= 2I_{DC} \\ P_{MaxEff} &= \frac{(V_{DD})^2}{8R_L} \end{aligned}$$

Therefore if the output load is 50Ω, the maximum efficiency is reached when the output power is $3.6mW$, i.e. $5.5dBm$, which is next to the design target. To maximize isolation, a driver stage is introduced before the power–amplifier. The amplifier chain designed, has been simulated, showing good performances if compared to the state of the art of PA for low–power applications. All the data in table 4.2 consider the PA and pre–PA isolation stage. Notice that in this case the balun is not required, and a dummy structure is introduced in order to load equally the positive and negative LO outputs.

	[6]	[7]	[8]	**This work (sim)**
Pout (mW)	1	4	0.3	3
$\eta_{PA}\%$	18.5	31.5	45	59.5
$\eta_{PA+VCO}\%$	—	—	21.9	40.3
PA int. coils	1	3	0	0

Table 4.2: ZigBee compliant power amplifiers state of the art

4.4.3 Conclusions

In this chapter a ZigBee compliant transmitter was described. The signal modulation is performed through an ADFLL, while the signal amplification is realized using a push–pull PA. The transmitter building blocks have been designed, but their proper working has been verified only theoretically. To complete the design, some mixed–signal simulation has to be performed, also in order to verify the good working of the whole transceiver.

Conclusions

In this thesis a complete ZigBee transceiver is presented.

The work starts from the study of the IEEE 802.15.4 standard, whose general features are compatible with ZigBee applications, which require to minimize power consumption and cost in order to have efficient and flexible system able to reshape itself dynamically.

After this brief introduction, both the receiver and the transmitter architecture can be chosen in order to satisfy the low–power and low–cost requirements of the standard. Nevertheless this is only the first step towards power and area minimization, and it has to be combined with proper design strategies. At the state of the art, the reduction of costs is related to the minimization of the integrated coils and external components. On the other hand the most promising solution to save power consumption seems to be bias and device sharing. A particularly promising structure was the LMV cell, which maximizes power saving, while maintaining a good flexibility, which can be exploited to optimize the design. This cell was chosen as the starting point for this work, and it was optimized in order to be used in a low–power, low–cost quadrature front–end. Two possible implementations for the complete receiver (which include the front–end plus the base–band) were proposed. They differ in the practical way to obtain signal quadrature and input matching. The choice between the two implementations is related to the noise target and to the quality factor of the available inductors.

The designed receivers were integrated in a $90nm$ CMOS technology. The measurements resulted in performance in line with the state of the art, while consuming a lower current and/or reducing the silicon area.

In the last part the focus is on the transmitter section, where the signal modulation is performed through an ADFLL, while the signal amplification is realized using a push–pull PA. Since ZigBee is time division, the ADFLL is shared with the receiver, where it is used to stabilize the oscillator frequency. The specs to design a ZigBee compliant ADFLL were derived and all the building blocks were designed in the digital domain. Nevertheless an optimization of the design is needed before the complete transceiver integration.

The estimated power consumption of the whole transceiver is about $5.4mW$ in RX mode (considering also the frequency synthesizer) and $9mW$ in TX mode, with a total efficiency of about 30%.

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