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Self-interference Cancellation Techniques for SAW-less Transceivers

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Abstract

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The adoption of mobile wireless communication technologies ranging from GSM to the future 5G radios has continuously required increased data rates and quality of service and, in general, the miniaturization of devices and costs reduction. At this contemporary world, one cannot imagine life without wireless communications. Practically, our mobile smartphones have become our daily companion which are used for different tasks ranging from writing emails, making both voice and video calls, live program streaming, IOT (internet of things) applications, and endless tasks we could not imagine in the past.

The present wireless radios have inevitably off-chip passive components like the SAW filters, Duplexer and high Q filters. These filters are needed to filter out unwanted signals such as large CW (continuous wave) blockers and self-interference signals (or TX leakage) by about 50dB. The fact that recent mobile wireless technologies like LTE and the future 5G propose the adoption of MIMO and carrier aggregation capable of managing multi bands in the system architecture, it implies that the number of antennas, external fixed frequency filters and on-chip building blocks would increase further. Hence, a huge increase in the form factor and cost will result unless some actions are taken.

This thesis proposes two innovative self-interference cancellation(SIC) techniques for transceivers while eliminating the use of external SAW filters/ Duplexers. This dissertation compares active and passive SIC techniques where the passive SIC technique has been fully integrated. The concepts, analysis and results are presented. These approaches specifically suppress self-interference while improving the linearity of the receiver with the benefit of low form factor, reduced cost and relaxed linearity requirements for the front-end building blocks. In the concluding part of the thesis, a control loop algorithm is proposed to optimize IIP2 of LNA (in a duplexer/SAW-less receiver suitable for TV white space applications) during process corners and temperature variations.

To my family members, chiefly to the memory of my father

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Introduction

The adoption of mobile wireless communication technologies ranging from GSM to the future 5G radios has continuously required increased data rates and quality of service and, in general, the miniaturization of devices and costs reduction. At this contemporary world, one cannot imagine life without wireless communications. Practically, our mobile smartphones have become our daily companion which are used for different tasks ranging from writing emails, making both voice and video calls, live program streaming, IOT (internet of things) applications, and endless tasks we could not imagine in the past. The drive for smart cities and drastic reduction of human greenhouse gases emission have been a push for the automotive industry to manufacture electric cars, as most developed countries have started issuing out deadlines for full electric cars utilization. The continuous growth in the demand of increased data rate has led to the evolution of different standards accommodating large number of bands, massive MIMO (Multi input Multi output) and the support of more simultaneous users. For instance, the global mobile data traffic per month is expected to grow to 49 Exabyte per month by 2021, a sevenfold increase over 2016 [1] as shown in Fig. 1. The stringent requirements for high data rates have continued to drive research towards achieving better and improved design specifications. A brief review of the mobile technology evolution will provide an insight towards understanding the research efforts made so far to meet these high data rate demands.

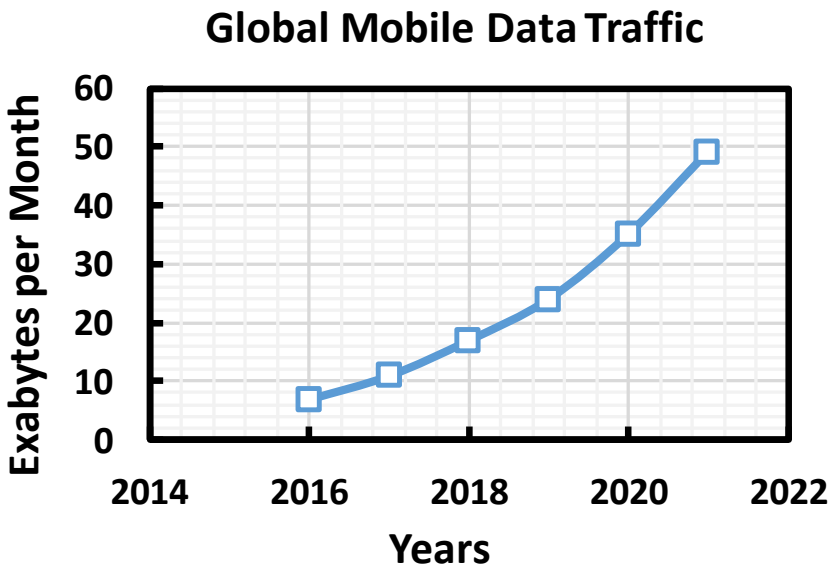

Fig. 1 The global mobile data traffic per month from2016 to 2021 [1]

The early stage of mobile communications sees the evolution of second generation mobile communication technologies, GSM (Global system for Mobile communications). GSM was designed as a circuit-switched system that established a direct and exclusive connection between two users on every interface between all network nodes of the system, with very low data rates. Over time, this physical circuit switching is being virtualized and many network nodes are connected over IP (Internet Protocol)-based broadband connections leading to the evolution of GPRS (General Packet Radio Service). The sending of data in packets gives rise to other applications that work with the internet. These 2G standards use TDMA (Time-Division Multiple Access). Due to the increase in the Internet and IP-based applications, two separate networks: a circuit-switched network for voice calls and a packet-switched network for Internet-based services are being maintained by network operators and this later leads to the evolution of UMTS (Universal Mobile Telecommunications System), which is a third-generation mobile standard. As years roll by, the UMTS radio network system has been considerably improved and now offers broadband speeds. This high-speed enhancement is referred to as High-Speed Packet Access (HSPA) and uses the Code-Division Multiple Access (CDMA).

Based on the number of inherent design limitations of UMTS, the Third Generation Partnership Project (3GPP) released fourth-generation referred to as Long-Term Evolution (LTE). LTE utilizes Orthogonal Frequency Division Multiplexing (OFDM) to transmit data over many narrowband carriers spaced by 180 kHz from each other, that is, a data stream is split into many slower data streams that are transmitted simultaneously. Several bandwidths have been specified for LTE since it is flexible in channelization: ranging from 1.25 MHz up to 20 MHz. In addition to the flexible bandwidth support, all LTE devices have to support Multiple Input Multiple Output (MIMO) transmissions, which allow the base station to transmit several data streams over the same carrier simultaneously. The highest theoretical data rate is 170 Mbit/s in uplink. With MIMO approach, the data rate can reach 300 Mbit/s in the downlink. LTE is designed to be universal since it supports GSM, GPRS, EDGE and UMTS because data sessions can be moved seamlessly between GSM, UTMS and LTE when the user roams in and out of areas covered by different technology standards. According to 3GPP, in the nearest future, the term "5G" is rapidly coming into the limelight and there is already a potential standard path towards the 5G era and this will support full-duplex, massive MIMO, and mm-wave mobile communications.

A complete receiver consists of several blocks both on-chip and off-chip. The most critical in terms of form factor and cost are the off-chip passive components like the external filters such as SAW, Duplexer and high Q filters. These filters are needed to filter out unwanted signals such as large CW (continuous wave) blockers and self-interference signals (or TX leakage) by about 50dB. The fact that recent mobile wireless technologies like LTE and the future 5G propose the adoption of MIMO and carrier aggregation capable of managing multi bands in the system architecture, implies that the number of antennas, external fixed frequency filters and on-chip building blocks would increase further. Hence, a huge increase in the form factor and cost will result unless some actions are taken. In literature, several research efforts have been made towards eliminating these external filters while proposing SAW-less transceiver

architecture. In the TDD (Time division duplexing) standard as shown in Fig. 2 (a) which is typical of 2G systems (GSM), the transceiver transmits for half of the time and receives for the other half while using same frequency band for both TX and RX. The isolation between the TX and RX is provided by the antenna switches and not the SAW and can still accommodate large CW blockers or SI due to the different time of operation. A greater challenge is faced in FDD (Frequency Division Duplexing) mode typical of 3G standards illustrated in Fig. 2 (b), where the TX and RX operate simultaneously in different frequency bands. The external SAW filters perform both TX and RX filtering but the residual self-interference from the TX at the RX input is still critical to the receiver sensitivity evaluation. In an FD (full Duplex) mode for LTE (4G) and the future 5G as shown in Fig. 2 (c), where the TX and RX overlap in time and frequency, a greater challenge will be faced. The in-band performance of the receiver would be worsened due to overlap of the RX and TX frequencies. The present LTE requires enlarged Radio Frequency (RF) signal bandwidths to meet the demand of high speed which however, results in the reduction of the frequency distance between the RX and TX channel. The leakage problem is exacerbated due to the simultaneous operation of the RX and TX.

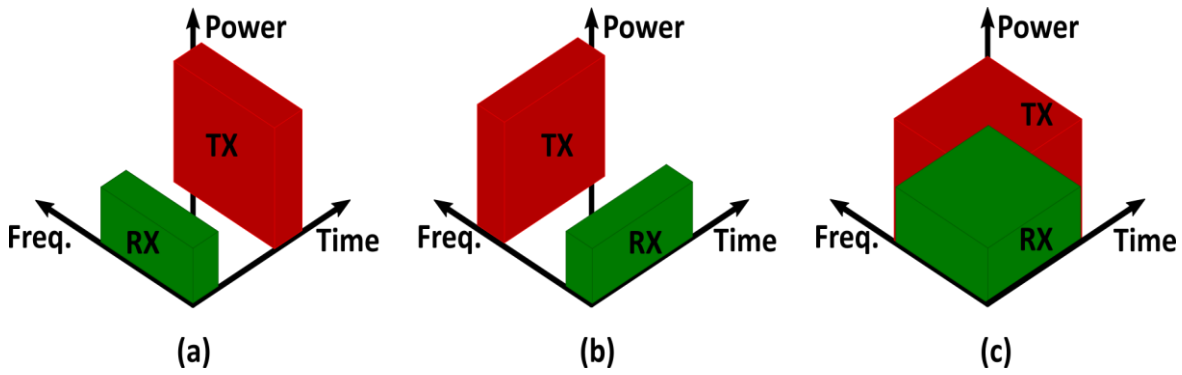

Fig. 2. Transmission and reception channel in (a) Time Division multiplexing (TDD) (b) Frequency Division Multiplexing and (c) Full-Duplex (FD) of a radio

The design challenges in duplexer based systems such as linearity degradation from in-band third order intermodulation and second-order intermodulation distortions

due to intermodulation of leaked TX signal with out of band blockers, as well as distortion from reciprocal mixing and also the wideband TX noise leakage in receiver band are great design nightmare for design engineers and researchers. Moreover, these design challenges are drastically exacerbated in SAW-less transceivers. Several authors have proposed different architectures to substitute the bulky off-chip filters with integrated blocks to mitigate these design challenges while achieving reduced form factor and cost reduction.

The research work presented in this thesis aims to substitute the bulky off-chip passive components with an integrated SIC (Self-Interference Canceller). The research also compares active and passive self-interference cancellation techniques where the passive SIC technique has been fully integrated. Below we describe the organization of the thesis.

Chapter 1 presents background knowledge useful in understanding the fundamentals of modern wireless transceivers. These include transceiver design challenges and that of SAW-less transceivers. Also included is the receiver linearity requirements and the effect of self-interference cancellation in a receiver.

Chapter 2 gives an overview on the recent state of the art techniques for self-interference cancellation in single and dual antenna SAW-less receivers.

In chapter 3, a low-power active self-interference cancellation technique is presented for SAW-less full duplex and frequency division duplex radios. The chapter also describes a concept to improve cross-modulation distortion which are common in active devices. At the end, simulation results are presented to validate the performance of the SIC.

Chapter 4 focuses on self-interference cancellation using passive devices with the goal of achieving low power and low noise contribution to the entire receiver chain. Measurement results are presented to prove the design performance of the system.

Chapter 5 discusses the analyses and design implementation of second order distortion cancellation in a common gate–common source (CG-CS) low noise transconductance amplifier (LNTA) in a direct-conversion receiver. Also presented is a background calibration concept to ensure optimum IIP2 of the LNA with respect to process corners, voltage and temperature variations.

Finally, the dissertation is concluded with a summary of the contributions of this research.

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[1] Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2016–2021 White Paper. Available online: https://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/mobile-white-paper-c11-520862.html (accessed on 12th September, 2017)

Chapter 1

Understanding Modern Wireless Transceivers

The emerging trend in the use of wireless devices such as smartphones, Bluetooth devices and wearable medical devices has continued to drive researches to designing low cost, low power, highly linear and high speed wideband transceivers. A radio frequency (RF) transceiver comprises basically a transmitter (TX), a receiver (RX) and other circuitry that provides efficient transmission and reception between them. The building blocks in a transceiver have been continuously redesigned to meet the present technological evolution, i.e., the scaling of CMOS devices. The basic building blocks of a complete transceiver consist of Low Noise Amplifier (LNA), quadrature down-conversion Mixer, Transimpedance Amplifier(TIA), Automatic Gain Control (AGC), and Analog-to Digital Converter (ADC) on the RX side, Power Amplifier (PA), Up-conversion Mixer and Digital to Analog Converter (DAC) at the TX side, and a PLL which is common between both RX and the TX as shown in Fig. 1.1. There are different transmitter and receiver architectures that have been proposed [1]. The most commonly used in today's receiver is the direct conversion architecture because of its compact building blocks, without the need of image reject filter, which makes it efficient in terms of cost. However, the drawbacks of this architecture such as LO leakage, DC offset, even order distortion and flicker noise can be emeliorated through careful design and layout. A comprehesive description of these effects is in

[1]. With good symmetrical layout of the oscillator and RF signal path, the issue of LO lekage can be minimised.

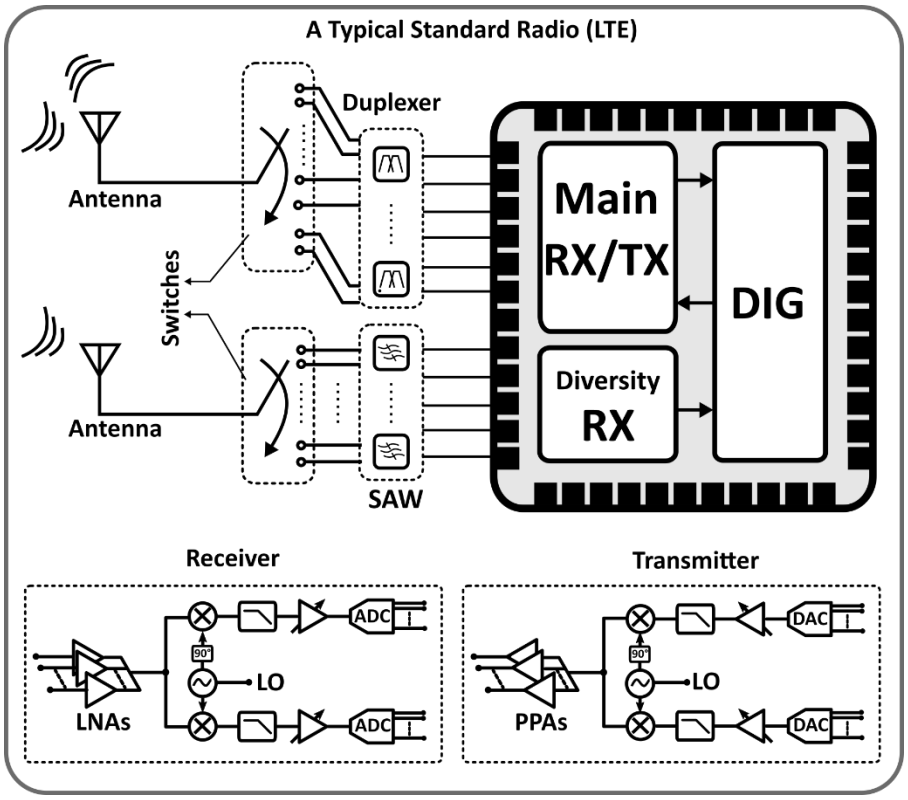

Fig. 1. 1 Block diagram of a multiband Transceiver

1.1 Transceiver Standard and Design Challenges

The LTE represents the most recent standards for wireless communications that was standardized by the 3GPP which was finalised and released first in 2008 [3]. 3GPP defines the performance of both Base Station (BS) and User Equipment (UE) for several network technologies. But for this thesis, the performance parameters to be reviewed are for UE, mainly for the LTE technology. These include sensitivity, bandwidth, blocking profile, linearity and Noise.

1.1.1 Receiver Sensitivity

Since a noisy environment is compounded with different signals (wanted and unwanted), the most vital performance of an RF receiver is to detect the wanted signal from the noisy environment without signal quality degradation. The term used in evaluating this important performance is the receiver sensitivity. The RX sensitivity is defined as the minimum detectable input signal power level with acceptable signal quality by a receiver for a given Output Signal-to-Noise-Ratio (SNR) approved by the 3GPP standard, and can be expressed as in (1).

$$P_{sens} = 10\log_{10}(K_B T \cdot BW) + SNR_{min} + NF, \quad (1)$$

where K_B is the Boltzmann constant, T is the absolute temperature expressed in Kelvin, BW is the channel bandwidth, SNR_{min} is the minimum output signal-to noise ratio of the receiver specified by the wireless communication standard, and NF is the receiver noise figure. In another expression, the receiver sensitivity is also given as $P_{sens} = P_{NoiseFloor} + SNR_{min}$, where $P_{NoiseFloor}$ is the total integrated input referred noise of the receiver determined by the receiver NF and the channel bandwidth and it is expressed as: $P_{NoiseFloor} = -174\frac{dBm}{Hz} + 10\log_{10} BW + NF$.

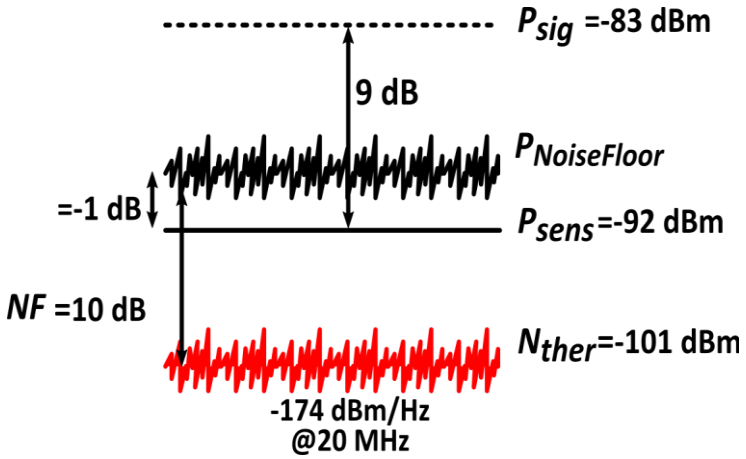

Fig. 1. 2 Illustration of RX sensitivity and thermal noise

During the design analysis of receiver building blocks, the maximum acceptable noise figure of the receiver must be carefully specified based on the standard given by the 3GPP. For instance, when a QPSK (Quadrature Phase Shift Keying) modulation scheme is used with a code rate of 1/3, the SNR is -1dB [4] in order to ensure the required Bit-Error-Rate (BER). For a 20 MHz LTE FDD channel bandwidth (E-UTRA Band 2, with downlink frequency range of 1930-1990 MHz), the required sensitivity level is -92 dBm. From (1), the maximum receiver NF that would still ensure that the receive signal is demodulated with acceptable quality is $NF \leq 174 - 10log_{10}(2 \cdot 10^7) - 92 + 1 = 10\ dB$ as illustrated in Fig. 1.2. However, in today's receiver, a NF of around 4 dB has been proposed [18], [19], where the insertion loss due to the external filters have been excluded.

1.1.2 Receiver Blocking Profile

The blocking characteristics describe the receiver ability to receive a desired signal at its allocated channel in the presence of an interferer, which can either be a signal with bandwidth of 1.4MHz, 3MHz, or 5MHz E-UTRA signal for in-band blocking or a CW signal, which appears at more than 15MHz distance for out-of-band blocking [2]. The in-band blockers are usually low power modulated signal while the out-of-band blockers are large power signals which can be up to 0 dBm [2]. Another interferer presents in the system is the Adjacent Channel Interferer (ACS). The blocking profile of interferers which the receiver must deal with is provided by the 3GPP and given in Fig. 1.3.

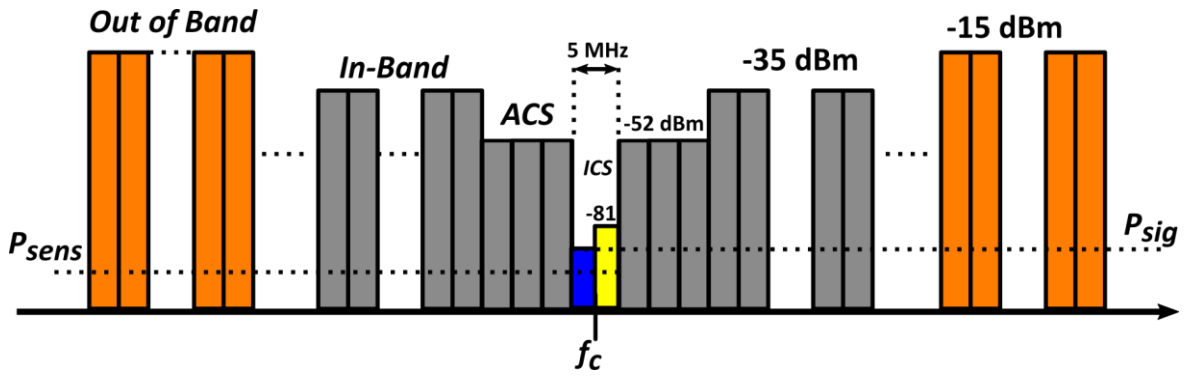

Fig. 1. 3 Blocking profile for a 5 MHz LTE signal [4]

1.1.3 Receiver Linearity

One of the most important functions of the SAW filters placed after the receiver antenna is to filter out the interferers, basically the out of band. Due to the non-linear characteristics of the RF front end devices, the interferers could inter-modulate or a modulated interferer cross-modulate with the desired signal. These would result in distortions degrading the desired signal quality. The linearity performance of these devices are characterised by gain compression (1 dB compression), third-order intercept point (IP3), either in-band IP3 or Out-of-Band IP3, and second-order intercept point (IP2). However, the linearity requirement for FDD and FD differs because in FD system, where the TX and RX operate simultaneously, the interferer is in-band which comes from the TX itself called the self-interference. On the other hand, in the FDD, the TX frequency is far from the RX. The interferers in this case could either be the TX leakage or a CW signal. Hence, the effective linearity is computed based on the power level of the leakage signals in both FDD and FD systems. In general, using a wideband self-interference canceller for both FDD and FD systems to suppress these interferers would greatly relax the linearity requirement of subsequent receiver front-end building blocks.

1.1.4 Transmitter Linearity

To measure the linearity of transmitter, the basic parameter used is the Adjacent Channel Leakage ratio (ACLR or ACPR, Adjacent Channel Power Ratio) [1], [5]. Due to the large power output of transmitters, for instance 24dBm in LTE for one transmit antenna port [2], unwanted signals from other transmitters are strictly regulated to avoid interfering with other transceivers. However, among these larger interferers, the most critical in the transmitter is the adjacent and the alternate channel signal as shown in Fig. 1.4. The ACLR is thus expressed as follows:

$$ACLR = \frac{\int_{f_0-\Delta BW/2}^{f_0+\Delta BW/2} PSD(f)df}{\int_{f_0-3\Delta BW/2}^{f_0+\Delta BW/2} PSD(f)df}\ , \tag{2}$$

where $PSD(f)$ represents the Power Spectral Density of the transmitted signal, while ΔBW is the TX channel bandwidth and f_0 is the TX centre frequency. In other words, the $ACLR$ is defined as the ratio of the power over an integrated bandwidth in the adjacent or alternate channel to the total wanted TX power. Due to the nonlinearity from the pre-power amplifier and main power amplifier, this leads to the creation of adjacent and alternate channel powers as a result of spectral regrowth, and also non-linear distortions in the TX signal.

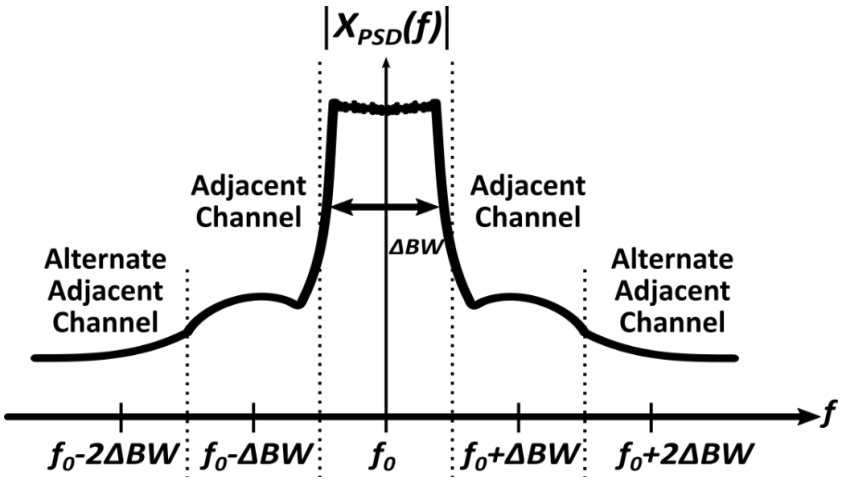

Fig. 1. 4 Adjacent and Alternate Adjacent Channels in a Transmitter Signal

1.1.5 Transmitter Out-of-Band Noise

The SAW filters after the PA actually attenuates the TX signal, but the residual TX leakage located at the RX frequency falls in-band adding to the receiver noise floor, which will eventually degrade the performance of the receiver. In general, the larger the TX bandwidth, the smaller the relative distance with the RX band and the more the noise contribution. As a consequence, the transmitter must be designed with very low noise. The major contributors of the out-of-band noise are the pre-power amplifier, DAC quantization noise and the thermal noise from the other TX baseband blocks. The noise contribution from the PA is generally small and can be neglected but that of the pre–power amplifier which scales with the output power level counts. When the output power is scaled down, the pre-power amplifier is also scaled down and hence, its relative noise contribution begins to increase. The TX noise is always expressed in dBc/Hz. In recent publications, TX noise of about -158dBc/Hz [20] has been reported.

The removal of SAW filters in the transceiver as shown in Fig. 1.5 would further exacerbate the effects of the interferers, especially on the receiver. One of the main focuses of this thesis is to analyse the challenges of going SAW-less and proposing solutions to mitigate these effects.

1.2 Challenges of SAW-less Systems

The coexistence of multiple bands for different applications such as Bluetooth, Wi-Fi/WiMAX and data-voice wireless communications would continue to generate increasing wireless radio complexity while imposing critical design challenges on both the designers of the transceiver building blocks. Moreover, the complexity, size and cost of the wireless radios would continue to be on the high side because these transceivers are dominated by large number of bulky passive components such as SAW filters/Duplexers that are responsible for attenuating out-of-band interferers. These components increase the chip pin count (large number of Input-Output pads)

and therefore, complicate the board design. The filtering of these huge interferers from the desired receive signals is nevertheless critical to relax the receiver linearity requirements. Since multi-mode multi-band radios require different filters for each band, the reconfigurability of these filters becomes a critical design challenge. The duplexer typically attenuates the TX signal by approximately 50 dB [1]. The elimination of these bulky external filters would therefore reduce board complexity, chip size and cost, and also eliminates their insertion loss that increases the total receiver Noise figure. This complexity reduction does not come without a penalty. There are lots of challenges that must be considered because the presence of modulated TX signals at the RX input places some constraints on the receivers [6] which are detailed as follows: The LNA must be highly linear (in terms of IIP3) to mitigate the generation of intermodulation distortion products, the down-conversion mixer must also have high IIP2 to reduce TX signal demodulation in band, the receiver synthesizer and the quadrature local oscillator must have very low phase noise to prevent the generation of reciprocal mixing, and finally, the receiver must have a very high dynamic range (ratio between maximum and minimum detectable signals) and compression point to prevent desensitization of the desired signal due to the TX leakage/interferer.

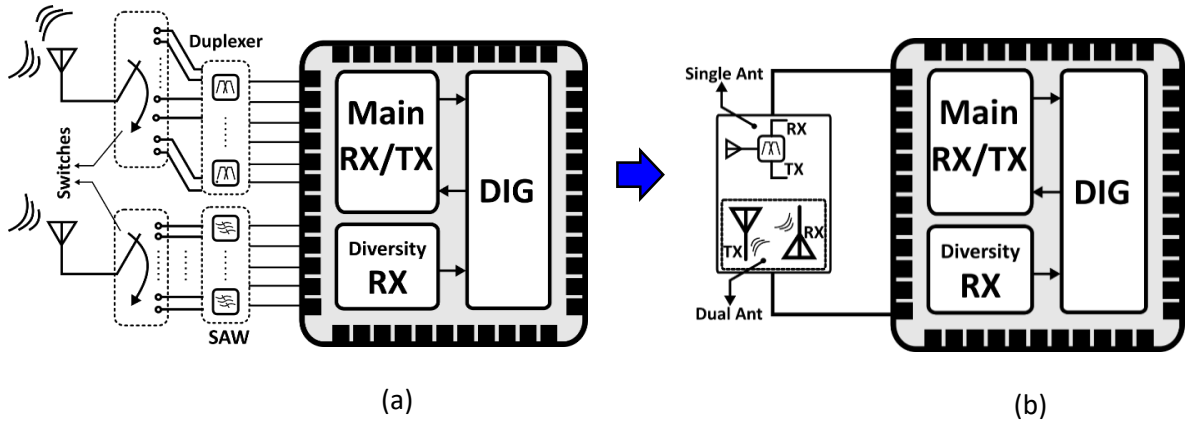

Fig. 1. 5 A Typical Transceiver (a)with (b) and without SAW filters/Duplexers

With the elimination of the RF filters, the problem associated with receiver as highlighted above would be discussed at length. While considering a simple direct conversion receiver, the system requirement for the linearity and noise would further be computed.

1.2.1 Receiver Gain Compression

The nonlinear properties of RF components become critical in the presence of interferers. The elimination of SAW filters before the RX front-ends makes the effect of interferers at the RX input more critical to the receive signal quality. One of the effects of this interferer on the receiver is called gain compression. To have a clear insight on the term gain compression, the nonlinear behaviour of a memoryless device would be analysed. The device input/output characteristics can be approximated with a Taylor's series expansion as:

$$V_o(t) \approx \alpha_1 V_{in}(t) + \alpha_2 V^2{}_{in}(t) + \alpha_3 V^3{}_{in}(t), \tag{3}$$

where $V_{in}(t)$ is the input signal, $V_o(t)$ is the output signal, α_2, α_3 are the second order and third order nonlinear coefficients, and α_1 can be referred to as the device small signal gain when both $\alpha_2$and α_3 are negligible for small input swings. Assuming a single tone input signal, $V_{in}(t) = Acos(\omega_0 t)$ passing through the nonlinear device, the output can be expressed as:

$$V_o(t) = \alpha_1 Acos\,\omega_0 t + \alpha_2 A^2 cos^2\omega_0 t + \alpha_3 A^3 cos^3\omega_0 t \tag{4}$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right) Acos\,\omega_0 t + \frac{\alpha_2 A^2}{2} cos2\omega_0 t + \frac{\alpha_3 A^2 A}{4} cos3\omega_0 t). \tag{5}$$

As can be seen from (5), the output signal of the nonlinear device exhibits multiple harmonics of the input frequency. The device gain $\left(\alpha_1 + \frac{3\alpha_3 A^2}{4}\right)$ is a function of the input signal amplitude. This, thus shows that as the input signal, A increases, the device gain deviates from its small signal value. In particular, a very large input signal amplitude would result in amplitude compression for $\alpha_1\alpha_3 < 0$, which is usually the

case of most RF circuits. For $\alpha_1\alpha_3 > 0$, the device experiences expansion. To get a feeling for the input level when considerable gain compression occurs, we use the concept of 1-dB compression point, P_{1dB}, defined as the input level that causes the linear small-signal gain to drop by 1 dB [1] as illustrated in Fig. 1.6. Thus, P_{1dB} is calculated by $P_{1-dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$.

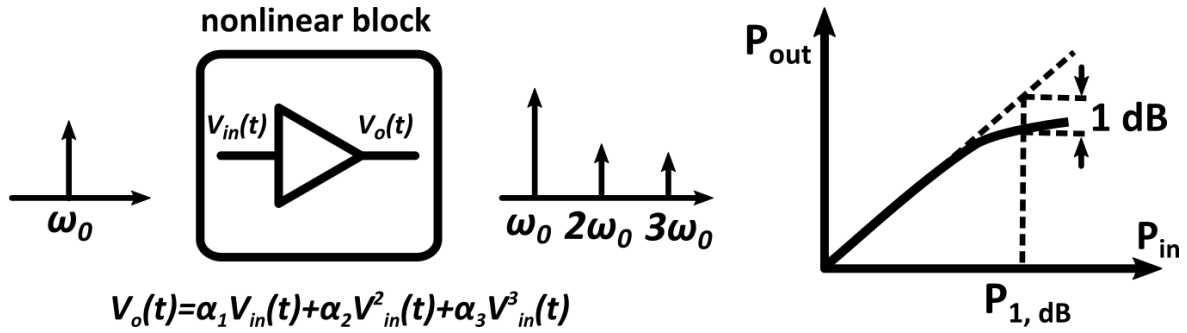

Fig. 1. 6 1-dB compression of a tone in a nonlinear block

The adverse effect of gain compression due to large interferer accompanied by a desired receive signal in a nonlinear device (for instance, LNA) is desensitization of the receive signal. This will eventually degrade the system SNR.

1.2.2 Intermodulation

Intermodulation in RF circuits arises when two out of band interferers (accompanying the desired signal) are present at the input of a nonlinear system. When these two strong interfering signals at frequencies ω_1 and ω_2 are sensed by the nonlinear system, they will mix and create also spurious signals at the output that are not harmonics of these two frequencies, which are known as intermodulation products. Considering a two-tone signal of amplitudes A_1 and A_2 appearing at the input of a nonlinear amplifier, $V_{in}(t) = A_1 cos(\omega_1 t) + A_2 cos(\omega_2 t)$, the amplifier output can be computed from (3) as:

$$V_o(t) = \alpha_1 A_1 cos(\omega_1 t) + \alpha_1 A_2 cos(\omega_2 t) + \cdots + \alpha_2 A_1 A_2 \, cos(\omega_1 - \omega_2)\, t + \cdots$$

$$+\cdots+\frac{3\alpha_3 A_1^2 A_2}{4}cos(2\omega_2-\omega_1)\,t+\frac{3\alpha_3 A_1^2 A_2}{4}cos(2\omega_1-\omega_2)\,t+\cdots, \qquad (6)$$

where some terms have been neglected for clarity, the tones at $2\omega_2-\omega_1$ and $2\omega_1-\omega_2$ are the third order intermodulation products (IM3) and the tone at $\omega_1-\omega_2$ is the second order intermodulation product (IM2). Intermodulation products are problematic in RF system designs for a range of reasons. The IM3 product creates additional in-band frequency content often called "spectral regrowth" which in a receiver it will corrupt the signal of interest, while in a transmitter can interfere with other wireless channels thereby corrupting other users transmitting in the frequency of the intermodulation product [7]. Hence, the IM3 level must be maintained low as prescribed by the 3GPP for wireless communication devices during circuit design.

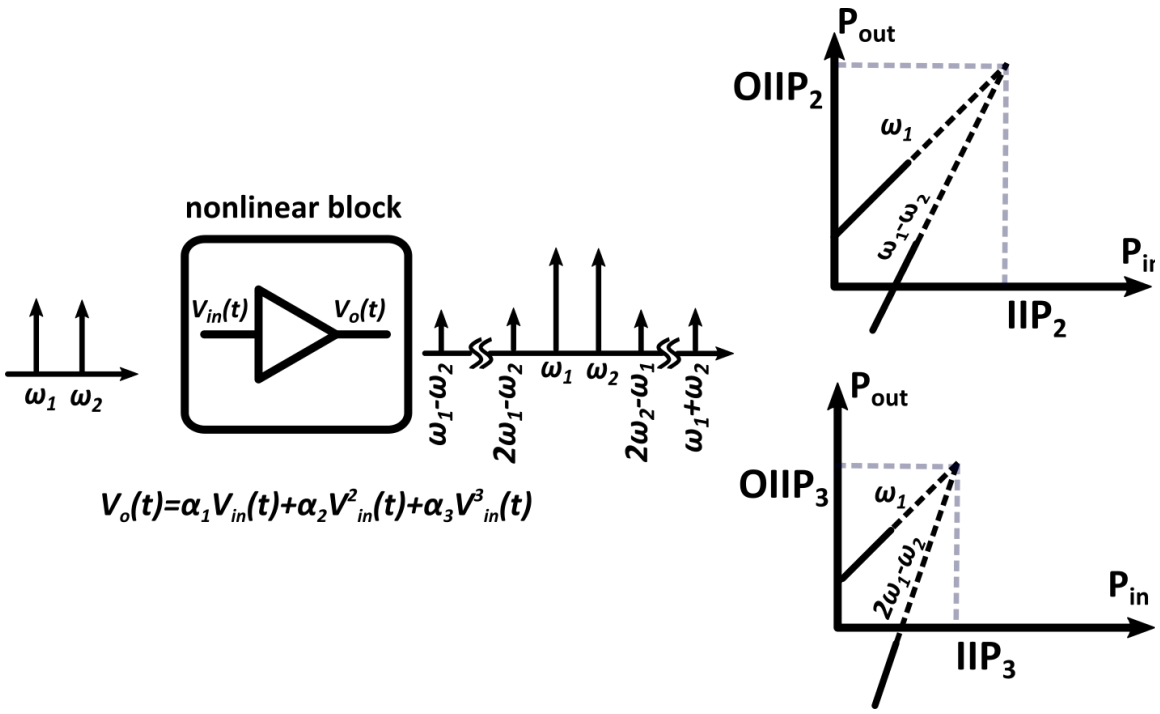

Fig. 1. 7 IIP2 and IIP3 definitions in a nonlinear block due to intermodulation of two tones

As shown in Fig. 1.7, the extrapolated point at which the IM3 intersects with the fundamental is referred to as third intercept point, IP3. When referred to the input

signal power, it is called Input IP3 (IIP3) and to the output is Output IP3 (OIP3). The IIP3 is expressed as, $P_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}$ and generally around 10dB more than 1 dB compression point. Also shown in Fig. 1.7 is the IIP2 plot. The extrapolated point at which the second order distortion product meet the fundamental is the Intercept point (IP2) expressed as , $P_{IIP2} = \frac{\alpha_1}{\alpha_2}$.

1.3 Computing the System Linearity Requirements for LTE FDD Receivers

1.3.1 Third order Intermodulation

Recall that the SAW filters/Duplexers are used to suppress the out of band interferers by around 50 dB. Considering the 20 MHz LTE FDD channel bandwidth (E-UTRA Band 2) with sensitivity level of -92 dBm, the signal power level, P_{sig} at the receiver input should be well above the sensitivity level (around -92 + 9 = -83 dBm). The P_{sig} must be received and demodulated correctly in the presence of self-interference and CW blocker. The IM3 power level prescribed by the 3GPP is calculated by $IM3 \leq 10\log_{10}\left(10^{P_{sig}/10} - 10^{P_{NoiseFloor}/10}\right)$. Assuming a 10 dB receiver NF, the noise floor, $P_{NoiseFloor}$ is -91dBm. Hence, the third-order intermodulation must be less than -83.7dBm.

For a two tone test where the self-interference signal P_{SI} is of the same power level as the CW blocker, P_{BLK} (i.e. $P_{SI} = P_{BLK} = P_i$), the IIP3 is calculated as: $IIP3 \geq \frac{3P_i - IM3}{2}$. However, in general, the calculation of the IIP3 depends on the frequency placement of the blocker and the self-interference from the RX signal. Elimination of the SAW filters would require that the TX and RX be isolated from each other. However, the low isolation (ISO) between them would impose severe linearity requirements on the receiver. In this case, the self-interference power level at the receiver input is given as; $P_{SI} = P_{TX} - ISO$.

When the self-interference is closer to the receive signal frequency as shown in Fig. 1.8, this is often termed full duplex frequency which is the most generally reported.

But, in the case where the CW blocker is closer to the receive signal frequency, it is termed half duplex frequency as depicted in Fig. 1.9. The IIP3 in the two scenarios are expressed below respectively.

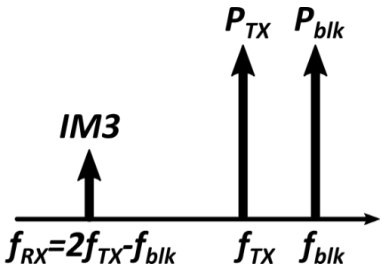

Fig. 1. 8 Full duplex frequency

$$IIP3_{FD} = P_{TX} - ISO + \frac{P_{blk} - IM3}{2}, \tag{7}$$

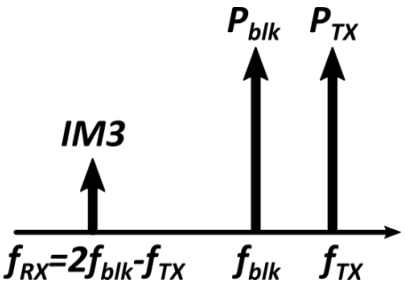

Fig. 1. 9 Half duplex frequency

$$IIP3_{HD} = P_{blk} + \frac{P_{TX} - ISO - IM3}{2}, \tag{8}$$

Since the TX power is always large (around 24dBm for LTE) and with limited isolation, the linearity requirement for the receiver is more demanding in the case of full duplex frequency. Since there have not been any standard as regards the level of isolation between the TX and RX, many authors have used different ISO values in their publications for their SAW-less receiver designs. Shown in Fig. 1.10 is the IIP3 requirement versus the level of TX-RX isolation for both the half duplexing and full duplexing scenarios. The minimum IIP3 to meet the 3GPP standard specified for wireless communication device sensitivity ($-92dBm$) for 30dB isolation is 28 dBm in the full duplex frequency and about 23 dBm for the half duplex frequency.

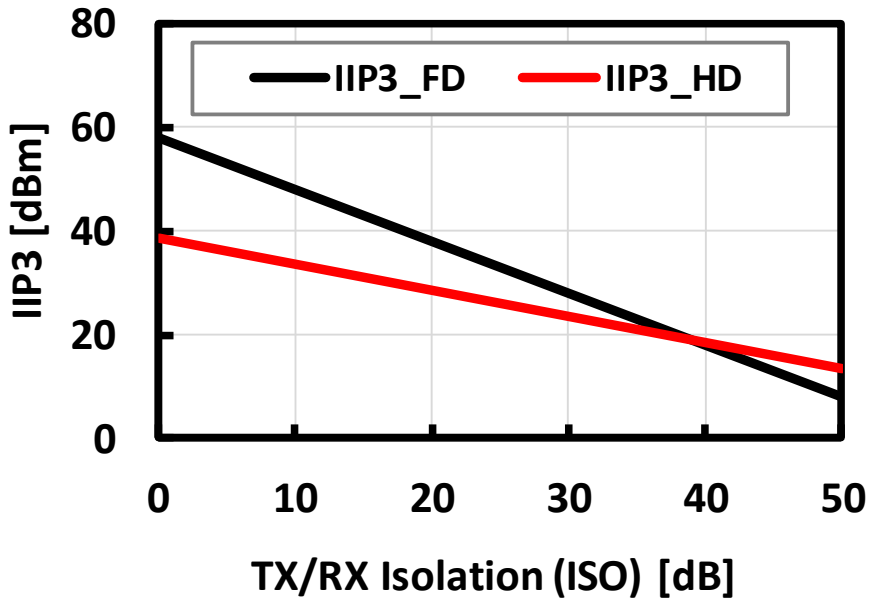

Fig. 1. 10 RX IIP3 as a function of TX/RX isolation for both full duplex frequency and half duplex frequency

1.3.2 Second order Intermodulation

In an ideal differential circuits, the IM2 level is zero, indicating an infinite IIP2 value. However, in real circuit implementations, the IIP2 of the differential circuit is limited due to nonidealities (mismatch). The most critical nonidealities comes from the asymmetry of the mixer, since the LNA is usually ac-coupled to the Mixer. The IP2 referred to the SAW-less receiver input is calculated as: $IIP2 = 2(P_{TX} - ISO) - IM2$, where the $IM2 \approx P_{sens} - SNR + 9$. The IIP2 is calculated to be 80 dB. This is a very challenging requirement, however, this value can still be relaxed further considering a correction factor when two tones are used for the IIP2 computation at the receiver input [8].

1.3.3 LO Phase Noise

The LO generation circuits in wireless transceivers are generally common for both the up-conversion and down-conversion signals. However, the generation of LO signal from the frequency synthesizers is far from being ideal. The real LO generation is

always associated with phase noise [1] which appears like a skirt around the ideal LO impulse signal as shown in Fig. 1.11. This noise is detrimental to the performance of wireless transceivers during the conversion of signals. In a receiver, this noisy skirt-like LO convolve with the blocker to generate a broadened down converted blocker whose noise skirt would corrupt the down converted desired signal.

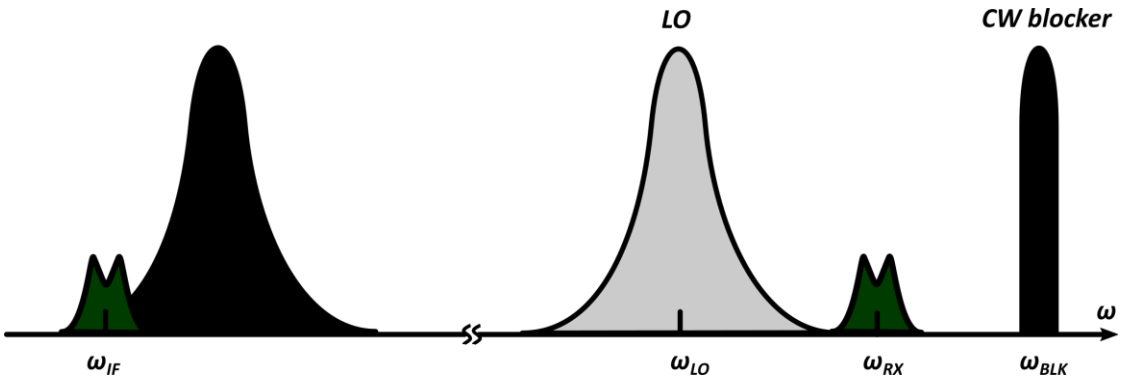

Fig. 1. 11 Reciprocal mixing due to noisy LO

While in a transmitter using the OFDM modulation scheme, the LO phase noise would impair each of the RF subcarrier making demodulation in the receiver problematic. This phenomenon is best described as Reciprocal Mixing. The reciprocal mixing has to be kept below the noise floor [11] and this can be expressed as:

$$PN_{\Delta f} + P_{Blk} + 10log_{10}BW < P_{noisefloor}\,, \tag{9}$$

where $PN_{\Delta f}$ is the phase noise at Δf frequency offset from oscillator carrier, P_{Blk} is the interfere power and BW is the bandwidth of the signal.

To mitigate the effect of phase noise, it requires an adequate suppression of the interferer, and the LO phase noise must be lowered in accordance to the level of interferer suppression. However, lowering the LO phase noise infers large power consumption in the frequency synthesizers.

For instance, in GSM mobile application, in TX the phase noise must be less than -162dBc/Hz at 20MHz offset frequency for 915MHz carrier [1] with a penalty of very

high amount of power consumed by the frequency synthesizer which could burn more than 30% of the wireless RX power [10].

1.3.4 TX Noise Leaking in RX band

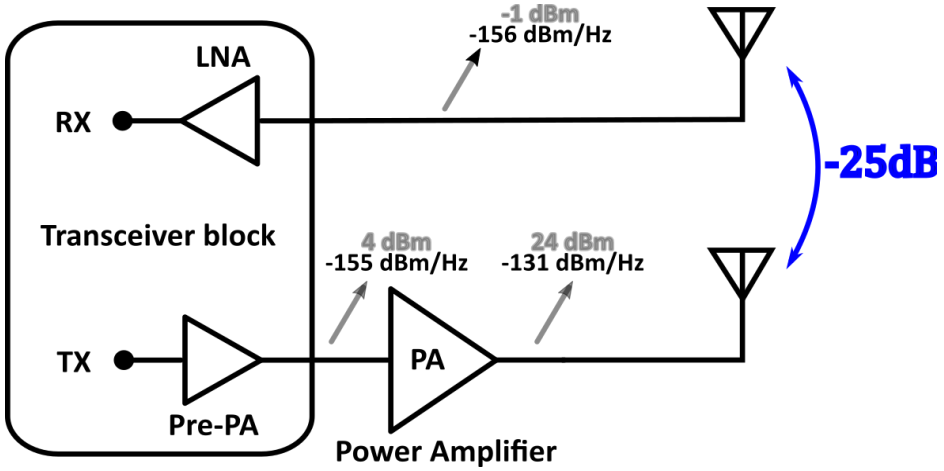

Fig. 1. 12 Numerical example of TX out of band noise requirement in RX band

As introduced in section 1.1.5, the TX noise falling in-band is another challenge in SAW-less receiver. The noise must be kept below the thermal noise floor ($-174\ dBm/Hz$) to avoid degrading the overall RX SNR. Supposing a finite isolation, ISO of 25 dB between the TX and RX, a TX power level of 24 dBm and a pre-power amplifier emitting 4 dBm with noise of -155 dBm/Hz, the TX noise, $P_{TX,noise}$ appearing in the RX band is -156 dBm/Hz which is far above the thermal noise floor. This can only be improved by either increasing the TX/RX isolation and/or introducing an RF canceller or noise cancelling techniques to suppress the TX signal power and noise. The TX noise relative to the TX power is the TX SNR (measured in dBc/Hz). Fig. 1.13 shows the TX noise in dBc as a function of the isolation. It shows that without SAW filters, the limited isolation is detrimental to the RX noise. Thus, further suppression of the TX signal leaked to the RX input is required, to compensate the filtering value (50dB) achieved while using the duplexer.

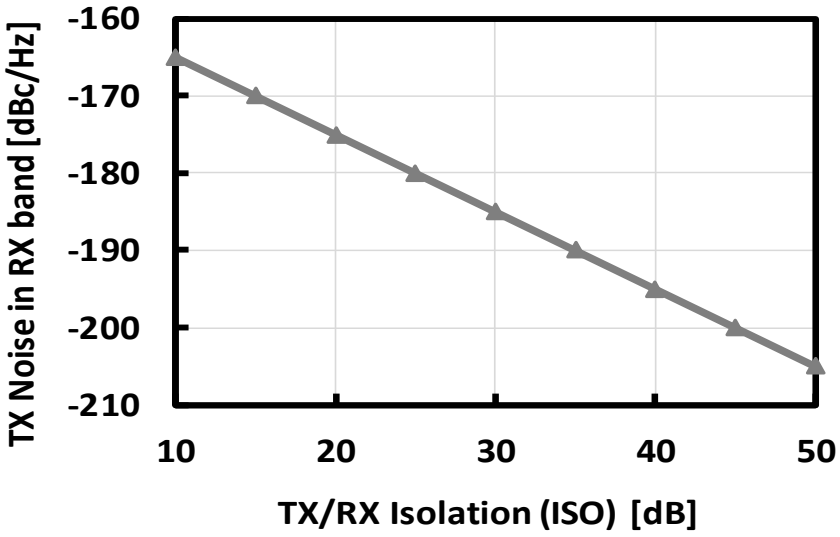

Fig. 1. 13 Transmitter out of band noise in RX band

The challenges of SAW-less receivers associated with the effect of the self-interference as analysed can be relaxed and mitigated by suppressing the SI further. Moreover, improving the TX-RX isolation would require a self-interference cancellation technique. The SI cancellation can be done in RF and further in baseband to additionally relax the dynamic range of the ADC.

1.4 Effect of SI Cancellation on the System Requirements

The introduction self-interference cancellation could be of great benefit or detrimental to the performance of the SAW-less receiver. However, the cancellation circuitry must be designed to ensure its benefits in improving the system performance outweigh the possible degradation that it introduces. Those aforementioned challenges in SAW-less receiver which includes linearity, ADC dynamic range and TX noise in RX band could be relaxed while introducing the self-interference canceller. These Self-Interference Canceller could be passive or active and a detailed description is left for the next

chapter. The canceller generates the TX replica, which is adjusted in magnitude and phase to cancel out the SI at the RX.

The suppression of the self-interference could be done solely in RF or in baseband or as a combination of the two cases. However, performing the cancellation of the interference signal in RF would help relax the requirements for the RX front-end building blocks instead of delaying the cancellation till the baseband in order to avoid desensitization of the LNA and other issues attached to SAW-less receivers as highlighted above. For the purpose of this dissertation, the analysis of the RF cancellation as illustrated in Fig. 1.14 would be considered. Considering a dual antenna SAW-less transceiver with TX-RX isolation, ISO, TX power (P_{TX}), and sensitivity level of -92 dBm, the new system requirement is analysed and detailed below:

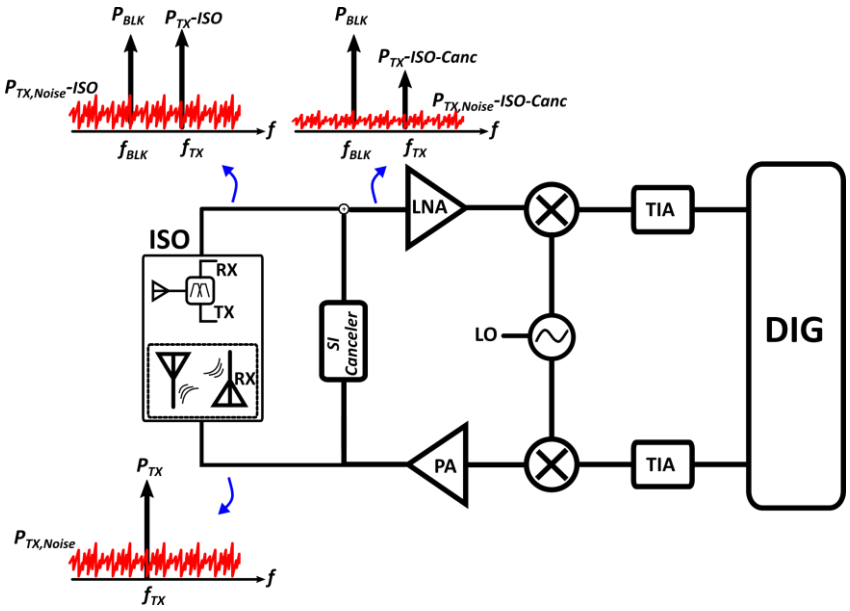

Fig. 1. 14 Self- interference cancellation illustration in RF

1.4.1 Linearity

One of the major advantages of SI cancellation is RX linearity equivalent improvement. The system linearity with self-interference cancellation

can thus be characterized by effective input intercept point both in-band and out of band.

Considering a two-tone test with SI and a blocker at the RX input, with the SI cancelled at the RX input, the relaxed intercept point for the second and third order with SI cancellation introduced can be computed as: $IIP3_{relaxed} = IIP3_{RX} - Canc$ and $IIP2_{relaxed} = IIP2_{RX} - Canc$. From (7) and (8), the effective receiver IIP3 is thus calculated as:

$$Eff.\ IIP3_{FD} = P_{TX} - ISO - Canc + \frac{P_{blk} - IM3}{2}, \tag{10}$$

$$Eff.\ IIP3_{HD} = P_{blk} + \frac{P_{TX} - ISO - Canc - IM3}{2}, \tag{11}$$

With an ideal canceller, the suppression of the SI signal by the canceller at the input of the receiver should give a corresponding improvement in the receiver linearity. Assuming a SIC of 20 dB, the receiver IIP3 is relaxed by 20 dB and 10 dB in the full duplex and half duplex case respectively. Illustrated in Fig. 15 is the required IIP3 of a receiver and the improvement of the relaxed IIP3 as a function of SI cancellation for the case of the full duplex frequency as generally reported as the RX IIP3. However, the finite linearity of the canceller will introduce distortion at the input of the RX which would eventually reduce the effective linearity improvement. The canceller must be designed such that its output third order distortion, $IM3_{canc}$ is much lower than the referred input IM3 of the receiver with the canceller active. The required canceller IIP3 can therefore, be calculated requiring $IM3_{canc} \leq IM3_{RX}$ as:

$$IIP3_{canc} \geq P_{TX} + \frac{(P_{blk} - IM3_{RX}) - G_{canc}}{2}, \tag{12}$$

Where $ISO = G_{canc}$, where G_{canc} is the gain of the canceller in dB, and the output canceller power level ($P_{TX} - G_{canc}$) is the SI power at the receiver input.

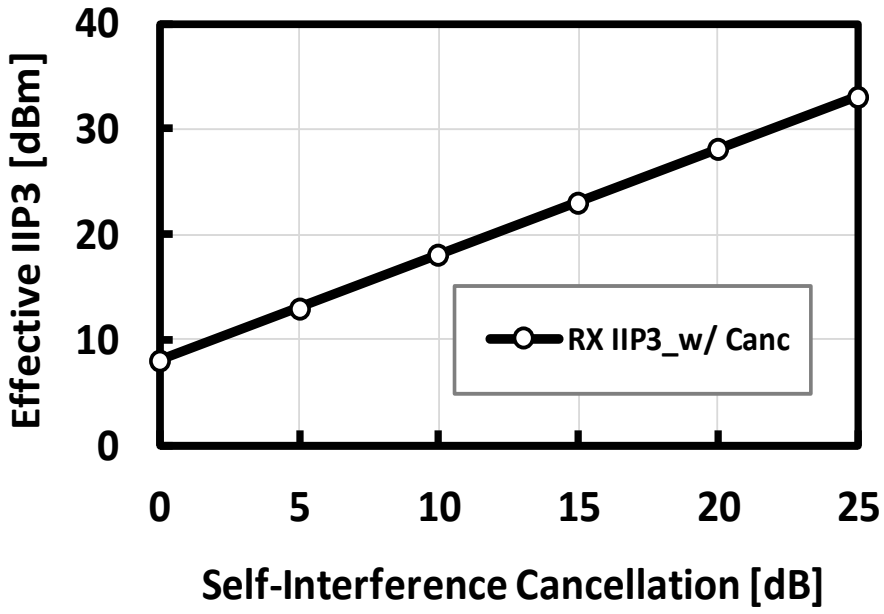

Fig. 1. 15 Receiver IIP3 requirement, and relaxed RX IIP3 improvement with canceller enabled

Fig. 1.15 depicts the effective IIP3 requirement of a receiver with the introduction of SI cancellation. While considering $P_{TX} = 24dBm$ and $IM3_{RX} = -83\ dBm$ ($\approx P_{sens} + 9 = -92\ dBm + 9$), ISO = 25 and $P_{BLK} = -15\ dBm$, the required IIP3 is 33 dBm which is difficult to achieve relying on the linearity of the front-end building blocks especially the LNA. Given a relaxed receiver IIP3 of 8 dBm, the effective IIP3 when cancellation of 25 dB is achieved is therefore restored back to 33 dBm. However, to ensure that the effective IIP3 reaches the required IIP3 with canceller enabled (at 30 dB of TX/RX isolation), the canceller must be designed with an IIP3 of 43 dBm as shown in Fig. 1.16 for a 24 dBm TX power input. This result becomes a bottleneck in the canceller design. A careful analysis, design and layout must be done to ensure the IIP3 target of the canceller is met.

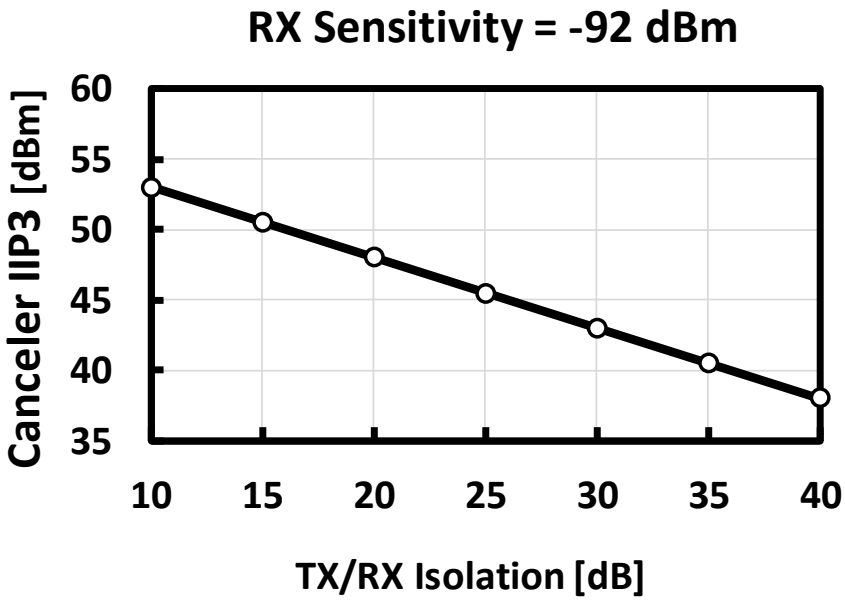

Fig. 1. 16 .Canceller IIP3 requirement as a function of TX/RX isolation

1.4.2 Dynamic Range

The key building block in digitization of demodulated signal is the Analog to Digital converter (ADC). The choice of the ADC depends on its role in quantization and the effect of SI on its performance. The upper limit performance depends on the power of SI while the lower limit depends on the quantization noise. The quantization noise must be lowered such that the desired signal is not degraded by the noise, while the SI power must not be too large to over-range the ADC input. The range between the upper and the lower limit of an ADC is quantified by its Dynamic Range defined as the ratio between the largest signal level the ADC can handle without distortion and the noise level, expressed in dB. The dynamic range also determines the maximum SNR [12]. However, the effect of quantization can best be studied by determining the SINR (Signal to Interference and Noise Ratio) [13].

Considering a total cancellation of SI in digital domain would be a much challenging task in the design of the front-ends because of the larger interferer getting through to the baseband without suppression. The effects on the front-ends such as desired signal desensitization, intermodulation distortion and the noise floor increment would still be there without any reduction. The ADC would also require a huge dynamic range to handle this interferer. For instance, with a TX power level of 24 dBm and a desired signal of -83 dBm (LTE specification), and considering an ISO of 25 dB, the dynamic range, DR as expressed in [14] is given by the calculation below while assuming the ADC's quantization noise to be around the RX sensitivity level.

$$DR = 24\ dBm - 25dB - (-92\ dBm) = 91\ dB, \quad (13)$$

ADC Dynamic range according to [15] is also expressed as: $DR_{|dB} \approx 6.02N + 1.76$, where N is the number of bits. The effective number of bits (ENOB) required by an ideal Nyquist-rate ADC with DR of 91 dB is given by:

$$ENOB_{|bits} \equiv N \approx \frac{DR_{|dB} - 1.76}{6.02} = \frac{91 - 1.76}{6.02} = 15\ bits. \quad (14)$$

The 15 bits requirement would eventually consume a large amount of power with a high sampling rate. However, to relax this requirement, the suppression of the SI at the RX input (at RF) by about 30 dB ($Canc_{|dB}$) would relax the ADC DR range to (91-30)=61 dB as illustrated in Fig. 1.17 bringing the $ENOB$ to 10 bits, which is a more relaxed requirement in the ADC design and power consumption.

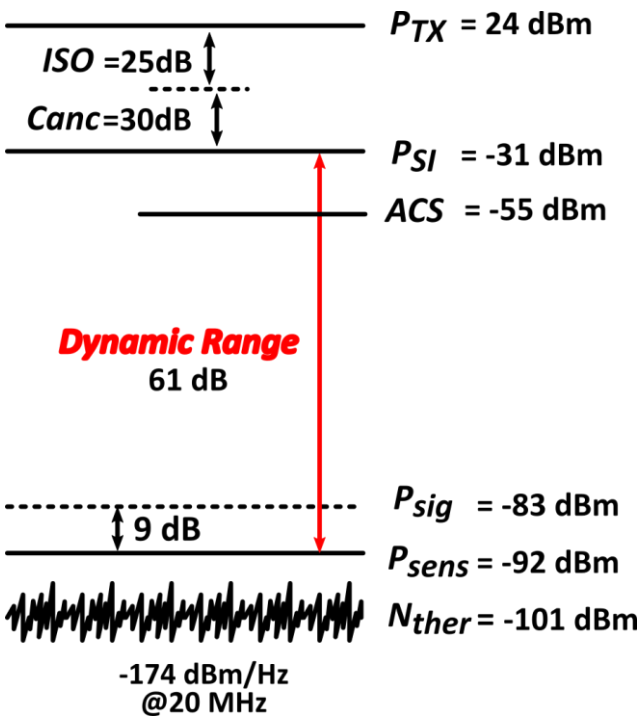

Fig. 1. 17 Estimation of Dynamic Range of a Receiver

1.5 Bandwidth Limitation on SI cancellation

Aside the nonlinearity of the canceller which causes distortion generation at the input of the receiver, another limitation of the canceller to the receiver is the bandwidth of the SI cancellation. A wider bandwidth would ensure the suppression of the noise of the leakage TX signal in the RX band. However, the delay introduced during the coupling from TX to RX would result in the narrow band SI cancellation if the canceller has a response which is flat in frequency. However, the delay in the SI through the TX and RX antennas thus, translate to phase shift. Most of the implemented cancellers operating as vector modulator, such as [16] produce a cancellation signal with a linear phase slope which are unable to perfectly imitate the phase slope of the SI signal, hence signal cancellation over a narrow frequency range is experienced. The small cancellation bandwidth would have limitation on the suppression of SI noise in the RX band. In [17], an auxiliary noise cancelling circuit is required to further suppress the TX noise in the RX band. For instance, considering

the SI in voltage, $V_{SI} = 10^{(-\frac{ISO}{20})} V_{Tx} \sin(\omega_{Tx}\tau)$, where ω_{Tx} is the TX frequency and τ is the delay from TX to RX and the cancellation signal V_{canc} as illustrated in a vector triangle in Fig. 1.18, where no amplitude error between the SI and the cancellation signal, that is $V_{SI} = V_{canc}$, then the vector sum of the signals gives a residual signal, $V_{res} = 2V_{SI} sin(^{\omega_{Tx}\tau}/_{2})$. The derivation is obtained from the simplified isosceles triangle shown in Fig. 1.18.b.

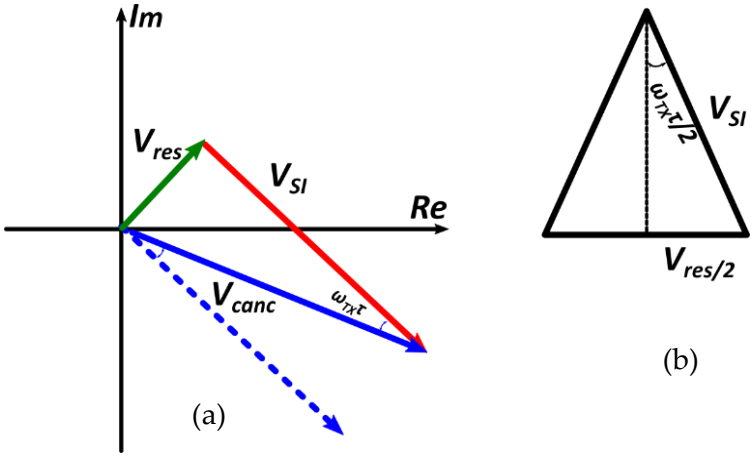

Fig. 1. 18 (a) Vector sum of the leakage and cancellation signal in the presence of delay; (b) An isosceles triangle of the vector sum

The phase error between the SI and cancellation signal introduced due to the group delay is expressed as: $\omega_{Tx}\tau = 2\sin^{-1}\left(\frac{V_{res}}{2V_{SI}}\right)$ and $\frac{V_{res}}{V_{SI}}$ depicts the level of achievable SI cancellation, that is, $\frac{V_{res}}{V_{SI}} = 10^{-\frac{Canc}{20}}$. The cancellation bandwidth, BW_{canc} is thus calculated as:

$$BW_{canc} = \frac{2}{\pi\tau}\sin^{-1}\left(\frac{V_{res}}{2V_{SI}}\right), \tag{15}$$

The relationship between the delay and the cancellation bandwidth is illustrated in Fig. 1.19 with different cancellation levels while considering a frequency-flat SI canceller. The figure illustrates that with a group delay of 2ns, a cancellation bandwidth of 9 MHz would be achieved for 25 dB of SI cancellation in the worst case.

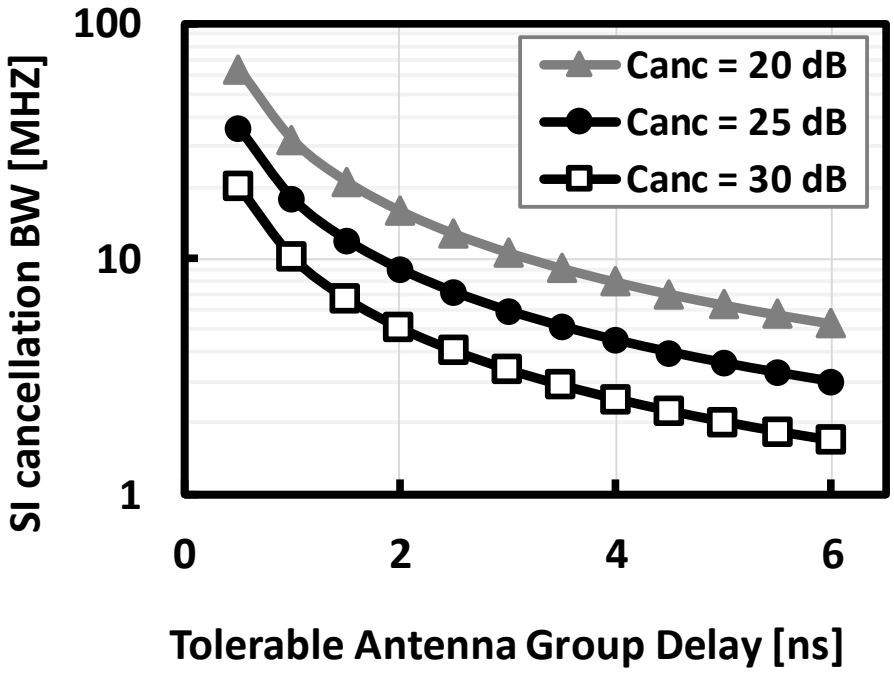

Fig. 1. 19 Calculated Cancellation bandwidth as a function of group delay for different levels of SI cancellation

1.6 Canceller Noise Contribution to the Receiver

The introduction of SI cancellation circuitry to replace the bulky off-chip SAW filters/ Duplexers does not come without penalty. The power consumption, linearity and noise must be thoroughly analysed to avoid degrading the system. The noise contribution of the canceller depends on the choice of cancellation, either in RF or at baseband. Considering an RF cancellation, the canceller can be connected directly at the input of the receiver or after the LNA. Connecting the canceller at the receiver input shows that the injected canceller noise adds to the Rx signal before any amplification. On the other hand, connecting the canceller after the LNA, its noise is scaled with the LNA gain (Friis' equation). Another important factor to consider in the canceller design is the type of components used. Several authors have presented passive and active cancellers. The choice of passive components means lower noise

compared to active but with some trade-offs, as it will be discussed further in the next chapter under literature review.

For the purpose of this thesis, the noise of the canceller for RF cancellation would be analysed. For case A, the canceller is connected at the input of the LNA while for case B, the cancellation is done at the LNA output as shown in Fig. 1.20. The isolation between the TX and RX can be related with the canceller gain, g_{canc}, implying that $g_{canc} \approx iso$ (expressed in magnitude), since the canceller is connected directly without the need of a coupler. This means that the canceller must have a high input impedance to avoid loading the PA and the output of the canceller is seen as a virtual ground for the leakage cancellation. The noise factor of the canceller is thus given as: $F_{canc} = 1 + \frac{V_{n,out,canc}^2}{4KTR_S\, g_{canc}^2}$. The system noise factor is therefore calculated as: $F_{sys} = 1 + \frac{V_{n,in,RX}^2}{4KTR_S} + \frac{V_{n,out,canc}^2}{4KTR_S}$, where $V_{n,in,RX}^2$ is the input referred noise of the receiver. The system noise figure for case A is thus expressed as:

$$NF_{sys,A} = 10log_{10}[F_{RX} + iso^2(F_{canc} - 1)]. \quad (16)$$

However, for case B, the noise of the canceller is scaled with the gain of the LNA, g_{LNA}, (expressed in magnitude) and the calculated system noise figure is expressed as:

$$NF_{sys,B} = 10log_{10}\left[F_{RX} + \frac{iso^2(F_{canc}-1)}{g_{LNA}^2}\right]. \quad (17)$$

Fig. 1.21 illustrates the noise figure of the system as a function of the canceller noise. The canceller noise is referred to its own input source impedance. The calculated system noise figure is plotted while assuming the RX NF of 5 dB for both case A and case B. The figures depict that the canceller contributes less noise in the scenario of case B at the expense of huge linearity requirement for the LNA, which would be required to avoid its desensitization and distortion generations due to the SI. This would further be reviewed in the next chapter. However, in the case of scenario A, the canceller contributes more noise when there is low isolation (for instance, ISO= - 20

dB). This is because the canceller has to attenuate less in order to generate the SI replica.

Fig.
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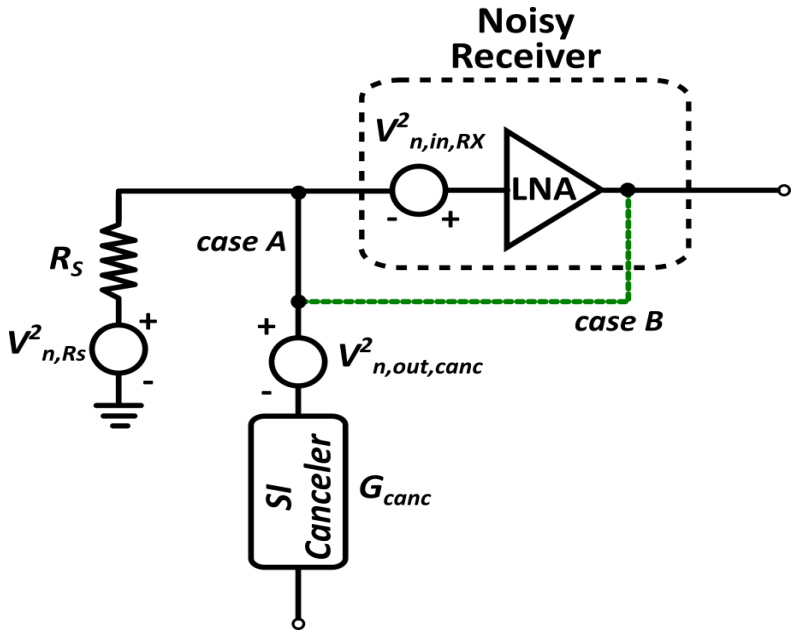
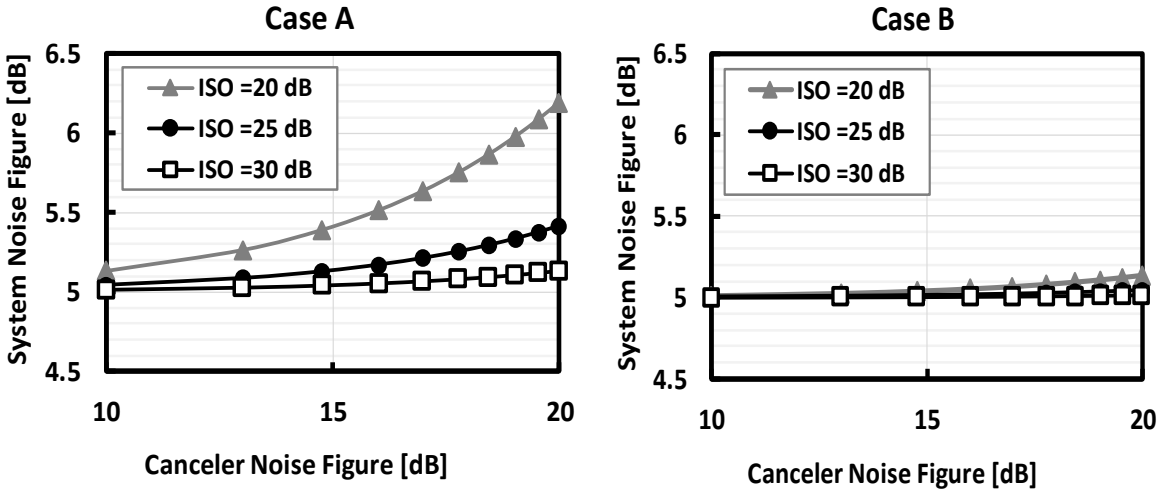


Fig. 1. 20 Simplified System for RF canceller noise analysis



(a) (b)

Fig. 1. 22 Estimated system noise figure assuming a RX NF of 5 dB (a) for Case A, with canceller connected at RX input; (b) Case B, where canceller is connected after LNA

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Chapter 2

Self–Interference Cancellation Techniques: A review

Self-Interference signals from transmitter to receiver have been of great impediments to RX sensitivity. Several researches have been carried out on the cancellation or suppression techniques of the SI signals in both wireline and wireless communications. The scaling down of CMOS technology provides millions of devices to be integrated on chip. This further encourages researches in the design of integrated canceller replacing the off chip SAW filters/Duplexers which can handle large SI, thus preventing receiver desensitization and improving the receiver linearity. Both Passive and Active SI cancellation circuitry have been proposed in prior works. This chapter discusses different SI canceller state of the art at full length. At the end of the chapter, a summary of the performance of different cancellers is tabulated to clearly explain the contribution of each paper to SI cancellation techniques and the need for further improvement in this research area.

2.1 Self-Interference Cancellers

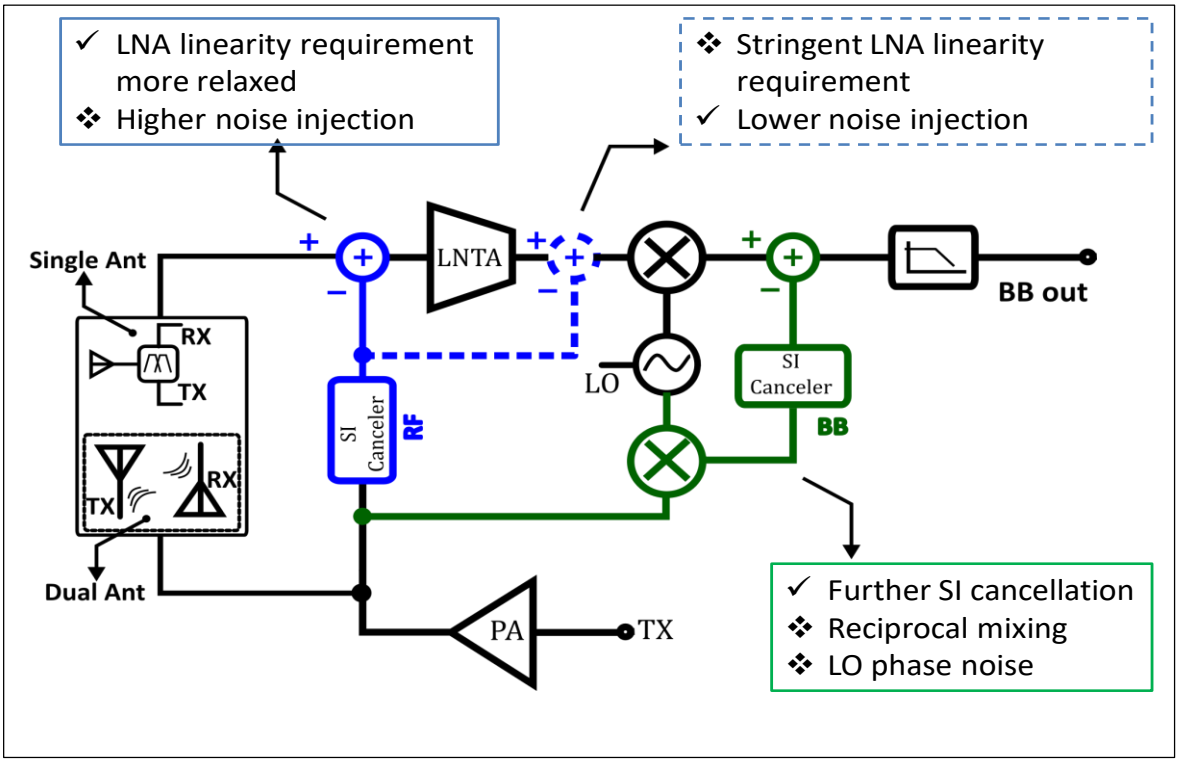

Fig. 2.1 Transceiver block diagram with generic self-interference cancellation in RF and baseband

Illustrated in *Fig. 2.1* is the general cancellation concepts reported in different prior works. The generic self-interference cancellation in a single antenna [1], [4] or dual antenna [2], [5] transceivers with limited SI isolation between the TX and RX involves the use of a generated transmitted signal replica, which is equal in magnitude and has a 180° phase difference compared with SI to cancel the latter out. This SI cancellation can either be done at RF, in base-band or as a combination of both. The cancelling of the SI in RF would help relax the linearity requirement of the RX front-ends. The further cancellation of the SI residue in base band would help relax the dynamic range of the rest of the receiver, especially the ADC. In both domains, the TX replica is generated by connecting the canceller to the PA output or at the PPA. The choice of down-converting the TX signal using the mixer might result in reciprocal mixing and addition of LO phase noise due to the non-ideal LO generation. The choice of

connecting the canceller at the RX input or after the LNA as shown in *Fig. 2.1* depends on the canceller circuitry, its noise contribution and RX (LNA) linearity. Connecting at the RX input would result in high noise injection and canceller distortions at the RX input while cancelling the SI after the LNA would lower the noise contribution of the canceller. Prior works on SI cancellation have either been categorized as pure passive, active or designed with both passive and active devices.

2.2 Active and Passive Cancellation Architectures

The design of SI canceller either in passive or active comes with trade off. The passive cancellers are designed with bulky components like inductors and capacitors and resistors which occupy large silicon. The lossy components would also result in loading the PA which could degrade the power efficiency. The possible reconfigurability and easy integration over fixed frequency SAW filters still make it a design choice. The use of passive components ensures highly linear cancellation circuitry with little or no distortion injection at the receiver input and with smaller noise contribution. The passive canceller provides also no gain in the cancellation signal, however, the canceller could handle larger TX signal up to 20 dBm as would be described in chapter 4 at its input without significant distortion contribution to the system.

Canceller design architectures with active components have the benefit of easy integration with small form factor. Active canceller provides gain in the cancellation signal but could only handle small TX signal required for the SI cancellation. This explains why an attenuator (which can be made of capacitors to prevent additional noise injection) is required to lower the TX signal. Another option is to connect the canceller to the PPA output, which has a maximum power of around 6 dBm. Active canceller does not load the TX, as a common source based active canceller provides large input impedance. Active components are not as linear as passive, the distortion

contribution of the active canceller degrades the effective linearity of the system. This, thus explains why minimal voltage swing (low TX power) is required at the input of the canceller to avoid excessive distortion contributions. The active canceller can also be easily disabled when a weak SI is received thereby saving power. Another contribution of active components to the system is the noise, which is a trade-off with the power consumption. Reducing the noise contribution requires burning a large power. Optimum design approach for active canceller must be adopted to ensure minimal noise contribution to the entire system.

Recent works have also shown cancellation architectures with both passive and active components which are used to provide signal attenuation, phase variation and also variable gain while generating the TX replica required for the SI cancellation. A review of the recent works involving both passive and active cancellation are described in the next section.

2.3 State-of-the-Art Active Cancellation Circuits

Calderin et al. JSSC 2017 [1]

In this work, an active canceller for Frequency Division Duplex systems is presented. The cancellation signal (that is, a TX replica current) is produced by a digital-to-analog (DAC) device that is shunted at the receiver input. In the single antenna architecture, the TX and RX are connected through series stacked impedance matching transformer to the antenna. The shunted DAC at the RX secondary terminal of the transformer, which acts as a controlled current source produces the SI interference cancellation current that cancels the TX SI appearing at this RX secondary terminal. At this cancellation node, the RX port appears as virtual ground to the SI which helps to shield the RX port from large voltage swing of the leaked TX signal. The condition for the SI cancellation is set by the DAC current expressed by: $I_{DAC} = I_{TX}\frac{\pi}{2N_{turns}}$, where π depicts the phase shift of the SI signal.

The DAC is designed with a scalable hard switching differential transistors connected to a tail current source providing both mixing and data modulation. The switching is performed using the same LO of the main TX to avoid uncorrelated phase noise between the cancellation signal and the SI. However, the adaptation of the DAC for SI phase shift is performed through I/Q LO generation in which the non-ideality of the LO generation circuitry does not provide a perfect quadrature signal resulting in a limitation in the DAC phase. But, the author employs an off-chip digital predistortion to reach a 50 dB cancellation of the SI when using a 10-bit resolution DAC.

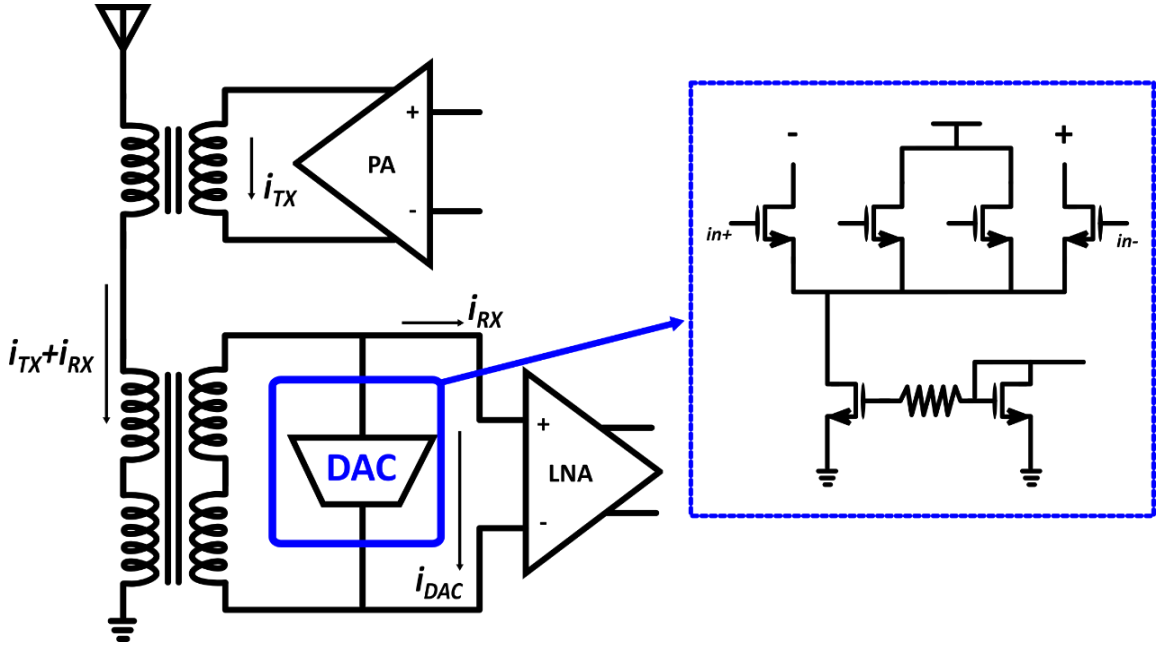

Fig. 2 2 A single antenna FDD transceiver using current DAC for SI cancellation at LNA input [1]

The receiver operates from a 2.5 V supply and the cancellation circuit (DAC) consumes a huge power (60 mW), about 60% of the total power consumed by the receiver with 1.1 dB NF degradation. The active canceller achieves a 50 dB SI cancellation with the help of an off-chip digital predistortion circuit compensating for the imperfect I/Q generation from the non-ideal on-chip LO circuitry. Also, the effective IIP3 as reported is 25 dBm with a -7 dBm leakage signal. However, the maximum SI leakage handled by the DAC is around 9.6 dBm.

The transceiver implemented with a transformer between the TX and RX provides 3 dB isolation (insertion loss) from TX to RX which depicts that the RX sees a huge SI signal corroborating why large SI replica is required to supress this leakage signal.

Yang et al. JSSC 2016 [2]

This work presents a self-Interference cancellation in a Full-Duplex transceiver where the TX and RX are operating at the same frequency and time. The paper presents a dual antenna transceiver employing a self-interference cancellation after the LNA for minimal noise penalty from the canceller. The cancellation signal is generated from the TX signal. The author considers a TX/RX isolation of 30 dB and a TX power of 20 dBm. This, thus indicates that the maximum leakage signal handled by the canceller is 0 dBm while considering a 10 dB LNA gain.

The implemented cancellation circuit consists of an attenuator acting as a voltage divider and also reverse-biased diode varactors. This is first needed to reduce the huge voltage swing from a 20 dBm TX power so as to avoid the device breakdown. Followed by the attenuator is a buffer implemented with high breakdown transistor to cope with the possible large TX output signal from the attenuator. To ensure a phase adjustment of the canceller, an I/Q generator follows the buffer to generate a quadrature differential signal and then connected to a phase shifter to guarantee the entire 360° phase is covered. The phase shifter implemented with Gm-cell, allocates different code weights to the quadrature signal which are later combined to generate the cancellation signal. The cancellation signal, which is in voltage, is later connected at the LNA output through a buffer (transconductor) to generate current cancellation signal and create a low impedance node for the cancellation.

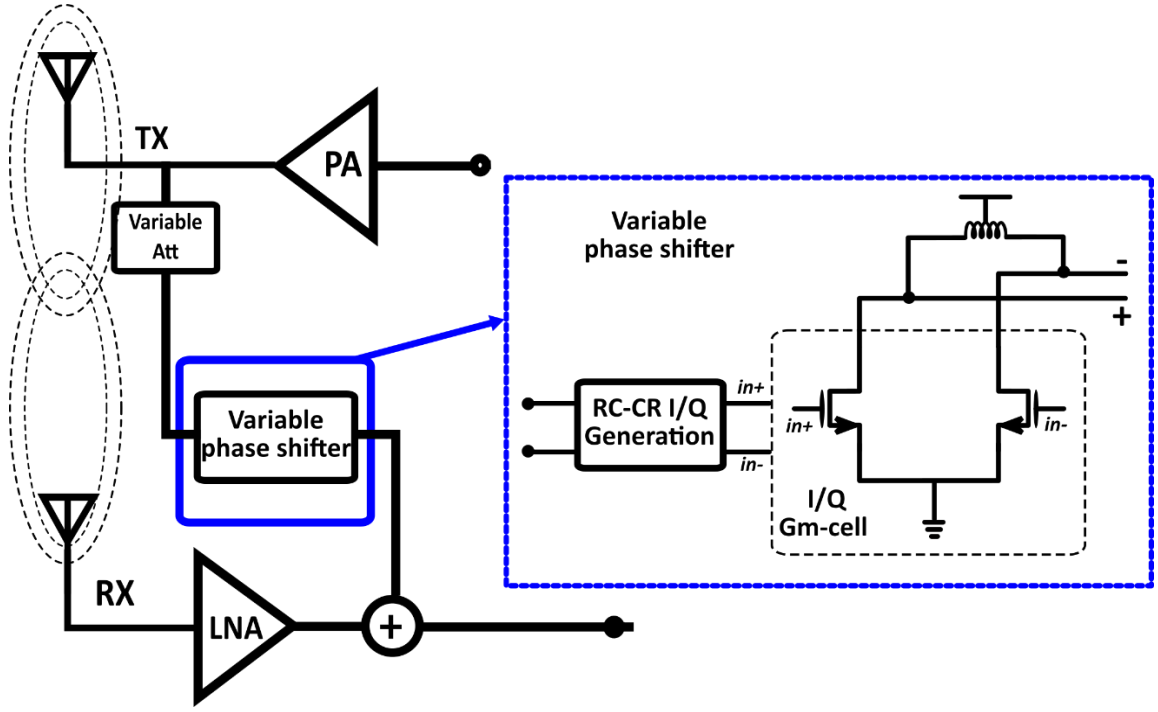

Fig. 2 3 Self-interference cancellation in a dual antenna transceiver using variable attenuators, and variable phase shifter designed from I/Q Gm-cell [2]

From the implemented system, it is noticed that the cancellation circuit occupies large area due to the buffers, attenuator, I/Q generators and the phase shifters, and the power consumption by this circuit would be a bottle neck to the chip design. However, the current drawn by the canceller was not reported but it is noticed that the entire system burns a huge power of 2W and the canceller achieves about 32 dB of SI cancellation. Since the cancellation was done after the LNA, the reported noise degradation of the canceller is around 0.6 dB.

Despite the fact that this work is targeted for Electron Paramagnetic Resonance Spectroscopy, the cancellation technique could still be applicable for mobile wireless applications.

Zhou et al. JSSC 2014 [3]

An active Self-interference cancellation embedded in a noise cancelling common gate-common source LNA in an FDD wireless receiver is presented. The work is designed for both single and dual antenna architectures. The concept of noise cancelling in CG-CS LNA is well known. The CS stage (usually a high transconductance for voltage sensing) is used to cancel the noise of the CG stage (which is used for impedance matching) when their outputs are added differentially. To fulfil the cancelling condition of the common gate noise, the condition:$g_{m,CG}R_{L,CG} = g_{m,CS}R_{L,CS}$ must be met, where the $g_{m,CG}$ is always equal to the input source conductance $1/R_s$. However, the early combination of the outputs in voltage-mode through the load resistors of the CS and CG could limit the achievable. The combination is usually done after the TIA where the currents are balance through the differential loads of each TIA branch. The author adopted this technique for the noise cancelling. The SI cancellation adapted from noise cancelling has the canceller connected to the gate of the CG device (appropriately scaled from the TX), in this way the SI is cancelled right at the input of the LNA using the same principle of noise cancelling. The condition for SI cancelling at the input is expressed as: $g_{m,CG}A_{canc} = I_{SI}$, where A_{canc} is the scaled gain of the canceller and I_{SI} is the SI signal arriving at the LNA input.

The integrated active canceller requires a phase shifter and variable Gain Amplifier (VGA). The phase shifter is adjusted to ensure the SI phase is matched while the VGA scales the TX signal for a proper replica of the SI magnitude. The canceller uses two I/Q 6-bit VGA to generate a phase rotated current signals, while an RF variable gain TIA is added to convert the current to voltage and later connected to the CG. The phase rotator VGAs are implemented with inverted-based transconductance using thick oxide device to handle large SI signal. One interesting concept about this design is that the injected noise of the canceller at the CG is cancelled right at the LNA input based on the noise cancelling concept. A second injection for TX leakage noise cancelling in the RX band is introduced at the output node of the CS.

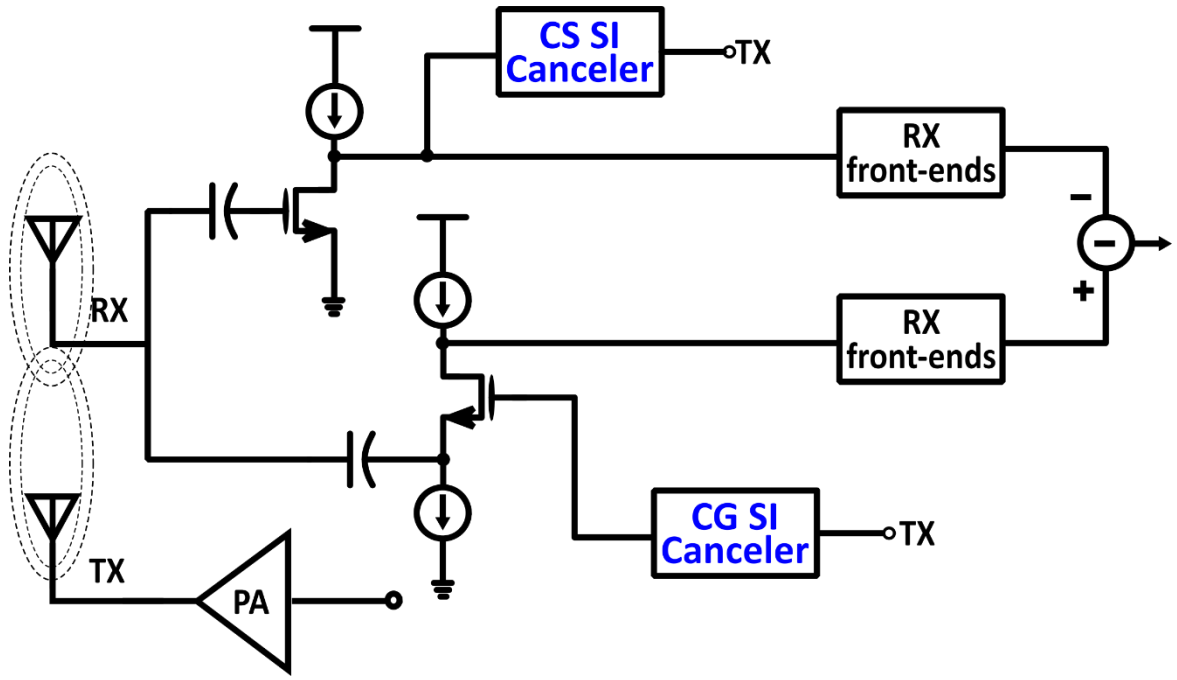

Fig. 2 4 Self-interference cancellation technique based on noise cancelling concept in a Common Gate-Common Source LNA [3]

The cancellation circuit consumes a large power (72mW) while handling a maximum SI of +2 dBm. The technique achieves a good effective IIP3 of 33 dBm (with more than 30 dB of SI cancellation) from an initial 14 dBm when the canceller is off. The noise degradation of the canceller is around 0.8 dB, indicating that the canceller noise is only partially cancelled at the LNA input due to second order nonlinearity of the CG and the CS devices.

2.4 State-of-the-Art Passive Cancellation Circuits

Zhang et al. JSSC 2015 [4]

This work describes one of the recent contributions to the SI interference cancellation techniques using passive devices for FDD radios. A four port canceller (FPC) utilizes a transformer-based RX matching network to generate the cancellation signal required for suppressing the SI. The canceller is placed between the TX and RX to augment the function of the off-chip SAW duplexer. This means that the FPC is only required to

suppress weak SI at the RX input. The input port (port 1) of the FPC connects to the off-chip duplexer while the RX signal is coupled to port 2 (LNA input) alongside the leakage TX signal. To cancel this TX self-interference, a TX replica with 180° phase shift is required. The coupling between ports 2 and 3 is accurately optimized to match the SI from port 1. Both the phase and the magnitude of the replica is scaled through a capacitor bank connecting the TX signal to port 3. Due to the limitation of the phase tuning range of the capacitor bank, another coupling from port 4 to port 3 is included. Port 4 has a varactor diode terminated to its winding to modulate the phase of the signal at port 3 thereby, extending the tuning range. The phase tuning range is given as: $Phase\ Tuning\ Range \approx \pi - \text{atan}\left(\frac{1}{Q}\right)$, where Q is the quality factor of the LC tank. The phase is thus, a function of the tank Q. To cover the entire 360°, additional switches were added in series with capacitor C2 which effectively doubles the tuning range by flipping the polarity of the coupled -TX signal.

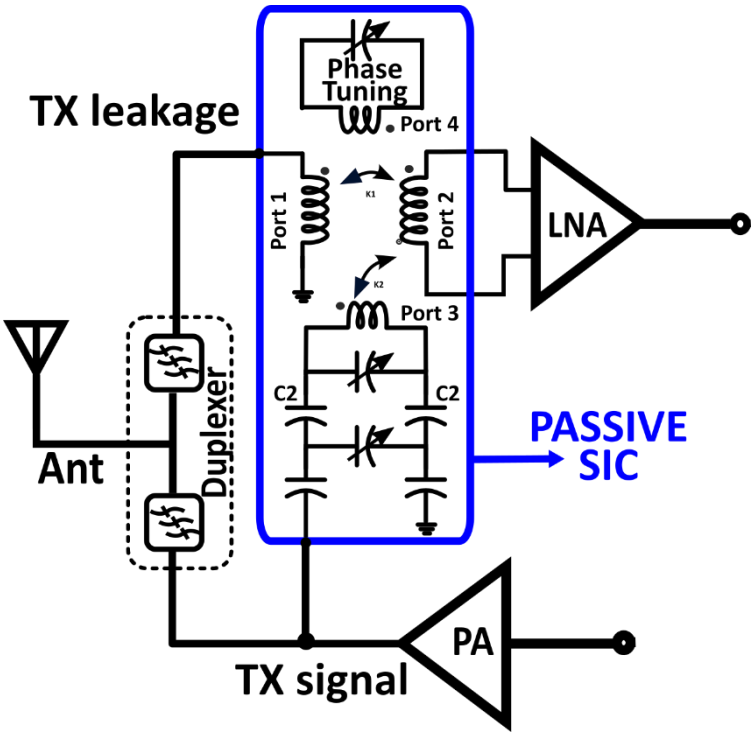

Fig. 2 5 A single antenna FDD transceiver using transformer coupling architecture for the SI canceller design [4]

The measured results from the cancellation circuits show more than 20 dB of SI cancellation over a 5 MHz bandwidth. However, the phase tuning range covered was just 50° due to the lower than expected quality factor of the transformer. Due to being passive, the cancellation circuit has little noise contribution and power consumption. The use of the off-chip duplexer for the single antenna system shows that the work motivation was not for SAW-less system. The effective IIP3 after a SI cancellation of more than 20 dB is 3 dBm.

Van den Broek et al. JSSC 2015 [5]

The ability of mixer first receivers to offer wide frequency tuneable input matching (through the frequency translation characteristics of passive mixers) and high linearity is an attractive performance for the RX but the receiver noise is always a bottleneck. The noise can however be reduced when using 25 % duty cycle LO [7]. In this paper, a mixer first receiver for full duplex radio with passive Vector Modulator (VM) Downmixer Self-interference canceller is presented. The passive vector modulator is implemented in a dual antenna mixer first receiver with a 20 dB isolation between TX and RX. The cancellation concept involves taking the cancellation signal from the TX, downmixing, phase shifting and amplitude scaling it and after performing the cancellation at the virtual ground input node of the TIA, after the main mixer.

The passive VM canceller consists of an array of linear passive mixers with phase rotator switches that inject the cancellation current at the TIA input node. It has a 5-bit resolution with minimum SI cancellation capability of 27 dB calculated by $20log_{10}(n+1)-3\,dB$, where n is the number of bit. An off-chip DAC controls the 5-bit VM, hard switched by 25 % duty cycle LO to achieve both amplitude scaling and phase shifting of the TX replica.

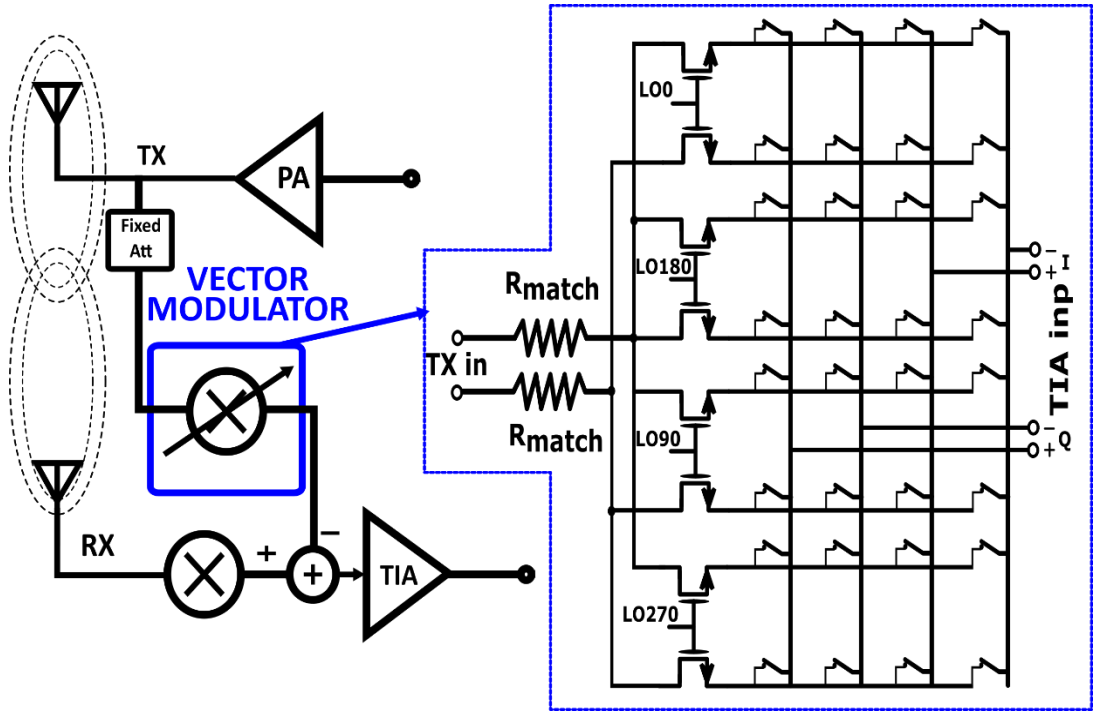

Fig. 2 6 A mixer first FD receiver using Vector Modulator Downmixer for self-interference cancellation [5]

The VM-based canceller burns up to 12 mW of power from a 1.2 V voltage supply. From the measurement results, the receiver noise degradation due to the canceller is about 6 dB. This huge degradation is also due to noise folding from the mixing action. Through the 27 dB SI cancellation over 16 MHz bandwidth, the receiver IIP3 was improved from 9 dBm to around 21 dBm. This limited improvement is due to the distortion introduced by the VM switches. However, increasing the switch size to reduce the on-resistance to reduce the switch distortion, would result in high parasitic capacitor in the switching path thereby creating a replica signal different from the SI in the main RX, which will eventually limit the SI cancellation level. This architecture is also prone to reciprocal mixing.

Luo et al, T-MTT 2016 [6]

The paper describes a tuneable N-path filters replacing the SAW filters in an FDD diversity receiver. The paper considers a 15 dB isolation from the main TX/RX and the

diversity receiver with a maximum TX power of 24 dBm. SI of 9 dBm arrived at the diversity RX and is filtered using a hybrid N-path band pass and band reject filters connected at the LNA input. The insertion loss of the hybrid N-path filter before the LNA raises the total RX noise figure.

Both the BPF and BRF are implemented with thick-gate oxide transistor switches and capacitor performing the passing of the desired signal and rejecting the coupled SI. They consist of eight paths, and LO with 12.5% duty cycle are used for the filter switching. For the BPF, the amount of out-of-band SI rejected by the filter is calculated by: $\frac{R_{SW}}{R_S+R_{SW}}$, where R_{SW} is the on-resistance of the switch and R_S is the source resistance ($= 50\ \Omega$). The BRF is further used to increase the OOB TX leakage rejection.

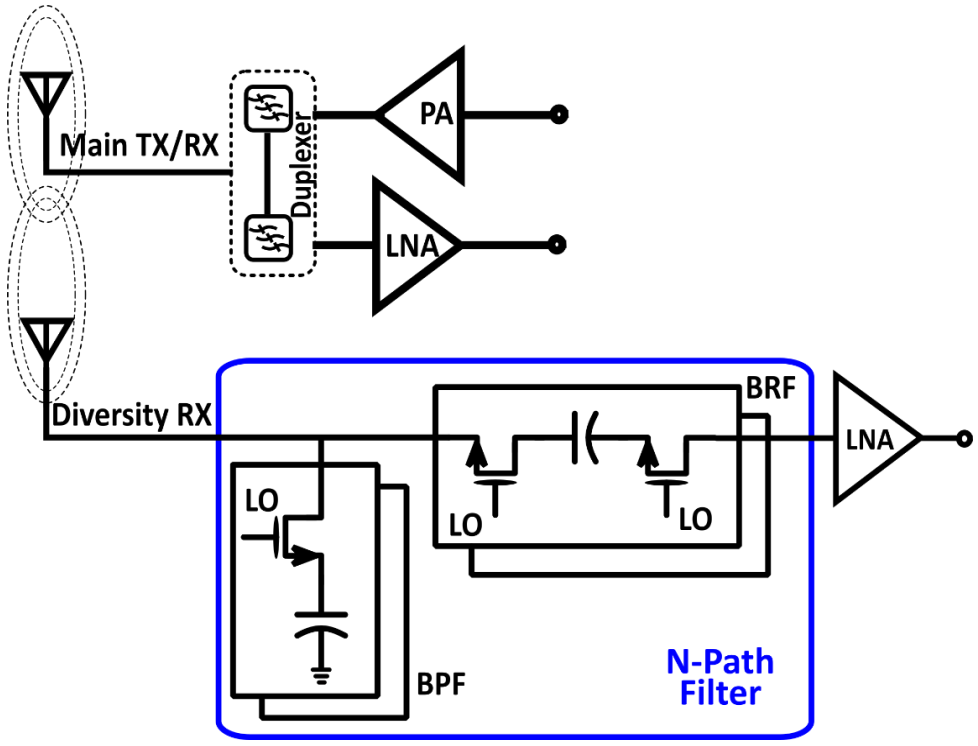

Fig. 2 7 An N-path based SI interference mitigation in a SA-less Diversity receiver [6]

This approach of filtering is only limited to FDD, because in full duplex, TX and RX are operating at the same frequency. About 40 dB of filtering was achieved by the combination of the BPF and BRF. The use of LO for the N-path switching makes it

susceptible to reciprocal mixing which would eventually degrade the RX NF. The achievable out of band IIP3 is 29 dBm, but the power consumption of the N-path filter-block is around 195 mW which makes this approach 1ess attractive for low power systems.

J. Zhou et al. ISSSC 2016 [8]

A recent applications of N-path filters for Self- Interference suppression in a full duplex radio is presented in [8]. In this single antenna work, the author was able to eliminate the insertion loss introduced through the reciprocity of the N-path filter, which is a major noise degradation factor in [6]. The author used a non-reciprocal circulator along with non-reciprocal N-path filter to avoid the 3 dB insertion loss. But, the circulator was not integrated. The non-reciprocal wave propagation was achieved using an N-path filter with ± 90° phase shift together with a $3\lambda/4$ transmission line loop with -270 phase shift. This results in destructive wave propagation in one direction and constructive in the other direction. The filter basically has a capacitor in between two switches, where one of the switches performs down-conversion and the other provides up-conversion, depending on the direction of propagation. The author combined the 15 dB isolation provided by the N-path filter-based non-reciprocal circulator and the analog baseband cancellation to achieve about 42 dB of SI cancellation over a 12 MHz bandwidth. The effective OOB IIP3 achieved is 19 dBm and the cancellation circuitry also contributes large noise in the receiver through the LO switching path due to LO reciprocal mixing. The cancellation circuit consumes 40 mW with LO path power inclusive. Despite the huge cancellation in the analog domain and the off-the-board digital cancellation, the effective IIP3 is limited and with large power consumption.

Aside the reviewed passive and active cancellation circuits, there are several other architectures that have been proposed to substitute the off-chip filters. One of the early works is the use of passive hybrid transformers (HT) [9], [10]. The HT allows to

connect transmitter and receiver to the antenna port while ensuring isolation between transmitter and receiver. The main limitation of HTs is that 3 dB of loss is incurred between the transmitter and the antenna as well as between the antenna and the receiver, degrading power efficiency and sensitivity. Furthermore, in typical HT configurations, the TX signal appears as a large common-mode signal at the LNA input due to parasitic coupling capacitors. A large common-mode leakage could saturate the LNA. The common-mode leakage could also cross-modulate with a jammer, thereby degrading the receiver linearity. The noise of the broadband common mode signal could also appear at the RX signal thereby degrading the receiver sensitivity. The author [9] proposed a differential HT that would cancel out this common mode leakage signal, but this would nearly double the power consumption and area, and additional loss from the balun (which is needed to convert the transceiver differential signal to single ended at the antenna port). In paper [10], the common mode coupling due to parasitic capacitor was addressed differently. The author relies on the LNA excellent linearity to tolerate blocker of up to -15dBm.

Another cancellation circuit using the concept of equalization, through an analog FIR filter in the RF side and another FIR filter in the baseband, was proposed in [11] for dual antenna full duplex system. The FIR filters consist in true-time-delay circuit, a buffer and a variable gain amplifier to implement the FIR filter tap. A 40MHz cancellation bandwidth was achieved with 50 dB leakage cancellation, however power consumption and noise degradation scale with the number of FIR taps.

2.5 Prior Works Summary

The challenges posed by going SAW-less in a transceiver have been addressed but not completely from each prior work as reported. A summary of the issues addressed by these researches for both passive and active self-interference cancellation techniques is given in Table 2.1. In the complete project of the proposed architecture of our

research group, all the four challenges highlighted in the table have been dealt with as it will be detailed in subsequent chapters.

Table 2. 1 Summary of the prior works

		[1] JSSC '17	[2] JSSC '16	[3] JSSC '14	[4] JSSC '15	[5] JSSC '15	[6] T-MTT '16
	Duplex scheme	FDD	FD	FDD	FDD	FD	FDD
	Architecture	Cancellation DAC	Variable Att. & Gm-cell	CG/CS LNA canceller	Transformer Coupling	BB Vector modulator	N-Path filter
		Active			Passive		
Major Challenges	Cross-modulation with OOB blocker	Marginal OOB IIP3	*na*	Marginal OOB IIP3	Low OOB IIP3	Low OOB IIP3	Low OOB IIP3
	IIP2	NO	*na*	NO	NO	NO	YES
	Reciprocal mixing with RX phase noise	NO	NO	NO	YES	NO	NO
	TX noise in RX band	NO	*na*	YES	NO	NO	YES

na- not reported in the paper

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Chapter 3

A Low-Power Active Self-Interference Cancellation Technique for SAW-less FDD and Full-Duplex Receivers

An active self-interference (SI) cancellation technique for SAW-less receiver linearity improvement is proposed. The active canceller combines programmable gain and phase in a single stage and is co-designed with a highly-linear LNA, achieving low noise and low power. A cross-modulation mechanism of the SI canceller is identified and strongly suppressed thanks to the introduction of an internal resistive feedback, enabling high effective receiver IIP3. TX leakage of up to -4dBm of power is suppressed by over 30 dB at the input of the LNA, with benefits for the entire receiver in terms of IIP3, IIP2 and reciprocal mixing. The design was done in a 40 nm CMOS technology and simulation results are reported. The system, including receiver and active SI canceller, consumes less than 25 mW of power, when the canceller is enabled it has a NF of 3.9-4.6 dB between 1.7 and 2.4 GHz and an effective IIP3 greater than 35 dBm.

3.1 Introduction

RF self-interference cancellation in a SAW-less receiver helps relax the other front-end building blocks linearity requirements, especially the LNA when SI cancellation is carried out at the LNA input. The use of active devices as highlighted in chapter 2 has the benefit of easy integration with smaller form factor and also providing cancellation signal gain. However, the linearity requirement of active canceller becomes crucial to the receiver chain design.

This chapter describes an active SI cancellation technique for a SAW-less receiver. In this work, the cancellation is designed alongside down-conversion mixers and baseband trans-impedance amplifiers (TIAs). Furthermore, an analysis of the system requirements and design details are reported. The active canceller is designed to adjust both its gain and phase to produce a signal that adds destructively to the SI signal, acting as a programmable vector modulator. The use of the SIC in the dual antenna system increases the TX-RX isolation from below 30 dB to well above 50 dB, as obtainable in a SAW-based system. This approach therefore, improves the effective receiver linearity. This chapter is organized as follows: Section 3.2 describes the system architecture and the system level requirements of the receiver chain. Section 3.3 describes the circuit implementation of the active SI canceller and the receiver chain. Section 3.4 discusses the simulation results, section 3.5 gives the performance summary while section 3.6 concludes the chapter.

3.2 System Architecture and Requirements

The proposed receiver with active SIC [1] is shown in Fig. 1. The analog RF canceller senses the TX signal from the PA and cancels out the modulated TX leakage signal at the input of the LNA. An auxiliary receive path is used to sense the broadband TX noise and cancel it out in the digital domain, as reported in [2]. The choice of cancelling the leakage signal at the LNA input relaxes the linearity requirement of the entire receiver chain, including the LNA, both in terms of IIP2 and

IIP3, and also reciprocal mixing is strongly reduced. However, the noise of the canceller is directly seen at the receiver input port and, therefore, the canceller must be designed with low noise. Cancelling the SI after the LNA, e.g. as proposed in [3], could result in LNA clipping and receiver desensitization at large SI levels. Similar considerations apply to the SI architecture proposed in [4], where SIC is carried out at baseband. Furthermore, the introduction of a down-conversion mixer in the SIC path may cause reciprocal mixing with the LO phase noise, further increasing RX noise.

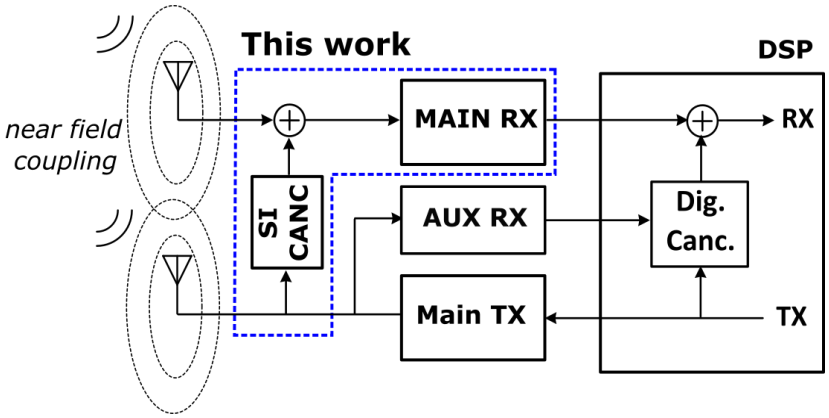


Fig. 3. 1 System block diagram

3.2.1 *Receive Chain*

3.2.1.1 Requirements for FDD

In a dual antenna mobile terminal, the isolation between TX and RX, is 20 dB to 30 dB [5]. Here we assume 25 dB TX-RX antenna isolation as a typical value. For the FDD scenario we consider as a reference 4G LTE band 2 with 20 MHz channel bandwidth [2]. With the maximum TX power of 23 dBm, the maximum TX leakage signal arriving at the RX antenna is -2 dBm. Removing external filters in front of the receiver, OOB blockers as high as -15 dBm may be present at the receiver input together with the -2 dBm TX leakage. This can cause strong in-band intermodulation if the receiver IIP3 is not sufficiently high. In the presence of a strong OOB blocker, the receiver sensitivity requirements of -92 dBm (for QPSK modulated wanted signals) may not be met [2].

Considering a signal-to-noise ratio of -1 dB for QPSK, the maximum noise/distortion level is -82 dBm. Assuming, pessimistically, that the receiver has the maximum allowed noise figure of 9.8 dB to barely meet the sensitivity requirement, the maximum third-order intermodulation level is -82.6 dBm. Hence, in the worst case, i.e. when the OOB blocker is at a frequency offset from the receiver twice the TX-RX frequency spacing, the *effective receiver IIP3 ([7])* should be larger than -2+(-15+82.6)/2= 31.8 dBm. Such a high value is nearly impossible to achieve using standard LNA design techniques and represents a challenging target even for SIC FDD receiver architectures. Assuming an RF SIC of 20 dB in front of the receiver, the receiver IIP3 requirement is decreased by the same amount to a more feasible value of 11.8 dBm. Nonetheless, the nonlinearities of the canceller are also very important and can easily become the bottleneck for the entire receiver. To illustrate this issue, we refer to Fig. 3.2.

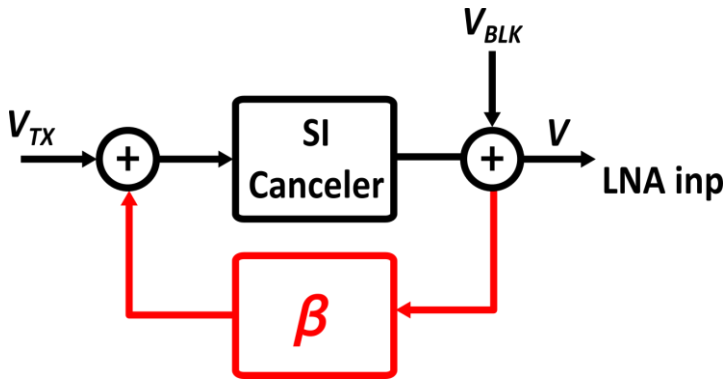


Fig. 3. 2 Canceller feedback linearization

The canceller sees the large TX signal at the input (V_{TX}) and a large blocker signal (V_{BK}) at the output. This causes two types of nonlinearities. First, due to the nonlinear canceller gain, the TX signal generates intermodulation products in the vicinity of the TX band. In FD mode, since TX and RX bands coincide, this is the main nonlinearity mechanism affecting the receiver effective IIP3. Second, due to the canceller limited reverse isolation, its output signals, including its nonlinear products, are modulated by the blocker at the canceller output (i.e. at the receiver input). This creates cross-

modulation products between the TX signal and the blocker, that degrades the SIC receiver effective IIP3 in FDD mode. We express the canceller characteristic using a Taylor series expansion as follows:

$$V_o = (\alpha_1 V_{TX} + \alpha_2 V_{TX}^2 + \alpha_3 V_{TX}^3)(1 + \lambda V_B) \quad (1)$$

assuming the TX signal is given by two tones ($V_{TX} = V_A cos(\omega_1 t) + V_A cos(\omega_2 t)$) and a CW blocker $V_{BK} = V_B cos(\omega_B t)$. The two nonlinear mechanisms described above generate two 3rd order nonlinear products: intermodulation between the TX input tones ($V_{o,IM3}$) and cross-modulation between the TX and the blocker ($V_{o,XM3}$):

$$V_{o,IM3} = (3/4)\alpha_3 V_A^3 (cos(2\omega_1 - \omega_2)t + cos(2\omega_2 - \omega_1)t) \quad (2)$$

$$V_{o,XM3} = (1/4)\alpha_2 \lambda V_A^2 V_B (cos(2\omega_1 - \omega_B)t + cos(2\omega_2 - \omega_B)t + 2cos(\omega_1 + \omega_2 - \omega_B)t) \quad (3)$$

To mitigate the cross-modulation product, which is the limiting factor in FDD mode, a feedback path (β) is introduced from the canceller output to its input. Hence, the canceller input signal becomes $V_{IN} = V_{TX} - \beta V_B$ and an additional cross-modulation term is generated:

$$V'_{o,XM3} = (1/4)\alpha_3 \beta V_A^2 V_B (cos(2\omega_1 - \omega_B)t + cos(2\omega_2 - \omega_B)t + 2cos(\omega_1 + \omega_2 - \omega_B)t) \quad (4)$$

Setting the feedback factor properly ($\beta = \lambda\alpha_2/\alpha_3$) the two cross-modulation products cancel each other: $V_{o,XM3} + V'_{o,XM3} \cong 0$. Notice that since both the canceller gain (α_1) and the feedback factor (β) are small, the loop gain is much smaller than one and hence no stability issue arises.

Requirements for FD

In full duplex transceivers, the simultaneous transmission and reception of signals at the same time and frequency makes self-interference cancellation an even greater

challenge. For this reason, FD transceivers typically target communication links over shorter distances, where lower transmitted power levels and receiver sensitivities can be tolerated. In this work we envision a dual antenna FD system with a transmitted power of 10 dBm and a sensitivity of -82 dBm. Assuming 25 dB antenna isolation, the TX leakage is -15 dBm and the total cancellation needed to have the SI below the RX sensitivity is (82-25+10=) 67 dB. The use of an RF canceller would not be able to achieve this cancellation due to nonidealities and low resolution constraints in the canceller design. Assuming 27 dB of cancellation in the RF domain, the other 40 dB would be done in digital domain (e.g. using an auxiliary path). Notice that both the TIA and the ADC must have a dynamic range (DR) greater than 40 dB. The effective receiver in-band IIP3 requirement can be computed assuming a 3 dB sensitivity degradation when the transmitted power is maximum, i.e. -15 + (-15+82)/2 = 18.5 dBm.

3.2.2 Self-interference Canceller Architecture

Prior works have proposed different ways of generating the SI cancellation signal. In [7], the SI canceller consists of a variable phase shifter followed by a PGA. Cascading the two functions degrades noise and linearity and raises the power consumption. An alternative solution to generate the cancellation signal requires the use of a passive RC-CR quadrature splitter followed by two programmable gain amplifiers [8]. A single-stage RC-CR can be used since a high precision quadrature is not required for this application. Nonetheless, the quadrature splitter loads the driving stage and increases the noise. In this work, the generation of the cancellation signal was achieved by merging the quadrature splitter with the variable gain functions. The canceller acts as two transconductors that generate and in-phase current signal (I) and a quadrature current signal (Q), as shown in Fig. 3.3. Both I and Q are generated by independently programmable transconductors. Hence, the vector sum of these currents can be set to be equal in magnitude and opposite in phase to the SI current at the receiver input.

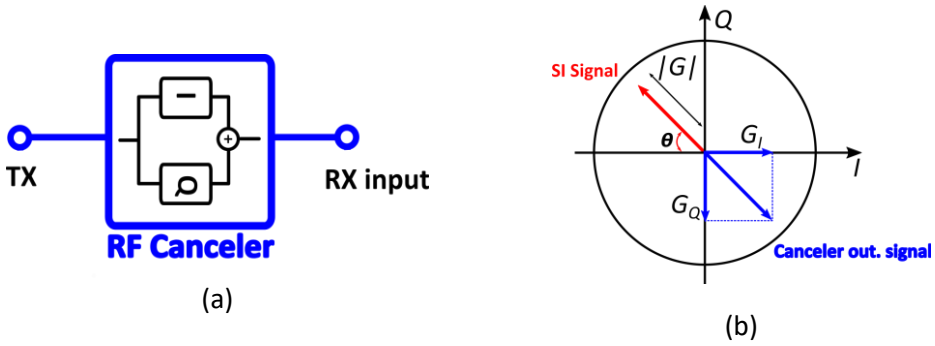


Fig. 3. 3 (a) Canceller block design concept; (b) Canceller gain adjustment

An important observation from [8] is that the quadrature precision is relaxed. In fact, assuming that the vector signals (I and Q) generated by the transconductors are not in perfect quadrature but have a phase error $\Delta\Phi$, as illustrated in Fig. 3.4.a. The result is that the sum vector will be I+Q' instead of I+Q. Since both I and Q are independently programmable, it will be possible to adjust the magnitude of I and Q' such that the desired vector is generated. However, the phase error will reduce the maximum magnitude that can be generated from A to A'=A*cos* ($\Delta\Phi$). So, if a 5% range reduction is acceptable, the maximum quadrature error will be *arccos* (0.95) =18.2°.

3.2.2.1 *Magnitude and Phase Errors on Cancellation*

The required resolution of the canceller depends on the desired cancellation level. In practice, the cancellation level is also severely limited by the frequency selectivity of the coupling between the TX and RX antennas. As shown in [9], considering a typical mobile platform size of 6 cm by 10 cm, a pair of planar inverted-F antennas, commonly used for mobile wireless applications, show a typical coupling of -20 dB and a group delay in the order of 2 nS. For a broadband canceller, this delay results in a minimum cancellation of 20 dB over a 14 MHz bandwidth. Hence, for a broadband canceller such as the one considered in this work, it is reasonable to determine the required canceller resolution based on a target cancellation level of 27 dB.

If the canceller is affected by a finite magnitude error (V_ε) and phase error (ϕ), the resulting relative cancellation error is computed as:

$$\varepsilon = -1 + cos\emptyset \pm \sqrt{\left(\frac{V_\varepsilon}{V_{SI}}\right)^2 - sin^2\emptyset}\,, \tag{5}$$

where V_{SI} is the self-interference signal, V_{canc} is the cancellation signal from the canceller, φ is the phase error, ε is the magnitude error and V_ε is the residual leakage signal. The maximum magnitude and phase errors for 20, 25 and 30 dB of cancellation are plotted in Fig 3.4.c. If a canceller architecture based on a phase shifter followed by a variable gain was chosen, the required phase and magnitude resolution for 25 dB cancellation would be 3.2° and 5.6% respectively. While the magnitude accuracy of 5.6% is easily achievable, a phase shifter with better than 3.2° resolution is not trivial. The chosen architecture based on two quadrature vectors significantly relaxes the resolution requirements. In fact, assuming each I and Q vector to be programmable with n bits, the minimum achievable cancellation level is [10]:

$$SIC_{dB} = 20log\left(\frac{2^n}{\sqrt{2}}\right) \tag{6}$$

With n=5 bits a SIC greater than 27.1 dB can be ensured.

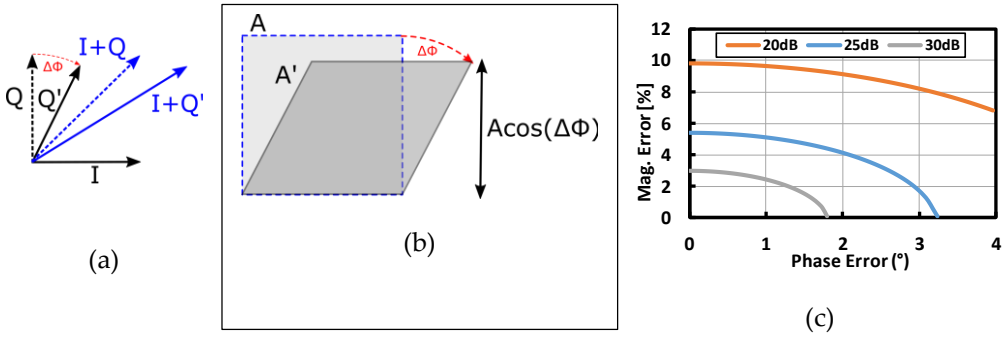


Fig. 3. 4 (a) Quadrature phase error; (b) Canceller range reduction due to quadrature phase error; (c) Cancellation in dB with corresponding output vector Magnitude and Phase error

3.3 System Implementation

The system is designed in 40 nm CMOS technology. Fig. 3.5 shows the full system which includes active self-interference canceller, LNTA, mixer and TIA.

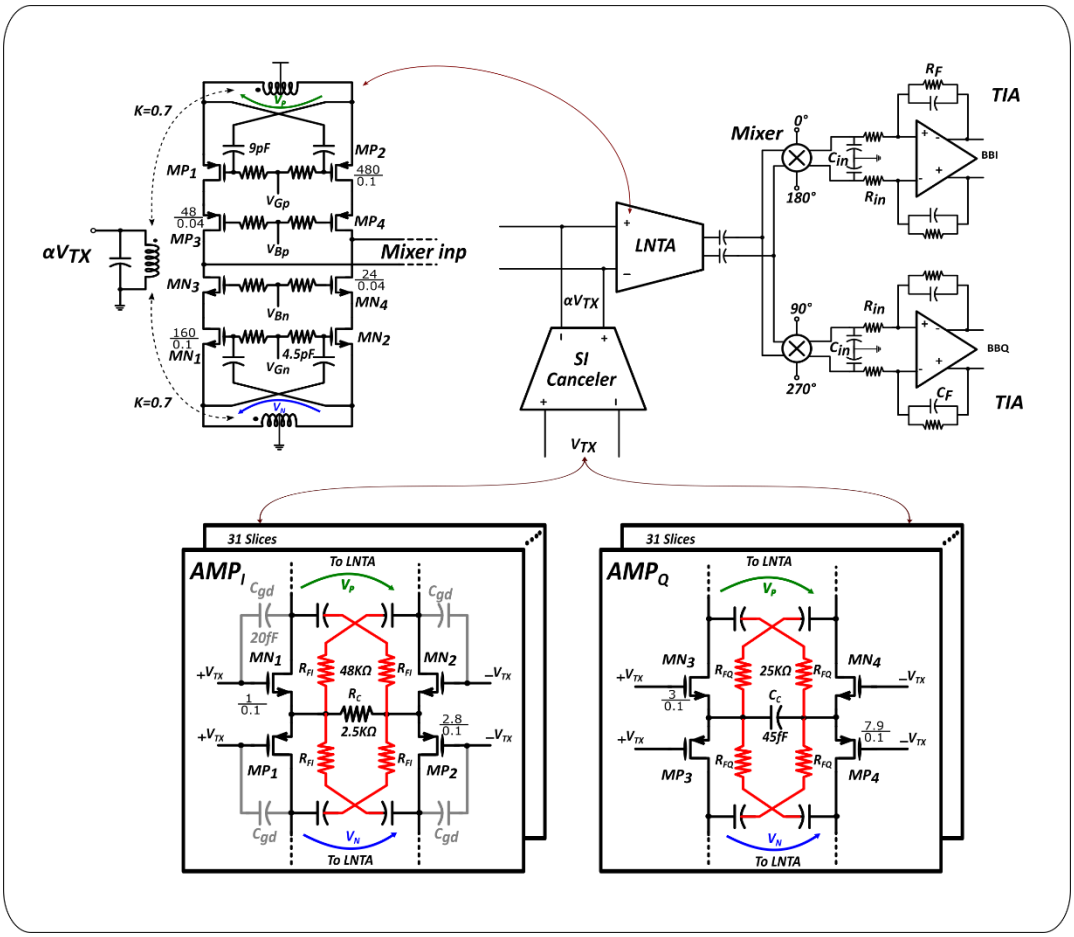


Fig. 3. 5 System architecture: Active SI canceller, LNTA, passive mixer and transimpedance filter

3.3.1 Low Noise Transconductance Amplifier (LNTA)

The LNTA, shown in Fig. 3.5, was designed based on the topology described in details in [11] and is used in this work primarily because of its low noise and high linearity. This is achieved using a transformer based complementary common-gate stage with current reuse between NMOS and PMOS input transistors working in class-AB. The three-coil transformer acts as a balun and provides a dual differential signal to the NMOS and PMOS input pairs. The cascode stages provide high output

impedance which makes it suitable for proper operation with the current-mode mixer. The main difference with respect to [11] is that the gates of the input transistors are not connected to the transformer but are simply cross-coupled. A similar approach was also followed in [12]. This allows to eliminate the external balun that was required in [11]. Cross-coupling increases significantly the immunity to common mode signals (including second-order distortion terms) at the input of the LNA since they are equally present at the gate and source of the input devices. As a result, composed second order nonlinearity, which is the dominant term in the CG LNA third-order distortion, vanishes, boosting the LNA IIP3. This allows to reduce the LNA current from 6 to 4 mA while achieving an IIP3 of around 14 dBm, as shown in Fig. 3.6.a.

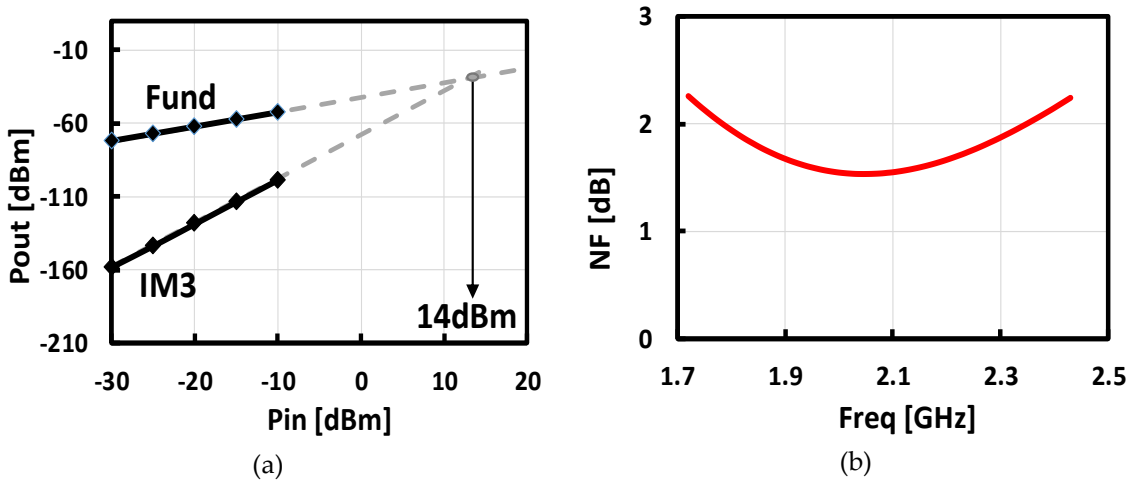


Fig. 3. 6 (a) LNA IIP3; (b) LNA NF vs RF Frequency

For the same reason, any common-mode second-order distortion term injected by the canceller is also suppressed and does not degrade the receiver IIP3. The noise figure of the LNTA is also improved thanks to cross-coupling. Neglecting transformer losses, the noise factor of the cross-coupled common gate is $NF_{CG} = 1 + \frac{\gamma}{2}$ [13]. Shown in Fig. 3 6.b is the simulated NF of the LNA, including transformer losses. It has a NF of 1.6-2.3 dB in the range between 1.7 and 2.4 GHz.

3.3.2 *Active Self-Interference Canceller*

The schematic of the proposed active SIC is shown in Fig. 3.5. It consists of two parallel transconductance amplifiers (AMP_I and AMP_Q) with independently programmable gains and quadrature output phases. To achieve the 360° phase coverage, a replica of AMP_I and AMP_Q with inverted polarities is used but only one of the two instances is active at any given time. Each transconductance amplifier consists of an array of identical elements (slices) that can be independently enabled or disabled, providing a maximum transconductance gain of 20 mS, digitally programmable with 5-bits of resolution. The cancellation current produced by these amplifiers is injected directly at the secondary of the LNTA input transformer. The canceller is designed to cancel up to -4 dBm of SI at the LNTA input and consumes a maximum of 6 mA. Each slice consists of a degenerated complementary transconductance stage. Resistive and capacitive degeneration allow to generate nearly quadrature signals. In reality, the gate drain-capacitance determines a right-hand side zero in the gain of AMP_I (G_{mI}) while the finite transistors transconductance determines a pole in the gain of AMP_Q (G_{mQ}), causing a phase deviation from ideal quadrature. The expressions of G_{mI} and G_{mQ} are:

$$Gm_I = \frac{gm_I}{1 + gm_I R_c}\left(1 - \frac{s}{\omega_Z}\right) \tag{7}$$

$$Gm_Q = \frac{sC_c}{1 + {s}/{\omega_p}} \tag{8}$$

where $\omega_z = gm_I/C'_{gd}$ and $\omega_p = gm_Q/C_c$ at the frequency of interest. ω_z is typically at a much higher frequency compared with ω_p. As a result, a significant phase error results creates a tilt in the canceller output vector constellation and reduces the covered range. Adding an explicit capacitance C_{gd} in parallel to the intrinsic gate-drain capacitance of AMP_I lowers ω_z, eventually canceling out the quadrature phase error

(phase compensation). The phase difference between AMP_I and AMP_Q before and after phase compensation is plotted in Fig. 3.7.

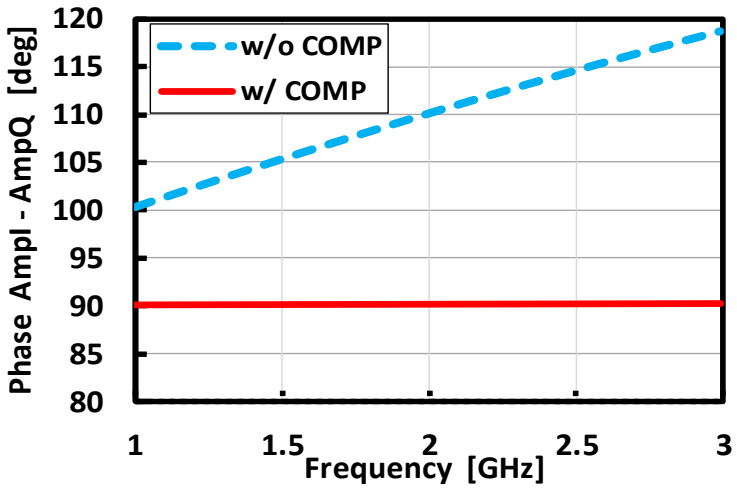


Fig. 3. 7 Quadrature error compensation

Fig. 3.8 shows the simulated normalized vector gain of the active canceller for all combinations of the control bits before and after the phase error compensation.

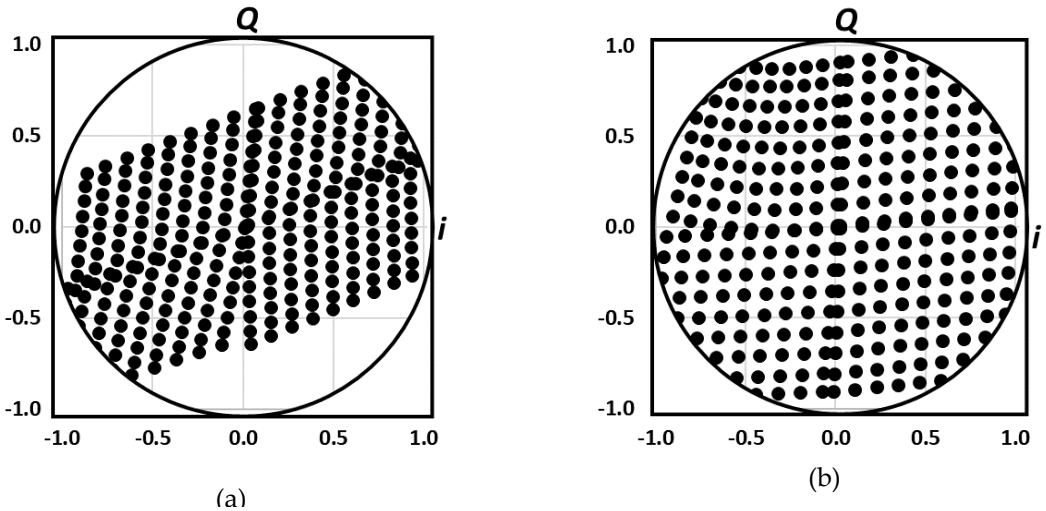


Fig. 3. 8 Canceller Constellation: (a) before compensation; (b) after compensation

3.3.2.1 *Canceller Noise Analysis*

The canceller output noise is added directly at the input of the receiver and must be kept low to achieve low overall NF. Both AMP_I and AMP_Q add noise proportionally to their transconductance, with AMP_Q contributing relatively less noise thanks to the capacitive (noiseless) degeneration. The SI signal at the receiver input determines the cancelling condition set by the magnitude (G_m) and phase (θ) of the canceller transconductance (i.e., the gain settings of AMP_I and AMP_Q). The noise current injected at the input of the LNTA from the canceller, neglecting the feedback resistors, is given as follows:

$$i_{n,canc}^2 = 8KT\gamma\left(\sigma G_{mI} + G_{mQ}\frac{\omega_o}{\omega_p}\right), \tag{9}$$

where $\sigma = \frac{\gamma+gm_IR_c}{1+gm_IR_c}\sigma = \frac{\gamma+gm_IR_c}{1+gm_IR_c}$ ($\sigma \approx 1$ for γ close to 1). The noise expression can be expressed as a function of the magnitude (G_m) and phase (θ) in relation to the self-interference signal as expressed in (10).

$$i_{n,canc}^2 = 8KT\gamma G_m f(\theta), \tag{10}$$

where $f(\theta) = \left(cos\theta + sin\theta\frac{\omega_o}{\omega_p}\right)$ is the excess noise factor accounting for the different contributions from AMP_I and AMP_Q. When AMP_Q is off $f(\theta) \approx 1$ and when AMP_I is off $f(\theta) \ll 1$. The canceller noise factor referred to its input is thus $F_{canc} = 1 + \frac{i_{n,canc}^2}{4KTR_sG_m^2}$. The noise current of the canceller referred to the input of the receiver is expressed by: $i_{n,canc,ref}^2 = 8KT(G_m + {}^1/_{R_{FI}} + {}^1/_{R_{FQ}})f(\theta)/[({}^{2n}/_{R_{LNA}})^2]$, where n is the LNA input transformer turn ratio, R_{LNA} is the differential LNA input impedance and R_{FI}, R_{FQ} are the cross coupled feedback resistances for AMPI and AMPQ respectively . For $n = 0.7$, $Gm = 20\,mS$ and $Rs = 50\,\Omega$, the maximum noise contribution to the system when AMP_I is fully ON, for $f(\theta) = 1$ is a factor of 0.58. The entire noise factor of the system is therefore $F_{TOT} = F_{RX} + G^2(F_{canc} - 1)$, where G is the canceller gain in magnitude.

Fig. 3.9 shows the simulated and calculated noise figure of the Canceller and LNA only where $NF_{LNA+Canc} = 10log_{10}[F_{LNA} + G^2(F_{canc} - 1)]$ with F_{LNA}=1.44 at 2 GHz from Fig. 3.6.b in section 3.1

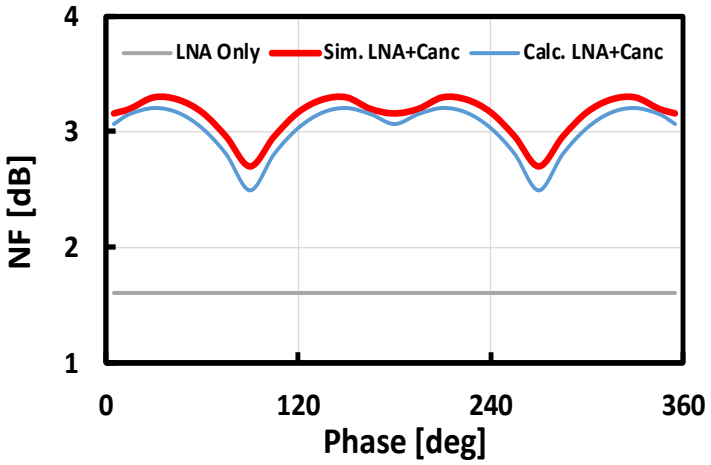


Fig. 3. 9 Noise Figure of LNA with Canceller as function of the phase shift

3.3.2.2 *Canceller linearization*

Due to the finite output conductance of the canceller transistors (MN1-4 and MP1-4), the blocker signal at the canceller output generates cross-modulation products with the TX signal, limiting the effective receiver IIP3. To address this issue, a feedback linearization technique is introduced, as anticipated in section II. The feedback resistors (R_{FI} and R_{FQ} in Fig. 3.5) are sized in such a way that a small fraction of the blocker signal appears at the AMPI and AMPQ inputs, generating intermodulation products that cancel out with the input-output cross modulation terms, improving the receiver effective IIP3. Simulation results will be reported in the next section.

3.3.3 *Baseband Trans-Impedance Amplifier (TIA)*

After the LNA, a current mode passive mixer driven by a 25% duty-cycle LO is used, followed by a baseband TIA, as shown in Fig. 3.5. The TIA has a pole at 22 MHz to attenuate large OOB interferers. The TIA is based on a three-stage operational

transconductance amplifier (OTA). The OTA design is based on the one in [14] but it has a wider bandwidth and is designed in 40 nm (versus 28 nm in [14]), which makes the design more challenging. In order to achieve wide bandwidth for better linearity instead of using Miller compensation capacitors, stability is ensured by introducing zeros both within the OTA and in the feedback network. The first stage of the TIA consists of PMOS telescopic–cascode amplifier, the second stage is a fully differential pair with both moderate gain and distortion while the third stage works as a complementary class AB, to ensure very high output voltage swing.

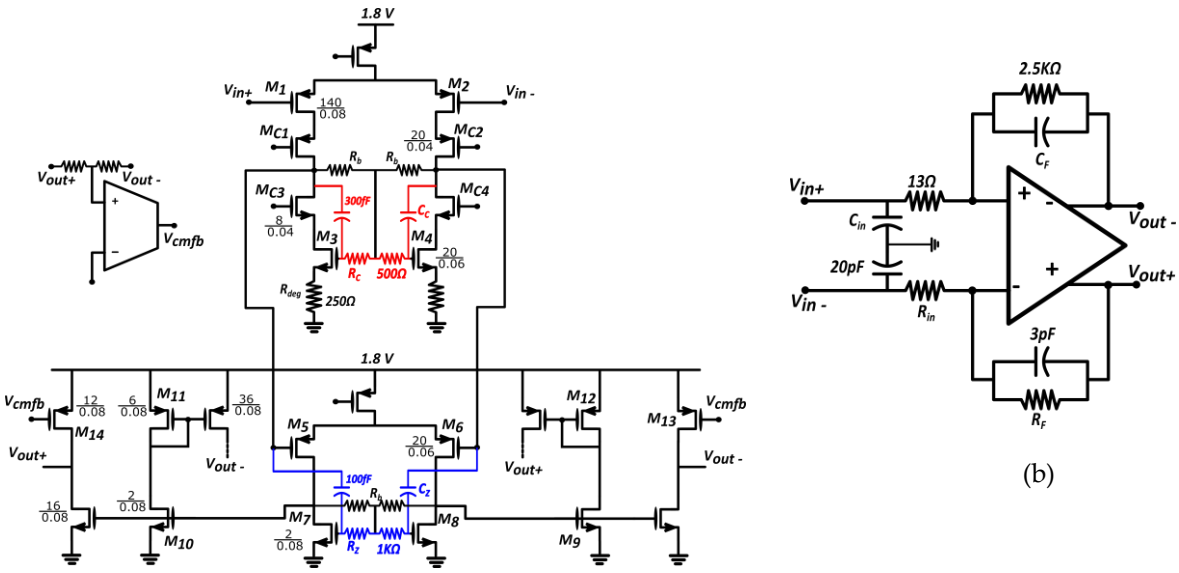


Fig. 3. 10 (a) Schematic of the 3-stage operational transconductance amplifier (OTA); (b) TIA schematic

Analysing the stability of the TIA, the following critical poles and zeros are identified. The first stage has a dominant pole, $\omega_{p,OTA,1}$ at 32 MHz and a high frequency zero, $\omega_{z,OTA,1} = 1/(R_cC_c)$. There is also a second pole at higher frequency, $\omega_{p,OTA,2} \approx G_{m,L}/C_{L,1}$ that must be well above the unity-gain loop bandwidth. To extend the bandwidth of the second stage, a feed-forward path is introduced through Rz and Cz. This gives a zero-pole doublet, in which the pole, $\omega_{p,OTA,3} = 1/(R_zC_z)$ is at twice the zero frequency and

the zero is used to cancel out the pole introduced by the second. Simultaneously, the pole of the second stage, $\omega_{p,OTA,3}$ is compensated for by the zero of the first stage $\omega_{z,OTA,1}$. A second dominant pole at 5 MHz, $\omega_{p,OTA,5}$ is created through the feedback network and the third stage at $1/(R_d//(R_F+r_o)C_{in})$, where R_F is the feedback resistor, R_d is the driving resistance of the mixer and r_o is third stage output resistance. A large C_{in} (20 pF in this design) filters out the blockers at high frequencies. With two dominant poles, the loop would not be stable. R_{in} is a small resistance placed in series with C_{in} to introduce a high frequency zero, $\omega_{z,OTA,3}$ at $1/R_{in}C_{in}$ (700 MHz), which is placed before the GBW (1.5 GHz) to ensure stability. From the loop gain simulations shown in Fig. 3.10, the loop has a DC gain of 70 dB, 1.5 GHz GBW and a phase margin of 85°. To ensure a stable DC quiescent point, a common-mode feedback circuit is introduced and its output connected to the PMOS of the last stage OTA as shown in Fig. 3.10.

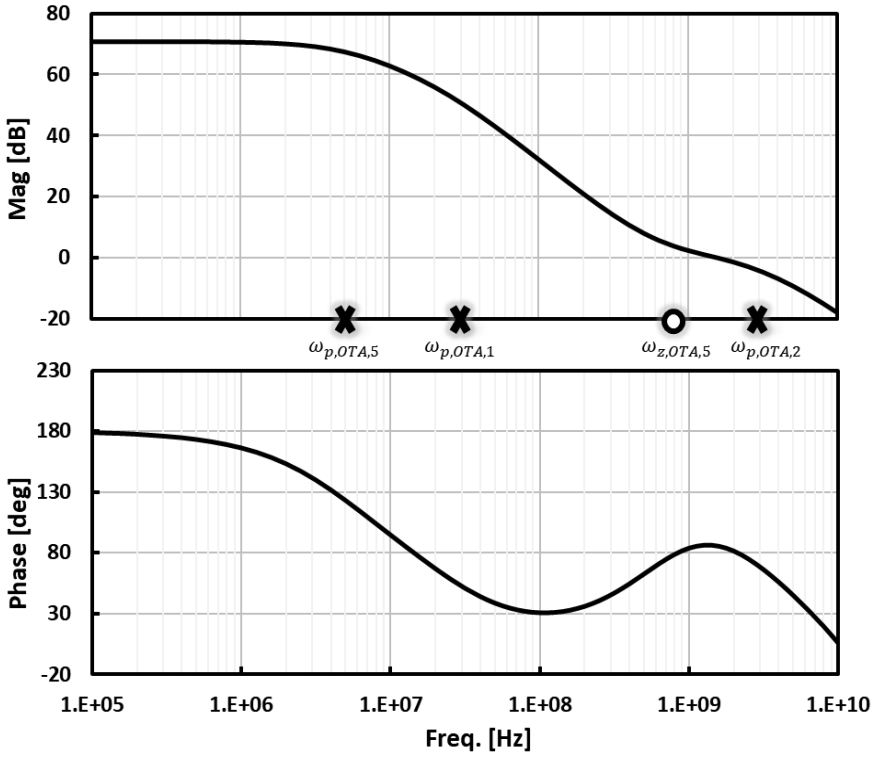
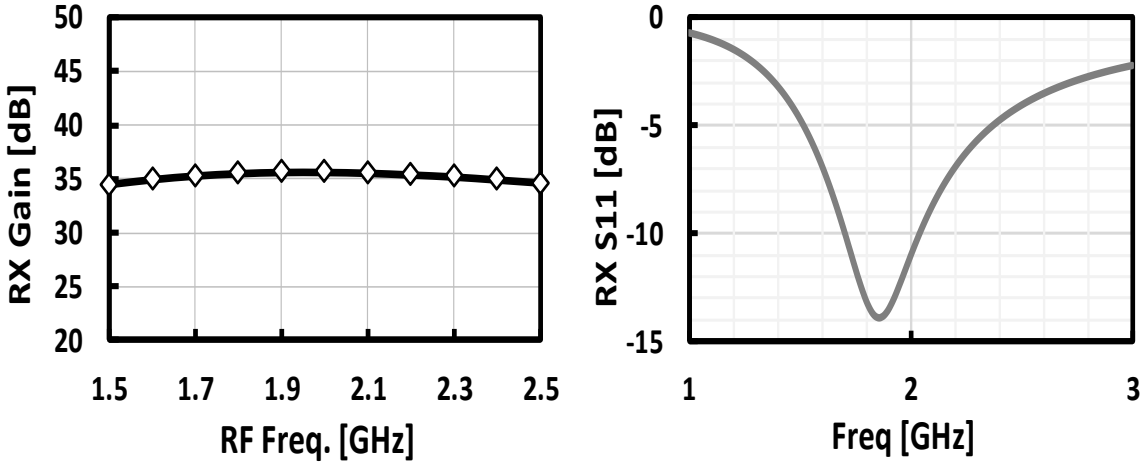


Fig. 3. 11 Loop gain Magnitude and phase of the TIA

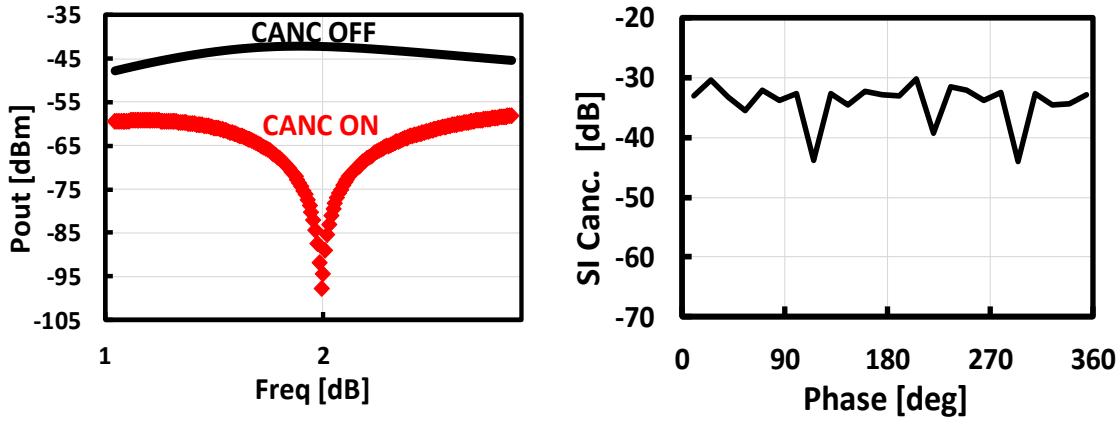
3.4 Simulation Results

The SIC receiver was designed in 40 nm CMOS technology and has a 1.8 V voltage supply. The active canceller draws a maximum current of 3 mA (AMP_I only) or 6 mA (AMP_Q only) depending on the self-interference power level and phase. The LNTA draws a current of 4 mA while the TIAs draw 1.8 mA each. The total power dissipation is 25 mW. The simulated performance of the canceller alongside the entire receiver chain is reported below. Fig. 3.12 (a) shows the simulated receiver gain ranging from 34.5 dB to 35.6 dB between 1 and 3 GHz and Fig. 3.12 (b) shows the S_{11} of the receiver simulated with the canceller off. The receiver has a -3 dB bandwidth of 22 MHz. Fig. 13.a shows cancellation of the SI versus frequency when the SI is programmed for optimum cancellation at 2 GHz. More than 30 dB of cancellation over a bandwidth of 80 MHz is achieved (no delay is introduced between TX and the SI). Fig. 13.b shows the cancellation of the SI as a function of the coupling phase over the entire 360°.



(a) (b)

Fig. 3. 12 (a) Receiver down-conversion gain; (b) Receiver impedance matching, S_{11}



(a) (b)

Fig. 3. 13 Self-interference cancellation (a) over RF frequency; (b) vs. canceller phase

The simulated receiver NF is plotted in Fig. 3.14. When the receiver NF is 4 dB, the noise contribution of the canceller is around 16%, the LNA contributes around 42% and the remaining blocks (Mixer and TIAs) 2%, as illustrated in Fig. 3.14.c. The system NF with the canceller turned off is shown in Fig. 3.14.a. The system without canceller has a NF of 3-3.7 dB in the range 1.7 to 2.4 GHz. When the canceller is turned ON, it goes from 3.9 dB to 4.5 dB as a function of the coupling phase. The pattern of the noise shown in Fig. 3.14.b is consistent with the analysis in Section 3. When AMP_I, with degenerated resistor, is turned ON more noise is generated, while when only AMP_Q is turned ON the noise decreases.

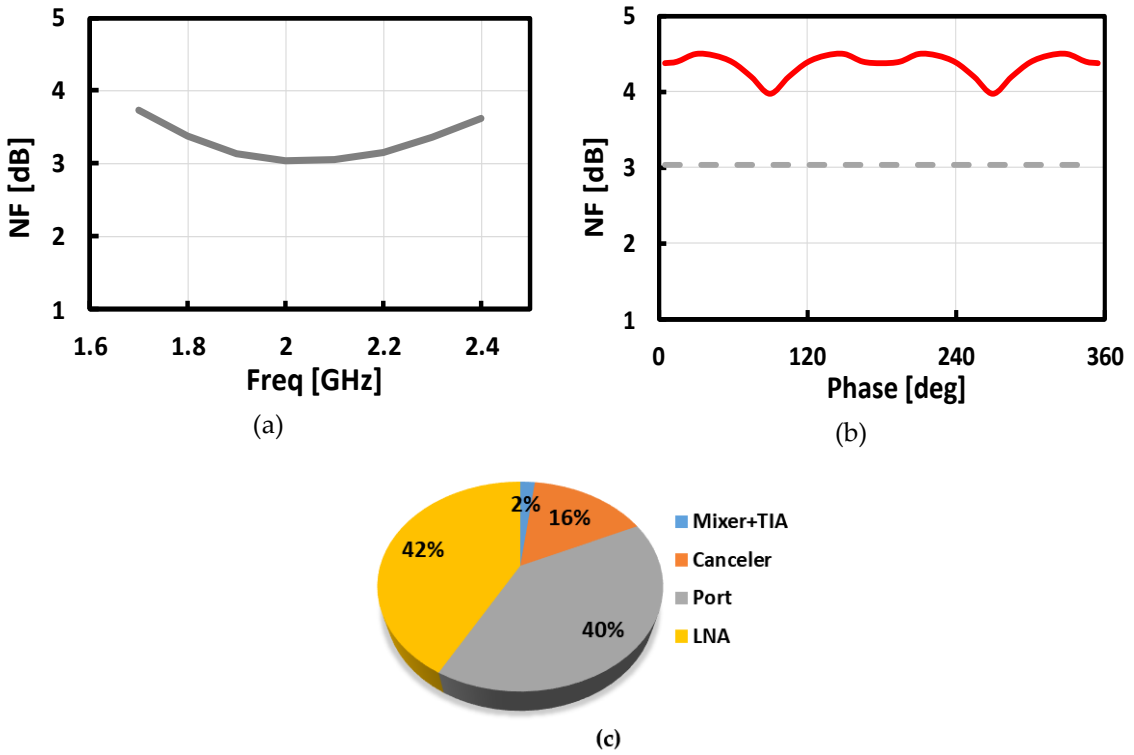
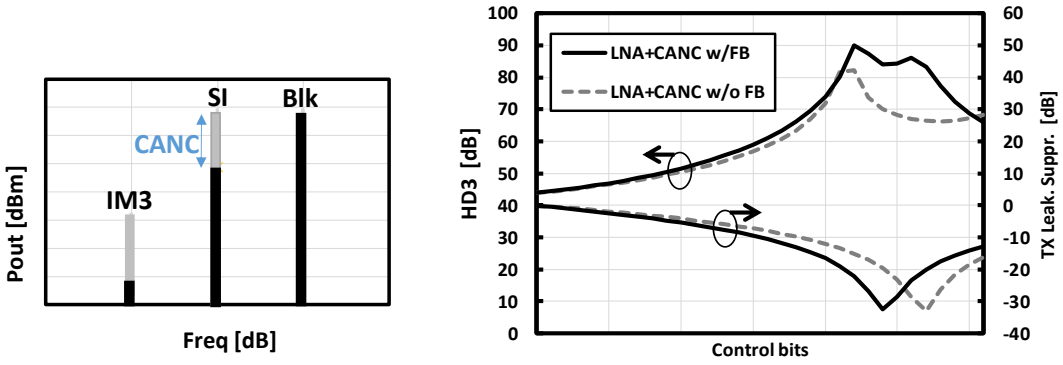


Fig. 3. 14 RX NF (a) vs input frequency; (b) with and without canceller as a function of canceller phase; (c) Noise summary of the system

Fig. 3 .15 shows the result of a two-tone test, one from the TX and one from the blocker at 100 MHz offset. The signal spectrum is shown in Fig. 3.15.a. Plotted in Fig. 3.15.b is the ratio between blocker and IM3 (HD3) as well as the TX leakage attenuation as a function of canceller gain setting for -6 dBm TX leakage at the receiver input. For the canceller without feedback resistors the peak in HD3 does not correspond to where optimum cancellation is achieved. At the point of optimum SI cancellation, the HD3 is dominated by canceller nonlinearities which is a product of the cross-modulation between the TX signal at the canceller input and the blocker at the LNA input. Adding the feedback resistors re-aligns the peak in HD3 with the peak in SI cancellation.



(a) (b)

Fig. 3. 15 Two-tone test: (a) spectrum with blocker at 10MHz offset; (b) with SI at the RX input as a function of canceller control bits

Fig. 3.16.a shows the receiver IIP3 vs the self-interference frequency for both in-band and OOB signals with the canceller disabled. The two tones f_{RF1} (TX leakage) and f_{RF2} (blocker) are swept over a range of frequencies such that the intermodulation term is constantly observed at $f_{IM3}(= 2f_{RF1} - f_{RF2})$ equal to 1 MHz and the LO is at 2 GHz. When the canceller is disabled the receiver IIP3 ranges from 4 dBm in-band to 18 dBm when f_{RF1} and f_{RF2} are placed 100 MHz and 199 MHz respectively away from the LO. The in-band IIP3 is limited by the TIA. When the canceller is enabled the receiver IIP3 ranges from 36.3 dBm in-band to 34.8 dBm OOB.

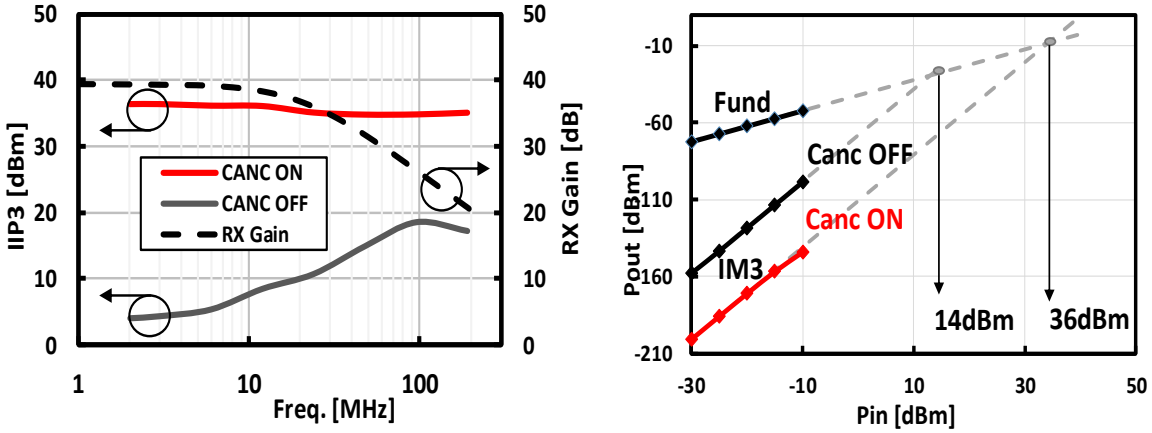


Fig. 3. 16 Receiver gain and effective IIP3 before and after cancellation: (a) vs two-tones frequency spacing; (b) vs input power for a frequency spacing of 45 MHz

The effective IIP3 improvement is strictly related to the cancellation. Ideally, for every 1 dB of SI cancellation, the effective IIP3 should improve by 1 dB, i.e. the IM3 should decrease with the square of the cancellation. In Fig. 3.17, the SI cancellation is up to 28 dB OOB. This is slightly more than the minimum cancellation of 27 dB that is guaranteed by the canceller resolution. However, it is noticed that the effective OOB IIP3 improvement is much less than the cancellation. This is due to the canceller nonlinearity, ultimately limiting the effective receiver IIP3. This is shown in Fig. 3.17, where the cancellation is varied by adjusting the canceller control bits. When the cancellation is above 18 dB the effective IIP3 remains constant, limited by the canceller intrinsic nonlinearities.

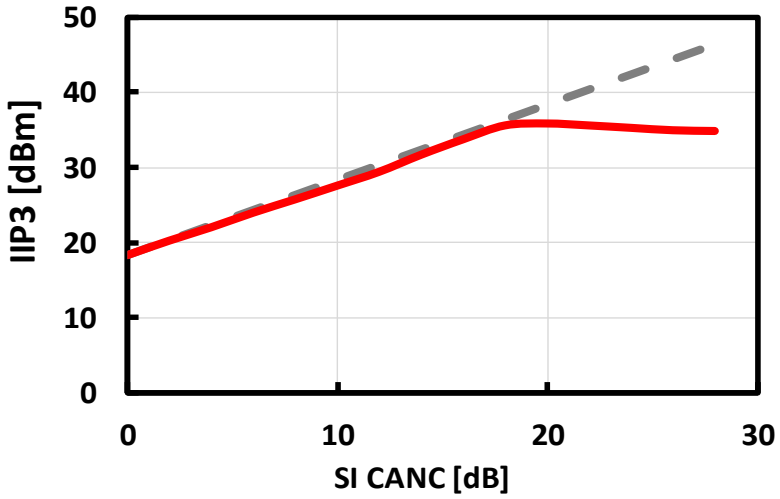


Fig. 3. 17 Effective OOB IIP3 vs SI cancellation

Additional critical system performance test that demonstrates the system full-duplex functionality is carried out by considering an in-band two-tone test with both tones applied at the canceller input, representing the TX signal. The tones are placed at 6 MHz and 10 MHz offset from the LO and the IM3 falls at 2 MHz. When the canceller is disabled the IIP3 is equal to 5.3 dBm. When the canceller is turned on and set to the proper setting for SI cancellation, the IIP3 improves to 21 dBm, as illustrated in Fig. 3.18. One interesting observation is that the output IM3 of the canceller becomes dominant at the RX input. In fact, in the SI cancellation full-duplex system, the effective receiver IIP3 is limited by the canceller IIP3 plus 3 dB, due to the LNA input transformer gain (-3 dB). The IIP3 of the canceller is thus, important and must be designed to be sufficiently high to guarantee both FDD and full-duplex operations.

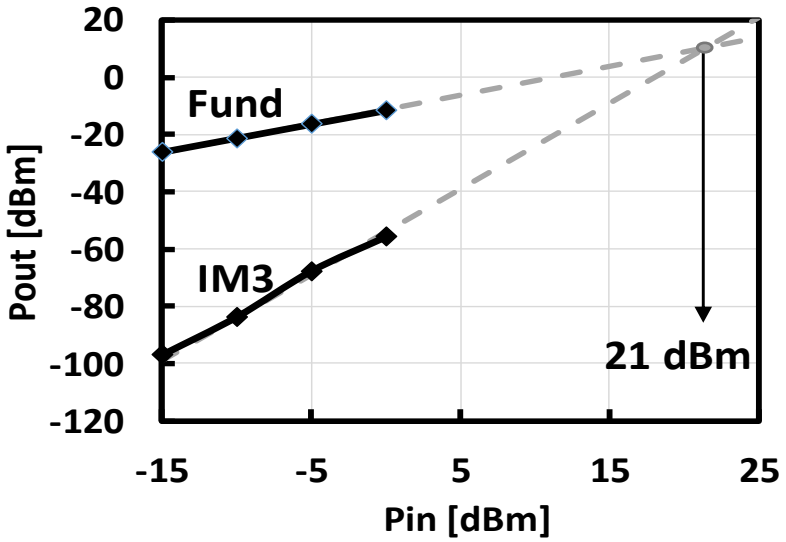


Fig. 3. 18 IIP3 with Two-tone cancellation at RX input

Another performance parameter of the receiver with the canceller is the 1 dB compression point (P_{1dB}). With the canceller disabled, the receiver, due to the presence of SI saturates, thereby desensitizing the RX signal. The 1 dB compression plot due to an in-band SI is shown in Fig. 3.19.a. The simulation is obtained with the SI placed at 10 MHz away from the carrier frequency (at 2 GHz) while the Rx signal is placed at 1 MHz offset. The in-band P_{1dB} referred to the receiver input is -23 dBm. When the canceller is turned ON, with more than 30 dB of SI cancellation, P_{1dB} is pushed to -1 dBm. For the OOB P_{1dB} evaluation, the SI is placed at 100 MHz away from the carrier frequency and the Rx signal is kept at 1 MHz. The receive signal is swept until saturation occurred at -9 dBm referred to the RX port while the canceller is disabled. When the canceller is turned on, the P_{1dB} is pushed to 7 dBm, as plotted in Fig. 3.19.b.

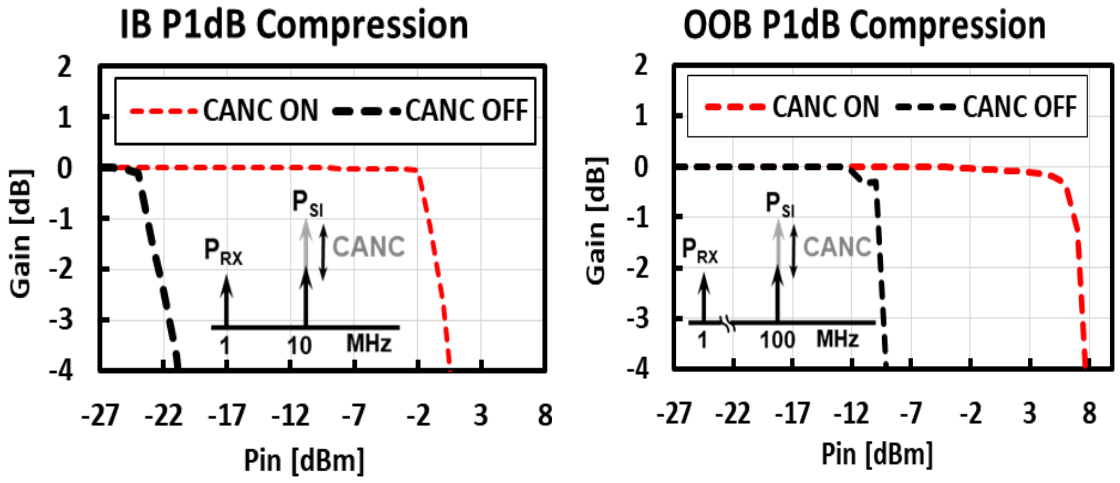


Fig. 3. 19 Receiver P1dB Compression with and without the Canceller: (a) In-band Compression at 10 MHz; (b) Out of band Compression at 100MHz as function of Input power

3.5 Performance Summary and Sate of the Art

This work is benchmarked against prior works focussing on SI cancellation for FDD and full-duplex systems [4],[7],[9] and [15] as shown in Table 3.1. The system achieves low noise figure and high effective IIP3 thanks to the improvement of the canceller cross-modulation distortion, while dissipating low power. TX leakage cancellation is performed in front of the LNA achieving more than 30 dB of cancellation over 80 MHz bandwidth. This solution addresses also the issues of receiver IIP2 and reciprocal mixing. Among prior works, only [7], which is tailored towards FDD applications, achieves similar IIP3 values and higher SI power handling capabilities. However, the TX leakage is cancelled only after down-conversion and recombination between common-gate and common-source paths, making it prone to IIP2 and reciprocal mixing. Furthermore [7] has much higher power dissipation and higher NF. However, to be fair, it must be noted that all of the other works in the table report measured results, while we are presenting only simulation results.

Table 3. 1 PERFORMANCE COMPARISON

	This work	**[7]b) JSSC Dec'14**	**[9] b) ISSCC '15**	**[15] b) ISSCC '15**	**[9] b) ISSCC '15**
FDD / FD	**FD/FDD**	**FDD**	**FDD**	**FD**	**FD**
Technology	40nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Frequency	1.5-2.5GHz	0.5-1.5GHz	0.8-1.4GHz	0.15-3.5GHz	0.8-1.4GHz
NF w/o canc	3dB	4.2-5.6dB	4.8-5.8dB	6.3dB	4.8-5.8dB
NF w/ canc	3.9-4.6dB	5-6.4dB	5.3/7dB	10.3-12.3dB	5.3/7dB
IP3 RX	14dBm	12dBm	17dBm	16.2dBm[a)]	-22dBm[a)]
Eff. IIP3	35 dBm	33dBm	27dBm	19dBm[a)]	2dBm[a)]
SI Cancellation	>30dB	30dB	20dB /25MHz	27dB	20dB /25MHz
Max TX Leak.	-4dBm	+2dBm	-8dBm	1.5dBm	-8dBm
Power	14mW RX 25mW canc	83mW RX 72mW canc	69mW RX 91mW/path	23-56mW	69mW RX 91mW/path

a) in-band IIP3;

b) measured results

3.6 Conclusions

A highly linear and low noise receiver front-end is proposed for dual antenna systems (for Full duplex and FDD) that is based on an active self-interference cancellation with a 5-bit resolution to implement an active programmable vector modulator. To meet the FD requirements, the SI cancellation can be improved in the digital domain [16]. The proposed canceller strongly attenuates the TX leakage of up to -4 dBm of power at the input of the LNA, with benefits for the entire receiver in terms of IIP3, IIP2 and reciprocal mixing. A cross-modulation mechanism of the canceller was identified and strongly suppressed thanks to resistive feedback. The effective receiver OOB IIP3 was improved from 14 dBm with the canceller disabled to 35 dBm with the canceller enabled. Compared with previous implementations lower power, lower noise and higher IIP3 with respect to self-interference was achieved.

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Chapter 4

A Low Power Wideband Receiver with an Integrated CMOS Passive Self-Interference Canceller

An integrated passive self-interference (SI) canceller co-designed with a low power wideband receiver is proposed for full duplex and FDD system. The passive canceller was designed with programmable gain and phase adjustment. The canceller output is a vector sum of the in phase and quadrature signal which is equal in magnitude and opposite in phase to the SI signal. Being passive, the Canceller contributes very low noise and low power consumption. SI of up to -2dBm of power is suppressed by over 20dB effectively improving the Rx IIP3. The canceller was designed in 28nm CMOS technology, with NF contribution of 0.5 - 0.9dB.

4.1 Introduction

The noise, distortion and power handling capability make passive devices more attractive over active devices in self-interference cancellation circuit as analyzed in chapter 2. A passive SI canceller used in a transceiver with TX power of 24 dBm to generate a SI replica needs a more careful design to achieve high effective receiver linearity without much impact of the canceller distortion. This chapter, presents a low power passive SI cancellation technique for an FD and FDD wideband receiver. In this work, the canceller is implemented together with LNA, down-conversion mixers and baseband trans-impedance amplifiers (TIAs).

This chapter is structured as follows: Section 4.2 and 4.3 describes the system level requirements and the system architecture of the receiver chain respectively. Section 4.4 describes the circuit implementation of the passive SI canceller and the LNTA while Sections 4.5 and 4.6 discuss the effect of canceller on RX input matching and noise. Section 4.7 gives a brief discussion of the Mixer and TIA and section 4.8 presents measurement results. Sections 4.9 discusses the performance comparison and section 4.10 highlights proposed design improvements. Section 4.11 concludes the chapter.

4.2 System Requirement

A passive canceller is more linear than the active canceller. In full duplex system, both the TX signal and the blocker are seen at the canceller input, thereby requiring excellent linearity at the canceller output so as not to degrade the entire system linearity. Thus, achieving high linearity with active devices is extremely challenging. As illustrated in the literature review, most published self-interference active cancellers attenuate the TX signal at the canceller input before phase and magnitude adjustment. However, with passive, the full TX power as high as 24 dBm (in LTE standards) could be applied directly to the passive canceller without linearity penalty. As analysed in chapter 3, the receiver IIP3 ($= P_{TX} - ISO + \frac{P_{blk}-IM3}{2}$) required for a dual antenna system with about

25 dB of isolation between the TX and RX is computed to be around 32 dBm for receiver IM3 level of -82 dBm when considering a TX power of 24 dBm and the IIP3 can be further relaxed by 12 dBm with 20 dB of SI cancellation. This can only be achieved with a canceller that does not contribute to the third order intermodulation distortion at the receiver input. For a full duplex system, a total of 90 dB SI cancellation is required and this cancellation level is distributed over the analog and digital domains. About 30 dB can be achieved in the analog domain with relaxed cancellation precision and the rest distributed over the digital cancellation. For a canceller to handle a TX power of 24 dBm at its input, the linearity requirement is computed as follows: In an FDD scenario, the blocker arriving at the RX input is also seen at the canceller output. From the 3GPP standard, an OOB blocker level as high as -15 dBm arrives at the RX input. The output IM3 of the canceller should be lower than that of the receiver. However, considering the receiver IM3 of -82 dBm, the referred IM3 to the canceller input is calculated as $IM3_{RX} - G_{canc}$, where G_{canc} is the canceller gain and this can also be expressed in terms of the isolation between TX and RX antennas. The canceller IIP3 is therefore:

$$IIP3_{canc} = P_{TX} + \frac{(P_{blk} - IM3) + G_{canc}|dB)}{2}. \quad (1)$$

For a canceller gain of -25 dB, the canceller input referred blocker-to-distortion ratio should be as low as 42 dBm. Therefore, the canceller IIP3 should be more than (23 + 42/2=) 44 dBm. This huge linearity requirement at the canceller input can best be achieved using passive components.

4.3 System Architecture

The system architecture considered in this project is a dual antenna transceiver similar to one of chapter 3, as shown in Fig. 4.1. It consists of a direct-conversion receiver (with LNTA, passive mixer and TIA) and a passive RF Self-interference canceller. In this architecture, the signal required for the SI cancellation is tapped directly at the TX output, and after both magnitude and phase scaling, the generated SI replica is

injected at the LNA input. This, ensures that both TX noise and SI are cancelled at the LNA input, however over a narrow band cancellation. The wideband TX noise is later cancelled in the baseband circuity through the auxiliary receiver as published in [1]. This cancellation technique using passive canceller ensures low distortion injection at RX input at full TX power of more than 20 dBm and lower noise degradation in the entire system. The relaxed receiver IIP3 without the canceller is further improved when the canceller is enabled, achieving the required effective RX IIP3.

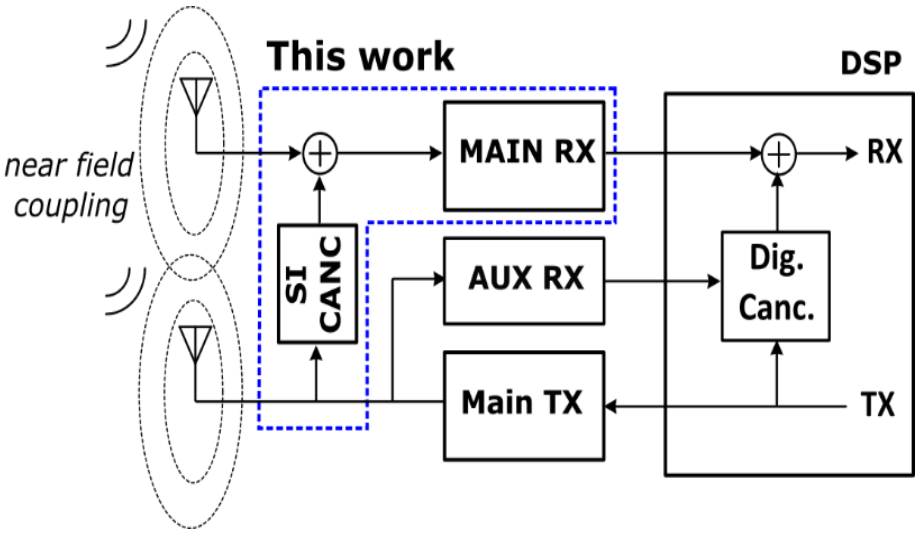


Fig. 4. 1 Block diagram of the proposed system

4.4 System Design Implementation

4.4.1 LNTA

The LNTA in [2] designed in 28 nm CMOS technology uses complementary PMOS and NMOS cross-coupled push-pull common-gates (CG) thus, ensuring a high 1-dB compression point. One of the key features of this design is the cross-coupling concept which doubles the transconductance, suppresses the MOS even-order distortion (improving the LNA IIP3) and lowers the CG noise. The design also has cascode transistors that provides large output resistance for better current mode operation, reducing loading effect of the next stage, and also providing reverse isolation. The LNA has a transformer with one primary and two secondary for the PMOS and NMOS

signal supply, with a coupling factor, k=0.7. The transformer functions as a balun, converting the single-ended signal to differential and allows a broadband source impedance boosting on the secondary. Due to the low coupling factor, the input impedance seen at the primary of the transformer has an inductive part that resonates with a series 3.2 pF capacitor. This capacitor value is chosen alongside the canceller output impedance to perform input power matching. The LNTA distortion is a function of the overdrive voltage ($V_{GS} - V_{TH}$) [3] of the CG transistors and the ratio between source and input impedance, ($1/g_m$). Source impedance boosting improves IIP3 by lowering the signal current and making distortion terms recirculate within the transistor that creates it. Similarly, when driving impedance is higher than $1/g_m$, the active device noise recirculates as well. Therefore, passive impedance boosting lowers noise and increases linearity for a given power dissipation. The LNTA schematic is shown in Fig. 4. 11. The transformer layout was optimized for minimum overall noise, considering antenna impedance of 50Ω. The simulated LNTA IIP3 is 27 dBm and its NF, including transformer losses is below 2.5 dB between 1.5 and 2.5 GHz while drawing only 8mA from 1.8 V voltage supply.

4.4.2 Canceller Design

The canceller is designed with programmable switched Resistors (R-DAC) and Capacitors (C-DAC) as in [2], thus, contributing minimal noise to the receiver chain. Both the R-DAC and C-DAC provide current signals that are in-phase and quadrature respectively to be injected directly at the LNTA input. The vector sum of these signals generates the cancellation signal, which is a replica of the SI equal in magnitude and 180° out of phase. In other words, the canceller acts as a vector modulator. The canceller with the R-DAC and C-DAC can adjust both the phase and magnitude independently, depending on the SI signal arriving at the RX input from the TX. The canceller has an input transformer that converts the TX input signal to differential and these secondary terminals can be controlled to generate signals covering 360° phase

by changing the canceller input polarity. The transformer positive secondary terminal provides an input in-phase signal to both the canceller R-DAC and C-DAC, achieving a phase coverage between 0 to 90°. The signal from the negative secondary terminal ensures phase coverage between 180° to 270°. Covering the entire 360° phase requires the use of positive signals for the R-DAC and negative signals for the C-DAC to achieve phase coverage between 90° to 180°. Interchanging the polarity between the two secondary terminals completes the entire 360° (i.e., 270°-360°) phase coverage. Transistor switches are used to achieve the switching actions. The passive canceller implementation is described in the following section.

4.4.3 The Transformer

The monolithic transformer shown in Fig. 4.2 is designed with inter-wound metal layers. In general, monolithic transformers can either be coplanar (broadside coupled) or stacked (edge coupled). The coplanar architecture achieves weak coupling between the primary and the secondary but reduces common mode coupling and thus, maximizing the quality factor, Q of both primary and secondary windings. Stacked architecture provide high coupling but with low Q if a single metal layer is used in the primary and secondary windings. Due to the high k, the stacked approach has been adopted in order to achieve maximum power transfer to the canceller. The low Q has no effect on the system noise, since the canceller noise is referred to the receiver input. Using a balun to convert the single-ended signal to differential will introduce a -3dB gain. The loss in the signal requires that the variable attenuators (for instance the R-DAC) following the balun be reduced by a factor of two thereby, contributing more noise to the system. Using a transformer with a higher transformer ratio, n will require attenuators with large impedance thus, reducing the noise contribution. However, achieving a larger transformer ratio would result in huge parasitic capacitors and large chip area. A transformer with ratio 1:2 has been adopted. This turn ratio was chosen to ensure moderate chip area and minimal noise contribution.

Being directly connected to the PA, it is important to have a transformer with very high input impedance, Z_{in} to avoid degrading the PA power efficiency. Since the canceller impedance, Z_{canc} is transformed to Z_{canc}/n^2, the transformer input impedance is further reduced and given as $Z_{in}||(Z_{canc}/n^2)$. This also shows why choosing a canceller with high impedance will be desirable.

Transformer Physical Design

The stacked 1: 2 transformer uses two metal layers, Metal 7 and AP. The former is an ultra-thick copper layer with very low resistive loss while the latter is of aluminum with higher loss but lower then to the Mx metal levels (M1-M6). The AP metal is used for the primary winding, which has three turns with width size of 12um and spacing of 4.5um. To achieve a turn ratio of 2, the secondary winding has six turns with width size of 5um each and spacing of 2um. Due to the low resistive loss of the M7, it was chosen as the secondary winding. The transformer layout is shown in Fig. 4.2(b). Electromagnetic simulation (EM) was used to characterize the transformer performance. The input primary winding has a Q of 8 and the secondary a Q of 6.

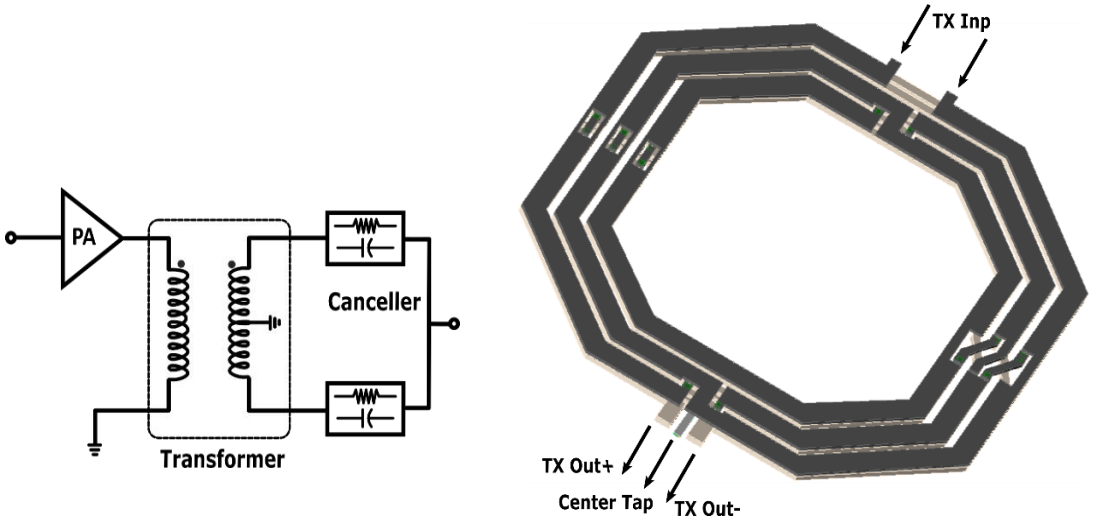


Fig. 4. 2 A 1:2 transformer for the passive canceller (a) schematic; (b) transformer layout

4.4.4 R-DAC and C-DAC

At the LNTA input where SI cancellation is carried out, the SI sees a low impedance (virtual ground) after cancellation. This condition simplifies the derivation of the canceller impedance value required for the SI cancellation. Considering the parallel combination of the R-DAC and C-DAC as a single impedance Z_{canc}, the current, I_{canc} flowing through this impedance must be equal to the SI current signal, I_{SI}. These two currents are subtracted at the LNA input and to avoid residual leakage current, the canceller (both R-DAC and C-DAC) has to have high resolution and precision. The canceller has been co-designed with the LNTA. The LNTA has a capacitor, C_{in} in series with the transformer primary winding, achieving source impedance boosting and noise matched. The choice of injecting the cancellation signal before or after the input series capacitor prompted careful analysis. One of the advantages of injecting the current after the capacitor is that, both blockers and SI would have been partially attenuated before cancellation occurs. This is beneficial since the third order intermodulation products are reduced. However, the idea of cancelling the SI after the series capacitor would further raise the noise impact of the canceller on the receiver since the attenuation through the canceller is reduced prompting a reduction in the canceller impedance value. The signal current needed for SI cancellation through the canceller impedance (R-DAC and C-DAC) are derived as follows. Considering a matched PA where the TX signal is tapped at its output and the cancelation signal injected at the LNTA input after the series capacitor, and also assuming a virtual ground for the SI signal at the LNTA input, the cancellation current I_{canc} is given as:

$$I_{canc} = \frac{2nV_{Tx}}{2Z_{canc} + n^2R_s}, \tag{2}$$

where n is the transformer ratio between primary and secondary winding, Z_{canc} is the canceller impedance, that is, the parallel combination of Resistor, R_{canc} and Capacitor, C_{canc} and Rs is source resistance (50Ω), while considering a matched TX port.

Also, the current signal of the SI arriving at the RX input for a given isolation is:

$$I_{SI} = \frac{2V_{SI}}{R_s+X_{in}} e^{i\omega_x t}, \quad (3)$$

where V_{SI} is the leakage TX signal arriving at the receive antenna with specific isolation, R_s is the Receiver antenna port impedance, the factor 2 appears since the SI sees an unmatched port at the receiver antenna side, while $\omega_x t = \theta$ is the SI phase variation between the TX and RX. For the leakage signal to be cancelled at the LNA input the condition $I_{SI} = I_{canc}$ must be met. Equating (2) and (3) gives

$$\frac{n}{\alpha} e^{-i\theta} e^{-i\left(<\tan^{-1}\frac{X_{in}}{R_S} - 90°\right)} = \frac{1}{\sqrt{R_S^2+X_{in}^2}} \left[n^2 R_s + \frac{2R_{canc}}{\sqrt{1+(\omega R_{canc}C_{canc})^2}}\right] e^{-i(<\tan^{-1}\omega R_{canc}C_{canc})}, \quad (4)$$

where $\alpha = \frac{V_{SI}}{V_{Tx}}$ (and can also be expressed in terms of the isolation, ISO (in dB) as $\alpha = 10^{-\frac{\text{ISO}}{20}}$) and $Z_{canc} = \frac{R_{canc}}{1+sR_{canc}C_{canc}}$ has be introduced in the derived equation.

Since the SI is not fixed in magnitude and phase (slow phase shifting due to near field effect), the canceller must track this slow shift in the phase of the self-interference. The value of the resistance and capacitance require to generate the SI replica for cancellation is derived from (4) and calculated by:

$$R_{canc} \approx n\frac{\sqrt{R_S^2+X_{in}^2}}{2\alpha}\sqrt{1+\tan^2(\theta-<\tan^{-1}\frac{X_{in}}{R_s}+90°)}, \quad (5)$$

$$C_{canc} = \frac{\tan(\theta-<\tan^{-1}\frac{X_{in}}{R_S}+90°)}{\omega R_{canc}}, \quad (6)$$

For a 25 dB isolation between the TX and RX $\alpha = 0.056$ and with $C_{in} = 3.6\,pF$, $R_s = 50\,\Omega$, and a zero phase shift in the SI, $\theta = 0$, the required R_{canc} for cancellation is 490 Ω for n=1while C_{canc} is calculated to be 160fF at 2 GHz.

4.4.4.1 Switch Design

The C-DAC and R-DAC have been implemented as switched capacitor and resistor respectively. They are being controlled by programmable code-words. The design of the switches becomes critical in the canceller design and its noise impact and distortion on the receiver require careful analysis.

There is a lot of research efforts in switch designs targeted for multiband wireless FDD radios [4], [5]. Some of the fundamental issues in switch design are related to its low breakdown voltage, low mobility, lossy substrate, parasitic capacitances and its junction diodes (source-body and drain-body). One of the common solutions is the use of triple N-well with resistive gate-floating and body-floating technique to ensure high power handling capability and high linearity as shown in Fig. 4.3.

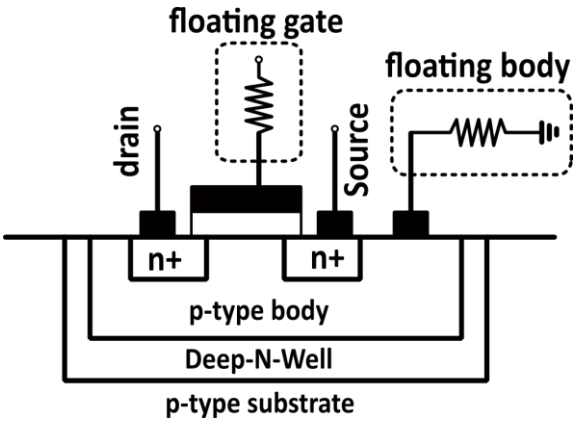


Fig. 4. 3 A simple view of NMOS in a triple-well structure with floating body and gate

In NMOS transistor, the source to body junctions are commonly reverse biased by connecting the body to a ground pad. This is not generally the case when a high voltage is observed at the source terminal. A large voltage swing can turn on the source to body junction diodes or the drain to body one therefore, creates a low impedance path. This affects the switch input impedance leading to high insertion loss and also poor power handling capability. The use of floating body technique ensures

that the input impedance of the switch remains constant by connecting a high value resistor from the body to ground. With this resistive floating body approach, at high negative voltage swing, the combination of the diode resistance and the floating body resistance still produces high input impedance value. Therefore, the only input impedance seen is that of the ON-resistance of the switch [5]. The use of deep n-well for the switch design provides better substrate isolation from the transistor body when using the body-floating resistor but creates additional p-n junction. Moreover, the deep n-well provides no parasitic bipolar junction transistors and therefore, prevents the occurrence of latch up. The floating gate resistor was also used to give an ac ground at the gate of the switch. Prior to the insertion of floating gate resistor, the parasitic gate to source and gate to drain capacitances create a low impedance path to ground leading to imbalances in the swing between source to gate and drain to gate. The use of floating gate resistor ensures the same swing effect at both the source and drain thereby mitigating any distortion generation. This idea is related to gate bootstrapping and from publications, bootstrapped devices have better linearity than direct grounded devices. In other words, this helps to maintain a zero V_{ds} and the linearity improves due to negligible gate modulation. Another technique used to improve switch linearity in an N-path filters is called bottom plate sampling. In this approach, two switches of high impedance were connected at both source and drain of the main switch. This, avoids any change in voltage between the source and drain thereby, mitigates possible distortion from the drain to source voltage swing.

In Fig. 4.4, the linearity of the switch as a function of the on resistance is illustrated with and without floating gate resistor. Since the canceller circuitry has a resistor, R_{canc} or capacitor, C_{canc} before the switch, the voltage swing of the signal is already reduced prompting flexibility in the choice of the switch on resistance. From the switch design, an on-resistance of 17 ohms was considered with minimal parasitic capacitance. Another effect observed during post layout simulation is that, the more the parasitic capacitance from the switch to ground the higher the noise contribution due to the

interconnect resistance connecting the canceller to the LNA input. The parasitic capacitor creates a noise current partition allowing the interconnect noise resistance to be seen when referring the system noise to the RX input. This observation was verified through simulation prompting the choice of higher on-resistance with corresponding lower parasitic capacitance without degrading the canceller linearity.

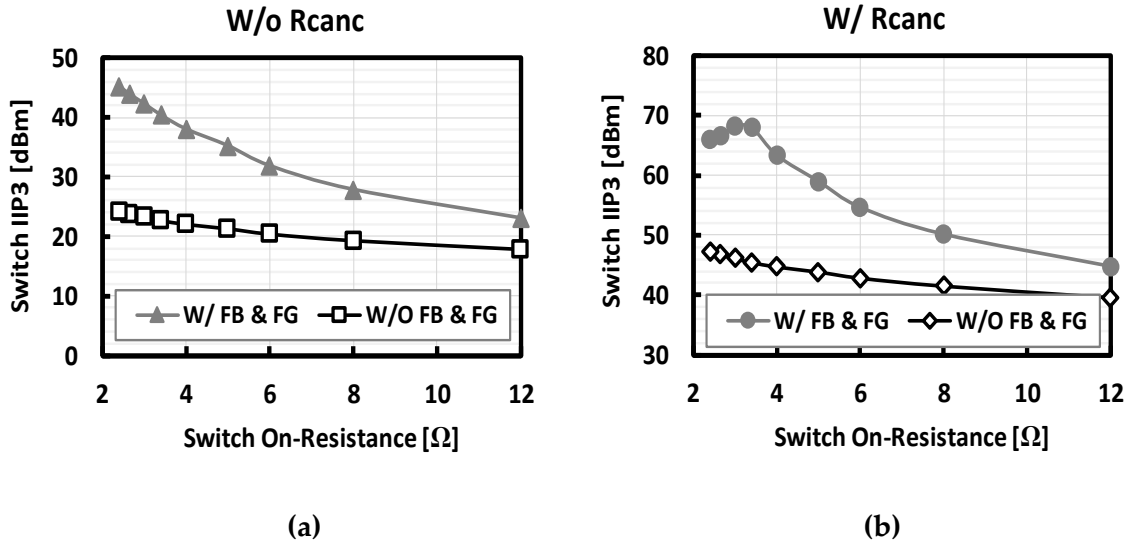


Fig. 4. 4 IIP3 of a simple NMOS transistor switch with and without floating gate and body resistors (a) without and, (b) with Rcanc= 500Ω placed in series before the switch

4.4.4.2 R-DAC Design Implementation

To cancel in-phase signals, resistor combinations are used to generate the SI replica. However, implementing the attenuator requires careful design considerations. A ladder resistor approach as shown in Fig. 4.5 was chosen to give small form factor for a 5-bit resolution. With 5-bit resolution, more than 27 dB of SI cancellation could be achieved as reported in chapter 3. The ladder R-DAC has the most significant bit (MSB) controlled by b0 and the least significant bit (LSB) by b4. When all the bits (b0 –b4) are high, that is, all switches are ON, gives the minimum resistance value and when all are off, give infinite attenuation assuming parasitic capacitors are neglected. The switching of the ladder branches for a specified bit code gives the required current to cancel out the self-interference signal. Each unit canceller resistor, *R* is 500 ohm.

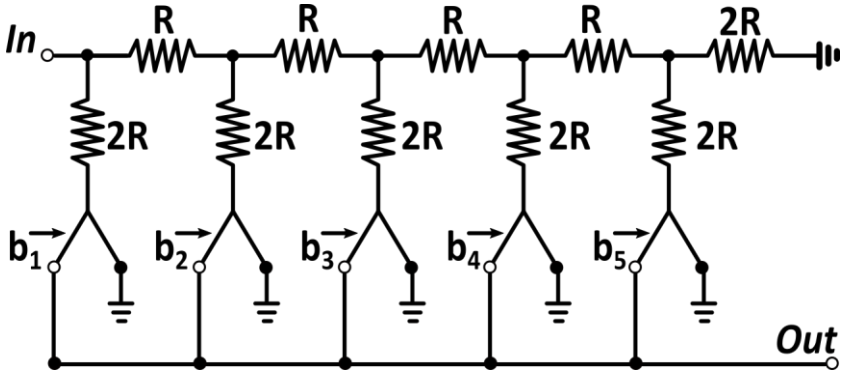


Fig. 4. 5 R-DAC implemented in a resistor ladder architecture

The resistor was chosen based on linearity simulation of different available resistors in 28 nm technology library. "LP_CMOM" resistor was chosen based on its high linearity. The resistor model obtained from TSMC CMOS design rule manual is defined as: $R(T,V) = R_0(1 + TC1\ \delta T + TC2\ \delta T^2)\ (1 + VC1\ \delta(V/L)\ + VC2\ \delta(V/L)^2)$, where R_0 is the nominal resistance value at $25°C$. The interesting thing about this equation is the third term product is a function of the voltage and the length of the resistor. To minimize the distortion of the resistor as a function of the voltage across it, its length L has to be large enough to bring this third term product to approximately 1. The longer the length L, the more linear is the resistor. However, the longer the length, L the larger the parasitic capacitance. In the optimized layout design with minimal parasitic capacitance, a unit resistance corresponding to $5K\ ohm$ was chosen. Ten $5K\ ohm$ were put together in parallel to achieve the unit resistance, R of $500\ ohm$.

4.4.4.3 Implementation of C-DAC

The C-DAC implementation was also considered as ladder architecture for simplicity and small form factor and to maintain a symmetrical structure with the R-DAC for easy switching. A 5-bit resolution achieves more than 27 dB cancellation when a full quadrature signal is required. The MSB is denoted by b0 and b4 is the LSB which gives the least cancellation current. For a unit resistor of 500Ω in the R-DAC, the unit capacitance is approximately 160fF. This small capacitance value does seem critical to

achieve with a small parasitic capacitance in the layout. The parasitic capacitance could be reduced when one avoids using lower metals layers for the capacitor layout. The farther the bottom plate to the substrate, the less the parasitic capacitance introduced. But, this does not come without the penalty of increasing the total metal plate resistance since higher metals have more resistive losses. In the layout, the bottom plate has three metal layers of the Mx- metals stacked together to reduce the resistive loss and it was ensured that the bottom plate is far from the substrate by avoiding the use of Metal 1 and 2. The C-DAC ladder structure is shown in Fig. 4.6.

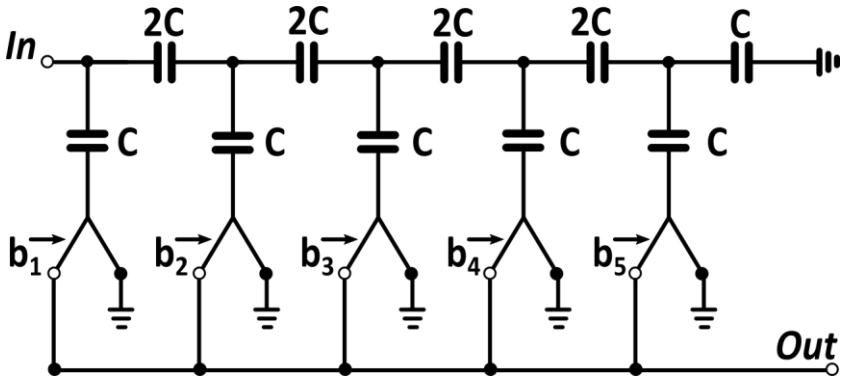


Fig. 4. 6 C-DAC implemented in a capacitor ladder architecture

The selection of the bits in both the R-DAC and C-DAC thus, provides a total of 1024 constellation points with a 5-bit resolution in a single quadrant (that is, covering a phase shift of 0° to 90°). To achieve a total phase shift coverage of 360°, the transformer shown in Fig. 4.2 is used to provide a differential TX signal. To cover the second quadrant, the C-DAC is connected to the positive secondary terminal and the R -DAC connected to the negative terminal ensuring a phase coverage from 90° to 180°. Changing between these terminals helps cover the entire 360° phase needed to track the phase changing of the SI.

In the final implementation, two parallel switches are connected to each ladder branch. For instance, in the MSB of the R-DAC, the codes controlling the switches are termed $bI0$ and $\overline{bI0}$ respectively. When bI0 is low (zero), the switch is turned off and to avoid leaving the branch floating, the second parallel switch with the bit, $\overline{bI0}$ sweeps the not needed current signal to ground. This approach does not only help maintaining constant signal division but also (1) prevents the large signal across the gate-source of the main switch from turning it on when should be off and (2) prevents the turning on of the reversed junction diode in the MOS switch through large negative signals. The canceller, comprising the R-DAC, C-DAC and the transformer was simulated to characterize its linearity. The simulation plot illustrated in Fig. 4.7 shows 49 dBm of IIP3 indicating that, it should not introduce any degradation to the receiver effective linearity.

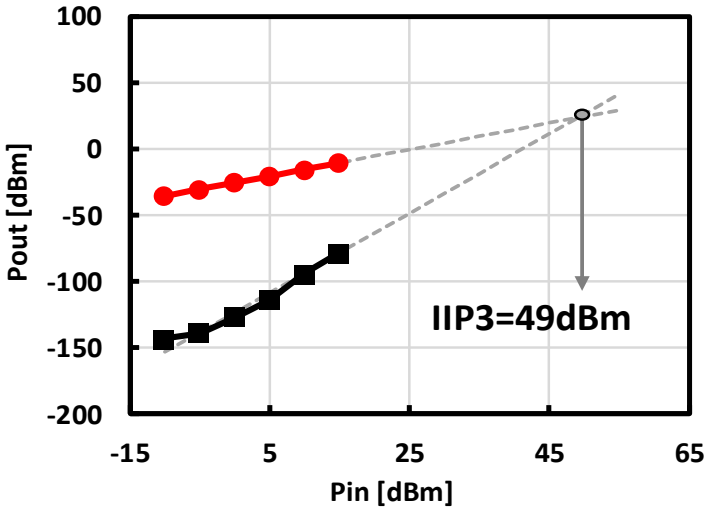


Fig. 4. 7 Simulated IIP3 of the passive canceller

However, during measurement it was discovered that the linearity of the canceller degraded through a bondwire connecting one of the ladder branch switches to ground. In the layout, both the transformer the secondary center-tap, and the second parallel switches of both R-DAC and C-DAC were connected together to a single pad-ground and later connected to the board ground through a bonding wire. The switch

thus, sees a finite impedance to ground producing a voltage swing at its output node. This voltage results in cross modulation which degrades not only the canceller linearity but the system effective linearity as it will be shown in the measurement results section. This effect also degrades the canceller constellation as unequal signal strength was observed in each of the quadrant. Through simulation, the effect of this bonding wire was demonstrated. It was also observed that connecting the canceller ground to the LNA ground would have mitigated this effect. Fig. 4.8 shows the canceller constellation simulated for a bond wire ground inductance of 1 nH, 2 nH and also using the LNA ground.

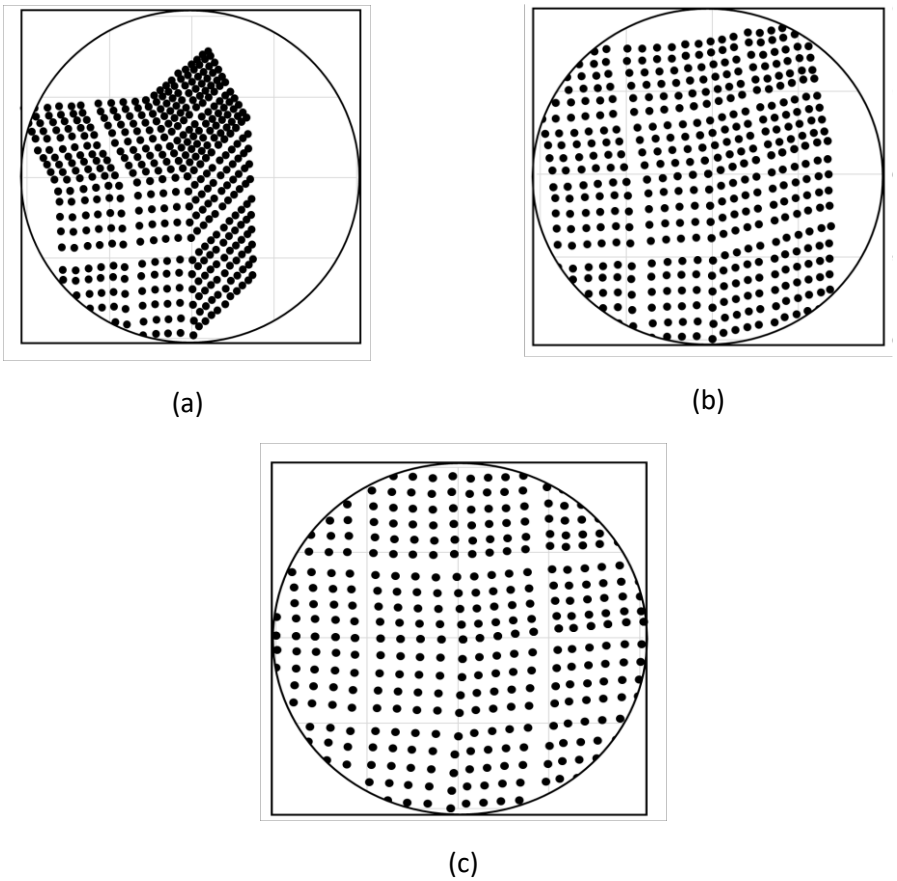
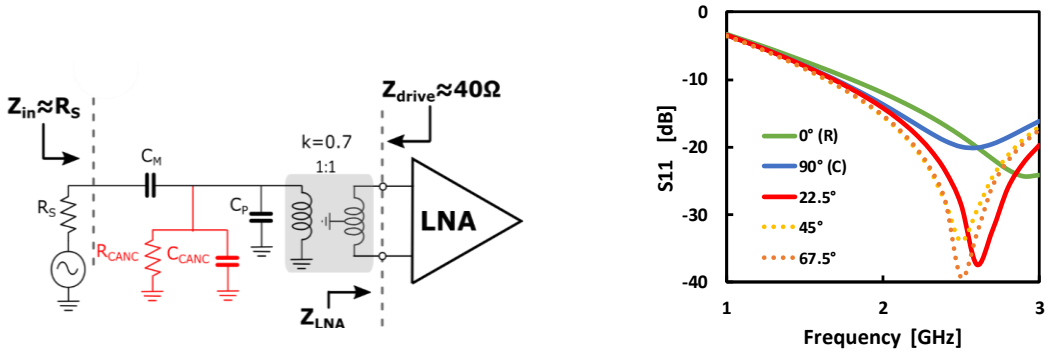


Fig. 4. 8 Simulated canceller normalized gain (a) bondwire inductance of 2nH; (b) bondwire inductance of 1nH; (c) LNA ground (about 0.2nH)

4.5 RX Matching Consideration

The suppression of the self-interference signal at the LNA input relaxes the LNA linearity requirement. The output impedance of the canceller seen at the input of the LNA changes the LNA matching property. The co-designing of the canceller with the LNA ensures that the input power matching is maintained for various configurations of the canceller as shown in Fig. 4.9 (b). However, when only the R-DAC is enabled, with total resistance of 500 Ω, the parallel combination with the Z_{drive} of 40 Ω still gives a driving impedance value that is a little below its initial value. The S_{11} is degraded but the matching is still below -10 dB between 1.8 GHz and 3 GHz as illustrated.



(a) (b)

Fig. 4. 9 (a) Receiver input impedance model with the canceller connected at LNA input; (b) simulated S11 for different canceller configuration based on self-interference phase shift

4.6 Passive Canceller Noise Analysis

In the design of transceiver building blocks, the noise of each block must be considered to avoid degrading the noise of the chain. The most critical of the blocks is the LNA because its noise is seen directly at the receiver input without being scaled by any gain. The same also applies to the canceller, since SI cancellation is done at the LNA input. The noise contributed by the canceller to the receiver noise factor, F_{RX} is given below:

$$F_{Sys} = F_{RX} + (R_s^2 + X_{in}^2)\left[\frac{1}{(R_{canc}+R_{sw})*R_s}\right], \quad (7)$$

where X_{in} is the reactance of the series capacitor at the input of the LNA, R_{canc} is the canceller resistance value which is a function of SI phase shift as derived in (5), R_{sw} is the on-resistance of the switches, R_s is the driving source impedance. From the derivation of the R_{canc}, it is seen that the lower the input capacitance to the LNA, the higher the R_{canc}. Since the reactance of the capacitor is squared as given in (7), the lower the capacitance value, the more the noise contributed by the canceller to the receiver. A capacitor value of 3.2 pF chosen does ensures minimum noise contribution. The noise simulation of the LNA with the canceller is illustrated in Fig. 4.10. When the SI experiences no phase shift, only the R-DAC is required to generate the SI replica and the noise of the canceller comes from the resistors and switches. On the other hand, at a quadrature SI phase shift, only the C-DAC is required and the canceller noise comes from the switches. This explains why the noise injection varies with the SI phase shift as shown in the plot. The LNA only has a NF of 2 dB, with the canceller enabled, the noise varies between 2.5 dB and 3 dB over the enter self-interference phase shift.

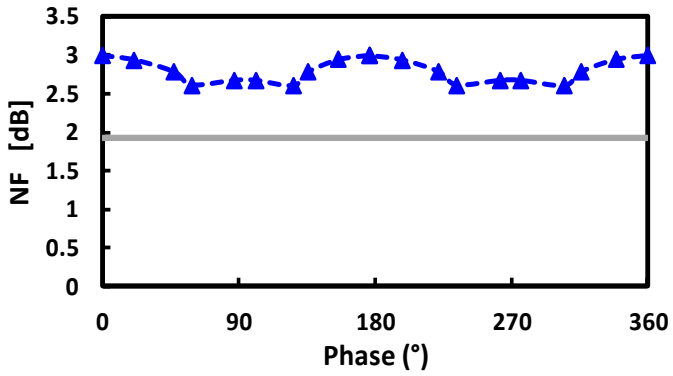


Fig. 4. 10 Canceller noise figure with the LNA only as a function of the self-interference phase shift

4.7 Mixer and TIA

The LNTA in the down-conversion receiver drives two I/Q 25% duty cycle current passive mixers followed by a TIA with a real pole at 20MHz (Fig. 4.11 (b)) providing a first order low pass filtering. The TIA, with three-stage operational amplifier is compensated for by exploiting passive feedback network to achieve wide bandwidth and low power [6]. At the output of the mixer, 20pF capacitors connected to ground provide low OOB impedance. 12Ω resistors in series with these capacitors create a zero in the loop gain, improving stability. The TIA is similar to the TIA described in chapter 3 [6] but this is implemented in 28 nm CMOS technology. The small increase in the in-band input impedance has almost no effect on the in-band IIP3.

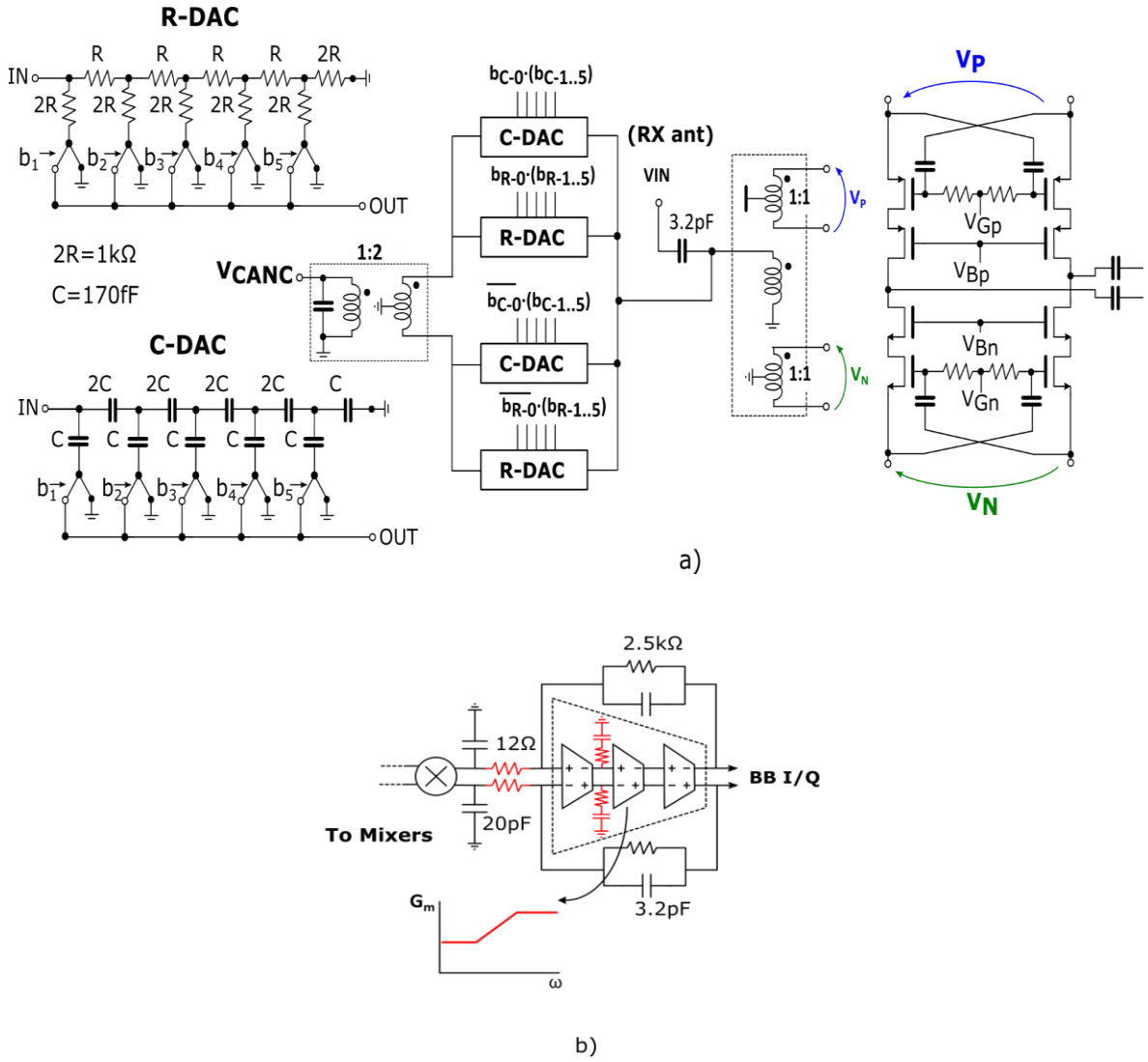


Fig. 4. 11 Receiver front-end with SI cancellation: (a) RF section, (b) baseband section

4.8 Measured Results

The system is implemented in 28 nm CMOS TSMC technology. A chip photo is shown in Fig. 4.12 and the area is shown in Table 1. The passive canceller in particular, occupies an active area of 0.16 mm^2. The chip is wire bonded and mounted on a PCB. This section describes the measured performance of the prototype for both FDD and FD operations with test set up shown in Fig. 4.13.

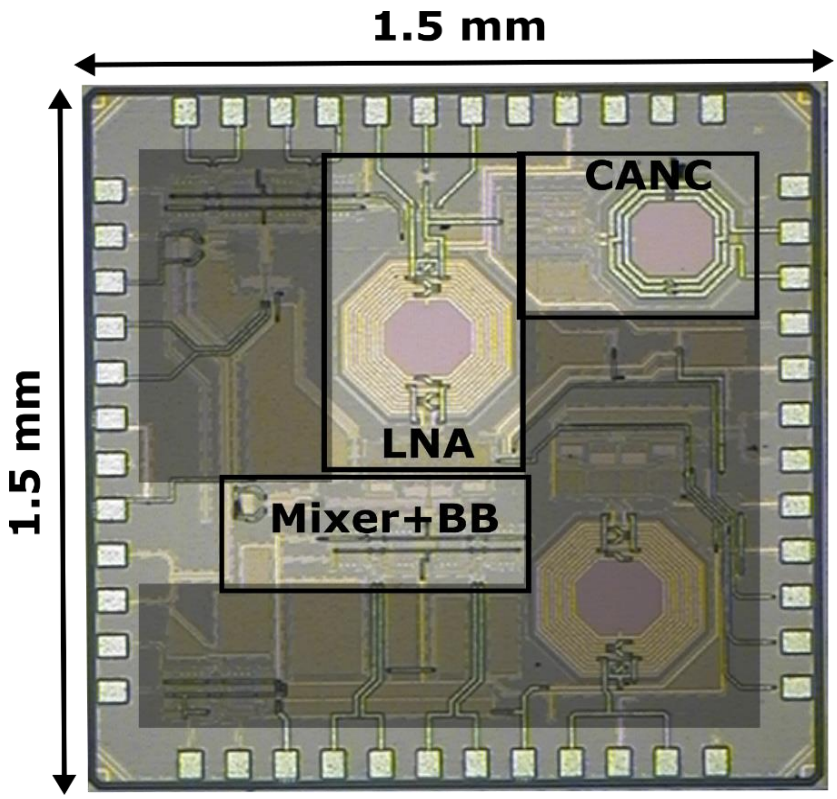


Fig. 4. 12 Chip micrograph of the 28 nm Receiver with Passive self-interference canceller

Table 4. 1 ACTIVE AREA OF THE RECEIVER WITH CANCELLER

Blocks	Active Area
Canceller	0.16 mm^2
LNA	0.34 mm^2
Mixer + TIA	0.1 mm^2
Total Active Area	0.5 mm^2

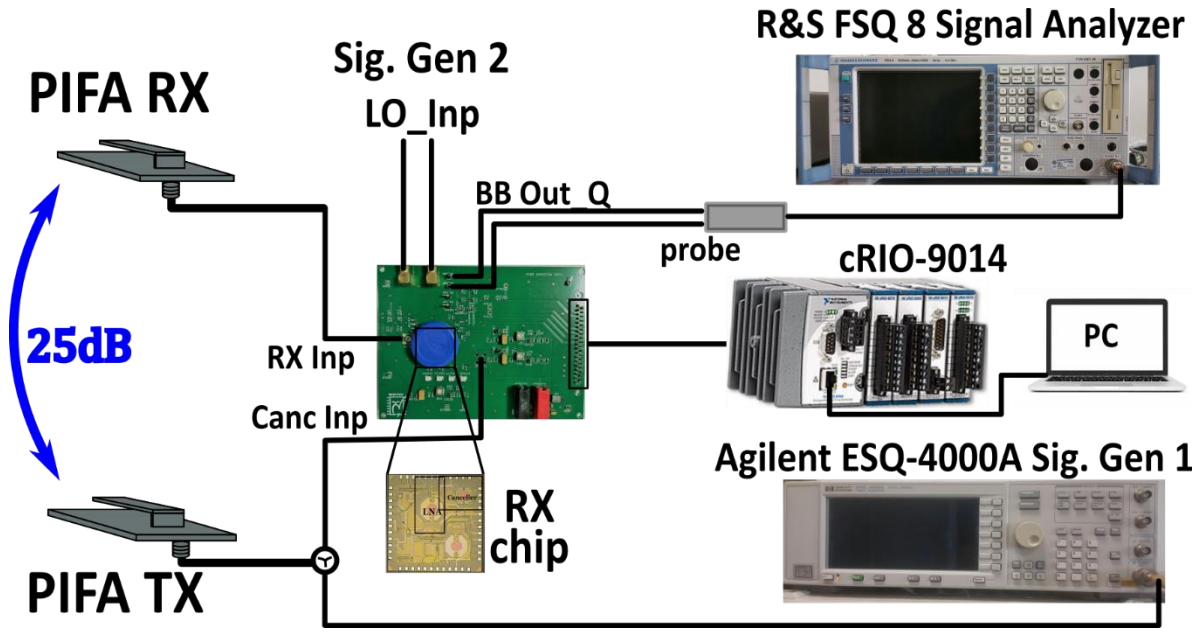


Fig. 4. 13 A test bench setup of the RX test chip using Planar Inverted-F antennas (PIFAs) with 25 dB of isolation between the TX and RX for validating the Self-interference cancellation at the RX input.

4.8.1 Passive Canceller

The characterization of the canceller is carried out using a Vector Network Analyzer (VNA). Since the integrated canceller has its output connected to the LNA input, the canceller transmission (S_{21}) is observed at the receiver input port. The measured gain is -20 dB at 2GHz when either the R-DAC or C-DAC fully on. The normalized vector-gain for all configurations of the bit for both DACs is reported in Fig. 4.14. For a 5-bit resolution, 1024 constellation points are available in each quadrant but the measured result is only reported for 81 constellation points per quadrant. The chip incudes a shift register that outputs the code-words needed to control the R-DAC and C-DAC, and also some other building blocks in the chip design. In Fig. 4.14, the Constellation distortion is traced back to signal un-balancing caused by the large balun centre-tap ground inductance introduced through the bondwire.

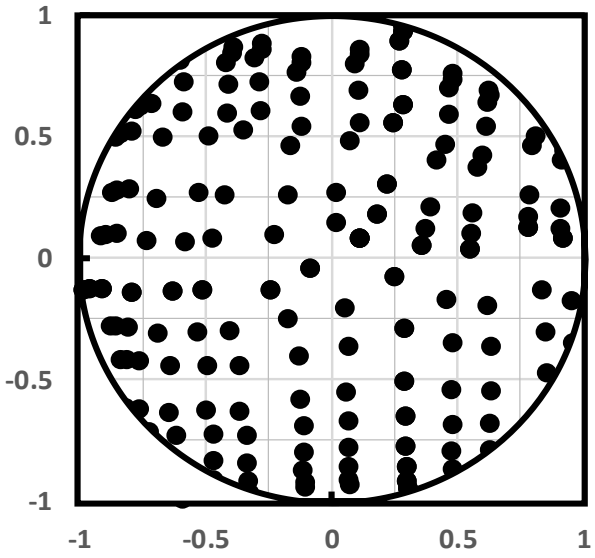


Fig. 4. 14 Canceller normalized vector gain

4.8.2 Receiver Chain

The receiver consumes 25 mW from 1.8 V power supply. Fig. 4.15 (a) shows the measured and simulated receiver gain ranging from 32.8 dB to 34.9 dB between 1.2 and 3 GHz and Fig. 4.15 (b) shows the S_{11} of the receiver measured with a VNA when the canceller is off. The receiver has a -3 dB BW of 20 MHz. The receiver noise is measured using the Rohde & Schwarz FSQ8 signal analyzer and the double sideband noise figure is 4.6 dB at 2 GHz and the NF varies from 4 to 5.4 dB between 1.2 and 2.5 GHz as shown in Fig. 4.16. Both NF and gain measurement are carried out with a probe for better accuracy and the results obtained are in good agreement with the simulation. A two-tone test is carried out using two HP ESG-4000A signal generators to determine the linearity of the receiver. The IB IIP3 in Fig. 4.17 (a) is 8 dBm with the tones placed at 10 MHz and 19 MHz offset from the LO frequency at 2 GHz. Also, the OOB IIP3 measured result is 18 dBm with the tones placed at 100 MHz and 199 MHz offset from the LO as plotted in Fig. 4.17 (b). Both the IM3 of the IB and OOB fall in-band at 1MHz during the linearity tests.

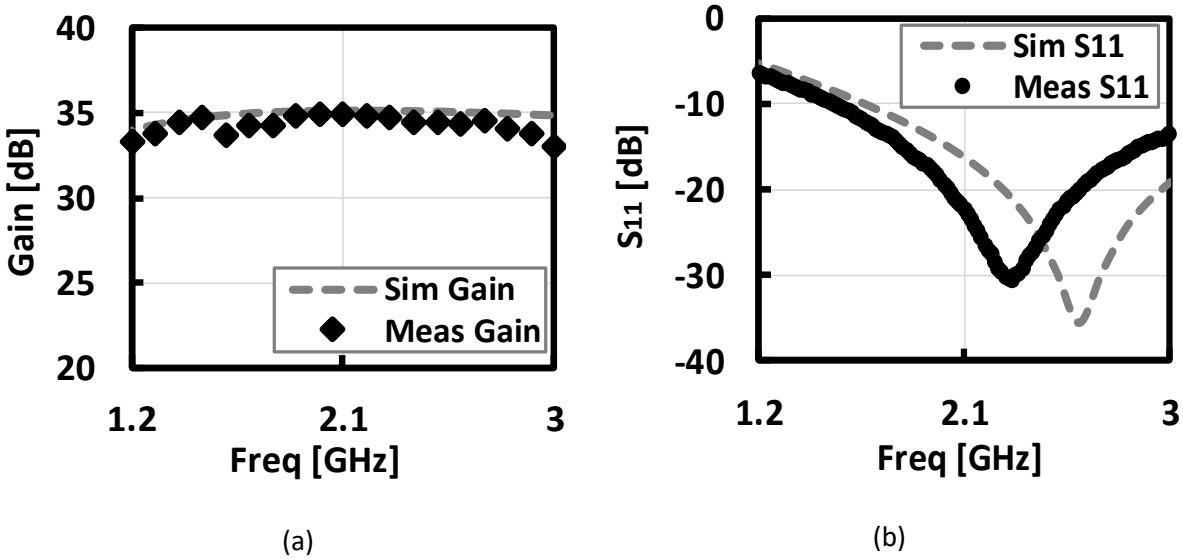


Fig. 4. 15 (a) Receiver down-conversion gain; (b) Receiver impedance matching, S_{11}

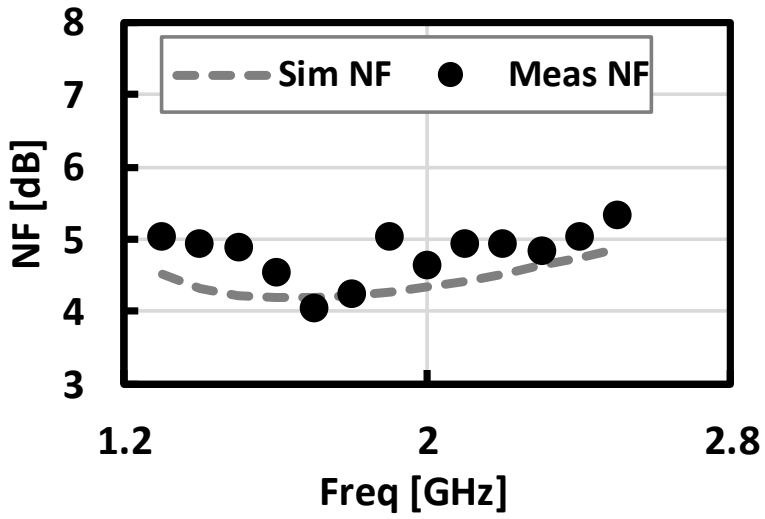


Fig. 4. 16 Receiver NF vs input frequency

The OOB IIP3, which is limited by the TIA, is almost 3 dB lower than the simulation results as shown in Fig. 4.18 and varies less than 1 dB from 1.3 to 2.5 GHz. For the P1 dB, the receiver compresses at -15 dBm and 0 dBm for the IB and OOB respectively.

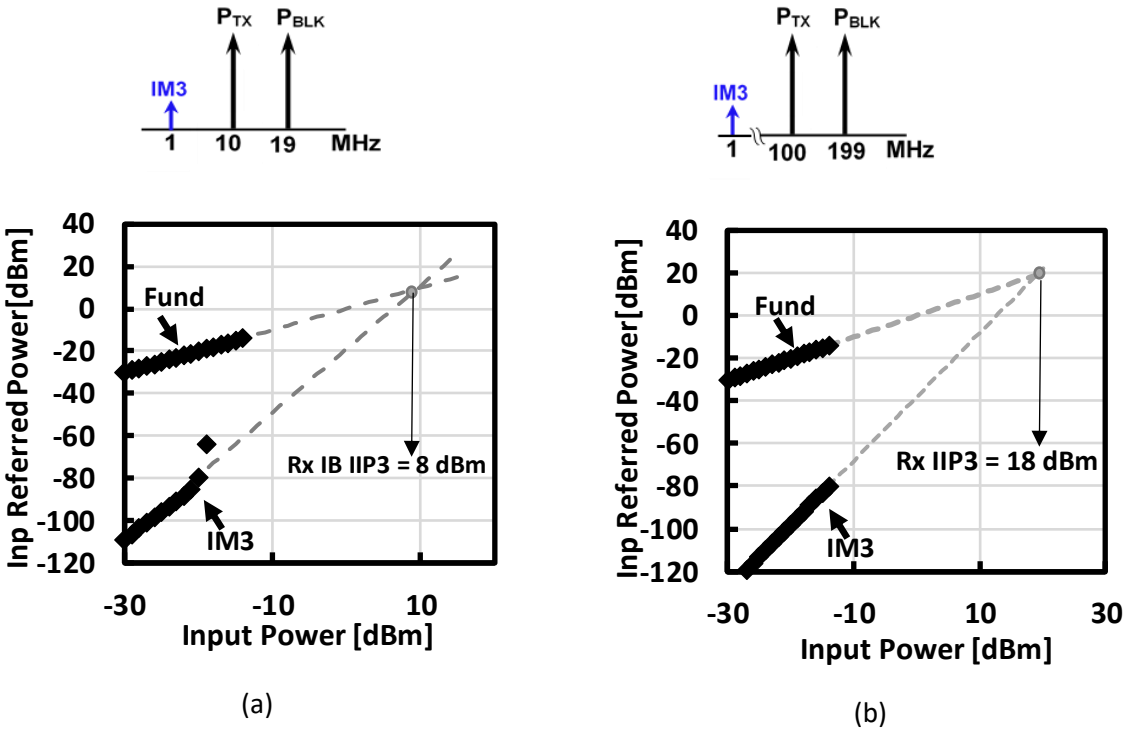


Fig. 4. 17 (a) Receiver in-band IIP3; (b)Receiver out-of-band IIP3

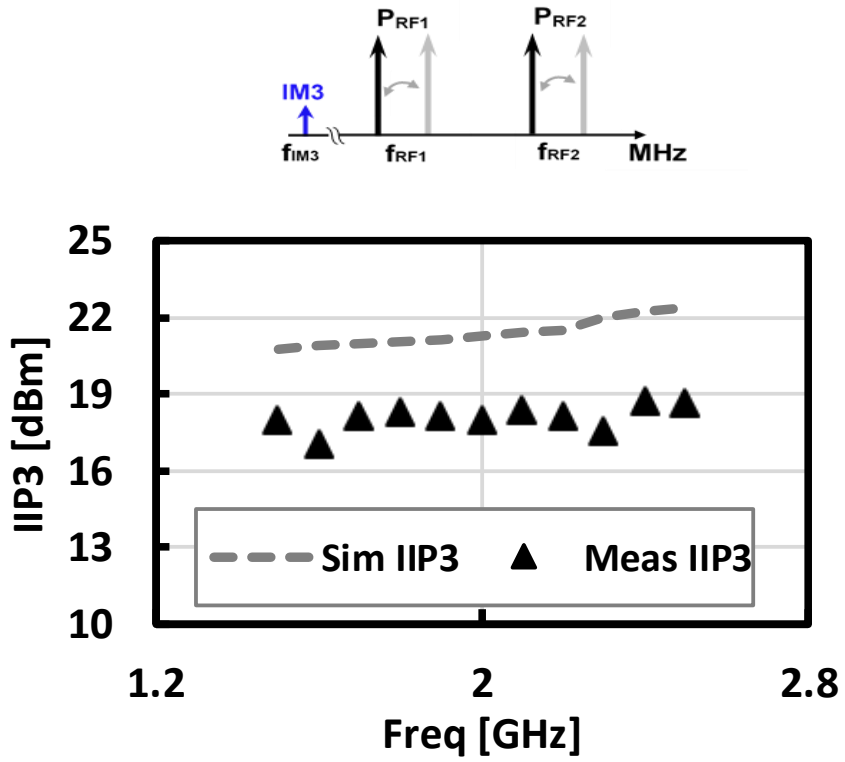


Fig. 4. 18 OOB IIP3 of the receiver as a function of input frequency

4.8.3 Receiver with Passive Canceller

The system measurement with the canceller enabled is carried out to validate the roles and importance of SI cancellation in a receiver. The receiver NF when the canceller is fully enabled is shown in Fig. 4.19 as function of SI phase shift. Turning on the canceller, degrades the receiver NF by 0.4 to 0.8 dB. To demonstrate the cancellation of the self-interference at the receiver input, the system is set up using two Planar Inverted-F antenna (PIFA) pair designed in [7] operating around 2.3 GHz, with a -25 dB coupling between the TX and the RX antennas and having a group delay of 2.8ns.

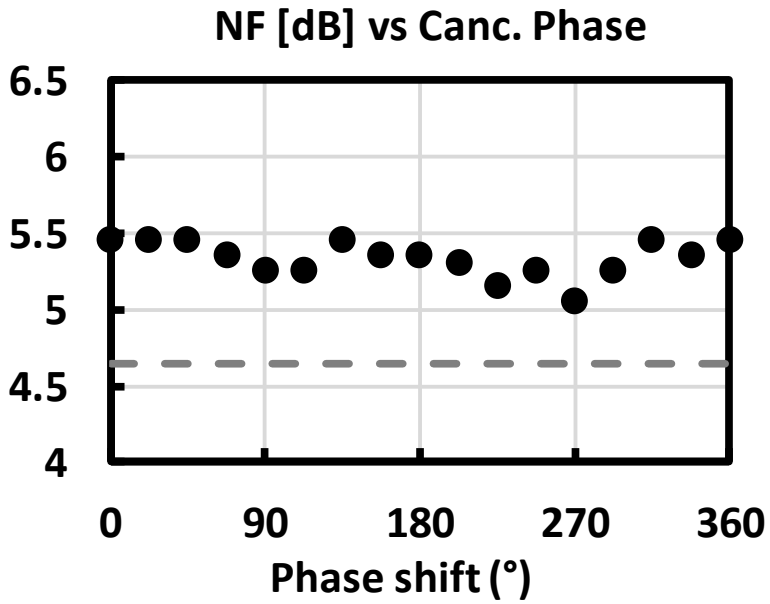
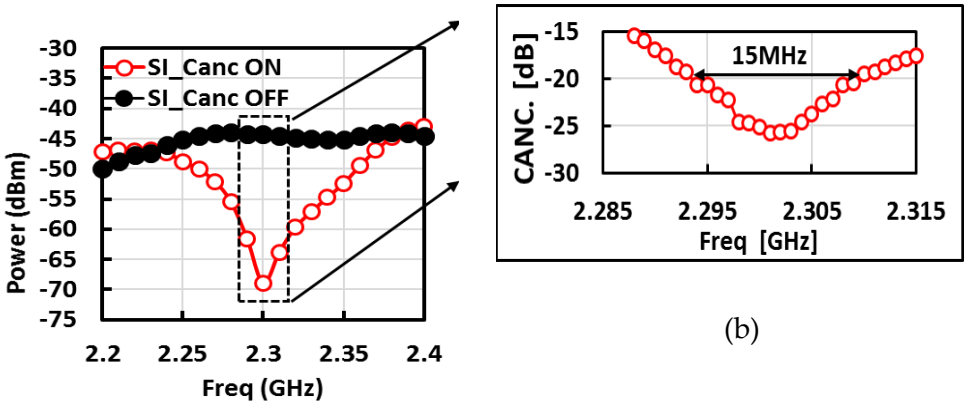


Fig. 4. 19 Receiver noise figure with canceller enabled at maximum gain versus SI phase.

A relative SI cancellation of more than 20 dB is achieved across 15 MHz bandwidth as shown in Fig. 4.20, when the measurement is carried out using CW signal. On the other hand, cancellation bandwidth is generally limited by the frequency selectivity in the leakage path. In addition, a 5 MHz BW WCDMA is transmitted from the Rohde & Schwarz SMU 200A Vector Signal Generator through one of the antennas. The

modulated SI from the TX antenna appearing at the RX input with 25 dB antenna isolation, is cancelled when the canceller is turned on, and more than 25 dB of cancellation is measured across the entire 5 MHz channel BW as shown in Fig. 4. 21..



(a) (b)

Fig. 4. 20 Cancellation bandwidth with a pair of PIFA(Planar Inverted-F antenna) (a) SI power with and without canceller enabled; (b) relative SI cancellation in dB

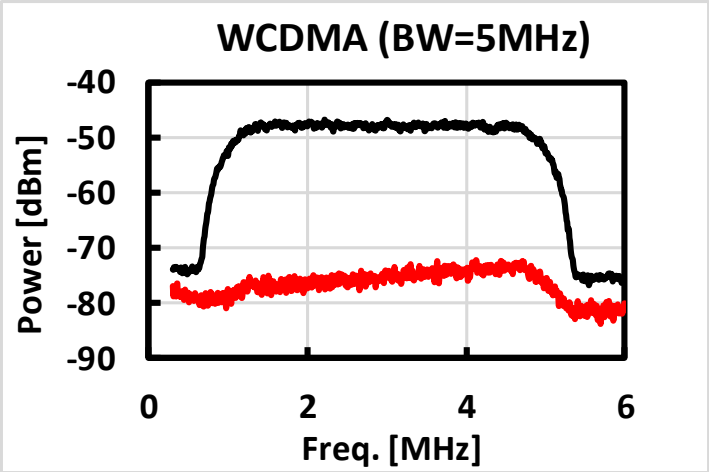


Fig. 4. 21 SI cancellation with WCDMA signal

Additional measurements are made to corroborate SI cancellation. Enabling the canceller, the receiver gain compression is pushed above 0 dBm for OOB and -5 dBm for IB SI from -15 dB IB without the canceller enabled as shown in Fig. 4.22. This measurement is carried out with two tones. For the IB, the two tones, RX signal and

the SI are placed at 1 MHz and 10 MHz respectively. With canceller enabled with 20 dB of SI cancellation, the RX signal is increased until compression observed at around -5 dBm. For the OOB, the RX signal and SI placed at 1 MHz and 100 MHz respectively.

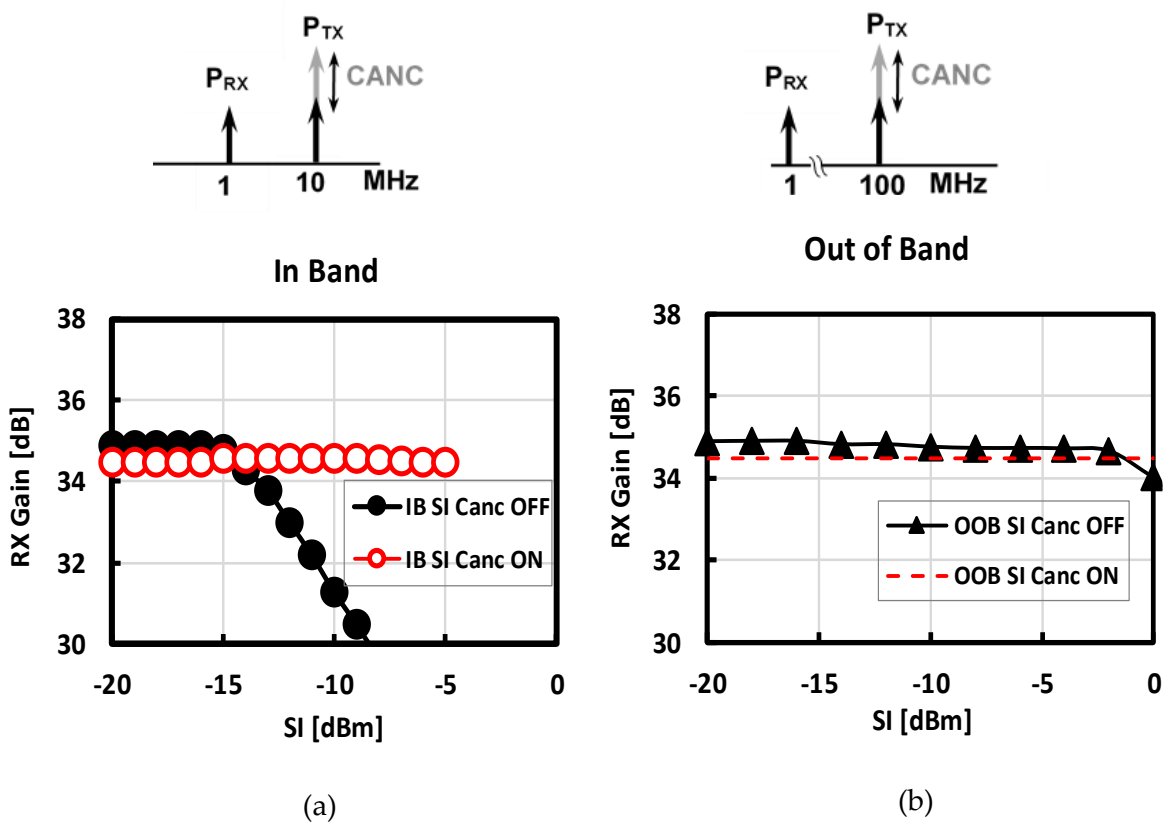


Fig. 4. 22 Gain compression versus SI power with canceller enabled and disabled (a) in-band; (b) Out-of-band

As earlier exemplified from the system analysis that SI cancellation improves the RX IIP3, the effective IIP3 due to inter-modulation between a CW blocker and the SI is measured and reported in Fig. 4.23 a) and b) versus cancellation. The effective IIP3 is illustrated for both half frequency duplexing ($IIP3_{HDF}$) and full frequency duplexing ($IIP3_{DF}$). Placing the blocker half-way between SI and the receive frequency, the IM3 falls in the RX band and therefore, should decrease linearly with the cancellation. Hence, the effective $IIP3_{HDF}$ improves by ½ dB for every dB of cancellation. The effective OOB IIP3 improves as expected up to 20 dB cancellation before saturating at 28 dBm due to canceller nonlinearities as shown in Fig. 4.23 (a). Also, placing the

blocker symmetric to the RX band with respect to SI, IM3 should decrease with the square of cancellation, therefore, improving the effective $IIP3_{DF}$ by 1 dB for every dB of cancellation. The same applies for cross-modulation between a modulated SI and an adjacent-channel CW blocker (triple-beat). The Measured results as illustrated in Fig. 4.23 (b), shows that IIP3 improves as expected up to 8 dB cancellation, saturating at 25 dBm due to canceller nonlinearities.

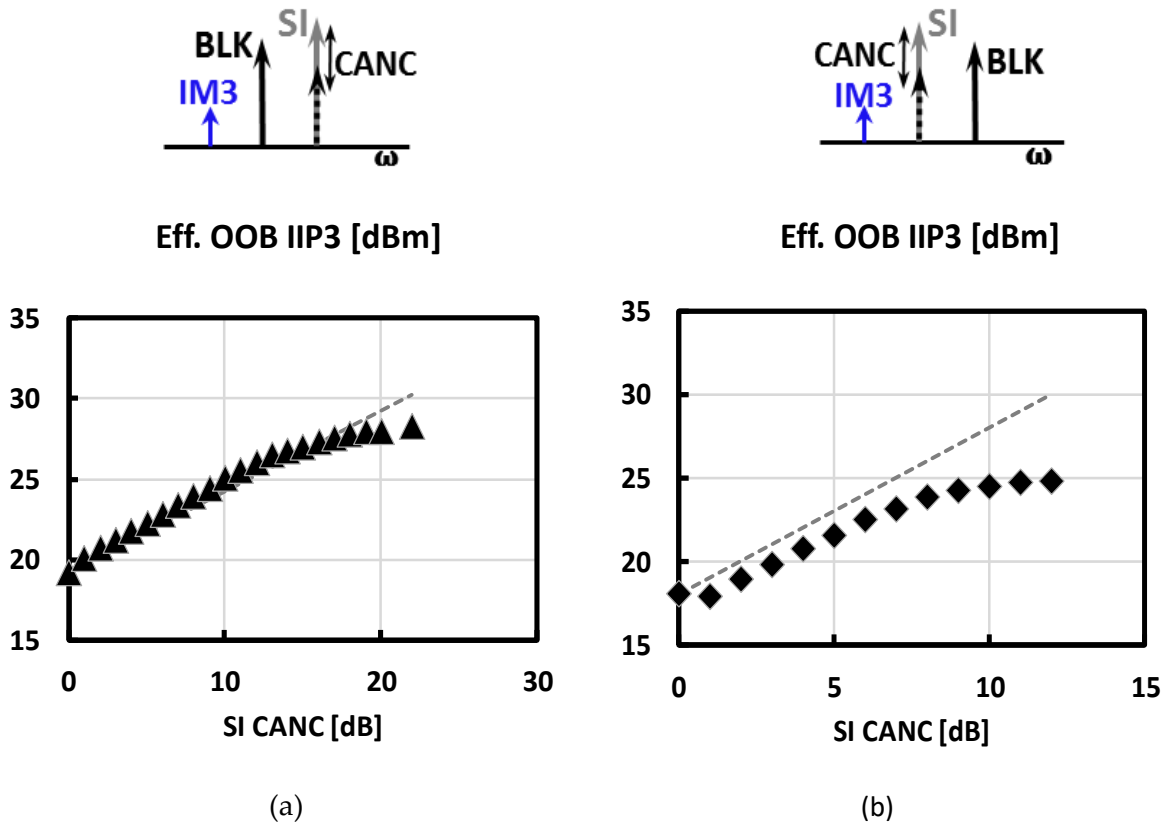


Fig. 4. 23 Effective OOB IIP3 in (a) half duplex frequency; (b) full duplex frequency as a function of self-interference power

The effective receiver IIP3 for IB SI is plotted in Fig. 4.24. The IIP3 improves from 8 dBm when the canceller is disabled to 25 dBm for 16 dB of cancellation. Beyond this, the effective IB IIP3 is limited by the canceller. Noted that the canceller distortion is almost independent of the frequency of blocker and SI. As a result, contrary to other cancellers, such as N-path, the maximum effective IIP3 is the same for IB and OOB SI.

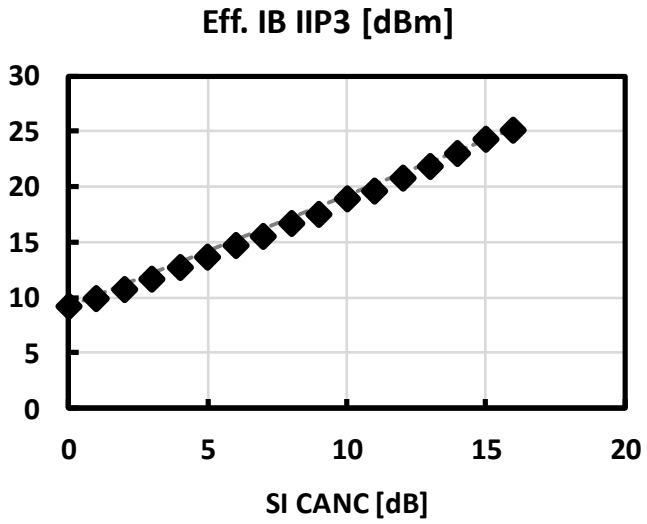


Fig. 4. 24 Effective in-band IIP3 vs. of self-interference power

4.9 Performance Summary and Sate of the Art

A comparison with the state of the art self-interference cancellation techniques is given in Table II. Compared with the active cancellers in [8], [9] and [10], the power dissipation is smaller, the NF is equal or better, effective OOB IIP3 is similar and the effective IIP3 for FD mode is much better. On the other hand, compared with the other passive SIC [11] the maximum TX leakage manageable with 360° phase control over broad frequency is much improved. Finally, the active chip area is the smallest.

Table 4. 2 PERFORMANCE SUMMARY WITH THE STATE-OF-THE-ART

	This work	**[8] JSSC'14**	**[10] ISSCC'15**	**[9] ISSCC'15**	**[11] JSSC'15**
FDD / FD	FD/FDD	FDD	FD/FDD	FD	FDD
CMOS Tech. nm	28	65	65	65	40
Frequency GHz	1-3	0.5-1.5	0.8-1.4	0.15-3.5	2.1-2.2
NF w/o canc dB	4-5.4	4.2-5.6	4.8-5.8	6.3	5*
NF w/ Canc dB	4.8-6.2	5-6.4	5.3-7	10.3-12.3	5*
IIP3 OOB dBm	18	12	17	N/A	3*
Eff. IIP3 OOB dBm	25 / 29	33	27	N/A	N/A
IIP3 IB dBm	8	N/A	-22	16.2	3
Eff. IIP3 IB dBm	25	N/A	2	19	N/A
SI cancellation dB	>20 on 15MHz #	30	>20 on 25MHz	27dB	>20 on 5MHz ^
Max rms TX Leak. dBm	-5	-1	-11	1.5	-23
Power mW	25	83 RX 72 canc	69 RX 91/path	23-56	10 LNA only
Area mm²	0.5 ‡	1.2 ‡	4.8	2	2.1

2.8ns group delay * with 1.5-2dB duplexer loss ^ 50° phase tuning ‡ active area w/o pads

4.10 Design Improvements

Several design improvements can be made to the canceller to increase the effective IIP3. The distortion from the canceller prevented achieving the simulated effective IIP3. Simulations indicate that canceller linearity is limited by its inductance to ground as shown in Fig. 4.25. In fact, the large SI injected in the canceller ground modulates the switches on-resistance leading to distortion. From simulations, it is observed that shorting together the canceller ground and receiver ground, the effective IIP3 reaches 35dBm for 20dB cancellation as shown in Fig. 4.26. To further corroborate this claim, Fig. 4.27 shows the simulated effective IIP3 for the half frequency duplex and Full frequency duplex as a function of the bonding wire inductance, achieving 40 dBm and 35 dBm respectively for an ideal ground. The smaller the inductance, the much improved the effective IIP3 would be.

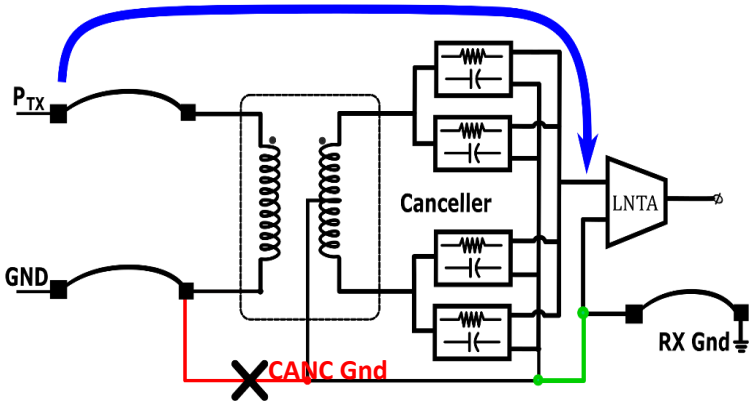


Fig. 4. 25 Effect of canceller ground due to bondwire connection

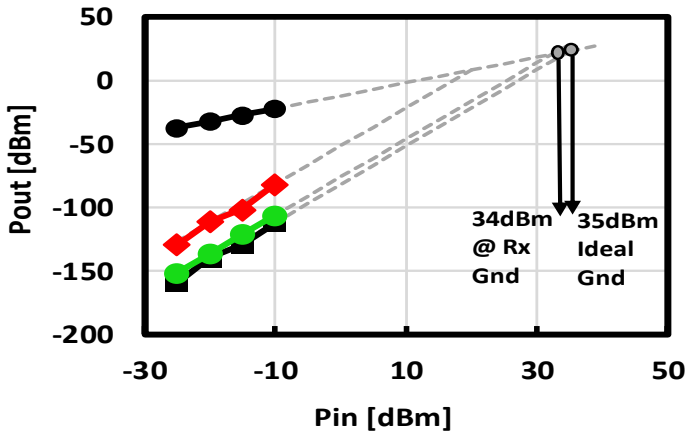


Fig. 4. 26 Effective RX OOB IIP3 with bond wire inductance and with improved grounding scheme

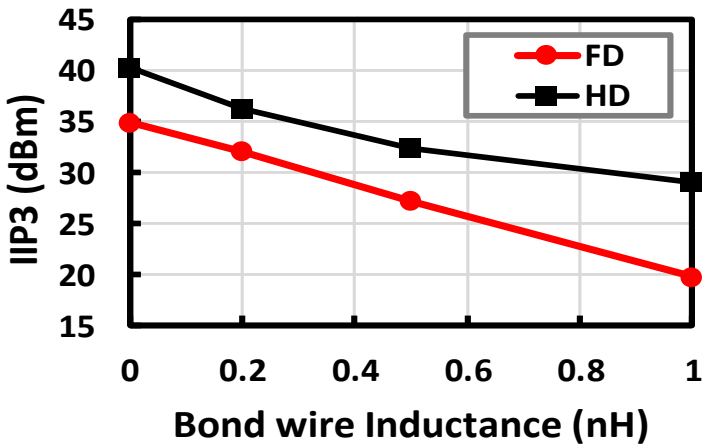


Fig. 4. 27 Effective IIP3 vs ground bondwire for HD and FD frequencies

4.11 Conclusions

This chapter demonstrates a dual antenna system with a frequency-flat passive self-interference canceller for FDD and FD applications integrated in 28 nm CMOS Technology. For 25 dB isolation, TX power level up to 20 dBm is tolerated by the SI canceller. Up to 25 dBm effective IB IIP3 and 25-28 dBm effective OOB IIP3 have been demonstrated when the canceller is enabled. Linearity and cancellation accuracy are limited by the canceller and specifically by its ground inductance. Simulation shows that in the same conditions connecting the canceller ground to the receiver ground the effective IIP3 reaches 35 dBm and the vector constellation of the canceller improves significantly.

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Chapter 5

Analysis of Second-Order Intermodulation Distortion Cancellation in a CG-CS LNA

A broadband, inductor-less noise-cancelling low-noise transconductance amplifier in a direct conversion receiver is presented. The proposed design is suitable for TV White-Space (TVWS) applications. The LNA has a single-ended input to differential output, eliminating the need for a preceding external balun. The LNA utilizes a common gate common source (CG-CS) architecture for simultaneous noise and second order-distortion cancellation of the CG branch. The use of complementary NMOS and PMOS intrinsically cancels the even order distortion of the CS. A control loop algorithm is proposed to optimize the LNA IIP2 during process corners and temperature variation and it achieves a value of more than 54 dBm. The receiver has a noise NF of about 3.5 dB and a good input matching with S_{11} less than -20 dB from 100 MHz to 1GHz.

5.1 Introduction

In wireless receivers the direct conversion architecture has become popular due to the high level of integration. Conventional radio architectures have off-chip fixed-frequency external pre-selection surface acoustic-wave (SAW) filters that filter out the out-of-band interferers. SAW filters relax the integrated receiver linearity requirements but cannot be easily tuned over multiple frequency bands. In a broadband receiver the issue of high linearity requirement is a major bottleneck in order to maintain acceptable signal sensitivity. For instance, a TVWS radio operates from 54 MHz to 862 MHz and the receiver must be tolerant to in-band interferers of up to -8 dBm [1]. Interferers generate both second-order intermodulation (IM2) and third-order intermodulation (IM3) products falling in-band, which may degrade the receiver Signal-to-Noise Ratio (SNR) if the IM2 and IM3 products are not well below the receiver noise floor. In broadband receivers second-order intermodulation is a more challenging problem than in narrow-band receivers. This is due to an additional second-order intermodulation mechanism that does not occur in narrow-band receivers. In fact, if two interferers with frequencies f_1 and f_2 appear at the input of an even order nonlinear block, an IM2 product is generated at frequency $f_1 \pm f_2$, which may fall within the signal band in broadband receivers. Hence, IM2 distortion may occur both in the low-noise amplifier (LNA) and in the mixer. In order to ensure the second-order distortion is below the noise floor, balanced topologies are always preferred. This however demands for an external balun that increases the system cost and can limit the bandwidth. As a result, a single-ended input LNA with high IIP2 is highly desirable. Furthermore, the conventional IM2 mechanism poses also greater concerns in a broadband receiver. In this case an IM2 product at frequency $f_1 - f_2$ is generated at RF and leaks to the baseband output due to mixer mismatches. In narrow-band receivers the LNA is typically ac-coupled through a large capacitor to the mixer and the low-frequency IM2 beat component at $f_1 - f_2$ generated in the LNA is filtered out. Hence, the dominant IM2 source is usually the down-conversion mixer.

However, in a broadband receiver, where the minimum signal frequency can be quite low (54 MHz in TVWS) a very large coupling capacitor would be needed, causing a large parasitic capacitance at the LNA output. This is turns lowers the driving impedance of the baseband TIA due to switched-capacitor effect of the mixer, degrading the receiver noise. For these reasons, direct dc-coupling of the LNA to the mixer is preferred. As a result, any low-frequency IM2 generated by the LNA is not blocked by the ac-coupling capacitor and can degrade the receiver IIP2. To mitigate this effect, it is important to generate a balanced differential signal prior to the mixer. In fact, it can be shown that a double-balanced mixer leads to higher IIP2 compared with a single-balanced mixer. It must be pointed out that while the first mechanism described in this section is of concern only when two large interferers are present at the receiver input with the right frequencies f_1 and f_2 such that f_1-f_2 or f_1+f_2 equals the desired channel frequency (a rather occasional event), in the case of the latter mechanism, any large modulated blocker within the wide input spectrum can cause in-band IM2. The above arguments motivate the need for a LNA with single-ended input, balanced differential output and high IIP2. In order to achieve broad bandwidth and high linearity, the current-mode receiver has been the most popular solution. [2]. Most research efforts in IIP2 improvement have been dedicated to down-conversion mixer. In this work, we analyse the importance of IIP2 and its improvement in a noise cancelling wideband LNTA.

5.2 Adjacent Channel Intermodulation in White Space Radios

The transition to digital technology has increased the amount of TV frequencies which are not being used in given location at a given time and this gives rise to the name TV white spaces (TVWS). The TV spectrum is divided into different channels; 2, 5-6, 7-13, 14-36, and 38-51 [3]. Since the RX should be wide as possible, high- power interfering signals could be received in this band and the RX should be able to efficiently

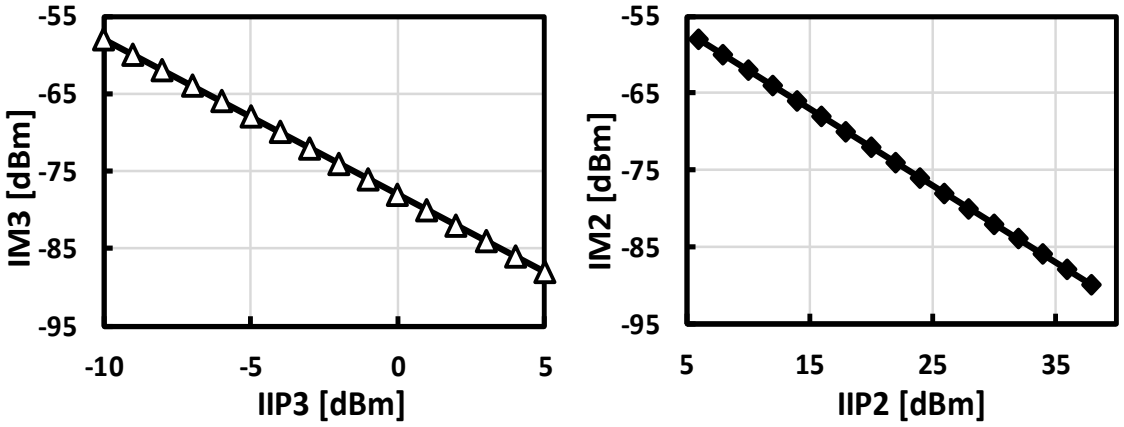
demodulate the desired signal in the presence of the high-power interfering signals within the white space band, therefore, requiring a highly linear receiver.

In USA for instance, the tolerable TX power in the TVWS can be as high as 20 -30 dBm for 6 MHz channel BW [3]. Since TX signal has alongside thermal noise, phase noise, and nonlinear distortions falling outside the TX signal bandwidth, the adjacent channel emissions must not be greater than 78.2 dBc [3]. Table I gives some example of available white space channels with corresponding co-channel and adjacent channel interference power levels.

Table 5. 1 WHITE SPACE CHANNELS WITH CO-CHANNEL AND ADJACENT CHANNEL INTERFERENCE

White space channel	Co-channel dBm	ACS (low) dBm	ACS (high) dBm
24	-87	-105	-62
26		-62	-26
32	-108		
41		-99	-61
43		-61	-55
47		-76	-26

The effect of the adjacent channel intermodulation in a nonlinear device linearity requirement is quantified by the IIP3 ($= \frac{3P_{ACS}-IM3}{2}$) and the IIP2 ($= 2P_{ACS} - IM3$). In the worst case with high interference power of -26 dBm of channel 26 for instance, the IM3 and IM2 level requirements as a function of IIP3 and IIP2 respectively is shown in Fig. 5.1. For IIP3 of 5 dBm, the IM3 level of –88 dBm must be ensured to keep a quality demodulated receive signal with a corresponding level of 36 dBm for the IIP2 requirement.



(a) (b)

Fig. 5. 1 Adjacent channel distortion power: (a) IM3 versus RX IIP3; (b) IM2 versus RX IIP2 with interferer power level of -26 dBm (channel 26) for 6 MHz channel BW

5.3 State of the Art

The noise of the LNA in a receiver is a critical factor that determines the receiver overall noise performance. Several wideband LNAs adopt a noise cancelling topology. To improve the LNA IIP2, several second order distortion cancellation techniques have been proposed [4], [5]-[13][9]. A common noise-cancelling LNA topology is based on a common-gate (CG) and common-source (CS) stage [11], [12]. The CG allows to fulfil the input matching condition over a wide bandwidth and the CS allows achieving low NF. In [11], a wideband LNA is designed adopting a combination of CG and CS stages to produce a balanced output signal with low noise and distortion. A resistively loaded stage was used to achieve the balanced output in voltage mode, which results in early output compression. With a careful choice of the bias point, a NF of around 3.5 dB and moderate IIP2 (between 20 to 25 dBm) are achieved and these values are basically dominated by the noise and distortion of the CS stage. However, with process corners and temperature variations the optimal bias conditions will change in a rather unpredictable way, highly degrading the IIP2. The noise-canceling LNA reported in [12], specifically designed for digital TV tuners operating within the frequency range of 54 MHz to 880 MHz, features a single- ended input and a single-

ended output and is also based on CG and CS stages. However, the cancellation of the CS stage second-order distortion is approached using complementary NMOS and PMOS structures. Since the NMOS and PMOS provide in-phase and out of phase second order distortions at their output drains, combining these signals eventually cancels out the second- order distortion. However, the poor matching between the complementary CS PMOS and NMOS devices will highly degrade the LNA IIP2 across process and temperature variations.

5.4 Simultaneous Noise and Distortion Cancellation in Proposed Solution

A single-ended input, balanced differential output noise-cancelling LNA has been recently proposed in [14] and is shown in Fig. 5. 2.

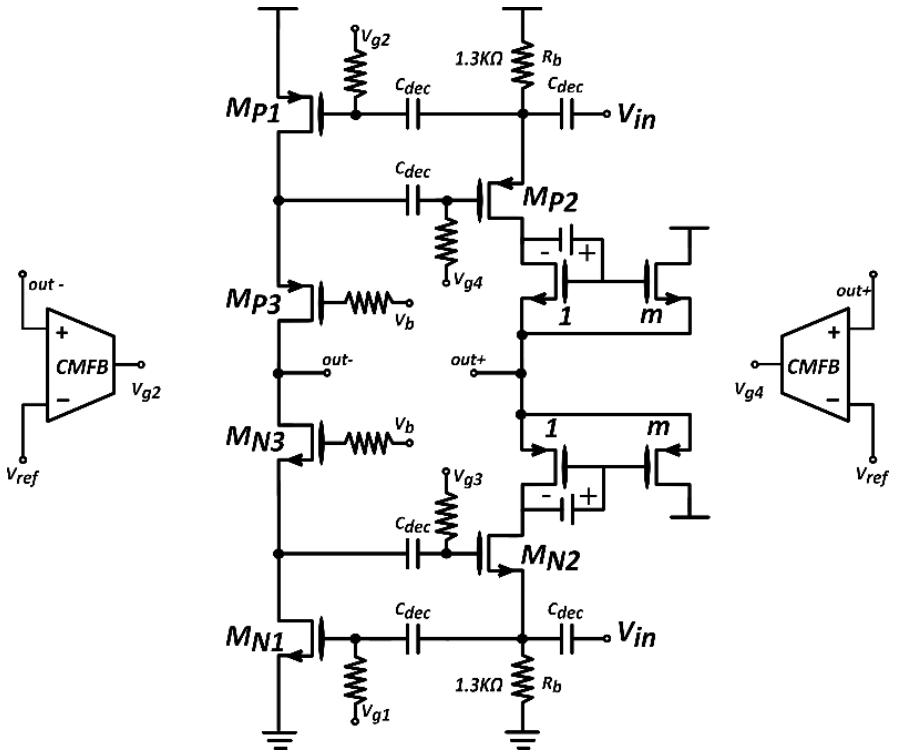


Fig. 5. 2 Schematic of the proposed LNTA

It is a single-ended to differential design with a balanced output current, which further simplifies the design of the mixer and baseband stages. This design, which is suitable for a TVWS, achieves a broadband input matching from 100 MHz to 1 GHz and a low

NF less than 2.6 dB. A detailed discussion of the LNA design for low noise can be found in [14]. A second order distortion analysis and the proposed concept of background calibration will be explained in this write up.

5.4.1 Impedance Matching and Output Balancing Analysis

In conventional CG LNA, input matching is realized when the CG transconductance is set as : $g_m = \frac{1}{R_s}$, where R_s is the source impedance. To produce a g_m of 20 mS using the CG transistor only, the current drawn will be around 1 mA. The current drawn can further be lowered to about half of that using a complementary pair. In the approach of [14], as shown in Fig. 5.2, using a complementary NMOS and PMOS, the current is reduced even further using a local feedback through the cascode stage of the CS, as initially proposed in [15]. At the nodes between the drain of the complementary CS and the source of its cascode, the input signal, V_{in} sees a voltage gain of $-G = \frac{g_{m,MN1}+g_{m,MP1}}{g_{m,MN3}+g_{m,MP3}}$. The complementary CG device required for input matching, sees its transconductance boosted by a factor of 1+ G. Therefore, the input impedance is lowered by the same factor and is calculated as:

$$R_s = \frac{1}{(g_{m,MN2}+g_{m,MP2})(1+G)}, \quad (1)$$

where $(g_{m,MN2} + g_{m,MP2}) = g_{m-CG}$. Hence, the bias current required to achieve impedance matching has been further reduced by 1+G, compared to the conventional simple CG transistor. This has the important consequence that it becomes possible to bias MN2 and MP2 with large on-chip resistors with negligible noise penalty and saving two external choke inductors. With the matching condition set, the voltage sensing CS stage transconductance should be set to a much higher value to lower the LNA noise. This however causes the output currents of the CG and CS stages to be of different magnitudes. As pointed out in [14], the unbalanced LNA output currents would further require additional baseband stage for signal recombination resulting in larger power consumption or higher noise. This will also require two different single

balanced mixers to down-convert the signal, eventually producing a lower RX IIP2. To address this issue, the LNA output currents are balanced using a current multiplier following the CG stages. The current multiplication factor β, 1+m in Fig. 5.2, is set according to ratio between the transconductance value of the CS stage and 1/Rs.

5.4.2 Distortion Cancelling Analysis

As analysed in [14], not only the noise of the CG device is cancelled but also its in-band IM2. This is depicted in Fig. 5.3.

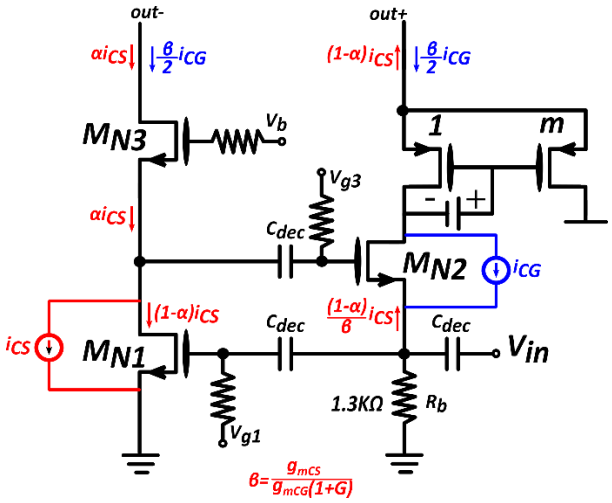


Fig. 5. 3 IM2 propagation in the proposed LNTA

As the distortion of the CG is cancelled through the CG-CS noise cancelling concept, the IIP2 linearity performance of the LNA depends on the distortion of the CS stage. In the proposed LNA, a complementary architecture is used in the LNA design to help improve the overall IIP2. The IM2 generated by MN1 is modelled as a current source (just like the equation of (3)) as $i'_{CS} = g'_{m-MN1}V_{in}^2$ where g'_{m-MN1} is the second-order nonlinear transconductance of MN1. Due to the loop formed by MN1, MN2 and MN3, a low impedance is observed at the drain of MN1. Hence, only a fraction of i'_{CS}, given as $\alpha i'_{CS}$, reaches the inverting output. The remainder, $(1-)\alpha i'_{CS}$, is mirrored to the non-inverting output with a gain of $1/(g_{mCS}R_S)$ and is then amplified by $\beta(= g_{mCS}R_S)$.

As a result, the differential output is simply i'_{CS}. The same considerations also apply to MP1.

The complementary topology of the LNTA can be exploited to cancel out the IM2 thanks to the opposite polarity of the two second-order transconductances of MN1 and MP1. This is typically achieved by biasing the two transistors around a sweet spot to ensure $g'_{m-MN1} = g'_{m-MP1}$, resulting in a sharp IIP2 degradation across process corners, voltage and temperature (PVT) variations [5],[11]. In this work, we have analysed the LNA variation to PVT and proposed a background calibration technique to ensure high IIP2 across PVT.

5.5 IIP2 improvement through Background Calibration.

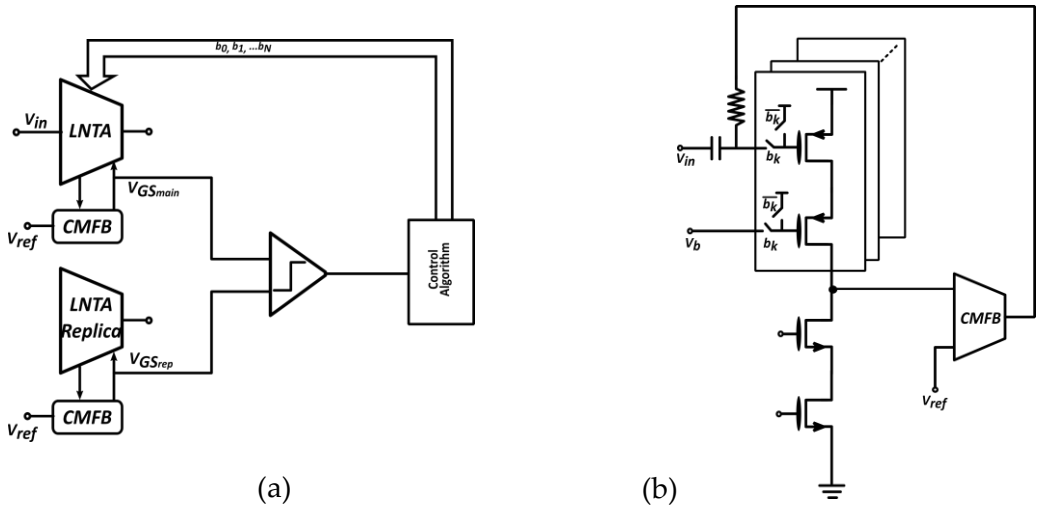


Fig. 5. 4 LNTA IIP2 automatic control loop: (a) Block diagram of the control loop; (b) detailed schematic of the CS branch with array of the PMOS device

The proposed LNA IIP2 background calibration concept is shown in Fig. 5.4. The NMOS transistor gate bias voltage is set through a current mirror, while the PMOS device is sliced and the effective size of MP1 is set by the automatic control loop. The gate bias of MP1 (V_{GMP1}) is set by the common-mode feedback (CMFB). Intrinsically, the CMFB ensures the drain current drawn by the NMOS equals the drain current from the PMOS. When a large RF signal is applied at the LNTA input, V_{GMP1} varies in

order to keep the average current of MP1 and MN1 the same. If $g'_{m-MN1} = -g'_{m-MP1}$, V_{GMP1} stays constant even when a large input signal is applied. This condition coincides with the IIP2 optimum. Therefore, monitoring the variations of V_{GMP1} allows to automatically detect the optimum IIP2 condition. In order to detect the variations in the gate bias of MP1, V_{GMP1} is compared with respect to the gate bias of the replica circuit, where no signal is applied. When a higher V_{GMP1} is observed compared to the replica gate bias, the comparator gives a high bit of 1. The control algorithm thus, generates a code-word that controls the array of the PMOS by reducing the width size. In the other scenario, when V_{GMP1} is lower, the comparators give a lower bit and the control algorithm increases the width of MP1. Note that the LNTA replica circuit is turned on only when calibration is required, to ensure and guarantee minimal power consumption overhead. This concept has been verified through simulations and the results are illustrated in the next section.

5.6 Simulation Results

The LNTA of [14] designed in 40 nm CMOS technology has been optimized for IIP2 improvement. The LNTA performance has been verified with direct-conversion mixer driven by 25 % duty cycle LO and TIA (exemplified in chapter 3) but redesigned for a 10 MHz channel bandwidth (required for a TVWS radios) with a unity gain bandwidth of 1.5 GHz, thus, completing a receiver chain. The LNTA CG branch draws a current of 260 μA and a current of 1.45 mA in the CS branch while, the TIA draws a current of 3 mA. The total signal path power dissipation is 13.8 mW from a 1.8 V voltage supply.

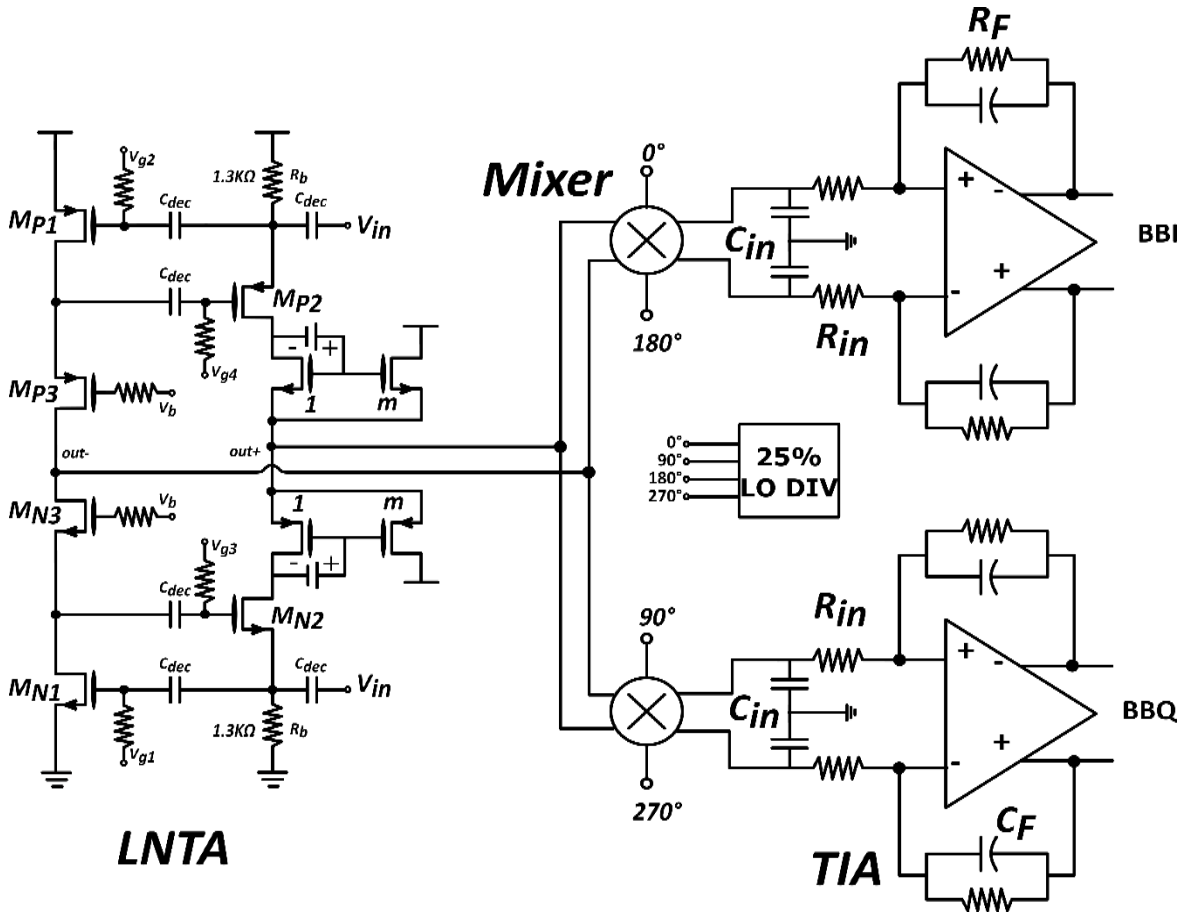
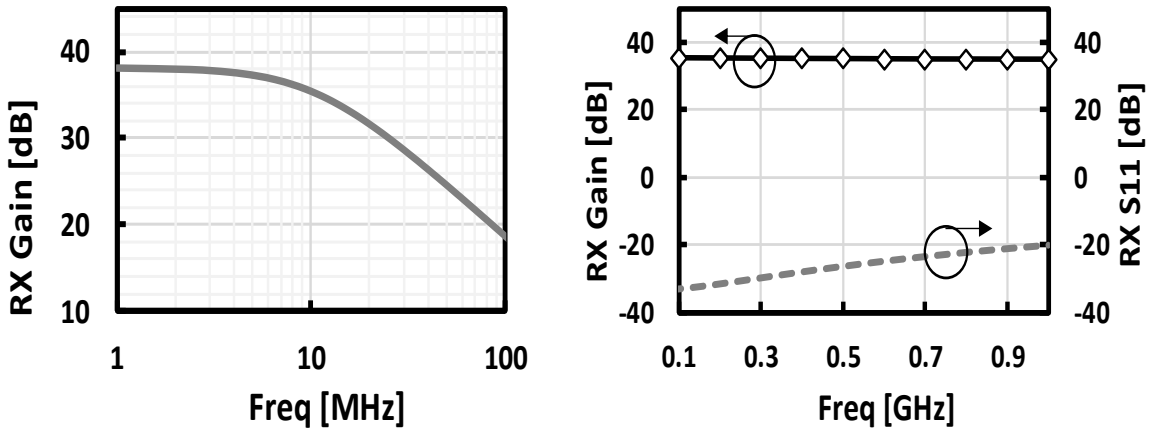


Fig. 5. 5 Receiver architecture with LNTA directly coupled to the mixer

The simulated direct-conversion receiver gain and the S11 plots are shown in Fig. 5.6. The receiver has an in-band gain of 35 dB with -3 dB bandwidth at 10 MHz as shown in Fig. 5.6a. Also shown in Fig. 5.6b is the gain over RF frequency between 100 MHz to 1 GHz with almost a flat gain on average of 35 dB with good input matching where S_{11} is well below -20 dB between the range of 100 MHz to 1 GHz. Reported also in Fig. 5.7 is the LNA and RX NF with values between 2.6 to 2.7 dB for the LNA and 3.5 to 3.9 dB for the RX where the RX noise is observed at 4 MHz in-band when sweeping the LO over a frequency range of 100 MHz to 1 GHz.



(a) (b)

Fig. 5. 6 (a) Receiver downconversion gain vs output frequency; (b) RX downconversion gain and S11 as function of the input frequency

For the linearity tests, the receiver IIP3 is simulated with two tones placed 6 MHz and 10MHz offset the LO frequency at 1 GHz. The Rx IIP3 is 1 dBm as the same for the LNTA as shown in Fig. 5.9. Also shown in Fig. 5.8 is the in-band gain compression due to an OOB blocker placed at 100 MHz offset from the carrier frequency. The gain compression is -4 dBm for the whole receiver and -3 dBm for the LNTA.

For the IIP2 test of the LNA, a two-tone test is carried out with one tone fixed at 1 GHz and the other tone is swept in frequency with an offset of 100 MHz to 900 MHz, where the intermodulation products falls in band. An IIP2 of more than 55 dBm (Fig. 5.10) over the entire 100 MHz to 900 MHz offset the fixed tone is achieved. This shows that the LNA is capable of cancelling the second order distortion that would be created when any interferer falls within the 0.1 – 1 GHz band of interest.

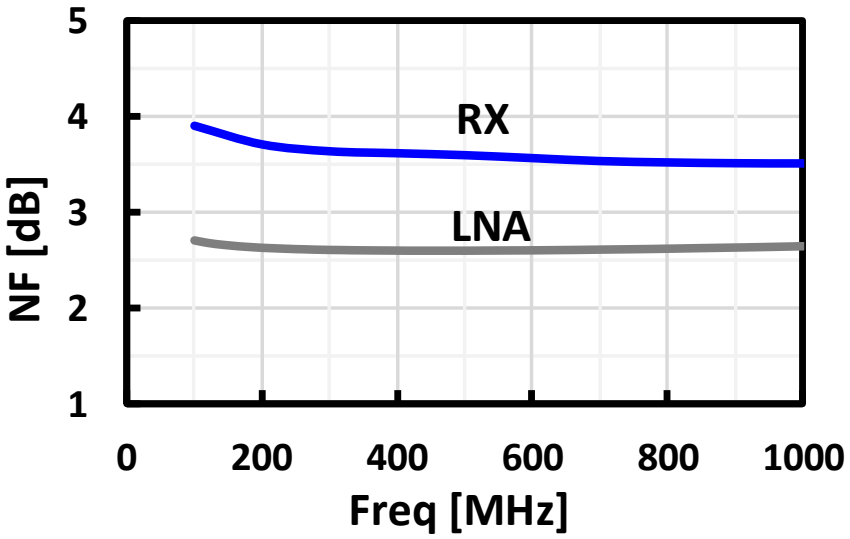


Fig. 5. 7 LNA and RX noise figure

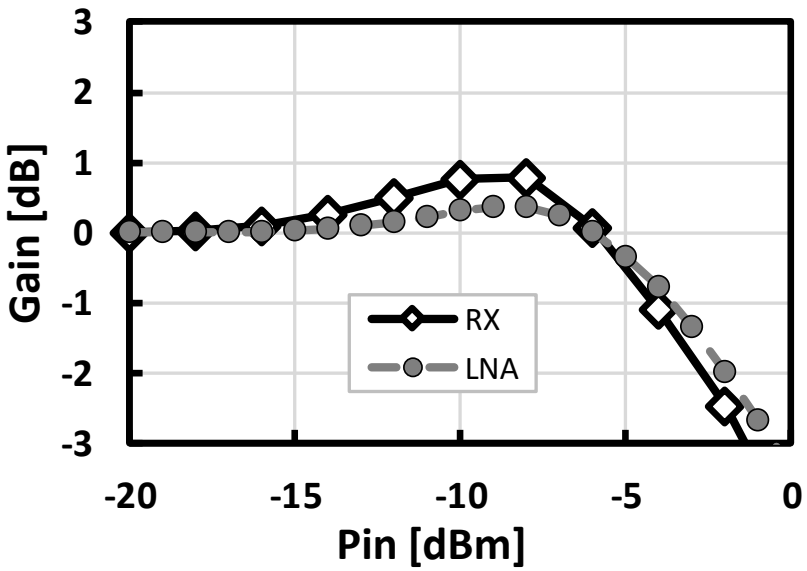


Fig. 5. 8 LNA and RX gain compression due to OOB blocker at 100 MHz offset carrier frequency

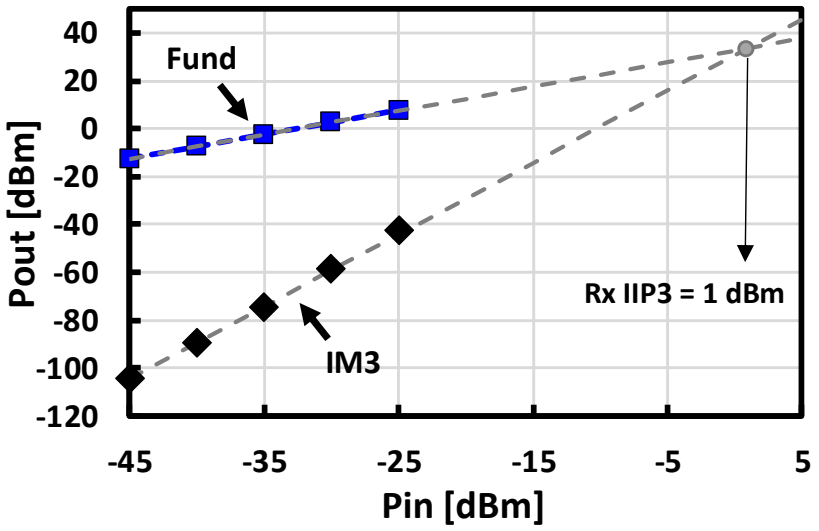


Fig. 5. 9 RX IIP3 for two 5 MHz spaced tones

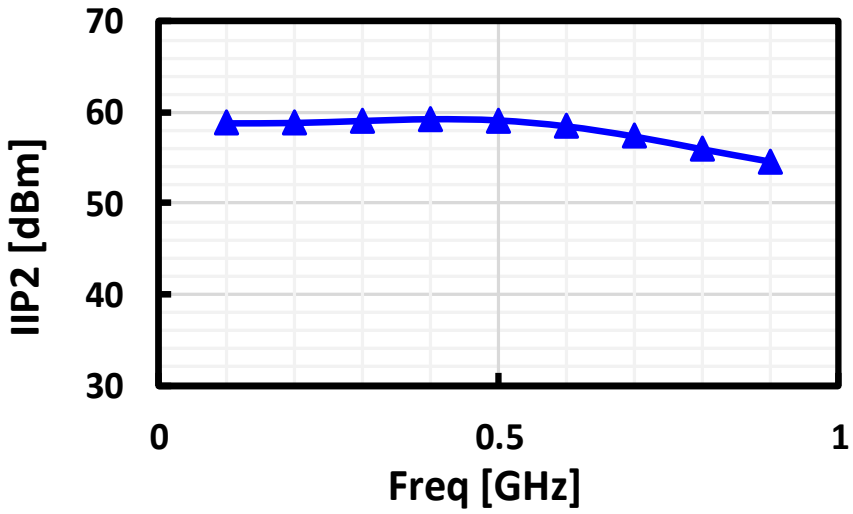


Fig. 5. 10 LNA IIP2 with blocker frequency falling between 100 MHz to 900 MHz

At higher frequency offset of the blocker, the IIP2 reduces due to parasitic capacitors resulting in the phase difference seen by the NMOS and PMOS drain source currents of the CS devices. To verify the background calibration concept, the LNA is simulated

for process corners variation before and after optimization as shown in Fig. 5.11 for an absolute temperature. In the worst case of an IIP2 of 32 dBm at FS, the IIP2 is improved with more than 24 dB to achieve a least of 54 dBm across process corners.

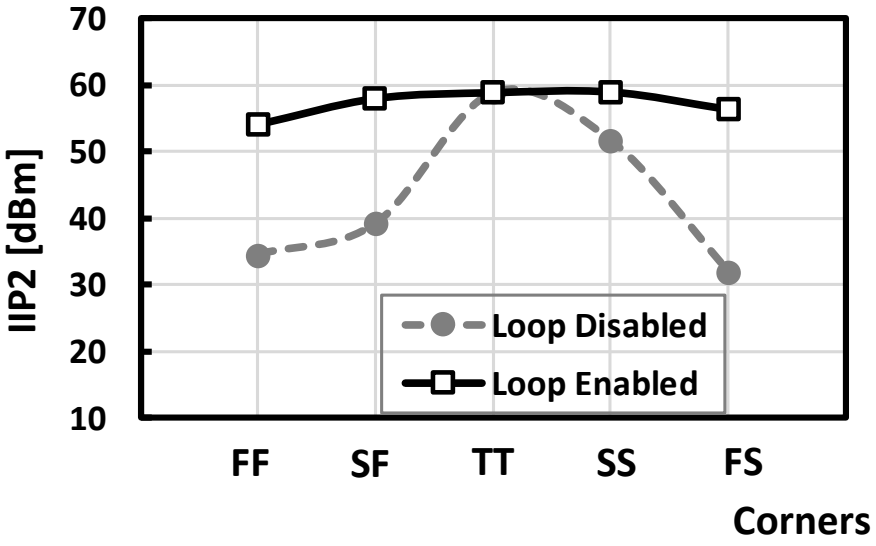


Fig. 5. 11 LNA IIP2 with and without optimization across process corners

5.7 Performance Summary

The LNTA performance in terms of IIP2 presents a bottleneck for the RX IIP2 since the IIP2 of the mixer becomes negligible due to the LNTA direct coupling. The design is compared with other solutions and summarized in Table II. However, it must be pointed out that this work only presents simulation results compared to others that are measurement results. The proposed solution has lower noise and much better IIP2 compared to [10] and [12] who also use complementary architectures to achieve higher IIP2 values. Also, the power consumption is far lower even when compared to the entire receiver chain. The IIP3 is lower and can be improved by considering design optimization similar to **Error! Reference source not found.**.

Table 5. 2 PERFORMANCE SUMMARY WITH THE STATE-OF-THE-ART

	This work	[10] JSSC '17	[12] JSSC '09	[11] JSSC '08
CMOS Tech. [nm]	40	180	180	65
Single Ended Input	Yes	No	Yes	Yes [b]
Design	LNTA/ RX	LNA	LNA	LNA
Frequency [GHz]	0.1-1	0.1-2	0.048-1.2	0.2-5.2
Supply [VDD)	1.8	2.2	2.2	1.2
Gain [dB]	35	17.5	14	13-15.6
S11	<-20	<-10	-9	<-10
NF [dB]	2.5-2.6 (LNA) 3.5-3.9	2.9-3.5[a]	2.9-3.2[a]	2.9-3.5
IIP3 [dBm]	1 (LNTA) 1	10.6-14.3[a]	2.3-3.6[a]	0-4
LNA IIP2 [dBm]	>54	39-44[a]	40-45[a]	20-22
Power [mW]	3 (LNTA) 13.8	21.3	34.8	21

[a] *maximum gain mode* [b] *single ended output*

5.8 Future Design Development

The results presented in this work are only preliminary simulation results that should be confirmed with experimental results. The calibration algorithm has only been implemented through manual optimization and needs to be further developed.

5.9 Conclusions

An inductorless wideband (0.1 to 1 GHz) noise-cancelling CG-CS LNTA implemented in a direction conversion receiver is illustrated in this work. It has been shown that noise and the IM2 distortion of the CG branch are simultaneously cancelled based on the noise cancellation concept. The complementary topology of the LNTA has been exploited to cancel out the CS branch IM2 thanks to the opposite polarity of the two second-order transconductances of the NMOS and PMOs devices. In this work, the LNA achieves an IIP2 of more than 54 dBm across process corners with the calibration concept introduced, thus, keeping the IIP2 high enough to make this solution suitable for TVWS applications. The RX consumes moderate power with noise between 3.5-3.9 dB.

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Glossary

ADCs Analog-to-Digital Converters

AGC Automatic Gain Control

BW Bandwidth

CDMA Code Division Multiple Access

CG Common-Gate

CMFB Common Mode Feedback

CMOS Complementary Metal-Oxide Semiconductor

CS Common-Source

CW Continuous Wave

DACs Digital-to-Analog Converters

DR Dynamic Range

FD Full Duplex

FDD Frequency Division Duplexing

FIR Finite Impulse Response

GSM Global System for Mobile Communications

HSPA High Speed Packet Access

I/Q In-phase / Quadrature

IB In-Band

IIP2 Input Second-Order Intercept Point

IIP3 Input Third-Order Intercept Point

IM2 Second-Order Inter-Modulation

IM3 Third-Order Inter-Modulation

IOT Internet of Things

LNA Low Noise Amplifier

LNTA Low Noise Transconductance Amplifier

LO Local Oscillator

LSB Least Significant Bit

LTE Long-Term Evolution

MIMO Multi-In-Multi-Out

MSB Most Significant Bit

NF Noise Figure

NMOS N-Channel Metal Oxide Semiconductor

OFDM Orthogonal Frequency-Division Multiplexing

OOB Out-Of-Band

OTA Operational Trans-Impedance Amplifier

PA Power Amplifier

PCB Printed Circuit Board

PIFA Planar Inverted-F Antenna

PMOS P-Channel Metal Oxide Semiconductor

PVT Process, Voltage and Temperature

QPSK Quadrature Phase Shift Keying

RF Radio Frequency

RX Receiver

SAW Surface Acoustic Wave

SI Self-Interference

SIC Self-Interference Cancellation

SNR Signal-to-Noise Ratio

TDD Time Division Duplexing

TDMA Time Division Multiple Access

TIA Trans-Impedance Amplifier

TSMC Taiwan Semiconductor Manufacturing Company

TVWS TV White Space

TX Transmitter

UMTS Universal Mobile Telecommunications System

VGA Variable Gain Amplifier

VNA Vector Network Analyzer

WCDMA Wideband Code Division Multiple Access